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Sciences

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Physics Degree Thesis

# A Low Power Front-End Amplifier for the Microstrip Sensors of the PANDA Microvertex Detector

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# Abstract

This thesis is part of the ongoing studies for the PANDA (antiProton ANnihilation at DArmstadt) Microvertex Detector (MVD) microstrip sensors readout electronics. The PANDA experiment is one of the key projects at the future Facility for Antiproton and Ion Research (FAIR), which is currently under construction at GSI, Darmstadt. It will perform precise studies of antiproton-proton annihilations and reactions of antiprotons with nucleons of heavier nuclear targets. The covered centre-of-mass energy between 1 GeV and 5 GeV allows very accurate measurements, especially in the charm quark sector, so it will be possible to explore the nature of the strong interaction and to obtain a significant progress in the understanding of the QCD spectrum and hadron structure [1]. The innermost PANDA detector is the MVD. It is made up by two different sensors: pixels and microstrips. The subject of this thesis is the design of these microstrip sensors readout system based, such as the pixel sensors, on the Time over Threshold (ToT) technique. The principles of this kind of measure will be widely discussed later, at the moment we only need to specify that this involves the design of a time-based ASIC (Application Specific Integrated Circuit). Moreover, considering that one of the main features of the PANDA experiment is that it's triggerless, it is necessary to perform time measures with accurate time resolution. This choice to extract the amplitude, and thus the energy, information through time measures allows to use a TDC (Time to Digital Converter) rather than an ADC (Analog to Digital Converter). TDCs are digital or analog circuits with a low dynamic range, so they are more suitable to be implemented with the well known CMOS technologies working with typical power supplies of  $(1.2 \div 1.5) V$ . The purpose of this thesis is thus to develop a low-power front-end amplifier optimized for time-based measures, in particular to study the feasibility of such a structure identifying the possible relative issues. The thesis has been organized as follows:

## Chapter 1

This chapter contains a more detailed introduction on the Panda experiment and a brief description of two points of its physics program: hadrons in nuclear matter and parton structure. Then there is an overview on the Panda detector structure involving the Target and the Forward Spectrometers. The core of the chapter is the description of the Microvertex Detector with particular attention paid on the microstrip sensors features and issues. In the end there is a table summarizing the key parameters of the system driving the design of the front-end electronics.

## Chapter 2

This is a theoretical chapter necessary for a better understanding of the problems encountered in the design of a front-end amplifier. The first part regards the study of the ideal cases where we use an ideal preamplifier and use a  $\delta$ -like pulse as input

signal. After that, is reported the discussion on the effects of non-idealities such as the issues due to a real amplifier or to a more realistic model of the signals coming from the detector. In the last part of the chapter is discussed the noise in front-end amplifier. The noise calculations are examined in detail both in simpler and more complicated cases in order to make it possible a comparison with the results obtained with the CAD simulations.

### **Chapter 3**

In this chapter, the ToT principle is introduced and the TDC necessary to perform accurate timing measurement is briefly described. The chapter then concentrates on the implemented front-end. The building blocks are described in detail at the schematic level and analyzed with the help of small signal analysis models.

### **Chapter 4**

In this chapter, the results of the CAD simulations are reported and the performance are discussed. The results shown focus on the study of the linearity of the ToT measures, the corner process analysis, the different behaviors due to temperature variations, the noise of the chain and the jitter of the comparator.

The main results achieved in this work and the issues that need to be addressed in the future are summarized in the conclusions.

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# Chapter 1

## The PANDA Experiment

### 1.1 Introduction

PANDA (antiProton ANnihilation at DArmstadt) is a subnuclear physics experiment involving more than 450 scientists from 17 countries that is planned to start in 2018. The experiment aim at investigating the physics of strong interaction and the hadron structure, acquiring understanding of the mechanism of hadron mass generation, quark confinement and probing the existence of glueballs and hybrids. In order to achieve these goals it will perform several measurements of antiprotons interactions with protons and nuclei in a fixed target setup. The innovation of PANDA, compared to other fixed target experiments, is due to the high luminosity ( $L \lesssim 2 \cdot 10^{32} \frac{1}{cm^2 s}$ ) and very good collimation of the incident antiproton beam which allow to have a large number of events and a more accurate statistics. An antiproton beam in the momentum range of  $1.5 GeV/c$  -  $15 GeV/c$ , provided by High Energy Storage Ring (HESR), gives access to a center of mass energy range from  $2.2 GeV/c^2$  to  $5.5 GeV/c^2$  in  $\bar{p} - p$  annihilations allowing a precise test of the Quantum Chromodynamics (QCD) between the perturbative and non perturbative regime. Figure 1.1 shows the accessible mass range of hadrons at the PANDA experiment in relation to the antiproton momenta required in the fixed target collisions.

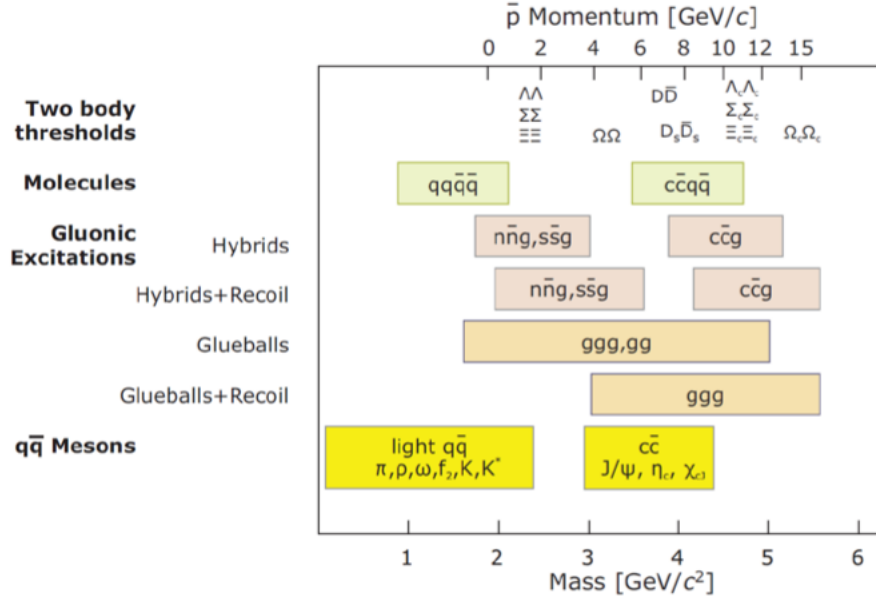


Figure 1.1: Mass range accessible at PANDA ( $2.2\text{GeV}/c^2 - 5.5\text{GeV}/c^2$ ). The upper scale indicates the corresponding antiproton momenta required in a fixed target setup.

With the accessible energy region at HESR it is possible to cover a larger range of studies compared with Low Energy Antiproton Ring facility (LEAR) of CERN (beam momentum up to  $2.2\text{GeV}/c$ ), such as:

- Investigation on the behavior of hadronic particles in nuclear matter for understanding the origin of hadron masses.
- Measurement of Generalized Parton Distributions (GPDs), transverse parton distribution functions, and electro-magnetic form factors in the time-like region in order to study the proton structure.

### 1.1.1 Hadrons in nuclear matter

PANDA foresees the possibility to study antiproton annihilations on fixed heavy nuclear targets. These reactions are ideally suited to investigate the modification of hadronic mass in nuclear matter and unravel its origin. The QCD vacuum is characterized by quark and gluon condensate, so the chiral symmetry (a symmetry of the QCD Lagrangian under which the left-handed and right-handed parts of Dirac fields transform independently) in QCD is spontaneously broken by the fact that the quarks do have mass linked to the condensate. However the light quark masses are much smaller than the hadronic scales and for this reason the chiral symmetry may be considered an approximate symmetry of the strong interactions.

A partial restoration of chiral symmetry is expected in dense nuclear matter and at high temperatures for the light quarks due to a change in the quark condensate leading to a deconfined state, thus to the formation of the Quark-Gluon Plasma. This should therefore lead to the modification of hadrons properties, like mass and width, when they are embedded in the nuclear matter. The high intensity beam, up to  $15\text{GeV}/c$  in PANDA, allows an in-medium extension of these studies towards the heavy-quark sector, especially for mesons containing open or hidden charm. Given the large contribution of the  $c$  quarks in the charmonium mass, the in-medium masses states are expected to be affected mainly by the gluon condensate. For this reason it is predictable a small shift of the in-medium mass ( $\sim 10\text{MeV}/c^2$ ) for the low lying charmonium states. The  $D$  mesons, which are made of a  $c$  quark coupled to a light antiquark, represents, together with the  $B$  mesons, a possibility to study the in-medium modifications of systems with a single light quark. Figure 1.2 shows the theoretical predictions for the drop of the  $D$  and  $D^*$  meson masses in relation to the surrounding nuclear matter density. The  $D$  mass dropping lowers the  $D\bar{D}$  threshold in the nuclear matter and consequently increases the production cross section of the  $D$  and  $\bar{D}$  mesons in antiproton nucleus reactions.

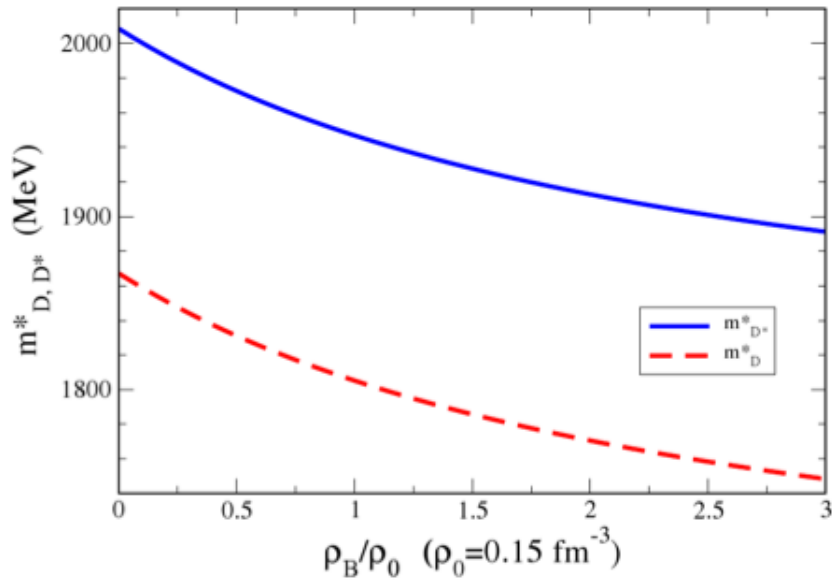


Figure 1.2:  $D$  and  $D^*$  meson effective masses as a function of nuclear matter density.

Another important study for a better understanding of the properties of charmed hadrons in nuclear matter is the measurement of the  $J/\Psi$  dissociation in the nuclear matter. This phenomenon is due to any interaction of  $J/\Psi$ , or its precursor



states, with the nuclear medium which could break the bound state of the charm composing it. The available data on the  $J/\Psi$  nucleon cross section are scarce and they are determined by indirect experimental information from the  $J/\Psi$  nucleon interaction in high energy  $pN$  (proton-Nucleus) collisions, so the deduced  $J/\Psi$  nucleon dissociation cross section has large uncertainties and its momentum dependence is unknown. In PANDA a reliable  $J/\Psi$  nucleus dissociation cross section will be obtained by the comparison of the production yield of  $J/\Psi$  in  $\bar{p}$  annihilation on  $p$  and different nuclear targets. This is important for the understanding of the charmonium suppression in relativistic heavy ion collisions, which is considered one of the most promising signature of the formation of the quark-gluon plasma.

### 1.1.2 Parton Structure

#### Generalized parton distributions

The binding force between quarks and gluons, which makes possible the formation of hadrons, has to be studied in the non-perturbative QCD regime. At the moment there is not a reliable fully quantitative calculation starting from QCD first principles, so the nucleon structure is described by phenomenological functions like form factors, parton densities and distribution amplitudes. In the infinite momentum approximation, the partons are free non-interacting particles and it is possible to describe the hadrons with the distribution of partons in the longitudinal direction given by the distribution functions, while elastic form factors give information on the charge and magnetization distributions in the transverse plane. The Generalized Parton Distributions (GPDs) unify and extend these concepts, giving a description of partons with functions of more variables and allowing a full three dimensional image of hadrons. The GPDs, introduced in the study of hard exclusive processes in lepton scattering experiments, contain informations on the distribution of partons both in the transverse plane and in the longitudinal direction and the quark and gluon angular momentum contributions to the nucleon spin. PANDA will conduct studies of Hard Exclusive Processes in  $\bar{p}p$  annihilation with various final states in a new kinematic region expecting new insights into the applicability and universality of these novel QCD approaches. Measurement of the Crossed-Channel Compton Scattering ( $\bar{p}p \rightarrow \gamma\gamma$ ) and Hard exclusive meson production ( $\bar{p}p \rightarrow \gamma\pi^0$ ) are foreseen.

#### The Drell-Yan process

The Drell-Yan process occurs in high energy hadron-hadron scattering, where a quark and antiquark from the interacting hadrons annihilate creating a virtual photon or  $Z$  boson, which then decays into a pair of oppositely-charged leptons as shown in Figure 1.3.

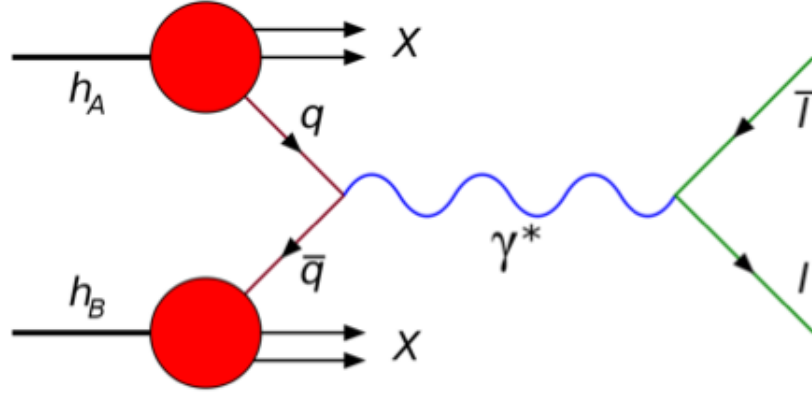


Figure 1.3: Drell-Yan process.

The Drell-Yan process is an ideal tool for investigating the transverse parton distribution functions. In PANDA the Drell-Yan process will be studied in semi-inclusive lepton production for di-muons in scattering of unpolarized antiproton beam over unpolarized proton target  $\bar{p}p \rightarrow \gamma^* \rightarrow \mu\mu + X$ . From the angular distribution of dileptons it is possible to evaluate the distribution function of a transversely polarized quark inside an unpolarized hadron  $h_1^\perp(x, \vec{k}_\perp^2)$ .

### Time-like form factor of the proton

The electromagnetic form factor of the proton is of upmost importance for the study of hadronic structure and internal dynamics at low energies as well as the higher energies where perturbative QCD applies. The measurement of the electron scattering on protons allows to determine the proton form factors in the region of space-like momentum transfer  $q^2 < 0$ . While  $\bar{p}p \rightarrow e^+e^-$  annihilation, shown in Figure 1.4, gives access to the proton electromagnetic form factors in the time like region  $q^2 > 4m_p^2c^2$ , where  $m_p$  is the proton mass.

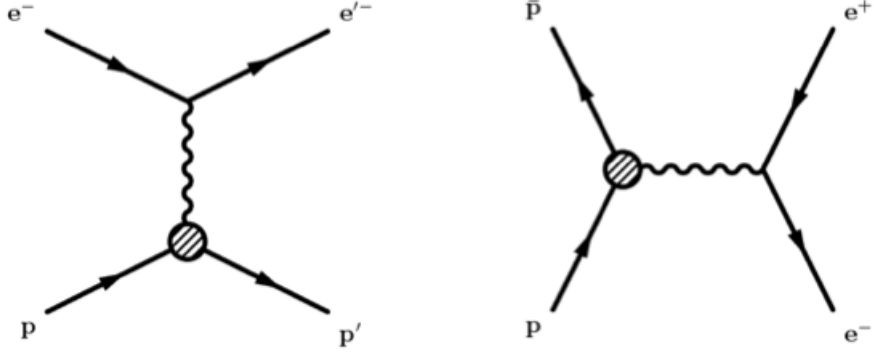


Figure 1.4: Feynman diagrams for electron scattering on proton (left) and its crossed channel  $\bar{p}p \rightarrow e^+e^-$  (right).

In the space-like region the form factors are real functions of  $q^2$ , and they are the Fourier transforms of the spatial charge ( $G_E$ ) and the magnetization distribution ( $G_M$ ). In the time-like region the form factors are complex functions, and represent the frequency spectrum of the electromagnetic response of the nucleon. The  $\bar{p}p \rightarrow e^+e^-$  in one photon approximation is a linear combination of  $|G_E|^2$  and  $|G_M|^2$ . The  $q^2 < 15\text{GeV}/c^2$  region of the proton time-like form factor have been measured by E760 and E835 experiments at Fermilab, but due to limited statistics  $|G_E|$  and  $|G_M|$  have not been measured separately. Thanks to its improved statistics and wide angular coverage, PANDA will measure the  $G_E$  and  $G_M$  separately with an unprecedented precision up to  $14\text{GeV}/c^2$  and the absolute and differential cross section up to  $22\text{GeV}/c^2$ . Therefore it is possible to test the transition to the perturbative QCD regime, where an asymptotic behavior is predicted for the proton magnetic form factor, moreover The PANDA rich particle identification plays an important role in the rejection of the  $\bar{p}p \rightarrow \pi^-\pi^+$  background with a cross section 106 times higher.

## 1.2 The PANDA Detector

It will provide:

- a  $4\pi$  solid angle coverage around the interaction point between the antiproton beam and the fixed target
- high event rate capability ( $2 \cdot 10^7 \text{ annihilations/s}$ )
- detection and identification of charged particles in a wide momentum range ( $100\text{MeV}/c - 15\text{GeV}/c$ )

- high momentum (1%) and tracking resolution of charged particles

The detector is divided in two parts: a target spectrometer surrounding the interaction region and a forward spectrometer mounted behind the target spectrometer. Using these spectrometers it is possible a full angular coverage of the spatial region around the interaction point.

### Target spectrometer

The target spectrometer, surrounding the interaction point, measures charged tracks for polar angles larger than  $22^\circ$ . It is made by:

- Solenoid Magnet: superconducting solenoid coil providing a maximum magnetic field of  $2T$  with a homogeneity better than 2% over the volume of the vertex detector and central tracker. It has an inner radius of  $90cm$  and a length of  $2.8m$ .
- Micro Vertex Detector (MVD): the closest detector to the interaction point, it is based on radiation hard solid state detectors, both pixel and microstrip. It is designed in order to track the charged particle for the vertex reconstruction and measure the energy loss per unit path-length ( $\frac{dE}{dx}$ ) for slow charged particle identification. In the current MVD design, there are two barrels of pixel detectors, two barrels of strip detectors and six disks arranged perpendicularly to the beam pipeline. The inner four layers of the disks are made of pixels, the following two are made of pixels on the inner part and strips on the outer one.
- Central Tracker: based on a barrel detector surrounding the MVD useful to obtain a good detection efficiency for secondary vertices. There are two methods proposed to achieve the desired detection efficiency. The first one is covering a large area around the MVD with straw tubes (STT) or a time-projection chamber (TPC). The second one is based on three sets of gas electron multipliers (GEMs) employed to detect particles emitted at angles below  $22^\circ$  which are not covered by STT or TPC.
- Cherenkov Detectors and Time-of-Flight barrels: the first ones cover the part of the momentum spectrum above  $1GeV/c$  while the second ones identify slower particles. Combining the information from both detectors it is possible to determinate the mass of detected particles.
- Electromagnetic Calorimeters: required to cover a large energy range (few  $MeV$  up to several  $GeV$ ), it is based on lead-tungstate inorganic scintillators. Lead-tungstate is chosen for its good energy resolution in photon, electron and hadron detection, fast response and high density.

- Muon Detectors: made by 72 strips of plastic scintillator counters mounted behind the iron yoke of the target spectrometer. In addition, an equal number of strips will be placed perpendicular to the beam axis, at the front of the solenoid magnet.

### Forward spectrometer

The forward spectrometer detect small angle tracks. It is made by:

- Dipole Magnetic: covers the entire angular acceptance ( $\pm 10^\circ$  in the horizontal direction and  $\pm 5^\circ$  in the vertical direction). It is used for momentum analysis of charged particles in forward spectrometer: the maximum bending power,  $2Tm$ , could deflect an antiproton beam at the maximum momentum of  $15GeV$  by  $2.2^\circ$  from the original track.
- Forward Trackers: based on a set of wire chambers allowing to track particles with high momenta as well as very low momentum particles. The expected momentum resolution of the system for  $3GeV$  protons is  $\frac{\delta p}{p} = 0.2\%$ . Furthermore, it makes possible to reconstruct tracks in each chamber separately, in case of multi-track events.
- Forward Particle Identification: based on a Ring Imaging Cherenkov (RICH) which separates  $\pi/K/p$  through two radiators: silica aerogel and  $C_4F_{10}$  gas.
- Forward Electromagnetic Calorimeter: based on lead-scintillator sandwiches readout with wavelength shifting fibers, it is a Shashlyk-type calorimeter with high resolution used to detect photons and electrons.
- Forward Muon Detector: based on 20 vertical strips for muon detection similar to the muon system of target spectrometer

## 1.3 Micro Vertex Detector (MVD)

Currently, the PANDA MVD group is engaged in different research and development activities for an optimized detector design starting from the experimental requirements. In particular, the INFN microelectronic group of Turin is studying the front-end electronics for the MVD taking into account the simulations of  $\bar{p}p$  and  $\bar{p}N$  collisions results. The basic specification for the MVD are:

- Spatial Resolution:  $\delta^3x \leq 100\mu m$  is required for a clear detection of the displaced vertices.
- Material Budget: since the MVD is the innermost detector it does not have to affect the outer detector components, therefore the MVD material budget has to be kept as low as possible.

- Time Resolution: the mean time between two interactions is 50ns, so a time resolution  $\delta t \leq 10ns$  is required in order to associate the MVD hits with the correct interaction.
- Readout Speed: taking into account the estimated MVD particle hit rate of  $3 \cdot 10^9$  the overall readout speed has to be in the order of  $\sim 100Gbit/s$ . This is due to the fact that the MVD has to send out to the offline electronics all the data which contains information on the hit position, timing and energy loss, since the PANDA detector will not have a centralized trigger system.
- Radiation Hardness: a fundamental parameter for the reliability of both sensors and electronics since the close position of the MVD to the interaction point and the high event rate.
- Device Thickness: lower than 1mm (1% of radiation length), to be able to detect low momentum particles and to avoid multiple scattering.

In the MVD will be used both silicon pixel detectors and double-sided silicon strip detectors (DSSD) as shown in Figure 1.5.

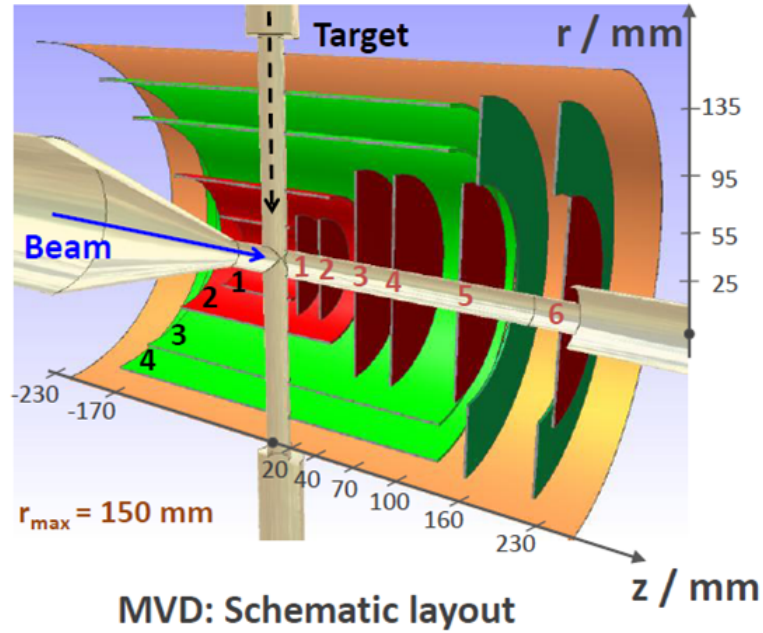


Figure 1.5: MVD schematic layout. The red area is covered with pixel sensors, the green one with DSSD.

The pixels will be used in the inner part, where the density of particles is higher, and each pixel sensor will have an active area of  $100\mu m \times 100\mu m$ , while the strips

will be used in the outer part, where the density of particles is lower. Since the subject of this thesis is to describe the front-end implementation for microstrip sensors, henceforward we'll focus on the description of DSSD.

### Double-Sided silicon Strip Detectors

The DSSD are made by an upper layer of strips arranged in rows and by a lower layer arranged in columns. When a particle hits the detector, its position is given by the intersection of the strip of the upper layer and the strip of the lower layer in order to obtain a two dimensional information. The use of this kind of sensor is preferred to pixel sensors since it allows the reduction of readout channels maintaining the same spatial resolution. In fact, a number  $N_{pixel} = \frac{A}{(\Delta x)^2}$  of channels is required to cover a square area  $A$  with a spatial resolution  $\Delta x$ , on the other hand with  $N_{strip} = 2\sqrt{N_{pixel}}$  strip readout channels it is possible to have the same performances with a significant reduction of the material budget. The main drawback of DSSD is the ghost hit. When two particles hit the detector at the same time, generating similar signals, it is more difficult to obtain the exact position of each particle by analyzing the cross points between the upper and the lower layer hit because more combinations are possible: the cross points where there is no interaction with the particle hitting are called ghost hits (Figure 1.6).

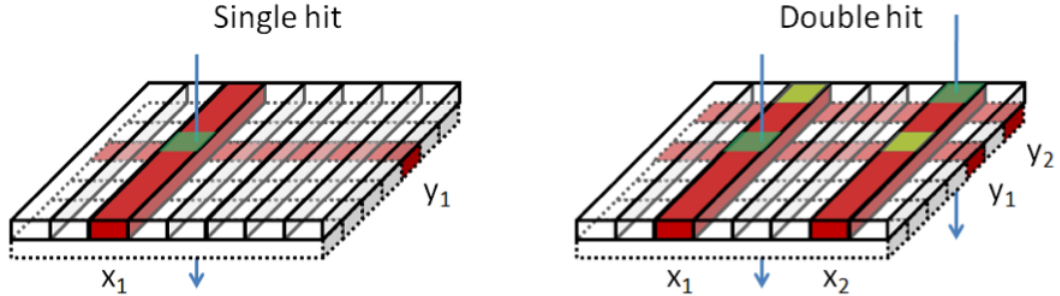
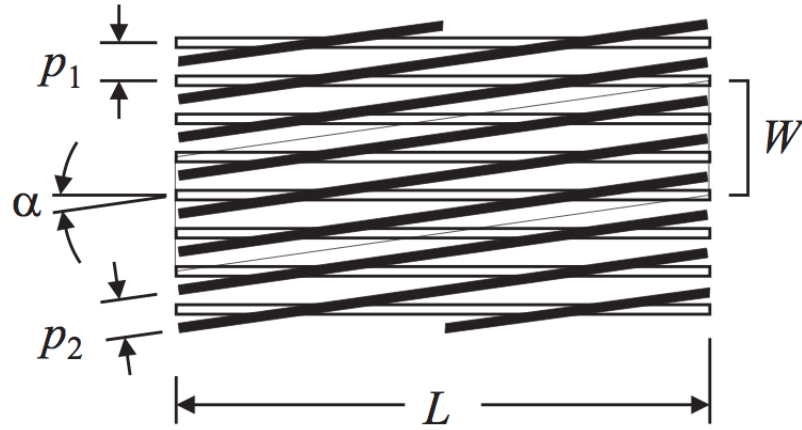


Figure 1.6: Ghost hit during a double hit on a double sided strip sensor.

A possible solution to this problem is to reduce the stereo angle, that is the angle between the strips of the two layers, rather than  $90^\circ$ . The area subtended by two sensing strips of length  $L_1$  and  $L_2$  arranged at an angle  $90^\circ$  is  $A = L_1 L_2$ , so the probability of ghost hits is maximal. However if we use a stereo angle  $\alpha < 90^\circ$ , as shown in Figure 1.7, the capture area, in the approximation  $L_1 = L_2 \equiv L$ , is:

$$A \approx L^2 \frac{p_2}{p_1} \tan \alpha + L p_2 \quad (1.1)$$

Figure 1.7: DSSD with a stereo angle  $\alpha < 90^\circ$ .

It is important to observe that decreasing the stereo angle  $\alpha$  minimize the probability to have a ghost hit but the price is a reduction of resolution in the longitudinal coordinate. This issue does not affect pixel detectors since in a matrix of pixels, each element correspond to one only pixel and, consequently, when a particle hits the detector, there isn't ambiguity about its position [13]. That is the reason why pixel detectors are employed in the inner part of the MVD and strip detectors in the outer layers where the hit rate is lower. The strips are rectangular shaped in the barrel part and trapezoidal in the disk part (Figure 1.8), their width (pitch) and stereo angle determines the spatial resolution. The pitch chosen is  $130\mu m$  for rectangular sensors and  $70\mu m$  for trapezoidal sensors, while the stereo angles are  $90^\circ$  and  $15^\circ$  respectively. There will be 12 million pixel and 200,000 strip readout channels with a total power dissipation of  $4kW$ .



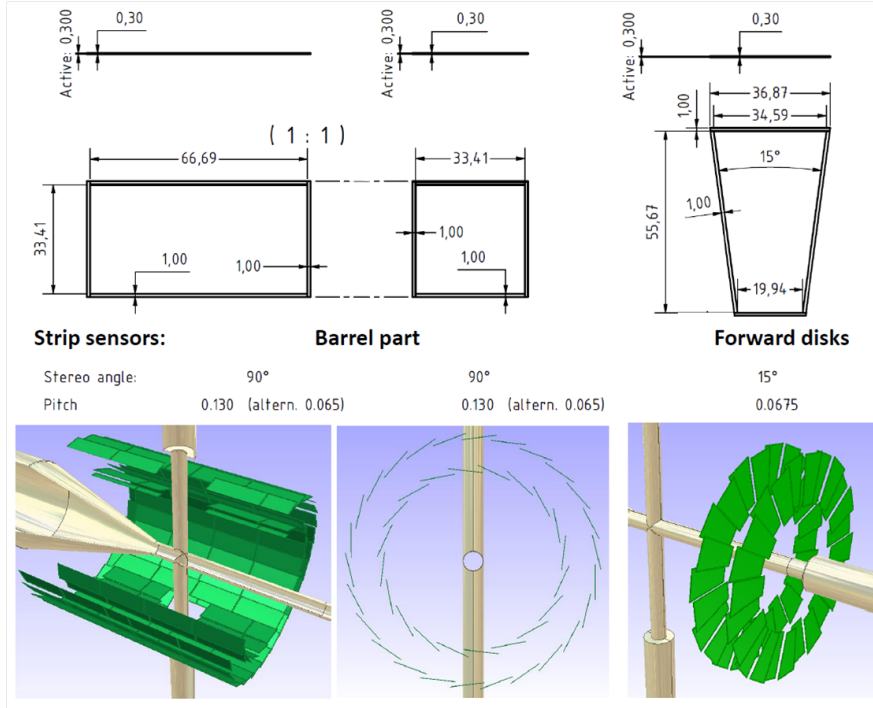


Figure 1.8: Double-Sided silicon Strip Detectors implementation.

The key parameters of the strip system that will drive the design of the front-end electronics are summarized in Table 1.1.

Parameter	Value
width	$\leq 8mm$
depth	$\leq 8mm$
input pad pitch	$\approx 50\mu m$
channels per front-end	$2^6 \div 2^8$
rectangular short strips capacitance	$< 10pF$
rectangular log strips capacitance	$< 50pF$
trapezoidal sensors capacitance	$< 20pF$
input ENC with $C_{det} = 10pF$	$< 800e^-$
input ENC with $C_{det} = 25pF$	$< 1000e^-$
dynamic range	$240ke^- (\approx 38.5fC)$
minimum SNR for MIPS	12
peaking time	$\approx (5 \div 25) ns$
digitization resolution	$\geq 8bit$
overall power dissipation	$< 1W$

Table 1.1: Requirements for the strip front-end ASIC.

## Chapter 2

# Front-End Amplifier

The term "front-end" indicates the very input stage in any electronic readout chains for nuclear physics detectors. With this term is usual to intend a combination of two stages: preamplifier and shaper. The first is directly connected to the sensor and it's the first device that process the signal generated by the charge released by the hitting particle, the second, as its name suggests, is responsible to manipulate the signal shape in order to make it easier to analyze it in the following stages. In this chapter we'll focus at first on ideal cases considering linear, time-invariant networks that are simpler to handle using the Laplace transforms; then we will discuss the effects of non-idealities and in the last part we'll approach to the noise calculations.

### 2.1 The preamplifier

The preamplifier stage is represented by a Charge Sensitive Amplifier. As it's easy to understand from its name, a Charge Sensitive Amplifier (CSA) is the block responsible to amplify the input charge signal. A CSA is built by connecting a capacitor  $C_f$  in the feedback path of a high gain voltage amplifier as shown in Figure 2.1.

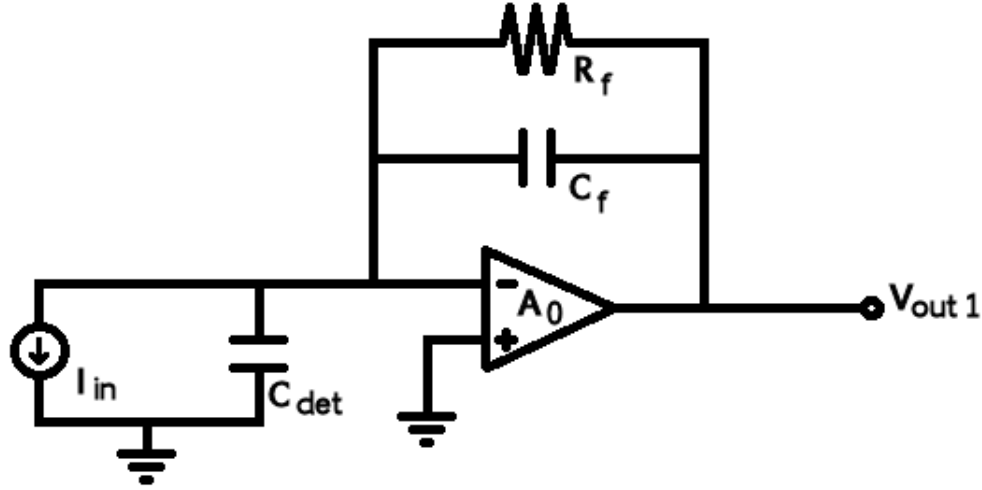


Figure 2.1: Charge Sensitive Amplifier implementation.

However, to achieve an appropriate bias point through the negative feedback mechanism, it is necessary to guarantee also a DC path between the output and the input of the amplifier, and this explains the presence of a feedback resistor  $R_f$  in the CSA block. Henceforward, we'll do some basic assumption to study the transfer function of the readout chain:

- The feedback resistor  $R_f$  has a value so high that its contribution to the signal processing can be neglected.
- The input signal can be approximated with a  $\delta$ -like pulse (easier to manage with respect to triangular shaped signals), so  $I_{in}(t) = Q_{in}\delta(t)$ .
- The core amplifier has infinite gain and bandwidth.

Under the assumptions mentioned above, the input-output relationship of the CSA can be written as:

$$V_{out}(t) = \frac{1}{C_f} \int I_{in}(t) dt = \frac{Q_{in}}{C_f} u(t) \quad (2.1)$$

where  $u(t)$  is the unit step function that is the integral of the Dirac- $\delta$ . For the time being, in all the graphics that will be presented the signals will be shifted by a proper amount of time from the origin with the purpose of a better visualization, so we'll use  $\delta(t - t_0)$  and  $u(t - t_0)$ . Adjusting the input charge and the feedback

capacitor values in order to obtain an output signal of 1V, the response of the CSA to a  $\delta$ -like pulse is shown in Figure 2.2. To have a 0V baseline, one would have a dual power supply, but in most applications a single rail powering is for system simplicity. This implies that the quiescent point of a circuit is usually different from the ground level. However, this is not relevant for our purposes, therefore we will represent signals starting from a 0V level.

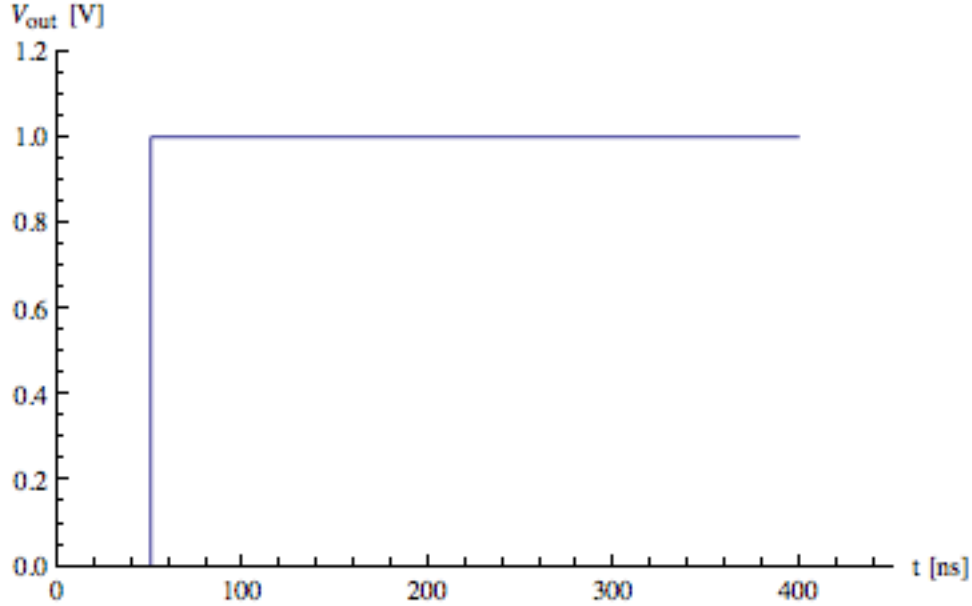


Figure 2.2: Output signal of the CSA with  $\frac{Q_{in}}{C_f} = 1V$ .

## 2.2 The shaper

Shaping implies manipulating and altering the frequency content of the original waveform, therefore a pulse shaper is primarily an analog filter [15, 3, 16, 10, 9, 14, 6]. As it is possible to observe in Figure 2.3, the simplest type of pulse shaper consists of two filters separated by a voltage buffer in order to decouple the time constants, while the rightmost buffer allows to drive the load of the following stages. The transfer function of this chain can be written as:

$$V_{out}(s) = \frac{Q_{in}}{sC_f} \cdot \frac{s\tau_z}{1 + s\tau_z} \cdot \frac{1}{1 + s\tau_p} \quad (2.2)$$

The first term represent the transfer function of the preamplifier stage, neglecting as assumed the contribute of the feedback resistor  $R_f$ , that is a simple integration stage; the second is the typical input-output relationship of a high-pass filter

where  $\tau_z = R_z C_z$  takes the name of derivation time constant, while the third is due to the low-pass filter with  $\tau_p = R_p C_p$  called integration time constant.

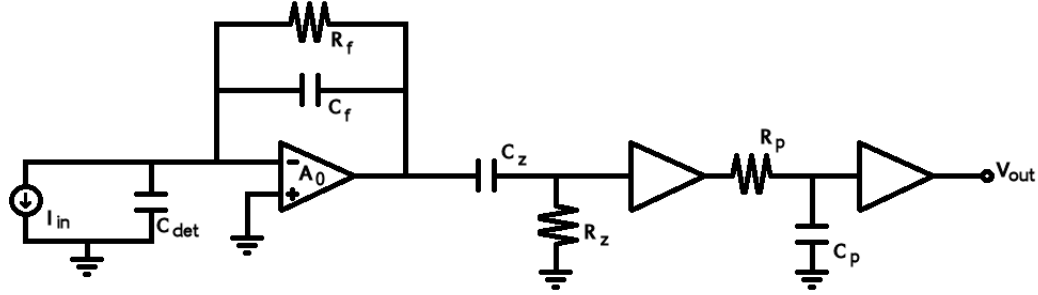


Figure 2.3: CR-RC shaping stage.

It is important to observe that the zero at  $s = 0$  introduced by the high-pass filter is cancelled by the pole in the same position due to the CSA stage, because this will become an issue when we'll drop off the hypothesis that  $R_f$  has an infinite value. The signal representation in the time domain, valid for  $\tau_z \neq \tau_p$ , is:

$$V_{out}(t) = \frac{Q_{in}}{C_f} \frac{\tau_z}{\tau_z - \tau_p} \left( e^{-\frac{t}{\tau_z}} - e^{-\frac{t}{\tau_p}} \right) \quad (2.3)$$

In the particular case  $\tau_z = \tau_p \equiv \tau$  the signal representation in the Laplace and time domain are, respectively:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \frac{\tau}{(1 + s\tau)^2} \quad (2.4)$$

$$V_{out}(t) = \frac{Q_{in}}{C_f} \left( \frac{t}{\tau} \right) e^{-\frac{t}{\tau}} \quad (2.5)$$

The value of the ratio  $\frac{\tau_p}{\tau_z}$  is a very important parameter since its optimization gets to the best compromise between the signal length and amplitude. If we fix  $\tau_z$  trying different values for  $\tau_p$  we obtain the graphic shown in Figure 2.4: it's easy to observe that the greater is  $\tau_p$  the lower is the signal amplitude whose shape become smoother and smoother. Moreover when  $\tau_p > \tau_z$ , the integration time constant starts to dominate the signal duration, but this is not a surprise since for  $\tau_p \gg \tau_z$  the signal equation becomes:

$$V_{out}(t) \approx \frac{Q_{in}}{C_f} \left( \frac{\tau_z}{\tau_p} \right) e^{-\frac{t}{\tau_p}} \quad (2.6)$$

with  $\tau_p$  playing the role of the decay time constant.

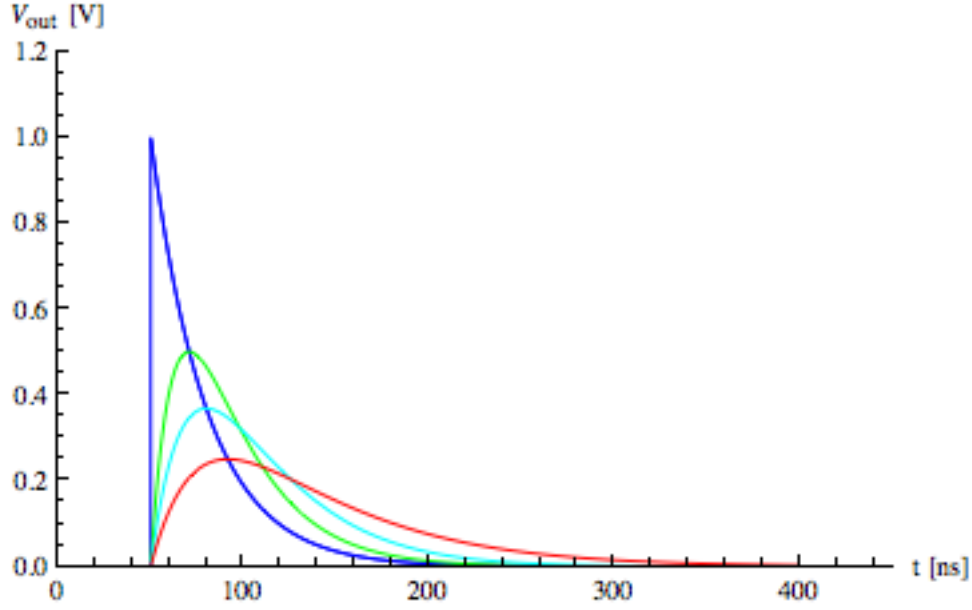
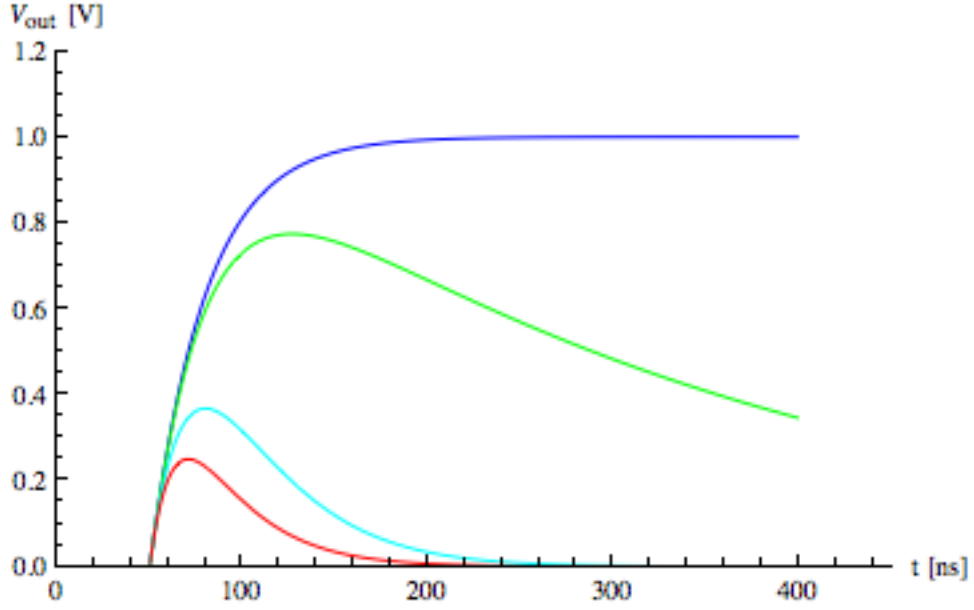


Figure 2.4: Optimization of  $\frac{\tau_p}{\tau_z}$ : fixed  $\tau_z = 30ns$ .

The next step is to fix  $\tau_p$  varying  $\tau_z$ , in this case the results are shown in Figure 2.5. The most interesting observation is for  $\tau_z = \infty$ , that is when there is no derivation of the signal as we can see from the equation below:

$$V_{out}(t) = \frac{Q_{in}}{C_f} \left( 1 - e^{-\frac{t}{\tau_p}} \right) \quad (2.7)$$

in this case the step at the CSA output is a smoother signal with a 10% to 90% rise time of  $\sim 2.2\tau_p$  assuming  $\frac{Q_{in}}{C_f} = 1V$ . Decreasing  $\tau_z$  the signals starts to be cut cut both in amplitude and duration and when  $\tau_z < \tau_p$  the slower time constant dominates the return of the signal to the baseline and only the amplitude is reduced.

Figure 2.5: Optimization of  $\frac{\tau_p}{\tau_z}$ : fixed  $\tau_p = 30ns$ .

According to these results,  $\frac{\tau_p}{\tau_z} = 1$  represent the best choice for the time constant values, in fact for a specific pulse duration this is the configuration that maximize the signal amplitude, so henceforward we'll consider only the case with  $\tau_z = \tau_p \equiv \tau$ . The time constant  $\tau$  plays a key role in the signal processing as we can observe solving the following equation:

$$\frac{\partial V_{out}(t)}{\partial t} = \frac{\partial}{\partial t} \left[ \frac{Q_{in}}{C_f} \left( \frac{t}{\tau} \right) e^{-\frac{t}{\tau}} \right] = \frac{Q_{in}}{C_f} \left( \frac{1}{\tau} e^{-\frac{t}{\tau}} - \frac{t}{\tau^2} e^{-\frac{t}{\tau}} \right) = 0 \quad (2.8)$$

the solution to this equation gives the time at which the signal reaches its maximum value, that is its peaking time  $T_p = \tau$ . The peak of the output signal is obtained by the following expression:

$$V_{out,max} = V_{out}(\tau) = \frac{Q_{in}}{C_f} \frac{1}{e} \quad (2.9)$$

If necessary, the gain loss equal to  $\frac{1}{e}$  can be recovered adjusting the gain of one of the buffers of the shaping block (Figure 2.3).

Another way to implement the shaping stage is to use two transimpedance amplifiers as shown in Figure 2.6. In this configuration we can notice a first difference with respect to the architecture mentioned above, that is the absence of any buffer stage to decouple the filters time constants since the low output impedance of the voltage amplifier is exploited to provide it. The transfer function of this chain is:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \frac{C_z}{C_1} \frac{R_2}{R_c} \frac{\tau}{(1 + s\tau)^2} \quad (2.10)$$

with  $\tau = R_1 C_1 = R_2 C_2$ . The signal expression in the time domain is then:

$$V_{out}(t) = \frac{Q_{in}}{C_f} \frac{C_z}{C_1} \frac{R_2}{R_c} \left( \frac{t}{\tau} \right) e^{-\frac{t}{\tau}} \quad (2.11)$$

and even in this case we found the relationship  $T_p = \tau$  with:

$$V_{out,max} = V_{out}(\tau) = \frac{Q_{in}}{C_f} \frac{C_z}{C_1} \frac{R_2}{R_c} \frac{1}{e} \quad (2.12)$$

where it's easy to observe a key difference with respect to the result obtained with a passive network, that is the presence of an additional gain given by:

$$G = \frac{C_z}{C_1} \frac{R_2}{R_c} \quad (2.13)$$

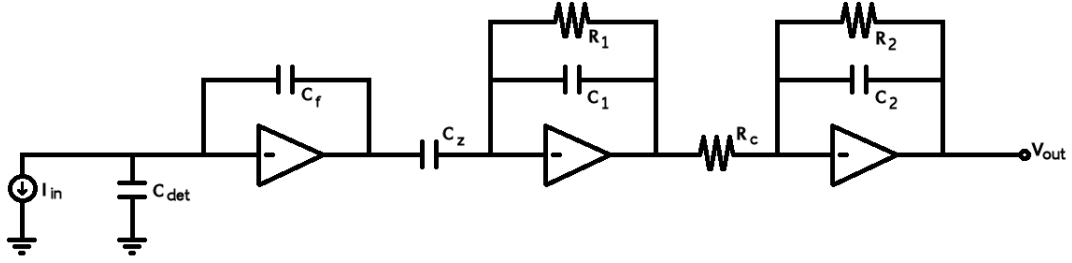


Figure 2.6: CR-RC shaping stage implemented with TIAs (TransImpedance Amplifiers).

### 2.2.1 CR-(RC)<sup>n</sup> shapers

The study we made so far can be used to explore the effects of adding other low-pass filtering stages, in order to modify the signal shape according to the informations of interest we want to extrapolate. The transfer function of such configuration can be written as:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \frac{\tau}{(1 + s\tau)^{n+1}} \quad (2.14)$$

where  $\tau = R_z C_z = R_{p1} C_{p1} = R_{p2} C_{p2} = \dots = R_{pn} C_{pn}$  since the considerations about the filters time constant made above are still valid. We can notice that the signal expression in the Laplace domain has  $n+1$  poles: 1 introduced by the high-pass filter and the remaining  $n$  given by the  $n$  low-pass filters. This result is



referred to a structure like that of Figure 2.3, but is valid also if we consider an architecture such as that of Figure 2.6 as long as we add the gain factor  $\frac{C_z R_2}{C_1 R_c}$ . The chain pulse response in the time domain is given by:

$$V_{out}(t) = \frac{Q_{in}}{C_f} \frac{1}{n!} \left( \frac{t}{\tau} \right)^n e^{-\frac{t}{\tau}} \quad (2.15)$$

By solving the following equation we can easily obtain the expression of the peaking time  $T_p$ :

$$\begin{aligned} \frac{\partial V_{out}(t)}{\partial t} &= \frac{\partial}{\partial t} \left[ \frac{Q_{in}}{C_f} \frac{1}{n!} \left( \frac{t}{\tau} \right)^n e^{-\frac{t}{\tau}} \right] = \\ &= \frac{Q_{in}}{C_f} \frac{1}{n!} \left[ \frac{n}{\tau} \left( \frac{t}{\tau} \right)^{n-1} e^{-\frac{t}{\tau}} - \left( \frac{t}{\tau} \right)^n \frac{1}{\tau} e^{-\frac{t}{\tau}} \right] = 0 \implies T_p = n\tau \end{aligned} \quad (2.16)$$

so it's easy to dimension the components of the low-pass filters in order to obtain the desired peaking time and maximum amplitude voltage according to the following relationship:

$$V_{out,max}(n) = V_{out}(n\tau) = \frac{Q_{in}}{C_f} \frac{n^n}{n!} e^{-n} \quad (2.17)$$

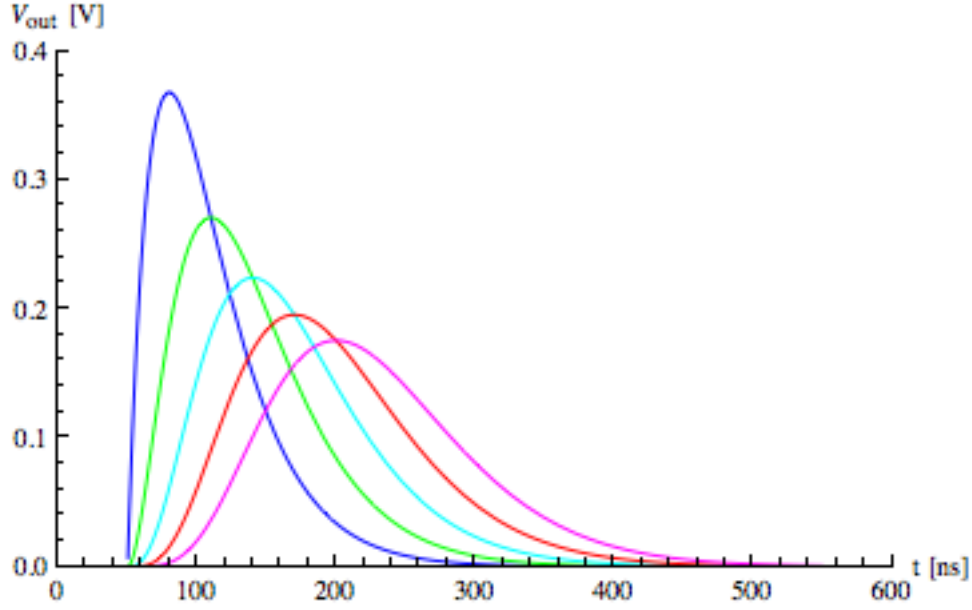
For a better understanding of this kind of architecture, we'll study two different cases:

### 1. Increasing $n$ without changing $\tau$

Assuming that  $\frac{Q_{in}}{C_f} = 1V$  we obtain as result the plots shown in Figure 2.7. We can notice that increasing  $n$  we have: higher peaking time, lower signal amplitude (that could anyway be adjusted by a proper additional gain), higher symmetry in signal shape. However, the amplitude attenuation is less remarkable in the transition  $n \rightarrow n+1$  as we can notice observing the following expression:

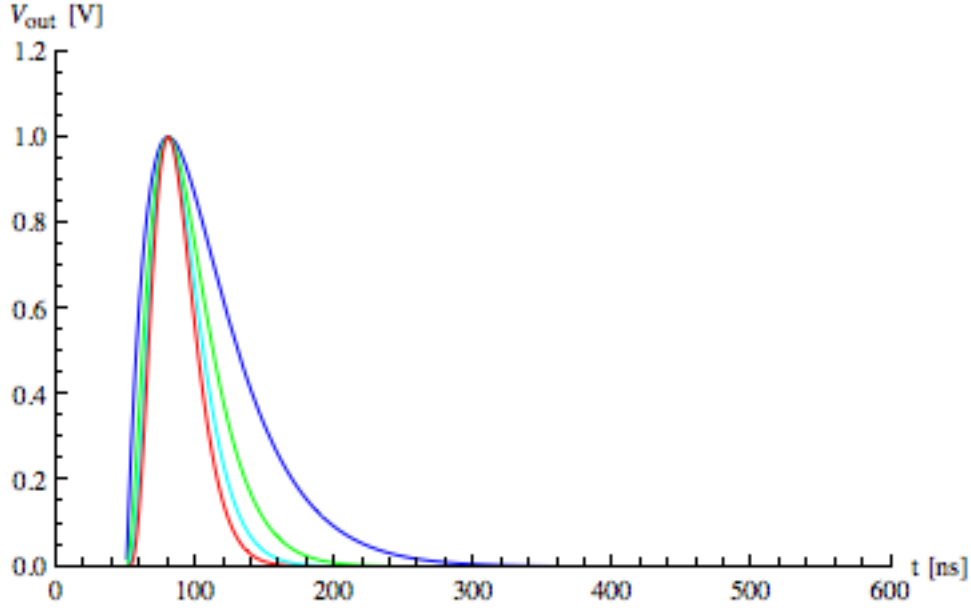
$$\lim_{n \rightarrow \infty} \frac{V_{out,max}(n+1)}{V_{out,max}(n)} = \lim_{n \rightarrow \infty} \left( 1 + \frac{1}{n} \right)^n \frac{1}{e} = e \cdot \frac{1}{e} = 1 \quad (2.18)$$

which implies that the amplitude drop stops for shapers of really high order.

Figure 2.7:  $CR-(RC)^n$  with  $\tau = 30ns$ .

## 2. Increasing n adjusting $\tau$ to have the same $T_p$

In this case we fix a certain value for  $T_p$ , so the time constant value will be  $\tau = \frac{T_p}{n}$ . The results of a n swing from 1 to 4 is shown in Figure 2.8, where the amplitudes have been normalized to 1V. The most interesting observation is that the higher is n, the faster is the signal return to the baseline value, but this doesn't surprise since increasing n both the derivation and integration time constants get shorter. In other words, higher order shapers allow for a faster signal with no drawback in terms of peaking time, so they represent a better choice for high rate applications.

Figure 2.8:  $CR-(RC)^n$  with  $T_p = 30ns$ .

## 2.3 Non-ideal behavior

As stated in Section 2.1, all the results obtained so far are valid under certain condition reported below:

- The feedback resistor  $R_f$  has a value so high that its contribution to the signal processing can be neglected.
- The input signal can be approximated with a  $\delta$ -like pulse (easier to manage with respect to triangular shaped signals), so  $I_{in}(t) = Q_{in}\delta(t)$ .
- The core amplifier has infinite gain and bandwidth.

In this Section we'll discuss what happens when we drop off this assumptions.

### 2.3.1 Finite feedback resistor effects

When a finite value of  $R_f$  is considered, the total impedance in the feedback path of the CSA is given by:

$$Z_f = \frac{R_f}{1 + sR_fC_f} \quad (2.19)$$

As a result, the full transfer function modify into the following expression:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \frac{\tau_f}{1 + s\tau_f} \cdot \frac{s\tau}{1 + s\tau} \cdot \frac{1}{1 + s\tau} \quad (2.20)$$

where  $\tau_f = R_f C_f$  is the time constant associated to the feedback network of the CSA. As in the previous section, for simplicity we'll consider an architecture like that of Figure 2.3 and a simple CR-RC shaping stage, but the results could be easily applied to the already studied cases. The most remarkable consequence of the finite value of  $R_f$  is the displacement of the preamplifier pole from  $s_{CSA} = 0$  to  $s_{CSA} = -\frac{1}{\tau_f}$  avoiding the cancellation with the zero at  $s_{hp} = 0$  introduced by the high-pass filter of the shaping stage. The effects of both these modifications in the transfer function can be observed considering the Bode plots of the CSA and of the full chain, shown in Figure 2.9 and Figure 2.10. From the first Bode plot, the one of the preamplifier stage, we can notice the first order low-pass filter behavior of the CSA: after the cut-off frequency  $f_{CSA} = \frac{1}{2\pi\tau_f}$  the gain drops with a slope of 20dB/decade. Studying the second Bode plot, regarding the full front-end chain, is evident a band-pass filter behavior: since the zero has been left in the origin, the gain rises with a slope of 20dB/decade, after the cut-off frequency  $f_{CSA}$  the effect of the zero is cancelled and the gain remains constant until the roll-off of 40dB/decade due to the double pole at the frequency  $f_{Shaper} = \frac{1}{2\pi\tau}$ .

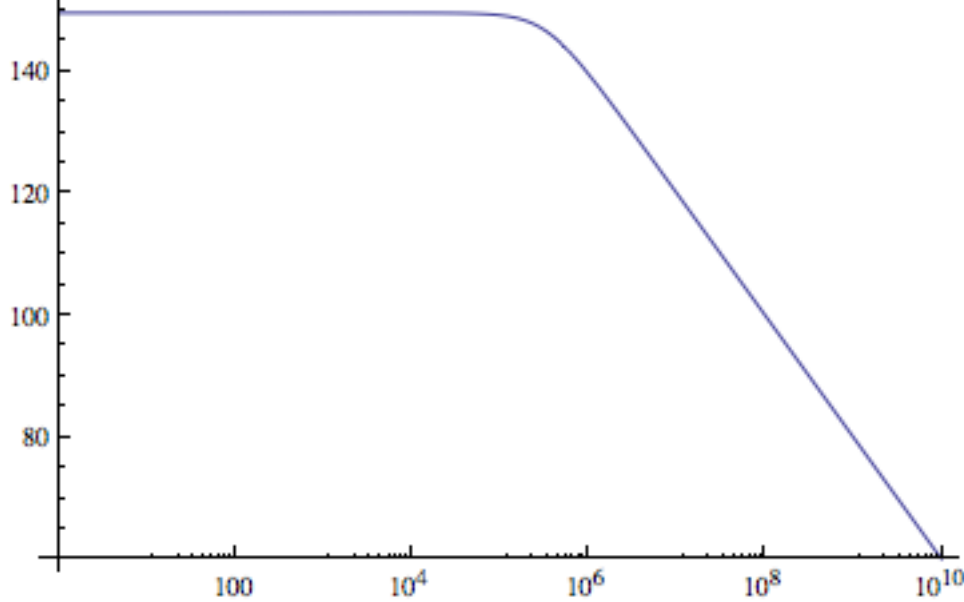


Figure 2.9: Bode plot of a CSA with finite feedback resistor  $R_f = 30M\Omega$  and feedback capacitor  $C_f = 100fF$ .

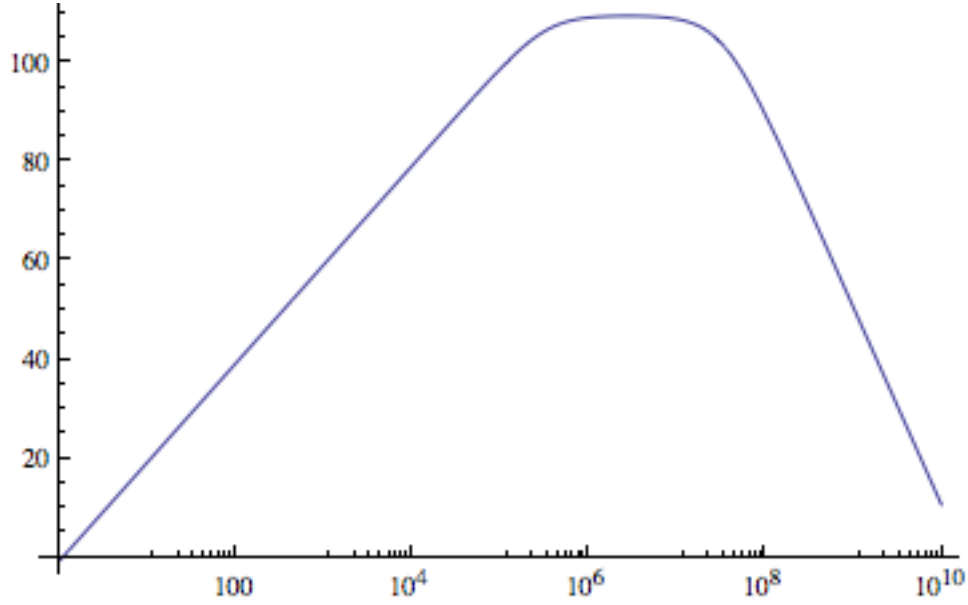


Figure 2.10: Bode plot of a CR-RC shaper with finite feedback resistor  $R_f = 30M\Omega$ , feedback capacitor  $C_f = 100fF$  and shaping time  $\tau = 30ns$ .

This “new” situation have both advantages and drawbacks: the low-pass filter behavior of the CSA leads to the suppression of DC impact and slow variations occurring in the CSA, on the other hand it may cause undesired consequences on the signal shape. These considerations become clear if we consider the signal expression in the time domain reported below:

$$V_{out}(t) = \frac{Q_{in}}{C_f} \frac{\tau_f}{\tau_f - \tau} \left[ \left( \frac{t}{\tau} \right) e^{-\frac{t}{\tau}} + \frac{\tau}{\tau_f - \tau} \left( e^{-\frac{t}{\tau}} - e^{-\frac{t}{\tau_f}} \right) \right] \quad (2.21)$$

For a better understanding of the above relationship it's more useful to consider the case with  $\tau_f \gg \tau$ :

$$\begin{aligned} V_{out}(t) &\approx \frac{Q_{in}}{C_f} \left[ \left( \frac{t}{\tau} \right) e^{-\frac{t}{\tau}} - \left( \frac{\tau}{\tau_f} \right) e^{-\frac{t}{\tau_f}} \right] = \\ &= \left[ V_{out}(t) \right]_{R_f=\infty} - \frac{Q_{in}}{C_f} \left( \frac{\tau}{\tau_f} \right) e^{-\frac{t}{\tau_f}} \end{aligned} \quad (2.22)$$

In this case it's easier to see the introduction of a negative term, the rightmost, that is subtracted to the main signal  $\left[ V_{out}(t) \right]_{R_f=\infty}$ . The pulse response to such a configuration is reported in Figure 2.11 that shows how the output signal goes well below the baseline value before it comes back to the 0V level in a time scale

defined by  $\tau_f$ . This negative tail takes the name of undershoot and if it lasts for a significant time the rate capability of the system might be compromised.

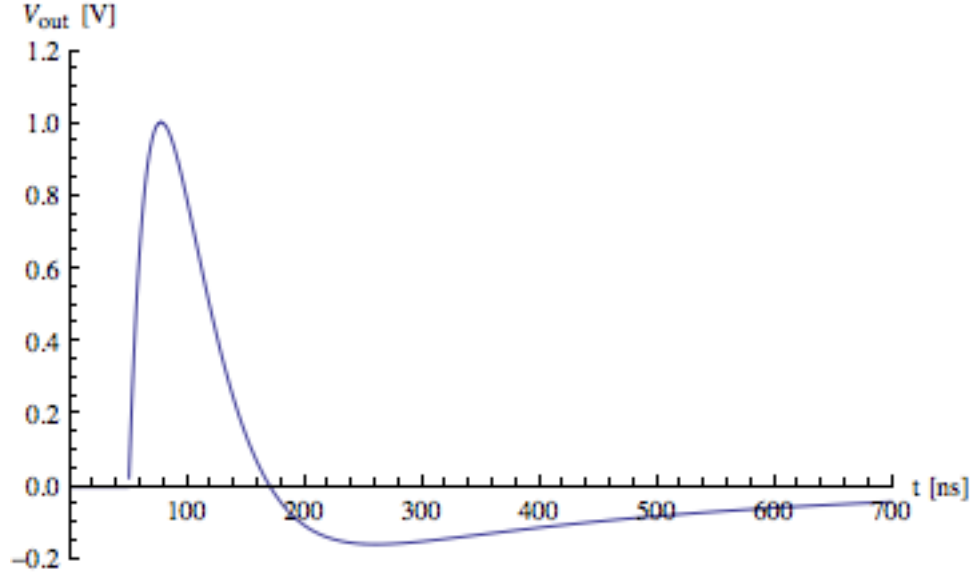


Figure 2.11: CR-RC pulse response with finite CSA feedback resistor.

This phenomenon is due to the presence of  $C_z$ , this capacitor connected in series to the CSA filters any DC component coming from this stage that, as a result, cannot intervene on the DC voltage level at the shaper output. Considering this, we can understand the appearance of the undershoot since the bipolar nature of the signal comes from the necessity to have a null contribution to the output DC value coming from the shaper. The most important effect of the undershoot is the baseline drift at high rates shown in Figure 2.12: the baseline value moves downwards until it reach a new voltage level the gives a zero average value of the output. This situation is referred to input signals with a constant rate, so does not occur in realistic physics cases where the signals produced by a sensor are randomly distributed in time, usually according to the Poisson statistics, generating baseline up and down fluctuations rather than the drift to a constant value. For a better understanding of this phenomenon, that needs to be mastered to avoid it's undesired effects, is useful to study what happens in the case  $t \gg \tau$  when the undershoot signal can be approximated as:

$$V_{undershoot}(t) \approx -\frac{Q_{in}}{C_f} \left( \frac{\tau}{\tau_f} \right) e^{-\frac{t}{\tau_f}} \quad (2.23)$$

This relationship shows that increasing  $\tau_f$  leads to two effects: reduction of the undershoot amplitude, increase of its duration. The reduction of the undershoot

amplitude, obtained increasing the value of  $R_f$ , does not prevent the baseline drift, that is generated by the AC coupling between the preamplifier and the shaper stages, but it worsen instead the rate capability since the constant drift value is reached in a significant longer time.

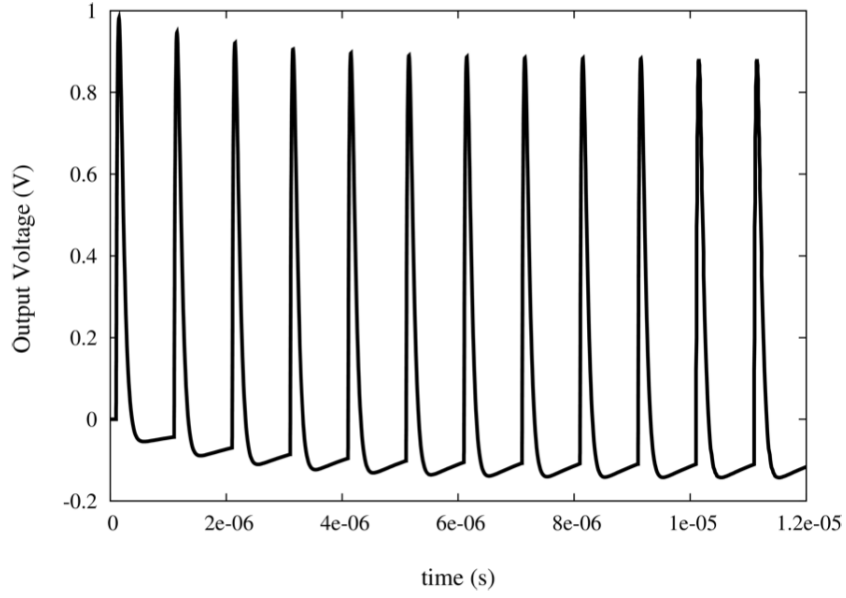


Figure 2.12: Example of baseline drift induced by a train of pulses with constant rate.

### 2.3.1.1 Pole-Zero Cancellation

The first solution to the undershoot issue is to move the zero introduced by the high-pass filter of the shaper in order to have  $s_{hp} = s_{CSA} = -\frac{1}{\tau_f}$ . The technique used to achieve this consists in connecting a resistor  $R_x$  in parallel to the capacitor  $C_z$  as shown in Figure 2.13.

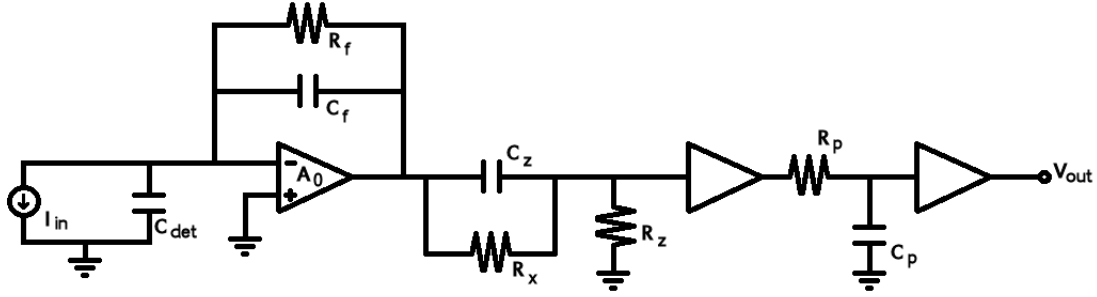


Figure 2.13: Pole-Zero Cancellation.

The new transfer function will be:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \frac{\tau_f}{1 + s\tau_f} \cdot \frac{R_z(1 + sC_zR_x)}{R_z(1 + sC_zR_x) + R_x} \cdot \frac{1}{1 + s\tau} \quad (2.24)$$

Looking at this relationship, it's obvious that if  $R_x = \frac{C_f}{C_z}R_f$  the zero in  $s_{hp} = -\frac{1}{C_zR_x}$  is cancelled with the pole in  $s_{CSA} = -\frac{1}{\tau_f}$  obtaining the expression:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \frac{\tau_{hp}}{1 + s\tau_{hp}} \frac{1}{1 + s\tau} \quad (2.25)$$

where

$$\frac{1}{\tau_{hp}} = \frac{1}{\tau} + \frac{1}{\tau_f} \quad (2.26)$$

define a new pole in  $s_{hp} = -\frac{1}{\tau_{hp}}$ . It's interesting to notice that if we want to match the derivation and the integration time constants, we need to put  $R_pC_p = \tau_{hp}$  rather than  $R_pC_p = \tau$ , but this issue does not occur if we use a chain like that of Figure 2.6 and operate a pole-zero cancellation by connecting a resistor  $R_x$  in parallel to  $C_z$  as shown in Figure 2.14.



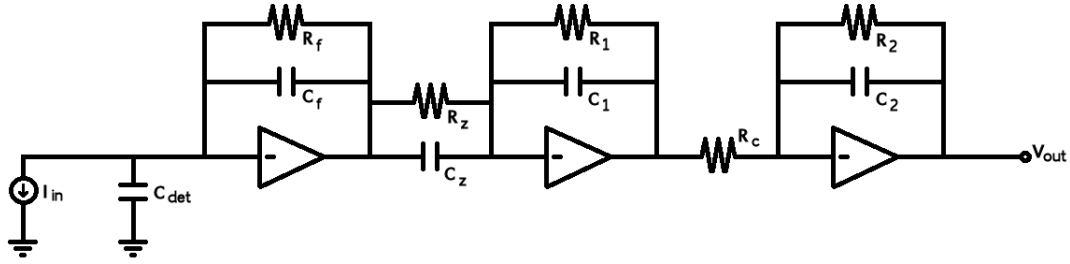


Figure 2.14: Pole-Zero Cancellation with a CR-RC shaper implemented through TIAs.

In this case the total transfer function is:

$$V_{out}(s) = \frac{Q_{in} C_z R_2}{C_f C_1 R_c} \frac{\tau}{(1 + s\tau)^2} \quad (2.27)$$

that is exactly the same obtained in the ideal case  $R_f = \infty$ , leading of course to the same expression in the time domain. As shown in Figure 2.15, the Bode plot of the entire chain highlights a strict low-pass filter behavior, so any signal starting from DC is amplified. A interesting study regards the comparison between the CSA output signal and the total output signal when a train of pulses with constant rate is sent as input. The result is shown in Figure 2.16: there is a significant baseline drift on the CSA output, which however doesn't occur at the end of the chain. This phenomenon found it's explanation observing that the current signal presented as input to the shaper is nothing but a replica of the sensor signal scaled by the factor

$$\frac{C_z}{C_f} = \frac{R_f}{R_z} \quad (2.28)$$

In other words, the combination of CSA and pole-zero cancellation network works as a fast current amplifier.

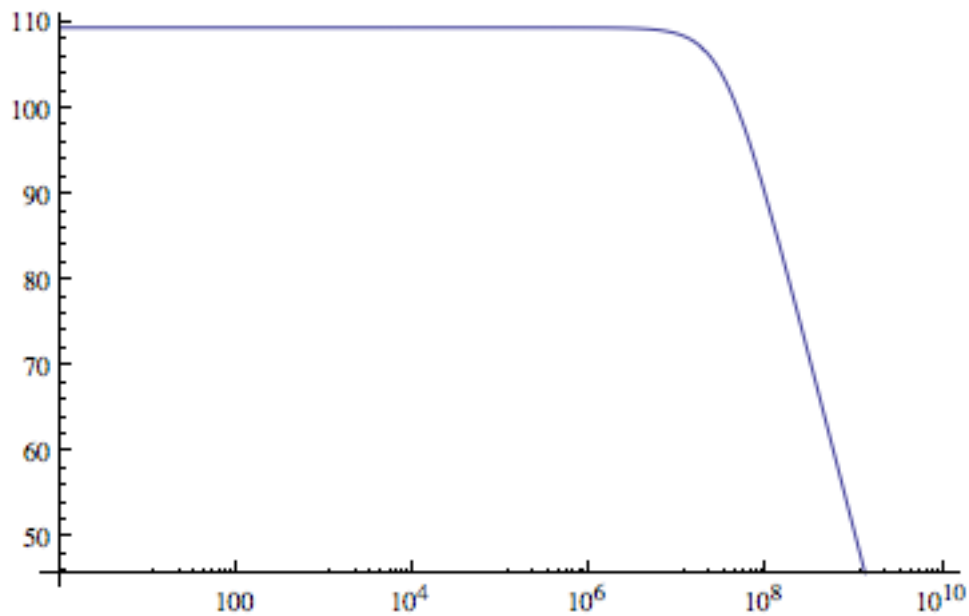


Figure 2.15: Bode plot of a CR-RC shaper with pole-zero cancellation.

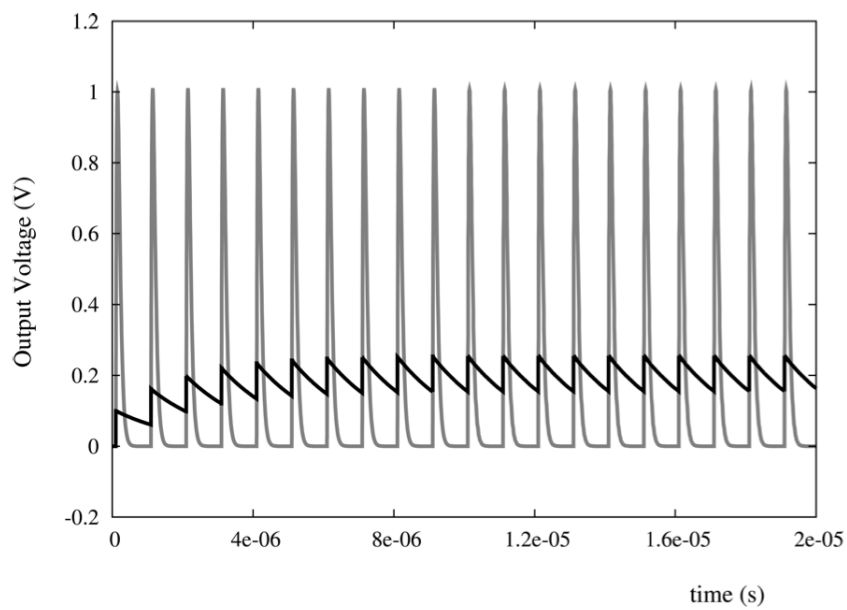


Figure 2.16: CSA and CR-RC shaper, with pole-zero cancellation, response to a train of pulses with constant rate.

### 2.3.1.2 Baseline Holder

As observed in the last part of the previous subsection, the circuit of Figure 2.14 behave as a low-pass filter, so it is sensitive to DC or low frequency variations occurring at its input. For many applications, such as semiconductor detectors, this can represent a serious issue considering that a silicon sensor has an intrinsic leakage current that must be absorbed by the front-end without compromising the system performance. The detector leakage current may also increase because of the exposition to radiation fields the damage the device bulk leading to a significant worsening, from common values of  $\sim \text{nA}$  even to  $\sim \mu\text{A}$  per channel. To overcome this problem an AC coupling between the different stages is necessary. The simplest way to achieve an AC coupling is a capacitor connected in series in the path from one block to the following one, however in many cases this wouldn't be enough and a more elaborated technique is required. The first solution is an architecture called Baseline Holder, shown in Figure 2.17.

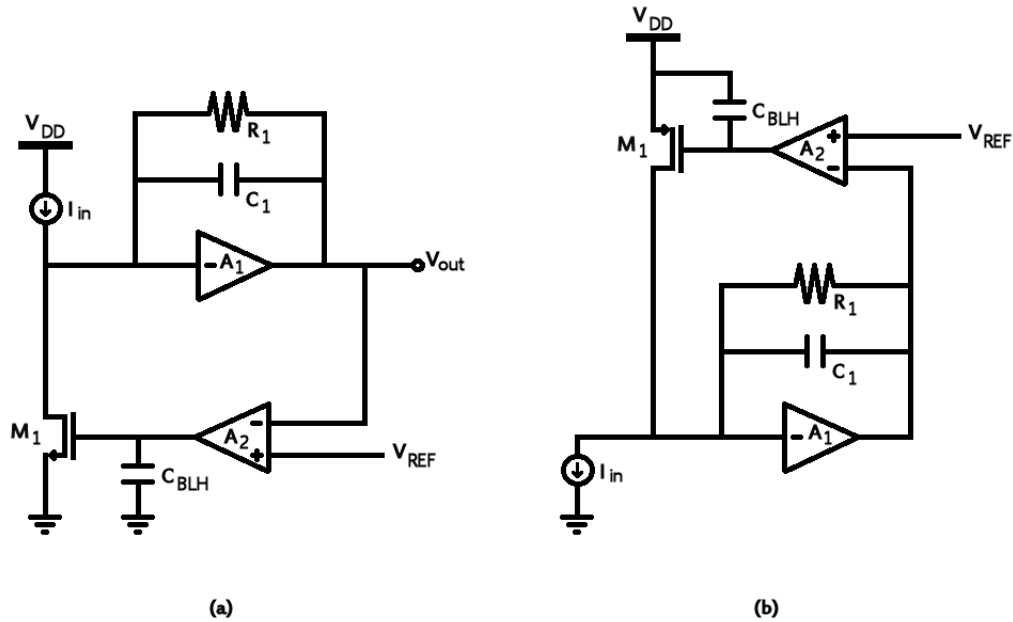


Figure 2.17: Baseline Holder: (a) implementation with nMOS; (b) implementation with pMOS.

To understand the way it works, let's consider for example the schematic (b): without the Baseline Holder a negative input current, like that drawn in Figure 2.17 (b), would flows in  $R_1$  raising the output voltage. Therefore, the input of the Baseline Holder differential amplifier, given by  $V_{BL} - V_{out}$ , decreases leading to a lower gate voltage for  $M_1$  that reacts increasing the current it pushes into the input node. Through this mechanism it is possible to hold the baseline voltage

value  $V_{BL}$ , as long as the loop gain is properly high. The Baseline Holder block can be considered as a single transconductance amplifier, with gain  $G_m = A_{d2}g_{m1}$  where  $A_{d2}$  is the differential voltage gain of  $A_2$  and  $g_{m1}$  is the transconductance of  $M_1$ . At this point we can proceed with a more quantitative analysis. Let's suppose that  $A_2$  has a transfer function like the following one:

$$A_{d2}(s) = \frac{(A_{d2})_0}{1 + s\tau_2} \quad (2.29)$$

The capacitor  $C_{BLR}$  is necessary to limit the differential stage bandwidth since we want only low frequency signals to be processed by the additional feedback loop. The Baseline Holder gain  $G_m$  can be rewritten exploiting the transfer function expression:

$$G_m(s) = A_{d2}(s)g_{m1} = \frac{(A_{d2})_0 g_{m1}}{1 + s\tau_2} = \frac{G_{m0}}{1 + s\tau_2} \quad (2.30)$$

where  $G_{m0}$  is the overall low frequency transconductance gain. A first assumption that simplifies the study of the circuit is  $\tau_2 \gg \tau_1 = R_1C_1$  since in this case we can neglect the capacitive part of the feedback impedance of  $A_1$  and consider only the resistive one. Considering the input node of  $A_1$  as a virtual ground, the input node equation can be written as:

$$I_{in} + \frac{V_{BL} - V_{out}}{R_1} - I_{BLH} = 0 \implies I_{in} = I_{BLH} + \frac{V_{out}}{R_1} \quad (2.31)$$

The  $I_{BLH}$  current of the Baseline Holder can be written as:

$$I_{BLH} = G_m V_{out} \quad (2.32)$$

leading to the input-output relationship of the circuit that is reported below:

$$\begin{aligned} \frac{V_{out}}{I_{in}} &= \frac{R_1}{1 + G_m R_1} = \frac{R_1}{1 + \frac{G_{m0} R_1}{1 + s\tau_2}} = \frac{R_1}{1 + G_{m0} R_1} \frac{1 + s\tau_2}{1 + s \frac{\tau_2}{1 + G_{m0} R_1}} = \\ &= \frac{R_1}{1 + G_{m0} R_1} \frac{1 + s\tau_2}{1 + s\tau_{BLH}} \end{aligned} \quad (2.33)$$

with

$$\tau_{BLH} = \frac{\tau_2}{1 + G_{m0} R_1} \quad (2.34)$$

that represents the pole introduced by the Baseline Holder. It's interesting to observe that in the case  $s = 0$ , that is the low frequency case, the above expression turns into the following one:

$$\frac{V_{out}}{I_{in}} = \frac{R_1}{1 + G_{m0}R_1} \quad (2.35)$$

To appreciate the task performed by the Baseline Holder, it's necessary to make a numerical example: assuming that  $R_1 = 100k\Omega$ ,  $g_{m1} = 100\mu S$  and  $(A_{d2})_0 = 10000$  the low frequency gain is equal to  $1\Omega$  and it means that a DC input variation of  $1\mu A$  produces a change in the output voltage of  $1\mu V$  rather than the  $100mV$  obtained without the additional feedback. For  $s > 0$  the zero at the frequency  $f_2 = \frac{1}{2\pi\tau_2}$  produce a rising edge with a slope of 20dB/decade until the pole at  $f_{BLH} = \frac{1}{2\pi\tau_{BLH}}$  is found. Above the pole frequency, we can use the approximation  $G_{m0}R_1 \gg 1$ , so the gain expression can be written as:

$$\frac{V_{out}}{I_{in}} \approx \frac{R_1}{G_{m0}R_1} \frac{s\tau_2}{\frac{s\tau_2}{1+G_{m0}R_1}} = R_1 \quad (2.36)$$

This result shows that high frequency signals are amplified by  $R_1$ . This separation in frequency is really important since the  $G_m$  feedback have to compensate only the undesired DC, or close to DC, components. The last study we are interested to do regards the Baseline Holder response to a sudden change in the input DC current. Representing the current variation in the Laplace domain as  $I_{in}(s) = \frac{I_{in0}}{s}$ , that is the Laplace transformation of a step in the time domain, and neglecting the time constant  $\tau_1 = R_1C_1$ , the transfer function of the circuit is:

$$V_{out}(s) = \frac{I_{in0}}{s} \frac{R_1}{1 + G_{m0}R_1} \frac{1 + s\tau_2}{1 + s\tau_{BLH}} \quad (2.37)$$

that corresponds to a signal in the time domain like the following one:

$$V_{out}(t) = \frac{R_1 I_{in0}}{1 + G_{m0}R_1} \left[ \left( \frac{\tau_2 - \tau_{BLH}}{\tau_{BLH}} \right) e^{-\frac{t}{\tau_{BLH}}} + 1 \right] \quad (2.38)$$

Considering the case with  $\tau_2 \gg \tau_{BLH}$  the above relationship becomes:

$$V_{out}(t) \approx I_{in0} \left( R_1 e^{-\frac{t}{\tau_{BLH}}} + \frac{R_1}{1 + G_{m0}R_1} \right) \quad (2.39)$$

that shows well that for  $t = 0$  is fully amplified by  $R_1$ . Then the first term decays exponentially to zero with  $\tau_{BLH}$  as time constant, obtaining the already studied suppressed DC gain represented by the second term. Therefore  $\tau_{BLH}$  defines the time-scale that the system needs to recover the baseline value after a sudden input change. Another important consideration regards the DC loop gain  $G_{m0}R_1$  that defines both the position of the pole, through  $\tau_{BLH}$ , and the low frequency attenuation. In a more realistic case we have to consider the contribution of the

feedback capacitance  $C_1$ , so that the transfer function turns into the following expression:

$$\frac{V_{out}}{I_{in}} = \frac{R_1 (1 + s\tau_2)}{s^2\tau_1\tau_2 + s(\tau_1 + \tau_2) + 1 + G_{m0}R_1} \quad (2.40)$$

obtained replacing  $R_1$  with the complex impedance

$$Z_1 = \frac{R_1}{1 + sR_1C_1} = \frac{R_1}{1 + s\tau_1} \quad (2.41)$$

The first important observation is that we have a second order transfer function, this means that in principle it could contains also complex poles leading to the circuit instability. To avoid this possible issue we need to impose that:

$$(\tau_1 + \tau_2)^2 > 4\tau_1\tau_2(1 + G_{m0}R_1) \quad (2.42)$$

Supposing that  $\tau_2 \gg \tau_1$  and  $G_{m0}R_1 \gg 1$  the above condition becomes:

$$\tau_2 > 4\tau_1G_{m0}R_1 \quad (2.43)$$

that gives a relationship between the low frequency time constant  $\tau_2$ , the shaping time constant  $\tau_1$  and the loop gain  $G_{m0}R_1$ . Such a structure offers two main advantages with respect to the use of a simple capacitance to perform the AC coupling: the cut-off frequency can be set by a proper chose of the current to be injected in the differential stage or by sizing the capacitor  $C_{BLH}$ ; moreover we can lock the output DC voltage in order to exploit the full dynamic range and to couple this stage with the following ones. A drawback of this architecture is that since the transfer function of the stage shows that it works like a high-pass filter, an undershoot occurs when it is driven by unipolar signals leading to the already discussed phenomenon of the baseline drift. The solution consists in an additional non-linear network providing a severe slew-rate limitation [7], made by a unity gain buffer dumped by a capacitor at the output (Figure 2.18), whose purpose is to distinguish between fast pulses (which must be left unaffected by the Baseline Holder) and slow variations (that we need to compensate through the Baseline Holder).

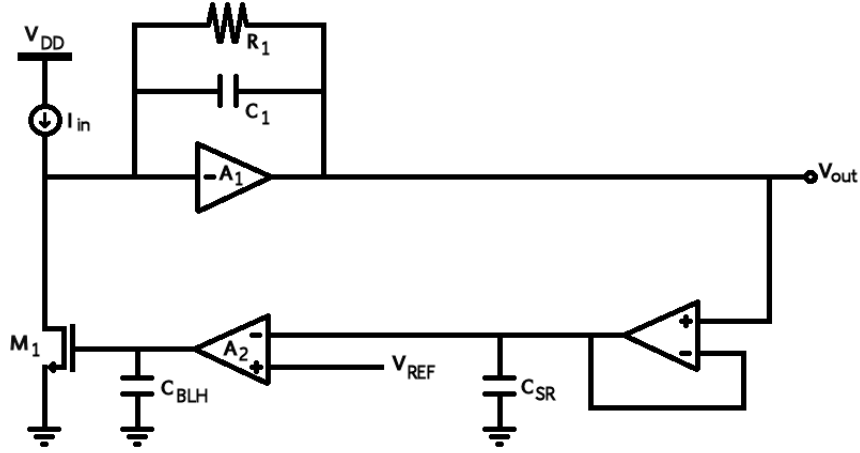


Figure 2.18: Baseline Holder with slew-rate limitation.

### 2.3.2 Sensor signal variation effects

Depending on the detector size and geometry, the signal produced by an hitting particle may have a quite complicated shape since the charge collection time is finite. A simple, but still significant, example useful to understand the effects of sensor signal shape consists in the use of an input current pulse that follows an exponential law, such as the one reported below:

$$I_{in}(t) = I_0 e^{-\frac{t}{\tau_c}} \quad (2.44)$$

In this case, the total charge delivered by the pulse will be:

$$Q_{in} = \int_0^{\infty} I_0 e^{-\frac{t}{\tau_c}} dt = I_0 \tau_c \quad (2.45)$$

where  $I_0$  is the peak current and  $\tau_c$  is the time constant representing the charge collection time. The Laplace transform of such a current pulse is given by:

$$I_{in}(s) = \frac{I_0 \tau_c}{1 + s \tau_c} \quad (2.46)$$

The transfer function of a CR-RC shaper considering that the input is not anymore a Dirac  $\delta$ -like pulse becomes:

$$V_{out}(s) = \frac{I_0 \tau_c}{C_f (1 + s \tau_c)} \cdot \frac{\tau}{(1 + s \tau)^2} \quad (2.47)$$

The signal expression in the time domain will be:

$$V_{out}(t) = \frac{Q_{in}}{C_f} \left[ \frac{t}{\tau - \tau_c} e^{-\frac{t}{\tau}} + \frac{\tau_c}{(\tau - \tau_c)^2} \left( e^{-\frac{t}{\tau_c}} - e^{-\frac{t}{\tau}} \right) \right] \quad (2.48)$$

An interesting analysis can be performed by sweeping  $\tau_c$  adjusting  $I_0$  in order to have  $Q_{in} = const$ . Figure 2.19 shows that the circuit response when  $\tau_c \ll \tau$  is the same observed with a  $\delta$ -like input pulse, in fact the signal expression can be approximated as  $V_{out}(t) \approx \frac{Q_{in}}{C_f} \left( \frac{t}{\tau} \right) e^{-\frac{t}{\tau}}$  that is the result we obtained in the ideal case, but as  $\tau_c$  increases we can see that the peaking time gets longer and the signal amplitude falls down.

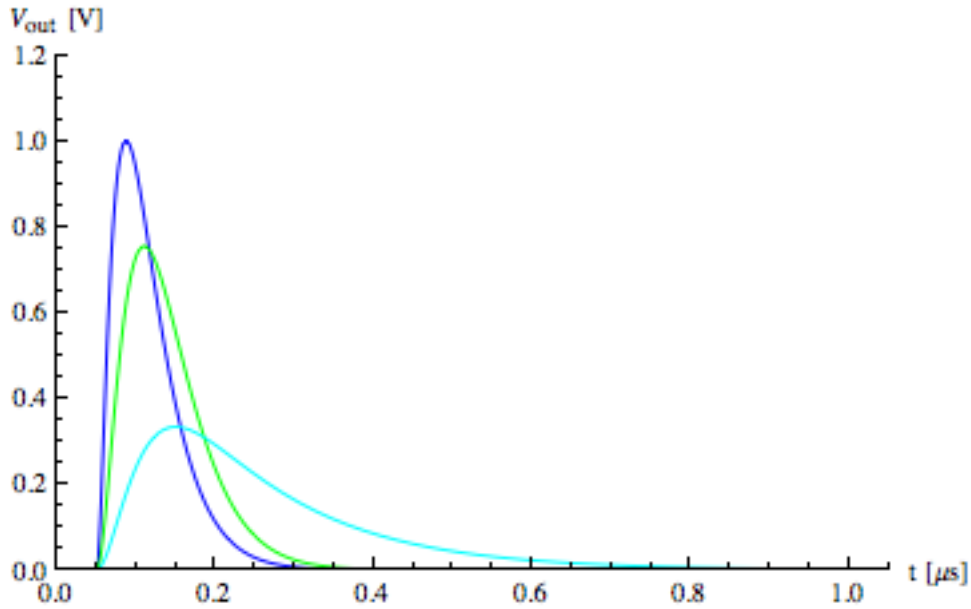


Figure 2.19: Response of a CR-RC shaper with  $T_p = 30ns$  to exponential current pulses with different collection times.

We are in presence of a form of ballistic deficit that is an amplitude loss occurring whenever two different mechanisms compete with each other with comparable speed: the signal formation and the reset of the system. It is really important to notice that this effect has been obtained considering a fully noiseless front-end. As we can observe in the Figure 2.20, a solution to this issue is to increase the shaping time  $\tau$ , but the price to pay is the worsening of the circuit rate capability.



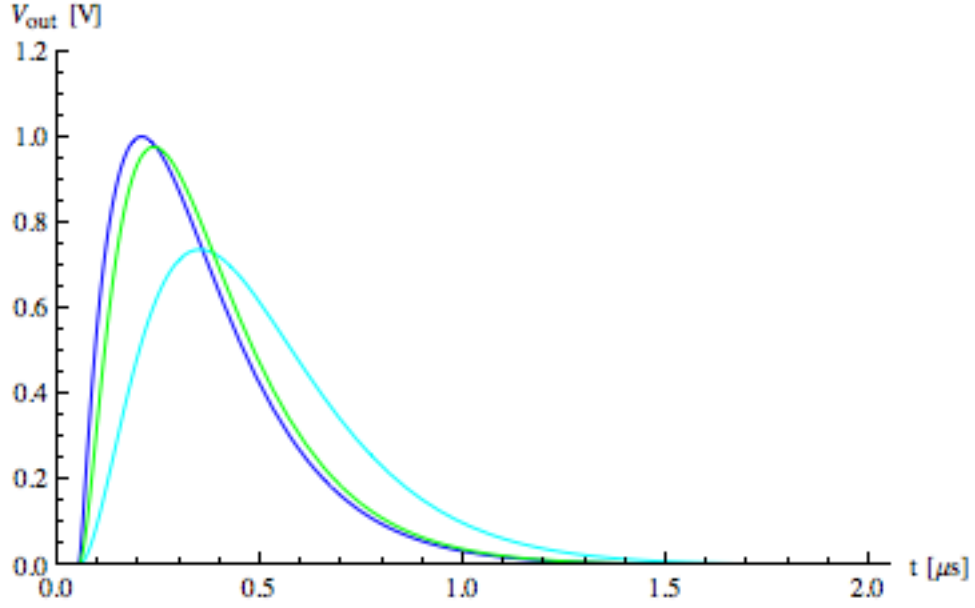


Figure 2.20: Response of a CR-RC shaper with  $T_p = 150ns$  to exponential current pulses with different collection times.

However, we have seen in the previous section that increasing the order of the shaper allows to have bigger peaking time maintaining a restrained signal duration and this is well proved observing the Figure 2.21. The graphic of Figure 2.22 compares the modifications of the pulse responses of a simple CR-RC and a CR-RC<sup>5</sup> shaper in presence of ballistic deficit due to an exponential current pulse input delivering the same charge with a fixed charge collection time  $\tau_c$ : we can notice that with high order filters the signal amplitude loss is smaller [2].

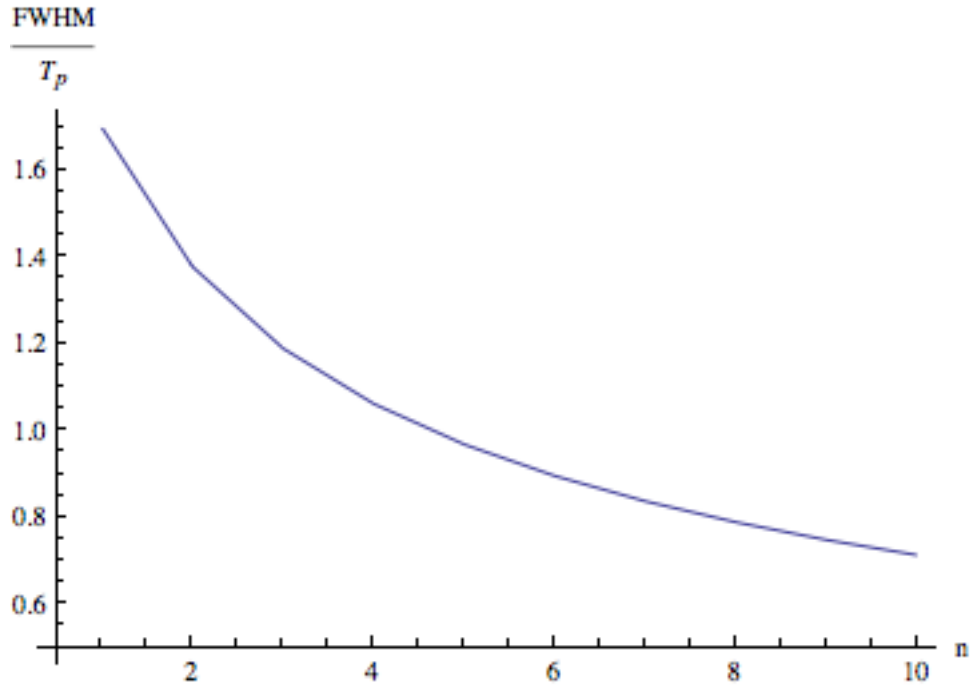


Figure 2.21: Ratio between the pulse width and  $T_p$  for shapers of different orders (in this case we assumed  $T_p = \tau_c = 30ns$ ).

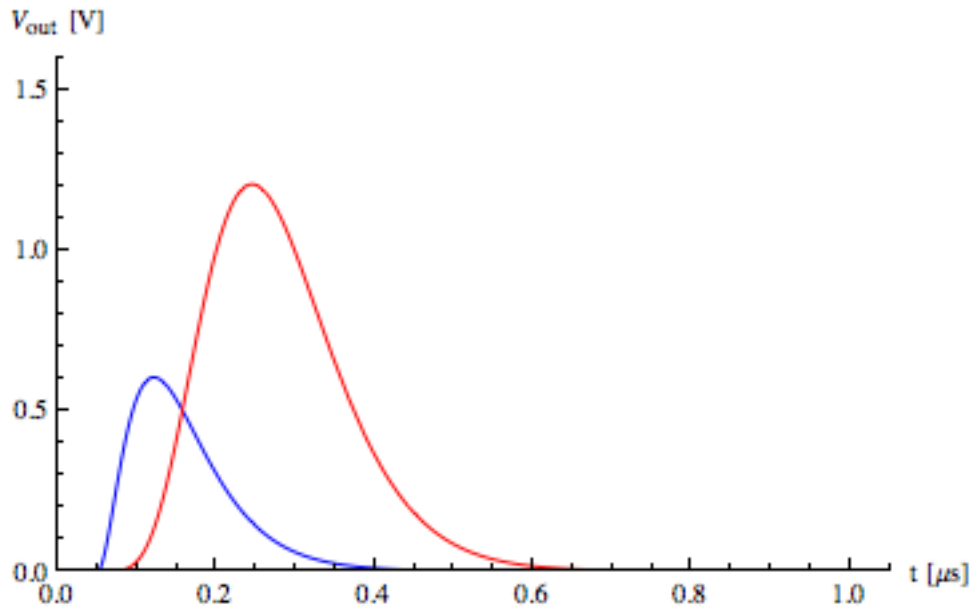


Figure 2.22: Comparison between the response of a CR-RC and a  $CR-(RC)^5$  shapers with  $T_p = 30ns$  to exponential current pulses with  $\tau_c = 50ns$ .

There is one more issue related to shape variations in the detector signal depending on the fact that these have a statistic nature. The charge collection time changes on an event by event basis, therefore the same deposited charge may generate signals with different shape and peaking time. A possible solution consists into sampling and integrating the full waveform exploiting the possibility to obtain the output voltage  $V_{out}(t)$  applying the convolution theorem:

$$V_{out}(t) = I_{in}(t) * h(t) = \int_{-\infty}^{\infty} I_{in}(u)h(t-u)du \quad (2.49)$$

where  $h(t)$  is the system response to a  $\delta$ -like pulse. Now we need to calculate the integral of the output signal:

$$\begin{aligned} \int_{-\infty}^{\infty} V_{out}(t) dt &= \int_{-\infty}^{\infty} I_{in}(t) * h(t) dt = \int_{-\infty}^{\infty} \left[ \int_{-\infty}^{\infty} I_{in}(u)h(t-u)du \right] dt = \\ &= \int_{-\infty}^{\infty} I_{in}(u) \left[ \int_{-\infty}^{\infty} h(t-u)dt \right] du \end{aligned} \quad (2.50)$$

The above integral can be further processed to obtain

$$\int_{-\infty}^{\infty} V_{out}(t) dt = \left[ \int_{-\infty}^{\infty} I_{in}(u)du \right] \left[ \int_{-\infty}^{\infty} h(t)dt \right] = Q_{in} \int_{-\infty}^{\infty} h(t)dt \quad (2.51)$$

which proves that integrating the output signal give us an information about the total charge.

### 2.3.3 Gain and bandwidth limitations in CSAs

The last case we need to discuss regards the effects of a charge sensitive amplifier with limited gain and bandwidth.

#### 2.3.3.1 Effects of finite gain

For our purpose, we can study the effects of a finite gain of the CSA neglecting the contribution of the feedback resistor  $R_f$ . When an amplifier has a finite gain  $A_0$ , the input node cannot be considered anymore as a virtual ground, so that the nodal equation for the input is:

$$I_{in} + V_{in}sC_{det} + [V_{in} - V_{out}]sC_f = 0 \quad (2.52)$$

and since  $V_{out} = -A_0V_{in} \iff V_{in} = -\frac{V_{out}}{A_0}$ , the input-output relationship is:

$$\frac{V_{out}}{I_{in}} = -\frac{A_0}{s[C_{det} + (1 + A_0)C_f]} \quad (2.53)$$

In order to obtain the ideal transfer function of such a state, we need to impose 2 conditions:

- $A_0 \gg 1$
- $(1 + A_0)C_f \gg C_{det}$

The Miller theorem allows to split the feedback capacitance  $C_f$  into a capacitance  $C_{f(in)} = (1 + A_0)C_f$  connected between the input node and the ground, and a capacitance  $C_{f(out)} = \left(1 + \frac{1}{A_0}\right)C_f$  between the output and the ground. This gives us an interpretation of the second condition, in fact  $C_{det}$  and  $C_{f(in)}$  are connected in parallel, so that the input charge will be:

$$Q_{in} = Q_{det} + Q_{f(in)} = V_{in} (C_{det} + C_{f(in)}) \quad (2.54)$$

However only  $Q_{f(in)}$  contributes to the signal and that means that the charge  $Q_{det}$  is lost to further processing. Moreover in a multichannel system the capacitance  $C_{det}$  can be seen as the combination of a capacitance  $C_{det(gnd)}$  connected to the ground and an inter-channel capacitance  $C_{det(ch)}$  creating a path between the input node and the two adjacent channels (Figure 2.23) leading to the cross-talk phenomenon.

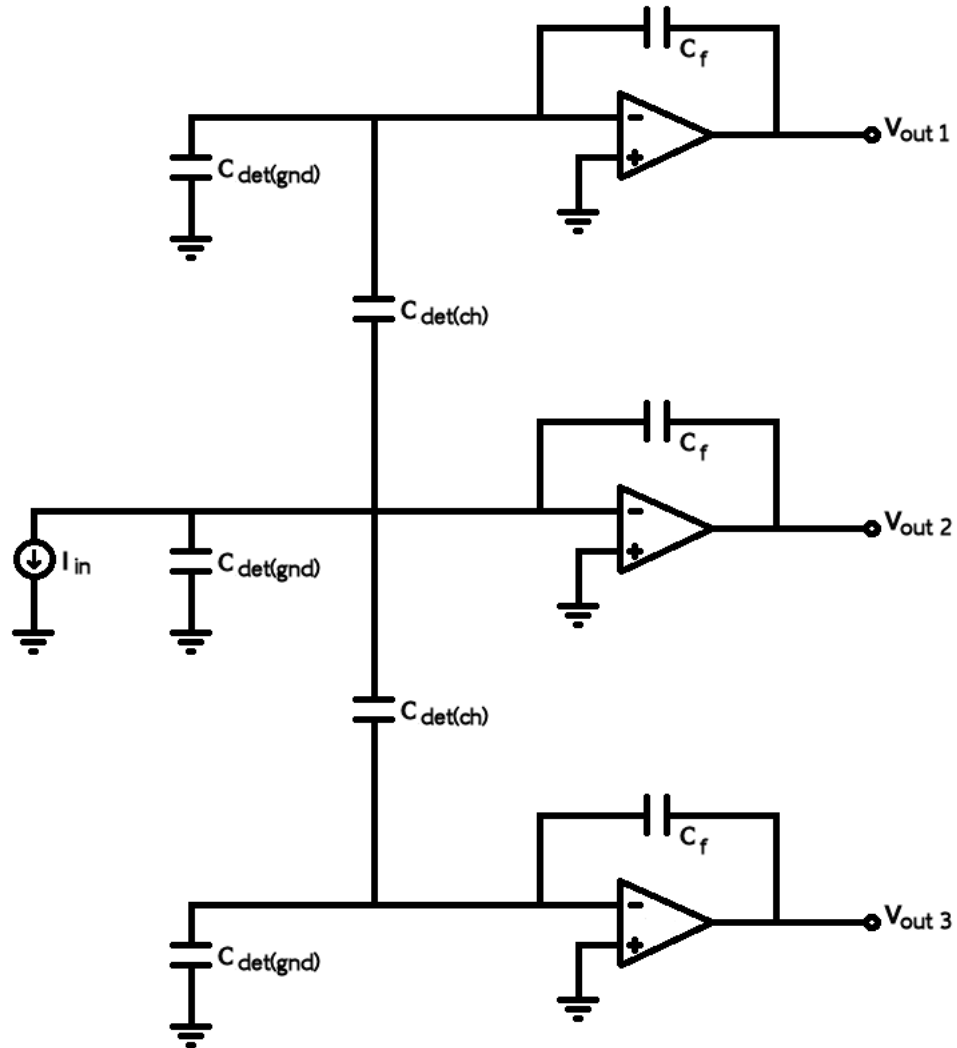


Figure 2.23: Cross-talk between a channel and the two adjacent one.

### 2.3.3.2 Effects of bandwidth limitation

Even in this case, we can neglect the contribution of the feedback resistor. As CSA we can use the model of a simple transistor, so that the small signal equivalent will be that represented in Figure 2.24 where  $R_L$  and  $C_L$  are the equivalent load resistance and capacitance, respectively.

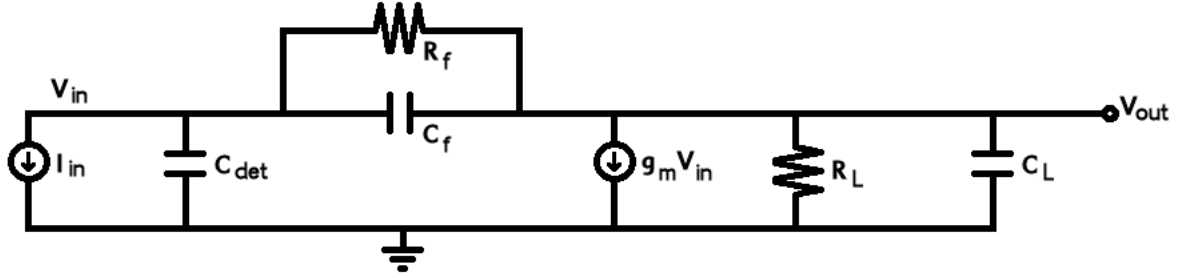


Figure 2.24: Small signal equivalent circuit of a CSA.

To obtain the transfer function we need to solve the following system:

$$\begin{cases} I_{in}(s) + V_{in}(s)sC_{det} + [V_{in}(s) - V_{out}(s)]sC_f = 0 \\ g_m V_{in}(s) + [V_{out}(s) - V_{in}(s)]sC_f + V_{out}(s)\left(\frac{1}{R_L} + sC_L\right) = 0 \end{cases} \quad (2.55)$$

Considering the case with  $R_L \rightarrow \infty$ , the system transfer function will be:

$$V_{out}(s) = -\frac{I_{in}(s)\left(1 - s\frac{C_f}{g_m}\right)}{sC_f(1 + s\tau_r)} \quad (2.56)$$

where

$$\tau_r = \frac{C_L C_{det} + (C_L + C_{det})C_f}{g_m C_f} \quad (2.57)$$

is the rise time constant. The response to a  $\delta$ -like input current in the time domain is given by:

$$V_{out}(t) = -\frac{Q_{in}}{C_f} \left(1 - e^{-\frac{t}{\tau_r}}\right) \quad (2.58)$$

To better understand the effects of bandwidth limitation, we need to consider two different cases.

### 1. $C_f \gg C_L$

In this case we have that  $\tau_r \approx \frac{C_L + C_{det}}{g_m}$  and assuming to have  $C_{det} \gg C_L$  we can further simplify the expression obtaining  $\tau_r \approx \frac{C_{det}}{g_m}$ . It is important to observe that the speed of the signal is weakly sensitive to the value of  $C_f$  and mainly depends on  $C_{det}$ .

## 2. $C_f \ll C_L$

Here we have that  $\tau_r \approx \frac{C_L C_{det}}{g_m C_f}$  so that the signal speed is limited by the ratio  $\frac{C_{det}}{C_f}$ .

For both cases we can observe that limiting the CSA bandwidth leads to an output signal that is not anymore an ideal step reaching the value  $\frac{Q_{in}}{C_f}$  in a null time, but it takes a time  $\tau_r$  to get to that level. In a more realistic case we cannot neglect the feedback resistor  $R_f$  and the transfer function turns into the following expression:

$$V_{out}(s) = \frac{I_{in}(s)R_f}{(1 + s\tau_r)(1 + s\tau_f)} \quad (2.59)$$

valid under the assumption that

$$\tau_f = R_f C_f \gg \frac{C_L + C_{det}}{g_m} \quad (2.60)$$

The pulse response in the time domain is then:

$$V_{out}(t) = \frac{Q_{in}}{C_f} \frac{\tau_f}{\tau_r - \tau_f} \left( e^{-\frac{t}{\tau_r}} - e^{-\frac{t}{\tau_f}} \right) \quad (2.61)$$

Solving the equation

$$\frac{\partial V_{out}(t)}{\partial t} = 0 \quad (2.62)$$

we can find the signal peaking time:

$$T_p = \frac{\tau_r \tau_f}{\tau_r - \tau_f} \ln \left( \frac{\tau_r}{\tau_f} \right) \quad (2.63)$$

In the end, we can evaluate  $V_{out}(T_p)$  obtaining:

$$V_{out,max} = \frac{Q_{in}}{C_f} \left( \frac{\tau_f}{\tau_r} \right)^{\frac{\tau_r}{\tau_r - \tau_f}} \quad (2.64)$$

So the step amplitude is modulated by a term depending on the ratio between the feedback time constant  $\tau_f$  and the signal rise time  $\tau_r$ . To have an idea of what kind of modulation are we talking about, if  $\frac{\tau_f}{\tau_r} = 100$  the signal amplitude attains 95.4% of its theoretical value and 99.3% if  $\frac{\tau_f}{\tau_r} = 1000$  (Figure 2.25). This amplitude loss is another example of ballistic deficit, but in this case it is the finite CSA bandwidth that limits the signal formation time rather than the detector.

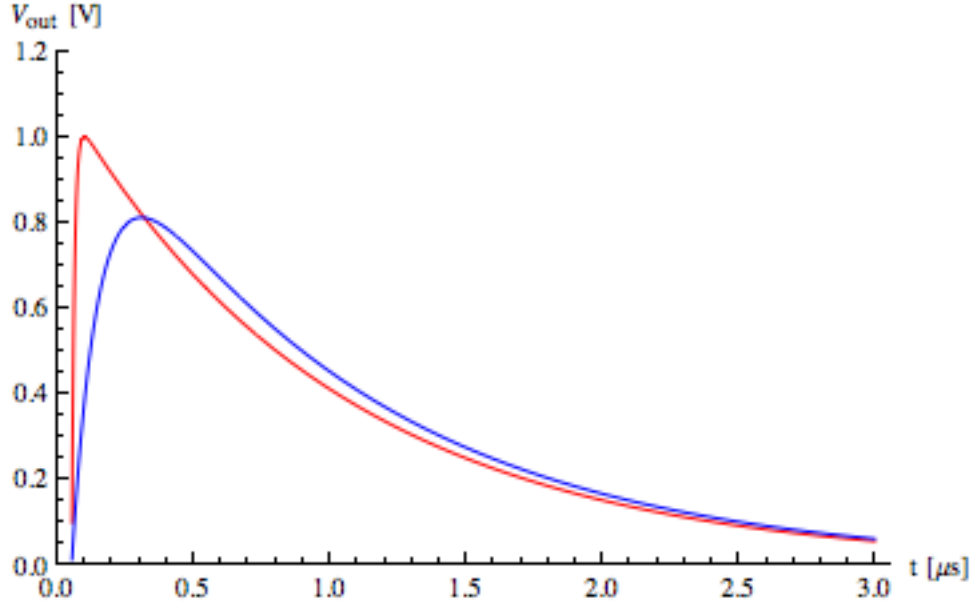


Figure 2.25: Response of a CSA with finite rise time constant with  $\tau_f = 1\mu s$  in the case of  $\tau_r = 100ns$  (blue curve) and  $\tau_r = 10ns$  (red curve).

## 2.4 Noise calculations

A key parameter in the design of a front-end for physics detectors is the noise of the system expressed through the Equivalent Noise Charge. The ENC is the number of electrons one would have to collect from a silicon sensor in order to create a signal whose peak corresponds to the rms noise of this sensor. The first step to obtain such an information is to identify the noise sources of the system under analysis and to model them with voltage or current generators. It is usual to refer to a noise source modeled with a voltage generator as “series noise”, and as “parallel noise” if we are in presence of a current noise source. The ENC can be expressed through the following expression:

$$ENC = \frac{V_{n(out),rms}}{V_{peak}(Q_{in} = q)} \Rightarrow [ENC] = \text{number of electrons} \quad (2.65)$$

where  $q = 1.6022 \cdot 10^{-19}C$  is the elementary charge corresponding to 1 electron. So, if we want to evaluate the ENC, we have to calculate the  $V_{n(out),rms}$  that is given by:

$$V_{n(out),rms}^2 = \int_0^\infty S_n^2 * |T_n(j\omega)|^2 d\omega \quad (2.66)$$



with  $S_n^2$  representing the power spectral density associated to a certain noise source, while  $T_n(j2\pi f) = \frac{V_{n(out)}}{V_{n(in)}}$  so that this transfer function might not coincide with the signal transfer function. If we are in presence of more uncorrelated noise sources, the total rms noise is obtained using the expression below:

$$V_{n(out),rms}(tot) = \sqrt{V_{n(out),rms}^2(1) + V_{n(out),rms}^2(2) + \dots + V_{n(out),rms}^2(N)} \quad (2.67)$$

It is important to notice that all our considerations take into account a system whose output is a voltage, however the method does not change in the case of a system with a current as output.

### 2.4.1 Noise sources in a front-end amplifier

Figure 2.26 shows a front-end amplifier with the equivalent noise generators representing the effects due to different kind of noise. It is important to notice that the voltage noise sources  $V_{nW}^2$  e  $V_{nF}^2$ , representing the white and the flicker noise respectively, are connected between the input and the output of the CSA (through the feedback path) since they are part of the core amplifier itself.

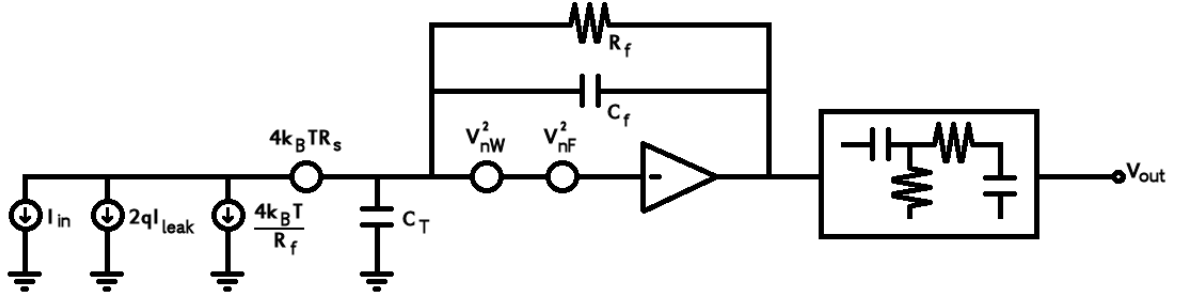


Figure 2.26: Noise sources in a front-end amplifier.

The generator who plays the role of the white noise can be split into several contributors:

- White noise due to the amplifier input transistor:

$$V_{nW1}^2 = 4k_B T \frac{1}{g_{m1}} \Gamma \quad (2.68)$$

where  $k_B$  is the Boltzmann constant,  $T$  is the absolute temperature,  $g_{m1}$  is the transconductance of the input transistor and  $\Gamma$  is the inversion coefficient that depends on the biasing region of the device.

- White noise due to the parasitic resistance of the gate of the input transistor and any internal resistor in series with the input (represented by  $R_{S,int}$  in the expression below):

$$V_{nW2}^2 = 4k_B T R_{S,int} \quad (2.69)$$

- White noise due to the current source biasing the input stage:

$$V_{nW3}^2 = 4k_B T \frac{g_{m2}}{g_{m1}^2} \Gamma \quad (2.70)$$

where  $g_{m2}$  is the transconductance of the transistor providing the bias for the input stage.

The expression for the flicker noise, that is the other term representing a noise contribution generated by the amplifier itself, is reported below:

$$V_{nF}^2 = \frac{K_f}{C_{ox} W L} \frac{1}{f} \quad (2.71)$$

where  $K_f$  is a constant for a given device gate length and bias condition,  $C_{ox}$ ,  $W$  and  $L$  are respectively the capacitance of the oxide layer, the width and the length of the input transistor gate, while  $f$  is the frequency of the input signal.

The last series noise source is given by the following expression:

$$V_{nR_S}^2 = 4k_B T R_S \quad (2.72)$$

where  $R_S$  represents the contribution due to any external resistance connected in series to the input stage.

As regards the parallel noise sources, modeled as current generators connected in parallel with the input current pulse representing the sensor signal, the main contributions are:

- Parallel noise due to the feedback resistor  $R_f$  of the CSA:

$$I_{nR_f}^2 = \frac{4k_B T}{R_f} \quad (2.73)$$

it is important to notice that the greater is  $R_f$ , the lower will be its contribution to the noise of the system.

- Parallel noise introduced by any additional current source directly connected to the input stage:

$$I_{nDC}^2 = 4k_B T g_{mDC} \Gamma \quad (2.74)$$

where  $g_{mDC}$  is the transconductance of the transistor implementing the current source providing the DC path to the sensor leakage current or the biasing of the active feedback network in the input stage.

These two terms refer to devices of the front-end amplifier, we have now to describe the contributions to the noise of the system given by the sensor and its biasing network:

- Parallel noise due to the detector leakage current who plays a key role in semiconductor sensors:

$$I_{n,leak}^2 = 2qI_{leak} \quad (2.75)$$

- Noise due to the sensor bias resistance:

$$I_{n,bias}^2 = \frac{4k_B T}{R_{bias}} \quad (2.76)$$

A really important observation is that all the parallel noise sources have white spectral density. Henceforward we will combine all the white series noise sources into one unique term

$$V_{nW}^2 = V_{nW1}^2 + V_{nW2}^2 + V_{nW3}^2 \quad (2.77)$$

and all the white parallel noise sources into

$$I_n^2 = I_{n,leak}^2 + I_{n,bias}^2 \quad (2.78)$$

Moreover the Figure 2.26 shows the presence of a capacitance named  $C_T$  that is given by:

$$C_T = C_{det} + C_f + C_{in} \quad (2.79)$$

where  $C_{det}$  is the detector capacitance,  $C_f$  is the feedback capacitance and  $C_{in}$  is the amplifier input capacitance, so that  $C_T$  represents the sum of all the capacitance seen between the input node and the ground. While for the other capacitances is easy to see that are connected between those two points, it is necessary a clarification as regards  $C_f$  since we have to consider the loading effect produced by the feedback capacitor on the amplifier. According to all these hypothesis, the following subsections will show the analytical calculations of all the main noise contributors for a simple CR-RC shaper generalizing later the results to higher order filters.

### 2.4.2 Noise in a CR-RC shaper

The first contribution we want to study is that of the white series noise corresponding to the voltage generator  $V_{nW}^2$ . The noise voltage is converted into a current by the capacitance  $C_T$  and this current is integrated on the feedback capacitance  $C_f$ :

$$V_{nW(CSA)}^2 = V_{nW}^2 \left( \frac{C_T}{C_f} \right)^2 \quad (2.80)$$

This voltage is then processed by the CR-RC shaper transfer function reported below:

$$T(s) = \frac{s\tau}{(1 + s\tau)^2} \quad (2.81)$$

According to what we have seen in the previous subsection, we need to make an integration in the frequency domain putting  $s = j\omega \rightarrow \tau = \frac{1}{\omega_0}$ . Using this formalism, that is exactly the same if we use the frequency  $f$  rather than the angular frequency  $\omega$ , the shaper transfer function becomes:

$$T(j\omega) = \frac{j\frac{\omega}{\omega_0}}{\left(1 + j\frac{\omega}{\omega_0}\right)^2} \quad (2.82)$$

and the noise voltage at the end of the shaper is thus given by:

$$\begin{aligned} V_{nW(out),rms}^2 &= \frac{1}{2\pi} \int_0^\infty V_{nW(CSA)}^2 * |T(j\omega)|^2 d\omega = \\ &= \frac{1}{2\pi} V_{nW}^2 \left( \frac{C_T}{C_f} \right)^2 \int_0^\infty \frac{\omega^2}{\left(\omega_0 - \frac{\omega^2}{\omega_0}\right)^2 + 4\omega^2} d\omega = \frac{1}{8} V_{nW}^2 \left( \frac{C_T}{C_f} \right)^2 \omega_0 \end{aligned} \quad (2.83)$$

It is also possible to express the above result as a function of the peaking time  $T_p$ , in fact:

$$\left\{ \begin{array}{l} T_p = \tau \\ \tau = \frac{1}{\omega_0} \end{array} \right\} \parallel \Rightarrow \omega_0 = \frac{1}{T_p} \quad (2.84)$$

leading to the following relationship:

$$V_{nW(CSA),rms}^2 = \frac{1}{8} V_{nW}^2 \left( \frac{C_T}{C_f} \right)^2 \frac{1}{T_p} \quad (2.85)$$

Whereas we aim at calculating the ENC, we need the expression of  $V_{peak}(q)$  that in the case of a CR-RC shaper is, as seen in Section 2.2, given by:

$$V_{peak}(q) = \frac{q}{C_f} \frac{1}{e} \quad (2.86)$$

and finally we obtain:

$$ENC_W = \frac{V_{nW} C_T}{q} \sqrt{\frac{e^2}{8} \frac{1}{T_p}} \quad (2.87)$$

The main observation is that  $ENC_W \propto C_T \cdot \sqrt{\frac{1}{T_p}}$ , meaning that the  $ENC$  due to white noise increases linearly with the total capacitance  $C_T$  and decreases with the square root of the peaking time. The next step is to evaluate the flicker noise whose spectral density is:

$$V_{nF}^2 = \frac{A_f}{f} \quad (2.88)$$

This noise voltage source gives as output of the CSA the following expression:

$$V_{nF(CSA)}^2 = \frac{A_f}{f} \left( \frac{C_T}{C_f} \right)^2 = 2\pi \frac{A_f}{\omega} \left( \frac{C_T}{C_f} \right)^2 \quad (2.89)$$

Repeating what we have done before we obtain:

$$V_{nF(out),rms}^2 = \frac{1}{2\pi} A_f \left( \frac{C_T}{C_f} \right)^2 \int_0^\infty \frac{2\pi}{\omega} \frac{\omega^2}{\left( \omega_0 - \frac{\omega}{\omega_0} \right)^2 + 4\omega^2} d\omega = \frac{1}{2} A_f \left( \frac{C_T}{C_f} \right)^2 \quad (2.90)$$

that divided for  $V_{peak}(q)$  gives:

$$ENC_F = \frac{C_T}{q} \sqrt{\frac{e^2}{2} A_f} \quad (2.91)$$

Even in this case the  $ENC$  increases linearly with the total capacitance  $C_T$ , but it has no connection with the peaking time  $T_p$ . The last step is to estimate the contribution of the parallel noise, that consists into the study of the CSA response to the input noise source  $I_n^2$  given by:

$$V_{nP(CSA)}^2 = I_n^2 \left| \frac{1}{j\omega C_f} \right|^2 = \left( \frac{I_n}{\omega C_f} \right)^2 \quad (2.92)$$

Integrating into the angular frequency domain we obtain:

$$\begin{aligned}
V_{nP(out),rms}^2 &= \frac{1}{2\pi} \left( \frac{I_n}{C_f} \right)^2 \int_0^\infty \frac{1}{\omega^2} \frac{\omega^2}{\left( \omega_0 - \frac{\omega}{\omega_0} \right)^2 + 4\omega^2} d\omega = \\
&= \frac{I_n^2}{8C_f^2} \frac{1}{\omega_0} = \frac{I_n^2}{8C_f^2} T_p
\end{aligned} \tag{2.93}$$

In the end we can write the expression of the  $ENC_P$  as before:

$$ENC_P = \frac{I_n}{q} \sqrt{\frac{e^2}{8} T_p} \tag{2.94}$$

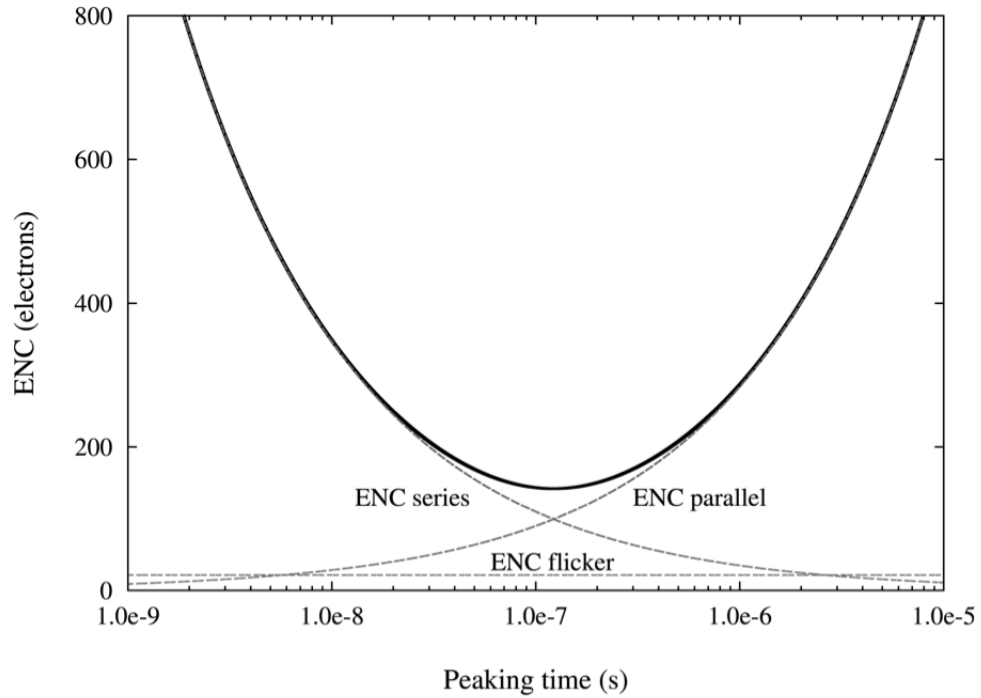
It is important to notice that  $ENC_P$  does not depend on the total input capacitance  $C_T$  and it is proportional to the square root of the peaking time  $T_p$ . Therefore, the total output noise of a simple front-end stage with a CR-RC shaper, expressed in terms of Equivalent Noise Charge is given by:

$$\begin{aligned}
ENC_{tot} &= \sqrt{ENC_W^2 + ENC_F^2 + ENC_P^2} = \\
&= \frac{V_{nW} C_T}{q} \sqrt{\frac{e^2}{8} \frac{1}{T_p}} + \frac{C_T}{q} \sqrt{\frac{e^2}{2} A_f} + \frac{I_n}{q} \sqrt{\frac{e^2}{8} T_p}
\end{aligned} \tag{2.95}$$

We observed that both the white series and the parallel noise contributions depend on the peaking time value in different ways: the first one decreases with the square root of  $T_p$ , the second one increase with the square root of  $T_p$ . Solving the following equation, it is possible to found an optimum value for this important parameter:

$$\frac{\partial ENC}{\partial T_p} = 0 \implies T_{p,opt} = \frac{V_{nW}}{I_n} C_T \tag{2.96}$$

that represents the ideal case when the two equivalent noise sources give the same contribution. This is easier to understand observing the Figure 2.27, the minimum noise is achieved at the intersection between the series and the parallel noise curves.

Figure 2.27: ENC VS  $T_p$ .

### 2.4.3 Noise in a $CR-(RC)^n$ shaper

The previous subsection can be seen as a particular case of a more generic one involving the use of  $n$  RC filters in the shaping stage [13, 11, 12]. The calculations follow exactly the same scheme, with the unique difference that the transfer function we have to use is that reported below:

$$T(s) = \frac{s\tau}{(1 + s\tau)^{n+1}} \quad (2.97)$$

As we made before, we need to express this function in terms of the angular frequency  $\omega$ :

$$T(j\omega) = \frac{j\frac{\omega}{\omega_0}}{\left(1 + j\frac{\omega}{\omega_0}\right)^{n+1}} \longrightarrow |T(j\omega)|^2 = \frac{\left(\frac{\omega}{\omega_0}\right)^2}{\left[1 + \left(\frac{\omega}{\omega_0}\right)^2\right]^{n+1}} \quad (2.98)$$

We can now work out again the results already obtained using the same noise sources. Since we want to evaluate the  $ENC$ , it is important to remember that with a  $CR-(RC)^n$  shaper the maximum value the output signal reach is given by:

$$V_{peak}(q) = \frac{q}{C_f} \frac{n^n}{n!} e^{-n} \quad (2.99)$$

### 1. White series noise

The total integrated rms noise is:

$$V_{nW(out),rms}^2 = \frac{1}{2\pi} V_{nW}^2 \left( \frac{C_T}{C_f} \right)^2 \int_0^\infty \frac{\left( \frac{\omega}{\omega_0} \right)^2}{\left[ 1 + \left( \frac{\omega}{\omega_0} \right)^2 \right]^{n+1}} d\omega \quad (2.100)$$

To solve the above integral, we need to make the following substitution:

$$\left( \frac{\omega}{\omega_0} \right)^2 = u \longrightarrow d\omega = \frac{\omega_0}{2\sqrt{u}} du \quad (2.101)$$

so we obtain:

$$V_{nW(out),rms}^2 = \frac{1}{4\pi} V_{nW}^2 \left( \frac{C_T}{C_f} \right)^2 \omega_0 \int_0^\infty \frac{u^{\frac{1}{2}}}{(1+u)^{n+1}} du \quad (2.102)$$

The solution can be found exploiting the Beta function through the expression below:

$$B(m+1, \alpha+1) = \int_0^\infty \frac{u^m}{(1+u)^{m+\alpha+2}} du \quad (2.103)$$

so the problem is reduce to the solving of the following system of equations in order to calculate the value of  $m$  and  $\alpha$ :

$$\left\{ \begin{array}{l} m = \frac{1}{2} \\ m + \alpha + 2 = n + 1 \end{array} \right\} \implies \left\{ \begin{array}{l} m = \frac{1}{2} \\ \alpha = n - \frac{3}{2} \end{array} \right. \quad (2.104)$$

Therefore we finally have:

$$V_{nW(out),rms}^2 = V_{nW}^2 \left( \frac{C_T}{C_f} \right)^2 B\left(\frac{3}{2}, n - \frac{1}{2}\right) \frac{\omega_0}{4\pi} \quad (2.105)$$

that, recalling the expression of the peaking time in the case of a shaper of generic order  $n$ , turns into:

$$V_{nW(out),rms}^2 = V_{nW}^2 \left( \frac{C_T}{C_f} \right)^2 B\left(\frac{3}{2}, n - \frac{1}{2}\right) \frac{n}{4\pi T_p} \quad (2.106)$$



Now ha we have all the elements we need, we can found the expression of the  $ENC_W(n)$  that will be given by:

$$ENC_W(n) = \frac{V_{nW}C_T}{q} \left( \frac{n!}{n^{n-\frac{1}{2}}} \right) \sqrt{\frac{e^{2n}}{4\pi T_p} B\left(\frac{3}{2}, n - \frac{1}{2}\right)} \quad (2.107)$$

## 2. Flicker noise

In this case, the total integrated rms noise is:

$$\begin{aligned} V_{nF(out),rms}^2 &= \frac{1}{2\pi} A_f \left( \frac{C_T}{C_f} \right)^2 \int_0^\infty \frac{2\pi}{\omega} \frac{\left( \frac{\omega}{\omega_0} \right)^2}{\left[ 1 + \left( \frac{\omega}{\omega_0} \right)^2 \right]^{n+1}} d\omega = \\ &= A_f \left( \frac{C_T}{C_f} \right)^2 \frac{1}{2n} \end{aligned} \quad (2.108)$$

So the final result will be:

$$ENC_F(n) = \frac{C_T}{q} \left( \frac{n!}{n^{n+\frac{1}{2}}} \right) \sqrt{\frac{e^{2n}}{2} A_f} \quad (2.109)$$

## 3. Parallel noise

In this last case, the total integrated rms noise is:

$$\begin{aligned} V_{nP(out),rms}^2 &= \frac{1}{2\pi} \left( \frac{I_n}{C_f} \right)^2 \int_0^\infty \frac{1}{\omega^2} \frac{\left( \frac{\omega}{\omega_0} \right)^2}{\left[ 1 + \left( \frac{\omega}{\omega_0} \right)^2 \right]^{n+1}} d\omega = \\ &= \frac{1}{2\pi} \left( \frac{I_n}{C_f} \right)^2 \int_0^\infty \frac{1}{\omega_0^2} \frac{1}{\left[ 1 + \left( \frac{\omega}{\omega_0} \right)^2 \right]^{n+1}} d\omega \end{aligned} \quad (2.110)$$

Operating the same substitution we made in the calculation of the white series noise, we get:

$$\begin{aligned} V_{nP(out),rms}^2 &= \frac{1}{4\pi} \left( \frac{I_n}{C_f} \right)^2 \frac{1}{\omega_0} \int_0^\infty \frac{u^{-\frac{1}{2}}}{(1+u)^{n+1}} du = \left( \frac{I_n}{C_f} \right)^2 B\left(\frac{1}{2}, n + \frac{1}{2}\right) \frac{1}{4\pi n \omega_0} = \\ &= \left( \frac{I_n}{C_f} \right)^2 B\left(\frac{1}{2}, n + \frac{1}{2}\right) \frac{T_p}{4\pi n} \end{aligned} \quad (2.111)$$

And finally we obtain the contribution of the parallel noise, that is:

$$ENC_P(n) = \frac{I_n}{q} \left( \frac{n!}{n^{n+\frac{1}{2}}} \right) \sqrt{\frac{e^{2n}}{4\pi} T_p B \left( \frac{1}{2}, n + \frac{1}{2} \right)} \quad (2.112)$$

#### 2.4.4 Noise indexes

Observing the results of our noise calculations, it is not difficult to see that all noise contributions can be expressed through a coefficient, which is specific of the particular pulse shaper used, usually called noise index. Therefore we can rewrite the results of the previous subsection using these coefficients (Table 2.1):

- White series noise  $ENC_W^2(n) = \frac{V_{nW}^2 C_T^2}{q^2} \frac{1}{T_p} N_W(n) \implies N_W(n) = \left( \frac{n!}{n^{n-\frac{1}{2}}} \right)^2 \frac{e^{2n}}{4\pi} B \left( \frac{3}{2}, n - \frac{1}{2} \right)$
- Flicker noise  $ENC_F^2(n) = \frac{A_f C_T^2}{q^2} N_F(n) \implies N_F(n) = \left( \frac{n!}{n^{n+\frac{1}{2}}} \right)^2 \frac{e^{2n}}{2}$
- Parallel noise  $ENC_P^2(n) = \frac{I_n^2}{q^2} T_p N_P(n) \implies N_P(n) = \left( \frac{n!}{n^{n+\frac{1}{2}}} \right)^2 \frac{e^{2n}}{4\pi} B \left( \frac{1}{2}, n + \frac{1}{2} \right)$

	1	2	3	4	5	6	7	8	9	10
$N_W$	0.92	0.85	0.93	1.02	1.11	1.19	1.27	1.34	1.41	1.48
$N_F$	0.92	0.64	0.52	0.45	0.40	0.36	0.34	0.31	0.30	0.28
$N_P$	3.69	3.41	3.32	3.27	3.25	3.23	3.22	3.21	3.20	3.19

Table 2.1: Noise indexes VS shaper order.

Besides these indexes allow to have more compact relationships, they are also useful to obtain a more general expression for the optimal peaking time:

$$T_{p,opt} = \frac{V_{nW}}{I_n} C_T \sqrt{\frac{N_W}{N_P}} \quad (2.113)$$

## Chapter 3

# Implementation

After this overview about the principles of a Front-End Amplifier, we can now discuss the real subject of this thesis: the implementation of a FE Amplifier for the microstrip sensors of the PANDA MVD. The first step regards the idea we want to develop, that is the method we would like to use in order to extrapolate the information of interest from the signals coming from the detector. The first part of this Chapter deal with the description of the Time over Threshold technique, that is actually the one chosen, and then we'll describe the architecture implemented to perform this kind of measure.

### 3.1 Time over Threshold technique

As its name may suggest, the Time over Threshold (ToT) is a technique based on the measure of the time a signal spends above a certain voltage threshold. The information we want to obtain from the input signals is the charge delivered by the particles that generates them. For a better comprehension of this method, we can observe the Figure 3.1 reported below.

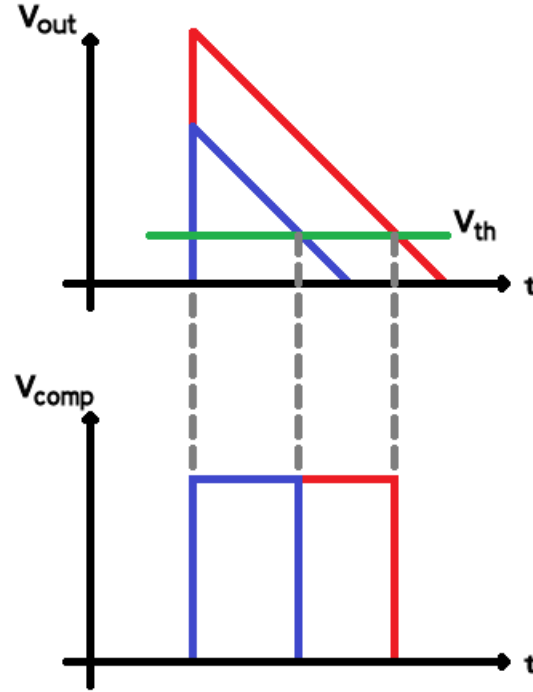


Figure 3.1: ToT principle.

We can see that the permanence of the signal above the threshold is proportional to its amplitude and thus to the charge deposited by the particle into the detector. Therefore, if we measure the two times at which the signal crosses the threshold, corresponding to the duration of the signal generated by the comparator, we can build a calibration curve binding this time with the input charge.

## 3.2 Time to Digital Converter

There are several ways to perform a ToT measure, but the one chosen involves the use of a Time to Digital Converter (TDC). This is basically due to two main factors:

- The need of a really accurate and fast time measure since one of the main constraint is the high rate capability of the microstrip sensors readout system.
- The possibility to exploit an architecture already developed by INFN [5], adapting the scheme to our purposes and thus reducing significantly the design phase time.

The architecture of the implemented TDC is shown in Figure 3.2.

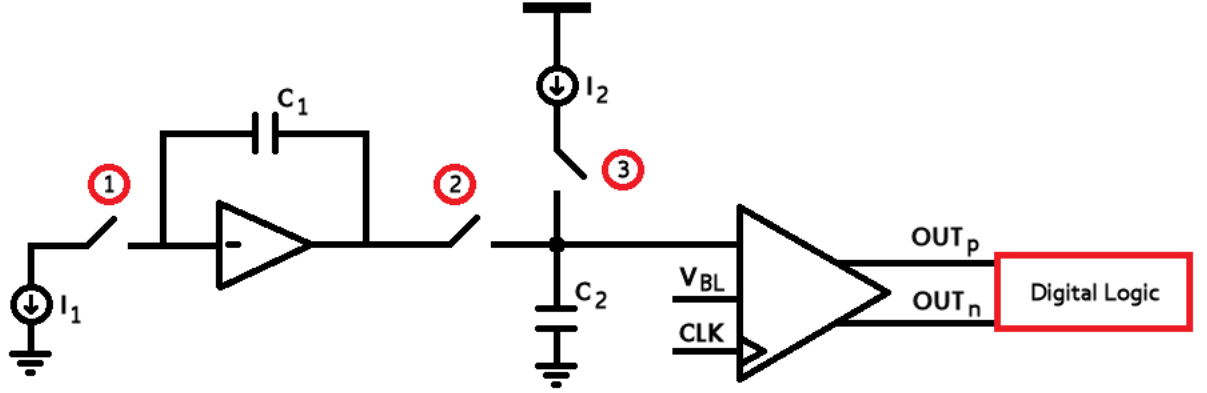
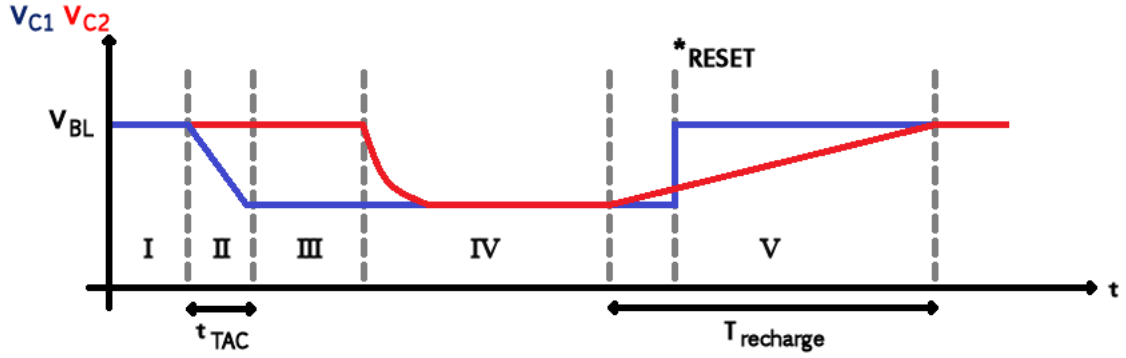


Figure 3.2: Architecture of implemented TDC.

When the comparator signal, coming from the front-end, fires, it closes the switch 1 allowing the current  $I_1$  to discharge the capacitance  $C_1$ , during a time called  $t_{TAC}$  that will be discussed later. After that, the digital logic closes the switch 2 so that the charge integrated on  $C_1$  is shared with the capacitance  $C_2$ . In the last step, the switch 2 is opened and at the same time the switch 3 is closed, the current  $I_2$  recharges  $C_2$  until the baseline voltage value is reached. The time spent during the recharge phase is given by:

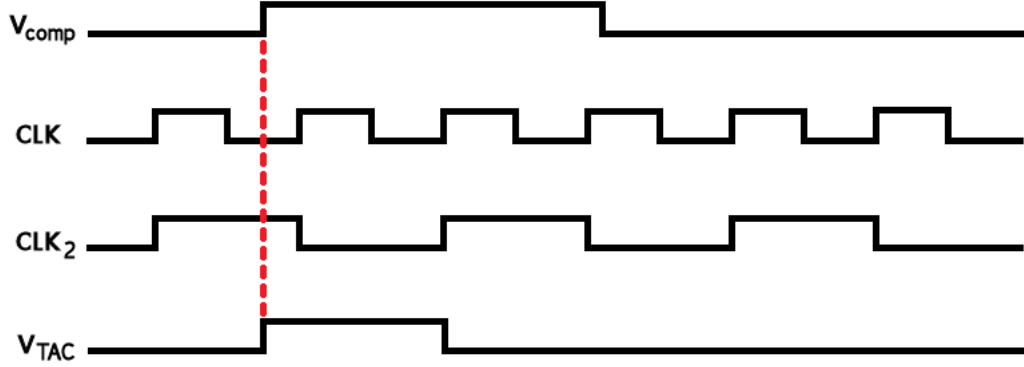
$$T_{recharge} = \frac{I_1 C_2}{I_2 C_1} t_{TAC} \quad (3.1)$$

This whole process is described in Figure 3.3 showing the voltages  $V_{C_1}$  and  $V_{C_2}$  varying with respect to time.

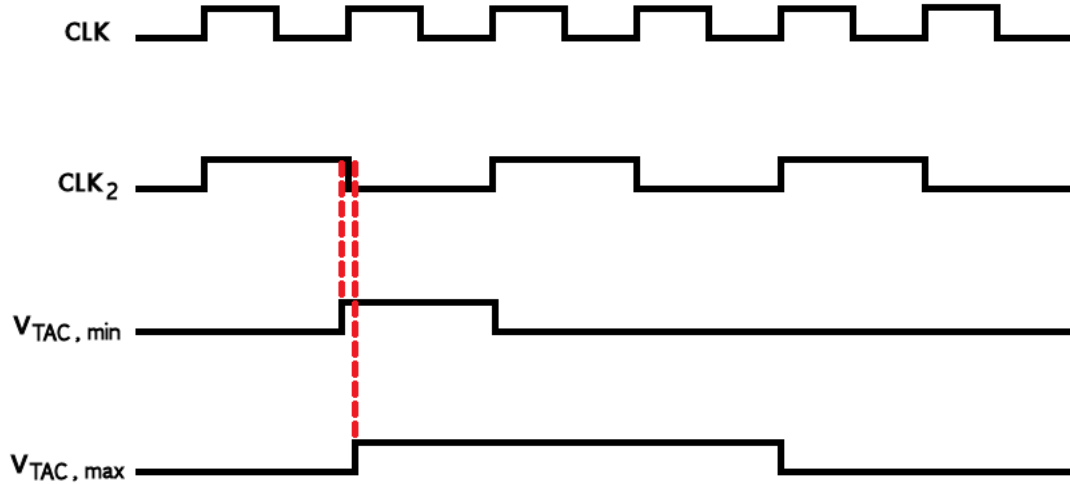
Figure 3.3:  $V_{C_1}$  (blue curve) and  $V_{C_2}$  (red curve) VS time

Zone	Open switches	Closed switches
I	1 2 3	none
II	2 3	1
III	1 2 3	none
IV	1 3	2
V	1 2	3

The use of a TDC rather than the PANDA system clock, that is 160MHz, to perform time measures is due to the resolution we want to have. Physics simulations show that we need a resolution of 10 bits, so if we use the clock period that is 6.25ns we will have a maximum signal length equal to 6.4 $\mu$ s. However, this value is definitely too long considering the high rate capability constraint requiring a maximum signal length of  $\sim 400$ ns leading to a binning time of  $\sim 400$ ps. Using a TDC the time necessary to perform the measure is proportional to  $t_{TAC}$  whose definition requires the introduction of a second slower clock  $CLK_2$  than the system clock  $CLK$  (Figure 3.4).

Figure 3.4: Definition of  $t_{TAC}$ .

We can see that  $t_{TAC}$  is the distance between the time at which the comparator fires and the first positive edge of  $CLK_2$  after a negative one. So the lower bound for  $t_{TAC}$  will occur when it starts from a time that is just before a negative edge of  $CLK_2$  since the nearest positive edge will be found after a time equal to  $\sim T_{clk}$ , vice versa when it starts from a time that is just after a negative edge the nearest positive edge will be after  $\sim 3T_{clk}$  as shown in Figure 3.5.

Figure 3.5: Lower and higher bounds for  $t_{TAC}$ .

Once we have understood the meaning of  $t_{TAC}$  we can focus on the other important parameter defining the binning time of our measure that is  $\frac{I_1 C_2}{I_2 C_1}$ . The already developed TDC uses the following values:

$$\left\{ \begin{array}{l} \frac{I_1}{I_2} = 32 \\ \frac{C_2}{C_1} = 4 \end{array} \right\} \implies T_{recharge} = 128 t_{TAC} \quad (3.2)$$

In this case we are able to achieve a binning time of

$$\frac{T_{clk}}{128} = \frac{6.25}{128} ns = 48.83 ps \quad (3.3)$$

that is very much smaller than the theoretical binning time we mentioned above. So we are allowed to reduce the ratio  $\frac{I_1}{I_2}$  in order to perform faster measures, in fact even if the binning time increases we still are comfortable in terms of high rate capability of the system.

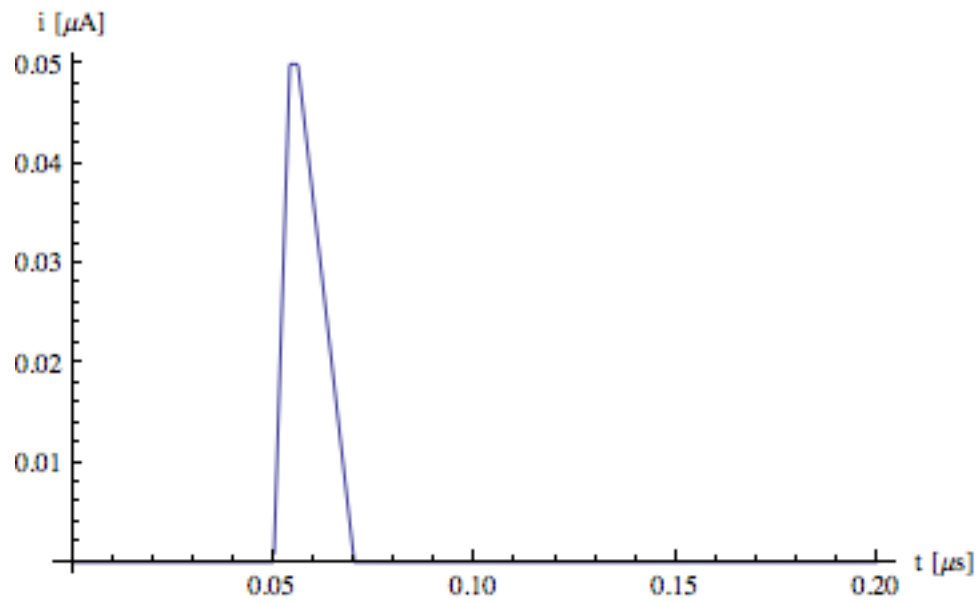
### 3.3 Front-End Amplifier

The starting point to build a front-end amplifier is what we have seen in Chapter 2. So the first step consists into a ToT measure using the well known transfer function reported below:

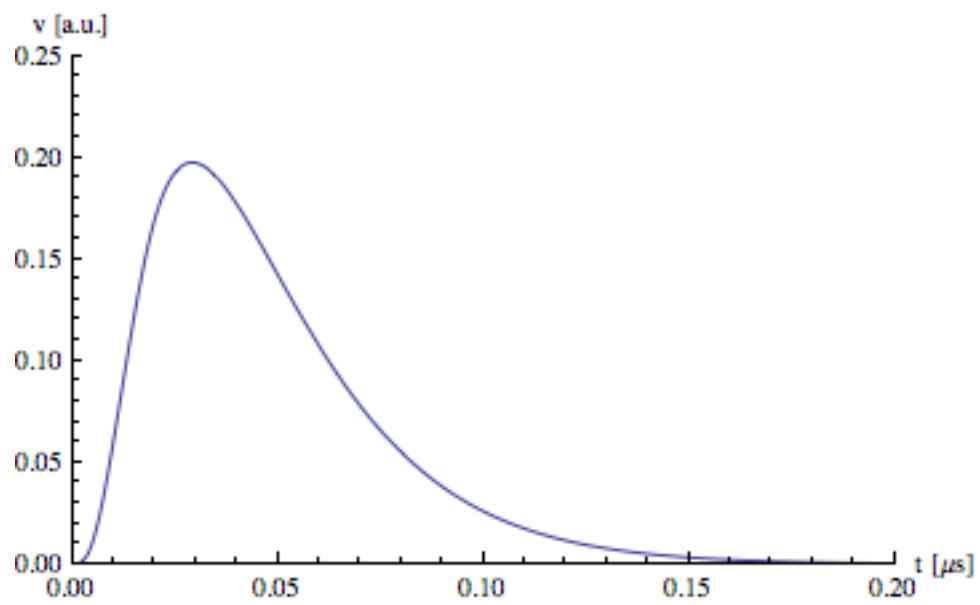
$$T(s) = \frac{1}{C_f} \frac{\tau}{(1 + s\tau)^2} \quad (3.4)$$

Using an input current signal like that shown in Figure 3.6 (a) and setting a threshold at an arbitrary value, we obtain the result shown in Figure 3.7.





(a)



(b)

Figure 3.6: (a) Input current signal; (b) output voltage signal.

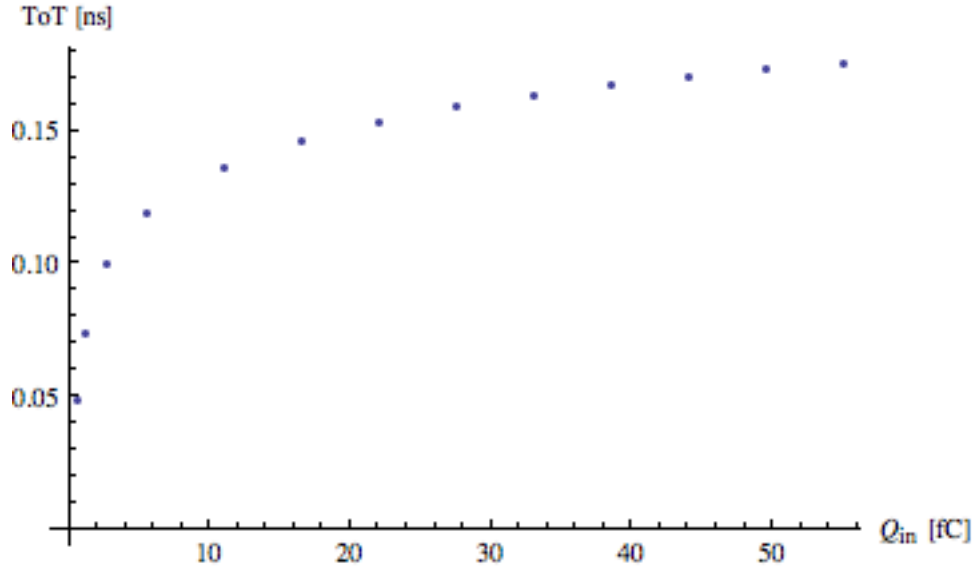


Figure 3.7: ToT measure with analytical calculations (threshold fixed at  $v=0.10$ ).

We can notice that the relationship between the ToT and the input charge doesn't follow a linear behavior. This could not be a problem, in fact the data follow a pretty smooth path that could be acceptable. However it is not a priori granted that from a real system one would obtain the same smooth behavior. In addition, a non-linear curve requires more calibration data and this can be a disadvantage in a high granularity system, where thousands of channels must be calibrated individually. Therefore, a different type of shaping which allows a linear time-over-threshold can be useful. However, the notions introduced in the previous chapter can be still used to evaluate the noise level, since for very small signal level such as the noise, the  $CR-(RC)^n$  shaper can still offer a valid approximation. So, we can start from a classic front-end amplifier, with proper modifications aimed at the improvement of the output linearity, using the results of the noise calculations showed in Section 2.4. In Figure 3.8 are shown the building blocks of the front-end we implemented, that will be discussed in detail in the following Subsections.

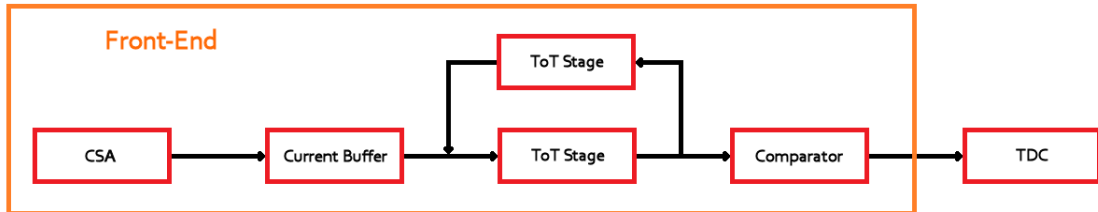


Figure 3.8: Implemented front-end amplifier (building blocks).

We can see that, with respect to the classic chain, we don't have a shaping stage anymore, but we can find two amplification stages connected through a current buffer, a baseline holder and, in the end, a comparator whose threshold will be set at  $\sim 10 V_{n(out),rms}$ . This last information leads to another important requirement: we need to have  $SNR(Q_{in,min}) > 10$  in order to be able to detect the lower input charge.

### 3.3.1 Preamplifier Stage

One of the main advantages in the design of a front-end amplifier using the ToT technique, with respect to "classic" chains aimed at amplitude measures, is the possibility to work with a saturated amplifier. In fact, the information we want to extract is the time spent by the output signal above a certain threshold, and this kind of measure can be performed even if the signal amplitude is cut at the power supply voltage. However, working with a saturated amplifier leads to some issues, such as the open-loop gain collapse. In such a situation, we can't consider the amplifier input node as a virtual ground and its voltage value starts to float leading to the already discussed cross-talk phenomenon. This is the reason why we introduce a Preamplification Stage in our chain: in order to minimize the cross-talk issue, we work with a linear amplifier in the very first stage and with a saturated one in the ToT Stage. Observing the implemented Preamplifier Stage, shown in Figure 3.9, we can notice the presence of a CSA with a pole-zero cancellation network that is quite different with respect to the one studied in Chapter 2.

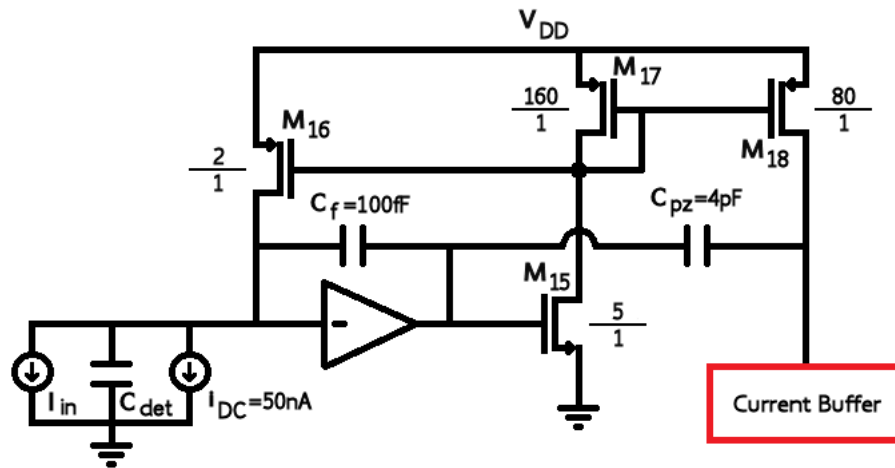


Figure 3.9: Preamplifier Stage.

Before a detailed description on how this kind of network works, will be shown the transistor level implementation of the CSA (Figure 3.10).

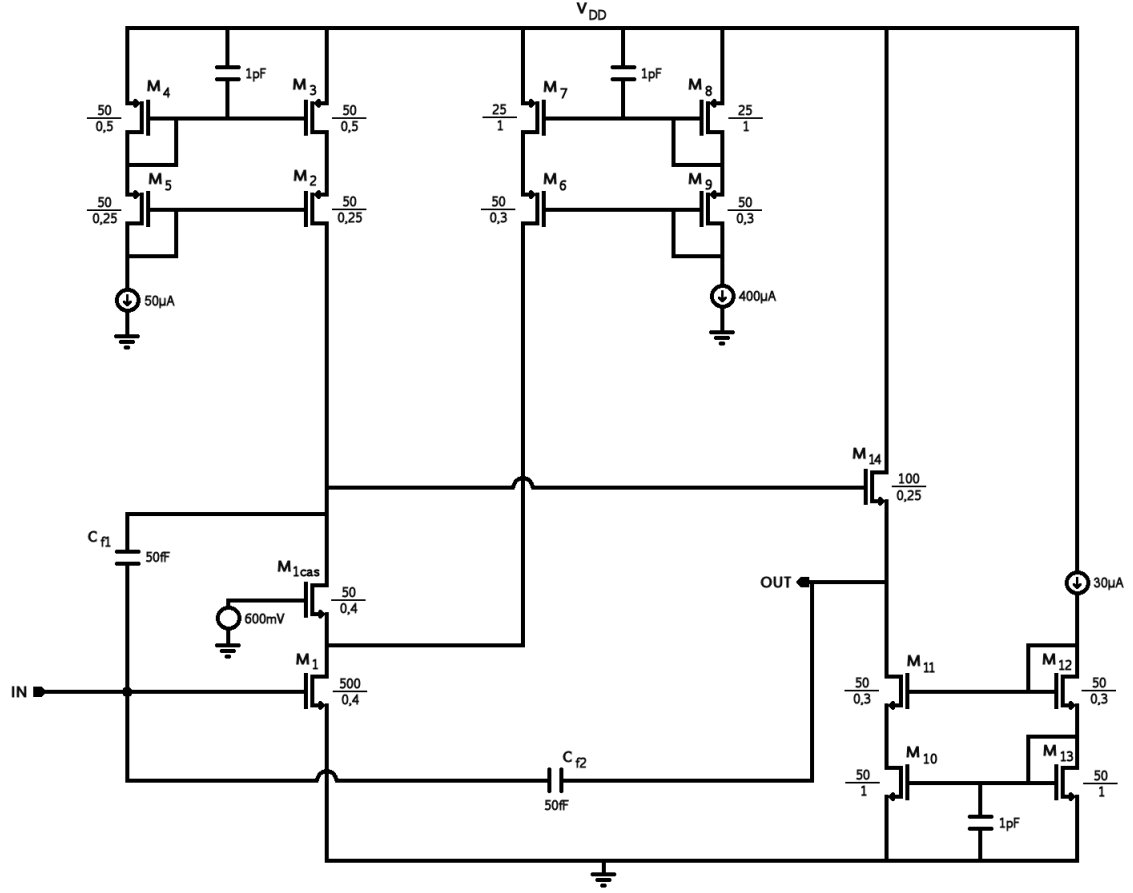


Figure 3.10: CSA (transistor level implementation).

The implemented CSA is composed by two stages: the first one is a double cascoded common source amplifier with an additional bias branch providing a better stability; the second one is a source follower amplifier with unitary gain. One of the most interesting feature of this implementation is the split of the feedback capacitance: we have a  $C_{f1} = 50fF$  connected in the feedback path of the first stage and a  $C_{f2} = 50fF$  connected between the input of the first stage and the output of the second one. From now on, we will consider only the capacitance  $C_f = C_{f1} + C_{f2} = 100fF$ , that is the value we would obtain if they were connected in parallel since the second stage is only a buffer. To understand how the feedback capacitance splitting aim at the amplifier stability, we have to study the small signal equivalent circuit (Figure 3.11) in three cases:

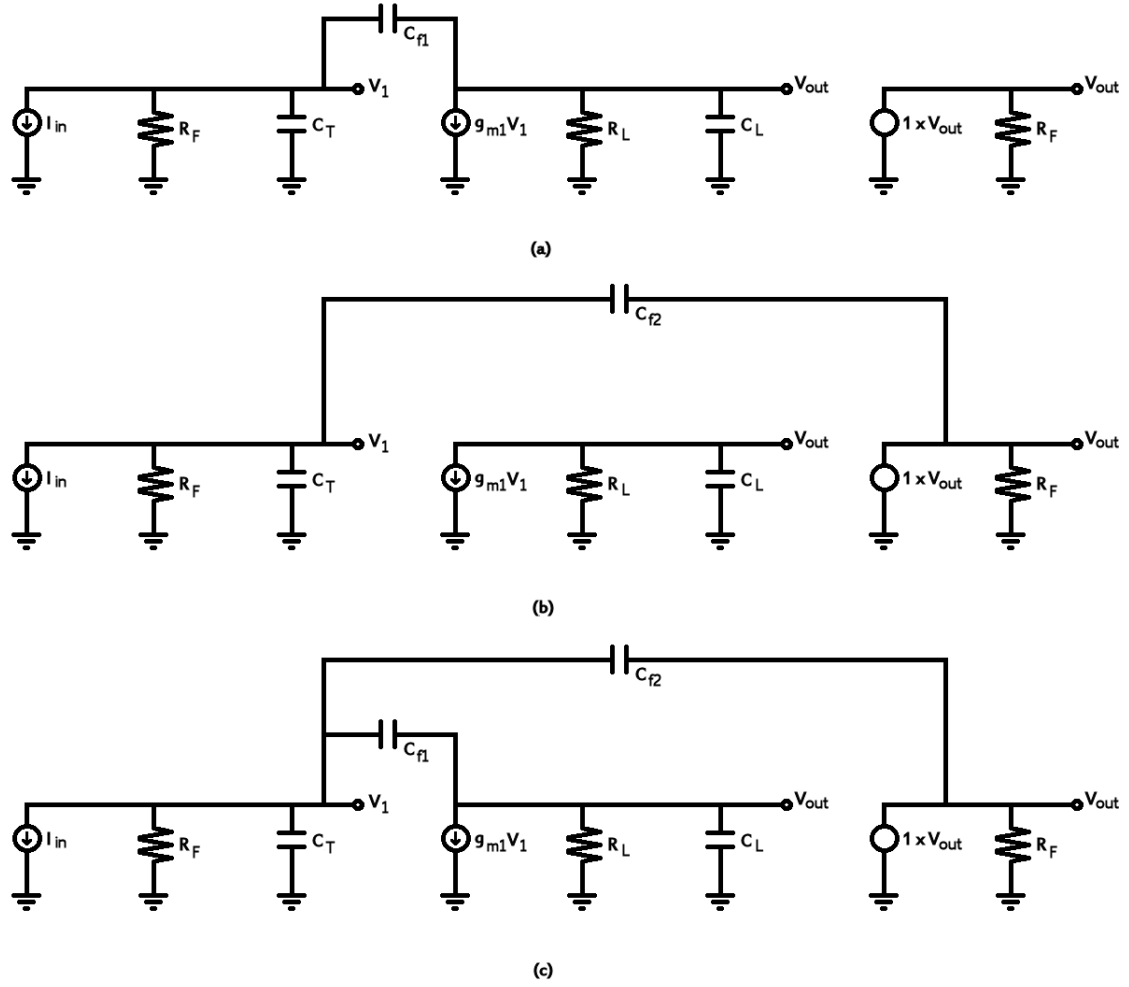


Figure 3.11: Small signal equivalent circuit of the CSA in three different cases: (a) case 1, (b) case 2 and (c) case 3.

**1.  $C_{f1} \neq 0$  &  $C_{f2} = 0$**

In this case, the total transfer function is that reported below:

$$T_1(s) = \frac{(g_{m1} - sC_{f1}) R_L R_f}{s^2 R_L R_f C_1^2 + s [R_L (C_{f1} + C_L) + R_f (C_{f1} + C_T) + A_{DC} C_{f1}] + 1} \quad (3.5)$$

where

$$C_1^2 = C_T C_L + C_T C_{f1} + C_L C_{f1} \quad (3.6)$$

and

$$A_{DC} = g_{m1}R_LR_f \quad (3.7)$$

In general, the coefficient of  $s$  is dominated by the term multiplying the DC voltage gain  $A_{DC}$ , thus we can use a more simplified version of the transfer function that is:

$$T_1(s) \approx \frac{(g_{m1} - sC_{f1})R_LR_f}{s^2R_LR_fC_1^2 + sA_{DC}C_{f1} + 1} \quad (3.8)$$

Assuming that the two poles are real and well separated in frequency, we can write the denominator of  $T_1(s)$  as follows:

$$(1 + s\tau_1)(1 + s\tau_2) = s^2\tau_1\tau_2 + s(\tau_1 + \tau_2) + 1 \approx s^2\tau_1\tau_2 + s\tau_1 + 1 \quad (3.9)$$

where we assumed  $\tau_1 \gg \tau_2$ . Comparing this last expression with the simplified transfer function, we obtain:

$$\left\{ \begin{array}{l} (\tau_1)_1 = A_{DC}C_{f1} \longrightarrow (\omega_1)_1 = -\frac{1}{(\tau_1)_1} = -\frac{1}{g_{m1}R_LR_fC_{f1}} \\ (\tau_2)_1 = \frac{R_LR_fC_1^2}{A_{DC}C_{f1}} \longrightarrow (\omega_2)_1 = -\frac{1}{(\tau_2)_1} = -\frac{g_{m1}C_{f1}}{C_1^2} \approx -\frac{g_{m1}C_{f1}}{C_T(C_L + C_{f1})} \end{array} \right. \quad (3.10)$$

where the last approximation is due to the fact that  $C_T \gg C_L, C_{f1}$ . Considering that the two dominant poles are that corresponding to the input and the output of the first stage, this case offers the best stability, but the drawback is a low accuracy in the pole-zero cancellation. In fact, in the non-ideal case, the output buffer has not a perfect unitary gain, but it has output impedance and capacitance, thus the equivalent feedback resistance  $(R_f)_{eq}$  would not be shunted to  $C_f$ .

## 2. $C_{f1} = 0$ & $C_{f2} \neq 0$

The transfer function in this case is:

$$T_2(s) = \frac{g_{m1}R_LR_f}{s^2R_LR_fC_2^2 + s[R_LC_L + C_L + R_f(C_{f2} + C_T) + A_{DC}C_{f2}] + 1} \quad (3.11)$$

where

$$C_2^2 = C_TC_L + C_LC_{f2} \quad (3.12)$$

Repeating what we have done in the previous case, we obtain the results reported below:

$$\left\{ \begin{array}{l} (\tau_1)_2 = A_{DC} C_{f2} \longrightarrow (\omega_1)_2 = -\frac{1}{(\tau_1)_2} = -\frac{1}{g_{m1} R_L R_f C_{f2}} \\ (\tau_2)_2 = \frac{R_L R_f C_2^2}{A_{DC} C_{f2}} \longrightarrow (\omega_2)_2 = -\frac{1}{(\tau_2)_2} = -\frac{g_{m1} C_{f1}}{C_2^2} \approx -\frac{g_{m1} C_{f2}}{C_T C_L} \end{array} \right. \quad (3.13)$$

In this case we operate a separation between the input and the output poles of the amplifier. This solution is the most advantageous from the point of view of the pole-zero cancellation because the feedback capacitance and equivalent resistance are connected in parallel, but is the worst in terms of stability since we don't split too much the dominant poles.

### 3. $C_{f1} = C_{f2} \neq 0$

This case represents our implementation choice, here the transfer function is:

$$T_3(s) = \frac{(g_{m1} - sC_{f1}) R_L R_f}{s^2 R_L R_f C_3^2 + s [R_L (C_{f1} + C_L) + R_f (C_{f1} + C_{f2} + C_T) + A_{DC} (C_{f1} + C_{f2})] + 1} \quad (3.14)$$

where

$$C_3^2 = C_T C_L + C_T C_{f1} + C_L (C_{f1} + C_{f2}) \quad (3.15)$$

The poles of the simplified expression of the transfer function are:

$$\left\{ \begin{array}{l} (\tau_1)_3 = A_{DC} (C_{f1} + C_{f2}) \longrightarrow (\omega_1)_3 = -\frac{1}{(\tau_1)_3} = -\frac{1}{g_{m1} R_L R_f (C_{f1} + C_{f2})} \\ (\tau_2)_3 = \frac{R_L R_f C_3^2}{A_{DC} (C_{f1} + C_{f2})} \longrightarrow (\omega_2)_3 = -\frac{1}{(\tau_2)_3} = -\frac{g_{m1} (C_{f1} + C_{f2})}{C_3^2} \approx -\frac{g_{m1} (C_{f1} + C_{f2})}{C_T (C_L + C_{f1} + C_{f2})} \end{array} \right. \quad (3.16)$$

This solution, that is the one actually implemented, represents the best compromise between the stability and the pole-zero cancellation.

We can now deal with the pole-zero network implementation. As we saw in the previous Chapter, the pole-zero cancellation in a standard front-end amplifier is obtained through a resistance  $R_x$  connected in parallel to the capacitance  $C_z$  at the output of the CSA so that  $R_x C_z = R_f C_f$ , where  $R_f$  is the impedance providing the feedback path in DC. In our implementation the pole-zero cancellation is achieved using active components (MOS transistors) rather than passive ones (resistances). To verify that this network actually works as planned, we have to calculate the equivalent impedances  $(R_f)_{eq}$  and  $(R_x)_{eq}$ . The first one is the impedance seen between the input and the output nodes of the CSA and can be evaluated considering the following steps:

1. The CSA is a TIA, so the input current  $I_{DC}$  is converted into a voltage value that we can call  $V_{CSA}$ .
2.  $V_{CSA}$  is then turned again into a current equal to  $V_{CSA}g_{m15}$ .
3. This current is converted into a voltage of  $V_{CSA}\frac{g_{m15}}{g_{m17}}$ .
4. Finally the voltage becomes a current  $V_{CSA}g_{m15}\frac{g_{m16}}{g_{m17}} \equiv I_{DC}$

Connecting all these information we get the expression reported below:

$$(R_f)_{eq} = \frac{V_{CSA}}{I_{in}} = \left( \frac{g_{m17}}{g_{m16}} \right) \frac{1}{g_{m15}} \quad (3.17)$$

and following the same steps we can obtain this other relationship:

$$(R_x)_{eq} = \frac{V_{CSA}}{I_{out}} = \left( \frac{g_{m17}}{g_{m18}} \right) \frac{1}{g_{m15}} \quad (3.18)$$

We can notice that by a proper sizing of the pMOS transistors  $M_{15}$ ,  $M_{16}$  and  $M_{17}$ , we can achieve the condition

$$\frac{(R_f)_{eq}}{(R_x)_{eq}} = \frac{C_{pz}}{C_f} \quad (3.19)$$

So, since  $g_m \sim \frac{W}{L}$ , replacing the transconductance of the transistors with their size values and the capacitors with theirs, we obtain:

$$\left\{ \begin{array}{l} (R_f)_{eq} = 80 \frac{1}{g_{m15}} \\ (R_x)_{eq} = 2 \frac{1}{g_{m15}} \end{array} \right\} \parallel \Rightarrow \frac{(R_f)_{eq}}{(R_x)_{eq}} = \frac{C_{pz}}{C_f} = 40 \quad (3.20)$$

This is also the gain factor amplifying the input current  $I_{DC}$ , in fact studying the small signal equivalent circuit of the Preamplifier Stage (Figure 3.12) we obtain the following system of equations:



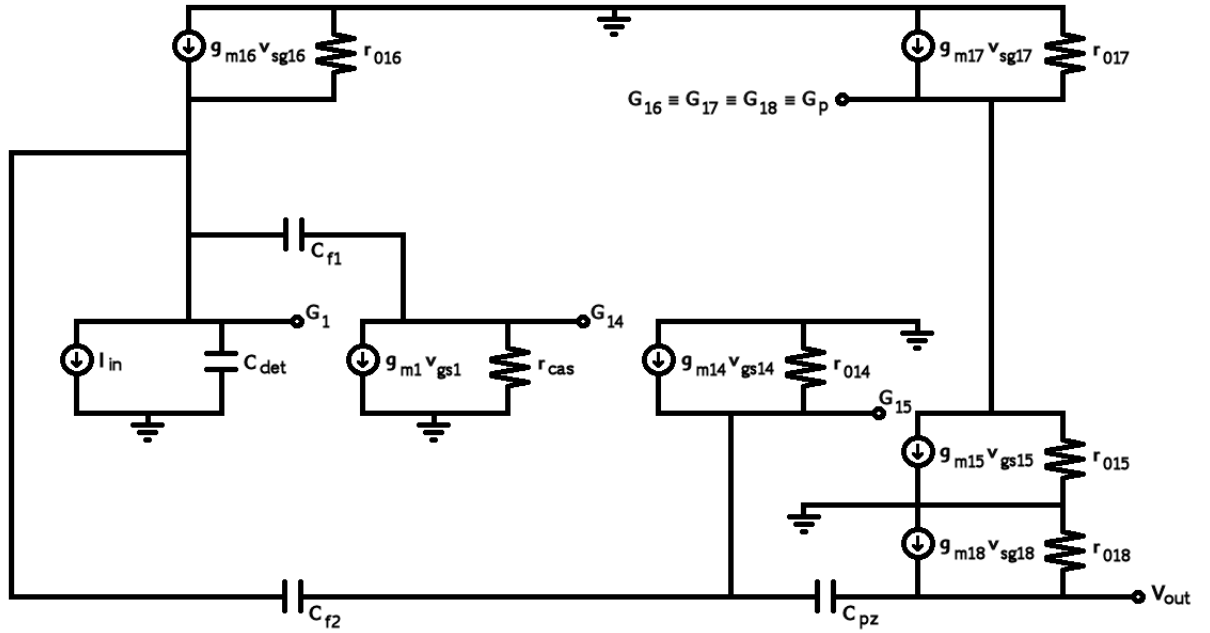


Figure 3.12: Small signal equivalent circuit of the Preamplifier Stage.

$$\left\{ \begin{array}{l}
 (G_1) \quad I_{in} + v_{G1} s C_{det} + (v_{G1} - v_{G14}) s C_{f1} + (v_{G1} - v_{G15}) s C_{f2} + g_{m16} v_{Gp} + \frac{v_{G1}}{r_{016}} = 0 \\
 (G_{14}) \quad g_{m1} v_{G1} + (v_{G14} - v_{G1}) s C_{f1} + \frac{v_{G14}}{r_{cas}} = 0 \\
 (G_{15}) \quad -g_{m14} (v_{G14} - v_{G15}) + \frac{v_{G15}}{r_{014}} + (v_{G15} - v_{G1}) s C_{f2} + (v_{G15} - v_{out}) s C_{pz} = 0 \\
 (G_p) \quad g_{m15} v_{G15} + \frac{v_{Gp}}{r_{015}} + g_{m17} v_{Gp} + \frac{v_{Gp}}{r_{017}} = 0 \\
 (out) \quad (v_{out} - v_{G15}) s C_{pz} + g_{m18} v_{Gp} + \frac{v_{out}}{r_{018}} = 0
 \end{array} \right. \quad (3.21)$$

With the approximation  $r_{cas} \rightarrow \infty$ , we finally get the transfer function (evaluated in the case  $s \rightarrow 0$  corresponding to the DC case) reported below:

$$\left| \frac{V_{out,preamp}}{I_{in}} \right| \approx \frac{g_{m18}}{g_{m16}} = 40 \quad (3.22)$$

### 3.3.2 Current Buffer

This building block has three main functions:

- Reduces the time constant given by the product of  $C_{pz}$  and the input impedance of the following stage.
- Provides a further current amplification besides the one given by the pole-zero cancellation network.
- Provides a proper output impedance for the Preamplification Stage in order to make it able to drive the ToT Stage.

To understand the first advantage given by a current buffer we need to evaluate the transfer function of the Preamplification Stage:

$$V_{out,preamp}(s) = I_{in}(s) \frac{C_{pz}}{C_f} \frac{R_p}{1 + sR_pC_{pz}} \quad (3.23)$$

where

$$R_p = \frac{R_x R_{in,CB}}{R_x + R_{in,CB}} \quad (3.24)$$

is the equivalent impedance given by the parallel between the pole-zero cancellation resistance  $R_x$  and the input impedance of the Current Buffer Stage  $R_{in,CB}$ . As far as we want that the Current Buffer provides a further amplification of the current, we want  $R_{in,CB}$  to be as small as possible. Under the assumption that  $R_{in,CB} \ll R_x \implies R_p \approx R_{in,CB}$  we can approximate the above expression:

$$V_{out,preamp}(s) \approx I_{in}(s) \frac{C_{pz}}{C_f} \frac{R_{in,CB}}{1 + sR_{in,CB}C_{pz}} \quad (3.25)$$

where it is easy to see that the smaller is  $R_{in,CB}$  the lower will be the time constant  $R_{in,CB}C_{pz}$  with a consequent increasing of the signal speed. We can now discuss the current amplifier role played by the Current Buffer through a brief introduction on how a current buffer works. The easiest way to implement a current buffer is a simple current mirror like that shown in Figure 3.13.

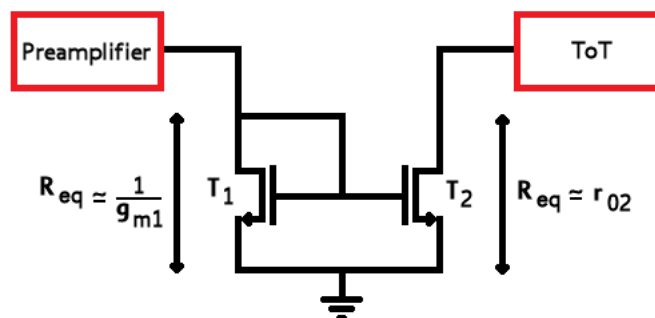


Figure 3.13: Current mirror implementation.

Considering that an ideal current amplifier needs to have null input and infinite output impedances, we want to approach as much as possible to such a situation. The technique we chose is called “ $g_m$ -boosting” and it is performed as illustrated in Figure 3.14.

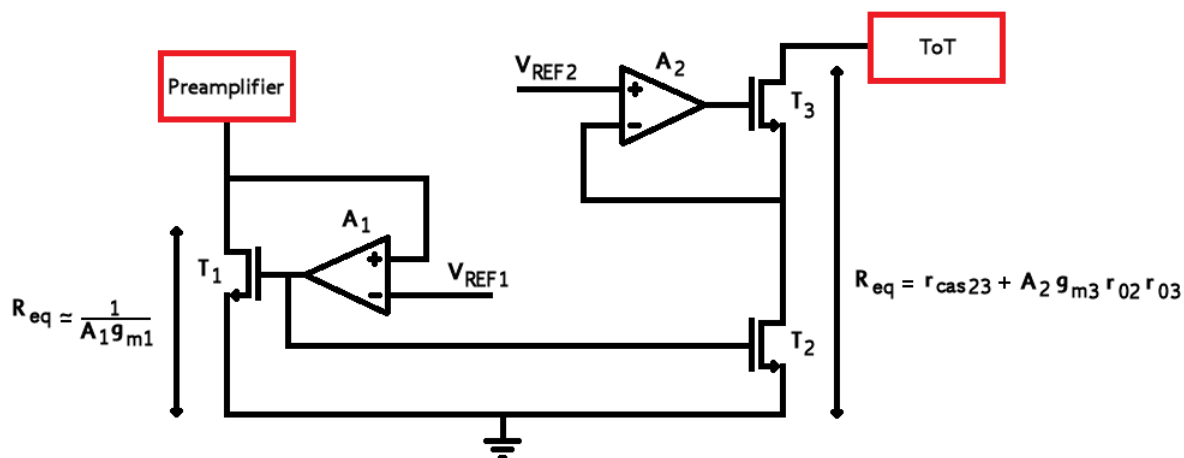


Figure 3.14: Current mirror with  $g_m$ -boosting.

The results reported in the figure are obtained through the small signal equivalent circuits of the input and the output branches. For the input part we have the circuit reported below (Figure 3.15):

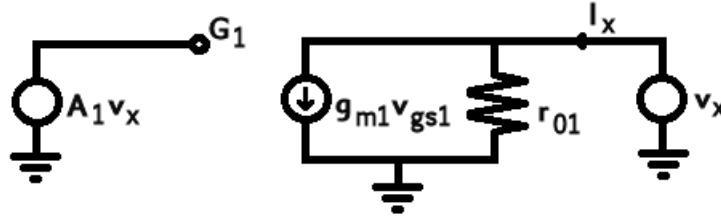


Figure 3.15: Small signal equivalent circuit to evaluate the input impedance of a  $g_m$ -boosted current mirror.

There is only one node, thus one equation:

$$A_1 g_{m1} v_x + \frac{v_x}{r_{01}} = I_x \implies R_{in} = \frac{v_x}{I_x} = \frac{1}{A_1 g_{m1} + \frac{1}{r_{01}}} \approx \frac{1}{A_1 g_{m1}} \quad (3.26)$$

where the assumption  $A_1 g_{m1} \gg \frac{1}{r_{01}}$  has been used to obtain the rightmost member. As regards the output impedance, the circuit we have to study is shown in Figure 3.16:

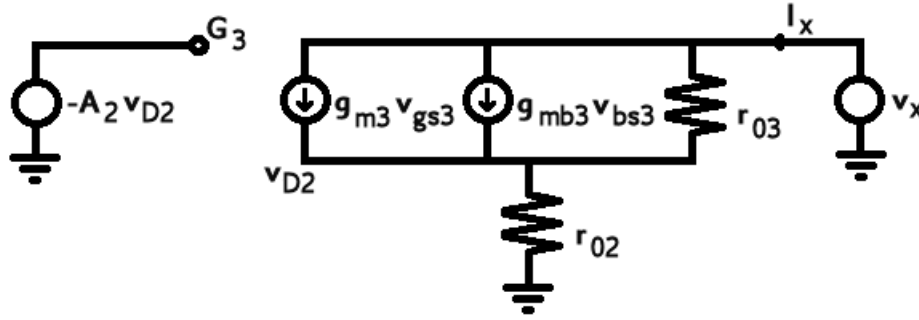


Figure 3.16: Small signal equivalent circuit to evaluate the output impedance of a  $g_m$ -boosted current mirror.

In this case we have two nodes, thus there is a system of equations to solve:

$$\left\{ \begin{array}{l} g_{m3}(-A_2 v_{D2} - v_{D2}) - g_{mb3} v_{D2} + \frac{v_x - v_{D2}}{r_{03}} = I_x \\ \frac{v_{D2}}{r_{02}} = I_x \end{array} \right\} \implies R_{out} = \frac{v_x}{I_x} = r_{cas23} + A_2 g_{m3} r_{02} r_{03} \quad (3.27)$$

where  $r_{cas2,3} = r_{02} + r_{03} + (g_{m3} + g_{mb3}) r_{02} r_{03}$  is the standard output impedance of a cascoded common source amplifier. However, such an implementation using operational amplifiers is not the most suitable since they are quite complicated devices to handle. This is the reason why we preferred to implement the Current Buffer exploiting simplest structures, obtaining the result shown in Figure 3.17.

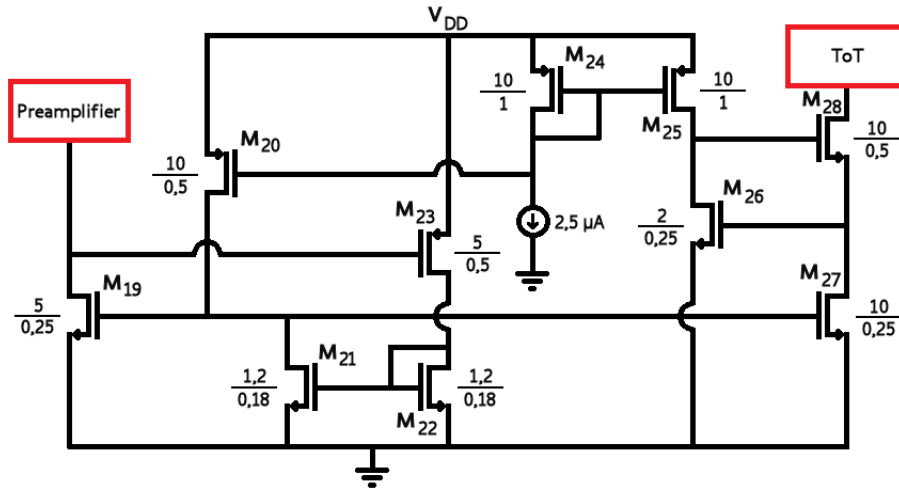


Figure 3.17: Implemented Current Buffer.

Even in this case is useful to split the circuit into input and output branches to study the equivalent impedances. The small signal equivalent circuit for the input part is shown in Figure 3.18.

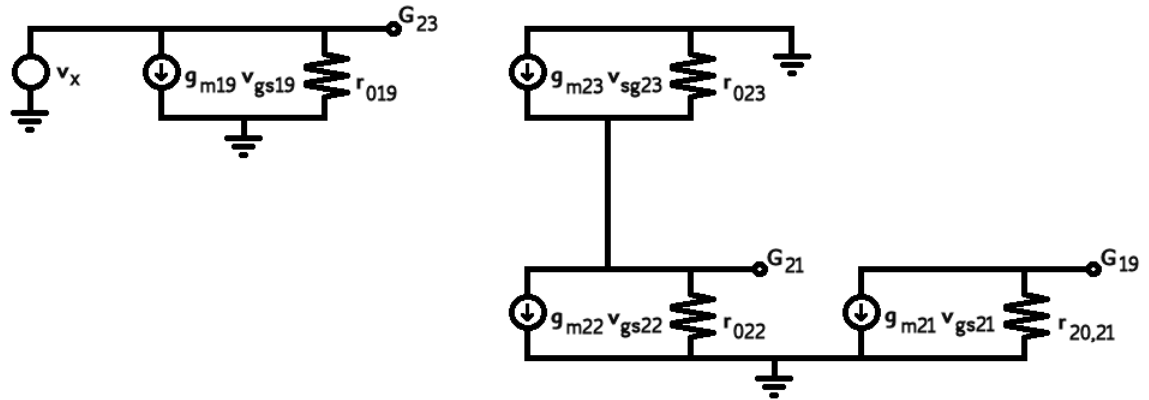


Figure 3.18: Small signal equivalent circuit to evaluate the input impedance of the implemented Current Buffer.

In this case, the circuit is a little bit more complicated with respect to the case with the operational amplifier. There are three nodes, corresponding to the gates of  $M_{19}$ ,  $M_{21}$  and  $M_{23}$ , thus a system of three equations to solve:

$$\left\{ \begin{array}{l} (G_{19}) \quad g_{m21}v_{G21} + \frac{v_{G19}}{r_{20,21}} = 0 \\ (G_{21}) \quad g_{m22}v_{G21} + \frac{v_{G21}}{r_{022}} + g_{m23}v_x + \frac{v_{G21}}{r_{023}} = 0 \\ (G_{23}) \quad g_{m19}v_{G19} + \frac{v_x}{r_{019}} = I_x \end{array} \right\} \parallel \Rightarrow R_{in,CB} = \frac{1}{A_1 g_{m19} + \frac{1}{r_{019}}} \approx \frac{1}{A_1 g_{m19}}$$
(3.28)

where

$$A_1 = \frac{g_{m21}g_{m23}r_{20,21}}{g_{m22} + \frac{1}{r_{22,23}}} \quad (3.29)$$

and

$$r_{i,j} = \frac{r_i r_j}{r_i + r_j} \quad (3.30)$$

The circuit to study for the output impedance is shown in Figure 3.19.

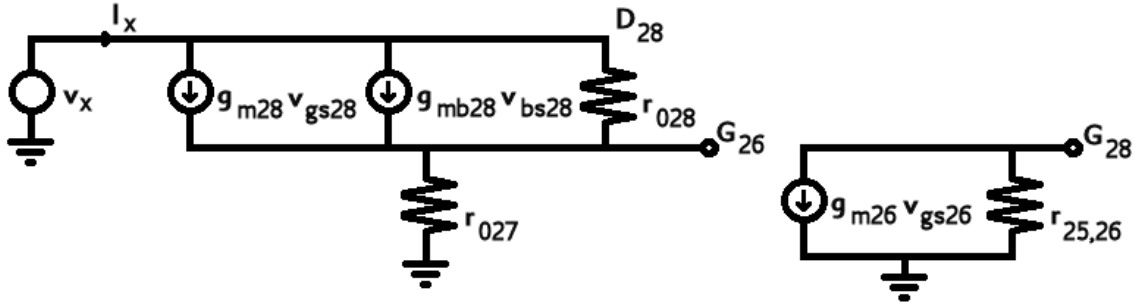


Figure 3.19: Small signal equivalent circuit to evaluate the output impedance of the implemented Current Buffer.

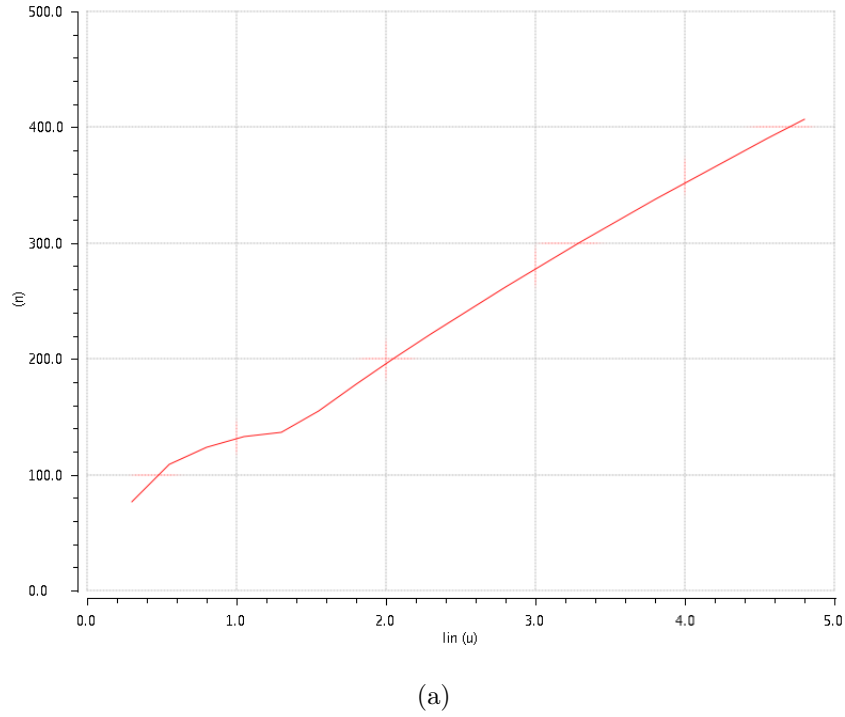
Even in this case we have three nodes and the system to solve is:

$$\left\{ \begin{array}{l} (G_{26}) \quad \frac{v_{G26}}{r_{027}} = I_x \\ (G_{28}) \quad g_{m26}v_{G26} + \frac{v_{G28}}{r_{25,26}} = 0 \\ (D_{28}) \quad g_{m28}(v_{G28} - v_{G26}) - g_{mb28}v_{G26} + \frac{v_x - v_{G26}}{r_{028}} = I_x \end{array} \right\} \parallel \Rightarrow R_{out,CB} = \frac{v_x}{I_x} = r_{cas27,28} + A_2 g_{m28} r_{027} r_{028}$$
(3.31)

with

$$A_2 = \frac{g_{m26}}{r_{25,26}} \quad (3.32)$$

We can notice that using common source amplifiers, that are absolutely easier architectures to manage rather than operational amplifiers, we obtain the same results shown before. The improvements provided by the Current Buffer can be seen in terms of linearity of the system, in fact observing the two graphics reported in Figure 3.20 it is clear the importance of this block.



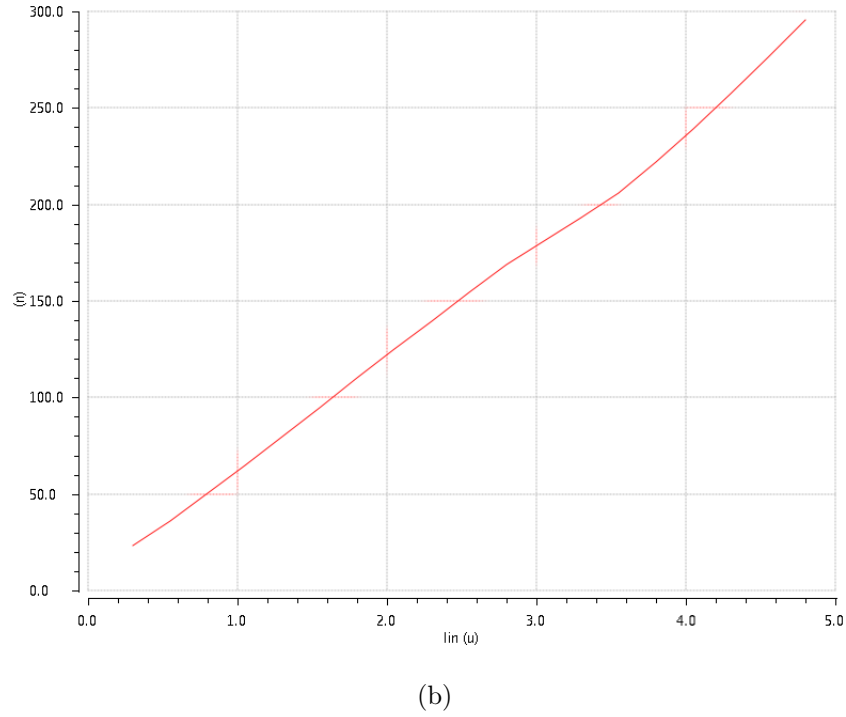


Figure 3.20: CAD simulation of ToT [ns] VS  $I_{in}$  [ $\mu\text{A}$ ] without (a) and with (b)  $g_m$ -boosting

### 3.3.3 ToT Stage

The ToT Stage is the second amplification stage. As mentioned in the previous Subsection, in this stage we work with a saturated amplifier leading to all the advantages and drawbacks already discussed. The implementation of the ToT Stage is shown in Figure 3.21.



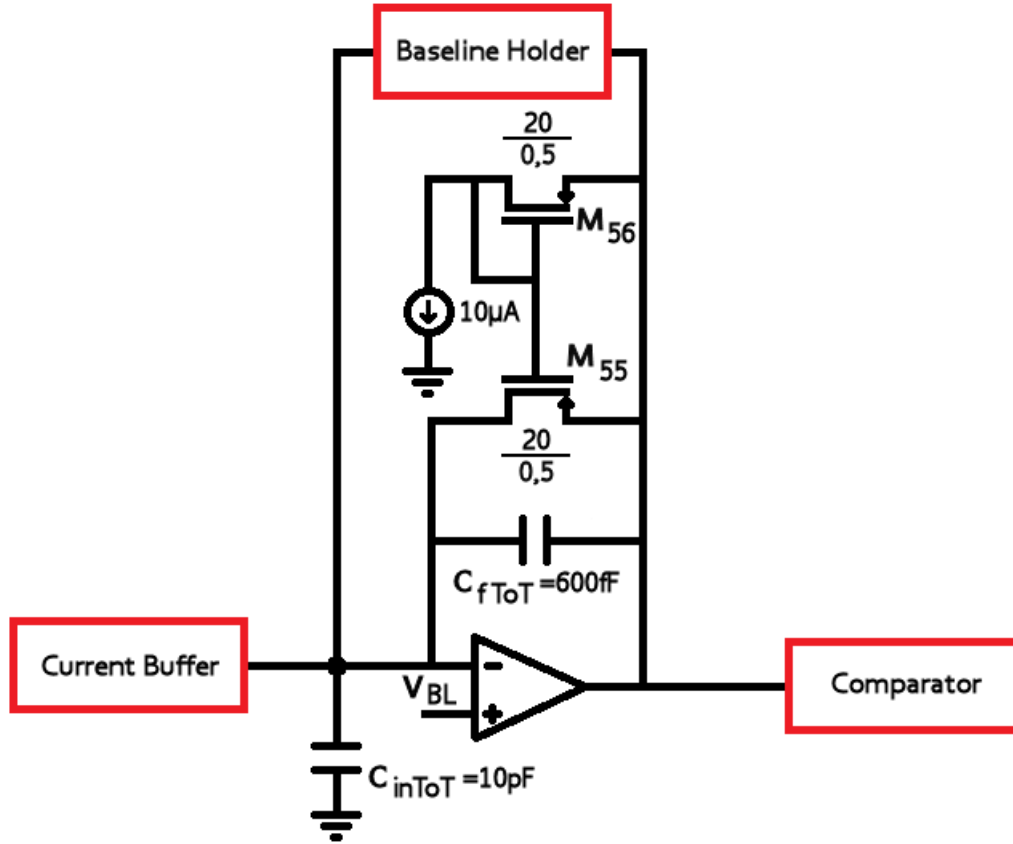


Figure 3.21: Implemented ToT Stage.

The input capacitance  $C_{in,ToT}$  provides, together with the Baseline Holder, a further reduction of the input node fluctuations due to the saturation of the amplifier. This is quite simple to understand considering the basic relationship connecting the integrated charge  $Q_{integ}$  with the capacitance:

$$\frac{dQ_{integ}}{dt} = \frac{dV_{BL}}{dt} C_{in,ToT} \quad (3.33)$$

So if  $\frac{dQ_{integ}}{dt} = const$ , the bigger is  $C_{in,ToT}$  the lower will be the baseline fluctuation. The feedback current source is built using pMOS transistors since they have a better radiation hardness. This device is one of the most important of the whole chain, in fact when the amplifier saturates it must recharge the feedback capacitance  $C_{f,ToT}$  where the current is integrated, so that the output linearity of the system depends on the linear behavior of this current source, thus on the possibility of the pMOS transistors to work in their saturation region. Let's now consider 3 different cases:

### 1. Quiescent point

When no input occurs at this stage, the pMOS transistor  $M_{55}$  acts like a linear resistor providing the DC feedback path.

### 2. $V_{\text{out,ToT}} < V_{\text{DS55,sat}}$

In presence of low input charge, the amplitude of the signal at the output of the ToT Amplifier is not enough to make  $M_{55}$  to work in its saturation region. In this case  $M_{55}$  acts like a non linear resistor and as result the ToT measure is proportional to the output signal amplitude (We will deal with this issue in the next Chapter when we'll show the results of the CAD simulations regarding the  $ToT(Q_{in})$  linearity)

### 3. $V_{\text{out,ToT}} > V_{\text{DS55,sat}}$

This is the correct working region of the current source. In fact, in this case  $M_{55}$  is saturated and together with  $M_{56}$  forms a current mirror providing the constant current recharging.

In Figure 3.22 is shown the transistor level implementation of the ToT Stage amplifier, that is the same implemented for the pixel sensors readout [4, 8]. We can notice the presence of two stages: the first one is a fully-differential amplifier, the second one is a common source amplifier. This structure offers the possibility to have a rail-to-rail output DC voltage. In fact, the only requirement is that both  $M_{37}$  and  $M_{38}$  work in saturation.

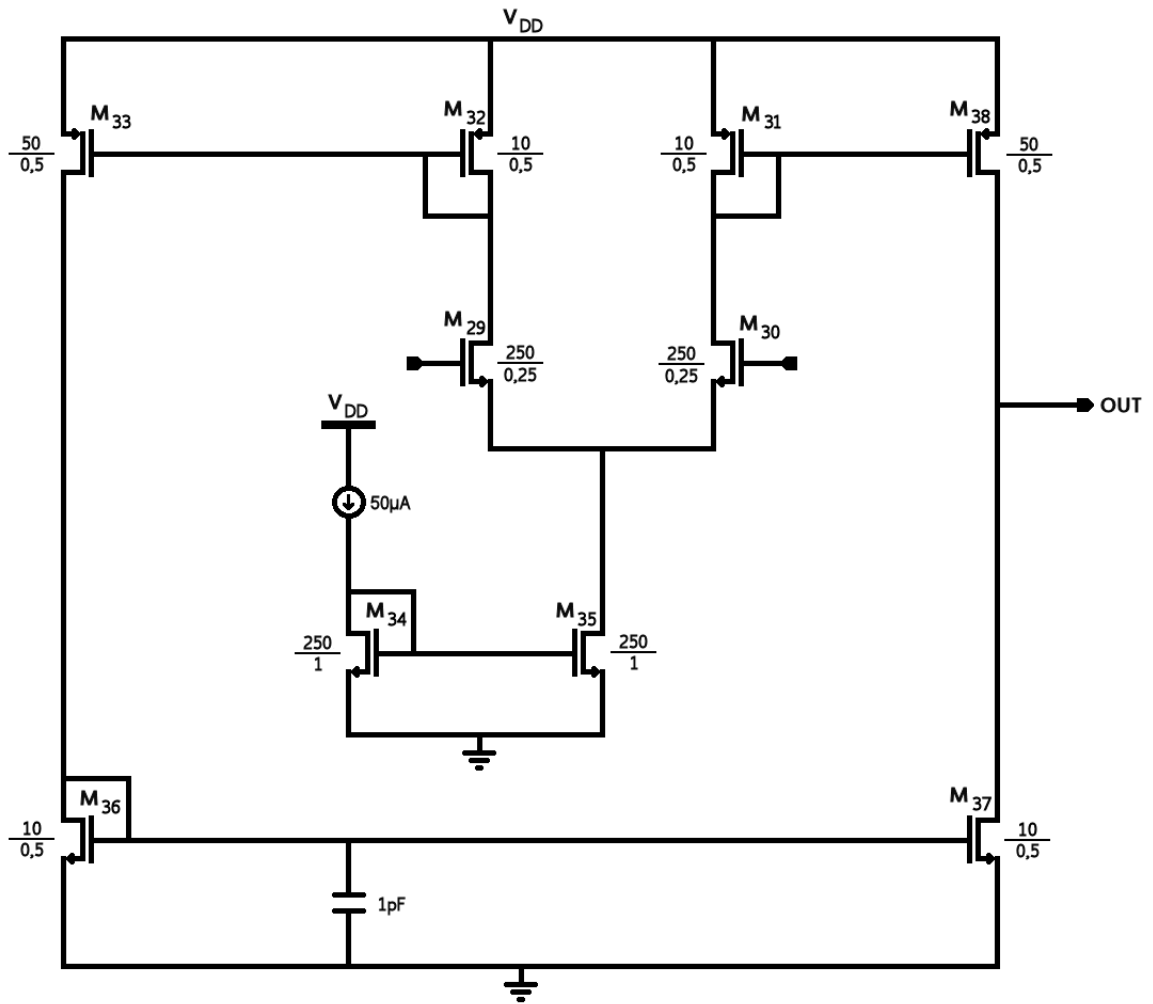


Figure 3.22: ToT Stage amplifier, transistor level implementation.



Chapter. One of the most interesting observation regards  $M_{43}$  since this transistor limits the voltage swing at the differential stage output. A proper discussion is also required to describe the task of  $M_{52}$  and  $M_{53}$  forming, together with the 1pF capacitance, a RC filter. In order to prevent the longest signals from being clipped by the leakage compensation circuit, a very low cutoff frequency is needed, otherwise a non-linearity will be introduced. This is the reason why we need to have a filter resistance as high as possible ( $\sim 10G\Omega$ ) and this is achieved through those two pMOS transistors with their gates and sources short circuited. Such a structure guarantees the desired value for the filter resistance when  $V_{DS53} < 0$ , but in the opposite case the role of the drain and the source is exchanged and the device becomes a diode connected transistor with the consequent drop of its equivalent impedance. If only negative variations of the differential output occurs,  $M_{53}$  would be enough to perform this task, but since we want to handle also with the case of variations of the opposite polarity,  $M_{52}$  is necessary.

The last stage is the Comparator, whose transistor level implementation is shown in Figure 3.24. It is a two stage amplifier: the first one is a preamplifying stage with a resistive load where the transistor  $M_{61}$  and  $M_{62}$  prevent the signal saturation, the second one is a high-gain stage whose output is connected to three buffers ( $M_{72} \dots M_{77}$ ) providing a full-swing output signal.

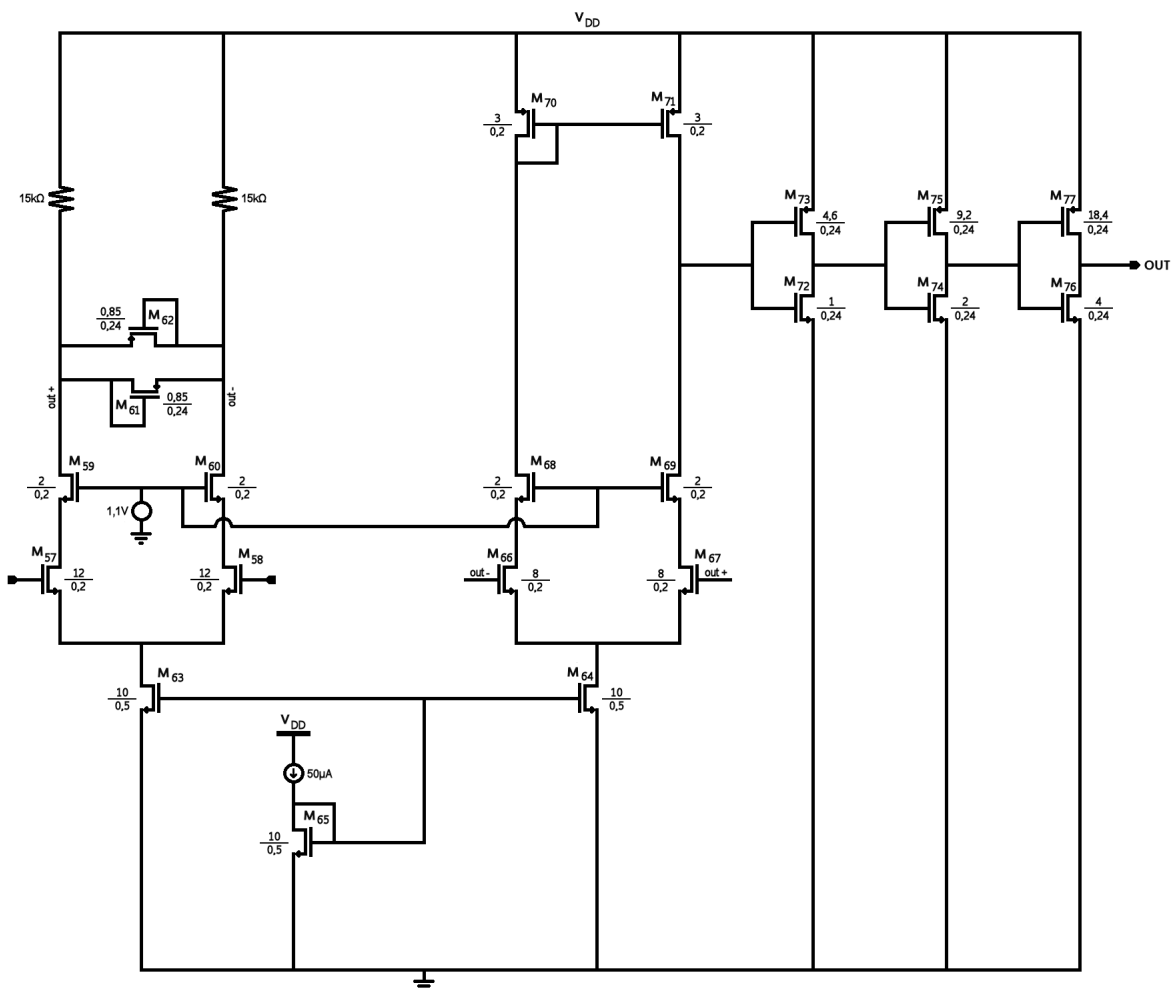


Figure 3.24: Comparator, transistor level implementation.

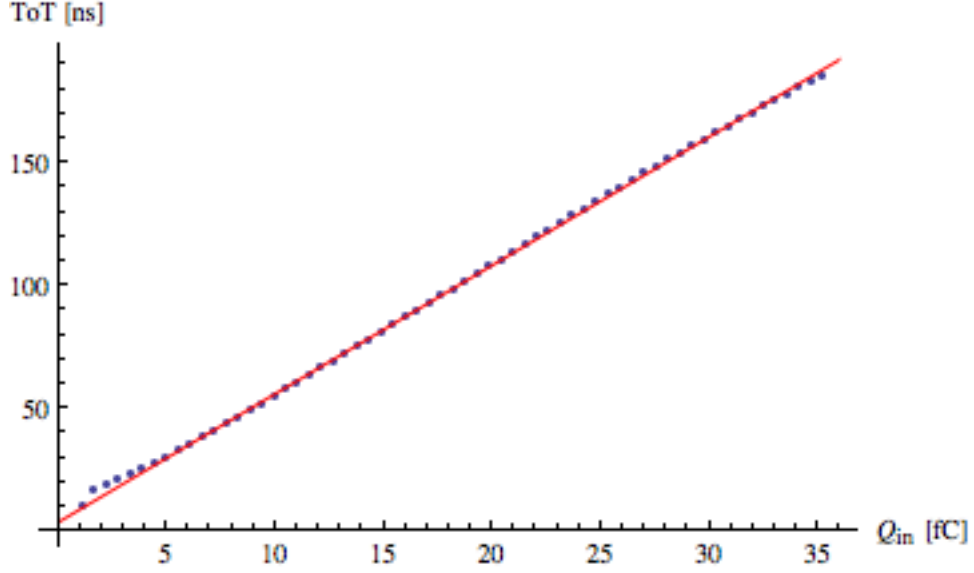
## Chapter 4

# Simulations

The most important tool for an analog electronics designer is with no doubt the electronic design automation (EDA) software. Among the many available on the market, the one we used is probably the most known among the experts: Cadence Design System. In particular, the features we used more are: Virtuoso Schematic Editor, providing a complete design environment with well-defined component libraries and the possibility to create new ones; Virtuoso Analog Design Environment (ADE), that is the tool allowing all kind of simulations on the designed schematic, from the parametric analysis to the Monte Carlo simulations, in order to thoroughly understand the circuit behavior. Using this software, we performed our simulations concentrating on two main features of the implemented front-end amplifier: the linear relationship between the ToT measures and the input charge, the dependence of the system noise on the detector capacitance.

### 4.1 Linearity

The linearity of the system is one of the most important goals of our design. Setting a threshold at a voltage of  $\sim 10V_{n(out),rms}$ , we plotted the time during which the output signal amplitude is higher than this value versus the input charge generating that signal. With a baseline of 687.7mV and a  $V_{n(out),rms} \simeq 1.1mV$  (with  $C_{det} = 5pF$ ), we chose a threshold  $V_{th} = 700mV$  obtaining the graphic shown in Figure 4.1.

Figure 4.1: ToT VS  $Q_{in}$ , simulations results.

Since this is the result of a software simulation and not a real measure, we don't have error bars, so to estimate how the data adapts to the fit, we can define a percentage error given by the following expression:

$$\sigma_{\%} = \frac{ToT_{fit} - ToT_{sim}}{ToT_{fit}} \quad (4.1)$$

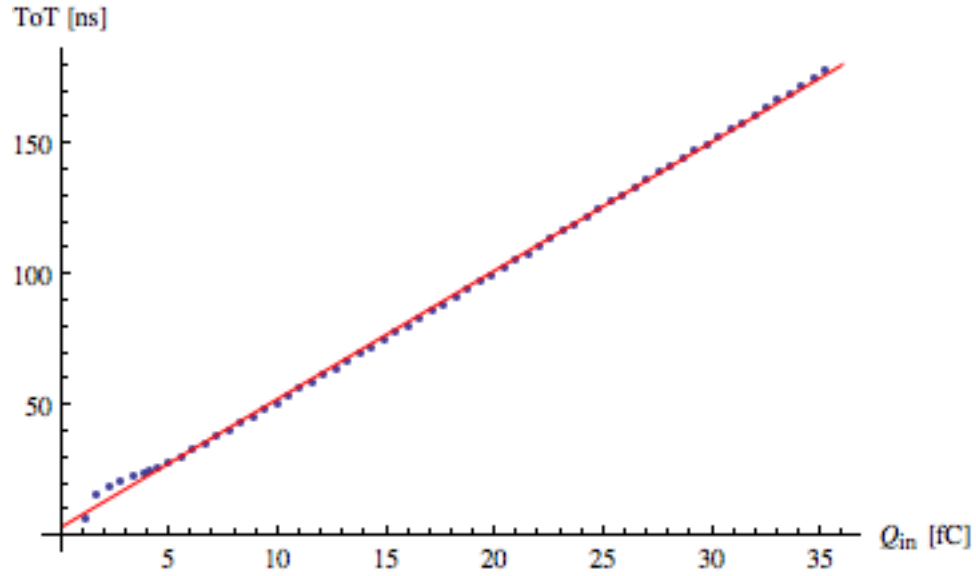
In this case we obtain  $\sigma_{\%} = 2.33\%$  and the result is not a surprise observing the points corresponding to an input charge  $1fC \lesssim Q_{in} \lesssim 5fC$  that definitely don't follow a linear path. As anticipated in the Subsection 3.3.3, this non-linearity is due to the current source of the ToT Stage. When the input signal amplitude is too low, the pMOS transistor  $M_{55}$  of the current mirror doesn't work in saturation, so that the recharging of  $C_{f,ToT}$  is not linear leading to that bending of the first part. The slope of the linear fit is  $Gain_{ToT} = 5.24 \frac{ns}{fC}$  leading to a maximum output signal duration of  $T_{signal} \simeq 180ns$  (with  $Q_{in} = 35fC$ ) that is a quite good result in terms of high rate capability of the system.

## 4.2 Corner Process Analysis

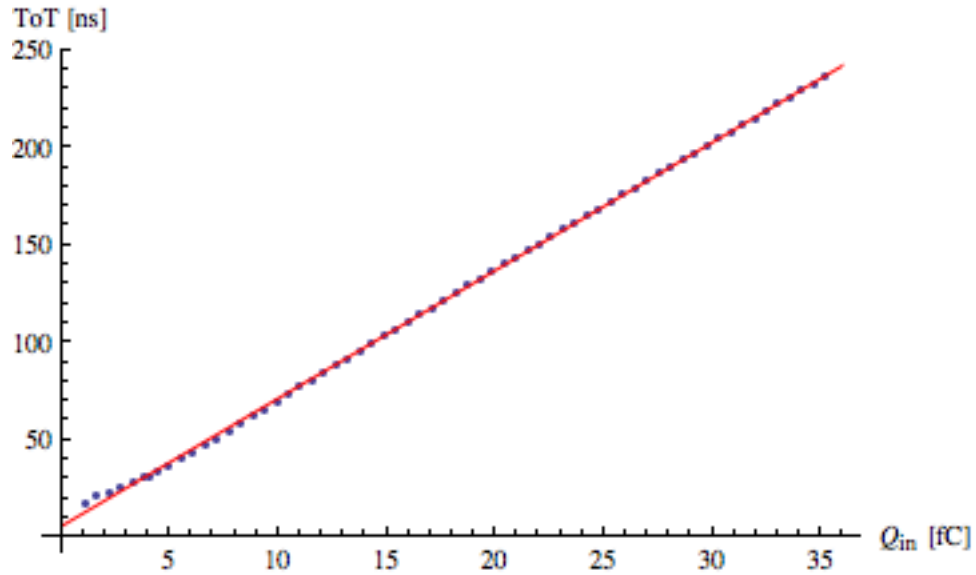
The manufacturing process can't guarantee an absolute precision of the key parameters defining the characteristic of the transistors (for instance the threshold voltage). These parameters could change from a batch to another in a certain range not predictable a priori. The corner process analysis allows to simulate



the effects due to the variation of a particular parameter affecting in the same way all the devices. We focused on the linearity in two particular configurations: Fast-Fast and Slow-Slow, that means that both nMOS and pMOS transistors are considered faster or slower than their nominal specifications. The results are shown in Figure 3.24.



(a)



(b)

Figure 4.2: (a) Fast-Fast configuration; (b) Slow-Slow configuration.

The first analysis regards the linearity of the system in these two configurations, so that we have to compare the percentage errors:

$$\sigma_{\%}(FF) = 3.13\%$$

$$\sigma_{\%}(SS) = 2.23\%$$

We can notice that these results confirm the hypothesis we did regarding the non-linearity of the system when  $1fC \lesssim Q_{in} \lesssim 5fC$ . In fact in the Fast-Fast configuration the pMOS transistor of the feedback current source of the ToT Stage is more sensitive to the voltage variations occurring at its drain, while in the Slow-Slow configuration we achieve a better linearity since the circuit response is slower. To make a comparison between these graphics and the one obtained with the nMOS and pMOS transistor in their standard configuration, we can observe the  $Gain_{ToT}$  we get, that are reported below:

$$Gain_{ToT}(FF) = 4.91 \frac{ns}{fC} \implies T_{signal}(FF) \simeq 170ns$$

$$Gain_{ToT}(SS) = 6.57 \frac{ns}{fC} \implies T_{signal}(SS) \simeq 230ns$$

The most important result is that even in the Slow-Slow configuration we get a signal duration that is very much lower than the required value of  $\sim 400ns$ .

### 4.3 Monte Carlo Simulation

This particular feature of the CAD simulator allows to see the effects of the mismatch and process variations. The first considers only the mismatch of devices, that is the difference between the sizes of the designed transistors and the actual manufactured; the second considers the variations of the process, not only of all the chips on one single wafer, but also the variations on different wafers, and even on different lots. The result of 100 runs for an input charge  $Q_{in} = 4fC$  is shown in Figure 3.25.

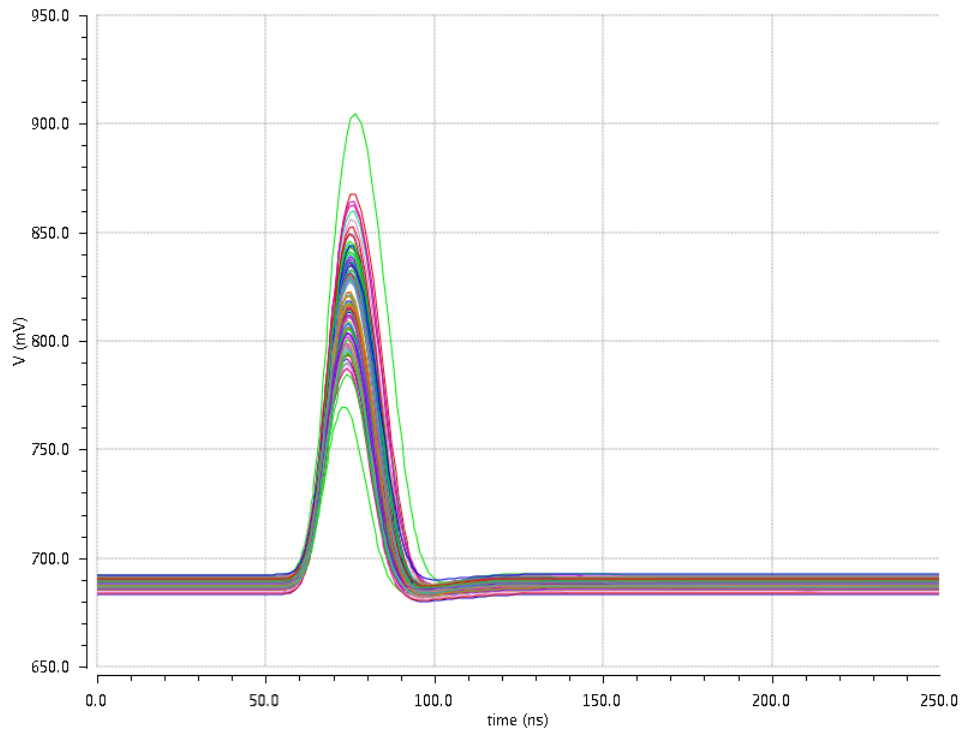


Figure 4.3: Monte Carlo simulation,  $Q_{in} = 4fC$ .

We can see that the random variations of the devices sizes definitely change the signal shape: the value of the baseline varies of  $\sim 10mV$ , the amplitude of the signal of  $\sim 130mV$  considering the maximum and the minimum. It is interesting to understand which variations, process or mismatch, is responsible of such a spread. The effects of the only process variations are shown in Figure 4.4.

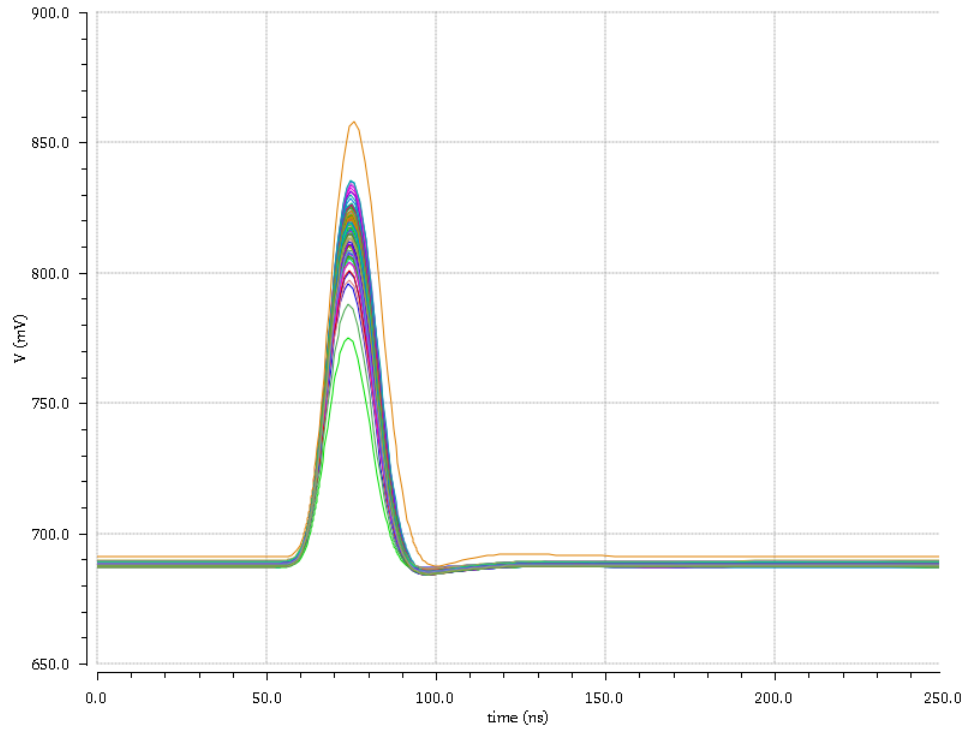


Figure 4.4: Monte Carlo simulation with only process variations,  $Q_{in} = 4fC$ .

In this case we can observe a significant decreasing of the amplitude spread, that could be further reduced by a proper tuning of the biasing sources. So the bigger contribution to the combined simulation should be given by the mismatch variations. This hypothesis is confirmed by the Figure 4.5 that puts in evidence an amplitude spread comparable with the one observed in the simulations with both kind of variations.

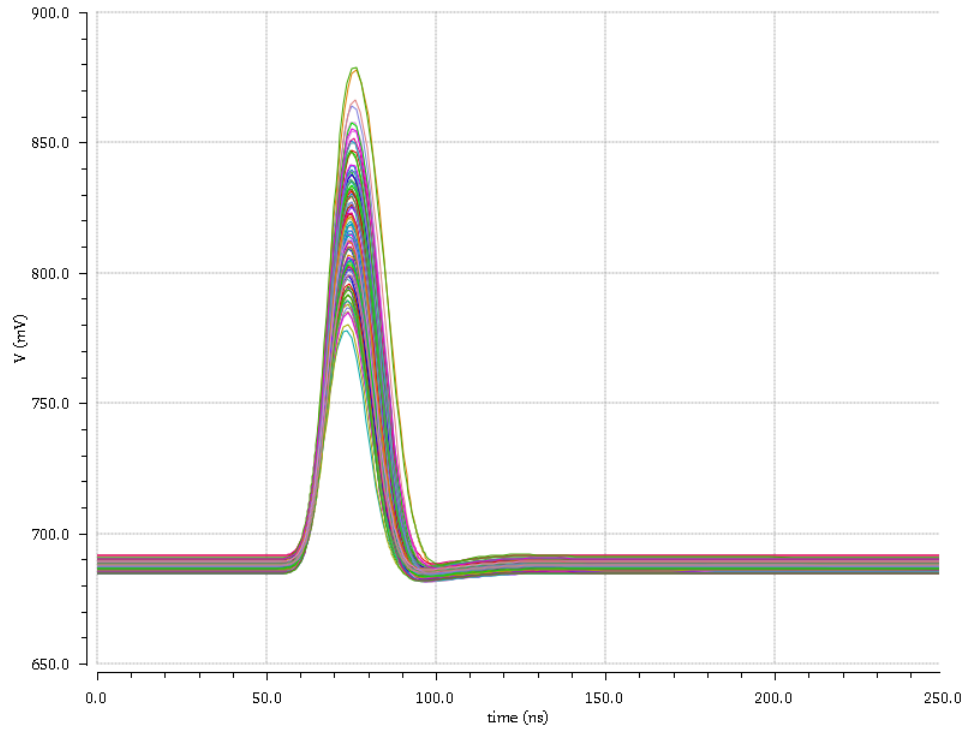


Figure 4.5: Monte Carlo simulation with only mismatch variations,  $Q_{in} = 4fC$ .

A useful feature of the Cadence Simulator allows to select the devices to ignore during the analysis, so we are able to understand which are the transistors whose mismatch causes this undesired effect. Considering that the matching between the sizes of the transistors is particularly important when they are part of a current mirror, we identified two possible suspects: the pMOS transistors  $M_{16}$ ,  $M_{16}$  and  $M_{18}$  providing the pole-zero cancellation; the input and output transistors of the current buffer  $M_{19}$  and  $M_{27}$ , respectively. Ignoring the effects of the pMOS transistors we obtain the result shown in Figure 4.6 that is not so different compared with Figure 4.5, so those devices are not the main responsible for the high amplitude spread caused by the mismatch variations.

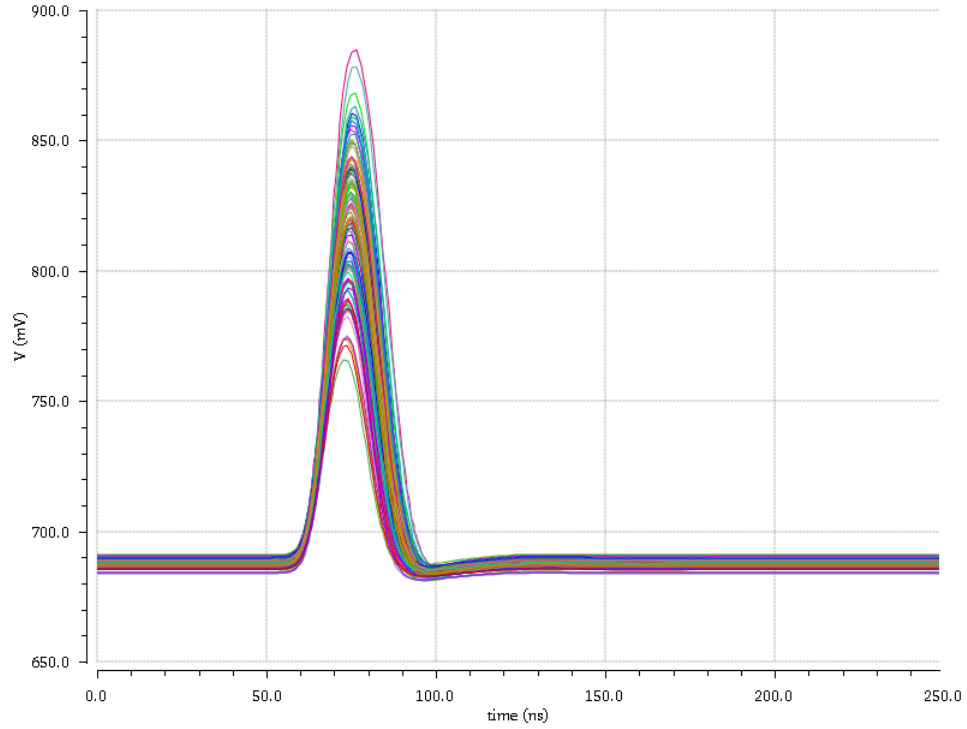


Figure 4.6: Monte Carlo simulation with only mismatch variations ignoring  $M_{16}$ ,  $M_{16}$  and  $M_{18}$ ,  $Q_{in} = 4fC$ .

If we exclude the contribution of the current buffer transistors, we obtain the graphic of Figure 4.7.

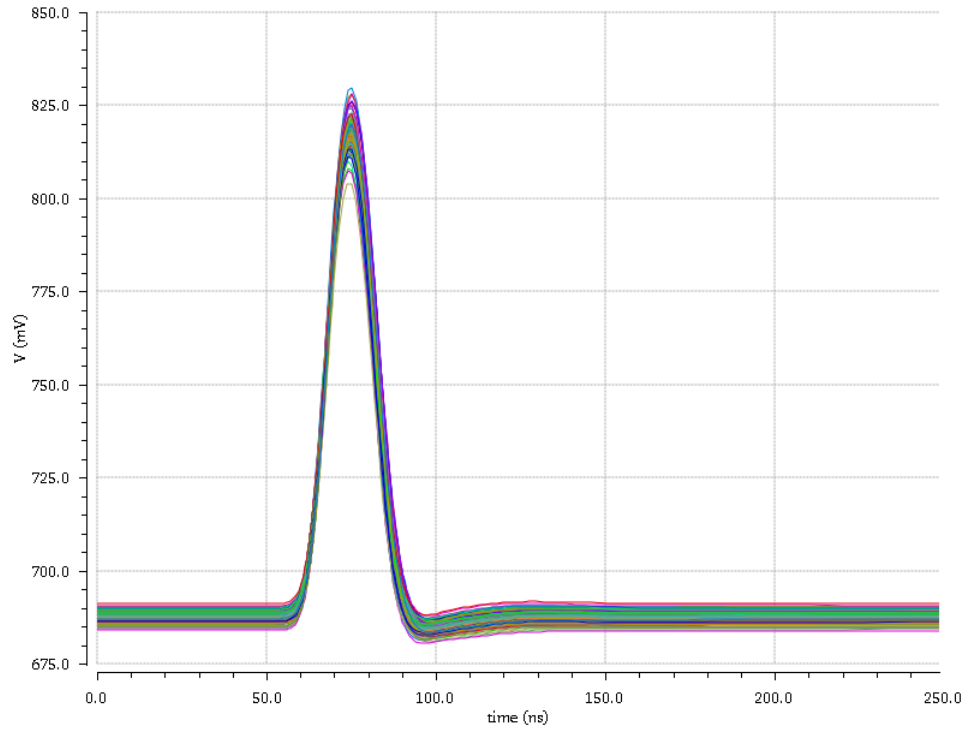


Figure 4.7: Monte Carlo simulation with only mismatch variations ignoring  $M_{19}$  and  $M_{27}$ ,  $Q_{in} = 4fC$ .

In this case the amplitude spread is significantly reduced, so we can conclude that the undesired effect observed is due to the mismatch variations of  $M_{19}$  and  $M_{27}$ . However, this is not a surprise if we observe that these transistors are much smaller than pMOSs of the pole-zero cancellation network, because we want the current buffer to be as fast as possible. Anyway, this problem is not so alarming since it can be easily solved implementing a programmable gain for the current buffer.

## 4.4 Temperature variations

Another important analysis for any circuit regards the variations of its behavior depending on the working temperature. Since we are mostly interested in the linearity of the system, we simulated this kind of measure for 6 different temperature. The result of the simulation is shown in Figure 4.8.

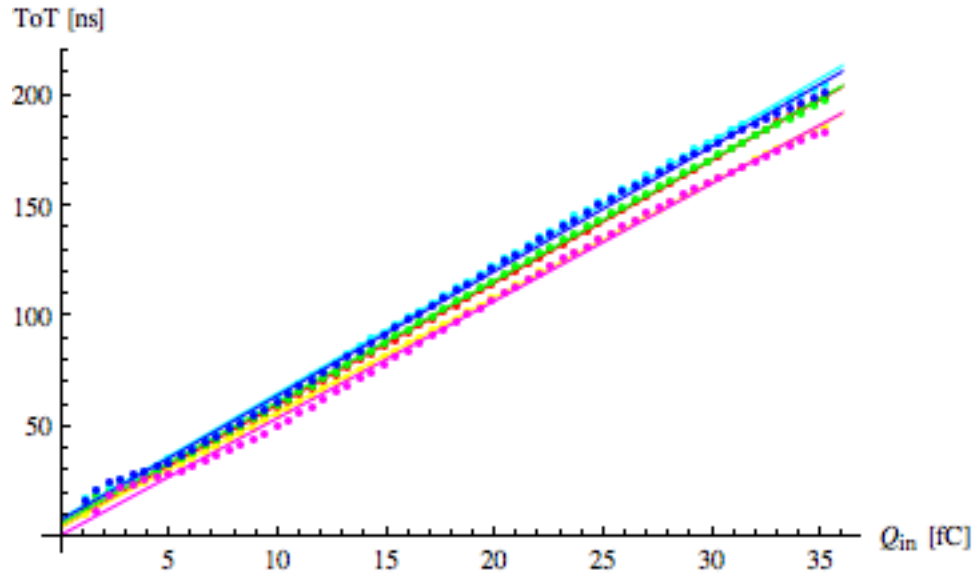


Figure 4.8: ToT VS  $Q_{in}$ , with temperature variations.

We can see that in a temperature range of  $0^{\circ}\text{C} < T < 125^{\circ}\text{C}$  the linearity doesn't suffer so much the temperature variation, except for the first part where we can notice a quite sensitive worsening when  $T > 100^{\circ}\text{C}$ . However, this is not a big deal since the circuit has to work at room temperature.



## 4.5 Noise

One of the most important analysis regards the noise of the front-end amplifier. The Cadence Simulator allows two different type of noise simulation. The first follows a path similar to the one we discussed in Chapter 2 since uses small signal equivalent models adding the contribution of the noise sources represented by voltage and current generators. Obviously the models used by the Simulator are much more complex and complete with respect to the ones we used to evaluate the noise of a front-end amplifier. The second type of simulation is called “transient noise” and allows to simulate the behavior of an architecture in presence of random fluctuations in the signals modeling the noise. In our simulations, we used both these kind of analysis and the results are reported in this Section.

As we have seen in Section 2.4, the noise of the system depends on two main parameters: the peaking time  $T_p$  and the input capacitance  $C_T$ . Since the first one is locked by the high rate capability constraint, we will focus on the latter. Considering that the implemented front-end amplifier must work with sensors of different size, and thus different capacitance, we simulated the noise variations occurring with different values for the detector capacitance and the result is shown in Figure 4.9.

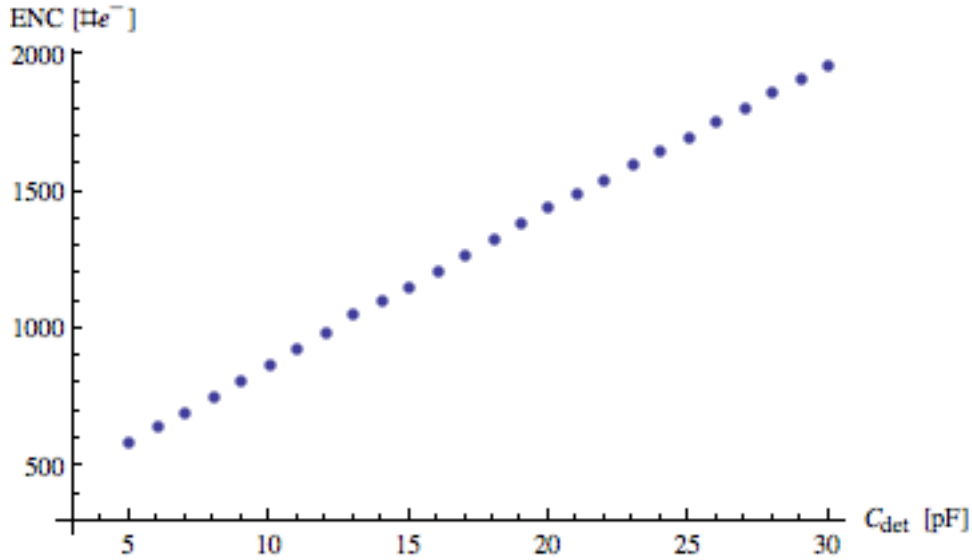


Figure 4.9: ENC VS  $C_{det}$ .

Another interesting feature of the CAD allows to identify the devices giving the bigger contribution to the rms noise evaluated through an AC analysis. This gives the chance to check if we operated an appropriate sizing of the components, in fact we can verify if the input transistor actually gives the dominant contribution to the noise of the system. In Table 4.1 are shown the top 5 devices with the percentages of influence on the noise of the system.

Device	Noise type	Percentage [%]
$M_1$	thermal	30.47
$M_1$	flicker	9.58
$M_{22}$	flicker	7.55
$M_7$	thermal	5.43
$M_3$	thermal	5.18

Table 4.1: Top 5 noise contributors.

There are two interesting things to observe: the most important contribution to the noise is actually given by the input transistor  $M_1$ , in fact, considering that the total noise is given by the root sum square of all the contributors, a percentage of 30% is enough to state that we operated a good sizing of the devices; the more complete models used by the CAD allow to find other possible noise sources that in a first analysis could be neglected and this is the case of  $M_{22}$ . We can now compare the results obtained using this first type of noise analysis with the theoretical noise calculations of Section 2.4. The basic assumption of the calculation reported in Chapter 2 is that we work with a linear system. Thus, the first step is to verify if the amplitude values of the output signals have a linear behavior as the input charge increase and if the peaking time remains constant. Using input signals, of both polarities, corresponding to very low input charges ( $\sim 0.1fC$ ), leading to output signals amplitude comparable with  $V_{n(out),rms}$ , we obtain the results shown in Figure 4.10:

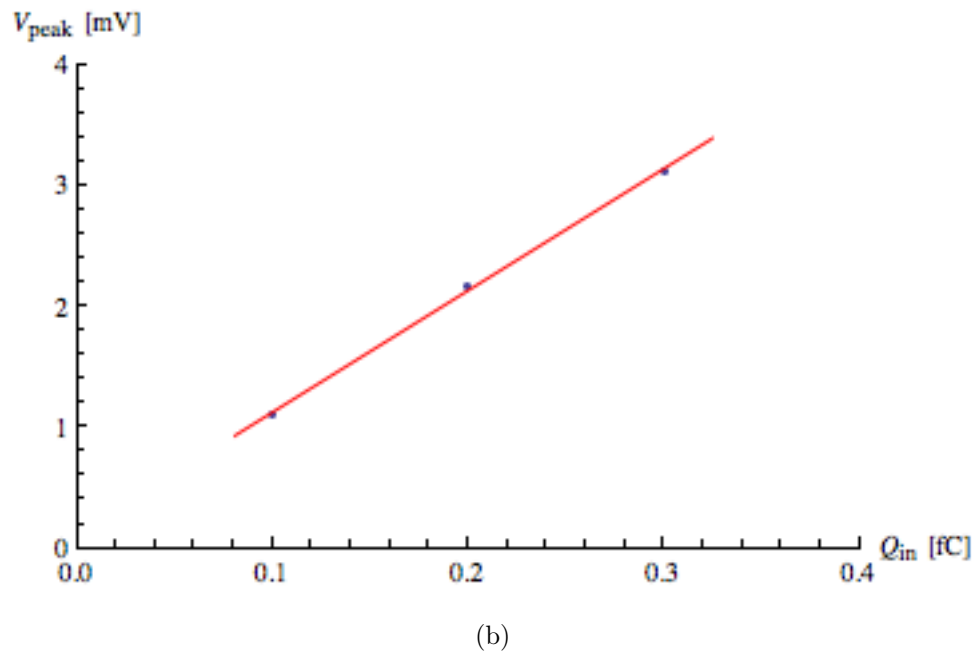
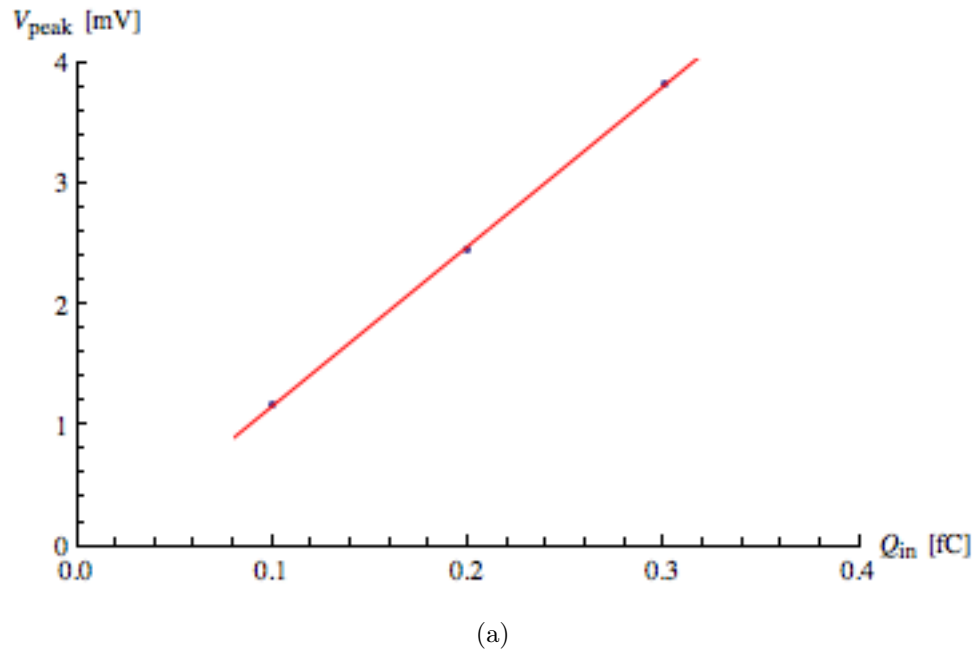


Figure 4.10:  $V_{peak}$  VS  $Q_{in}$  with (a)  $I_{in} > 0$  and (b)  $I_{in} < 0$

The percentage errors of these two fit are reported below:

$$\sigma_{\%}(I_{in} > 0) = 0.65\%$$

$$\sigma_{\%}(I_{in} < 0) = 0.96\%$$

In these conditions the mean peaking time is:

$$T_p \approx (20 \pm 1) \text{ ns}$$

that means a variation of  $\sim 4\%$ . All the results allow us to conclude that the system can be considered linear. The second type of noise analysis, the transient noise analysis, helps to achieve a better understanding of the system through the study of the baseline noise distribution. The result of such analysis is shown in Figure 4.11:

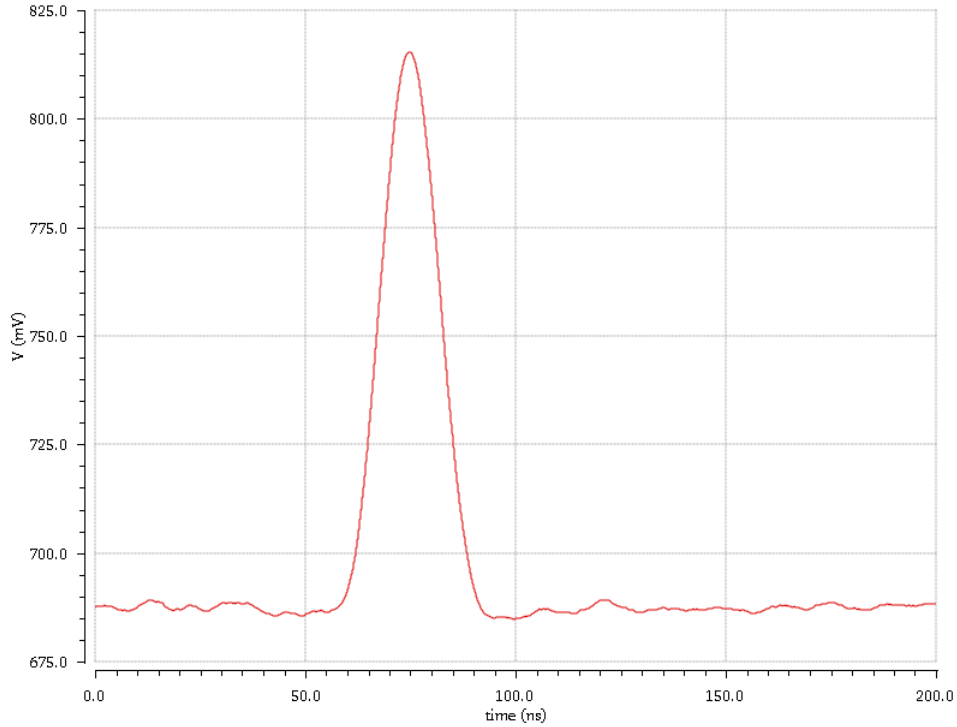


Figure 4.11: Example of output signal in transient noise analysis ( $Q_{in} = 4fC$ ).

where we can notice that we are able to obtain very realistic signals. In such a situation, we can verify that the noise distribution of the baseline voltage value (Figure 4.12) is of Gaussian type as shown in Figure 4.13:

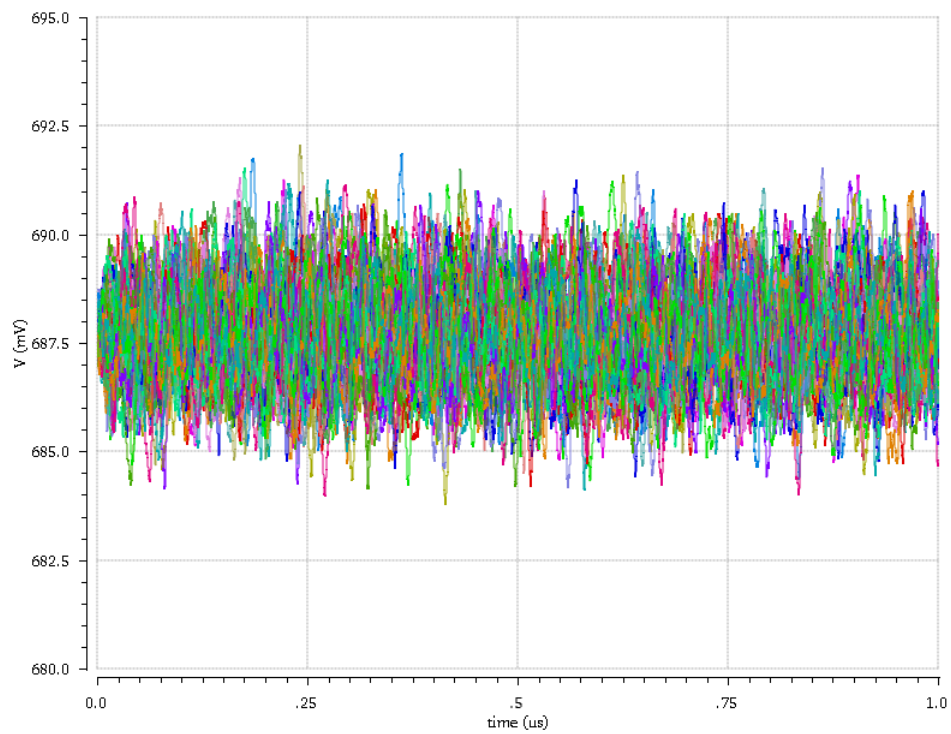


Figure 4.12: Baseline voltage noise with 50 runs.

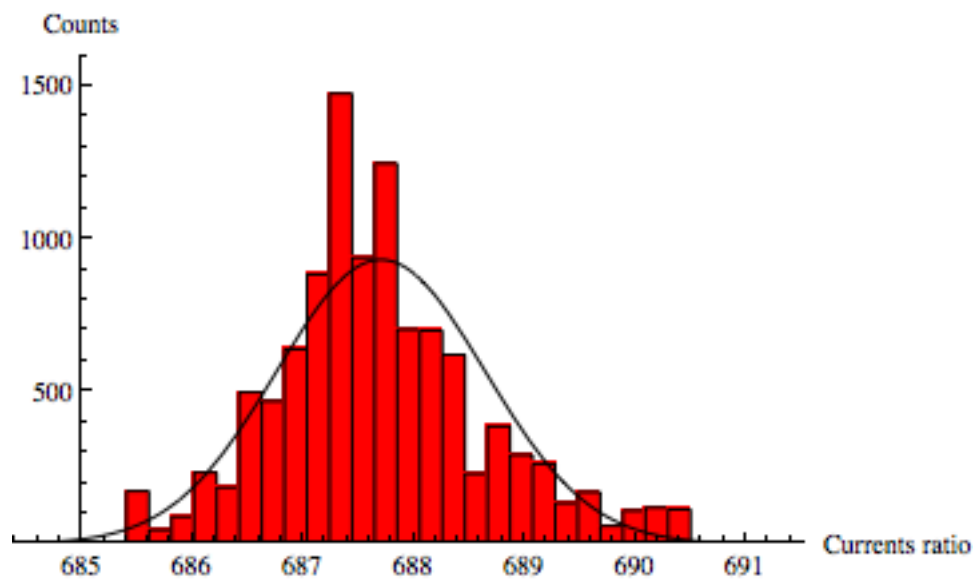


Figure 4.13: Gaussian fit of the baseline noise distribution.

whose key parameters are:

$$\mu = 687.7mV$$

$$\sigma = 0.9mV$$

We can also see that simulating multiple runs, the histograms show a typical Gaussian distribution made by the overlapping of the single distribution of each run (Figure 4.14).

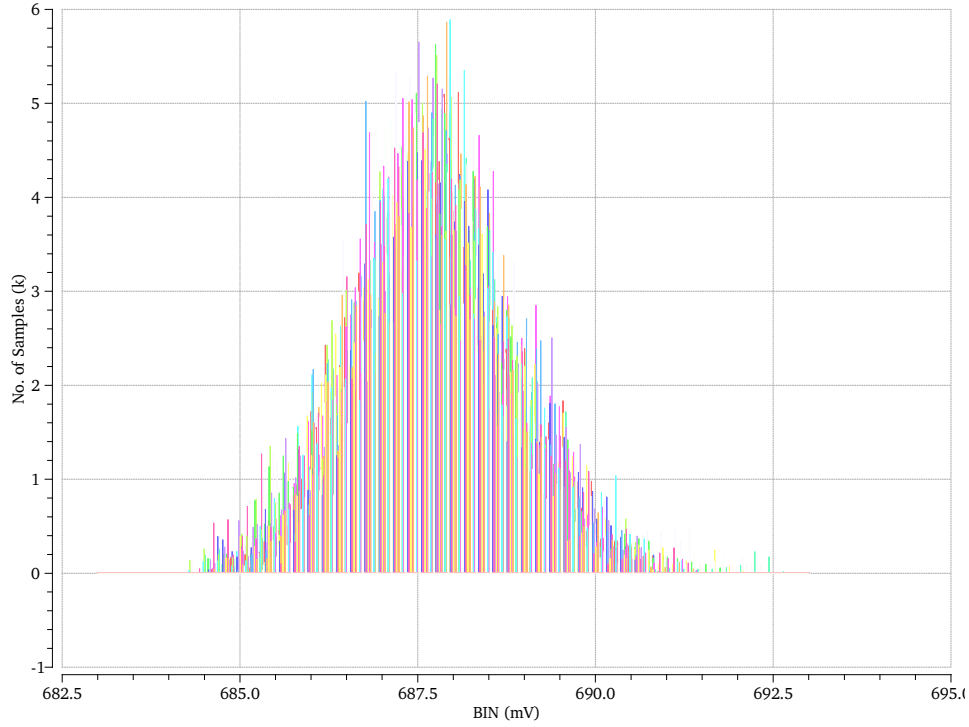


Figure 4.14: Gaussian fit of the baseline noise distribution with 50 runs.

Now we need to model the implemented front-end with a  $CR-(RC)^n$  shaper. With an input signal  $Q_{in} = 4fC$ , the best result is achieved with a 9th order shaper (Figure 4.15):

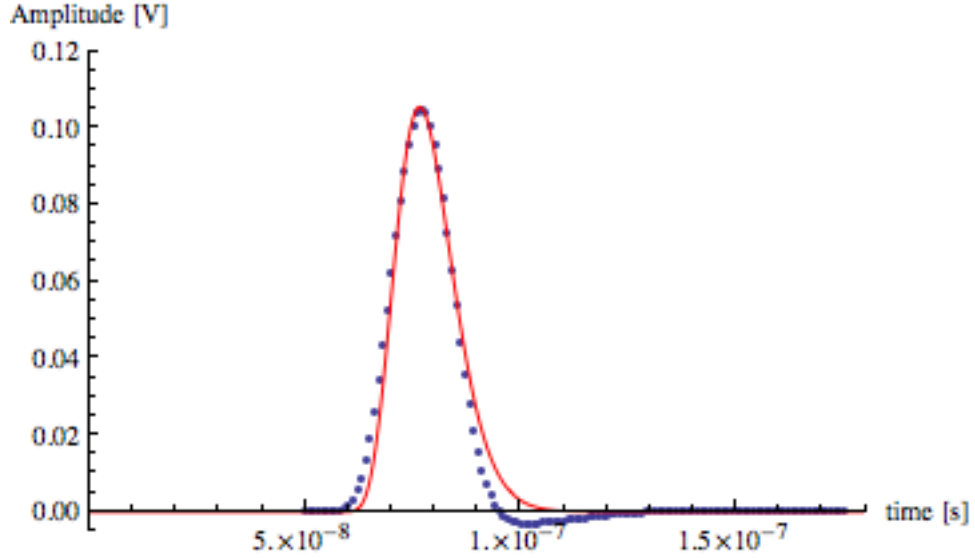


Figure 4.15: Implemented front-end output signal VS  $CR-(RC)^9$  shaper.

We see that the fit is not perfect, especially for the trailing part of the signal. The undershoot suggests that a system with complex conjugate poles could give a better approximation. However, the noise coefficient of the filter would not change so much, so we can use a simple  $CR-(RC)^9$  modeling. The power spectral densities of each noise contribution are reported below:

$$V_{nW}^2 = 4k_B T \frac{1}{g_{m1}} \Gamma = 1.57 \cdot 10^{-18} \frac{V^2}{Hz}$$

$$V_{nF}^2 = \frac{K_f}{C_{ox} W_{M1} L_{M1}} \frac{1}{f} = 6.95 \cdot 10^{-13} \frac{V^2}{Hz}$$

$$I_{nP}^2 = 4k_B T g_{m16} = 2.07 \cdot 10^{-26} \frac{A^2}{Hz}$$

Considering that  $M_1$  works in weak inversion we put  $\Gamma = 0.5$  and for the flicker noise we assumed a reasonable common value for  $K_f = 2 \cdot 10^{-24} JHz$  and  $t_{ox} = 2.4nm$ , while the parallel noise is given by the pMOS transistor  $M_{16}$  biasing the input node. Comparing the simulated and the theoretical data, we obtain the graphic shown in Figure 4.16:

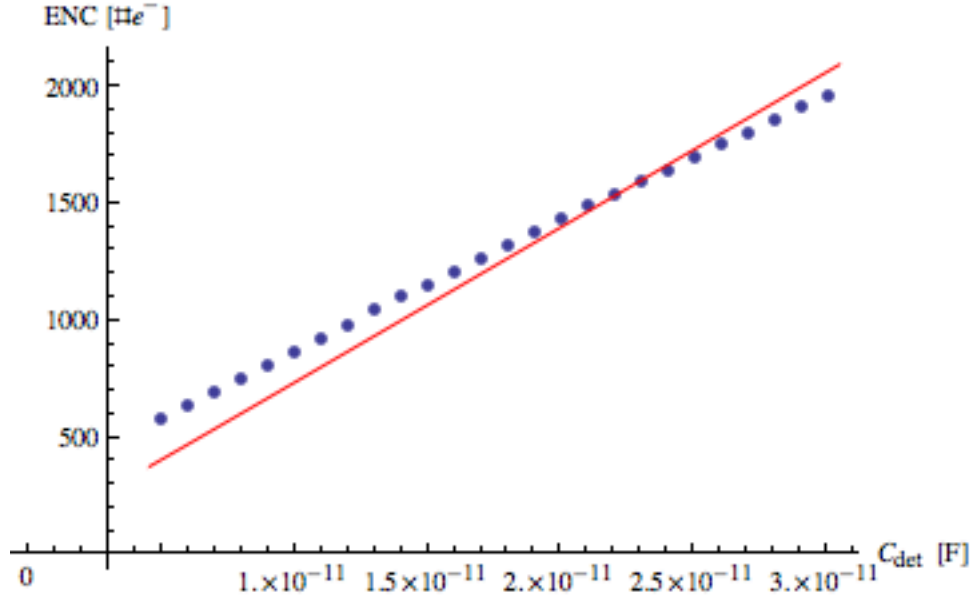


Figure 4.16: Comparison between simulation results and theoretical models.

where we have taken into account the total input capacitance  $C_T = C_{det} + C_{in} + C_f \approx C_{det} + 1pF$ , obtaining a percentage error of  $\sigma_{\%} = 11.9\%$ , that can be considered a reasonable result for a first evaluation. In this case we can see that the contribution of the parallel noise is well lower than the one of white and flicker noises, but this is true as far as we don't take into account the sensor leakage current that in the worst case could be very high ( $\sim \mu A$ ). In a more realistic case we must consider an additional term in the  $I_{nP}^2$  expression given by (2.75) reported below:

$$I_{n,leak}^2 = 2qI_{leak} = 3.2 \cdot 10^{-25} \frac{A^2}{Hz}$$

where we considered  $I_{leak} = 1\mu A$ . The Figure 4.17 shows that even in this case the noise doesn't rise so much to compromise the resolution:



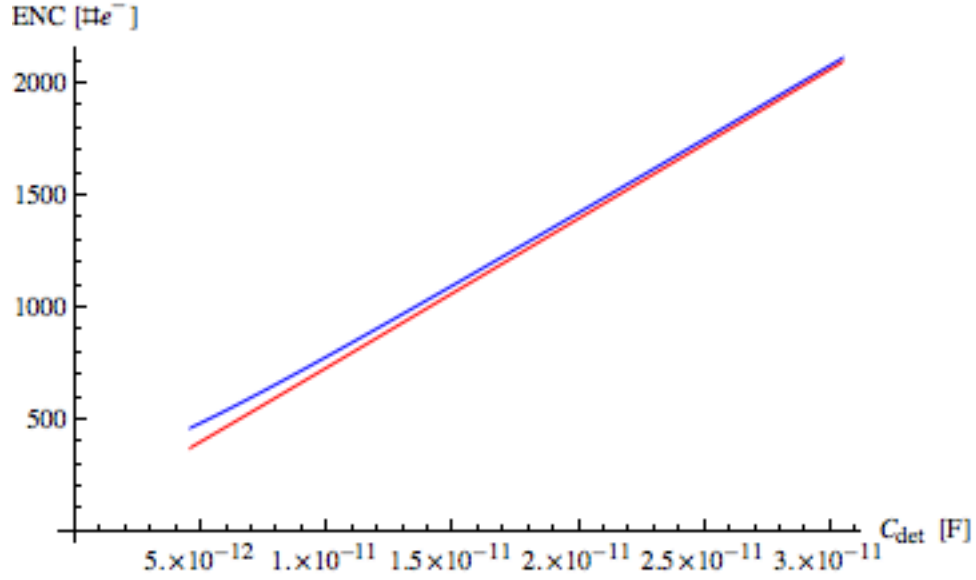


Figure 4.17: Comparison between theoretical models with (blue) and without (red) the sensor leakage current.

## 4.6 Comparator jitter

Jitter is defined as the deviation from the ideal timing of an event. We can evaluate this important parameter in two different ways. For both methods we'll calculate the total jitter as the root sum square of the jitter simulated for the leading and the trailing edges since the ToT technique is based on the difference of two time measures.

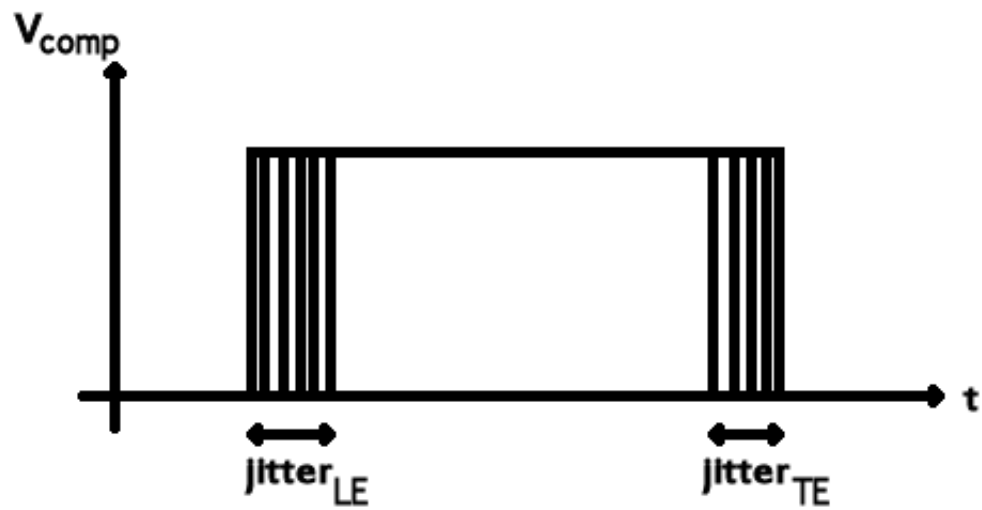
### Method 1

With an input signal corresponding to a charge  $Q_{in} = 4fC$ , we measured the slope of the signal coming out from the ToT Amplifier both for the leading and the trailing edges. The total jitter is then obtained through the following expression:

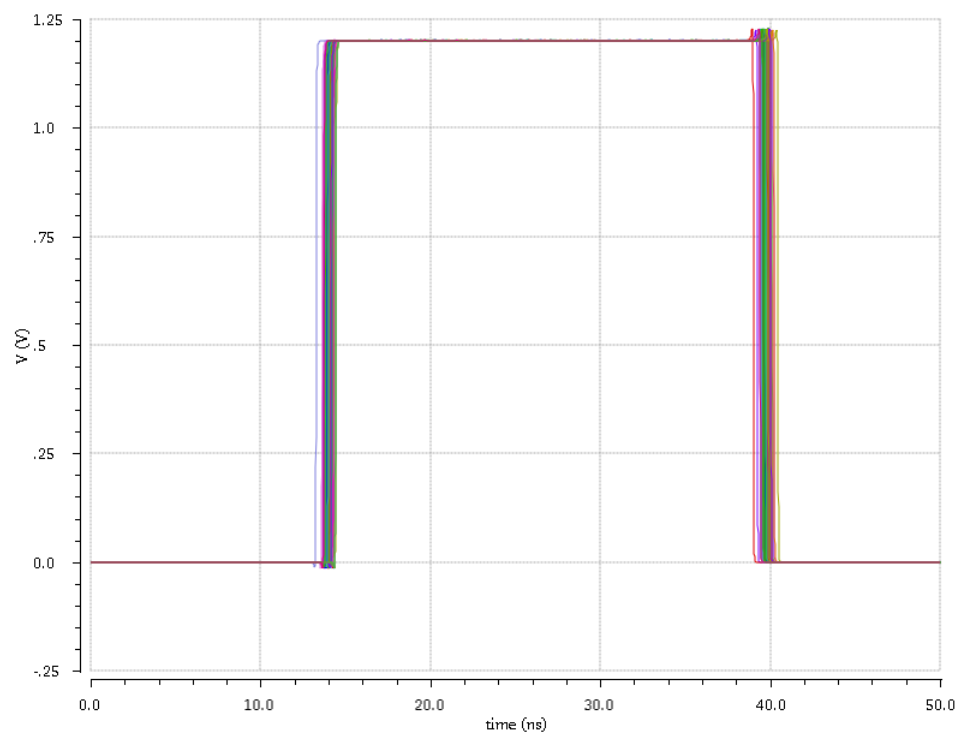
$$\begin{aligned}
 (\sigma_t)_1 &= \sqrt{\left(\frac{V_{n(out),rms}}{\frac{\partial V_{out}}{\partial t}}\right)_{LE}^2 + \left(\frac{V_{n(out),rms}}{\frac{\partial V_{out}}{\partial t}}\right)_{TE}^2} = \\
 &= \sqrt{\left(\frac{1.109 \cdot 10^{-3}}{5.559 \cdot 10^6}\right)^2 + \left(\frac{1.109 \cdot 10^{-3}}{5.048 \cdot 10^6}\right)^2} = 296.75ps
 \end{aligned} \tag{4.2}$$

### Method 2

In this case we performed a transient noise analysis measuring the peak-to-peak value both for the leading and the trailing edges as shown in Figure 4.18.



(a)



(b)

Figure 4.18: Jitter measure with method 2 theoretical principle (a) and simulation result (b).

The total jitter we get in this case is:

$$\begin{aligned}
 (\sigma_t)_2 &= \sqrt{\left(\frac{jitter_{LE}}{6}\right)^2 + \left(\frac{jitter_{TE}}{6}\right)^2} = \\
 &= \sqrt{\left(\frac{1.251 \cdot 10^{-9}}{6}\right)^2 + \left(\frac{1.249 \cdot 10^{-9}}{6}\right)^2} = 294.63ps
 \end{aligned} \tag{4.3}$$

The fact that  $jitter_{LE} \simeq jitter_{TE}$  is due to the fact that, with an input charge  $Q_{in} = 4fC$  the ToT Amplifier is not saturated and the output signal has a quite symmetrical shape. According to the results obtained with this two methods, we can conclude that the total jitter of the comparator is:

$$\sigma_t = (295.7 \pm 1.5) ps$$

We see that for a signal of  $Q_{in} = 4fC$  the average duration is  $\sim 26ns$ . This gives a signal-to-noise-ratio of

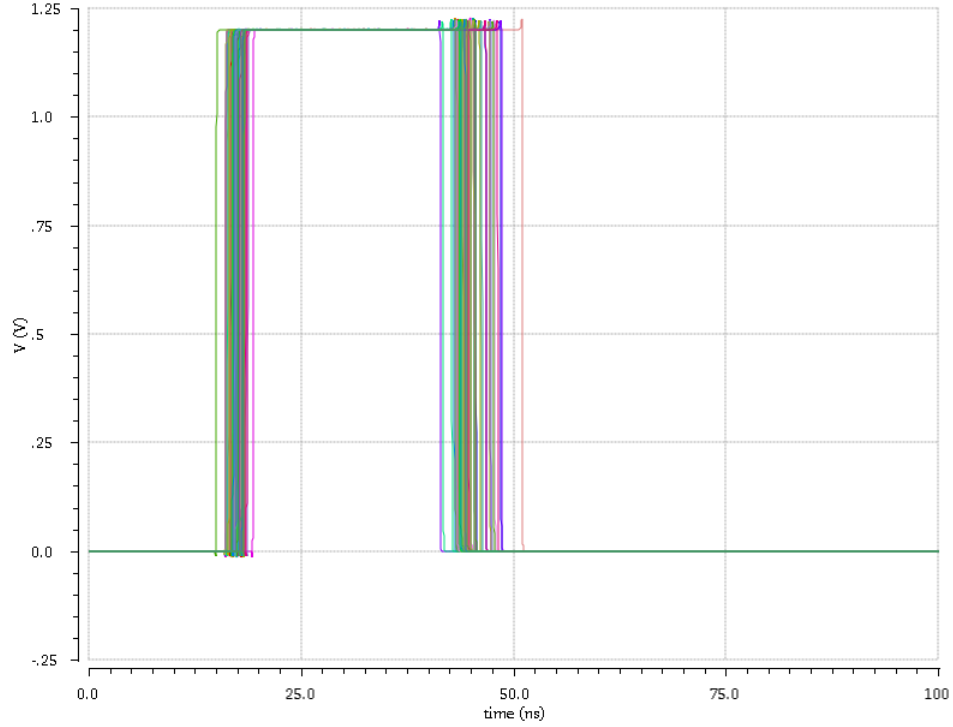
$$\frac{duration}{jitter} \approx \frac{26}{0.3} \approx 87$$

which is smaller than the value obtained through amplitude measures:

$$\frac{amplitude}{rmsNoise} = \frac{129.4}{1.109} \approx 117$$

This is due to the fact that the time measurements are based on a difference of two values both affected by noise, while in the amplitude measurements we only consider the noise at the peak. This hypothesis is confirmed by the observation that the two SNRs are scaled by a factor  $\sim \sqrt{2}$  coming from the root sum square of the noise errors in the jitter formula.

It is important to study the resolution of the ToT measurement also for the maximum expected sensor capacitance, that will yield a significantly higher noise. The result with an input capacitance  $C_{det} = 30pF$  is shown in Figure 4.19:

Figure 4.19: Jitter simulated with  $C_{det} = 30pF$ .

Proceeding as before, we can calculate that the total jitter in this case is:

$$\sigma'_t = (1.5 \pm 0.4) ns$$

The SNR evaluated with the formulas above are:

$$\frac{duration}{jitter} \approx \frac{26}{1.5} \approx 17$$

and

$$\frac{amplitude}{rmsNoise} = \frac{74.63}{2.843} \approx 26$$

that again differs for a factor  $\sim \sqrt{2}$ . We can conclude that the system provides an adequate resolution even in the worst case.

## Conclusions

The aim of this thesis is to explore the possibility of applying a high resolution time-based architecture to the readout of microstrip sensors at high rates. The basic idea is to exploit Time over Threshold measurements. However, to obtain large dynamic range and high rates, the front-end signals duration should be kept as short as possible. The signal duration is then measured with low-power Time to Digital Converters. In this thesis the possibility of having a front-end which allows a linear ToT measurement was explored. Non-linear systems could also be considered since they are easier to design from the electronics point of view. However, its calibration can be cumbersome, hence in this work the design of a linear front-end has been studied. It is important to stress that the linearity we are interested in a time-based measurement is not the one between the input charge and the signal peak, but that between the input charge and the signal duration. Considering that the implemented architecture, widely described in Chapter 3, is only a first design representing the starting point for the next future analysis, the results we obtained can be considered quite satisfying. The goals we aim at regard, above all, the improvement of the linearity for low input charges and the design of architectures to handle with signals with different polarities. The linearity can be improved by increasing the gain of the full chain, in such a way that the feedback transistor of the ToT stage works in saturation already for the minimum charges of interest. This can be achieved in different ways: increasing the gain of the first stage, of the current buffer and of the ToT stage or a combination of all the above. In principle, increasing the gain in the first stage is more advantageous, because it improves also the signal to noise ratio. However, one must be careful in not saturating the input stage, which would increase significantly the cross-talk. Increasing the gain in the first stage or in the current buffer increases also the DC current that must be handled by the baseline holder. Therefore, an increase of the gain of the ToT stage by reducing its feedback capacitance could be the best solution. In the present design such a capacitance has a fairly large value ( $C_{f,ToT} = 600\text{fF}$ ) due to the need of compensating the operational amplifier used in the ToT stage, but this value could be reduced by improving the design of the OTA. Another important point is that the circuit must serve double sided silicon sensor, which are delivering signal of opposite polarity if the electronics is connected to the n-side or the p-side. It is planned to handle this issue just by acting on the topology on the input stage, by selecting between two complementary feedback networks. The design should be done in such a way that the architecture of the current buffer and of the ToT stage do not need to be changed.

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