A Low-Power Front-End Amplifier for the Microstrip Sensors of the PANDA Microvertex Detector

Tesi Magistrale

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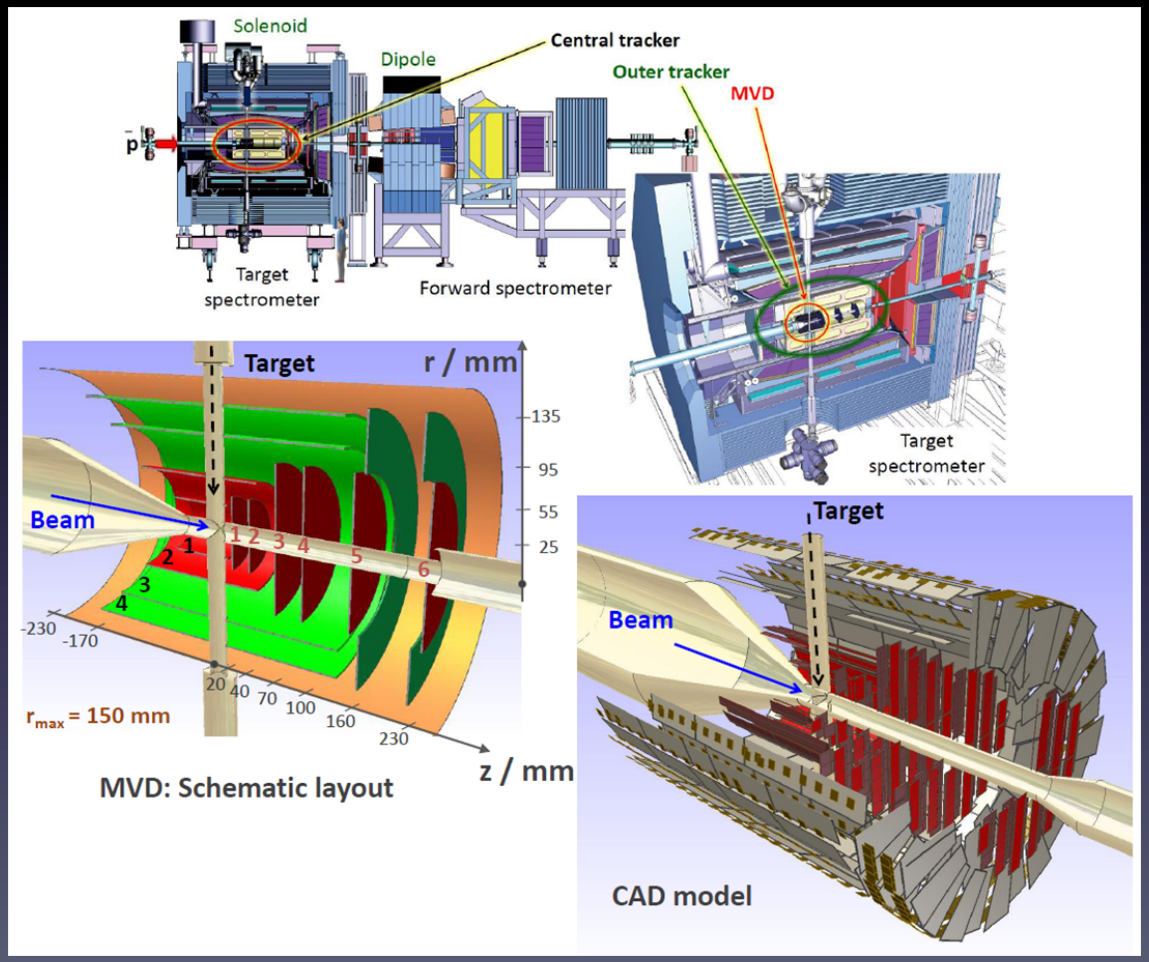
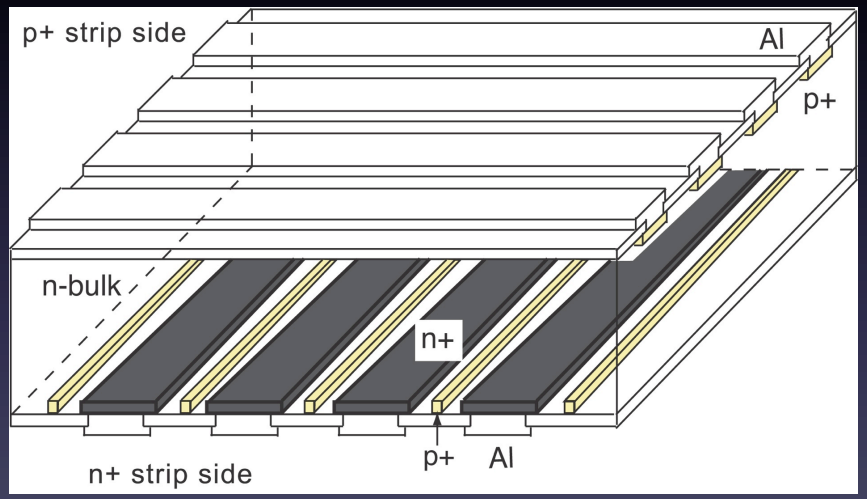
Relatore: Angelo Rivetti

Microvertex Detector

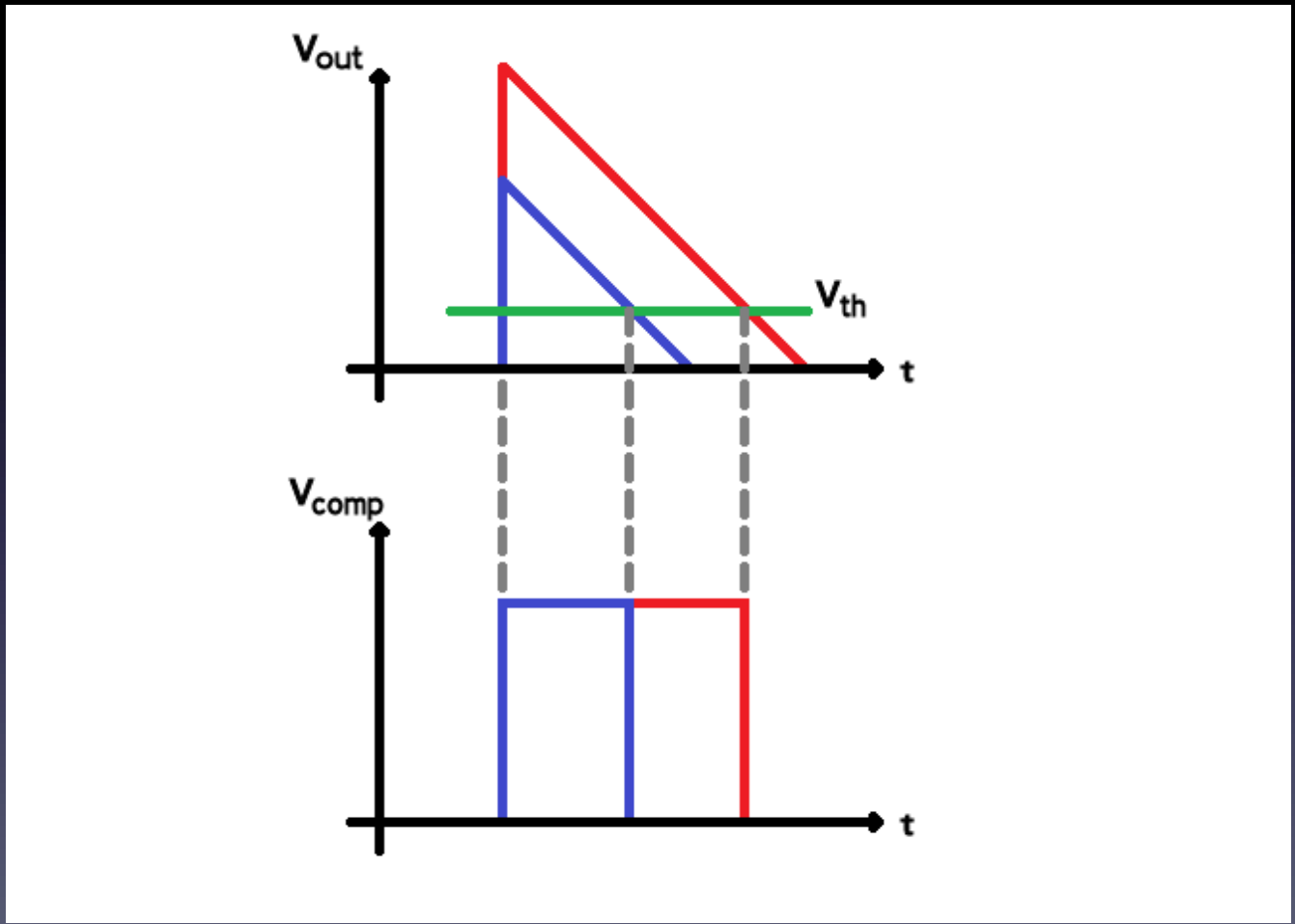


Microstrip Sensors requirements

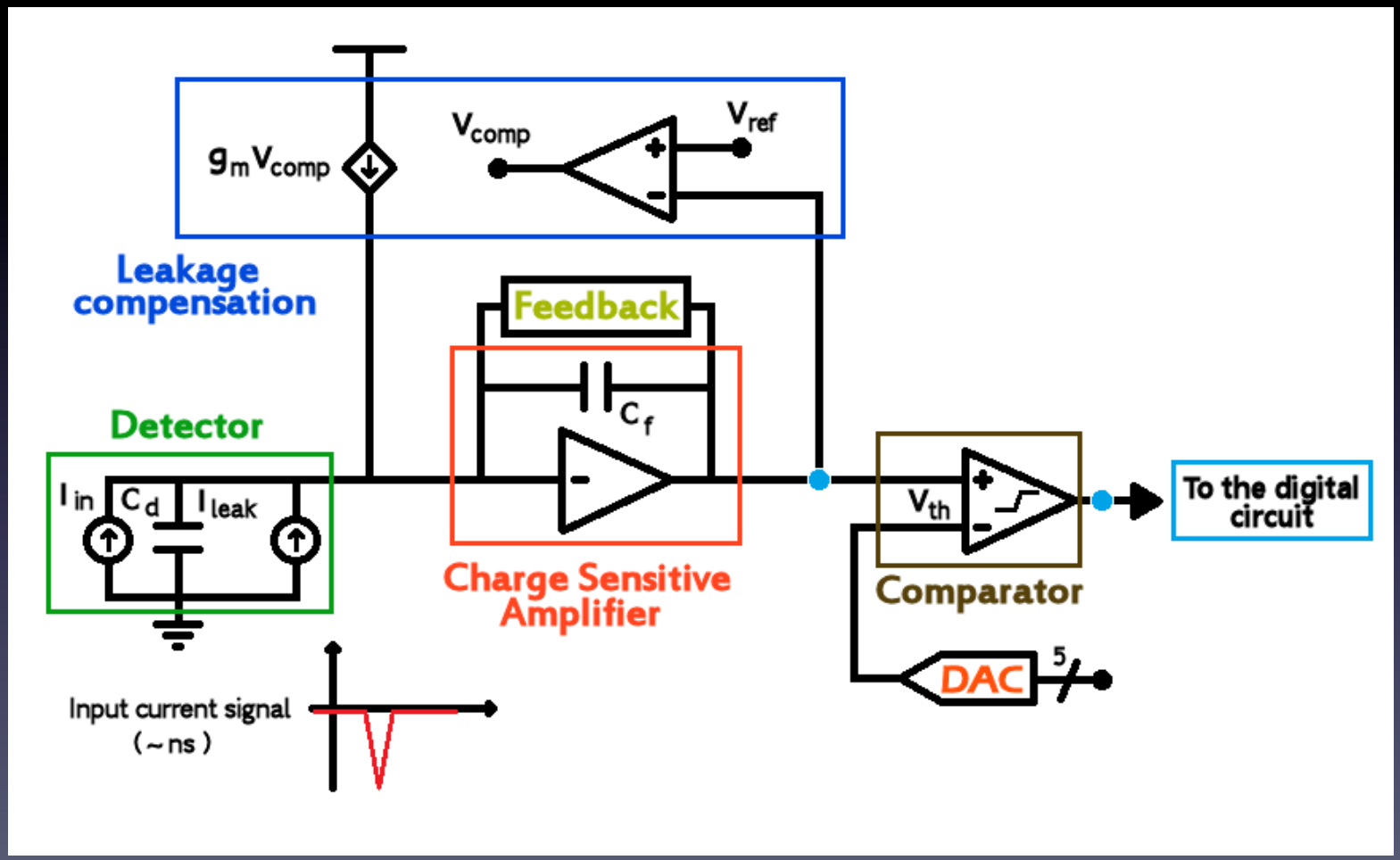


- Specifications
  - Length ~ 8-10 cm
  - Width ~ 60-80 μm
  - Pitch ~ 100 μm
  - C_{det} ~ 5-30 pF
- Goals
  - Dynamic range ~ 9 bits
  - Noise < 2000 e^-
  - Power consumption ≤ 4 mW/ch

ToT technique



Pixel readout cell

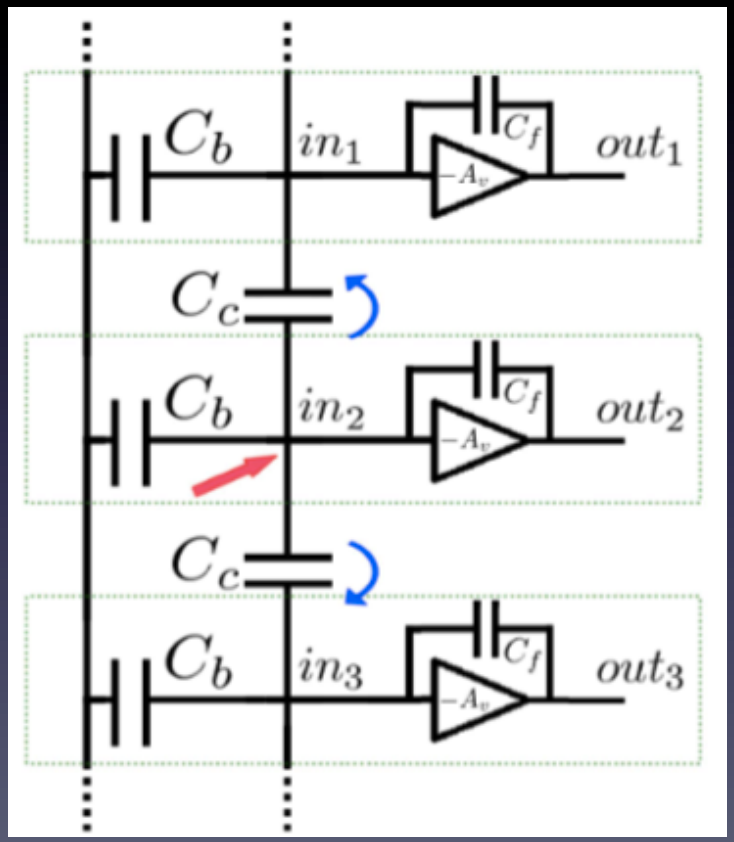


Pixels vs Strips

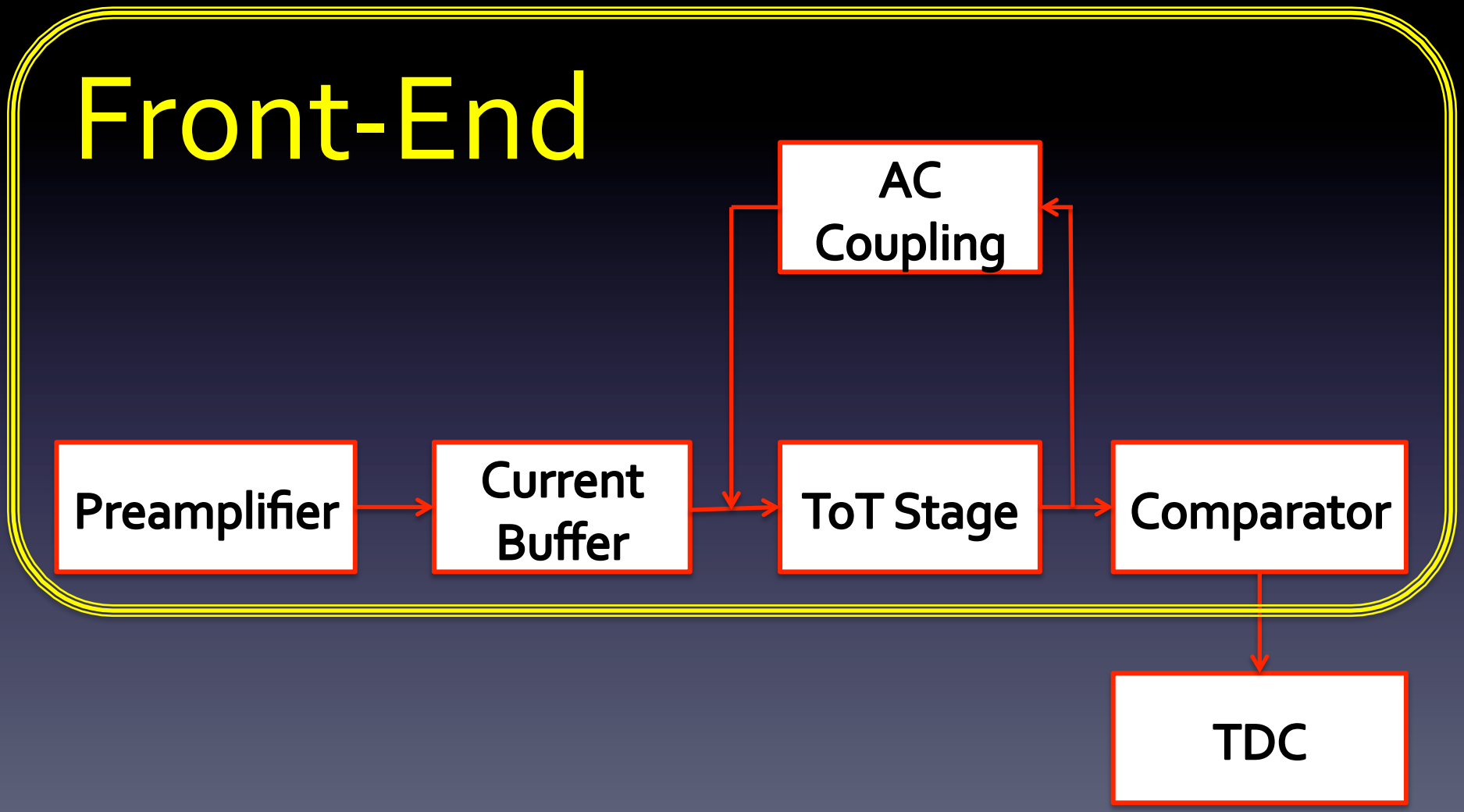
Speed

- Pixels event rate ~ 1 kHz
- Strips event rate ~ 30 kHz

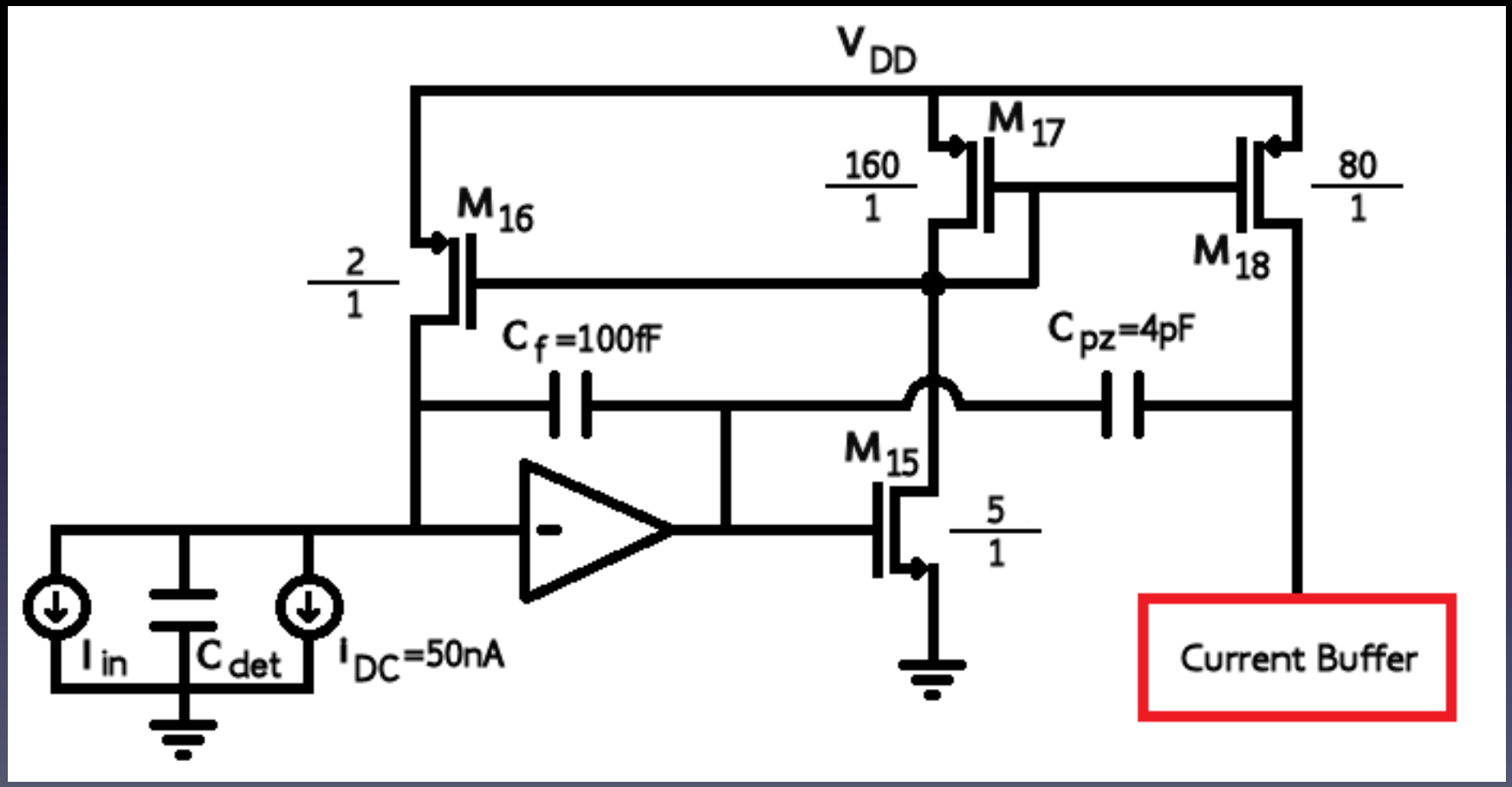
Cross-talk



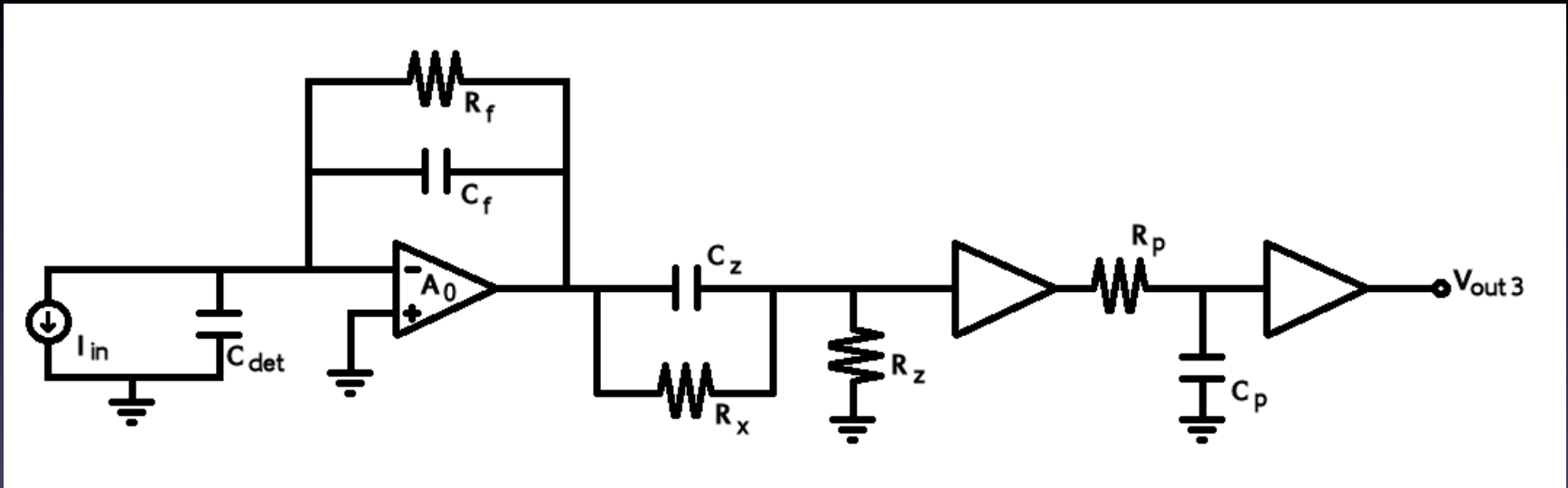
Implemented input stage



Implemented FE Stage: CSA

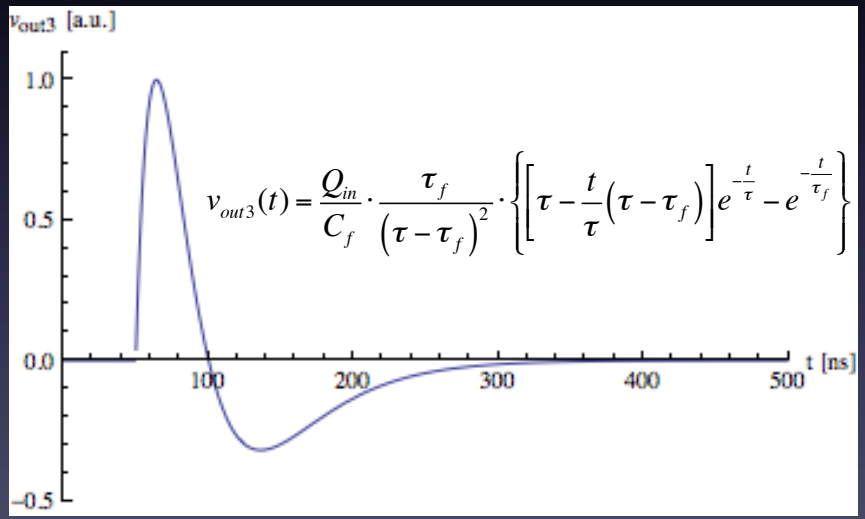


Pole-zero cancellation (1)



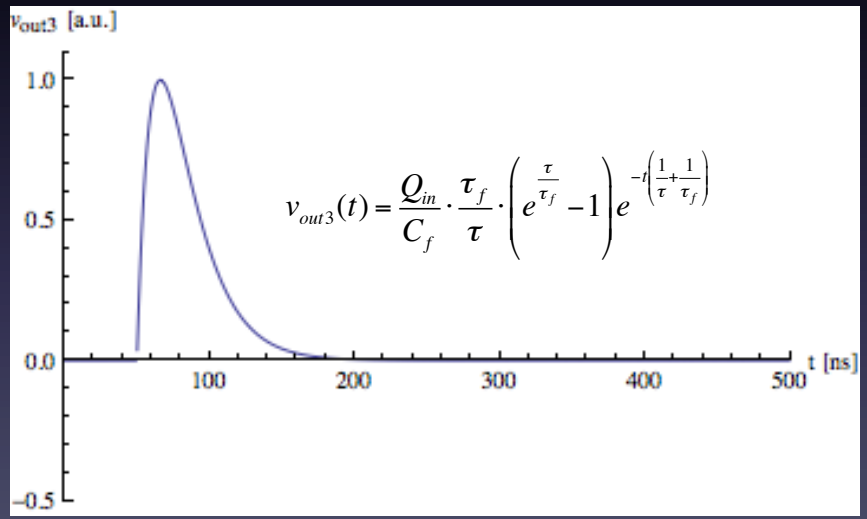
Pole-zero cancellation (2)

Without cancellation



$$H_3(s) = \frac{Q_{in}}{C_f} \cdot \frac{\tau_f}{1 + s\tau_f} \cdot \frac{s\tau}{1 + s\tau} \cdot \frac{1}{1 + s\tau}$$

With cancellation



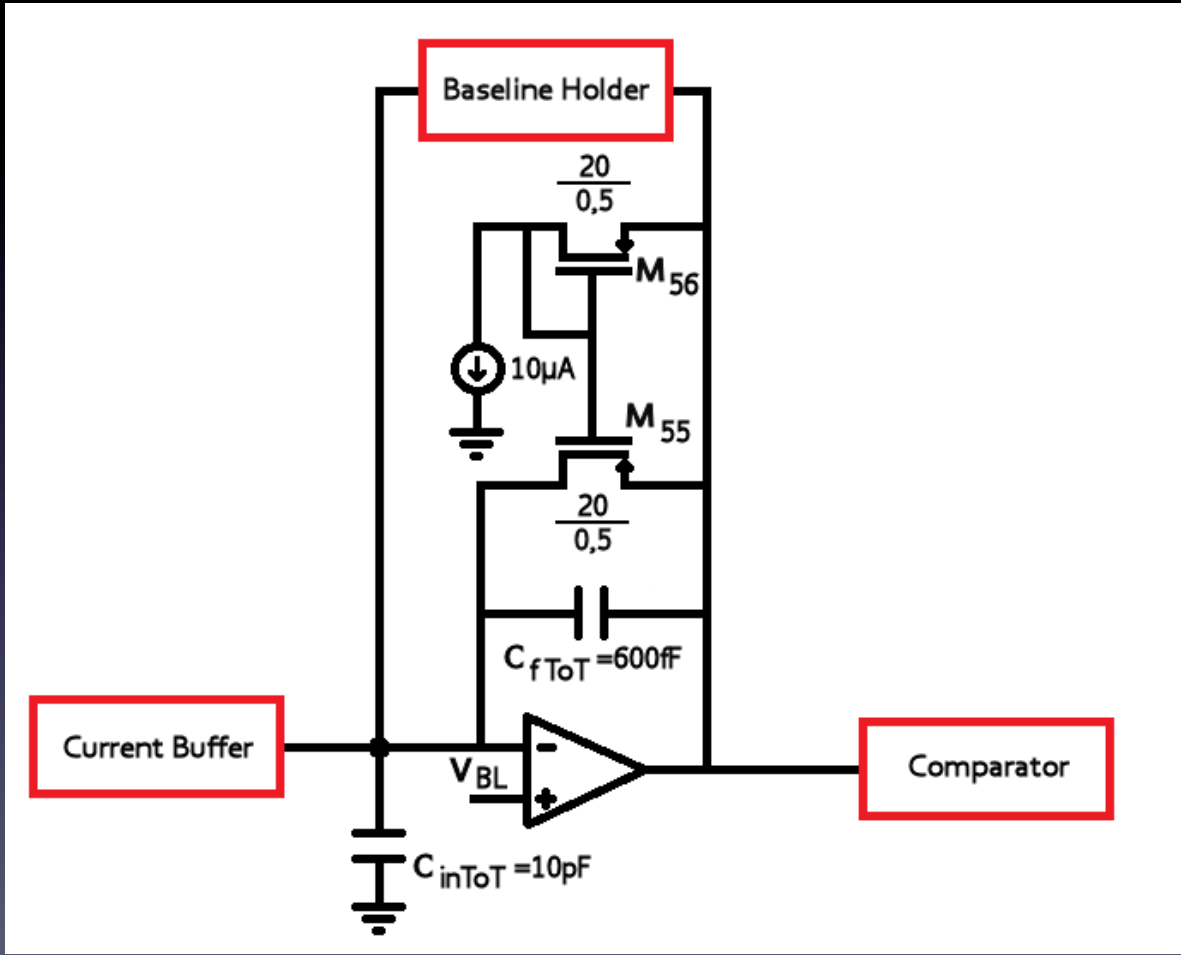
$$H_3(s) = \frac{Q_{in}}{C_f} \cdot \frac{\tau}{1 + s\tau\left(1 + \frac{1}{s\tau_f}\right)} \cdot \frac{1}{1 + s\tau}$$

Implemented pole-zero cancellation

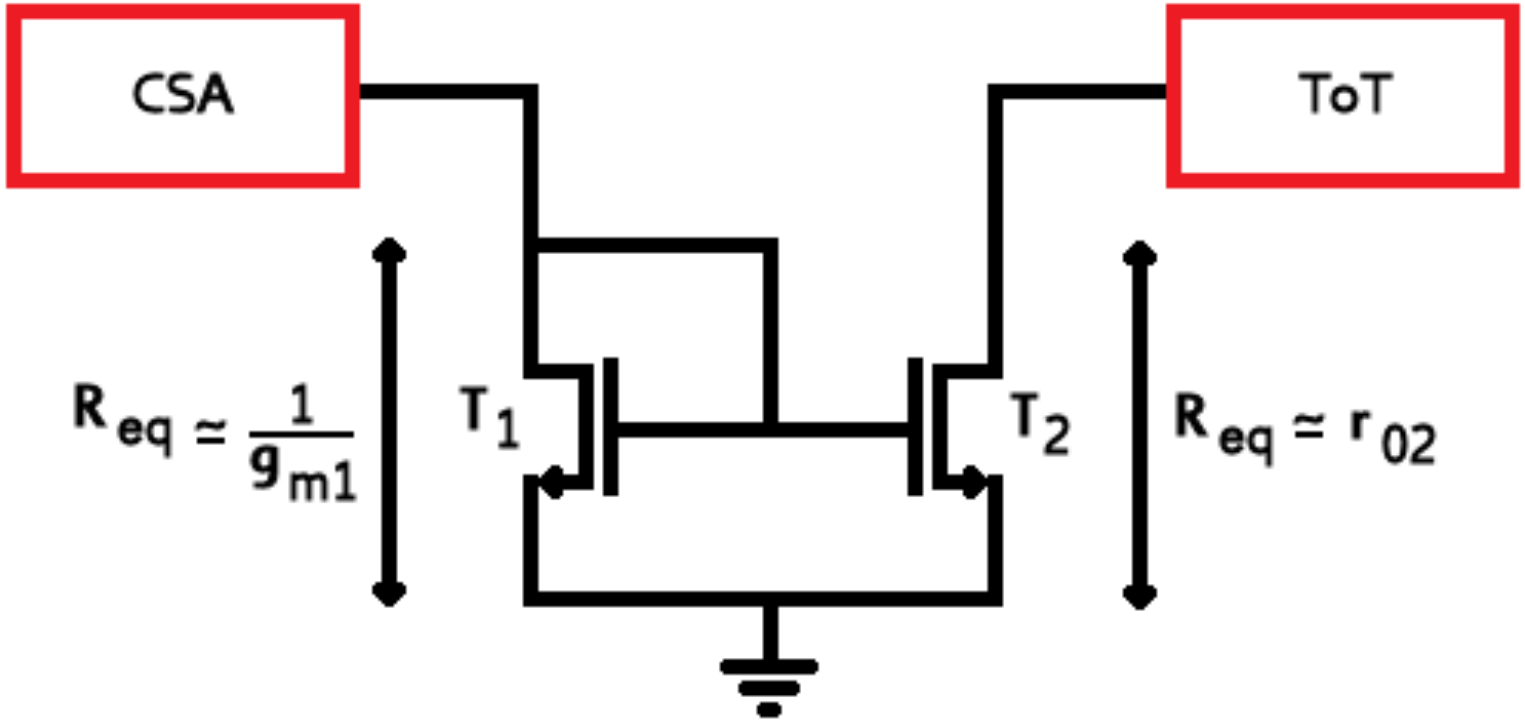
- $$\left(R_f\right)_{eq} = \frac{v_{preamp}}{I_f} = \left(\frac{g_{m17}}{g_{m16}}\right) \cdot \frac{1}{g_{m15}}$$
- $$\left(R_x\right)_{eq} = \frac{v_{out}}{I_{out}} = \left(\frac{g_{m17}}{g_{m18}}\right) \cdot \frac{1}{g_{m15}}$$
- $$\frac{g_{m17}}{g_{m16}} = 80$$
- $$\frac{g_{m17}}{g_{m18}} = 2$$

$$\frac{\left(R_f\right)_{eq}}{\left(R_x\right)_{eq}} = \frac{C_{pz}}{C_f} = 40$$

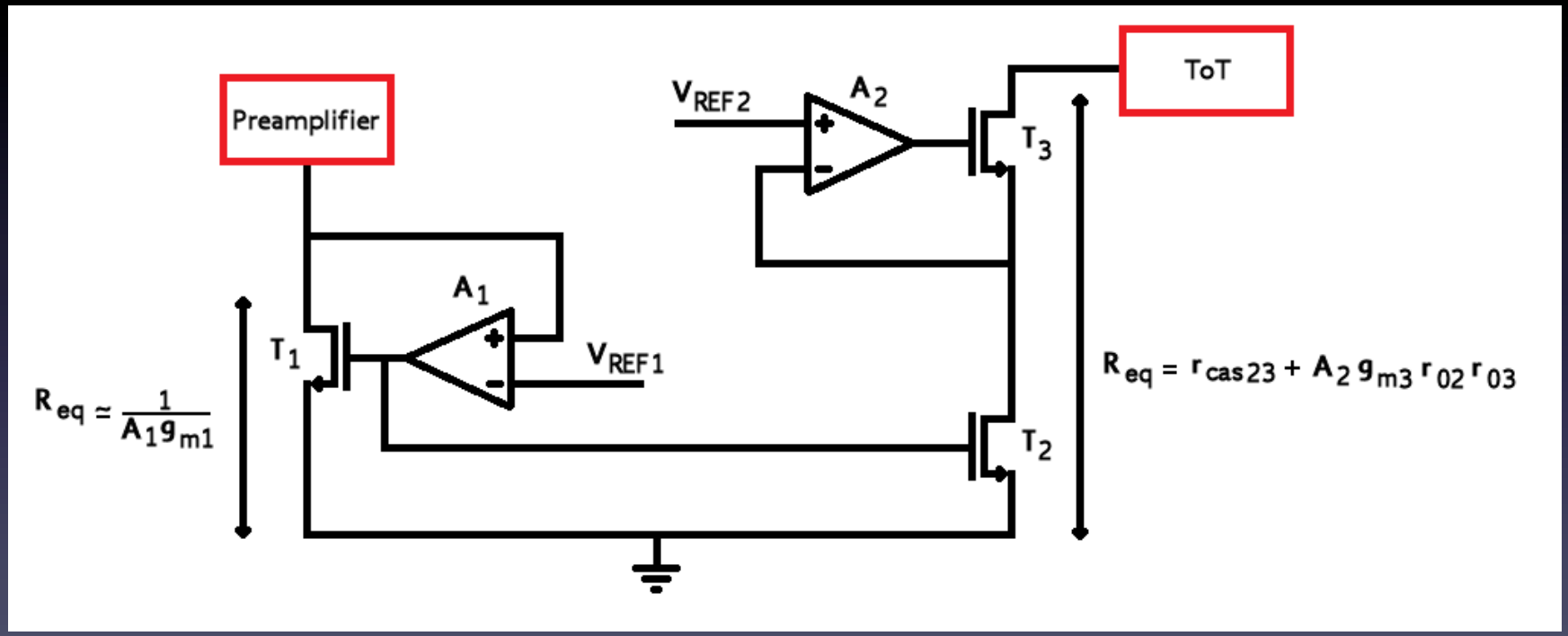
Implemented FE stage: ToT Stage



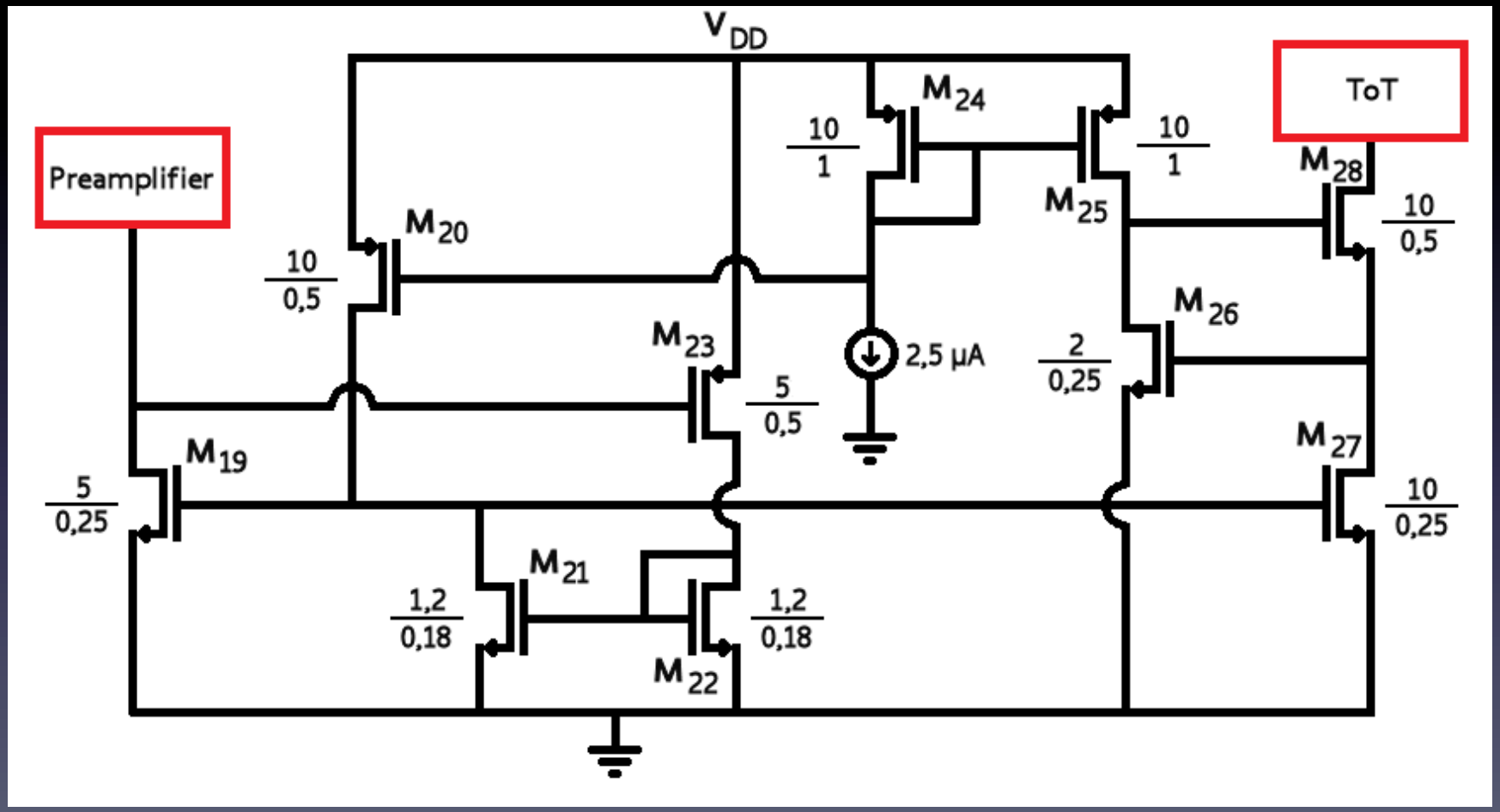
Current Buffer



Current Buffer with g_m-boosting

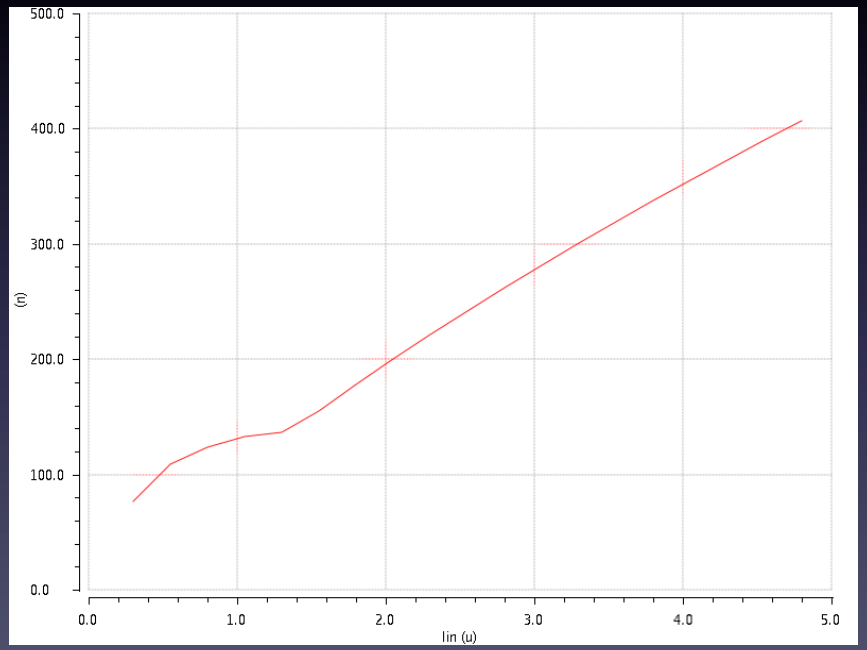


Implemented FE stage: Current Buffer (1)

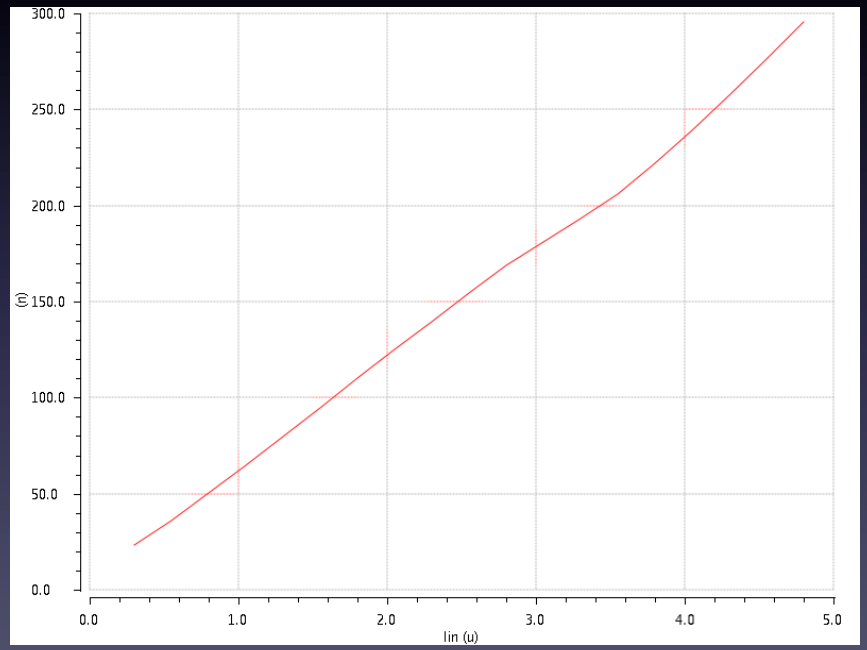


Implemented FE stage: Current Buffer (2)

Without g_m-boosting



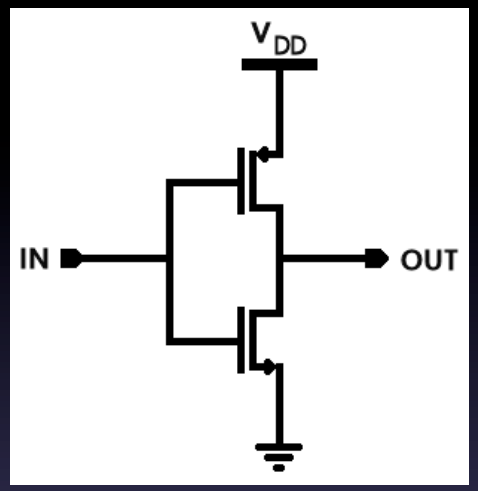
With g_m-boosting

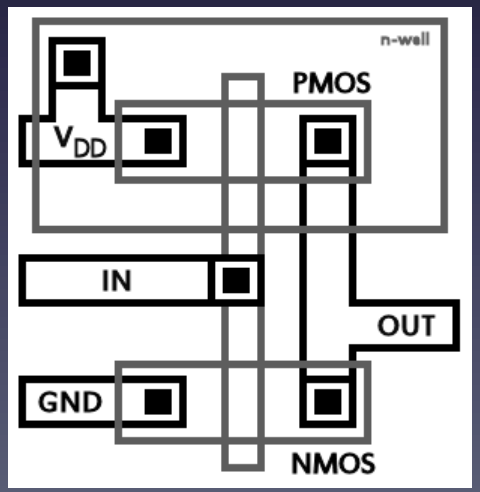


IC implementation flow

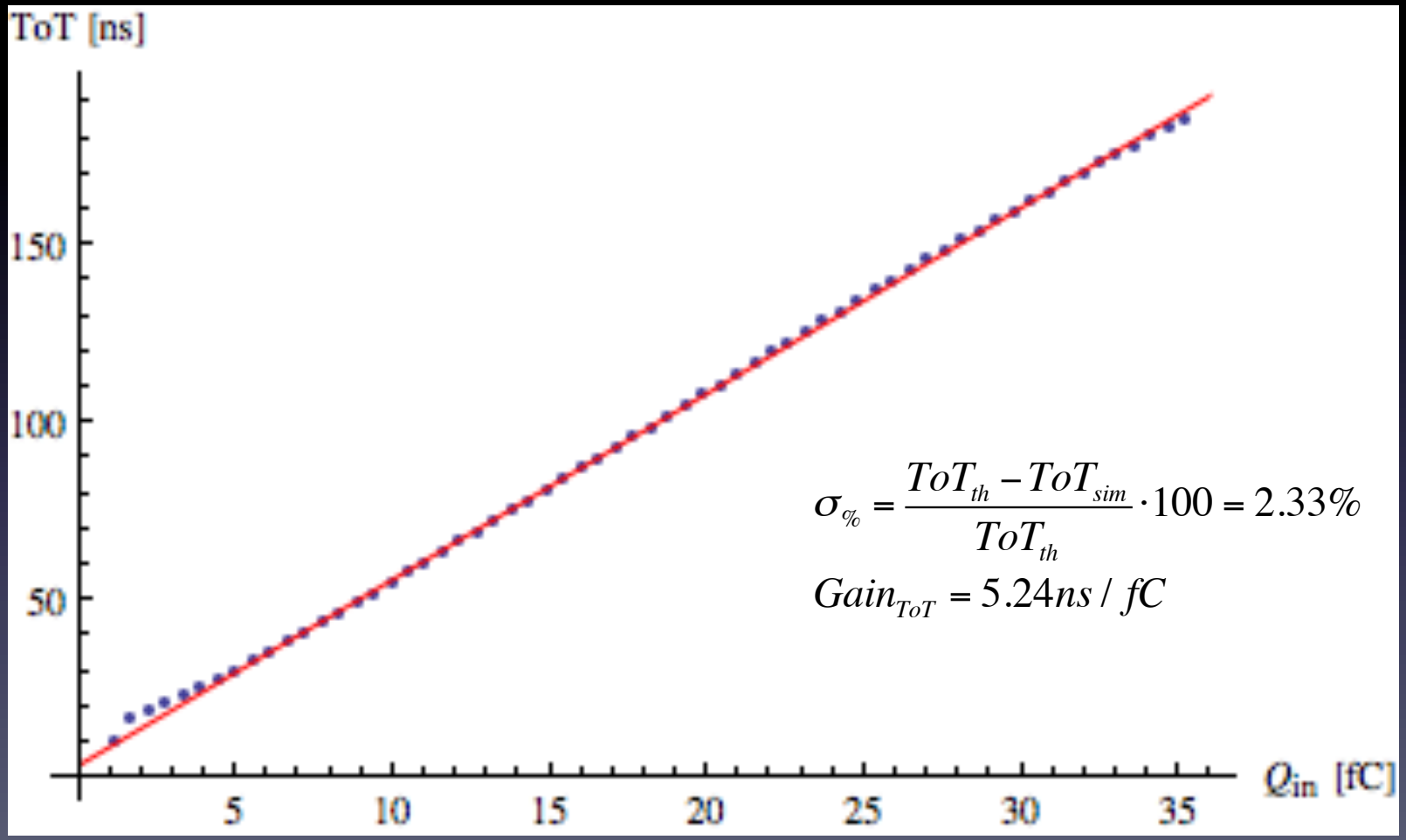
- Schematic design
- Layout design
- Post-layout verification
  - Simulations with passives
  - LVS (Layout VS Schematic)
- Manifacturing (~ 3 months)
- Typical manpower involved

  ~ 10 years man





Simulations: Linearity

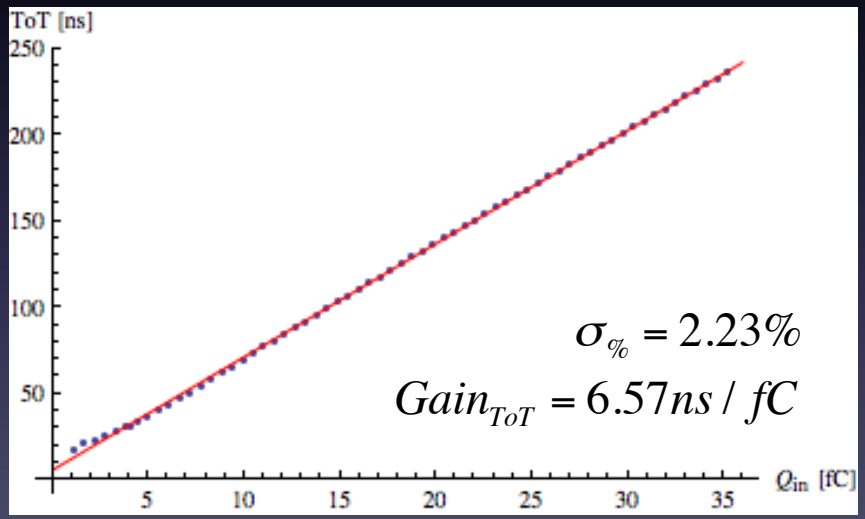


$$\sigma_{\%} = \frac{ToT_{th} - ToT_{sim}}{ToT_{th}} \cdot 100 = 2.33\%$$

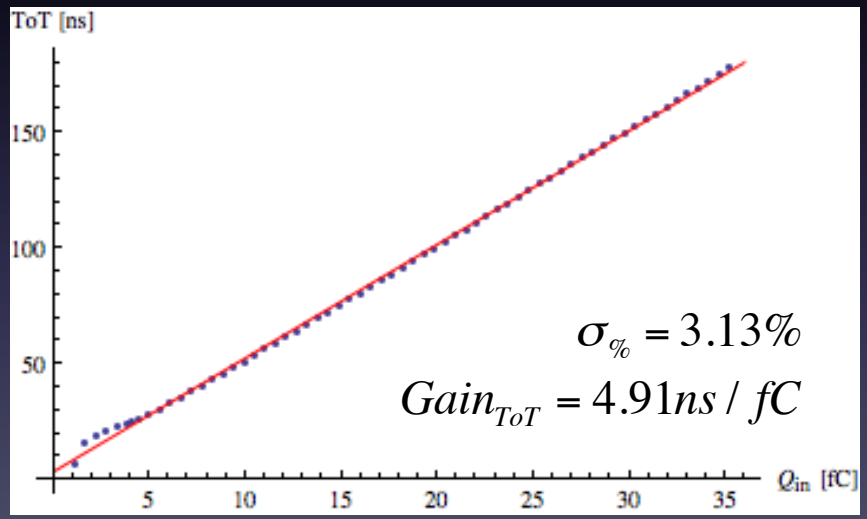
$$Gain_{ToT} = 5.24 ns / fC$$

Simulations: Corner Process

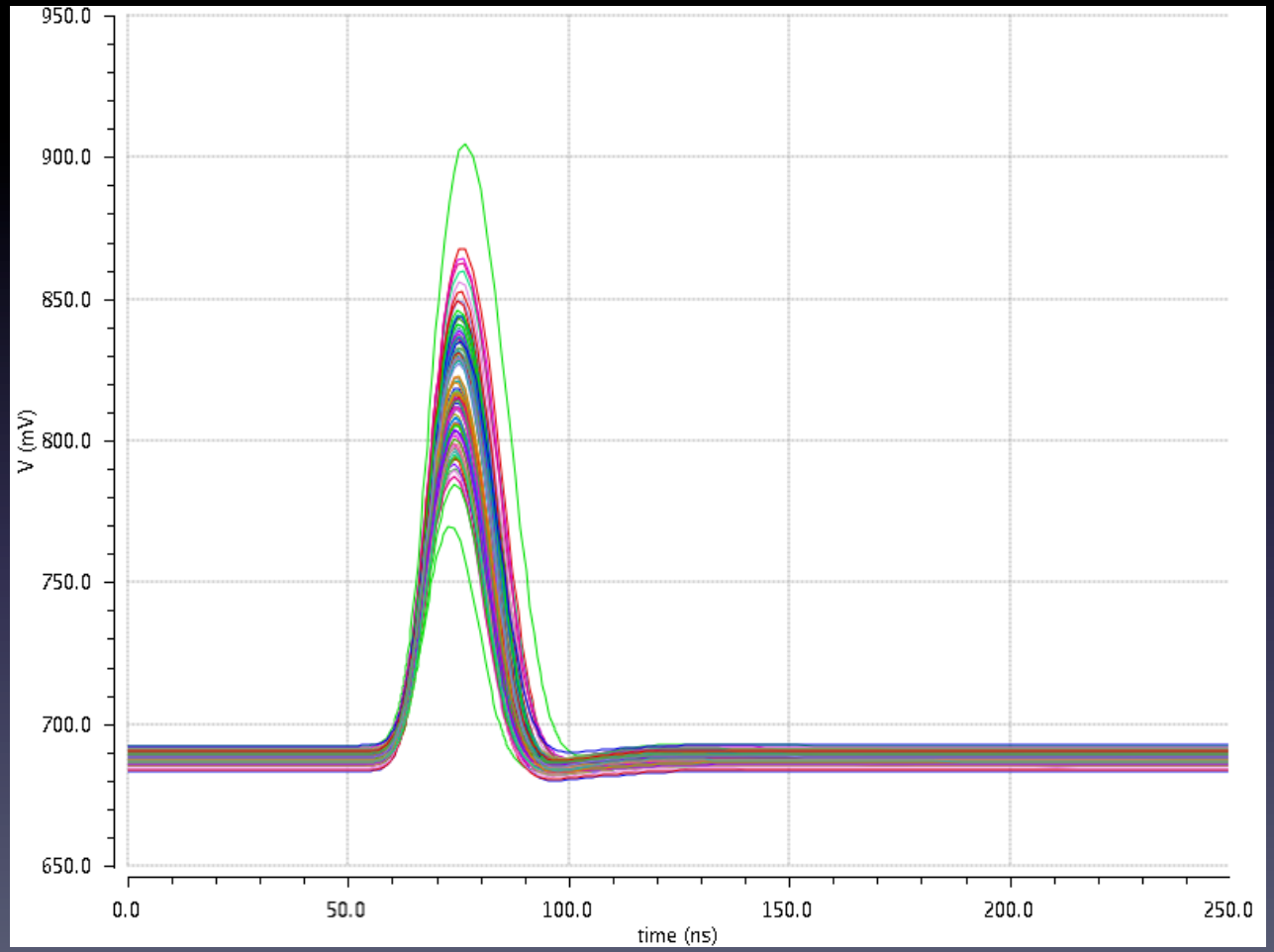
Slow-Slow configuration



Fast-Fast configuration

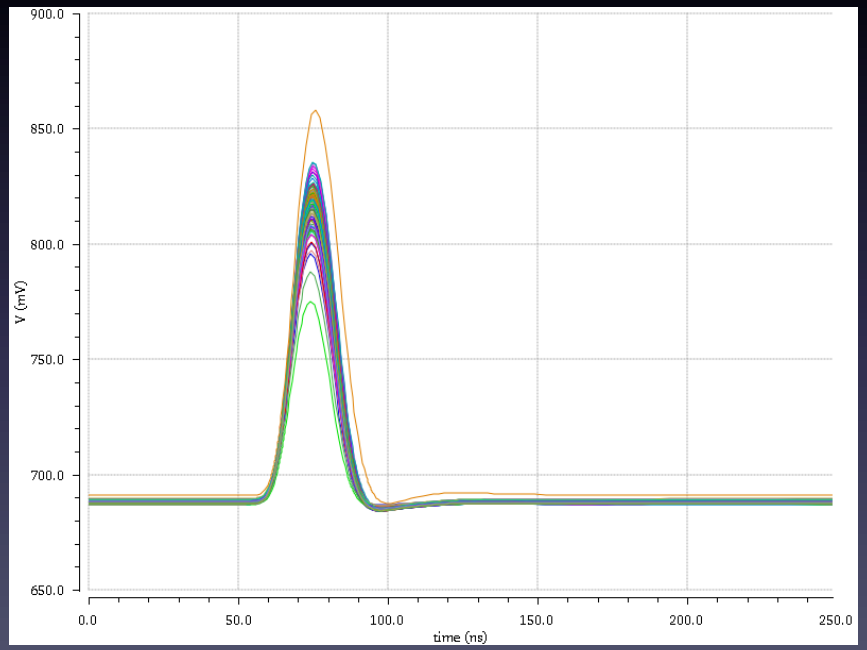


Simulations: Monte Carlo (1)

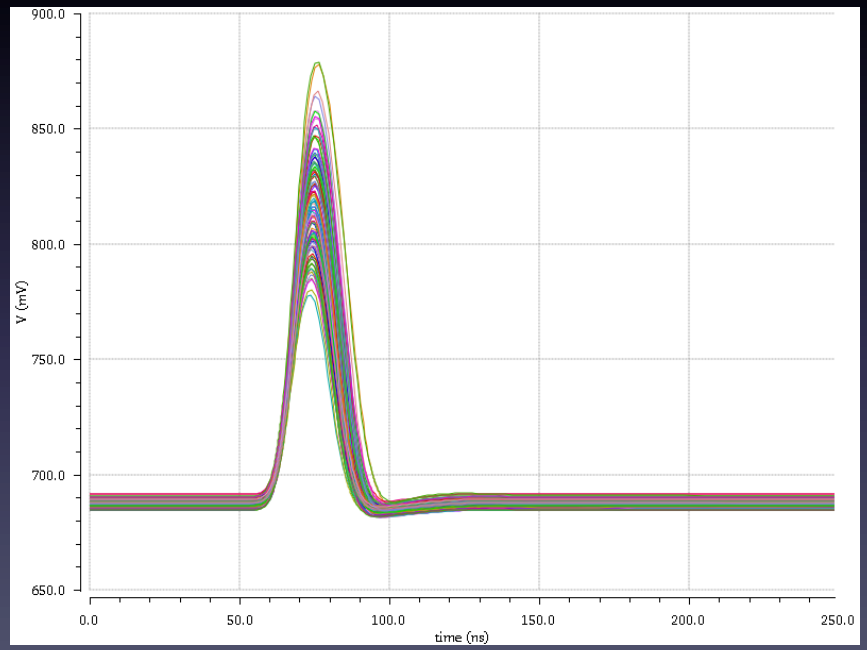


Simulations: Monte Carlo (2)

Process variations

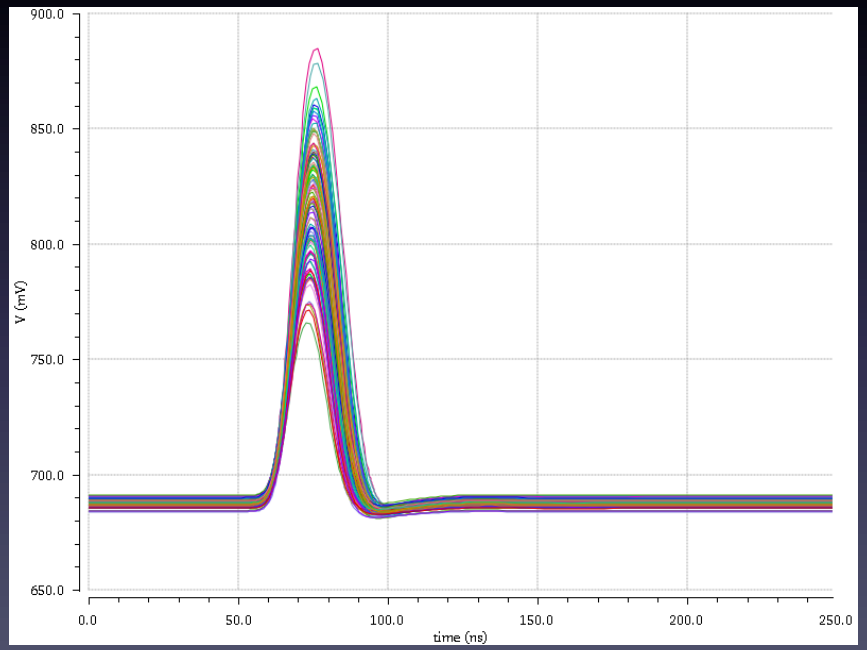


Mismatch variations

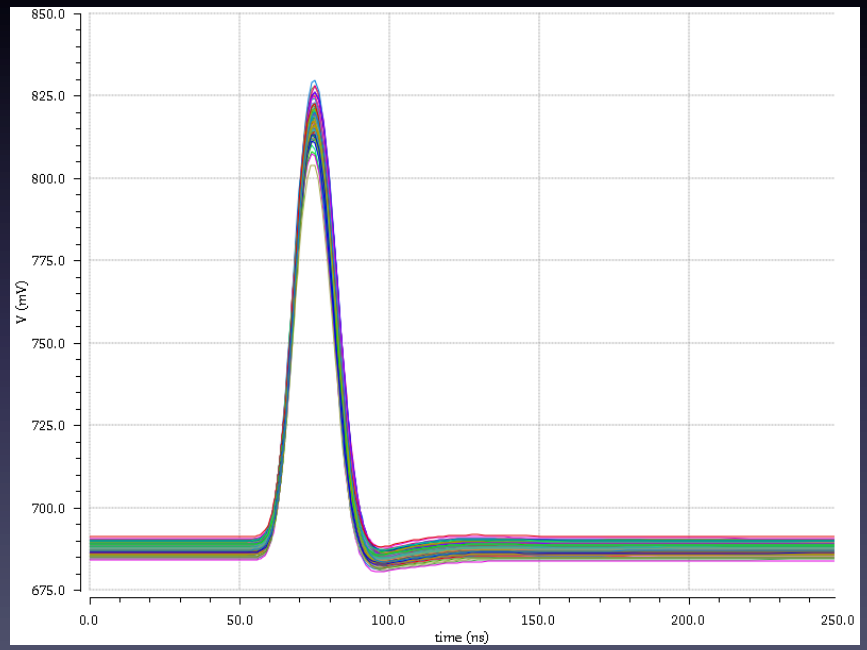


Simulations: Monte Carlo (3)

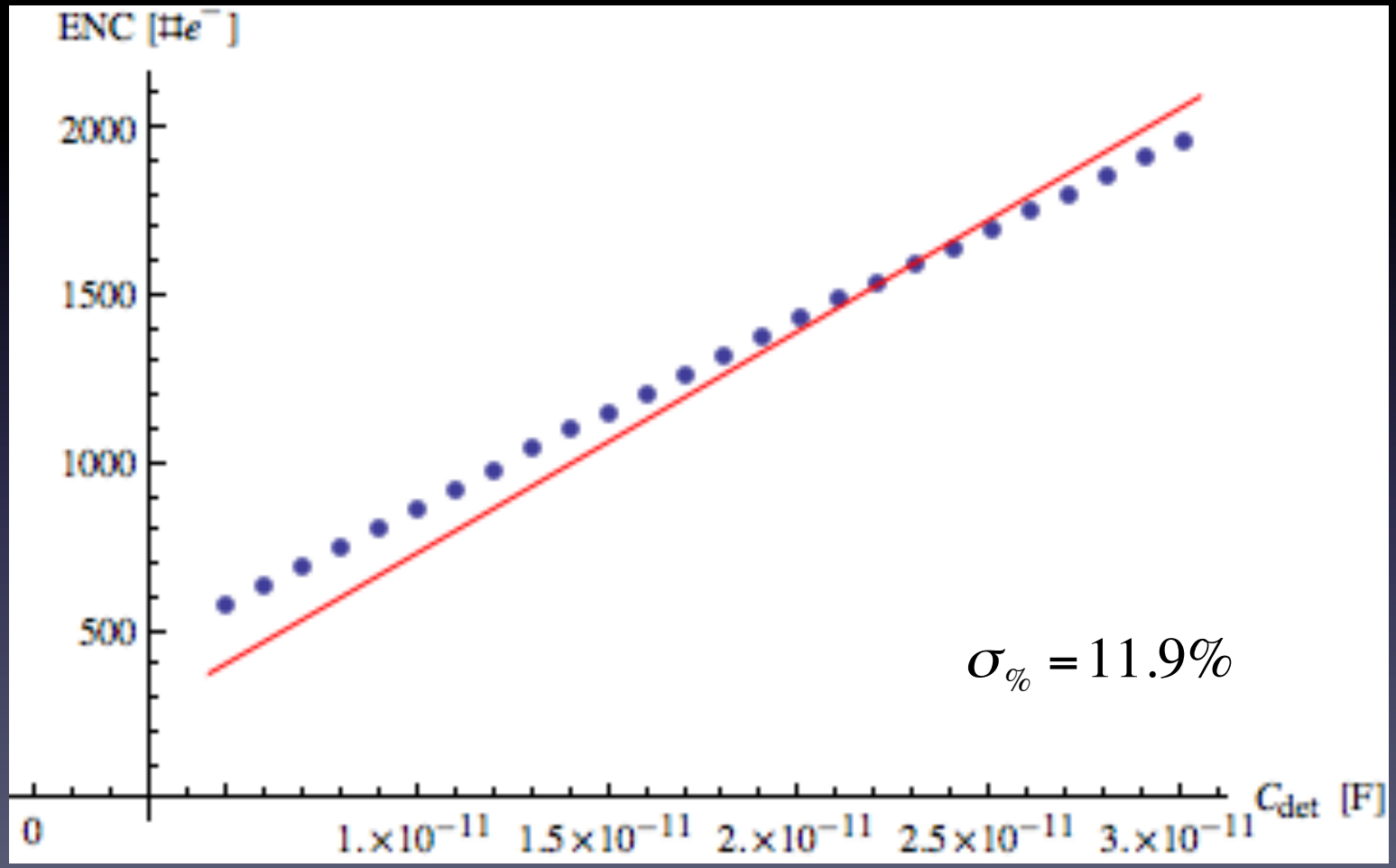
MC without input biasing current mirror



MC without current buffer current mirror



Simulations: Noise



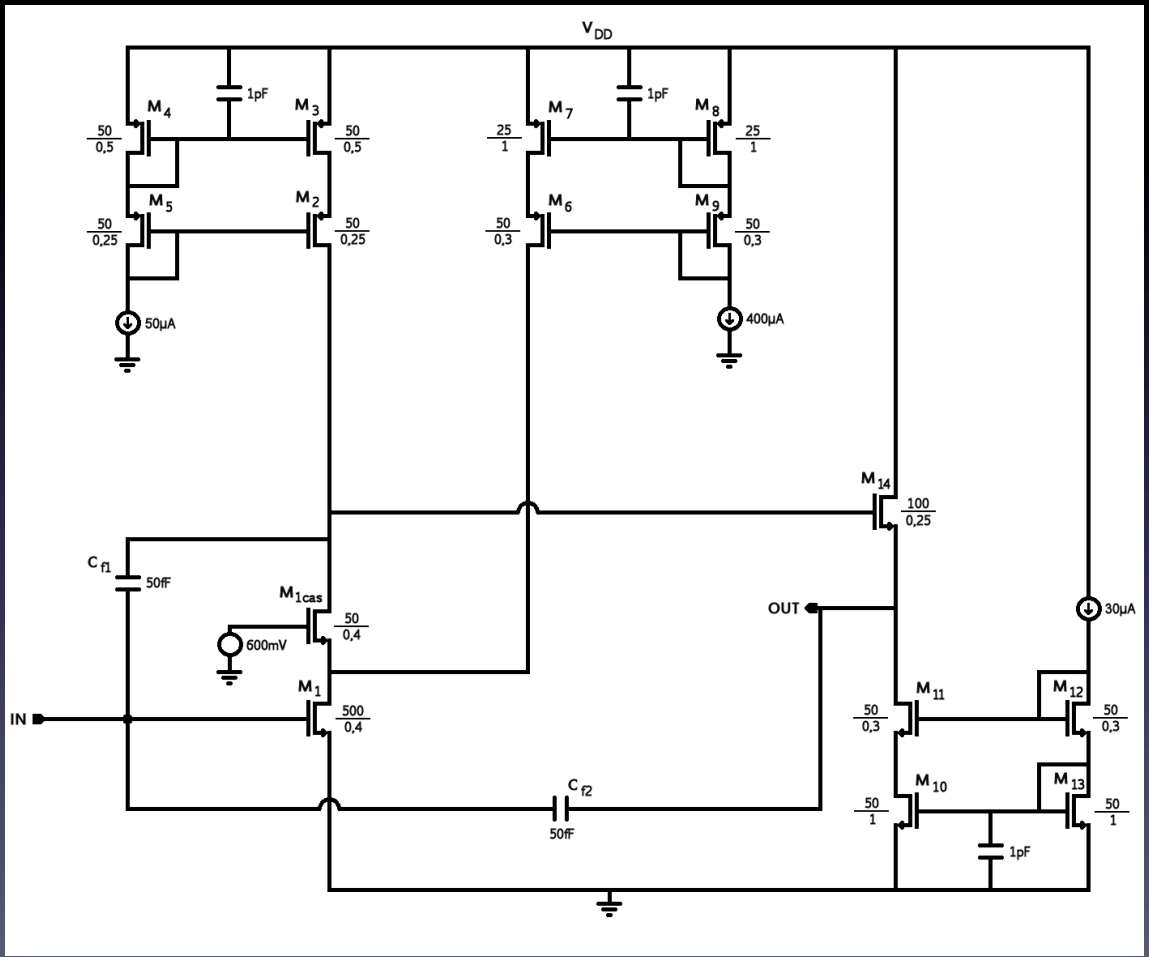
Conclusions and perspectives

- Matching between electronics and physics simulations (performed by my German collegues)
- Improvement of the ToT stage output linearity
- Topology adjustment to process signals of both polarities
- Layout design

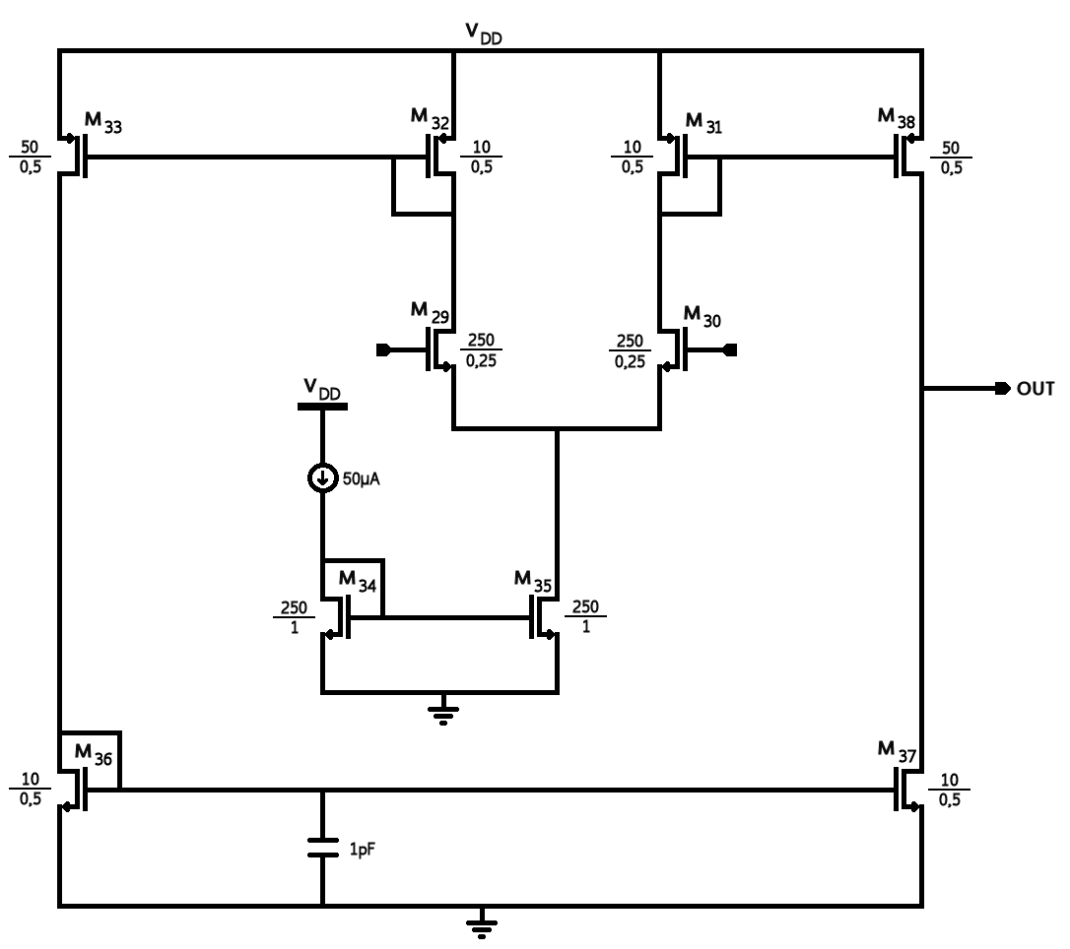

Thank you for your
kind attention

Backup Slides

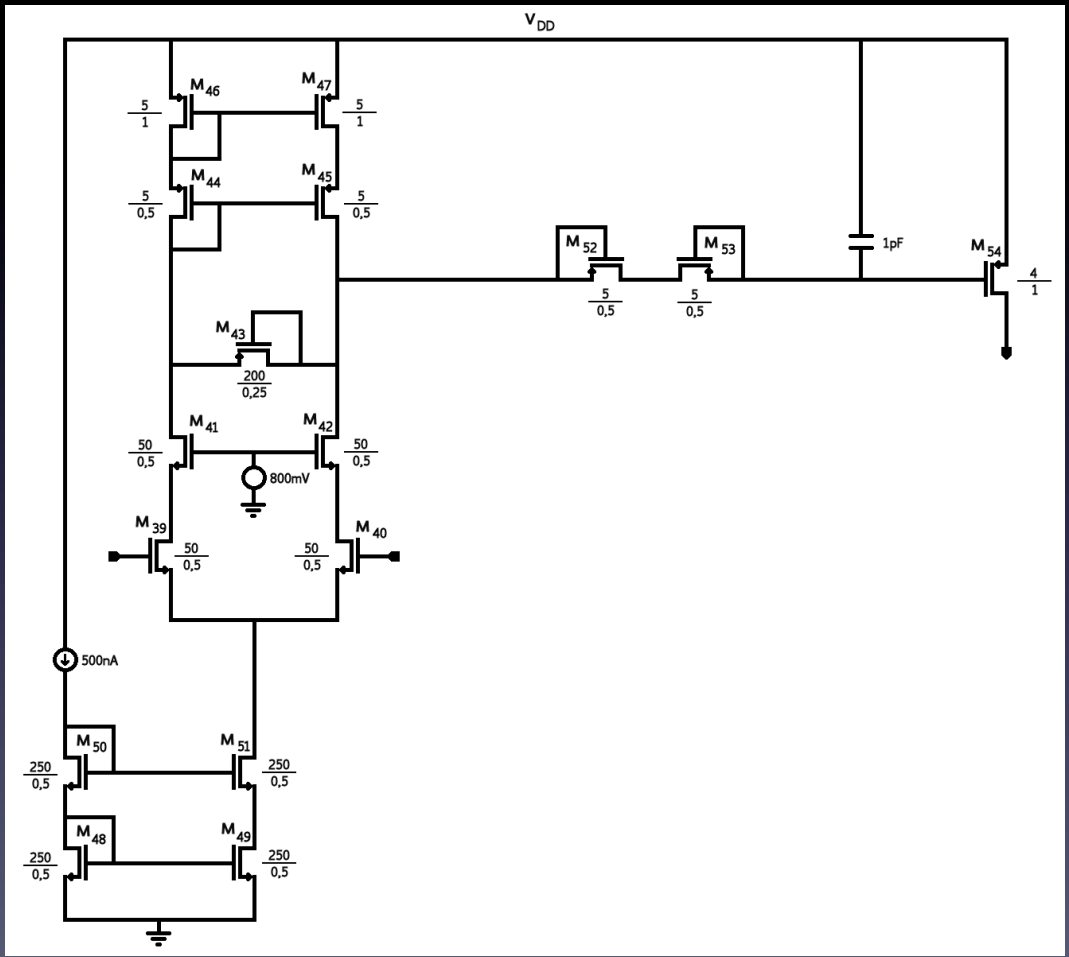
CSA schematic



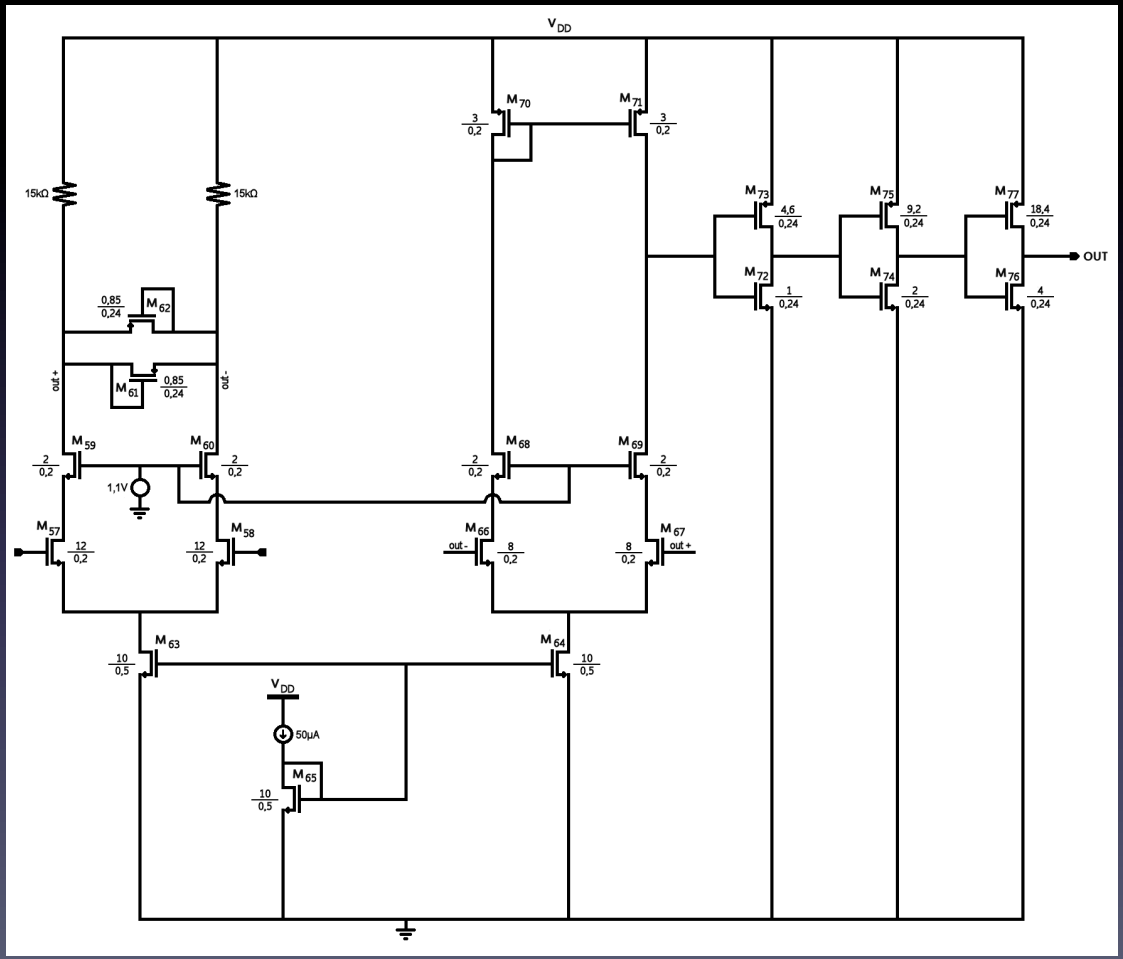
ToT Amplifier schematic



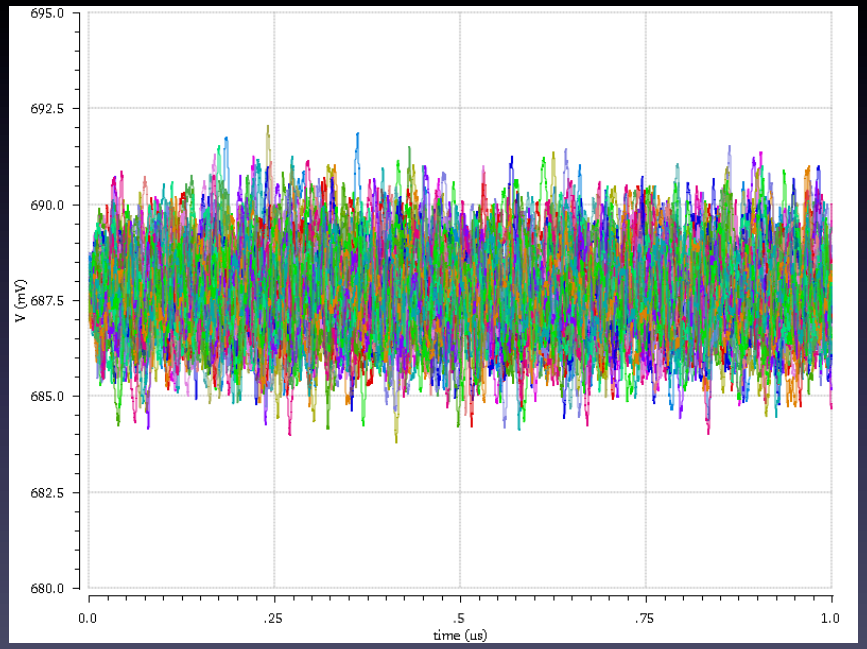
Baseline Holder schematic

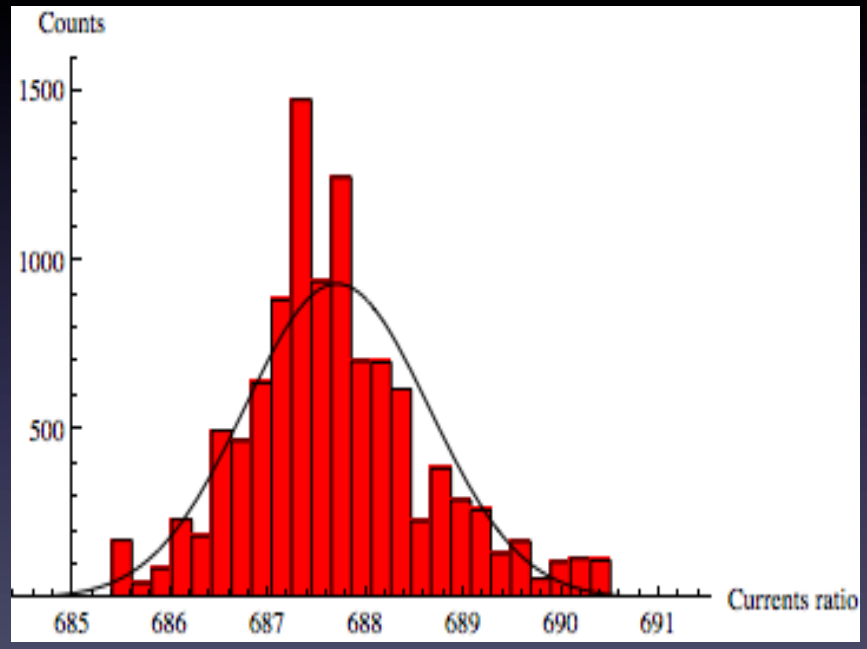


Comparator schematic

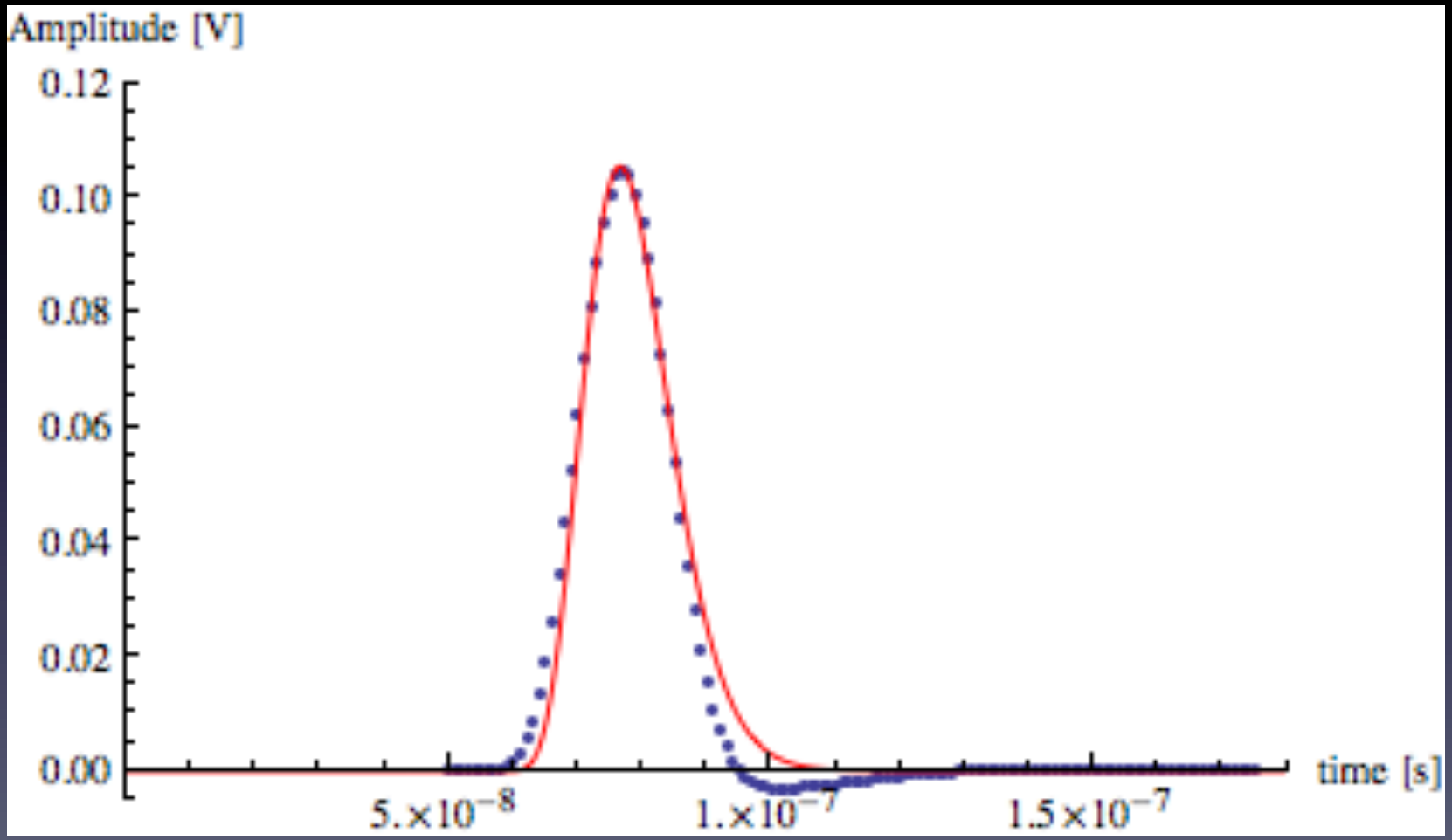


Simulations: Gaussian noise (1)

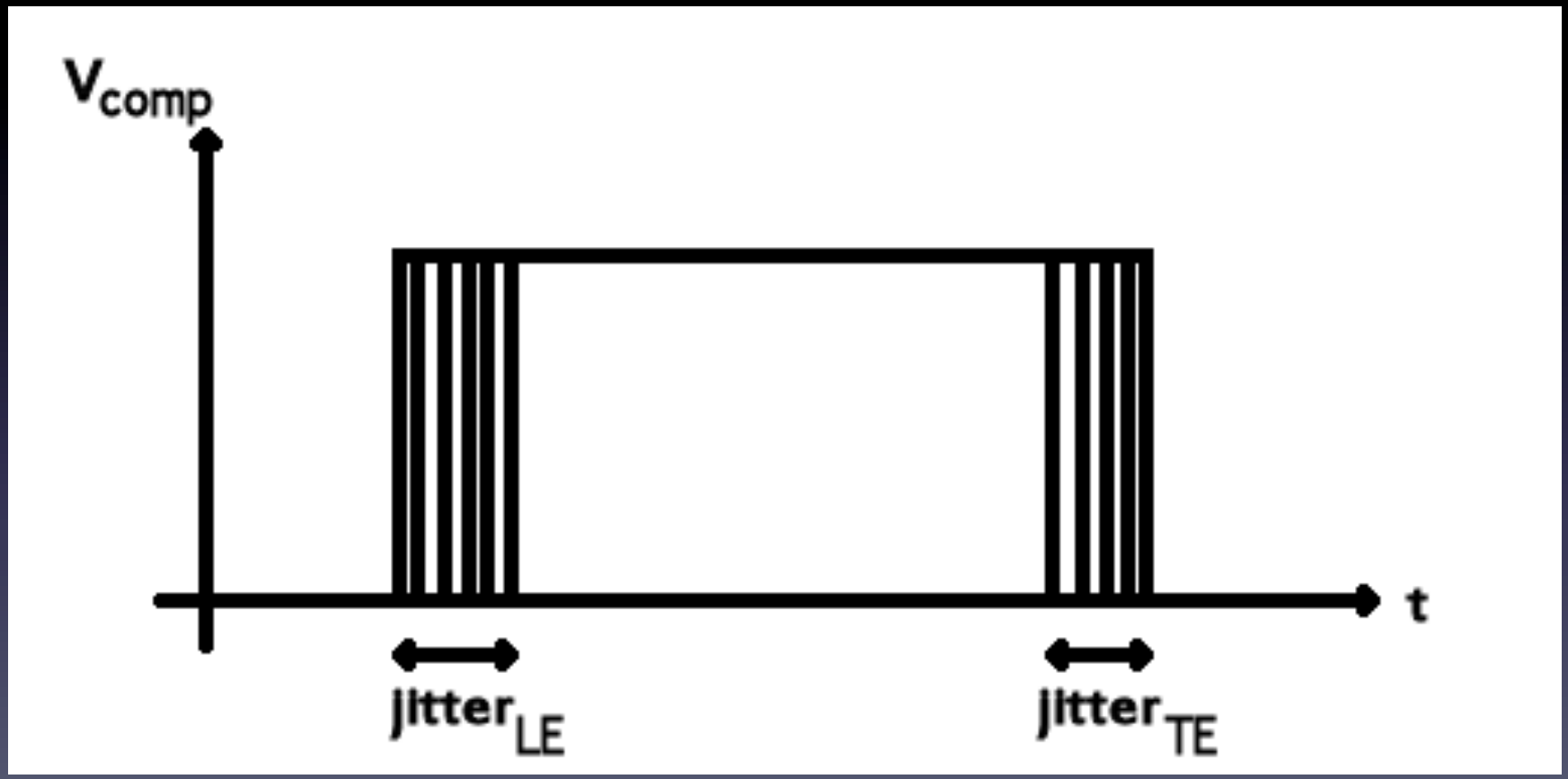




Simulations: Gaussian noise (2)

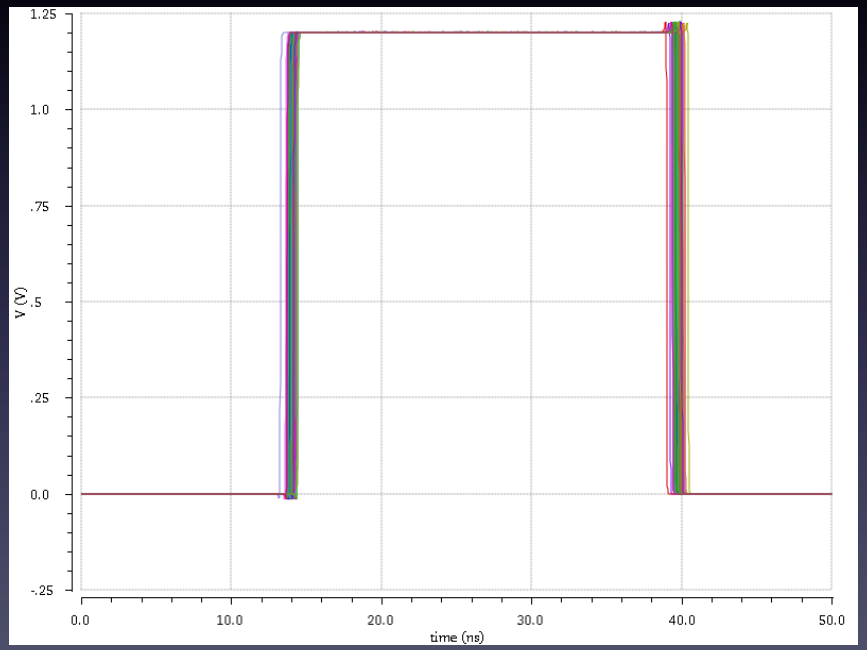


Simulations: Jitter (1)



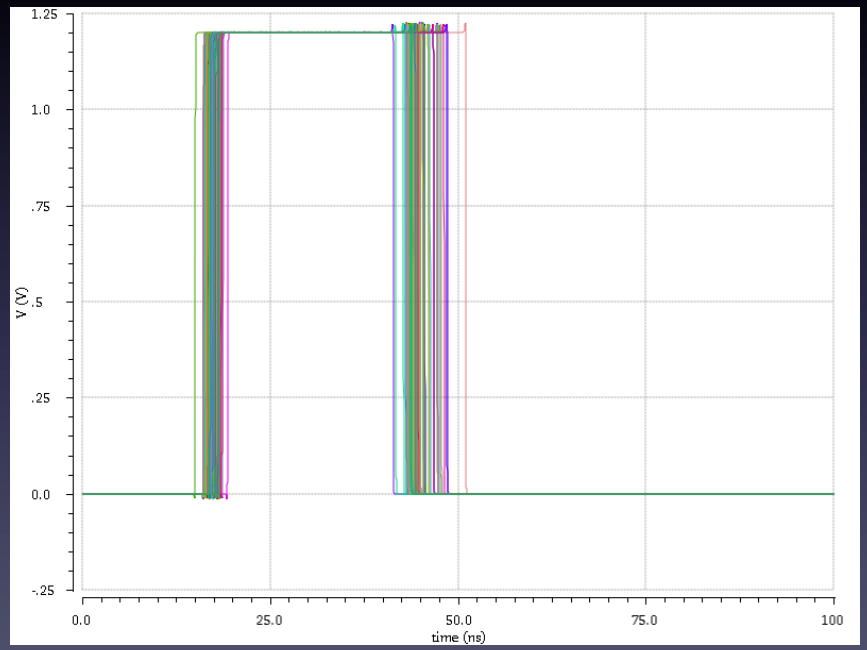
Simulations: Jitter (2)

C_{det} = 5 pF



σ_t ~ 300 ps

C_{det} = 30 pF



σ_t ~ 1.5 ns