Torino Graduate School in Physics and Astrophysics
XXIV cycle

Integrated Front-End Electronics for High Precision Timing Measurements with Radiation Detectors

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Outline

- The NA62 experiment
- Precise extraction of timing information from nuclear radiation pulses
- Front-End architectures for the NA62 Gigatracker (GTK)
- Results from the prototypes of the developed architectures
- A new P-TDC front-end ASIC with improved pulse shape rejection
- Conclusions

Section 1
The NA62 experiment

Physics motivations

$$K^+ \to \pi^+ \nu \bar{\nu}$$

- The NA62 experiment at CERN SPS accelerator will collect 80 events with a S/B of 1:10 and a branching ratio of 10^{-10} in two years of data taking to measure the $|V_{td}|$ element in Cabibbo-Kobayashi-Maskawa (CKM) matrix:

$$BR(k^+ \to \pi^+ \nu\bar{\nu}) = 6 r_{k^+} BR(k^+ \to \pi^0 e^+ \nu) \frac{G_l}{G_F^2 |V_{us}|^2}$$

$$G_l = \frac{\alpha G_F}{2\pi \sin^2 \theta_W} [V_{ts}^* V_{td} X(x_t) + V_{cs}^* V_{cd} X_{NL}^l]$$

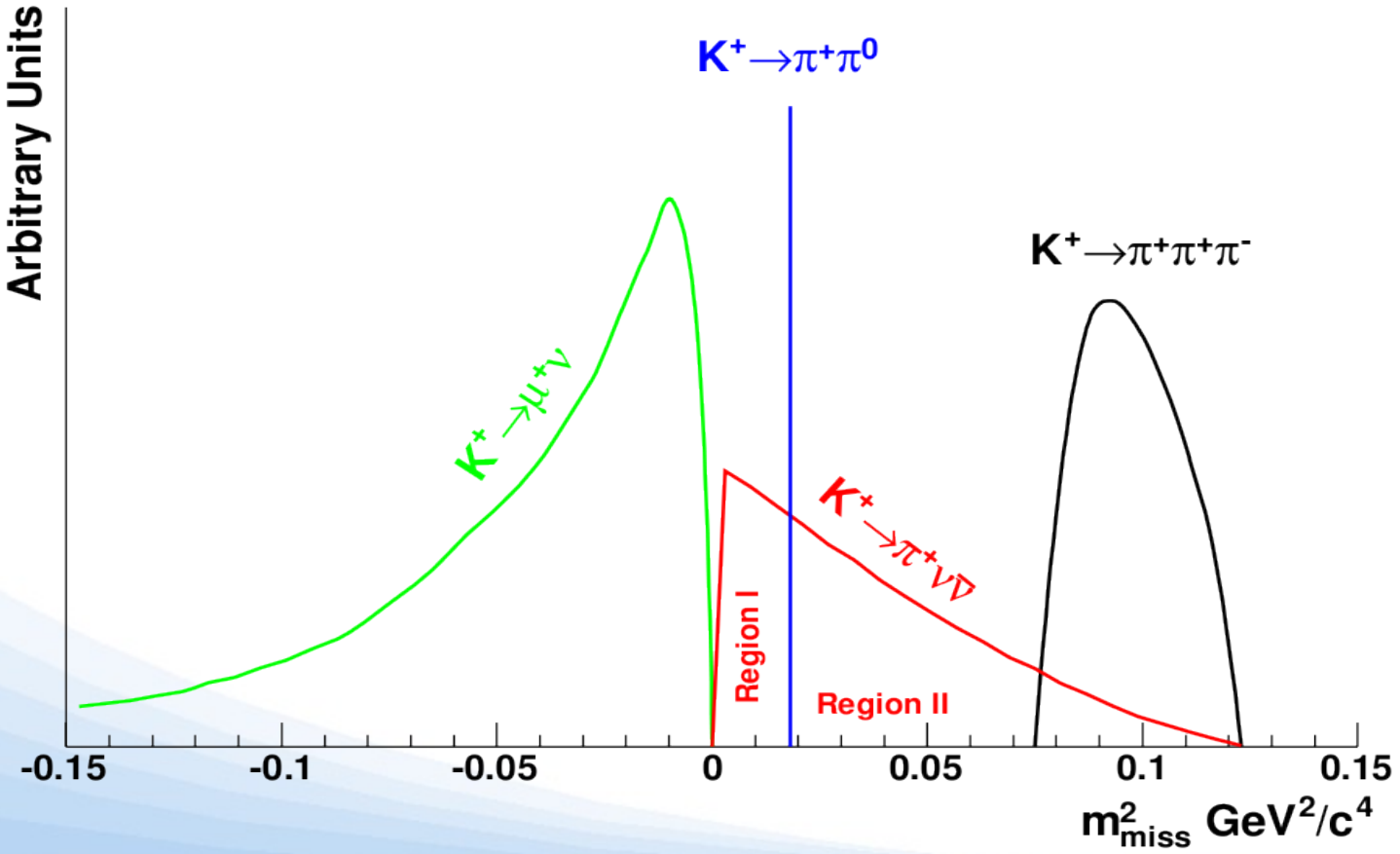
- It offers a unique opportunity to test the SM and to deepen the knowledge of the CKM matrix
- $8 \cdot 10^8$ particles/s at 75 GeV/c

Experimental approach

Decay mode	BR	Background rejection
$k^+ \to \mu^+ \nu$ ($k_{\mu 2}$)	63%	μ PID, kinematics
$k^+ \to \pi^+ \pi^0$	21%	γ veto, kinematics
$k^+ \to \pi^+ \pi^+ \pi^-$	6%	Charged particles veto, kinematics
$k^+ \to \pi^+ \pi^0 \pi^0$	2%	γ veto, kinematics
$k^+ \to \pi^0 \mu^+ \nu$ ($k_{\mu 3}$)	3%	γ veto, μ PID
$k^+ \to \pi^0 e^+ \nu$ (k_{e3})	5%	γ veto, E/p

Experimental approach

- Region I: $0 < m^2_{miss} < m^2_{\pi 0} - (\Delta m)^2$
- Region II: $m^2_{\pi 0} + (\Delta m)^2 < m^2_{miss} < MIN[m^2_{miss}(\pi^+\pi^+\pi^-)]$



Experimental approach

$$m^2_{miss} = m^2_k \frac{1-|P_\pi|}{|P_k|} + m^2_\pi \frac{1-|P_k|}{|P_\pi|} - |P_k||P_\pi|\theta^2_{\pi k}$$

$$\frac{\Delta|P_k|}{|P_k|} \sim 0.3\%, |P_k| = 75 GeV/c$$

$$\frac{\Delta|P_\pi|}{|P_\pi|} \sim 1\% \text{ at } 30 \text{ GeV/c}$$

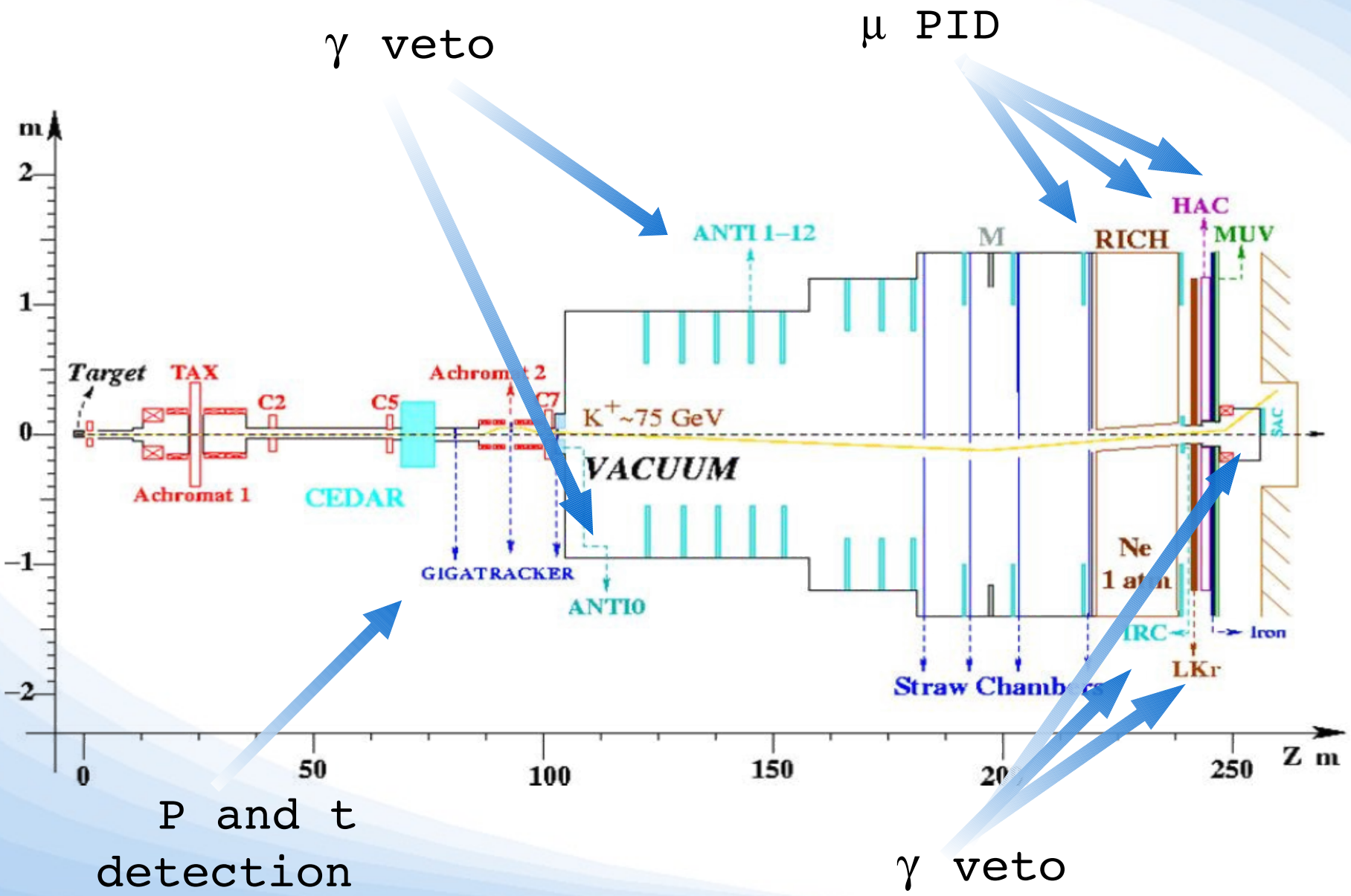
$$\Delta\theta_{\pi k} \sim 50 - 60 \ \mu rad$$

$$\Delta(m^2_{miss}) \sim 8 \cdot 10^{-3} GeV^2/c^4$$

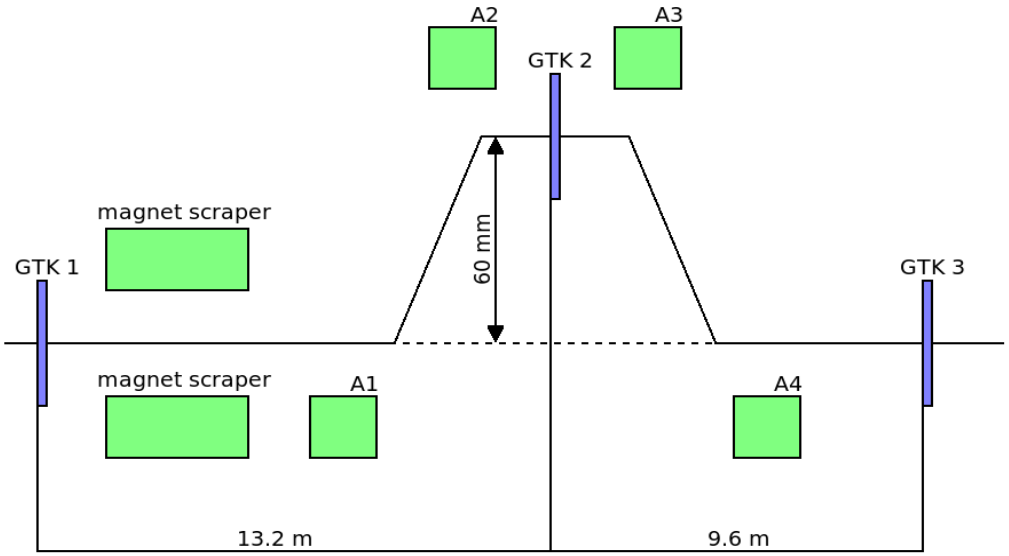
GTK:

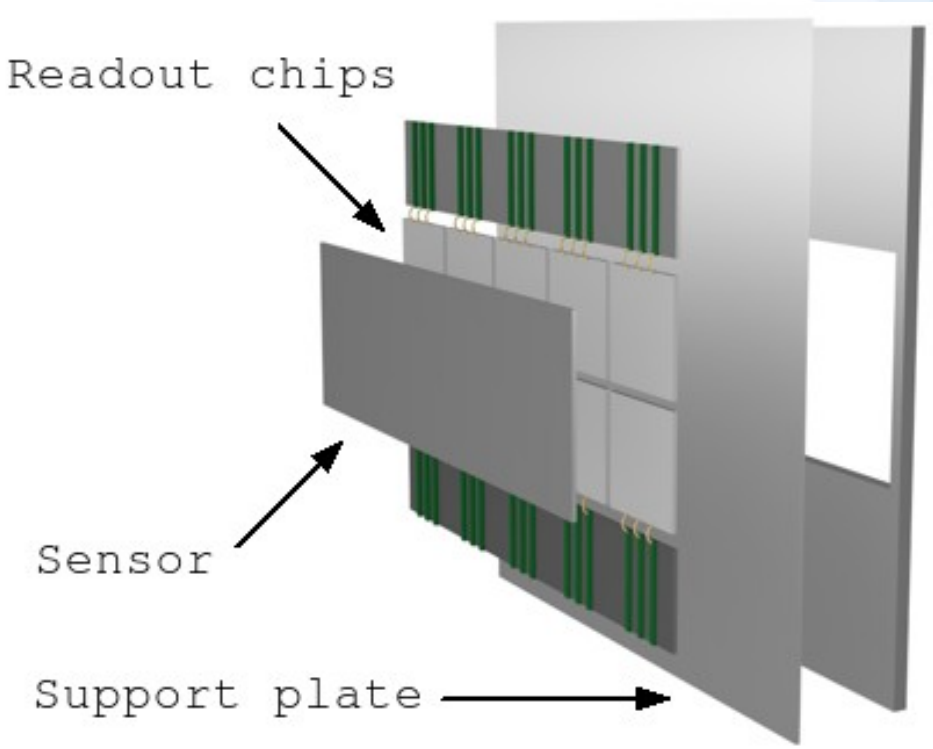
- 300μm x 300μm pixel
- ~100 ps time resolution due to high particle rate ($60 MHz/cm^2$)

Experimental setup



GTK detector





- 3 GTK stations
- One silicon sensor of 60mm x 27mm x 200µm
- 2 x 5 readout chips bump bonded to the sensor

Readout chip specifications

- Time resolution of 200 ps RMS on the single station
  (3 stations → 200/√3=115 ps)
- Efficiency > 99%: 1 fC threshold
- Dynamic range: 1 fC – 10 fC
- Dead time < 1%: maximum event rate of 135 kHz/channel
- Power consumption < 2 mW/channel
- Radiation tolerance: SEU and integral dose deterioration of the sensor
- Pixel size: 300μm x 300μm
- Material budget per station: 0.5% X_0

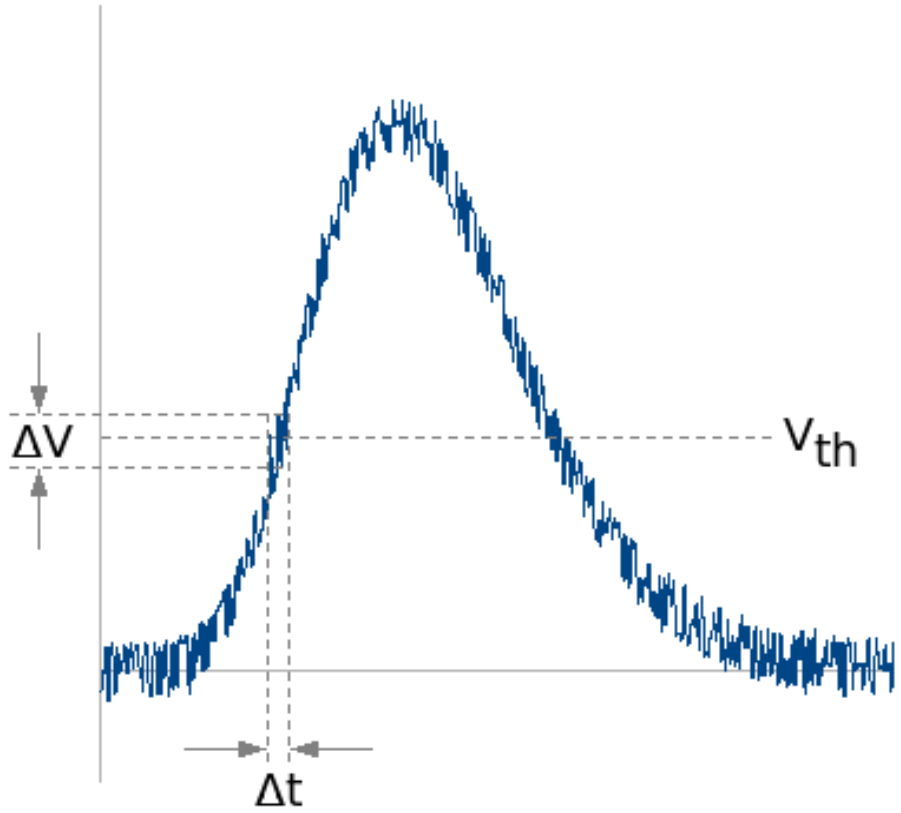
Section 2

Precise extraction of timing information from nuclear radiation pulses

Timing errors

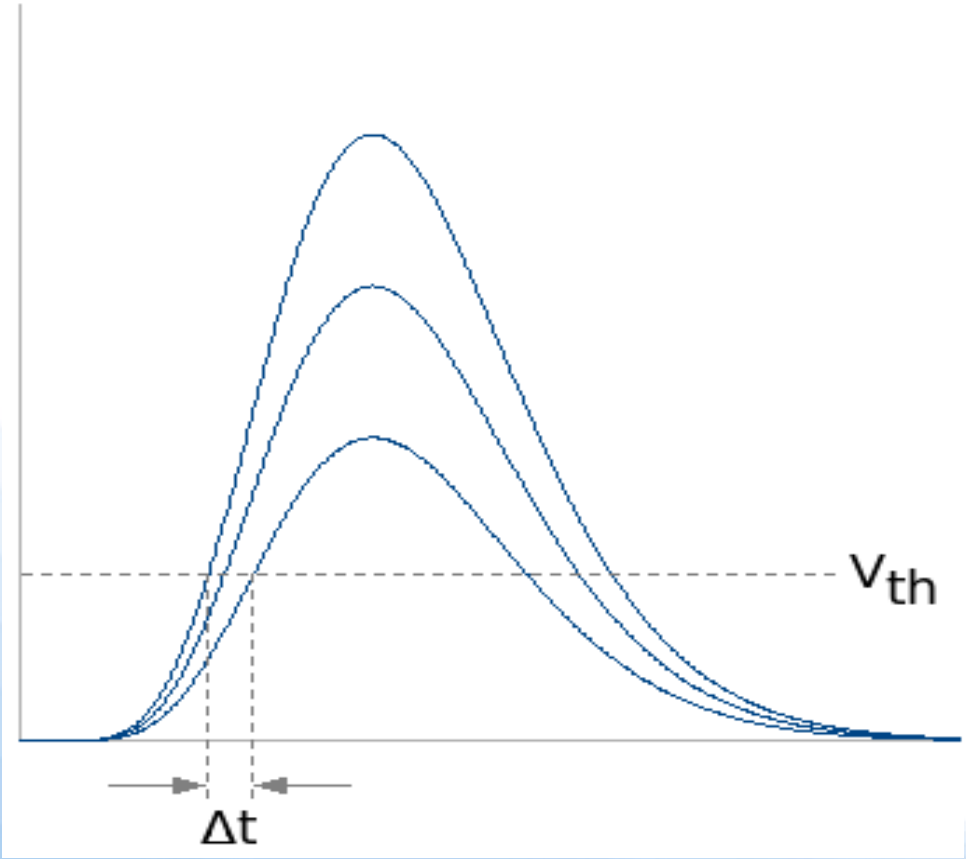
$$\sigma_t = \frac{\sigma_n}{\frac{dV}{dt}\Big|_t}$$

- **Jitter:** timing uncertainty induced both by the electronic noise and by statistical fluctuations of the signal from the detector



Timing errors

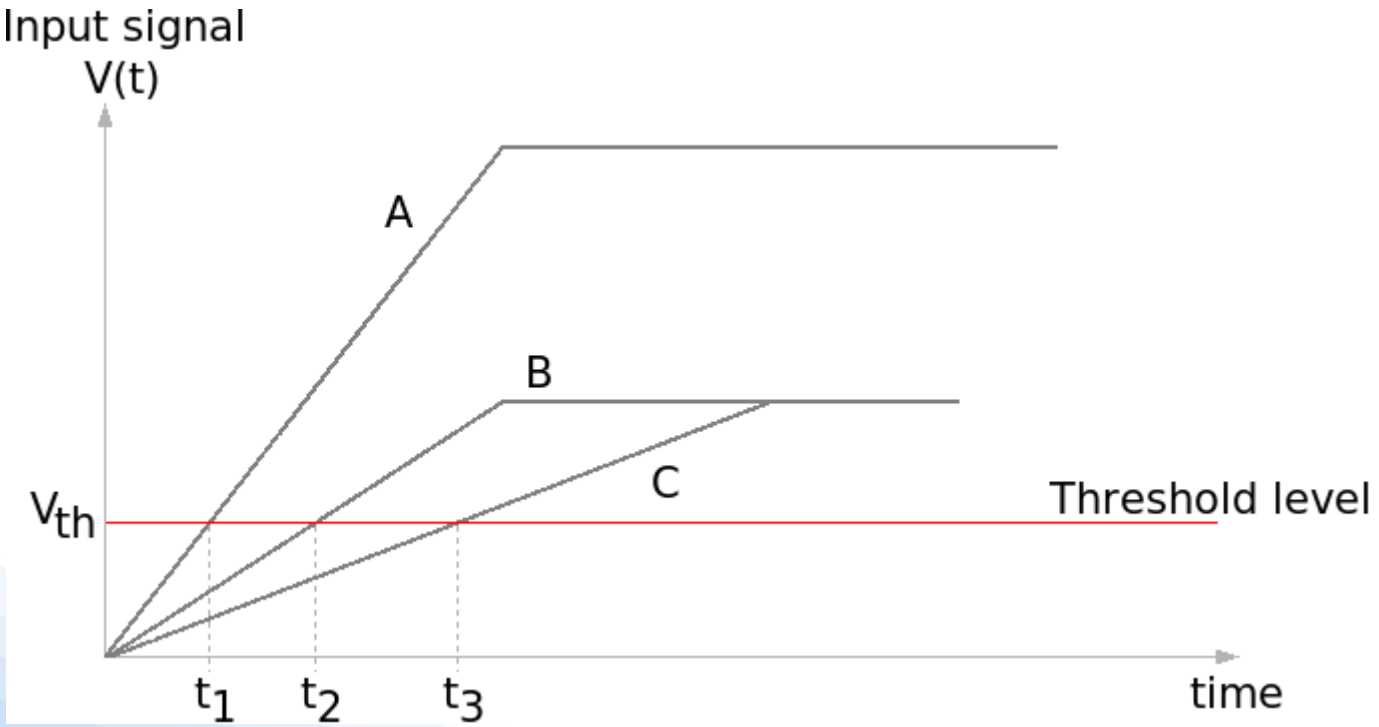
- **Drift:** long term timing error due to component aging, temperature variation or total dose effects in the detecting system



- **Time walk:** signals with constant rising time and different amplitudes will cross the threshold at different times

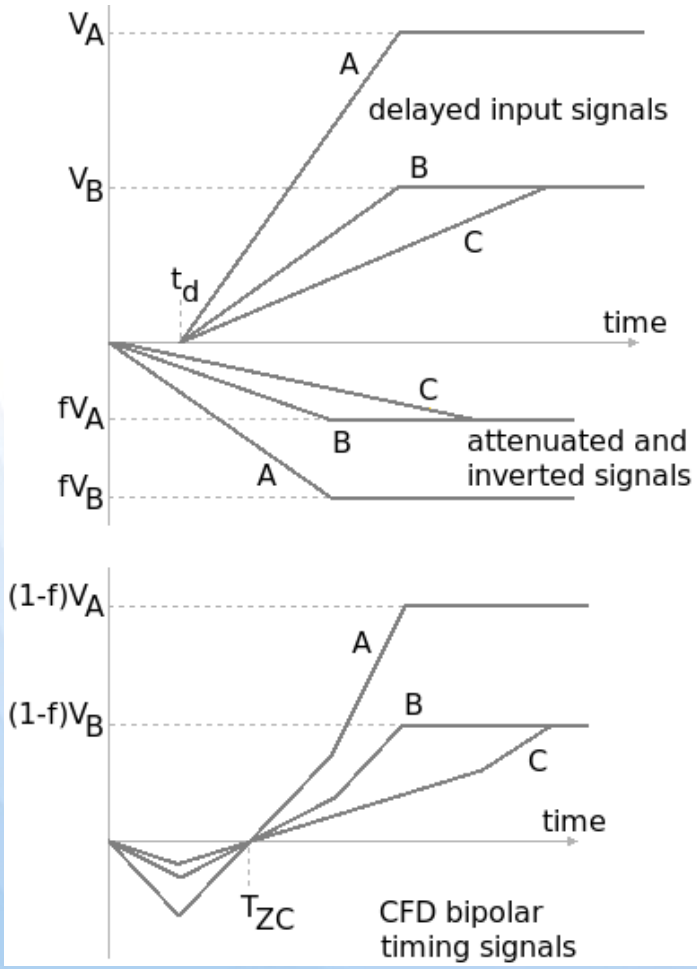
Timing techniques

- **Leading edge:** the measured time depends both on the amplitude and on the rise time of the signal



Timing techniques

- **Constant Fraction:** for linear signals the zero crossing is independent from the amplitude and from the rise time of the input signal. For a CR-RC signal the independence from the rise time is preserved for $t_d \ll \tau$ and/or for $f \ll 1$



Linear signals

$$V(t) = \frac{At}{t_r}$$

$$V(t_{zc} - t_d) = fV(t_{zc})$$

$$t_{zc} = \frac{t_d}{1 - f}$$

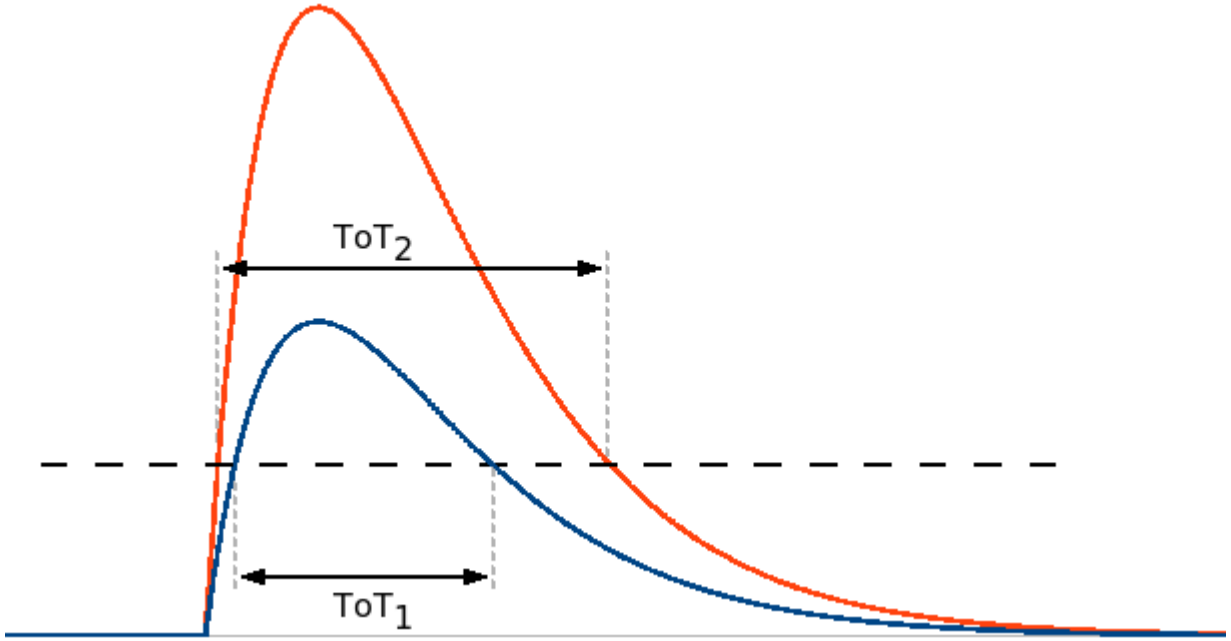
CR-RC shaper

$$V(t) = Ate^{-\frac{t}{\tau}}$$

$$t_{zc} = \frac{t_d}{1 - fe^{-\frac{t_d}{\tau}}}$$

Timing techniques

- **Amplitude correction:** e. g. Time over Threshold (ToT) technique



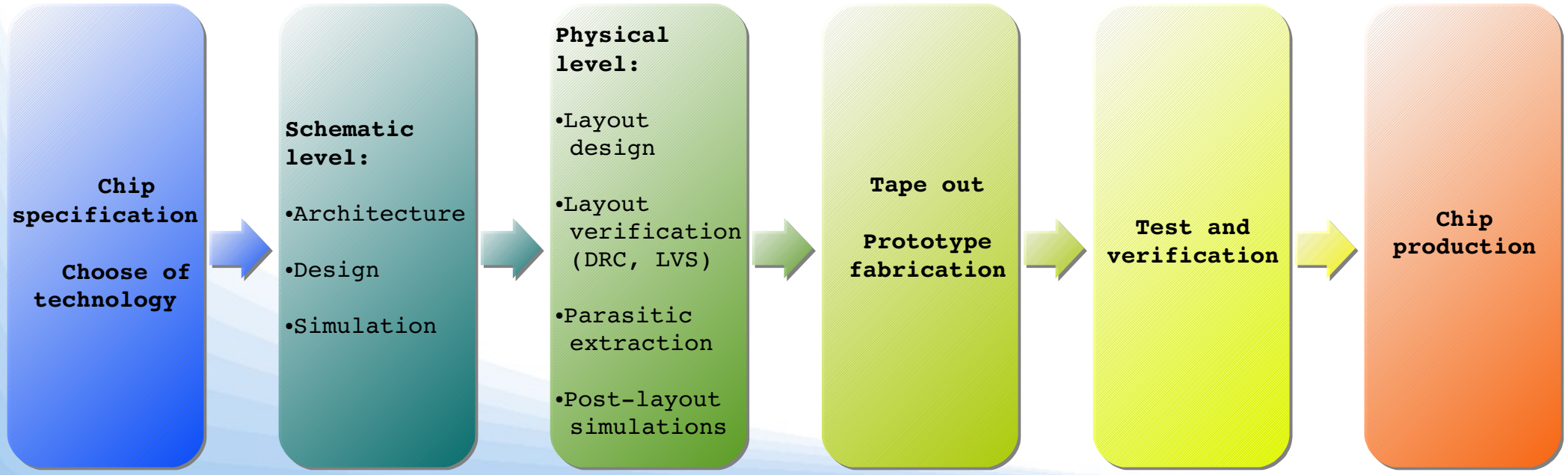
the time walk correction is based on an algorithm derived from the correlation between the pulse width and the experienced time walk

Section 3
Front-End architectures for the NA62 GTK

Application Specific ICs

0.13 IBM CMOS technology: good radiation hardness

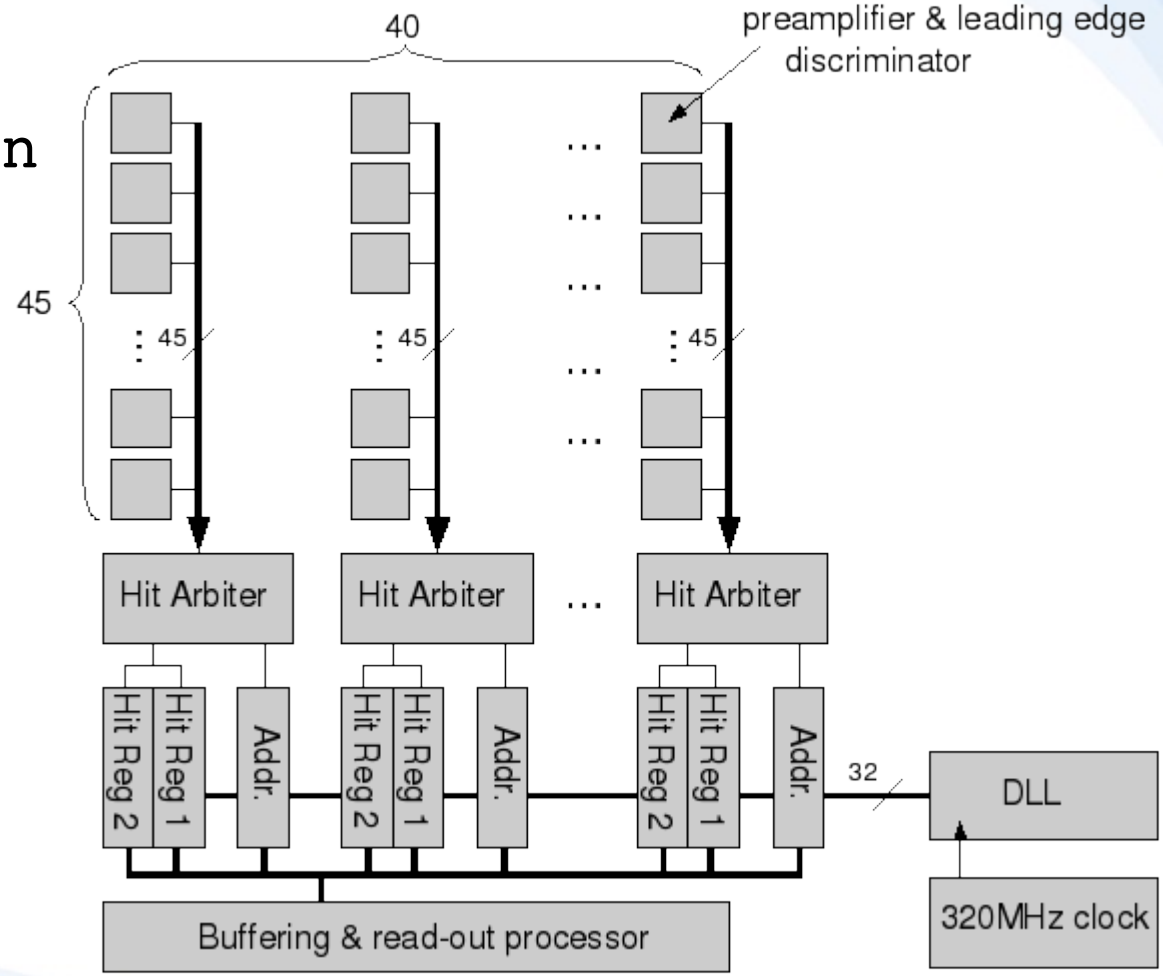
- Full size chip: 400 000 $
- Multi Project Wafer for prototyping: 2000-3000 $/mm^2



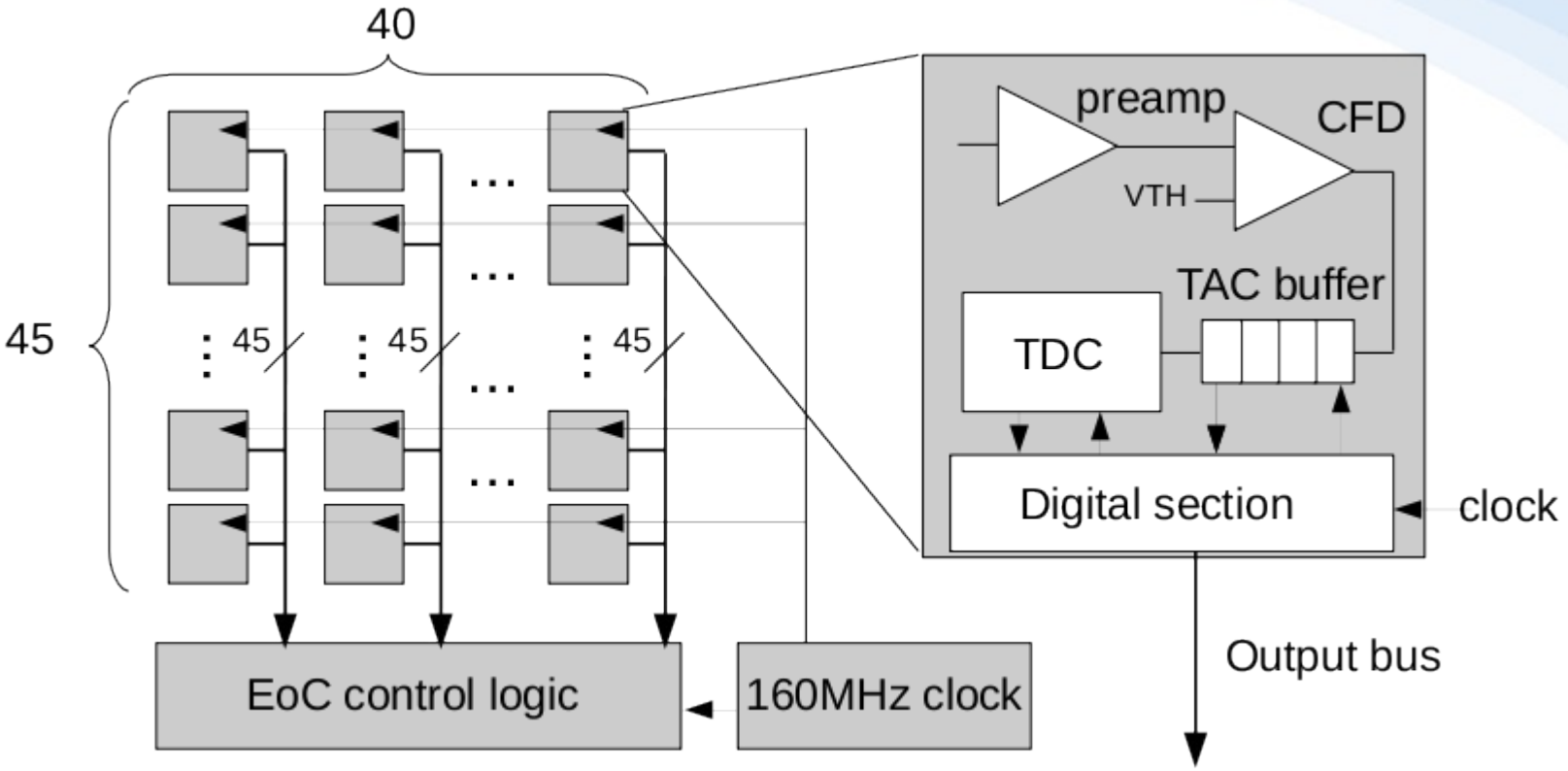
EoC architecture

End of Column approach

- Complete separation between the analog and digital sections
- 13.5 mm long transmission lines
- ToT: offline correction of time walk
- 9x2 DLL based TDCs



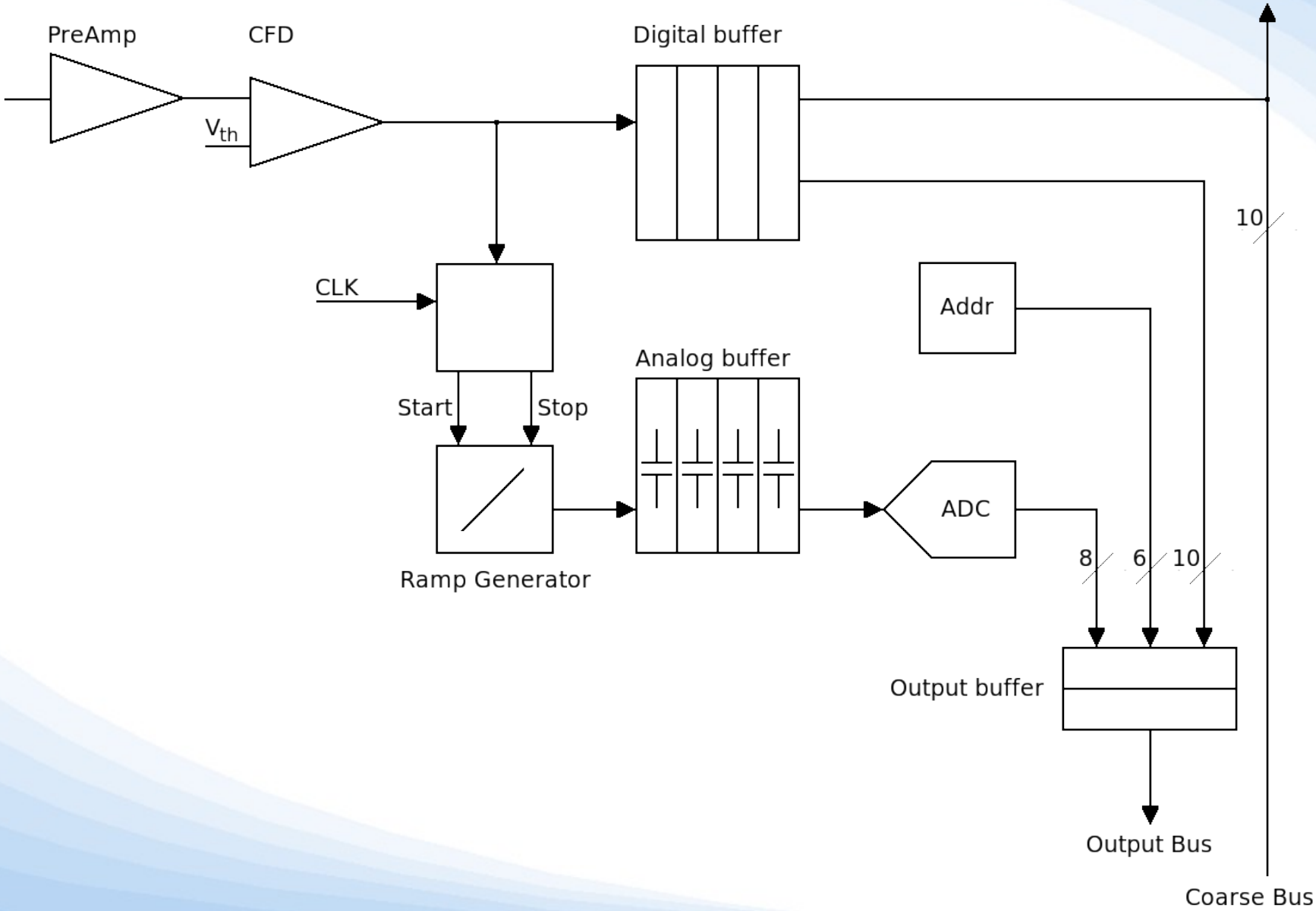
P-TDC architecture



Local approach

- CFD: online correction of time walk
- 1800 fast/slow ramp TDCs

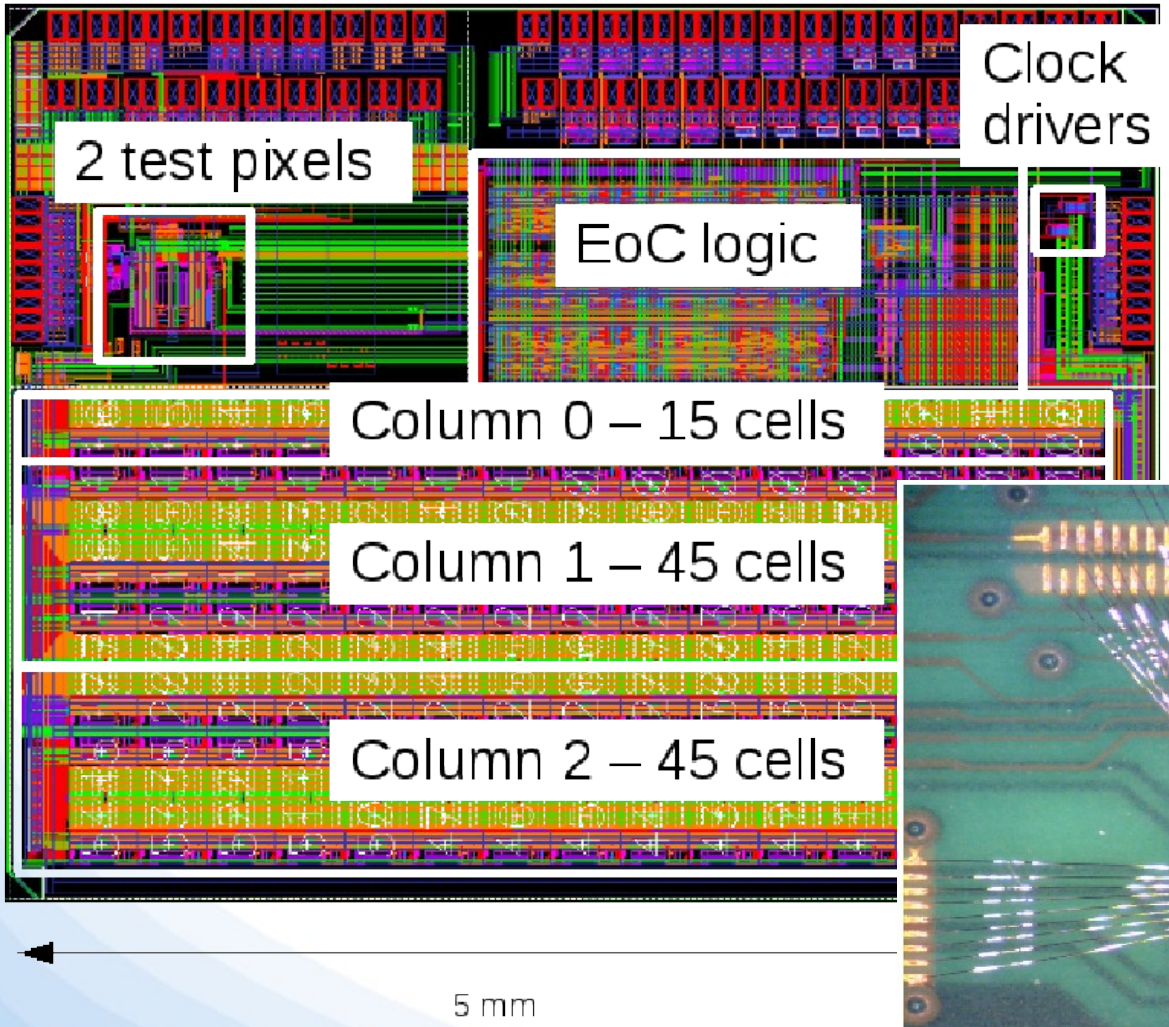
P-TDC pixel

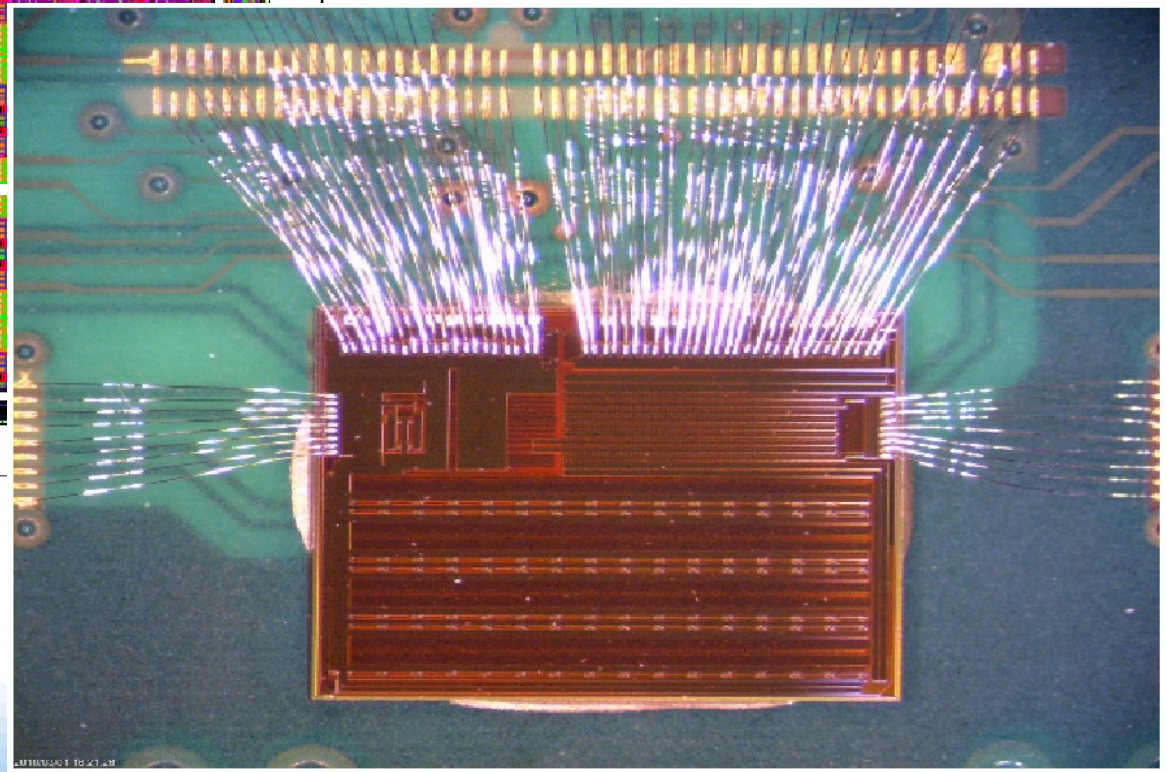

PreAmp
CFD
Digital buffer
V_{th}
10
CLK
Addr
Analog buffer
Start
Stop
ADC
8
6
10
Ramp Generator
Output buffer
Output Bus
Coarse Bus

Section 4

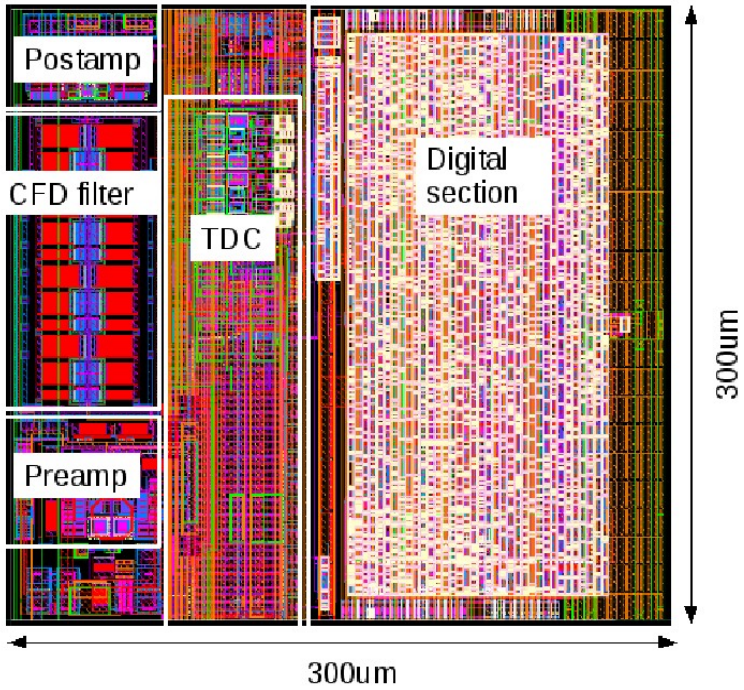
Results from the prototype of the developed architectures

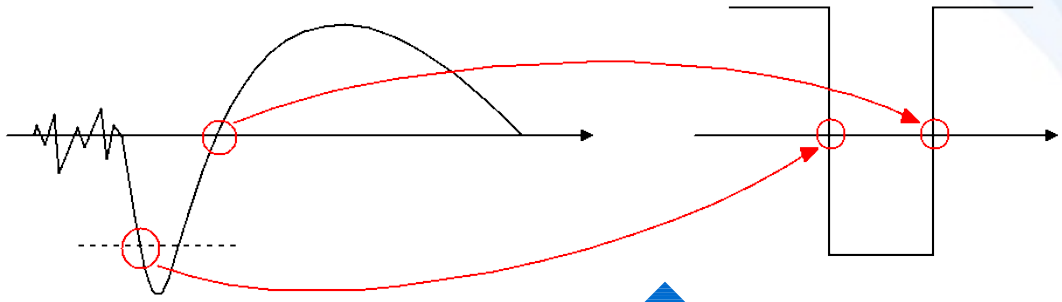
The P-TDC demonstrator chip

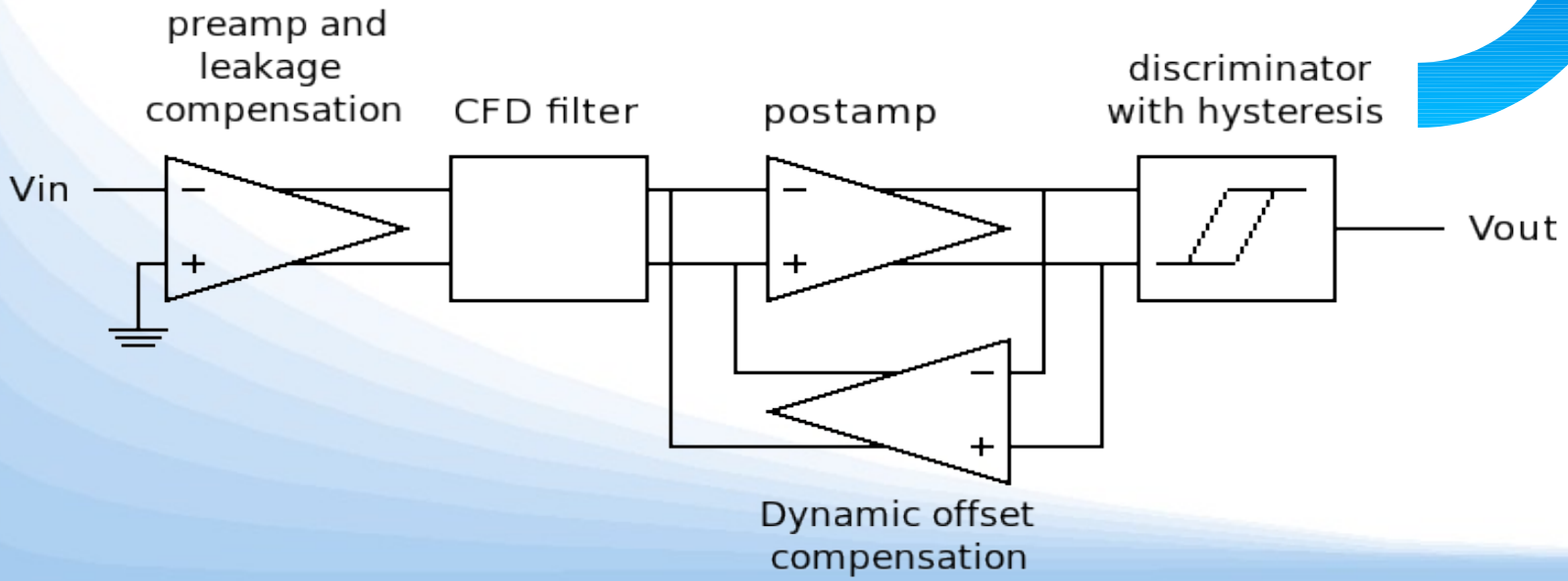




The P-TDC pixel layout

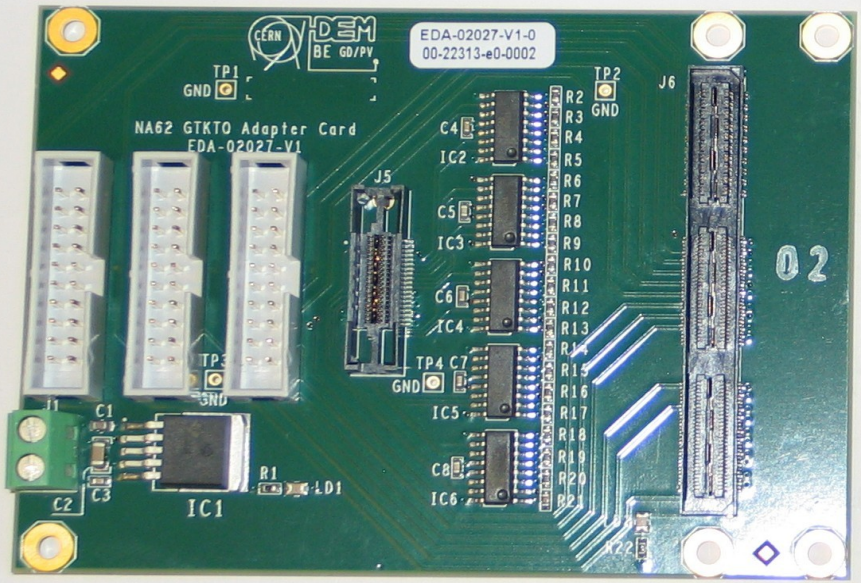




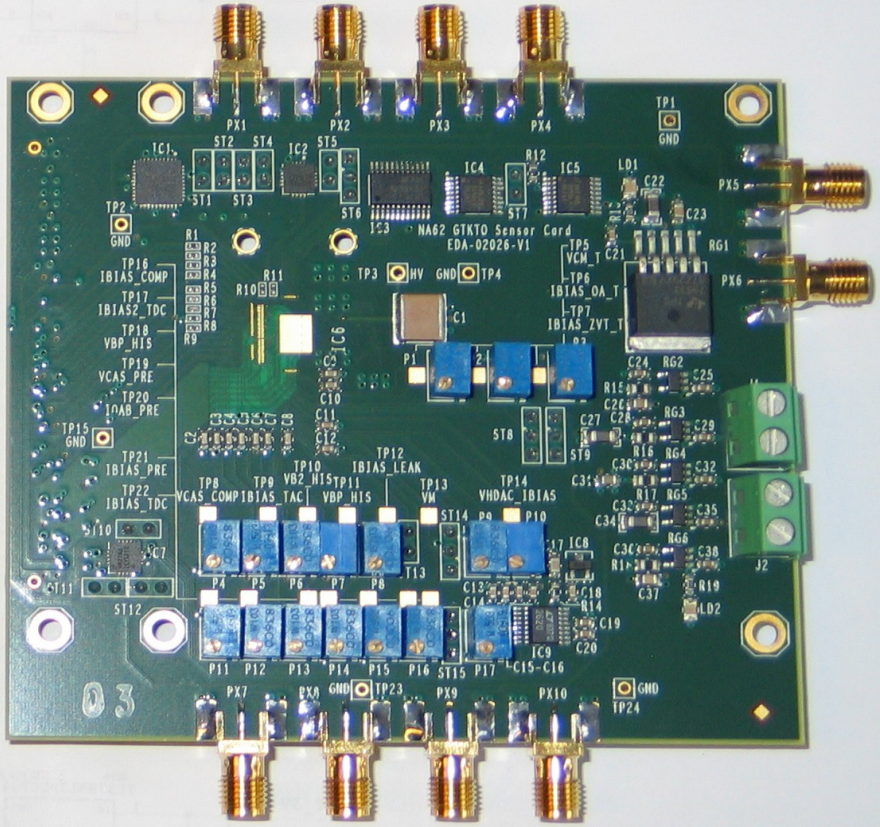


The testing system

Adapter card

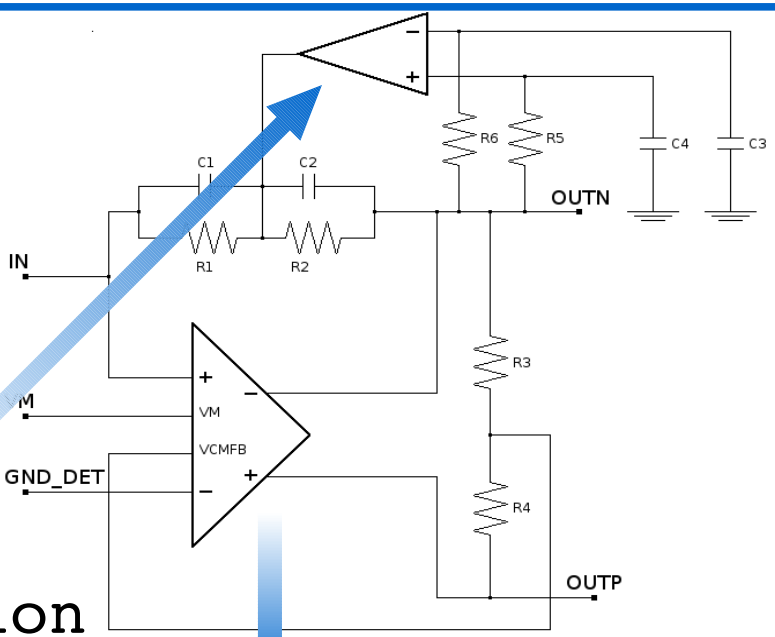


Sensor card



- Sensor card for the test with the FPGA
- Adapter card for the test with the DPG and LSA
- Labview routines implemented by Richard Wheadon

The preamplifier: schematics



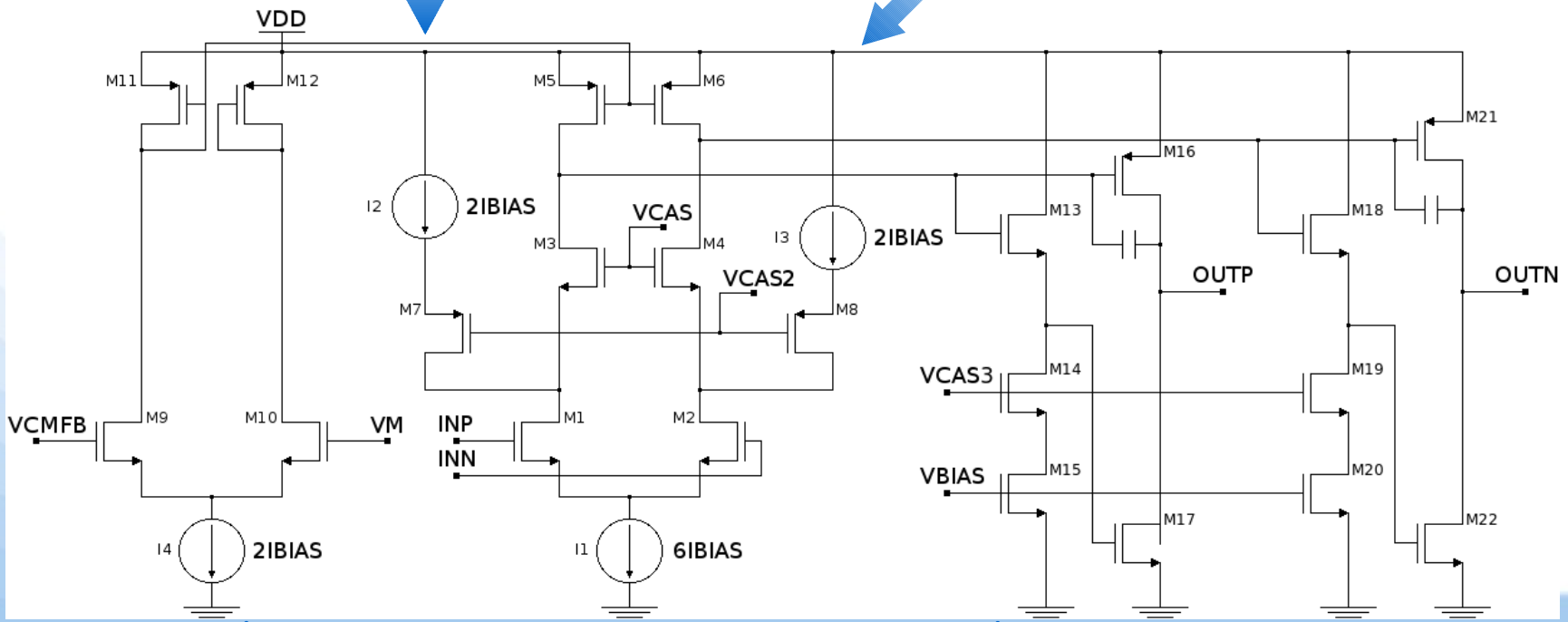
Gain: 80 mV/fC

Peaking time: 3.5 ns

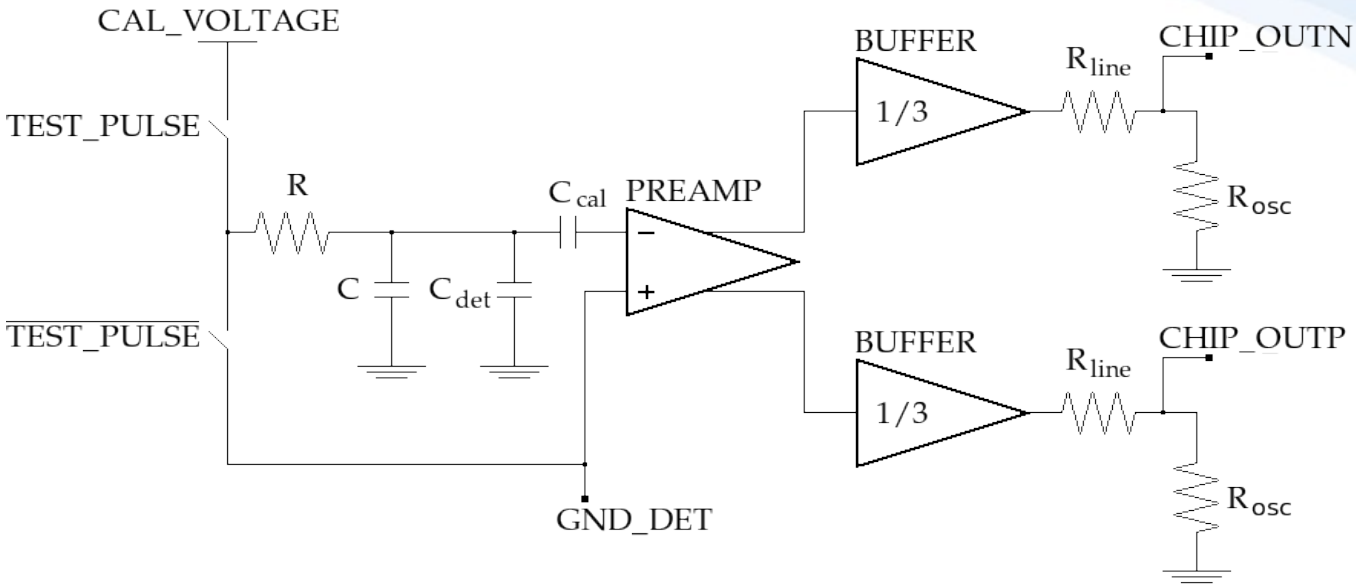
Linear up to 10 fC

Leakage compensation

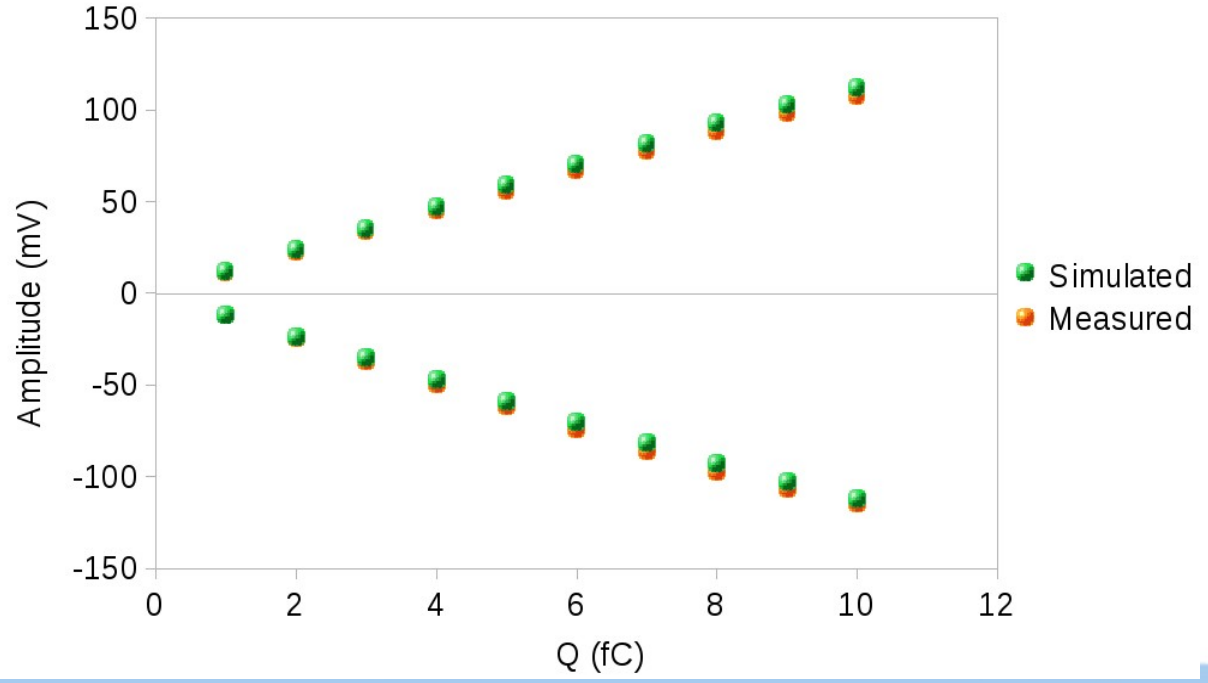
Two stages op-amp with class AB output



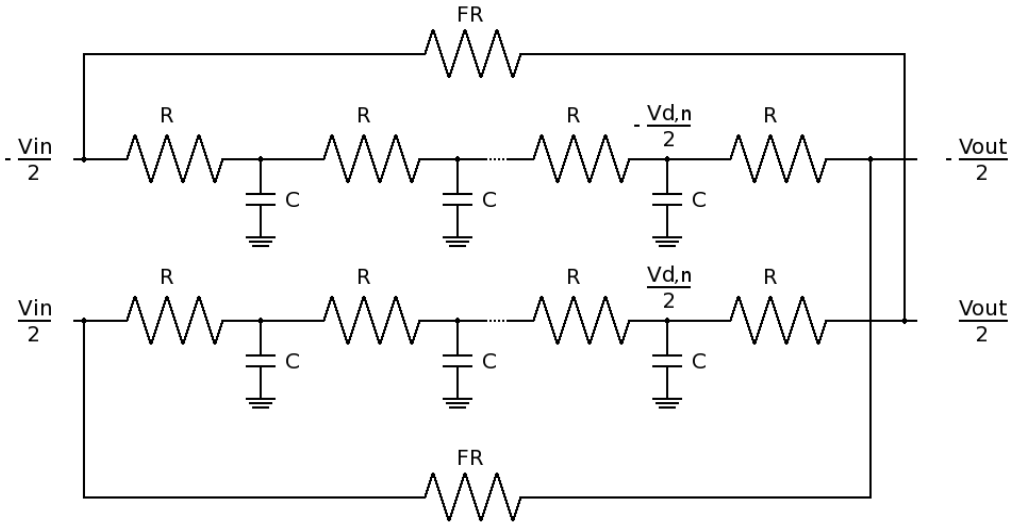
The preamplifier: results



3.2 ns
rise time
(20%-80%)



The CFD: schematics



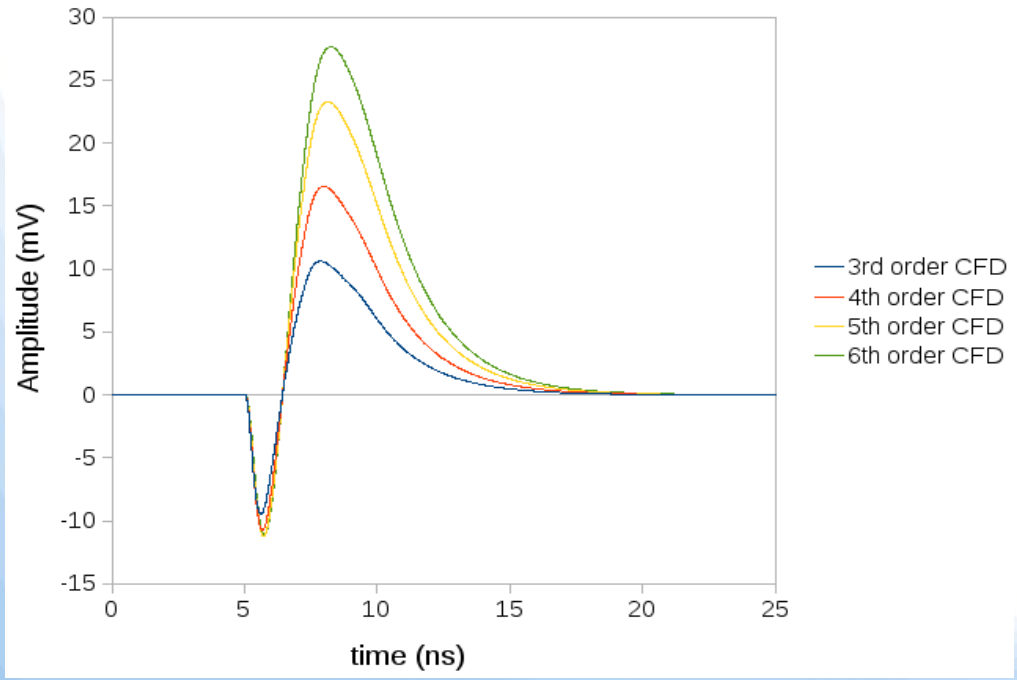
4^{th} order programmable RC delay line and cross coupling fraction

$$V_{out}(s) = V_{d,n}(s)\frac{F}{1+F} - V_{in}(s)\frac{1}{1+F}$$

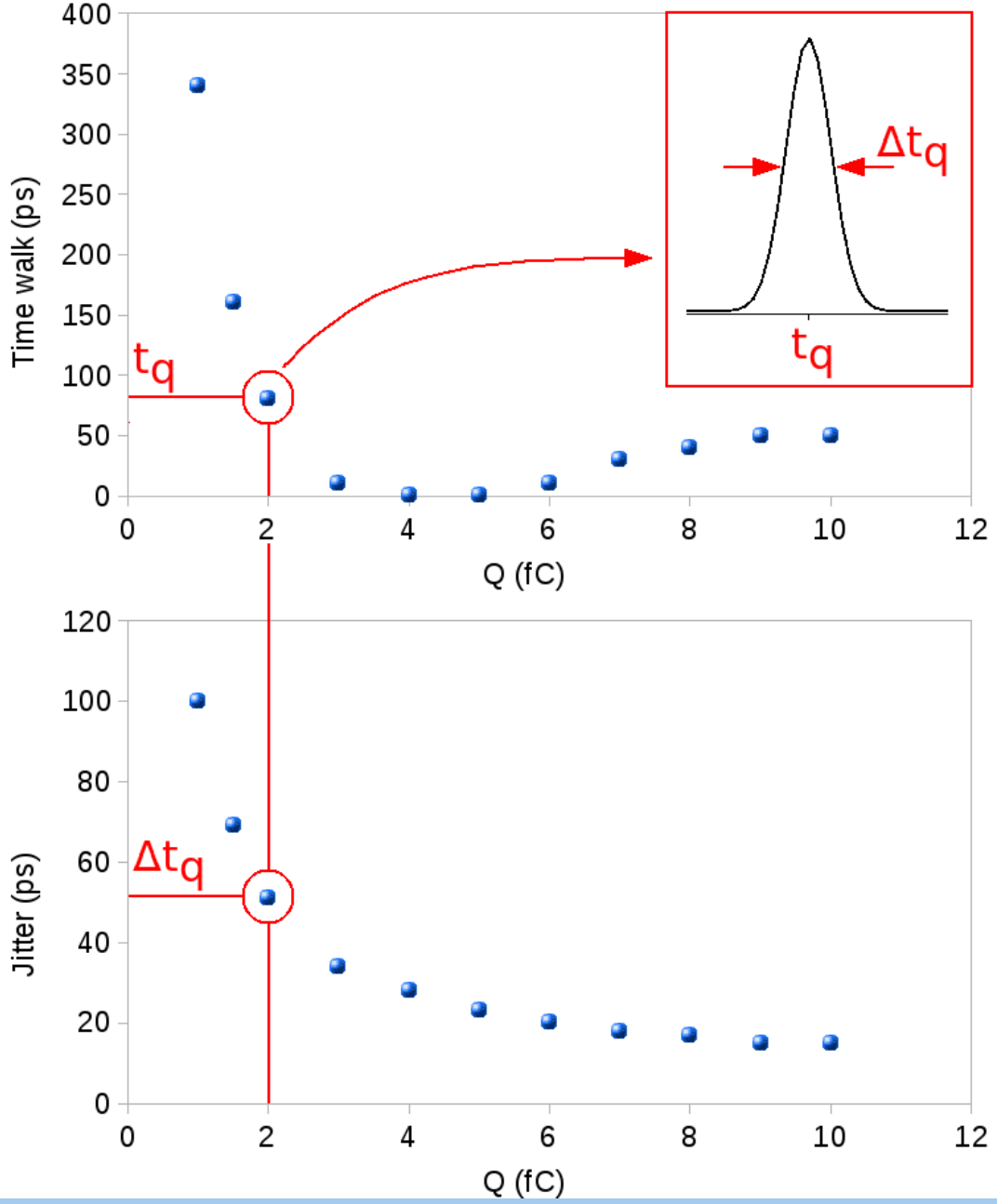
$$V_{d,1}(s) = V_{in}(s)\frac{F}{sRC+2+F(sRC+1)}$$

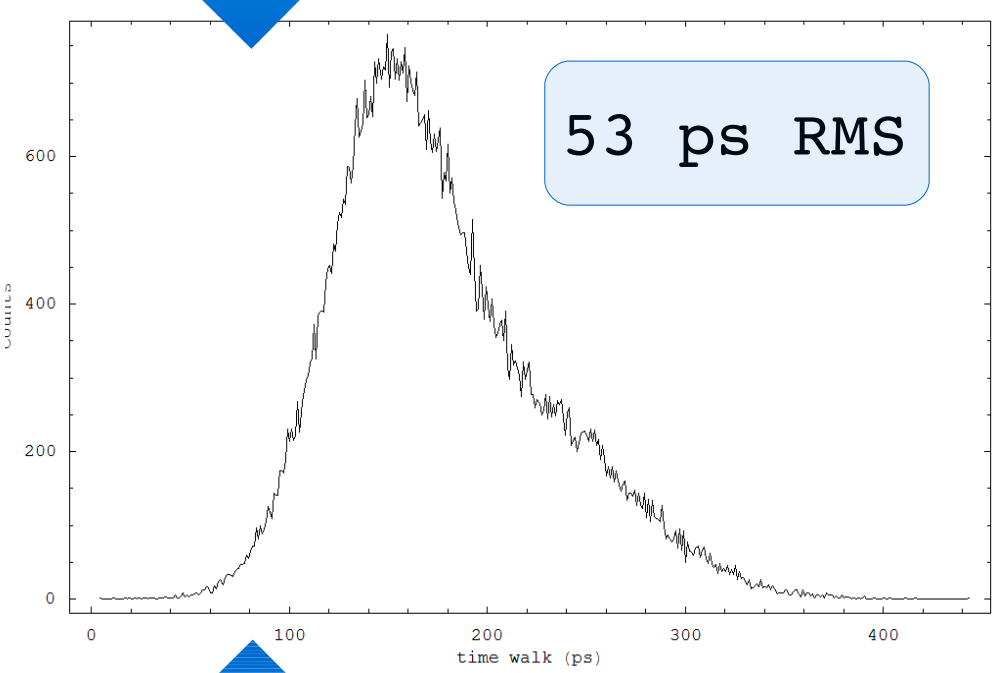
$$V_{d,n}(s) = V_{in}(s)\frac{A_n(s)}{B_n(s)+FC_n(s)}$$

$$A_n(s) = (F+1) - B_{n-1}(s)$$
$$B_n(s) = B_{n-1}(s)(sRC+1) + C_{n-1}(s)$$
$$C_n(s) = sRCB_{n-1}(s) + C_{n-1}(s)$$



The CFD: results





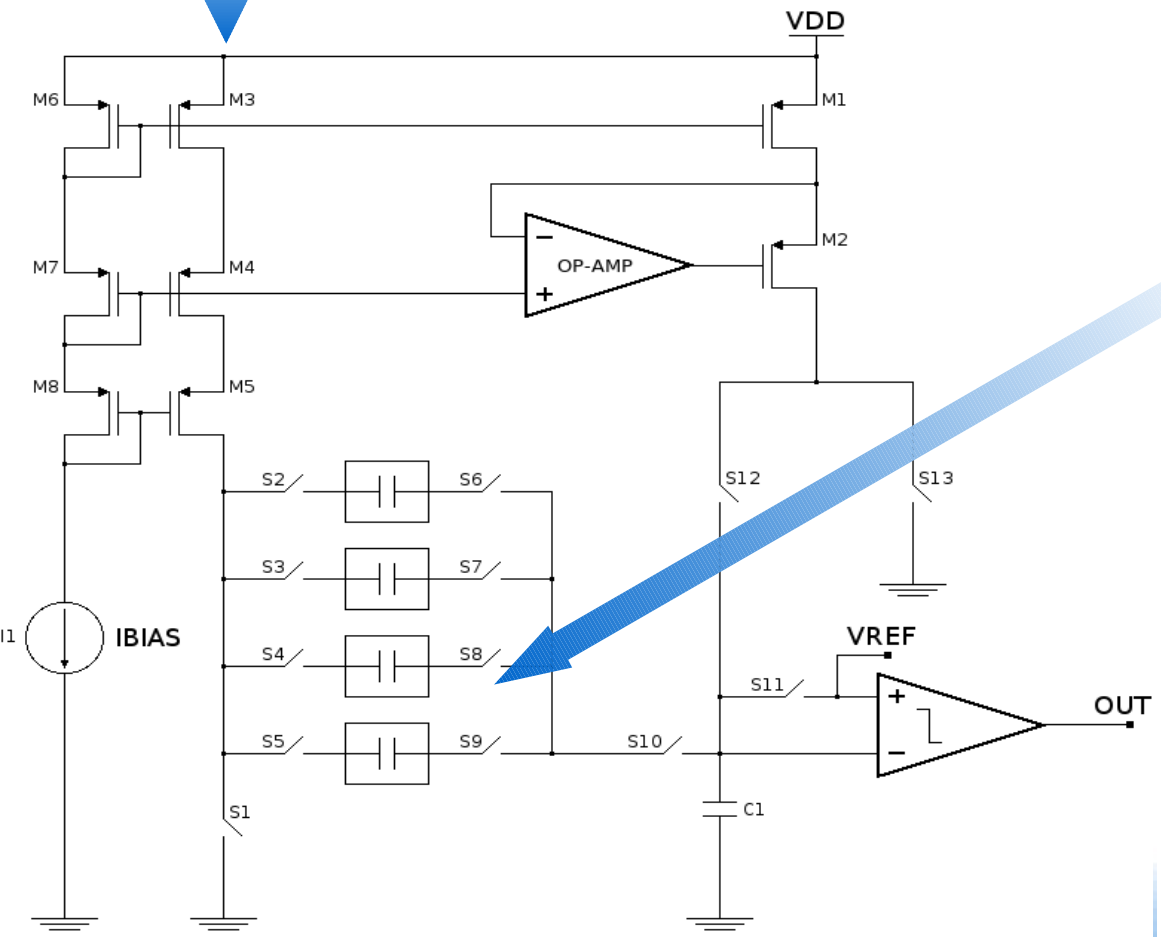
The TDC: schematics

The dual slope Wilkinson TDC:

- $4*6,25/2^8=98$ ps @ 160 MHz
- Minimum ramp: 1 Tck
- Maximum ramp: 3 Tck
- Dead time: 1.2µs

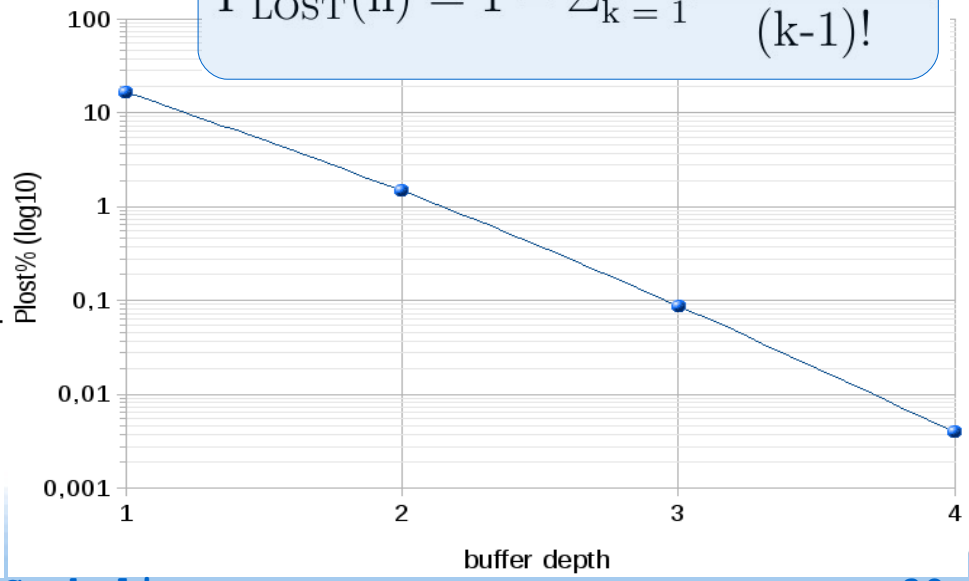
Fast ramp

Slow ramp

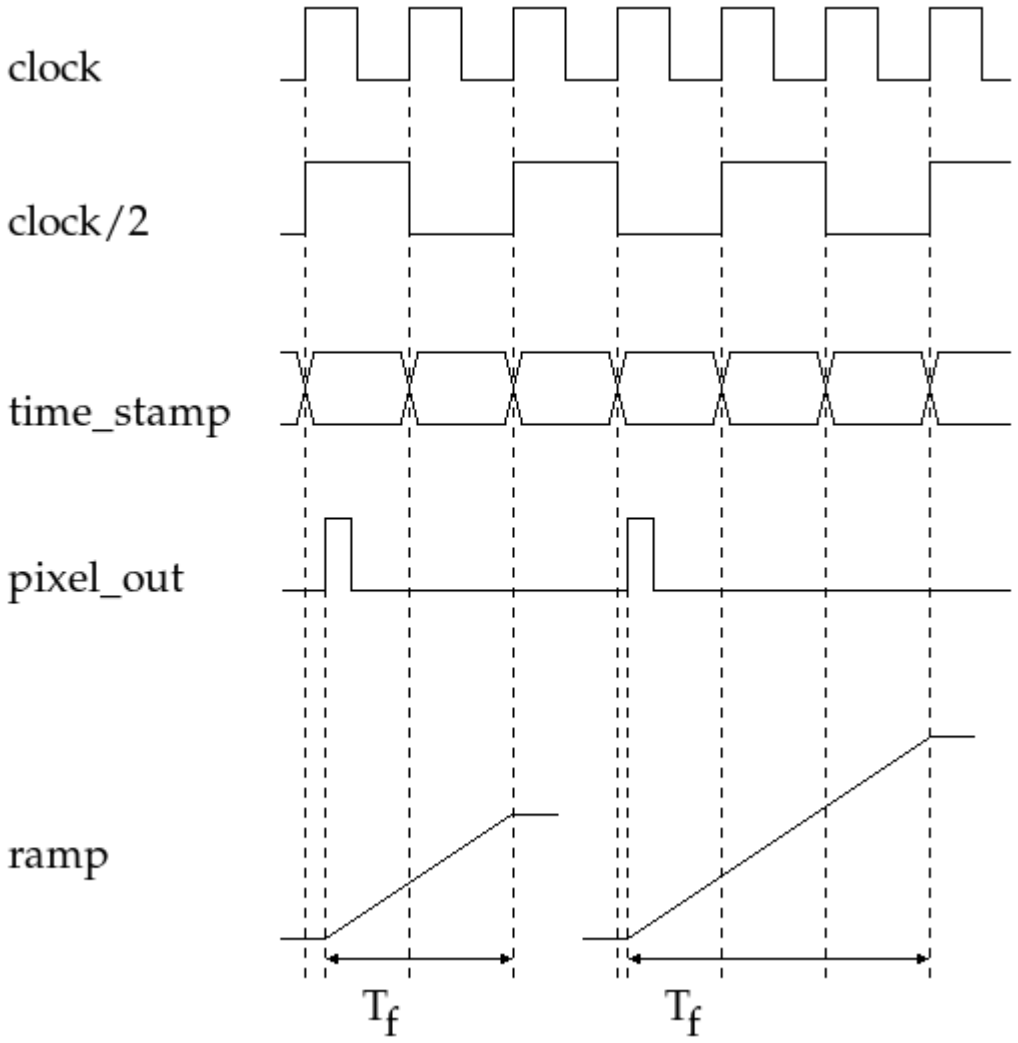


Four TAC buffers:

$$P_{LOST}(n) = 1 - \Sigma_{k=1}^{n} \frac{(\lambda\tau)^{k-1} e^{-\lambda\tau}}{(k-1)!}$$



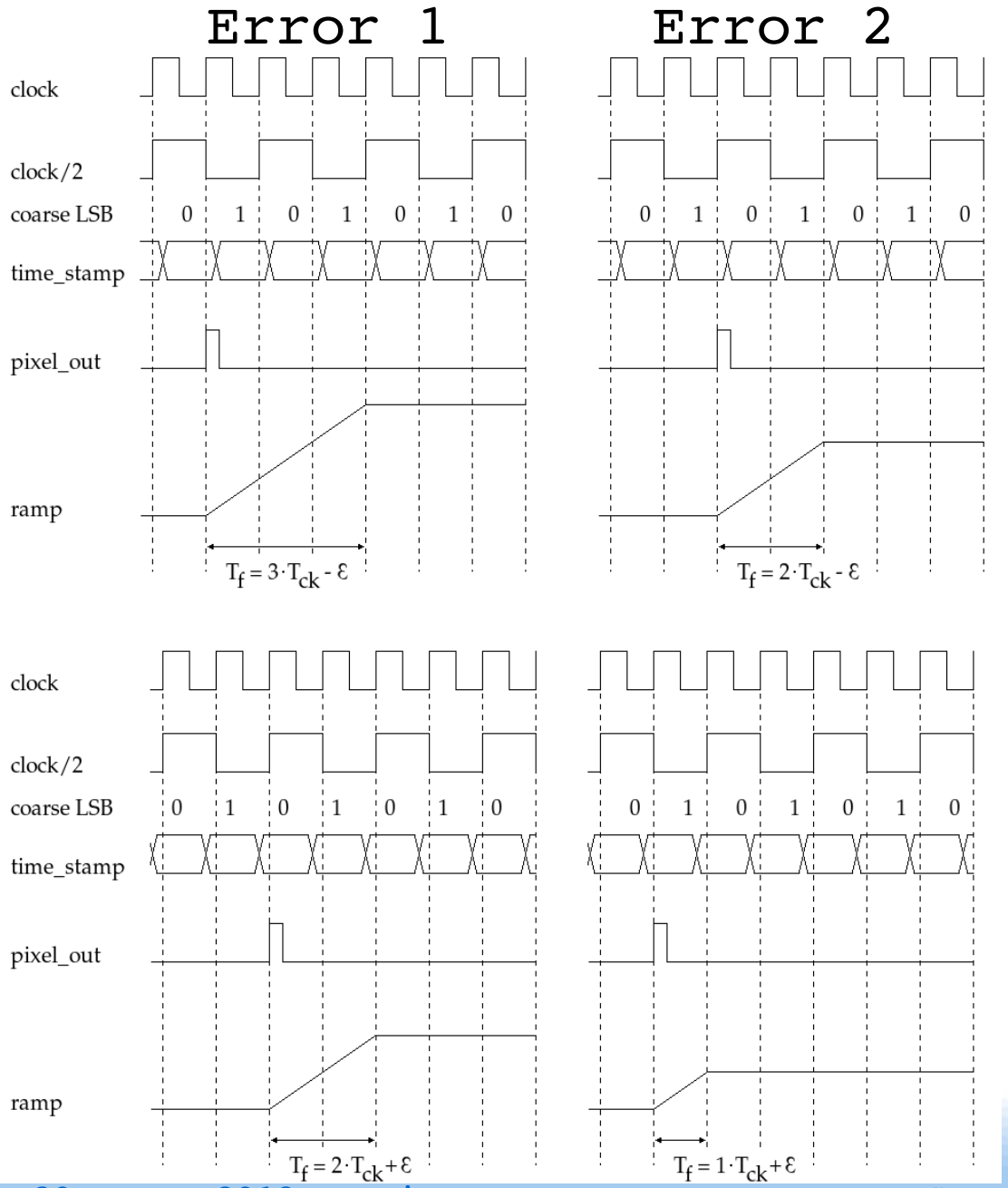
The TDC: time reconstruction



$$T = T_c + (2T_{ck} - T_f) \quad \text{if } T_f < 2T_{ck}$$

$$T = T_c + (3T_{ck} - T_f) \quad \text{if } T_f \geq 2T_{ck}$$

The TDC: time reconstruction



coarse LSB	fine MSB	total time
0	0	$T_c + 2T_{ck} - T_f$
1	1	$T_c + 3T_{ck} - T_f$
0	1	Error 1
1	0	Error 2

coarse LSB	fine MSB	T_f	total time
0	0		$T_c + 2T_{ck} - T_f$
1	1		$T_c + 3T_{ck} - T_f$
0	1	$3T_{ck} - \epsilon$	$T_c + 4T_{ck} - T_f$
0	1	$2T_{ck} + \epsilon$	$T_c + 2T_{ck} - T_f$
1	0	$2T_{ck} - \epsilon$	$T_c + 3T_{ck} - T_f$
1	0	$1T_{ck} + \epsilon$	$T_c + 1T_{ck} - T_f$

The TDC: results

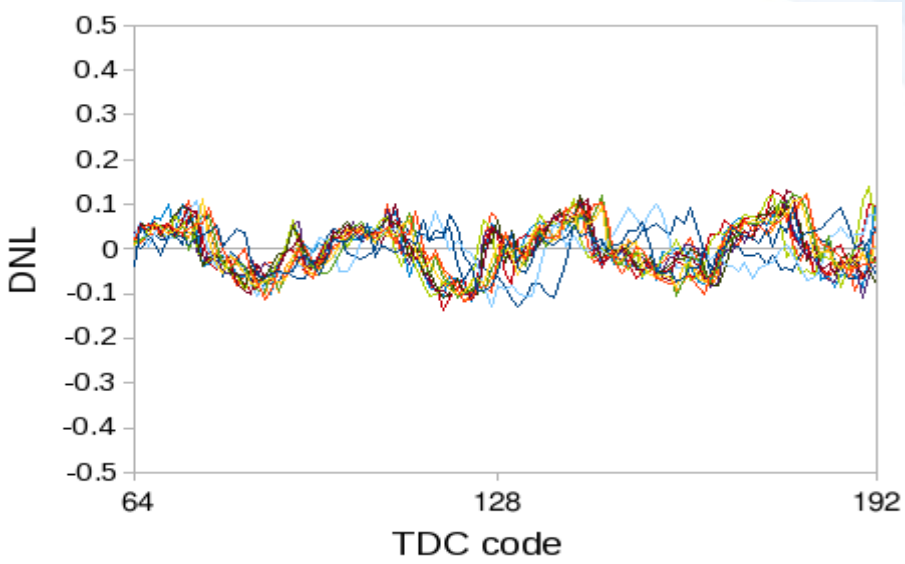
10^6 random TP to the 7-bit TDC: $N_{th} = \frac{10^6}{2^7}$

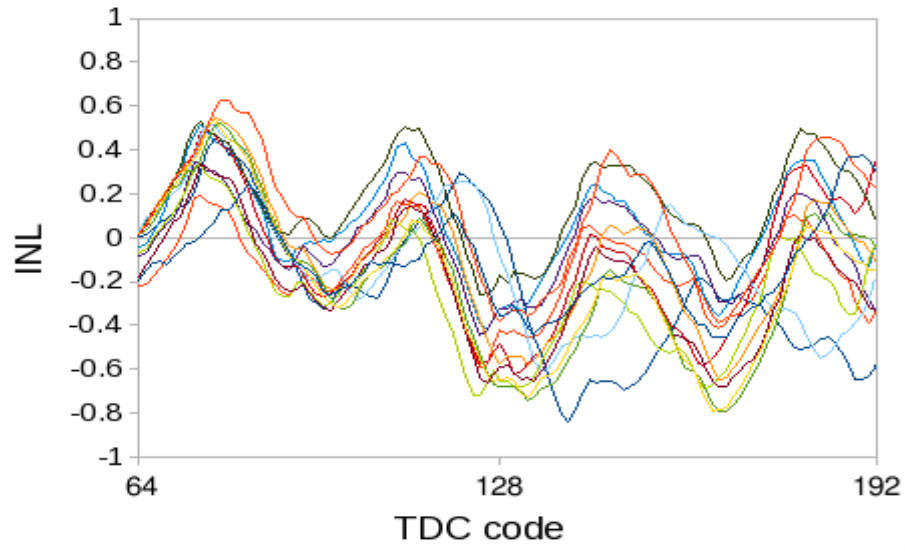
$$DNL(i) = \frac{N_{meas}(i) - N_{th}(i)}{N_{th}(i)}$$

$$INL(i) = \Sigma_{k=0}^{i} DNL(k)$$

$$|DNL(i)| < 0.5$$

$$|INL(i)| < 1$$

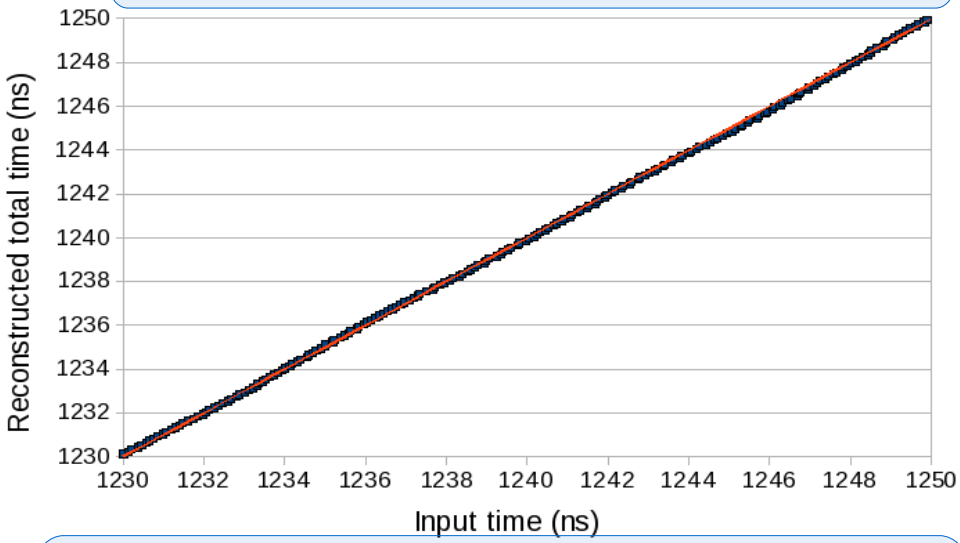




TDC configuration	
00	Running mode
01	Calibration mode ($1T_{ck}$)
01	Calibration mode ($3T_{ck}$)
11	Test mode

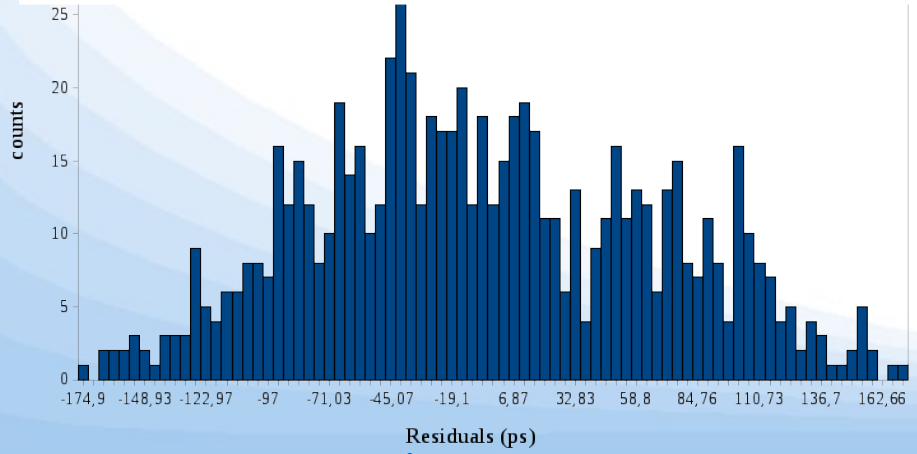
The TDC: results

196 ps bin @ 80 MHz

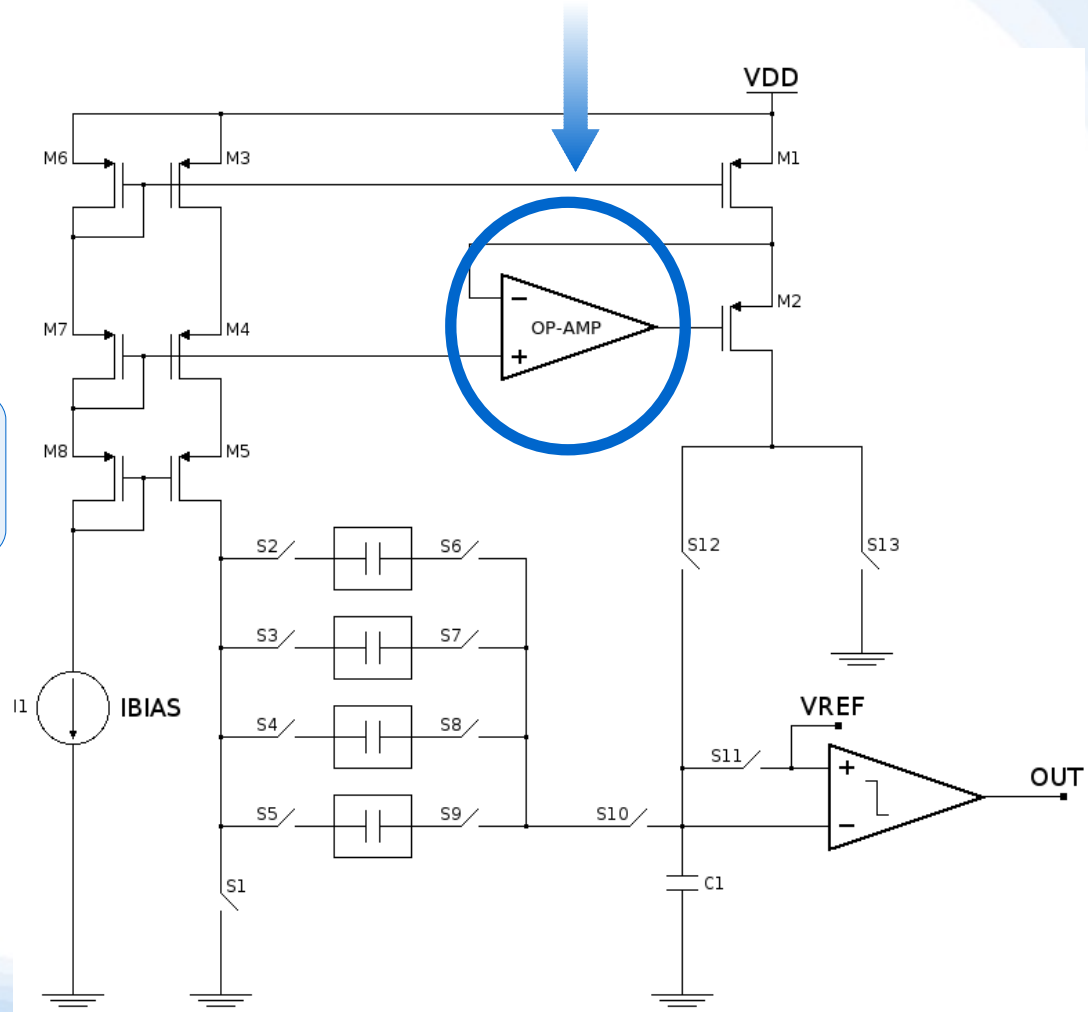


Error: 350 ps peak2peak

(73 ps RMS)

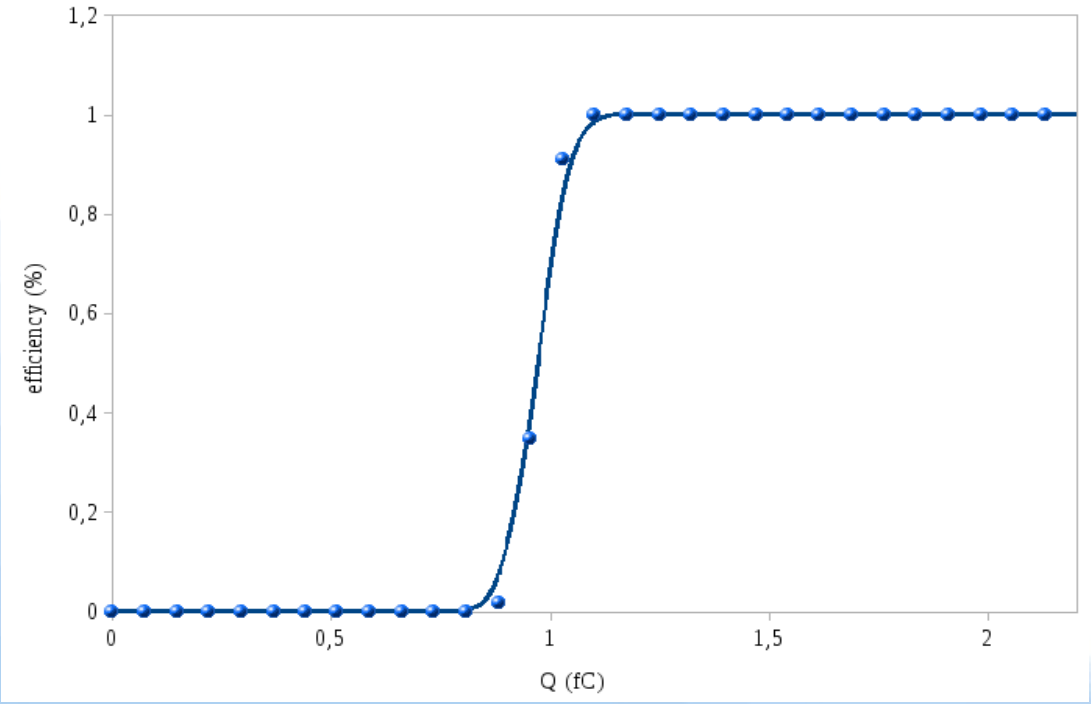


PSRR to be optimized



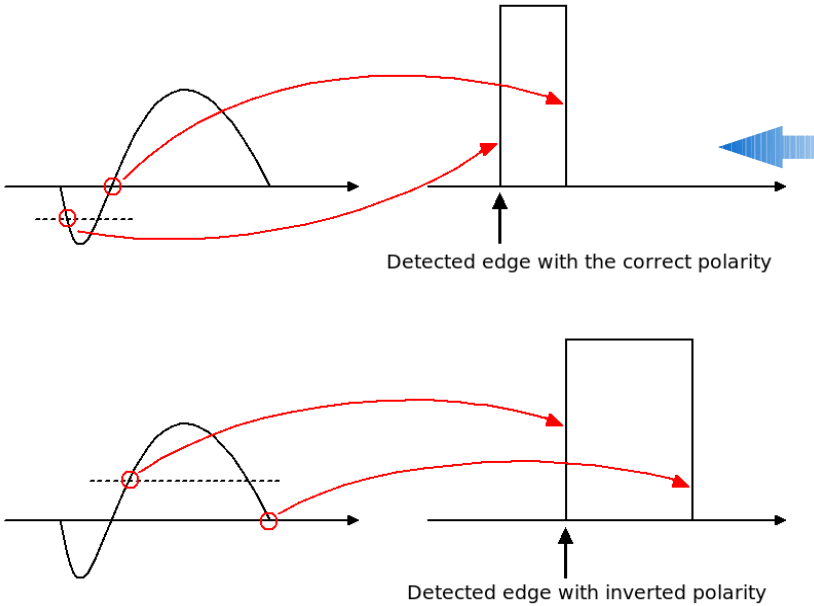
The full Front-End

Supply	Power consumption @ 1.2 V
Analog	897 μW/pixel
Digital (pixel)	343 μW/pixel
EoC	125 mW @ 160 MHz
Total	2.43 mW/pixel

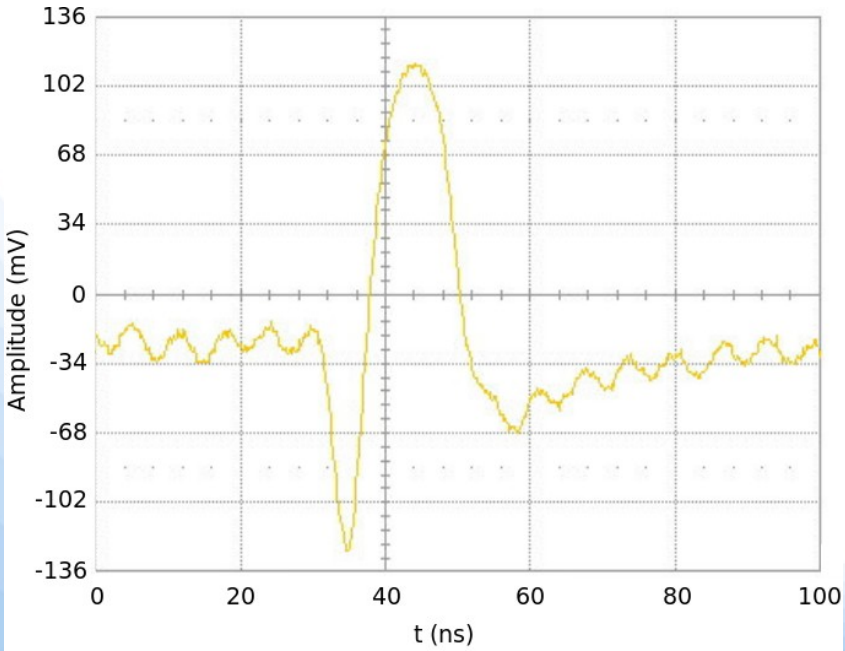


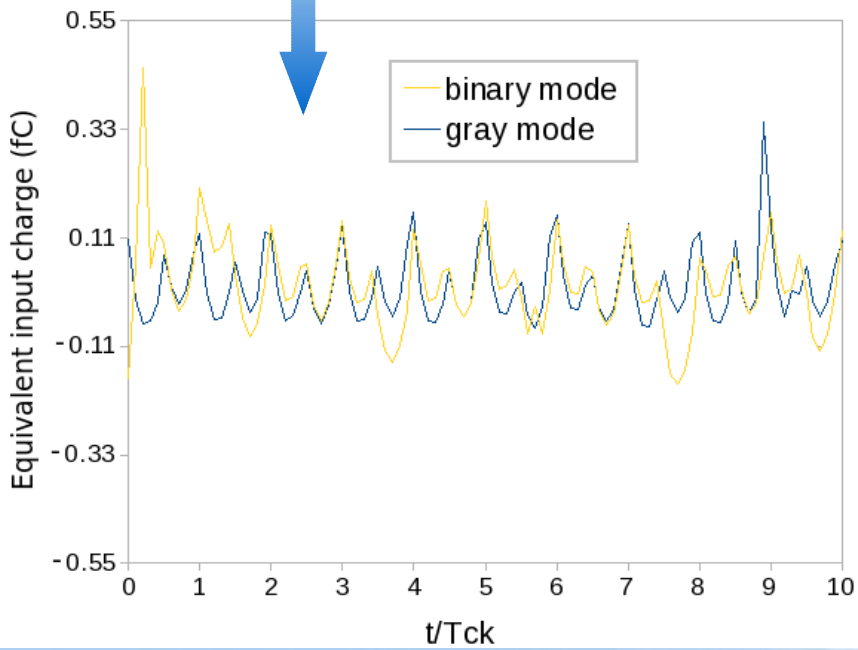
- 50% efficiency at 1 fC
- ENC = 310 e^-

Problems

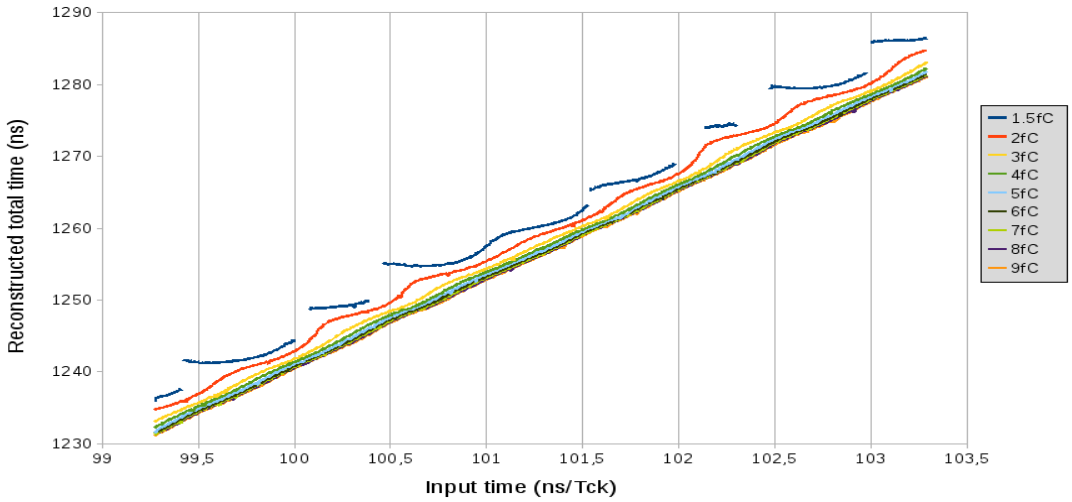


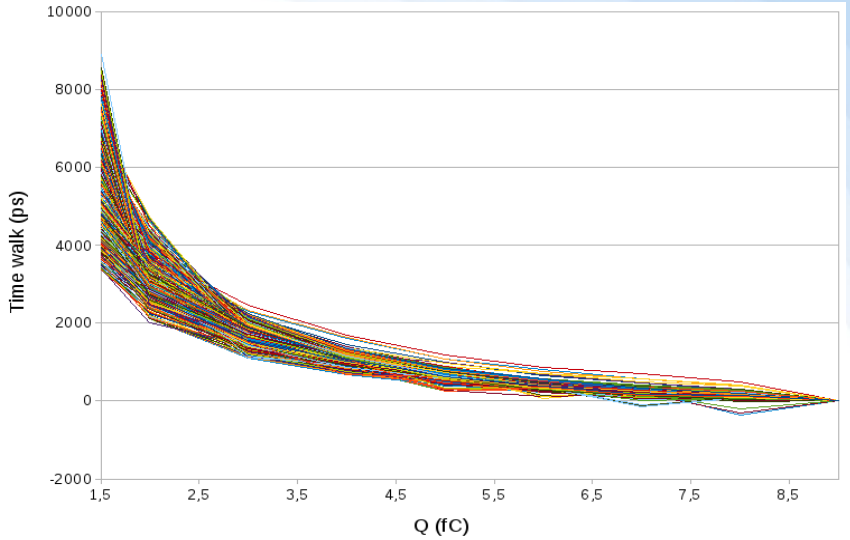
- Issue in the asynchronous digital logic of the CFD
- Substrate noise due to clock drivers





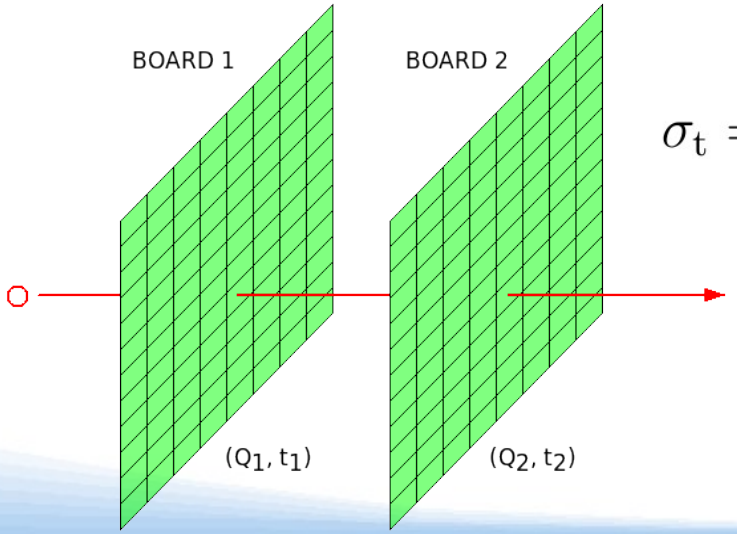
The time resolution





Time walk evaluated with Montecarlo simulations:
955 ps RMS

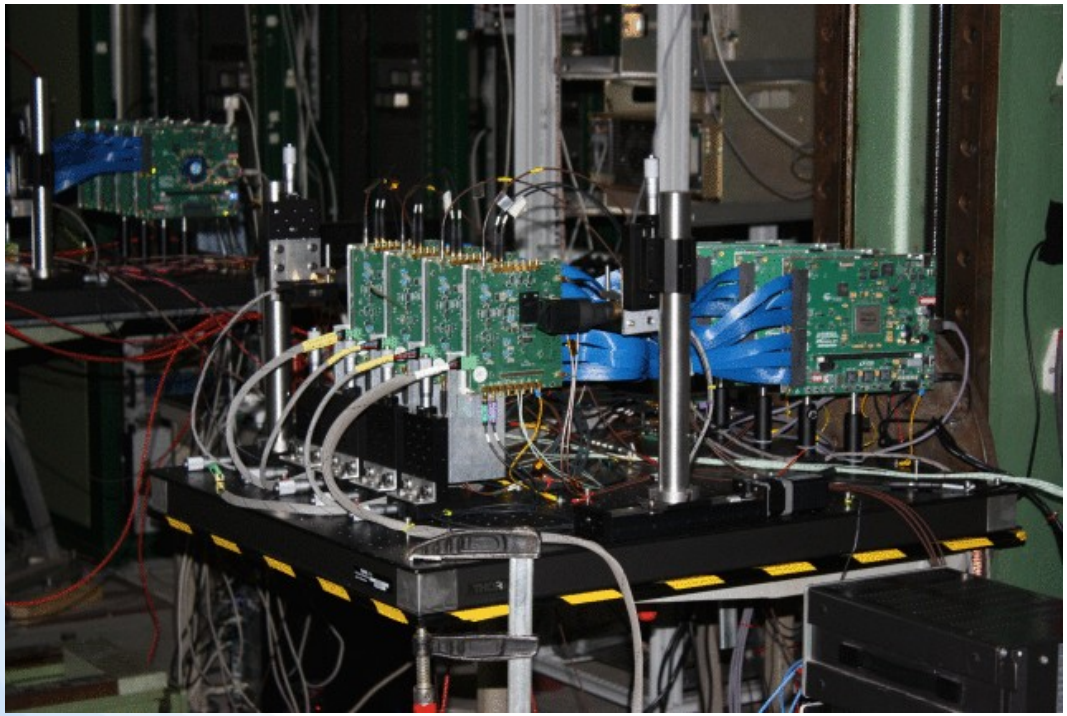
- Q_i randomly extracted from the Landau distribution
- t_i corresponding to Q_i extracted from a random time walk curve

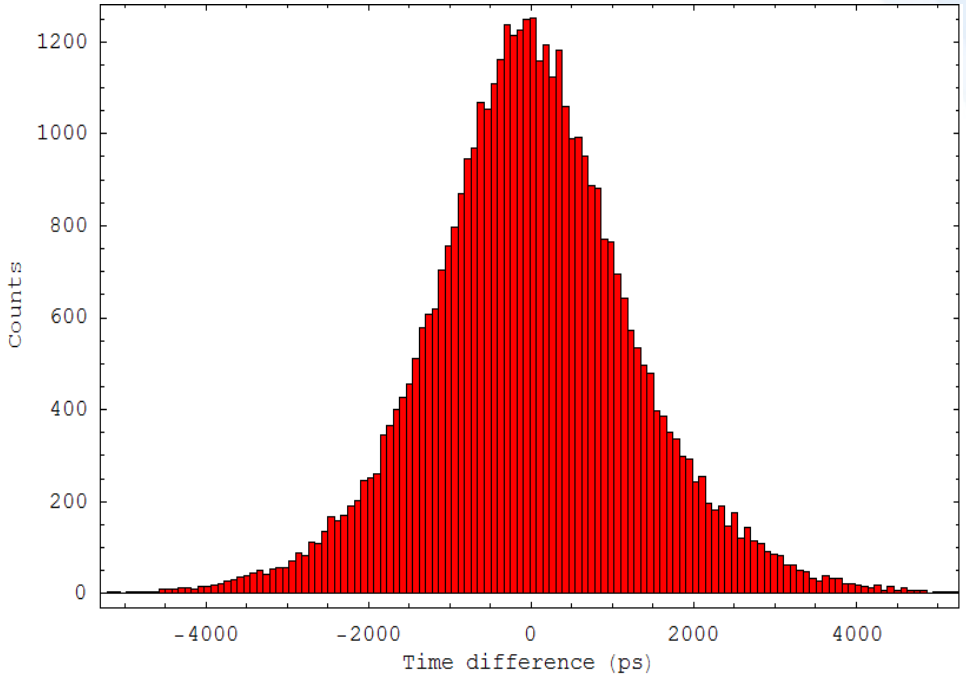


$$\sigma_t = \frac{\mathrm{RMS}(\Delta t)}{\sqrt{2}}$$

The time resolution

Beam test at CERN PS East Area in September 2010

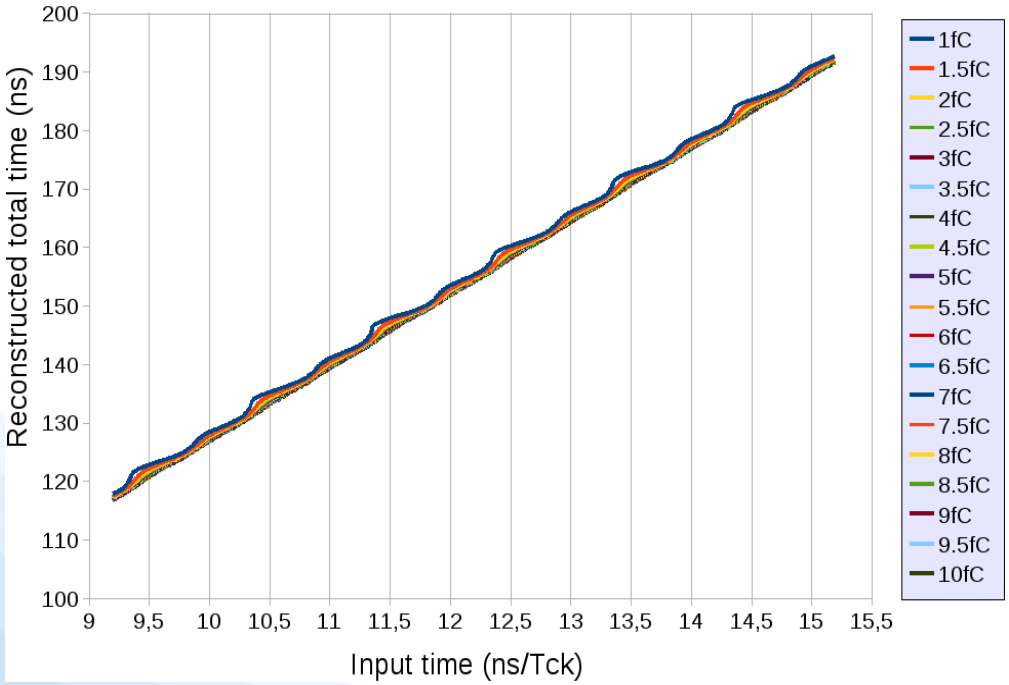


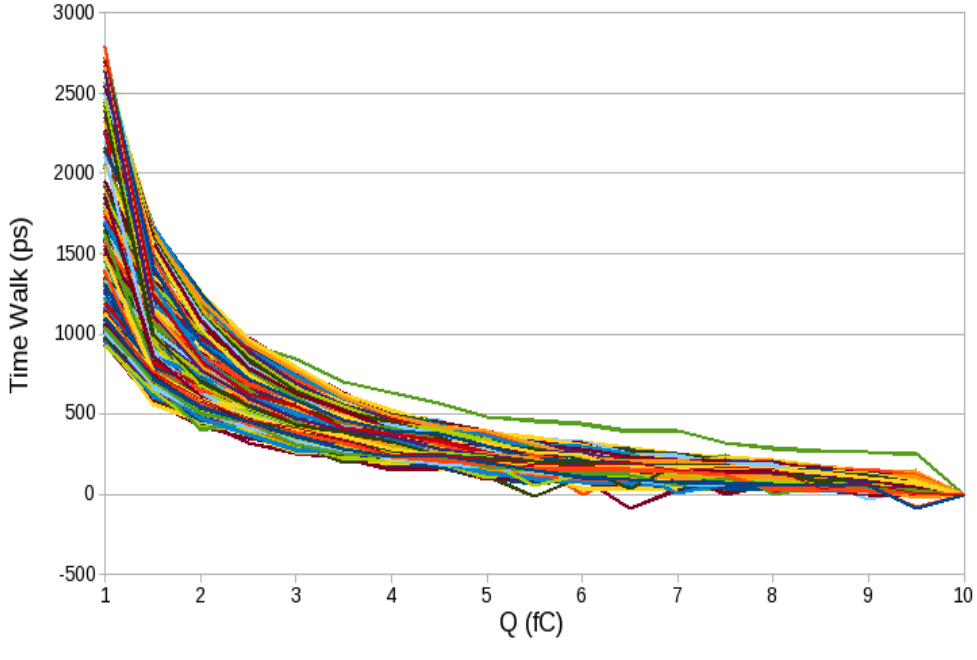


Time resolution: 910 ps RMS

The time resolution

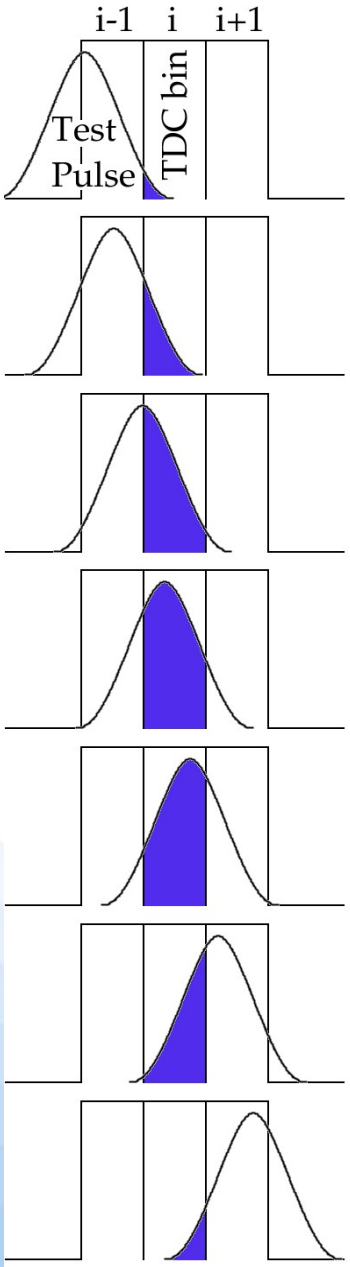
Optimization of the PCB: a capacitor on the reference voltage of the preamplifier increases the digital noise pick-up

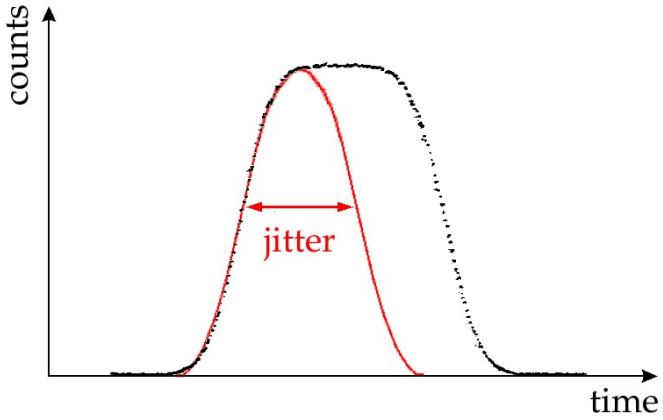


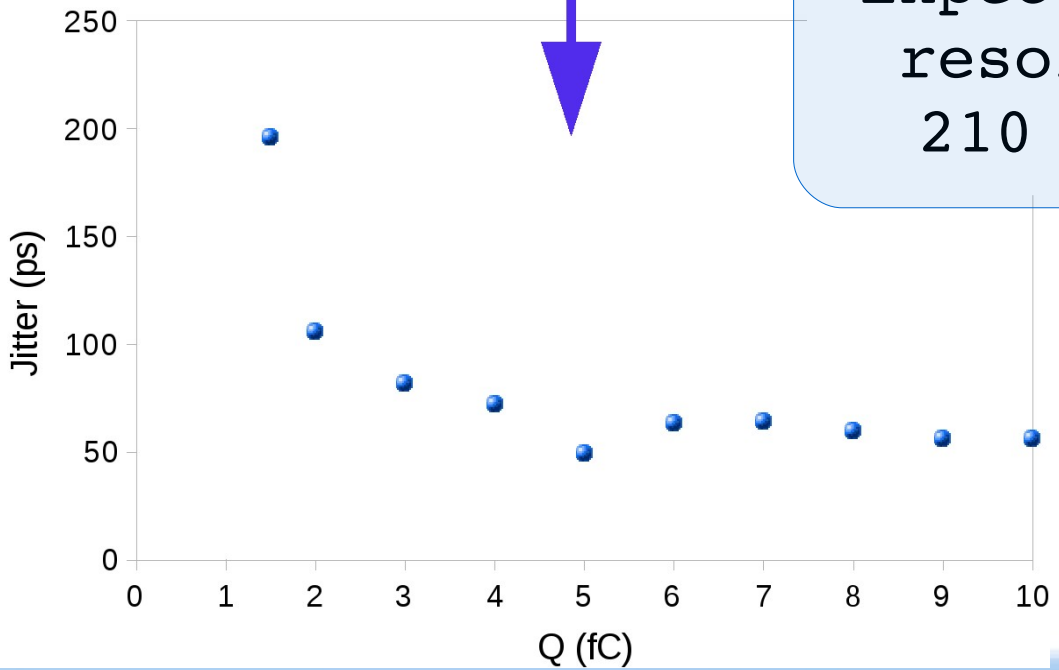


Time walk evaluated with Montecarlo simulations:
184 ps RMS

The time resolution

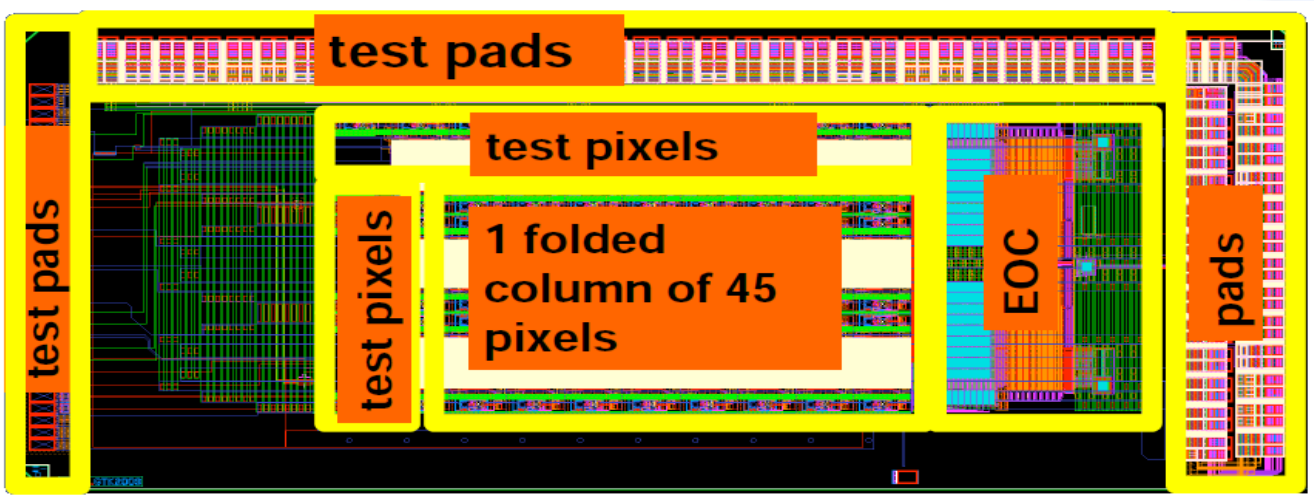






Expected time resolution: 210 ps RMS

The EoC demonstrator chip



70 ps RMS at the laser test

Signal shape variations

175 ps RMS at the beam test

A comparison

- The time resolution obtained with the EoC demonstrator is adequate for the purpose of the NA62 experiment, but is relatively close to the upper limit of 200 ps RMS. Due to its simplicity this architecture is ready for the engineering run: the challenge will be to preserve the good performance measured with the prototype at the full system level.
- All the blocks in the P-TDC architecture proved functional, but the digital noise limited the global timing performance to 900 ps RMS during the beam test. A new beam test should be performed to confirm the expected time resolution of 210 ps RMS obtained after the optimizations and another prototype step is required to test this architecture.

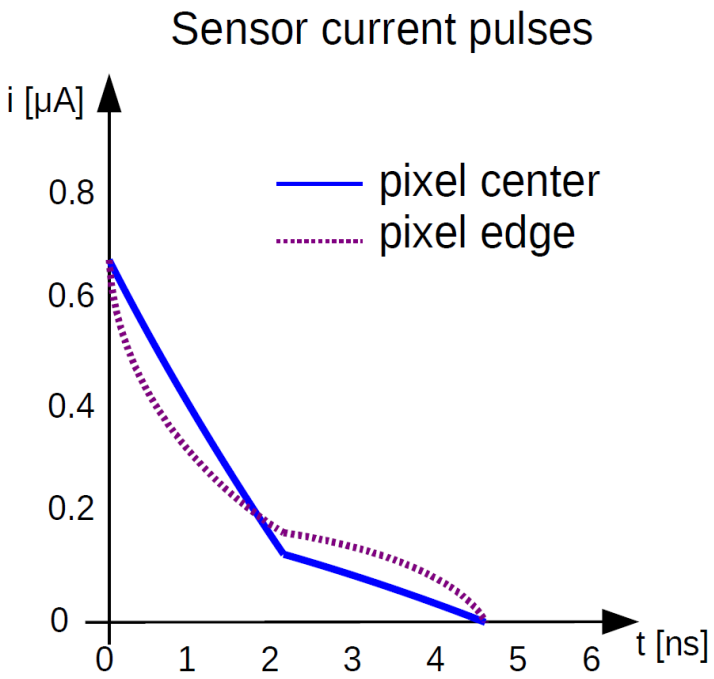
A comparison

- In principle a CFD based approach could be more resilient to the effect deriving from statistical shape variation, provided that the delay and the fraction of the CFD network are properly chosen. Additionally it could reduce significantly the burden of the calibrations.
- Thanks to its flexibility the P-TDC architecture is attractive for many medical, physical and commercial applications.
- Anyway, for the contingency of the experiment the EoC architecture has been chosen as the baseline solution for the GTK, while the P-TDC found place in other applications.

Section 5

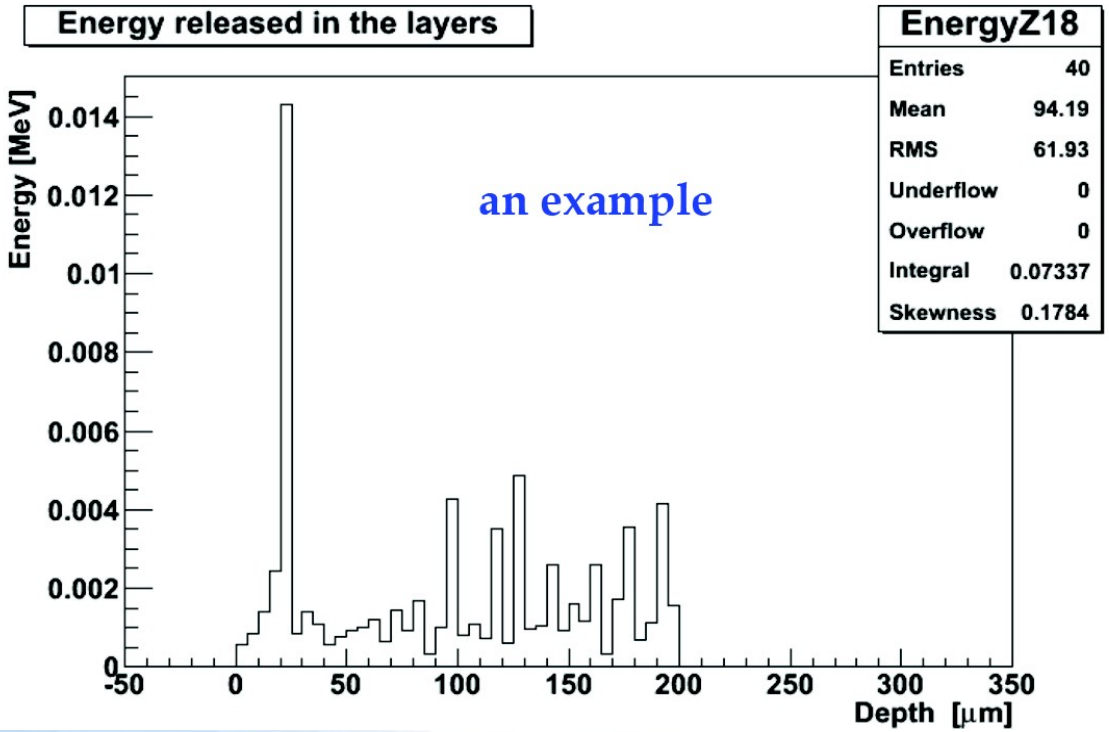
A new P-TDC front-end ASIC with improved pulse shape rejection

Signal shape variations



Border effect

Charge straggling

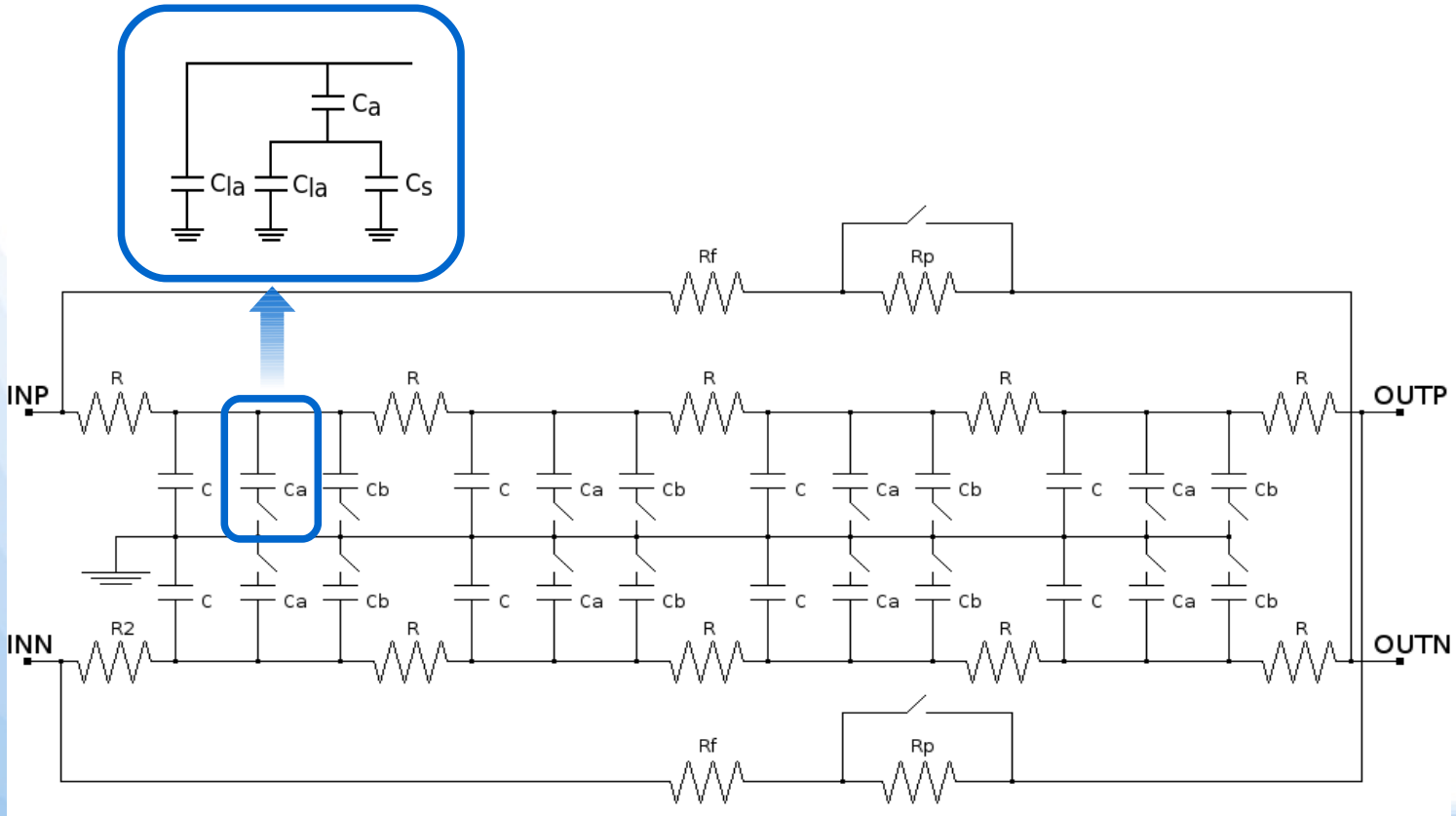


The CFD optimization

- Halved delay for better rejection of signal shape variations
- Optimization of components for process variations

$$V(t) = Ate^{-\frac{t}{\tau}}$$

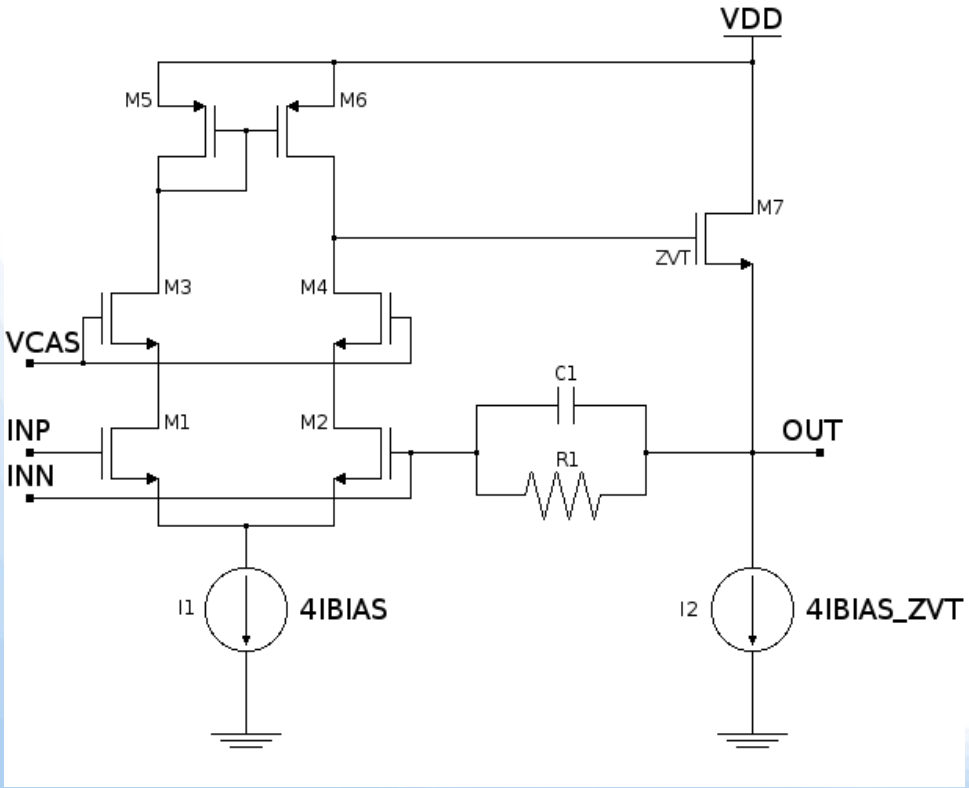
$$t_{zc} = \frac{t_d}{1 - fe^{-\frac{t_d}{\tau}}}$$

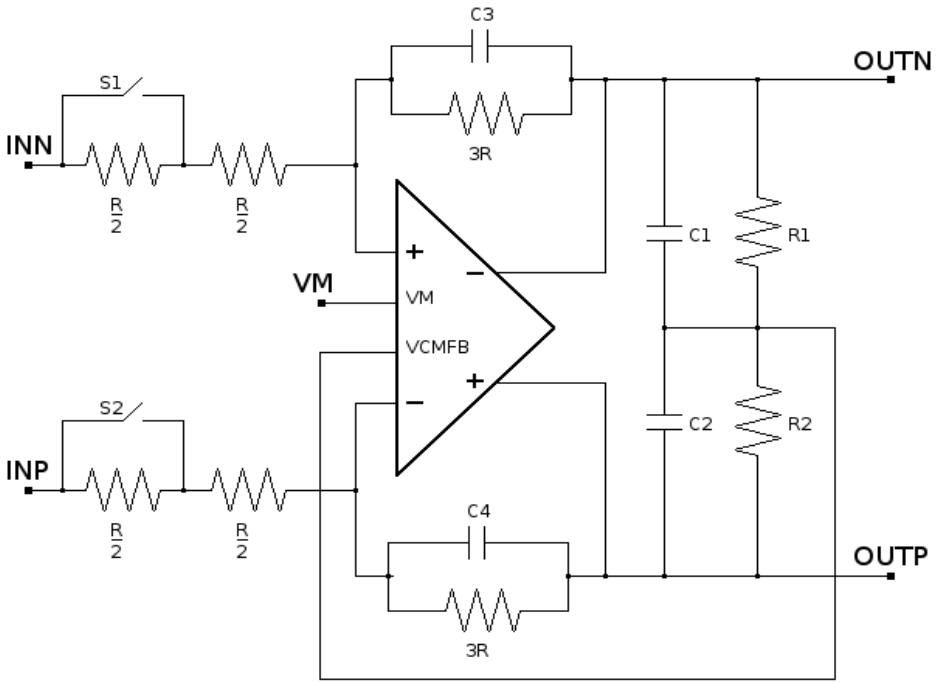


Component	value
R	629.1 Ω
R_f	6R
R_p	R
C	7.64 fF
C_a	76.18 fF
C_b	166.18 fF

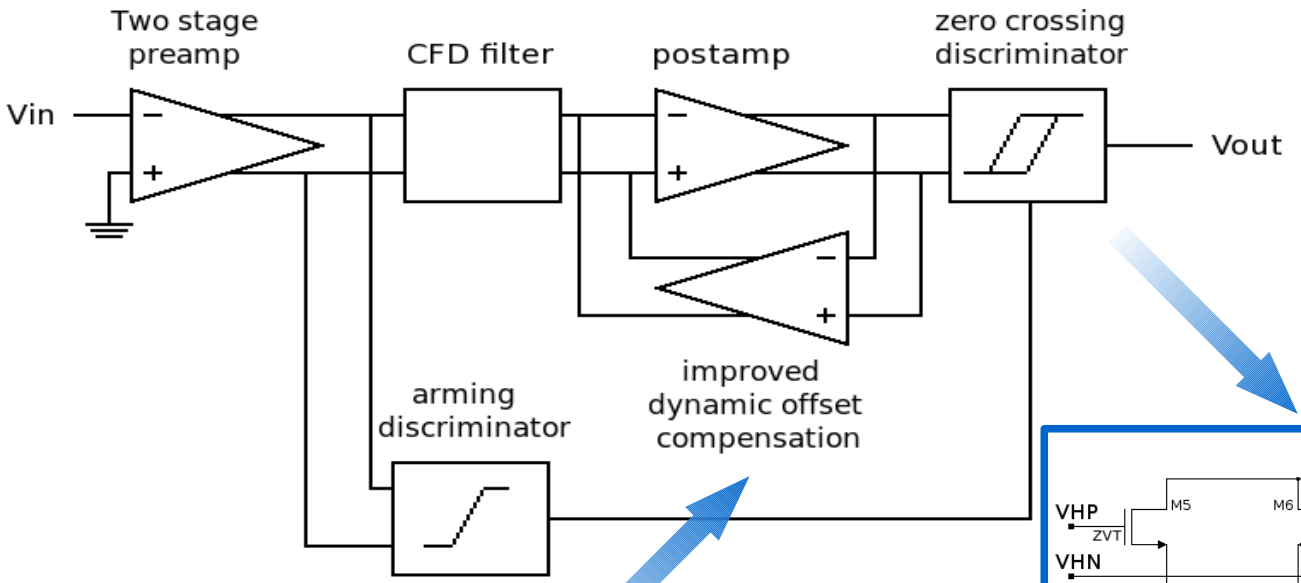
The new preamplifier design

- Back to a one pole single-ended configuration for better stability
- Programmability of the second stage to face the effect of sensor deterioration

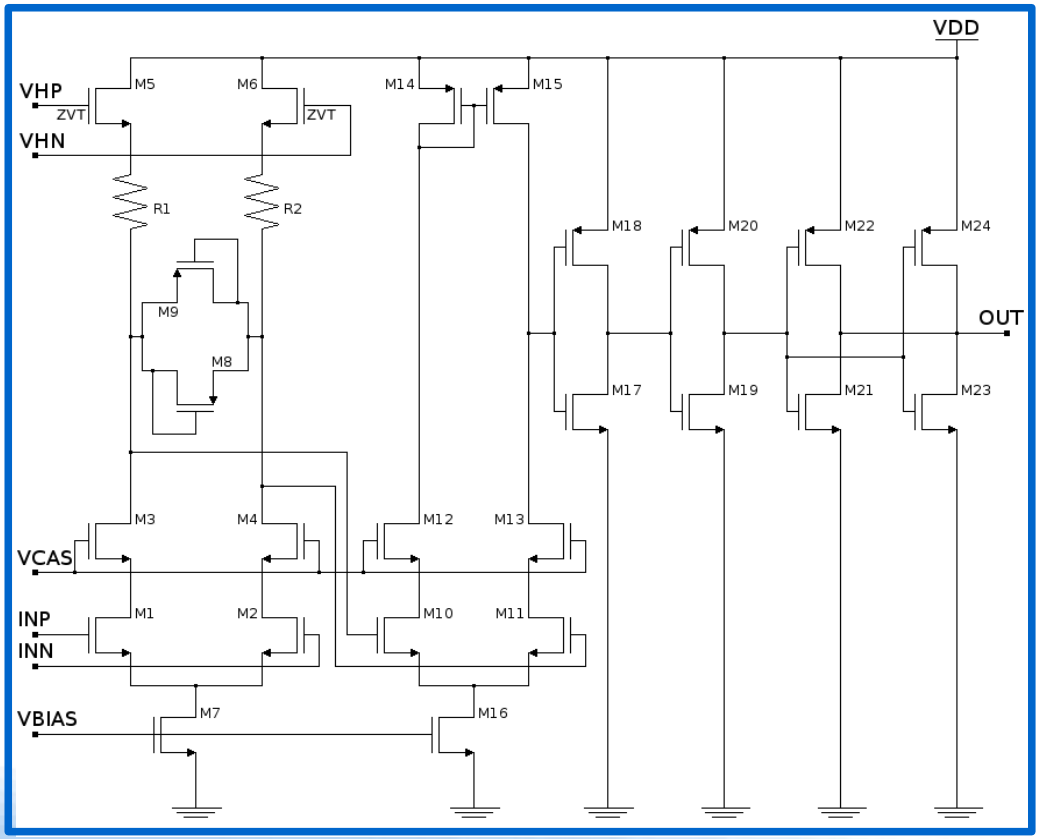




The improved Front-End



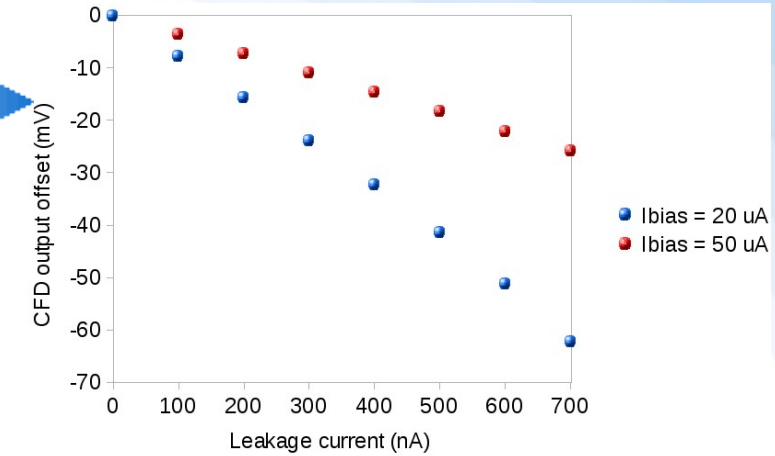
Leakage compensation performed at this point

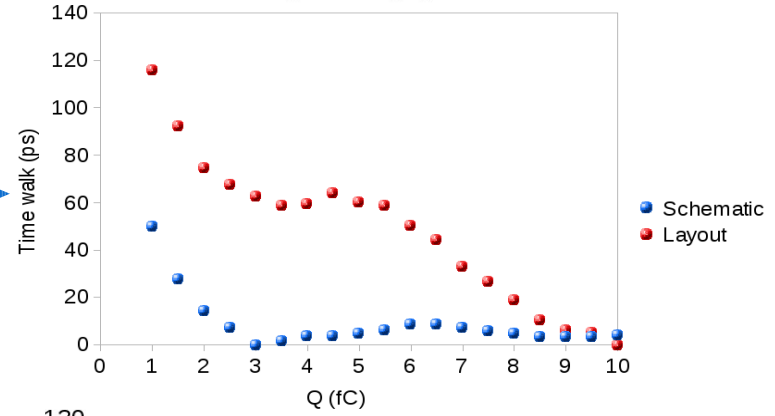


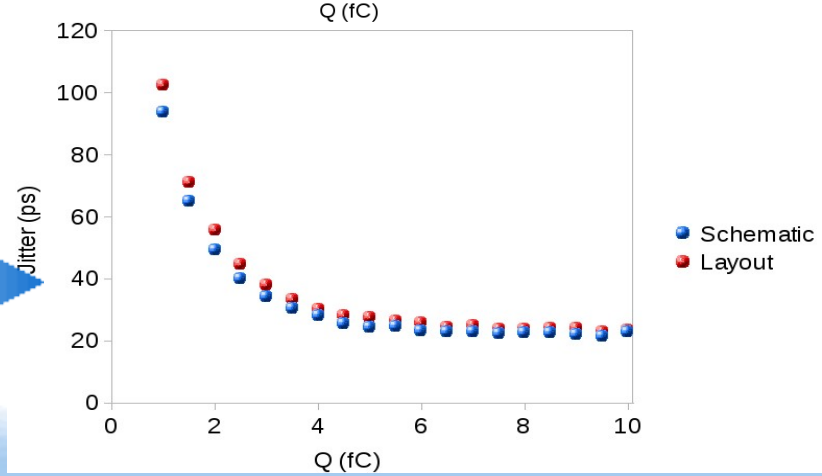
Simulation results

Preamplifier gain	95 mV/fC
Preamplifier peaking time	3 ns
ENC	308 e^-
Dynamic range	1-10 fC
Leakage compensation capability	± 700 nA
Overall offset referred at the discriminator input	+38 mV ÷ −22 mV
ZC discriminator contribution to offset referred at its input	±10 mV
ZC discriminator charge sensitivity	28 ps peak-to-peak
Time resolution in typical mean	68 ps RMS
Power consumption	1.18 mW

	Component area (μm^2)	Power consumption (μW)
First stage preamplifier	29 x 51	180
Preamplifier replica	29 x 33	45
Second preamplifier stage	48 x 84	606
CFD filter	141 x 69	0
CFD postamplifier	25 x 82	156
Arming discriminator	31 x 12	96
ZC discriminator	31 x 12	96

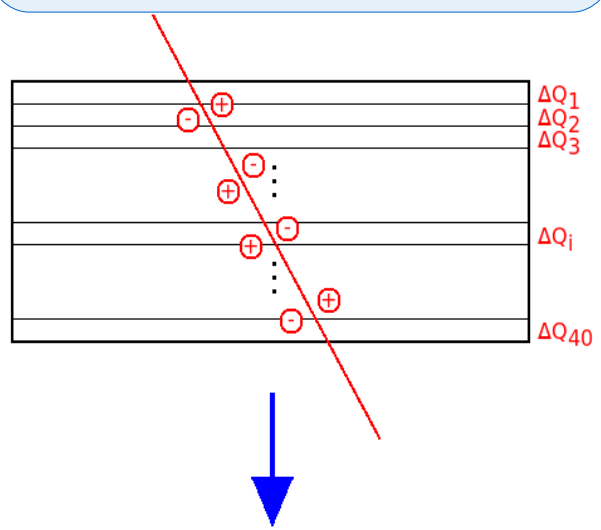


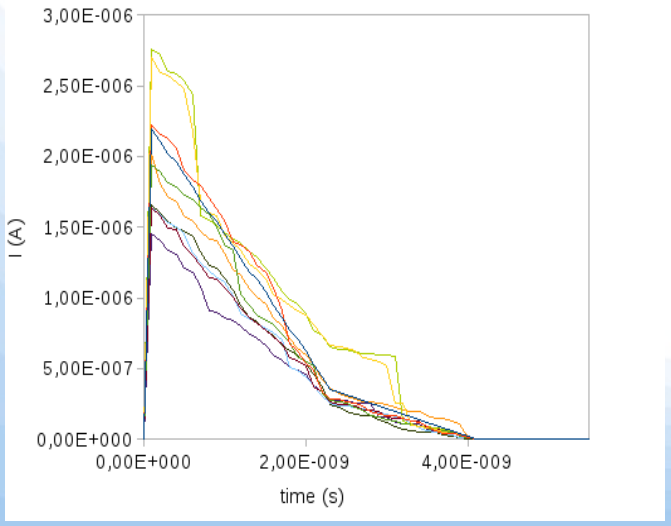




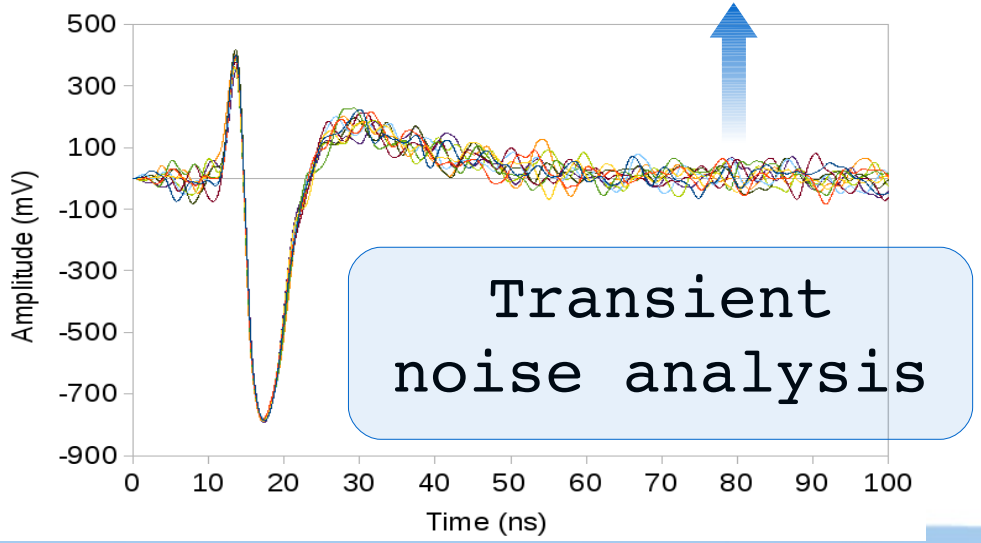
Simulation results

200 Montecarlo simulations with Ocean





Schematic results			
Process corner	RMS Jitter @ 1MIP (ps)	Error due to signal variations (ps RMS)	Time resolution (ps RMS)
Typical mean	40	20	53
$+1.5\sigma$	45	27	48
$+3\sigma$	52	23	59
-1.5σ	38	23	52
-3σ	38	21	67
Layout results			
Process corner	RMS Jitter @ 1MIP (ps)	Error due to signal variations (ps RMS)	Time resolution (ps RMS)
Typical mean	47	27	68
$+1.5\sigma$	50	31	55
$+3\sigma$	59	30	86
-1.5σ	44	27	65
-3σ	45	24	95



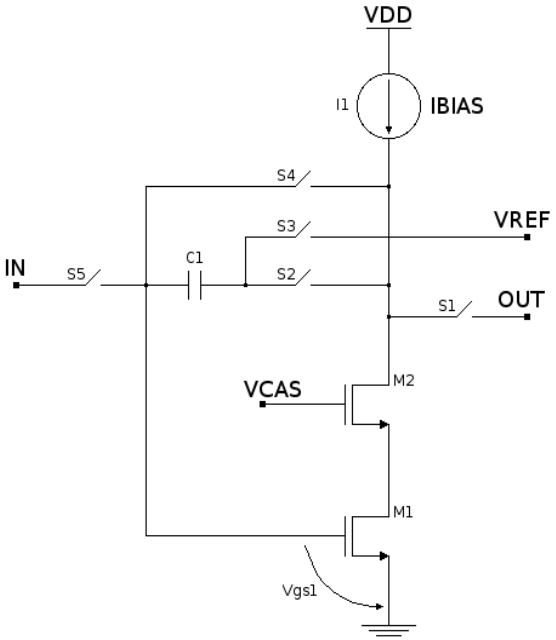
Transient noise analysis

Conclusions

- This work focused on the development of a low power front-end for precise timing (~100 ps RMS) multichannel applications in the framework of the R&D of the GTK for NA62
- The CFD represents an effective approach to minimize time walk when the dynamic range is not too large so that the linearity of the system can be maintained
- The development of a prototype, produced in 2009 and tested in 2010, allowed to test the functionality of the single blocks and of the full chip architecture
- Problems are mainly due to noise injection which in a first phase resulted in more than 900 ps RMS. However optimizations led to a time resolution of the order of 210 ps RMS
- A new design is under development to improve the signal shape rejection
- It also combines the timing and amplitude amplitude leading to a flexible architecture suitable for a lot of other modern timing applications besides the GTK

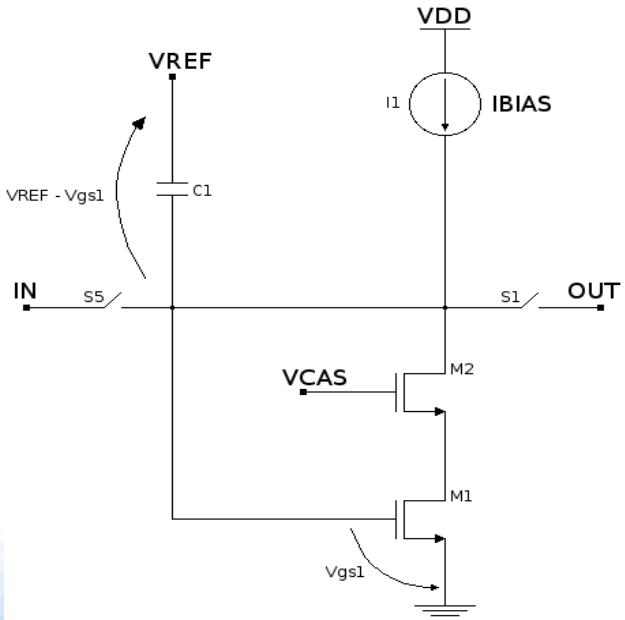
Questions?

The TAC: schematics

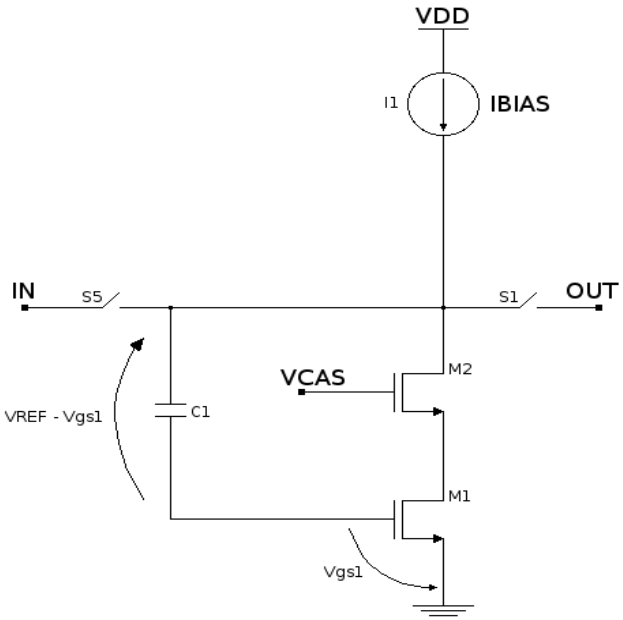


The TAC:

- Reset mode: S3, S4 closed
  S2 open
- Normal mode: S3, S4 open
  S2 closed

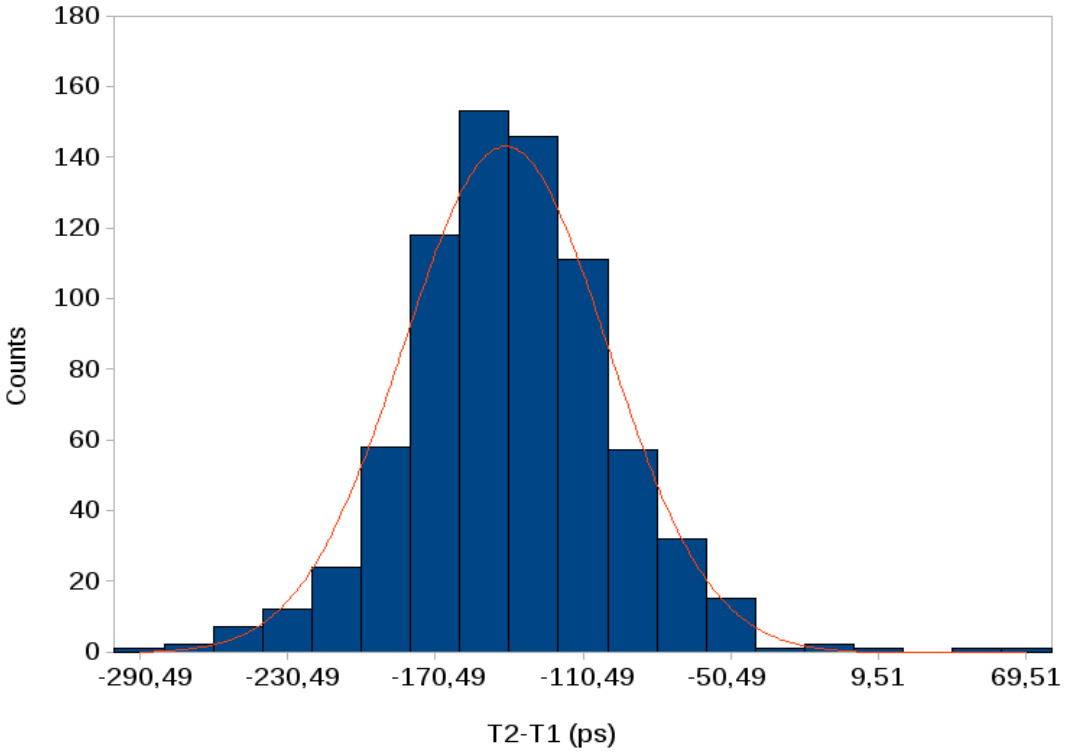


RESET



NORMAL

The TDC: results



One Test Pulse every 16 clock cycles: measure dominated by the non linearities of the ramp

	Measured quantity	Mean value (ps)	Standard deviation (ps)
BUFFER II	T_2 - T_1	-149.83	41.35
BUFFER III	T_3 - T_1	-111.46	79.71
BUFFER IV	T_4 - T_1	-211.50	61.05