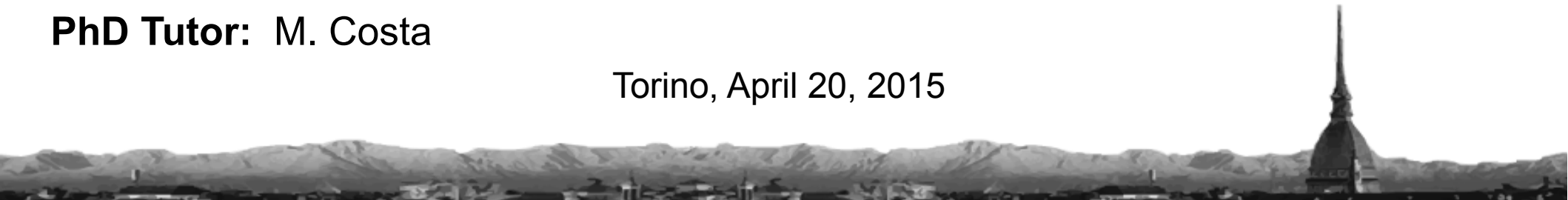
Development of Integrated Pixel Front-End Electronics in 65 nm CMOS Technology for Extreme Rate and Radiation at HL-LHC

Luca Pacher

University of Torino
Graduate School in Physics and Astrophysics
XVII cycle

Supervisor: A. Rivetti
PhD Tutor: M. Costa

Torino, April 20, 2015

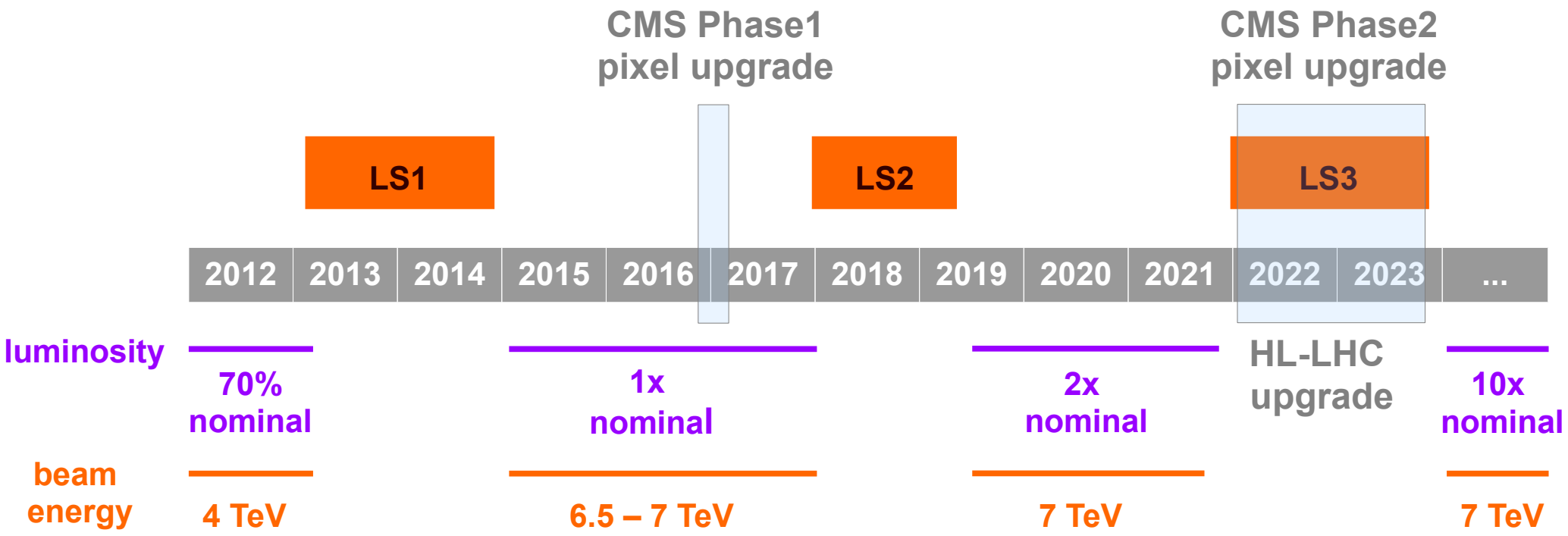


Outline

- Background, framework and motivations
- Synchronous Front-End design in 65 nm CMOS technology
- Test results from first prototypes
- Conclusions

Part I – Background, framework and motivations

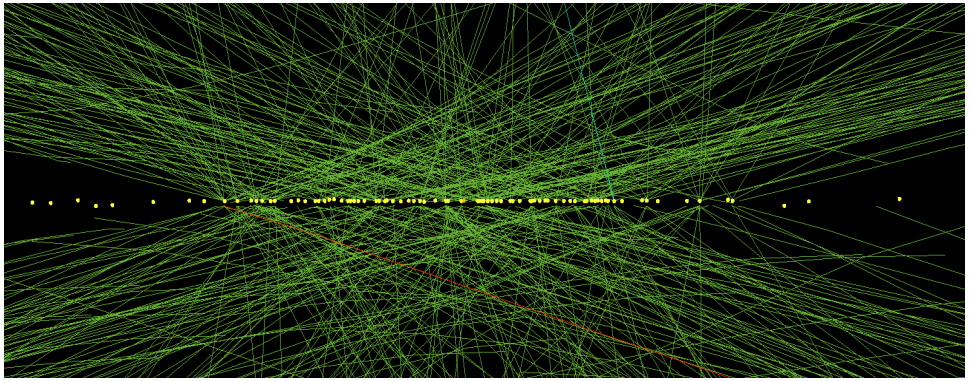
LHC timeline



- 3 main LHC commissioning periods referred to as **Phase0** (up to LS1), **Phase1** (after LS1) and **Phase2** (after LS3)
- **shutdown** time-slots for maintenance and machine performance improvements
  - nominal LHC: 10^{34} cm^{-2} s^{-1} luminosity, 14 TeV centre-of-mass energy
  - **High-Luminosity (HL) LHC**: 10^{35} cm^{-2} s^{-1} luminosity, 300fb^{-1}/year, foreseen 3000 fb^{-1} in 10 years

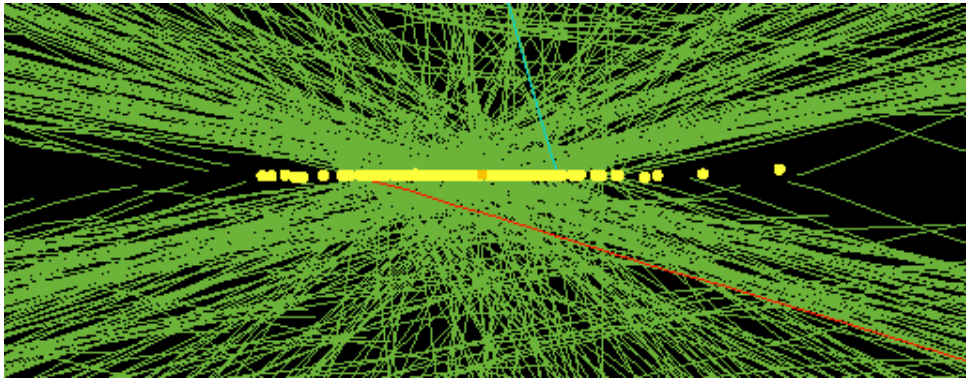
LHC luminosity upgrades

LHC Phase 1



- Up to 2 x 10^{34} cm^{-2} s^{-1}
- 7 TeV/beam *p-p*
- PU 50-70
- 50-25 ns BX

LHC Phase 2



- ~10^{35} cm^{-2} s^{-1}
- 7 TeV/beam *p-p*
- PU 140-200
- 25 ns BX mandatory

The foreseen HL-LHC upgrade will introduce **unprecedented operating conditions** in terms of **track densities** (10x Phase0) and **radiation levels** (10x Phase0).

Phase 2 pixel upgrades motivations

Parameter	LHC Phase0	LHC Phase1	LHC Phase2
luminosity	10^{34} cm^{-2} s^{-1}	2x10^{34} cm^{-2} s^{-1}	10^{35} cm^{-2} s^{-1}
PU	~20	~50	140 or higher
particle flux	50 MHz/cm^2	200 MHz/cm^2	500 MHz/cm^2
hit rate	200 MHz/cm^2	600 MHz/cm^2	1-2 GHz/cm^2
TID (10 years)	1.5 MGy	3.5 MGy	10 MGy
signal threshold	2.5-3 ke	1.5-2 ke	1 ke or below
L1 trigger latency	2-3 μs	4-6 μs	6-20 μs

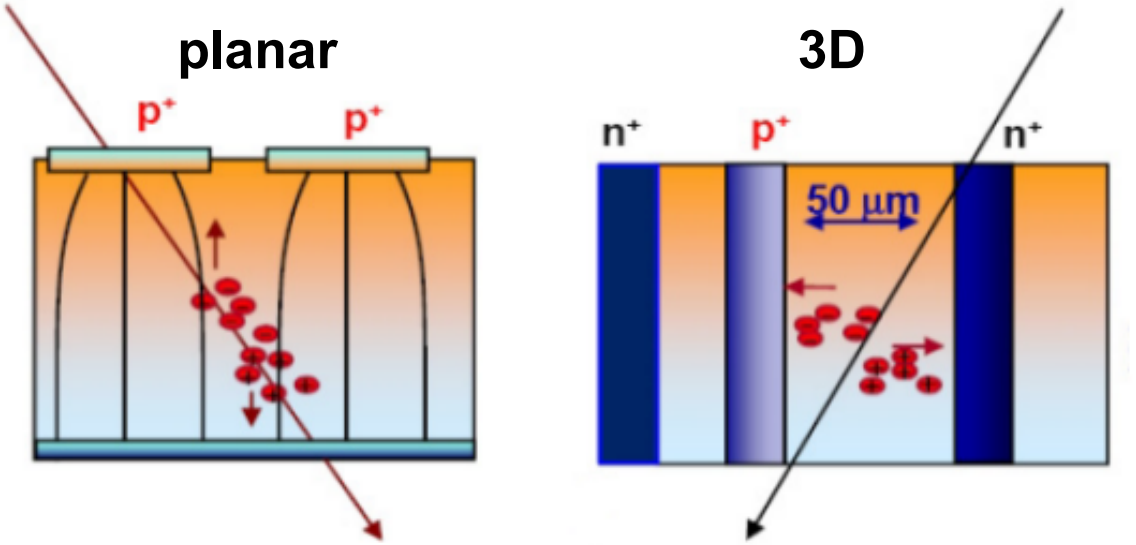
design of a new pixel readout chip required for HL-LHC

*N.B. This is essentially a talk on **analogue** pixel Front-End electronics ! No digital readout considerations are discussed ... please, ask if you are interested in some readout aspects*

New pixel ASIC requirements /1

- **sensor** choice not yet finalized :
  - very likely planar sensors in the outer layers
  - ongoing RD studies for innermost layers (thin planar sensors? 3D sensors? diamonds?)

- certaily **thinner sensors** to ensure adequate radiation tolerance
  - assume about 100μm thickness (1MIP ~10ke) for Phase2 (280μm current)
  - **low-noise** and **very low-threshold** Front-End electronics requirements



- **50 fF** up to **300 fF** total input capacitance
- **1 ke** minimum detectable charge
- **20 nA** worst case leakage currents (TBC)

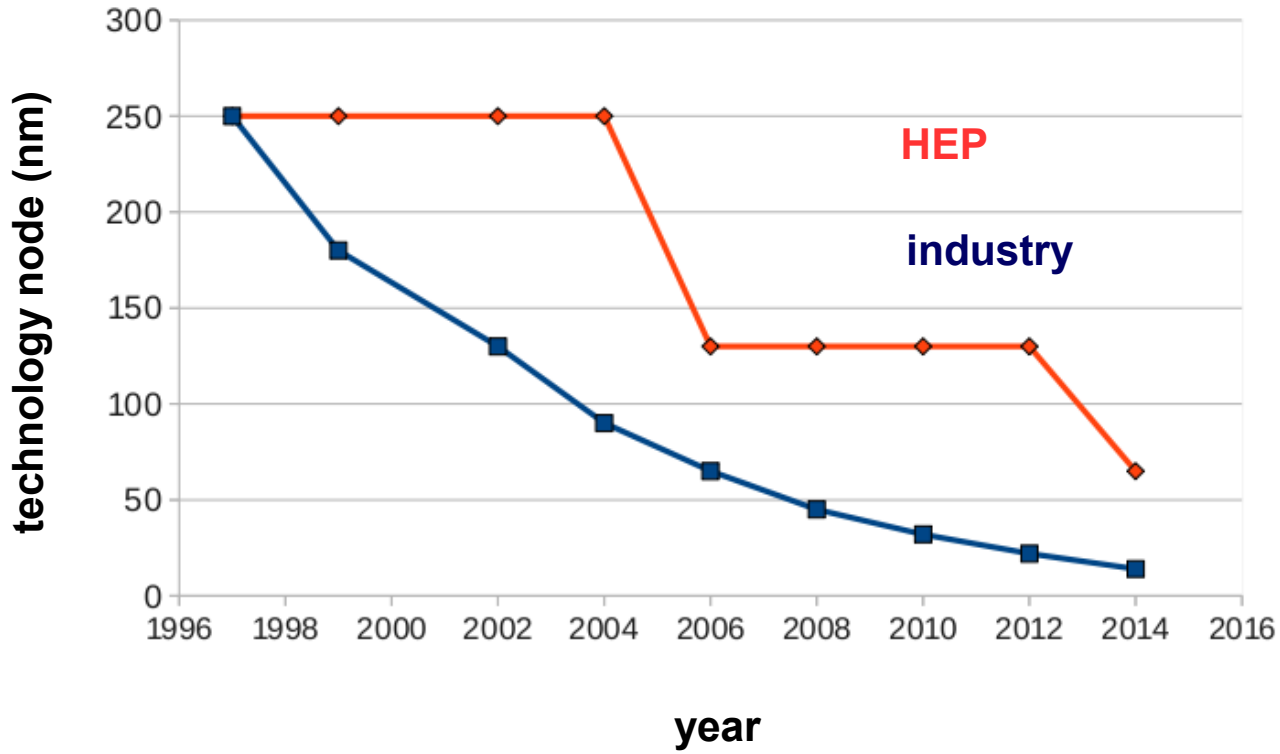
New pixel ASIC requirements /2

- increased track densitites => 10x Phase0
  - **smaller pixel size** for necessary **granularity**
  - assume 50μm x 50μm or 25μm x 100μm (100μm x 150μm current CMS pixels)
- increased **hit rates** => assume 2 GHz/cm^2
  - 50kHz/pixel for 50μm x 50μm pixels
- larger amount of digital data to handle => ~100 Gb/s for a ~ 2cm x 2cm chip
  - **charge encoding** ... at the pixel level
  - **buffering** ... at the pixel level
  - **trigger matching** for **zero suppression** ... at the pixel level !
  - more **on-pixel intelligence** and local data storage capabilities
  - possible contributions to the L1 trigger ?
- much larger **output BW** => ~3 Gb/s (40 MHz in the present CMS ROC...)

IC technology choice (and... HEP vs industry)

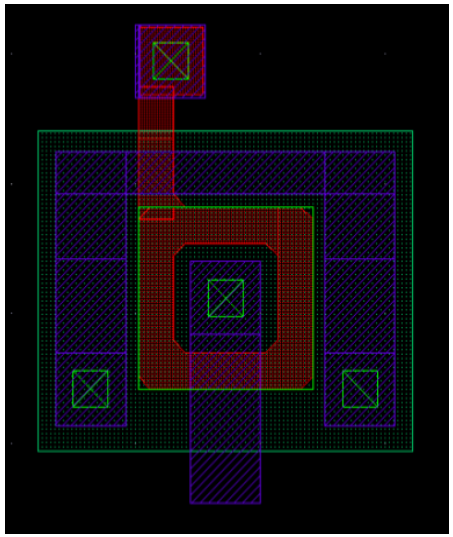
A commercial **65 nm CMOS** has been chosen by the **pixel ASIC community** as a promising fabrication technology for the Phase2 generation pixel readout chips

- present LHC experiments based on a commercial **CMOS 250 nm RHBD**
- Phase1 LHC upgrades and many other HEP projects now use **CMOS 130 nm** (e.g. FE-I4 chip for the ATLAS IBL, GBT project, TimePix, ToPix, VeloPix etc.)

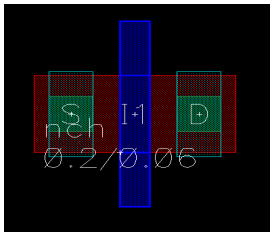


Why 65nm ? /1

- thinner gate oxides increase the **radiation tolerance**
- RHBD techniques with **Enclosed Layout Transistors (ELT)** no more required
- 65 nm demonstrated to be radiation tolerant up to 3 MGy TID, better than 130 nm (now to be confirmed up to 10 MGy)



full-custom library
0.25µm ELT NMOS



Not in scale !

standard library
65 nm NMOS

Why 65nm ? /2

- **low power**
  - 1.2 V supply voltage, same as 130 nm CMOS (2.5 V in 0.25 μm)
- a 65 nm offers **higher integration densities** w.r.t. 130nm
  - chance of implementing more **on-pixel intelligence** for efficient zero suppression schemes (on-pixel trigger matching)
- **improved speed** (~GHz)
- **mature technology**
  - introduced ~10 years ago
  - long term support and availability (OK for Phase2 ~2022)
- at present 65 nm CMOS represents **the most advanced technology node** adopted to implement full-custom solutions for radiation detection and measurements in particle physics and medical imaging applications

IC design in 65 nm

- digital design gains from **technology scaling** in terms of speed, integration density (higher functionality) and power/gate

- analogue design more challenghing
  - increased device-modeling complexity and number of **design rules**
  - **short channel effects** cannot be neglected
  - reduced **voltage headrooms** and single-transistor **intrinsic gain**

New communities on 65 nm CMOS

- similar requirements (and uncertainties) between ATLAS/CMS experiments Phase2 pixel upgrades

- joint ATLAS/CMS collaboration for sharing efforts in **technology qualification**
  - collaboration extended to other groups interested in designing in 65 nm
  - approved and officially supported by CERN as **RD53**

- ~ 20 institutes from around the world
  - about 100 collaborators, 50% ASIC designers
  - **strong Italian component** from INFN institutes (Bari, Bergamo/Pavia, Padova, Perugia, Pisa and Torino)

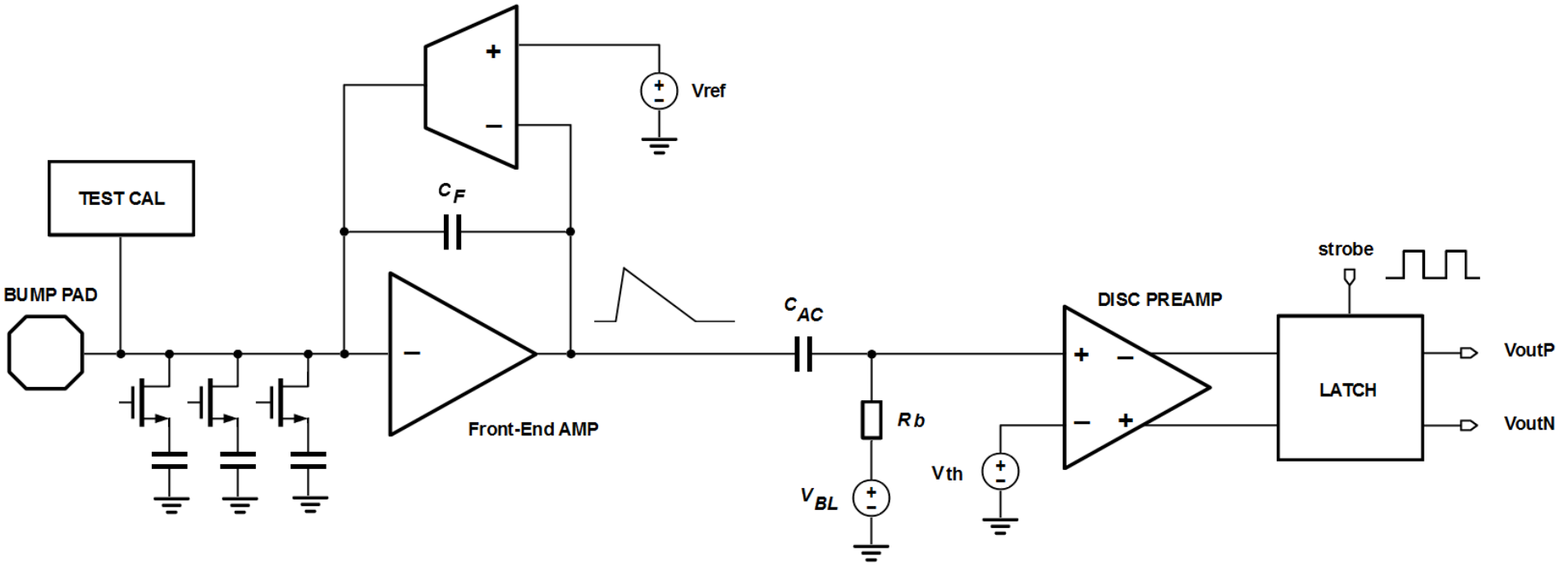
- **Italian** CMS/ATLAS groups submitted in July 2013 a detailed proposal to INFN CSN5 to finance a new RD on CMOS 65nm for the next three years
  - **CHIPIX65 project** approved in October 2013
  - **first sumbmission** to the foundry on October 2014 !

Part II – Pixel Front-End design in 65 nm CMOS

Analogue FE requirements

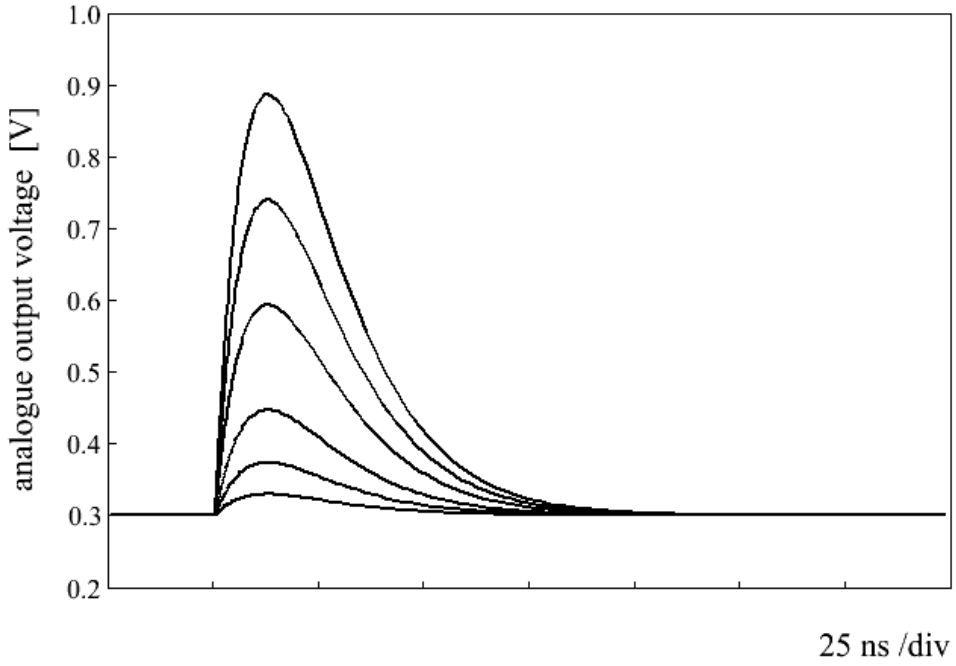
Parameter	Value
hit rate	2 GHz/cm^2
pixel size	50 µm x 50 µm (50% A + 50% D)
pixel rate @ 2 GHz/cm^2	50 kHz/pixel
power budget	10 µW/pixel (A+D)
hit time resolution	25 ns
signal threshold	1 ke or below
analogue power budget	5-6 µW/pixel @ 1.2 V
WC leakage current	20 nA at highest irradiation levels
linear dynamic range	up to 30 ke (4 MIP)
charge resolution	5-8 bit in less than 400 ns
noise budget	ENC < 150e @ 100 fF
sensor polarity	negative (electron collection)

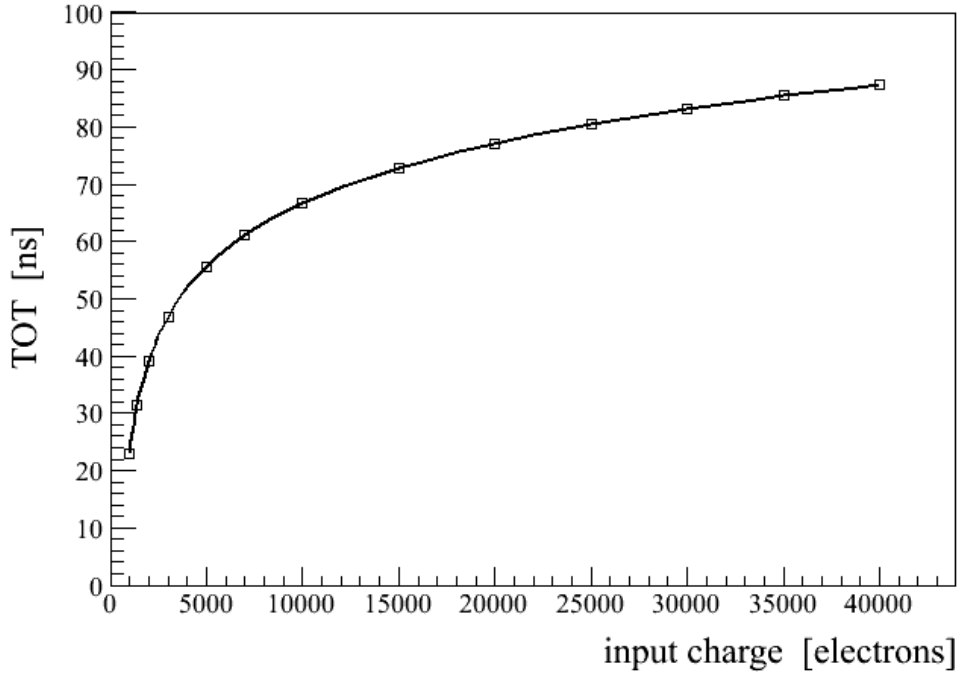
FE (simplified) architecture



- **shaper-less** FE chain => power, size ...
- CSA + transimpedance feedback network => signal shaping + leakage comp.
- test charge injection + shunt capacitors to emulate a sensor
- discrete-time voltage comparator => **synchronous FE architecture** !
- threshold adjustment by means of **autozeroing** (not shown...)

Time-over-Threshold /1

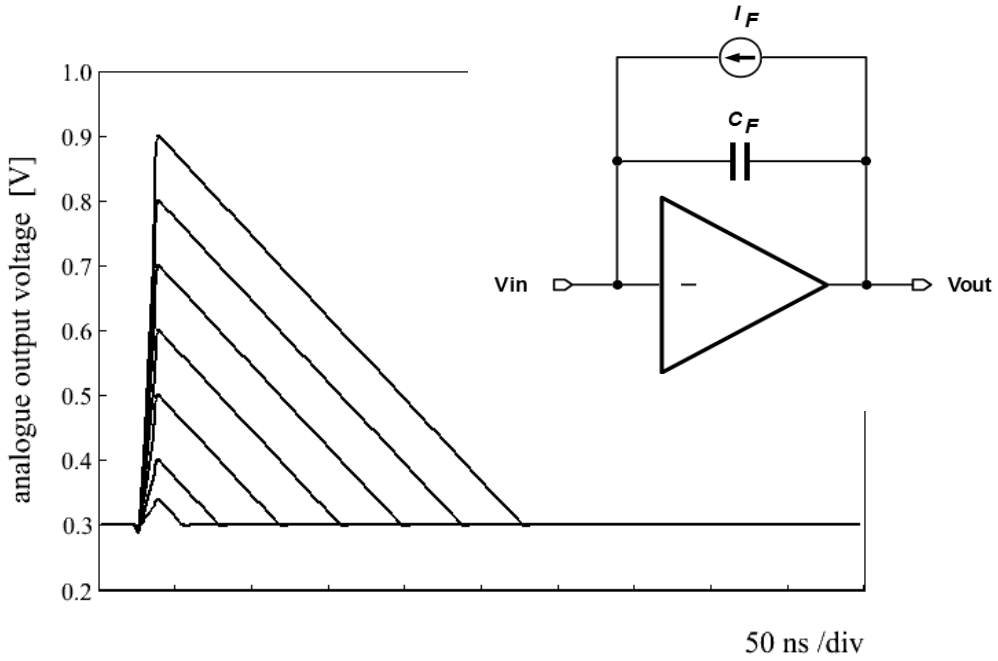


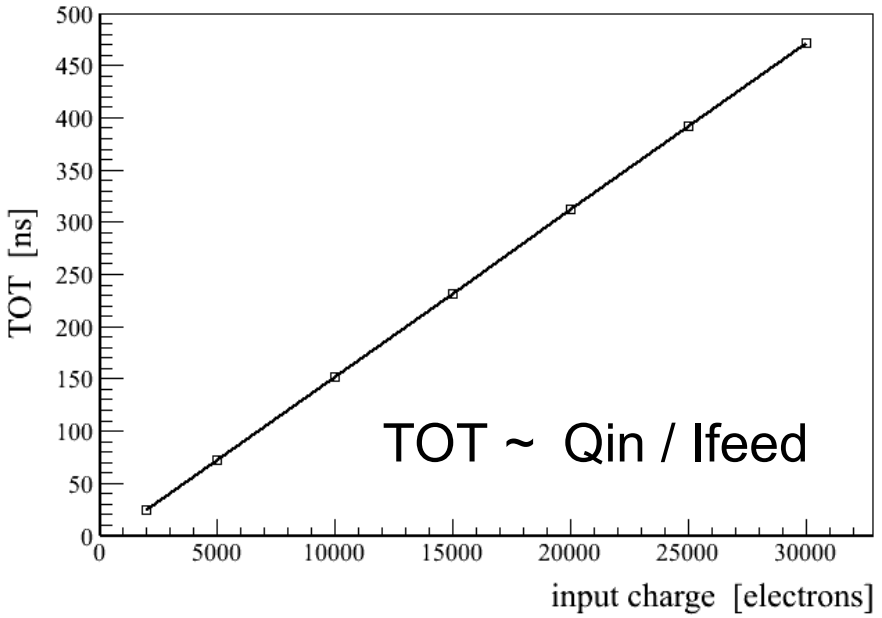


A resistive feedback (e.g. CR-RC) leads to a non-linear relationship between TOT and input charge

- not a limiting factor, just use LUTs for offline calibrations

Time-over-Threshold /2





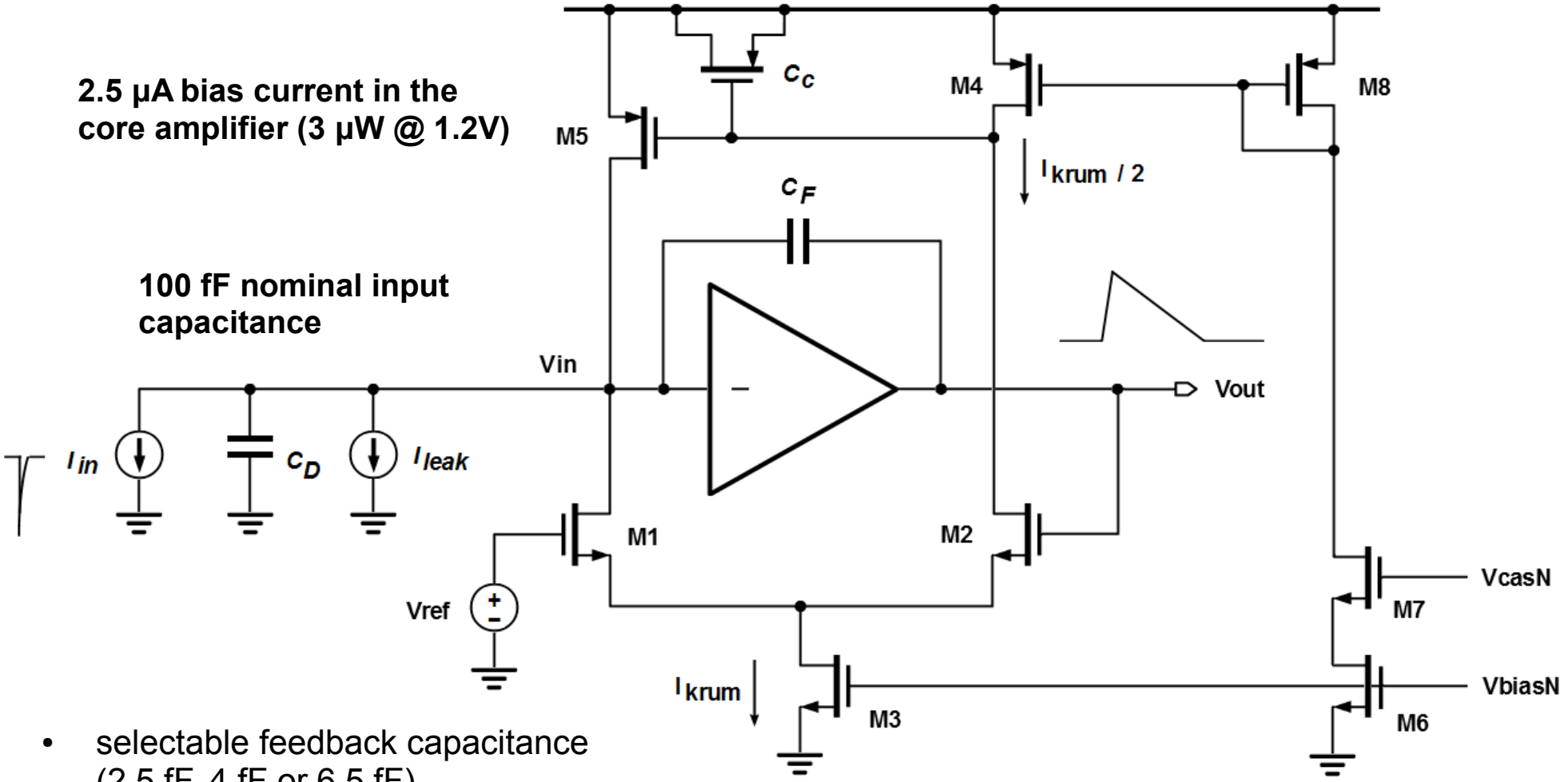
Triangular shaping with **constant current feedback** provides a linear relationship between TOT and input charge

- this remains true **also when the core amplifier saturates**
- well suited for **low-voltage headrooms**

Front-End amplifier/shaper

2.5 µA bias current in the core amplifier (3 µW @ 1.2V)

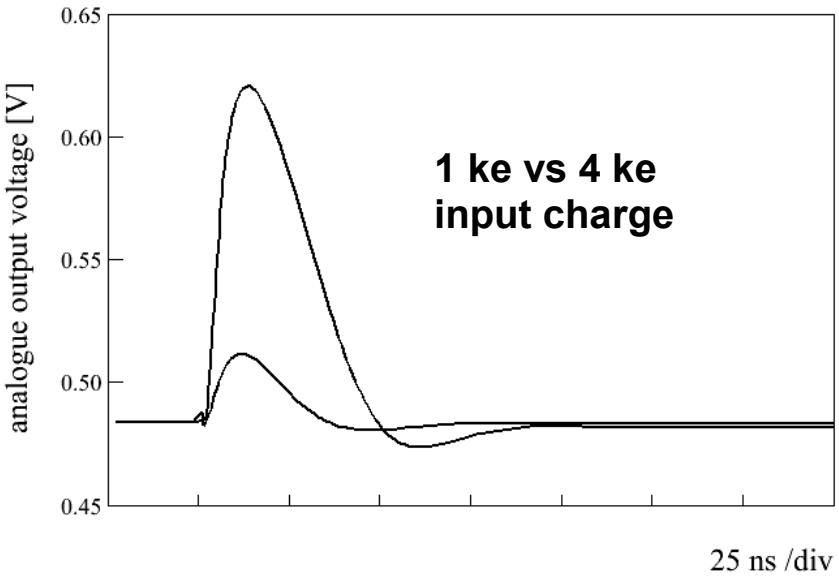
100 fF nominal input capacitance

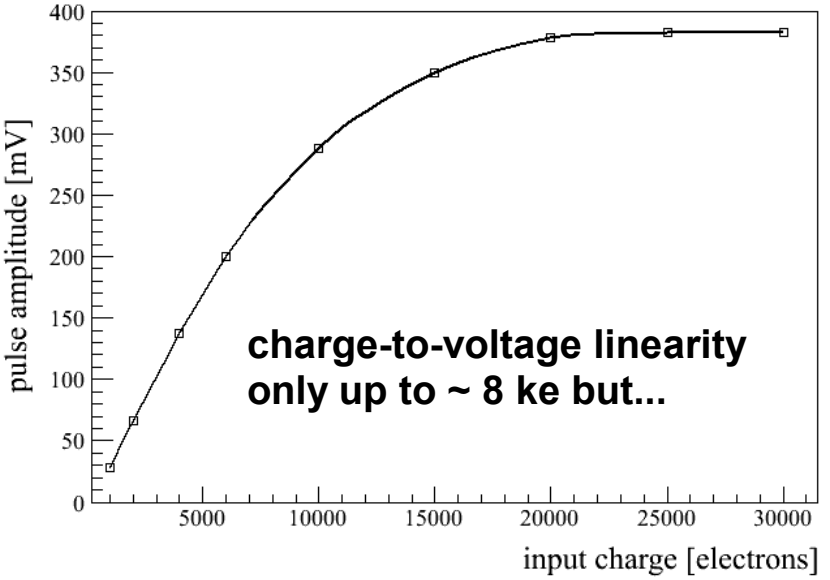


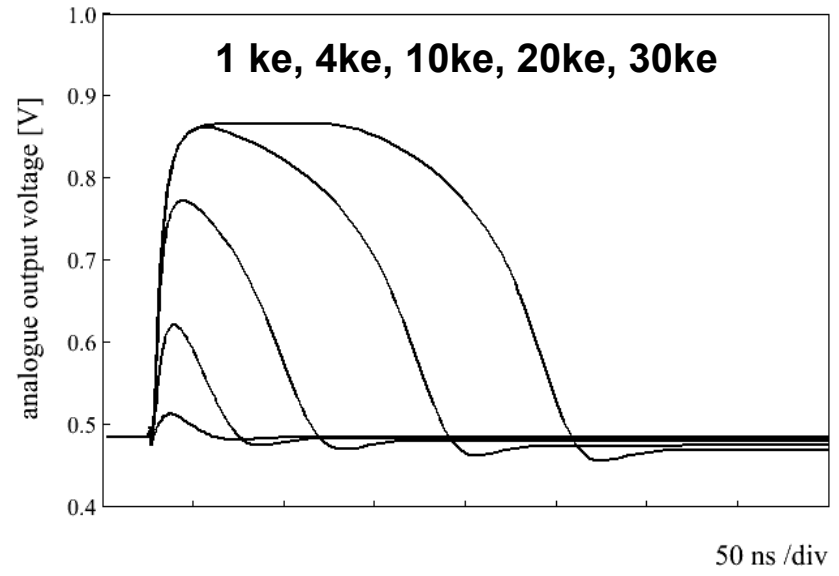
- selectable feedback capacitance (2.5 fF, 4 fF or 6.5 fF)
- 1 nA – 100 nA feedback current
- 12.5 ns nominal peaking time

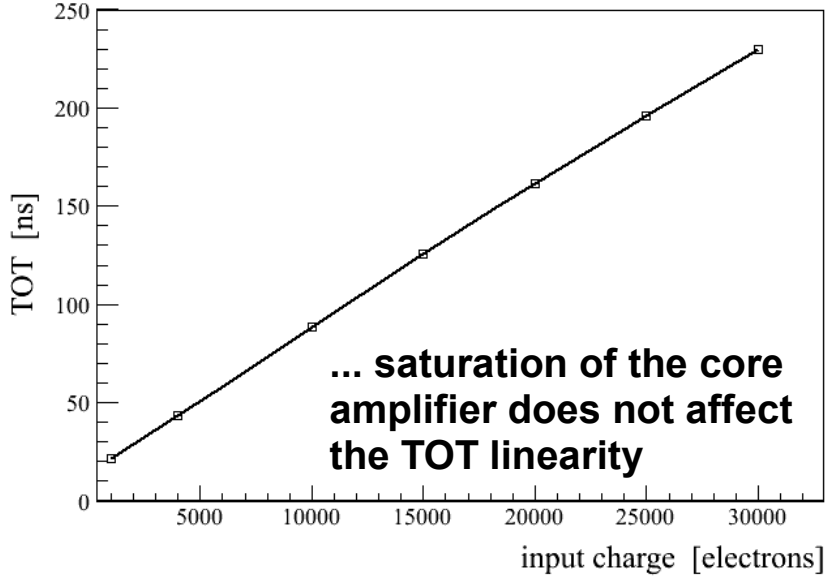
[F. Krummenacher, NIM A 1991]

Impulse response and linearity

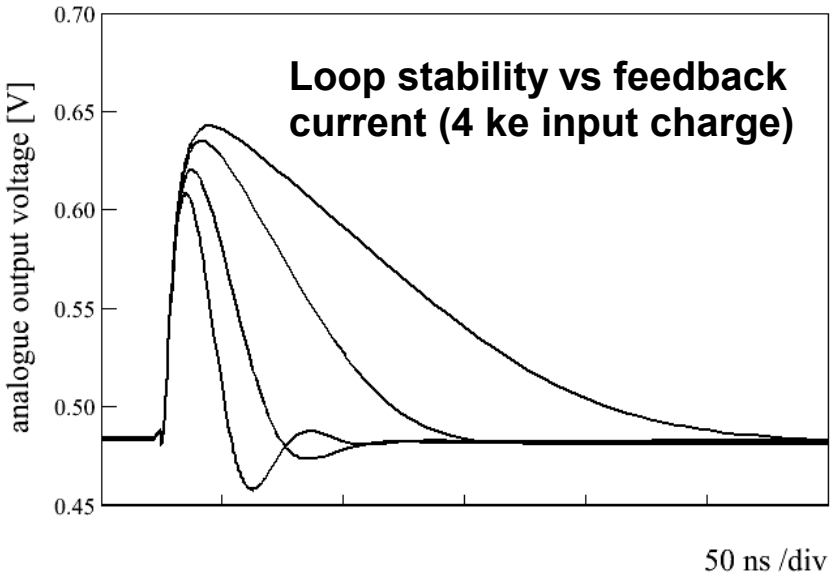


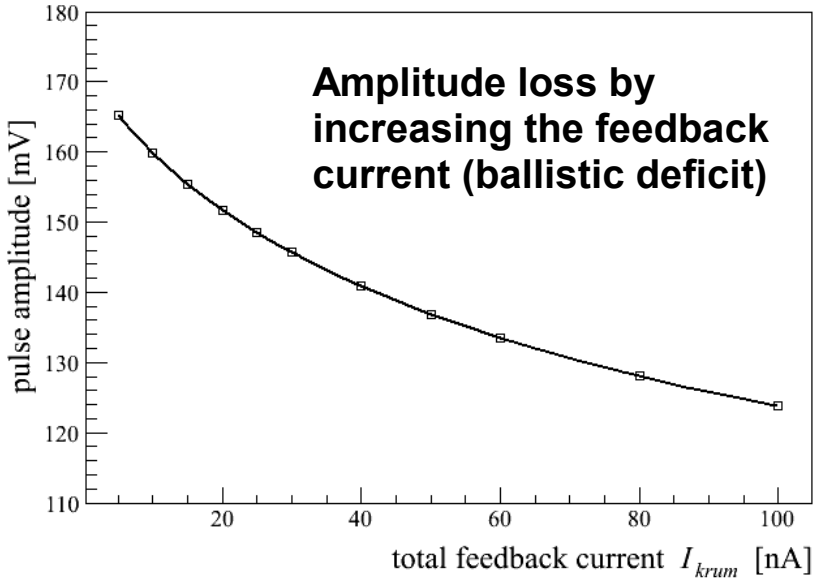


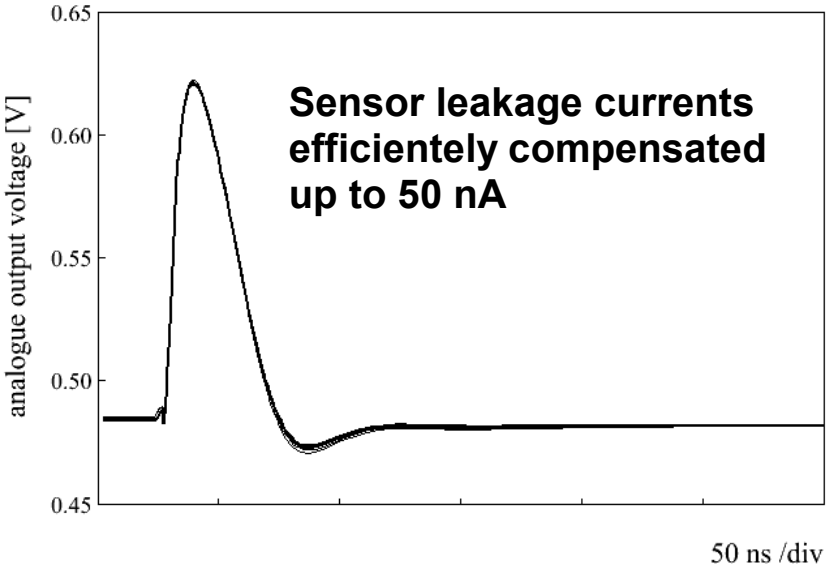


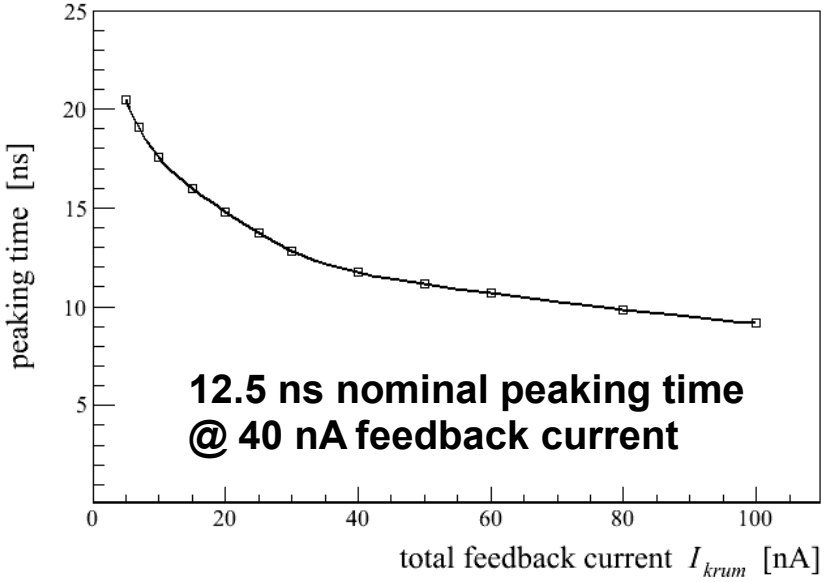


Closed-loop stability

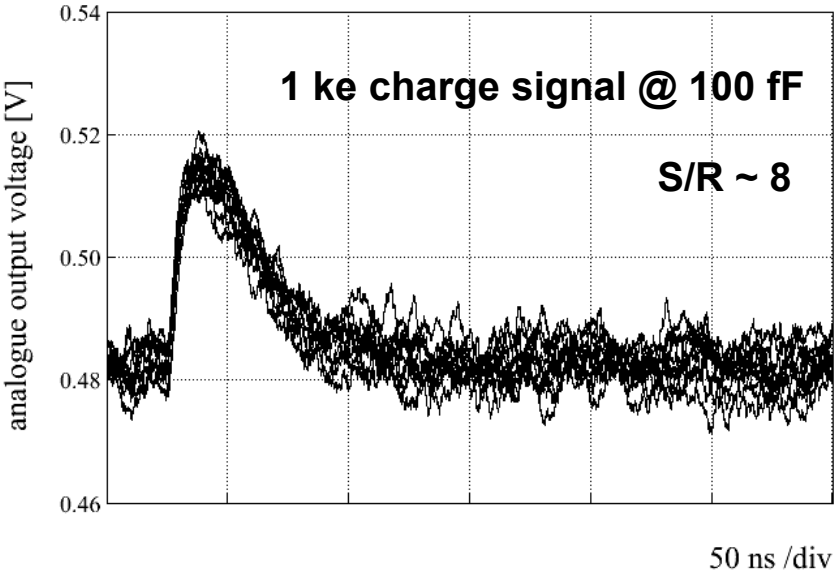


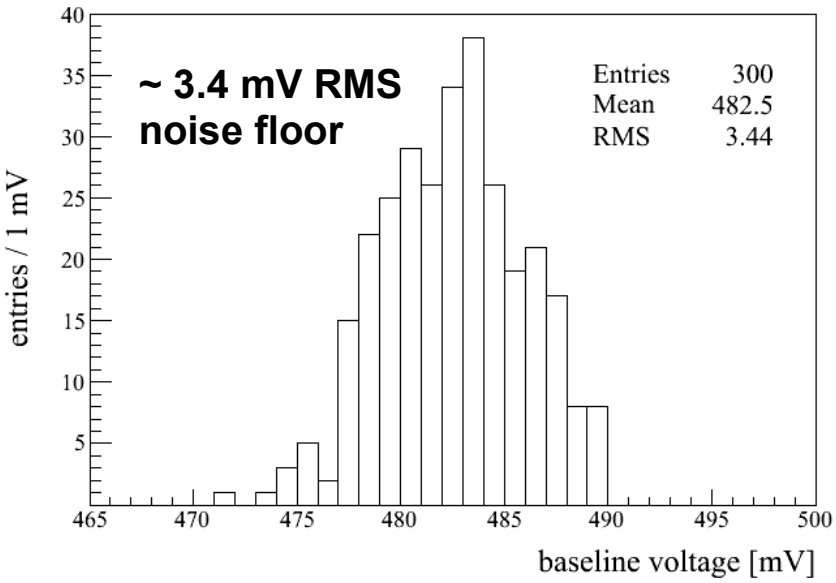


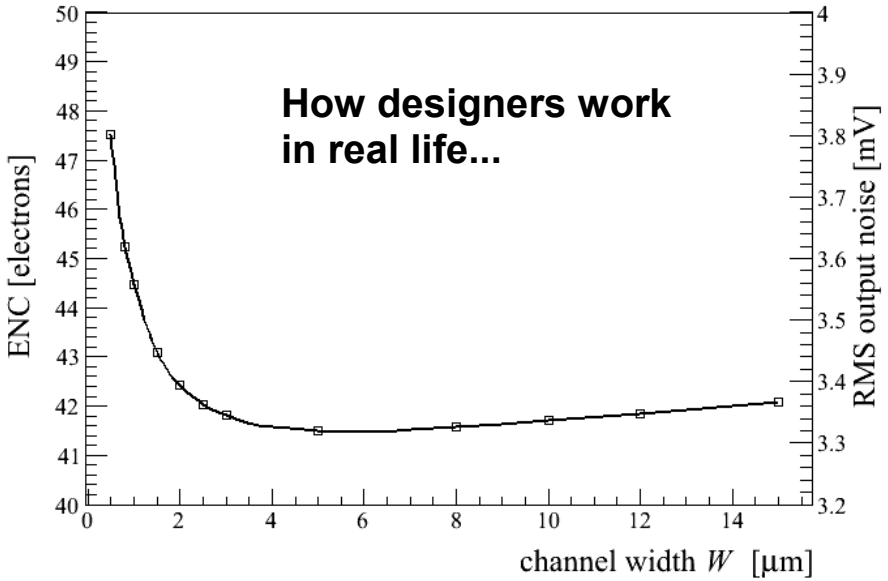


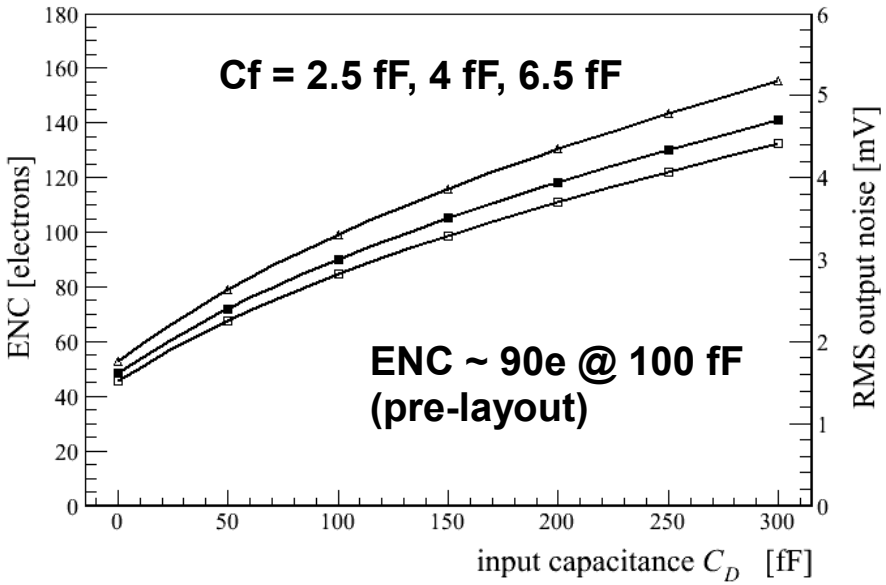


Minimum detectable charge and noise



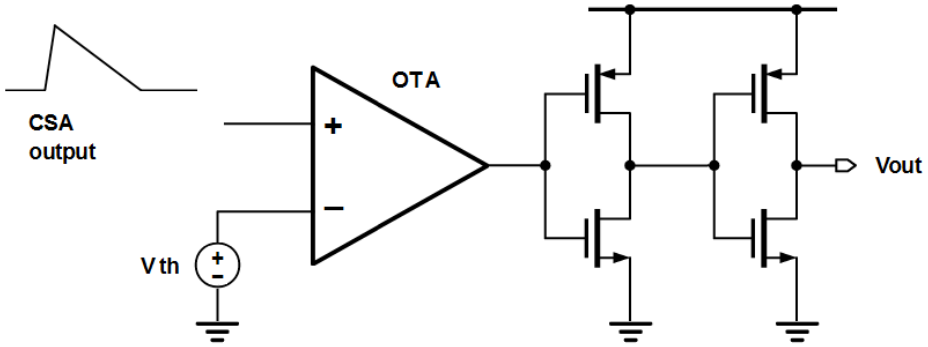




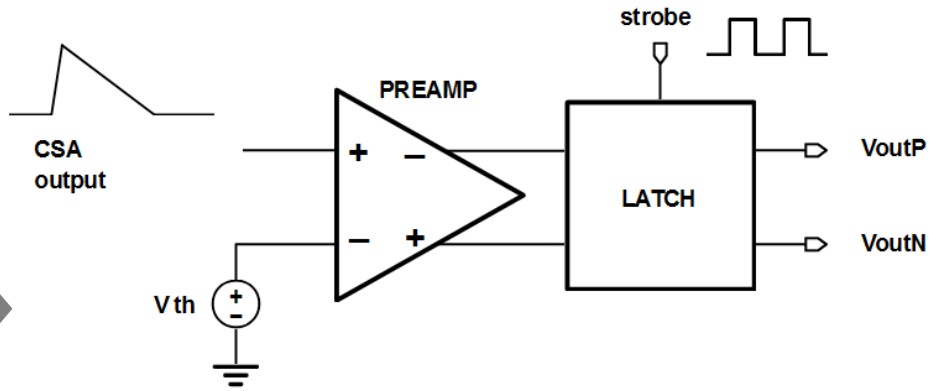


Analogue brainstorming

continuous-time comparator

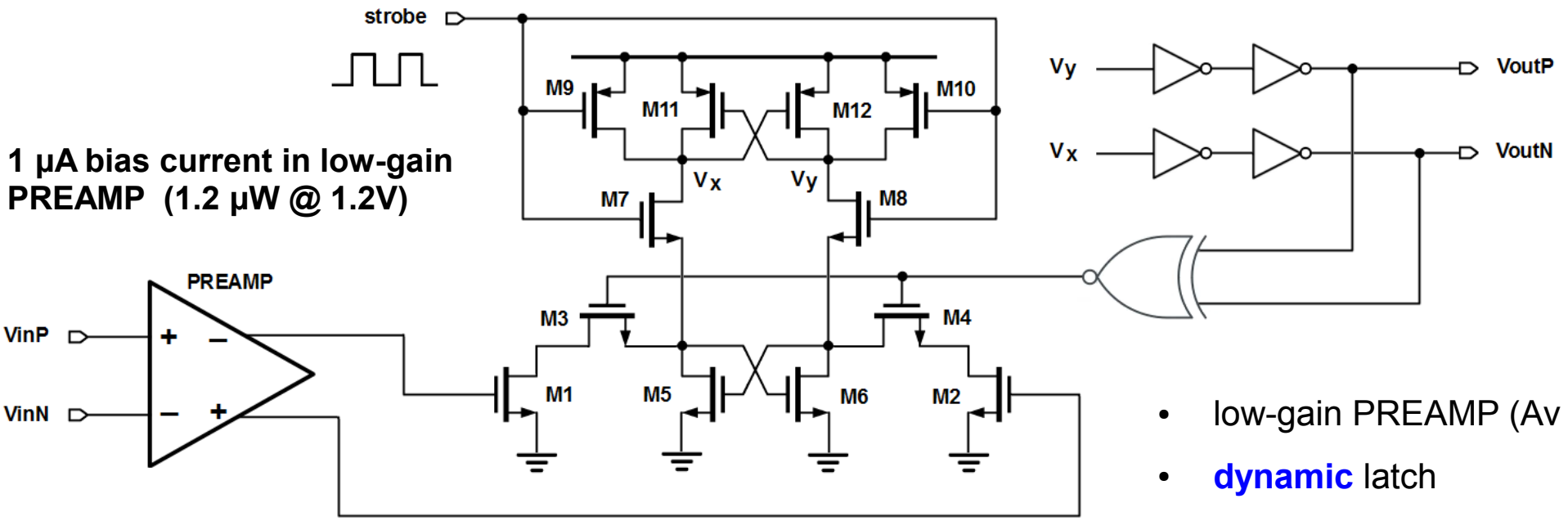


track-and-latch comparator



- try to explore **innovative solutions** for hit discrimination and charge encoding
- take advantage of the **speed** offered by a **65nm CMOS**
- what about a ***synchronous*** Front-End approach ?

Track.... and latch



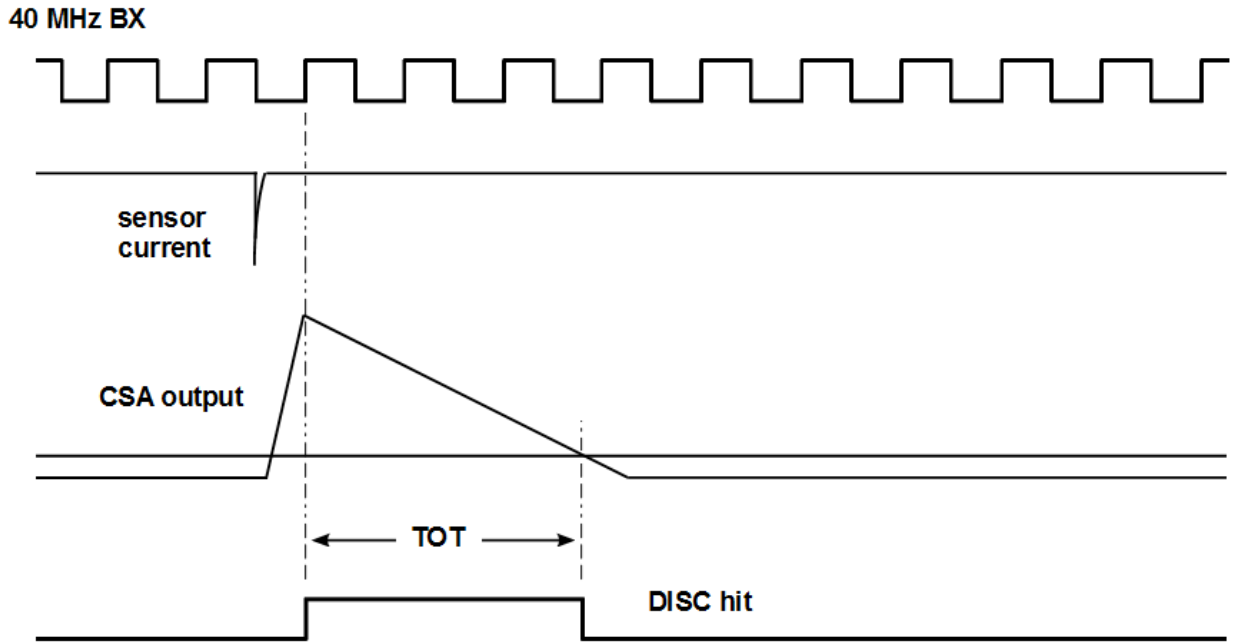
1 µA bias current in low-gain PREAMP (1.2 µW @ 1.2V)

- low-gain PREAMP (Av ~ 6)
- **dynamic** latch

The usage of a synchronous comparator introduces several advantages

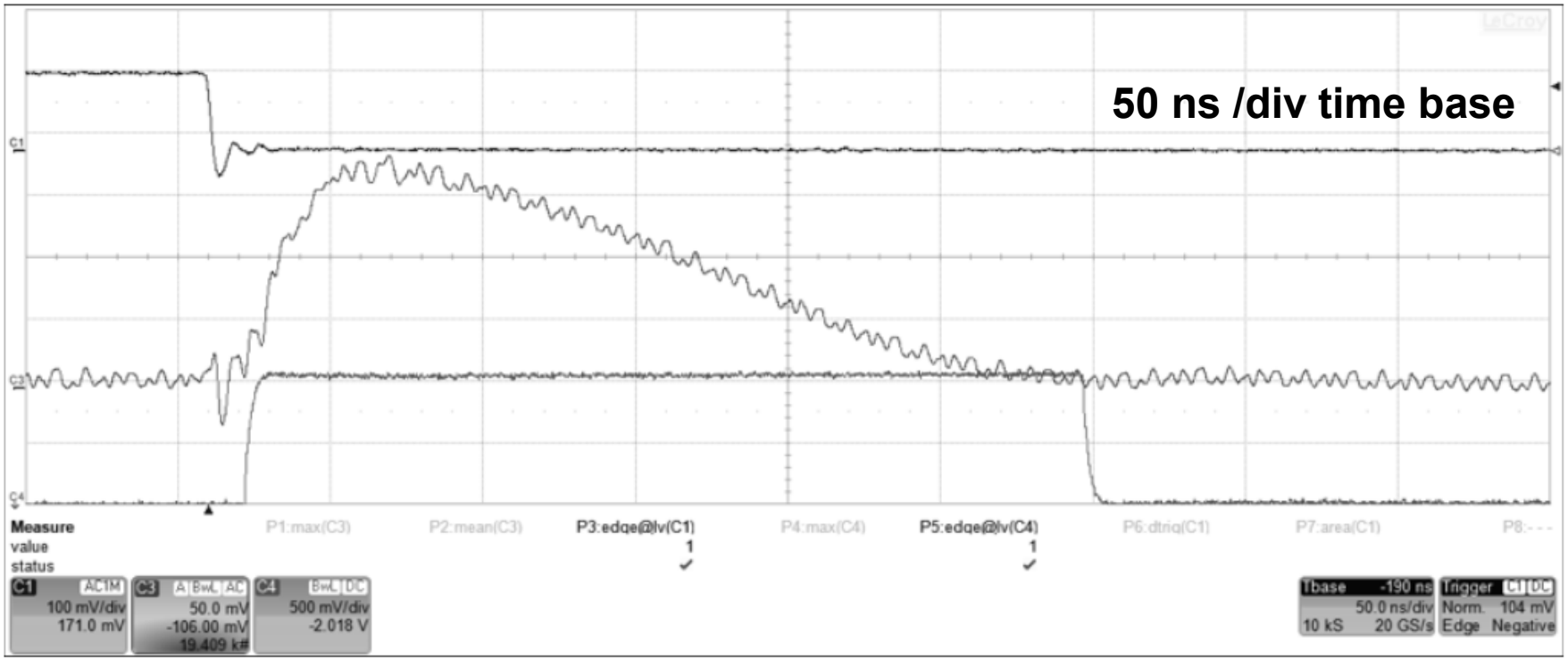
- better performance compared to OTA-based FE discriminators (speed, power, resolution)
- the hit generation is **synchronized** with a 40 MHz clock, avoiding time-walk issues in the time-stamp assignment
- can naturally include **autozeroing techniques** for the threshold adjustment
- CMOS latches can be easily turned into **local oscillators**

Synchronous FE operations



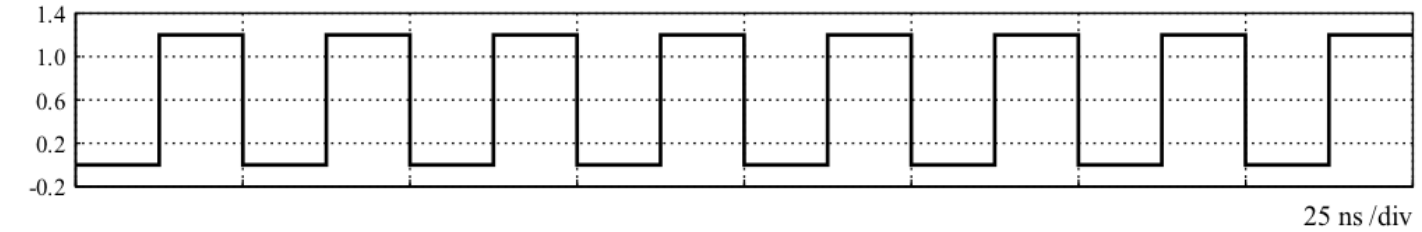
- at the LHC *pp* collisions occurs at each BX (nominal 40 MHz collision frequency)
- **positive feedback** enabled half-cycle after the BX
- FE amplifier designed with **nominal 12.5 ns peaking time**
- **peaking time variations** do not compromise synchronous operations, provided that a signal is found above the threshold at the **sampling time**

Appetizer....

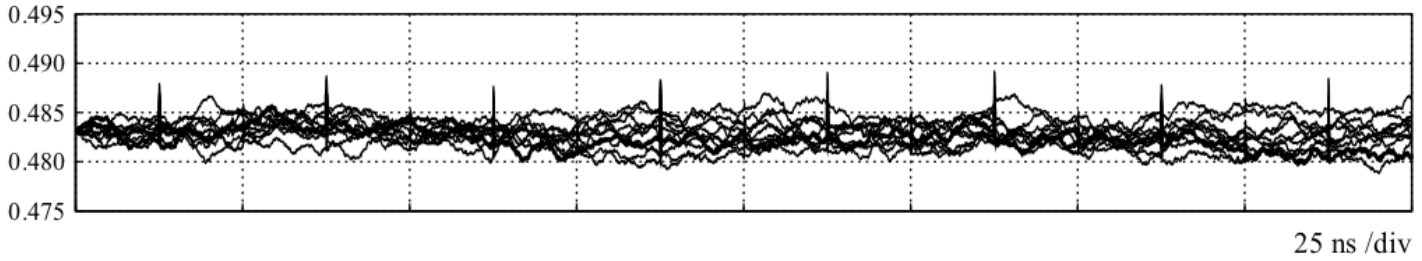


N.B. The duration of the hit pulse is an integer number of 25 ns clock cycles !

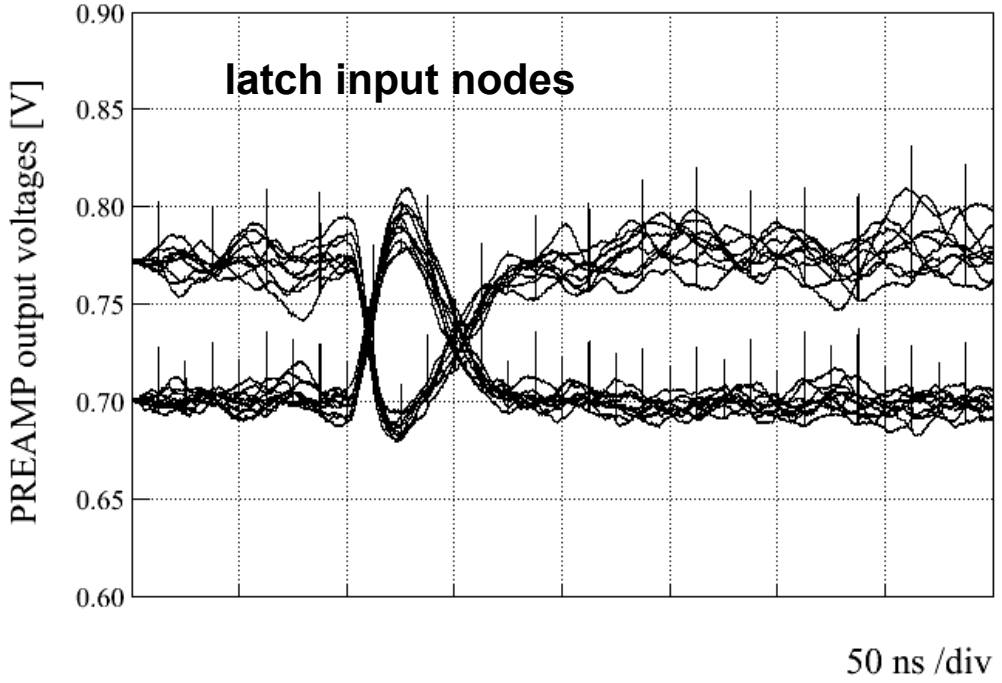
Digital-induced noise



40 MHz strobe



CSA baseline



Complete analogue chain simulation including strobe activity and transient noise (pre-layout)

HEP vs industry (revised)

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A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure

Chun-Cheng Liu, *Student Member, IEEE*, Soon-Jyh Chang, *Member, IEEE*,
Guan-Ying Huang, *Student Member, IEEE*, and Ying-Zu Lin, *Student Member, IEEE*

***Abstract*—This paper presents a low-power 10-bit 50-MS**
cessive approximation register (SAR) analog-to-digital con
(ADC) that uses a monotonic capacitor switching proc

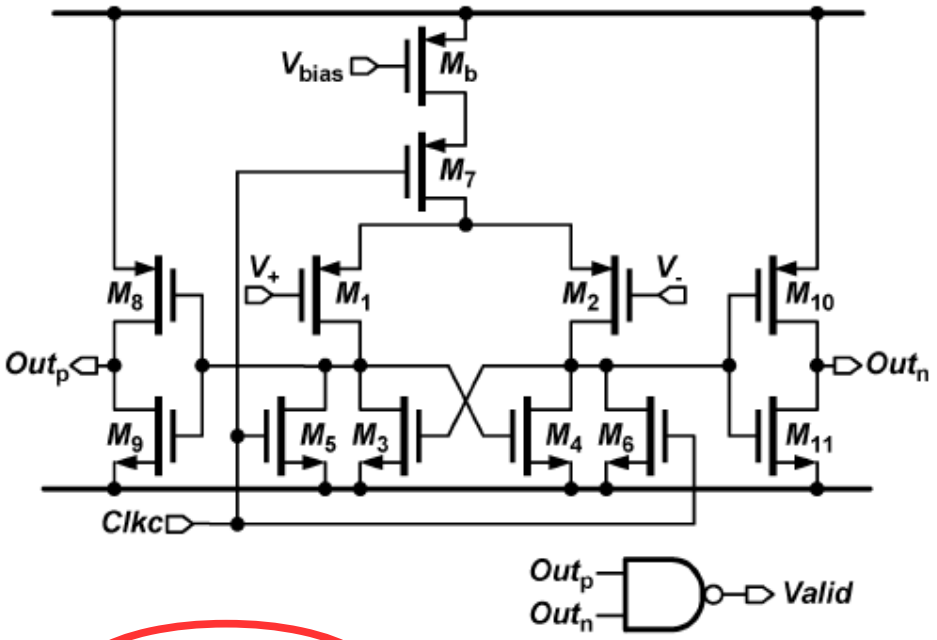


Fig. 8. Dynamic comparator with a current source.

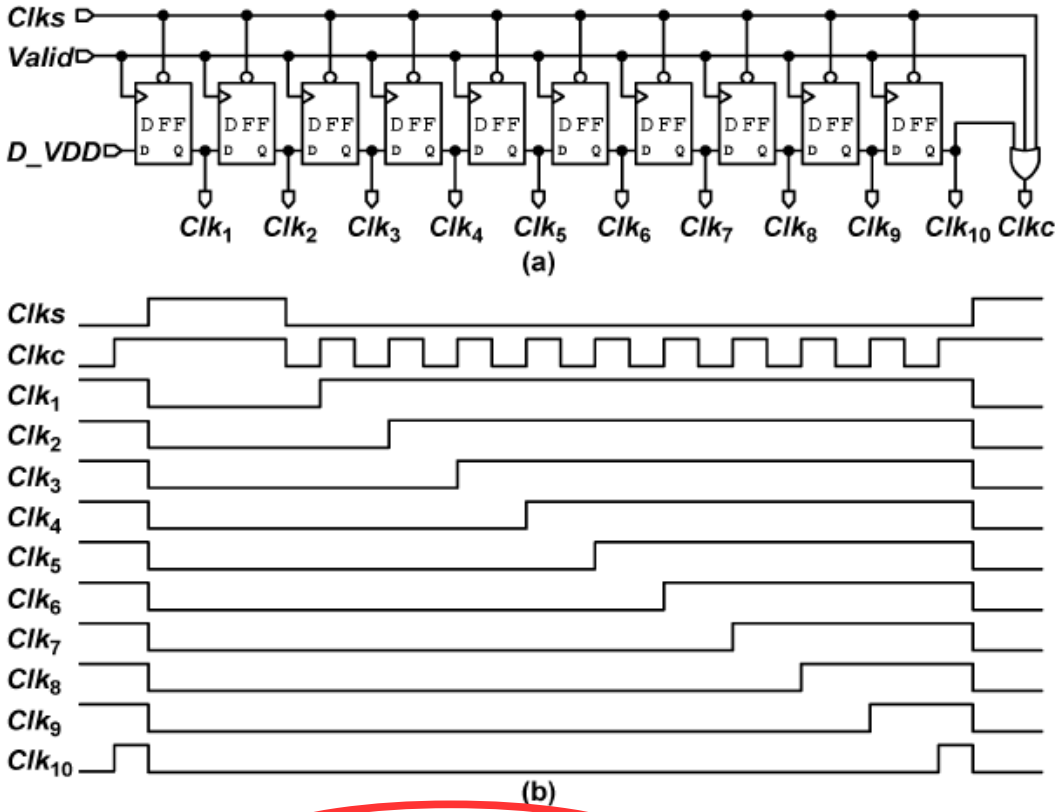
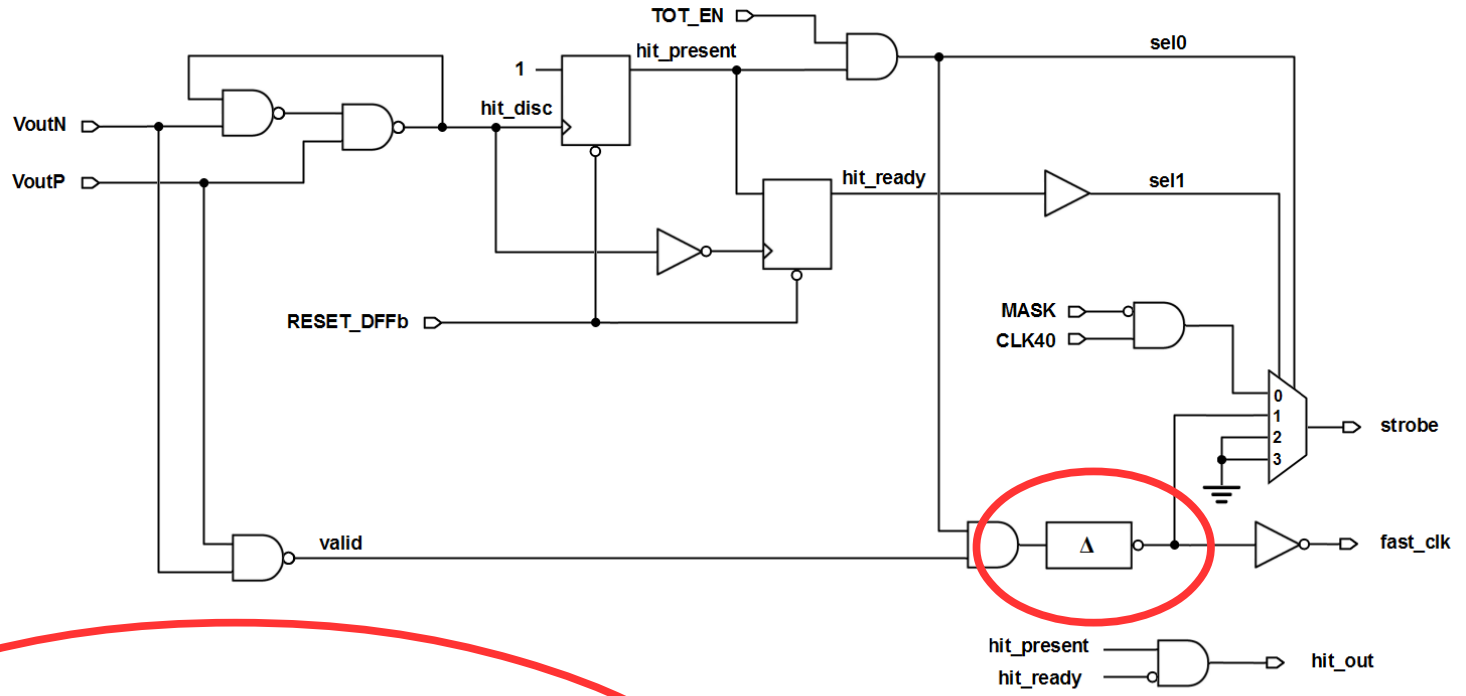
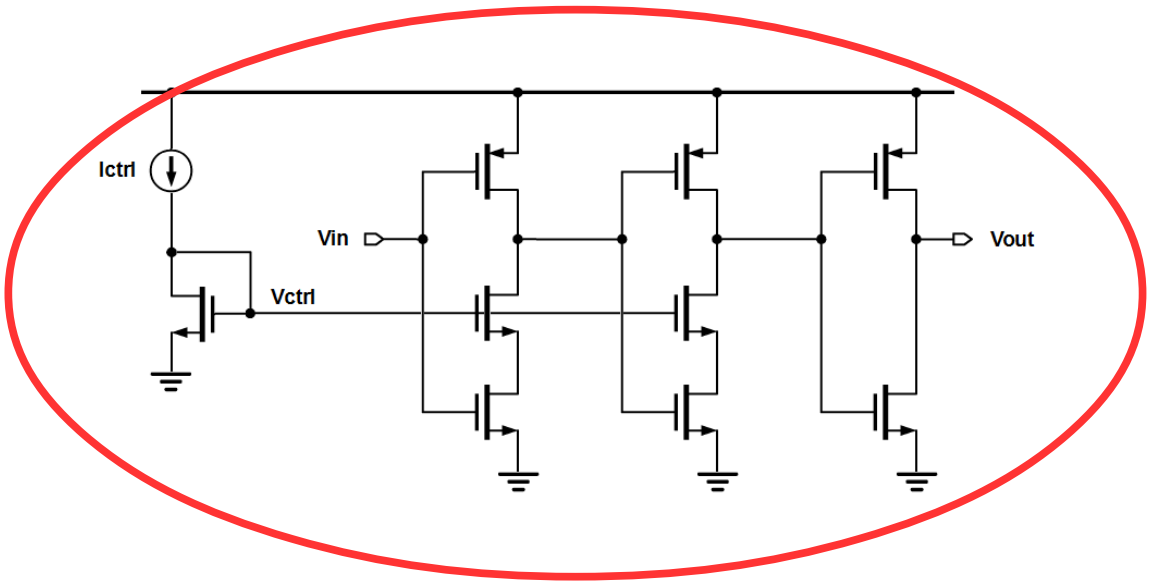


Fig. 9. Asynchronous control logic: (a) Schematic. (b) Timing diagram.

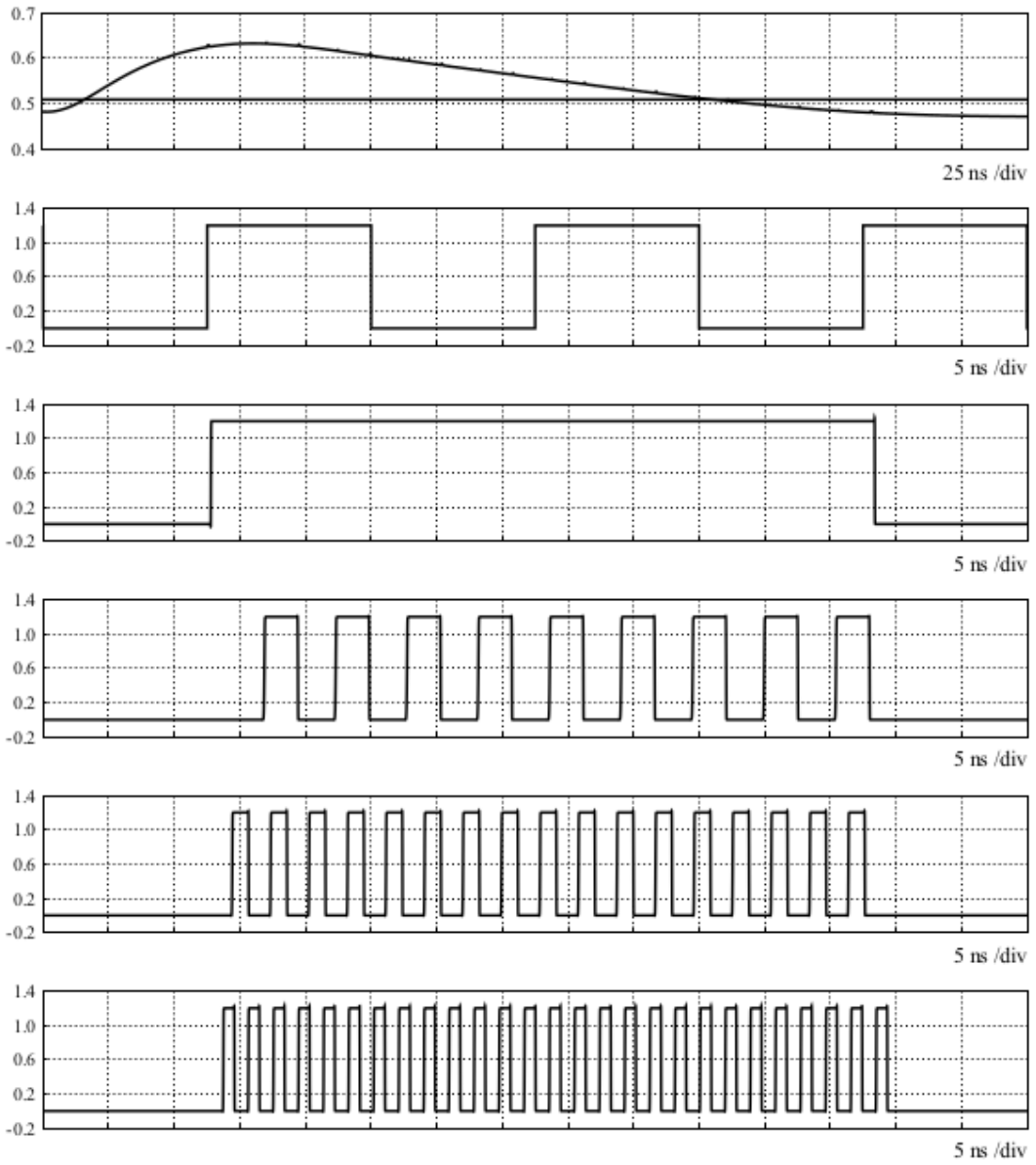
Hit (asynchronous) logic





- CMOS latches can be turned into oscillators by means of **asynchronous logic**
- insert a **variable-delay element** in the feedback loop to tune the frequency of the oscillation

TOT counting with self-generated clock



CSA output

40 MHz master clock

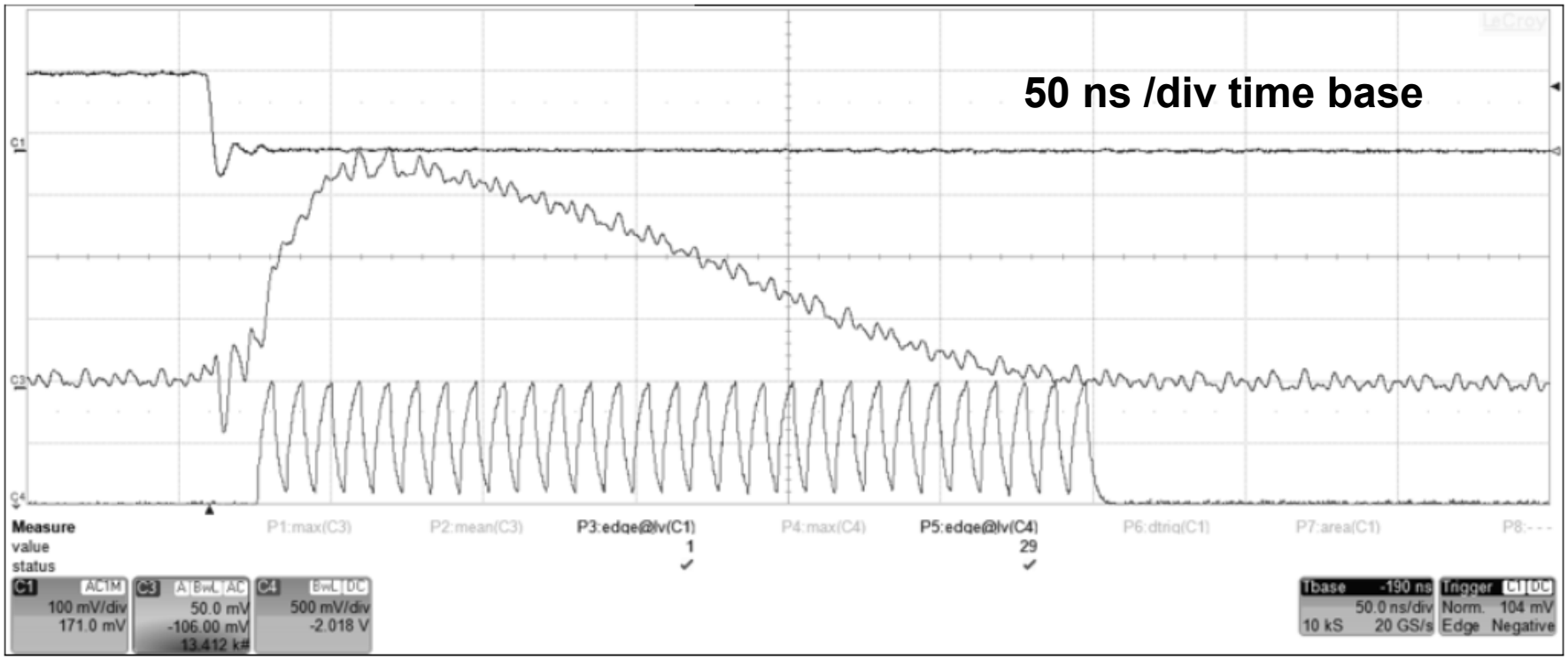
Hit pulse

200 MHz @ 50 nA

600 MHz @ 150 nA

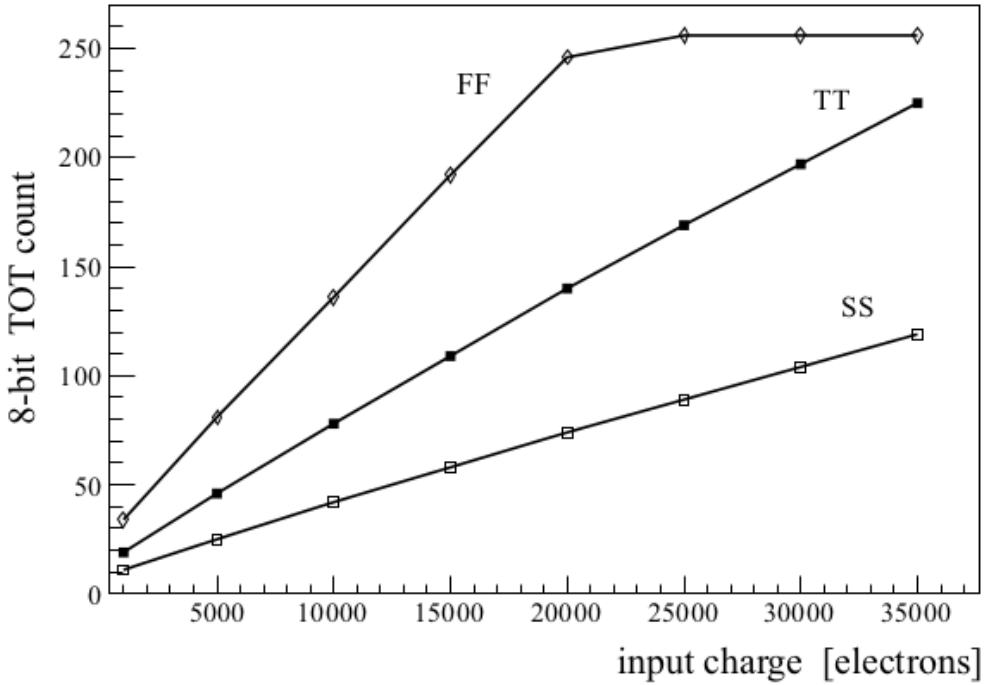
800 MHz @ 300 nA

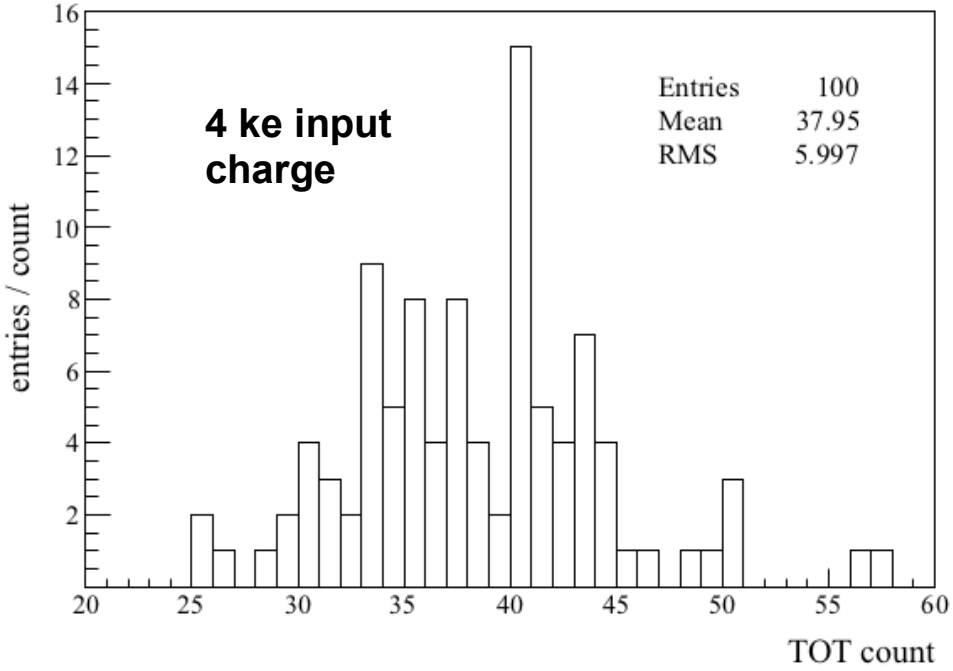
More than an appetizer...



- electrical functionality OK !
- self-generated ~100 MHz clock for TOT encoding

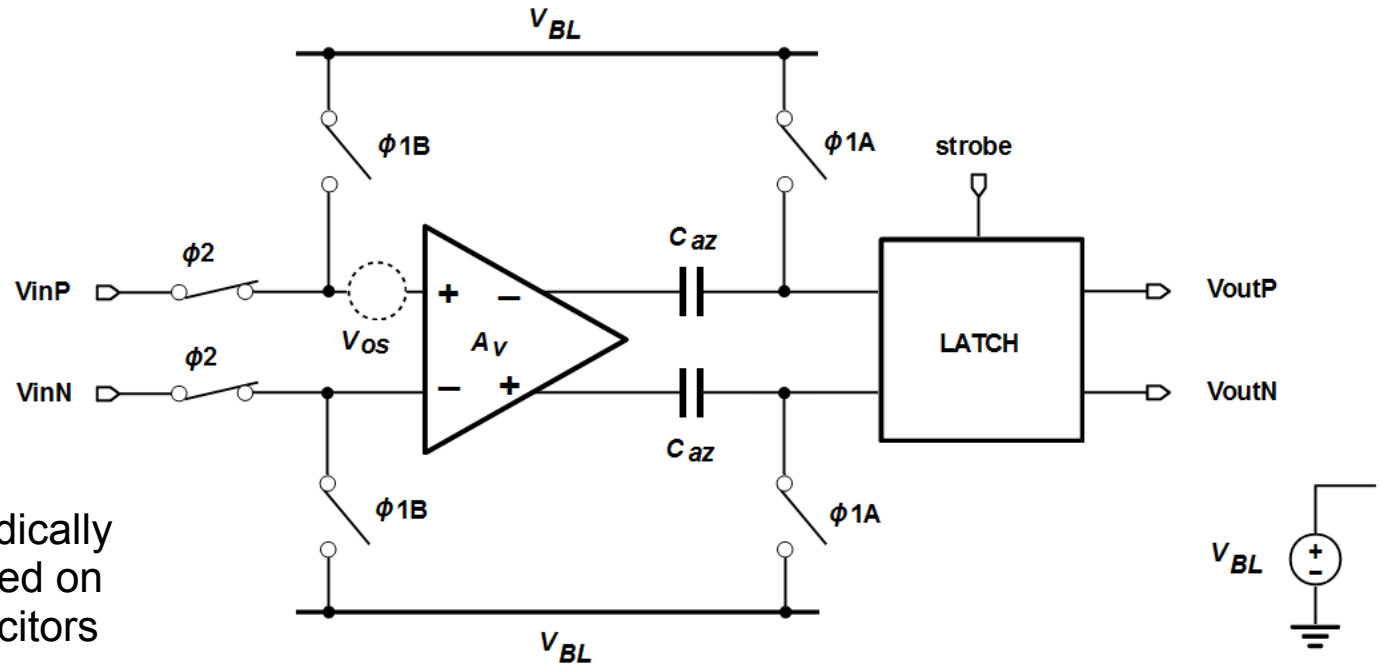
TOT digitization



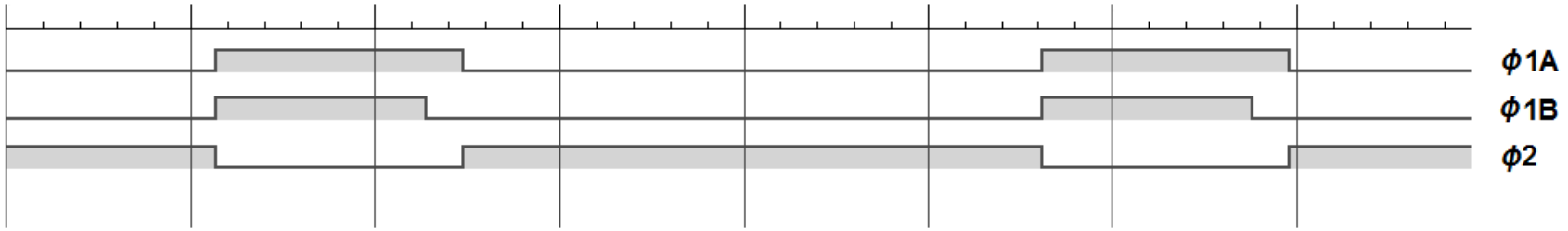


- 8-bit TOT encoding up to 3.5 ke with ~ 650 MHz self-generated clock can be retrieved in less than 350 ns ! (~300 ns signal duration for 3.5 ke input charge)
- PVT variations can be always compensated with PLL techniques
- pixel-to-pixel variations in the number of TOT counts due to mismatches ~15% RMS

Autozeroing /1



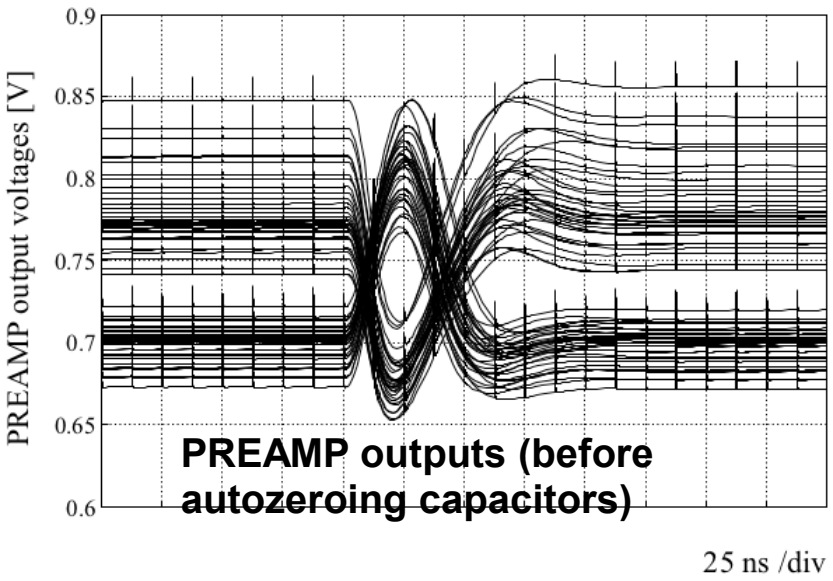
the offset is periodically sampled and stored on autozeroing capacitors



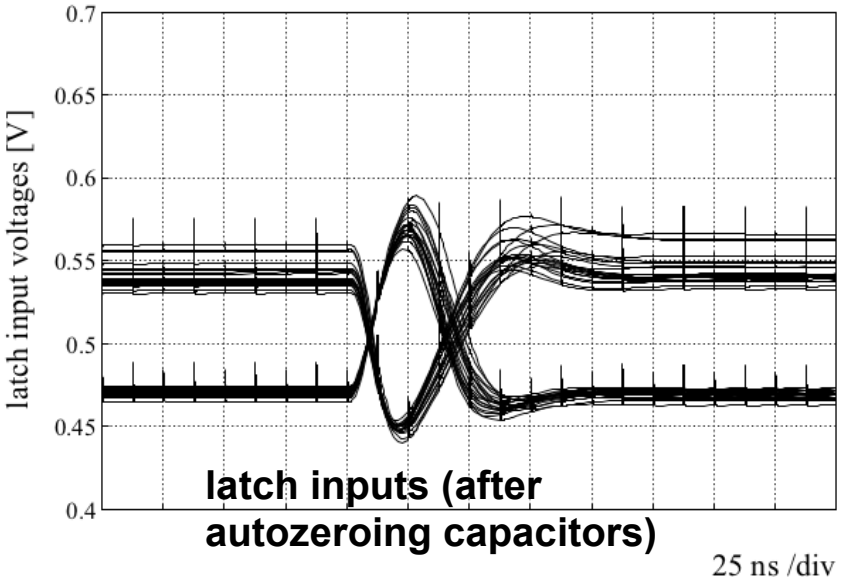
Pixel-to-pixel threshold variations compensated by means of **Output Offset Storage**

- the **absence of a local DAC** avoids the need of SEU tolerant registers in the digital part (hence well suitable in a harsh radiation environment !)

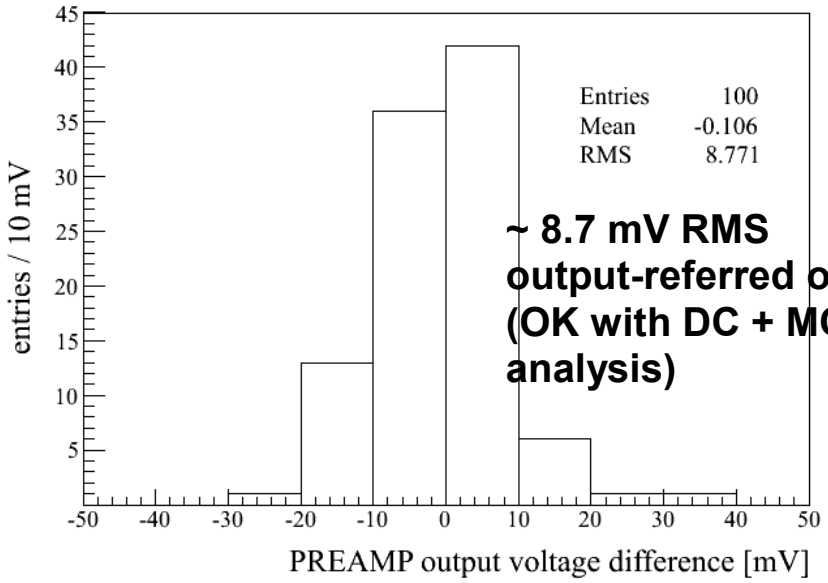
Autozeroing /2



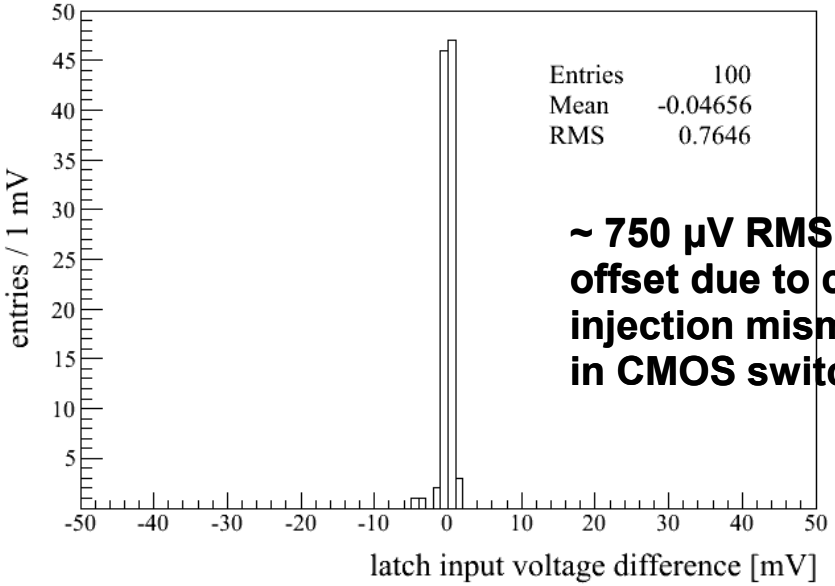
PREAMP outputs (before autozeroing capacitors)



latch inputs (after autozeroing capacitors)



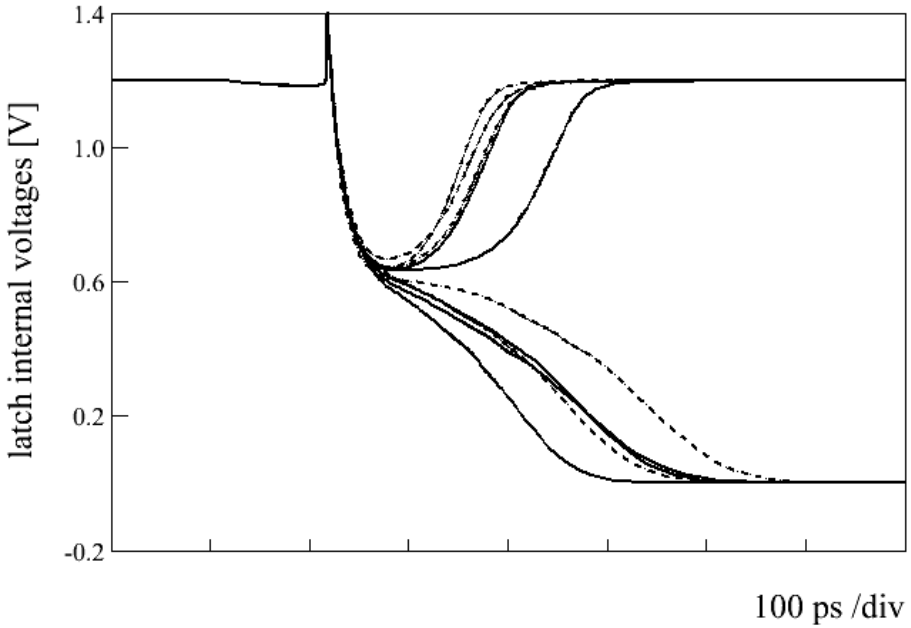
~ 8.7 mV RMS output-referred offset (OK with DC + MC analysis)

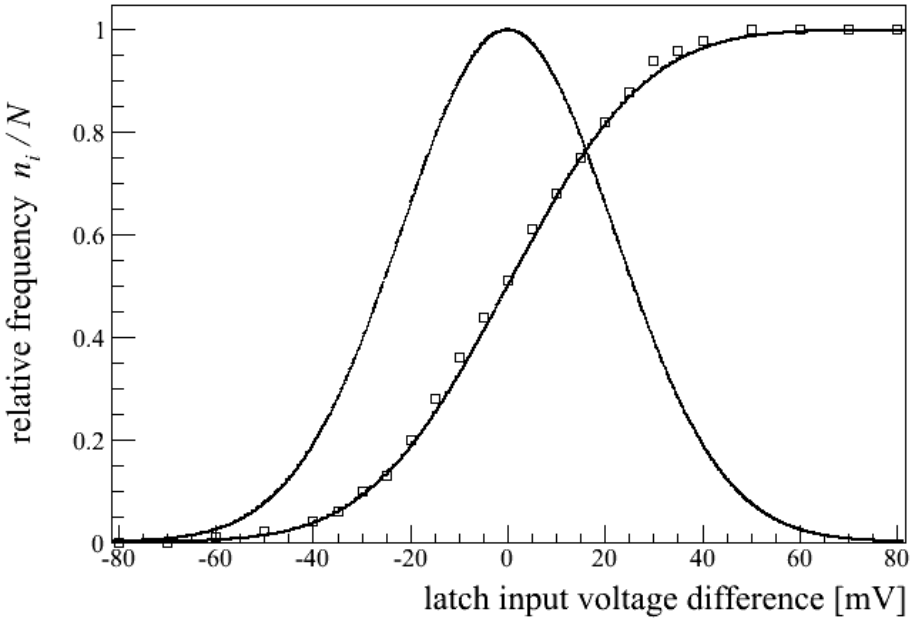


~ 750 µV RMS residual offset due to charge injection mismatches in CMOS switches

Latch dynamic offset

~ 22 mV RMS latch dynamic offset
(~ 75 e RMS @ 4 fF feedback capacitance)

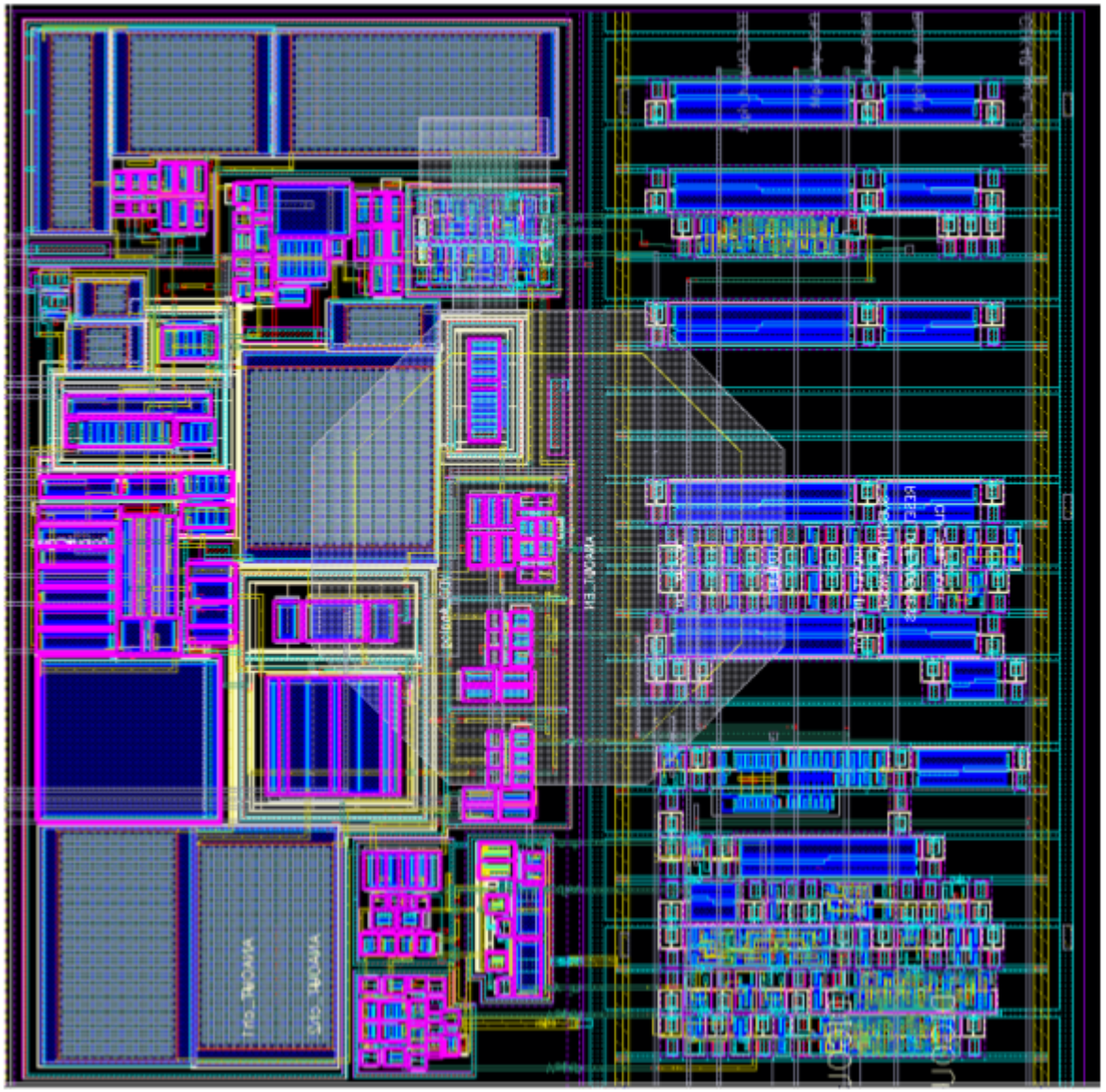




The dominant contribution in the residual offset is due to uncompensated **latch dynamic offset**

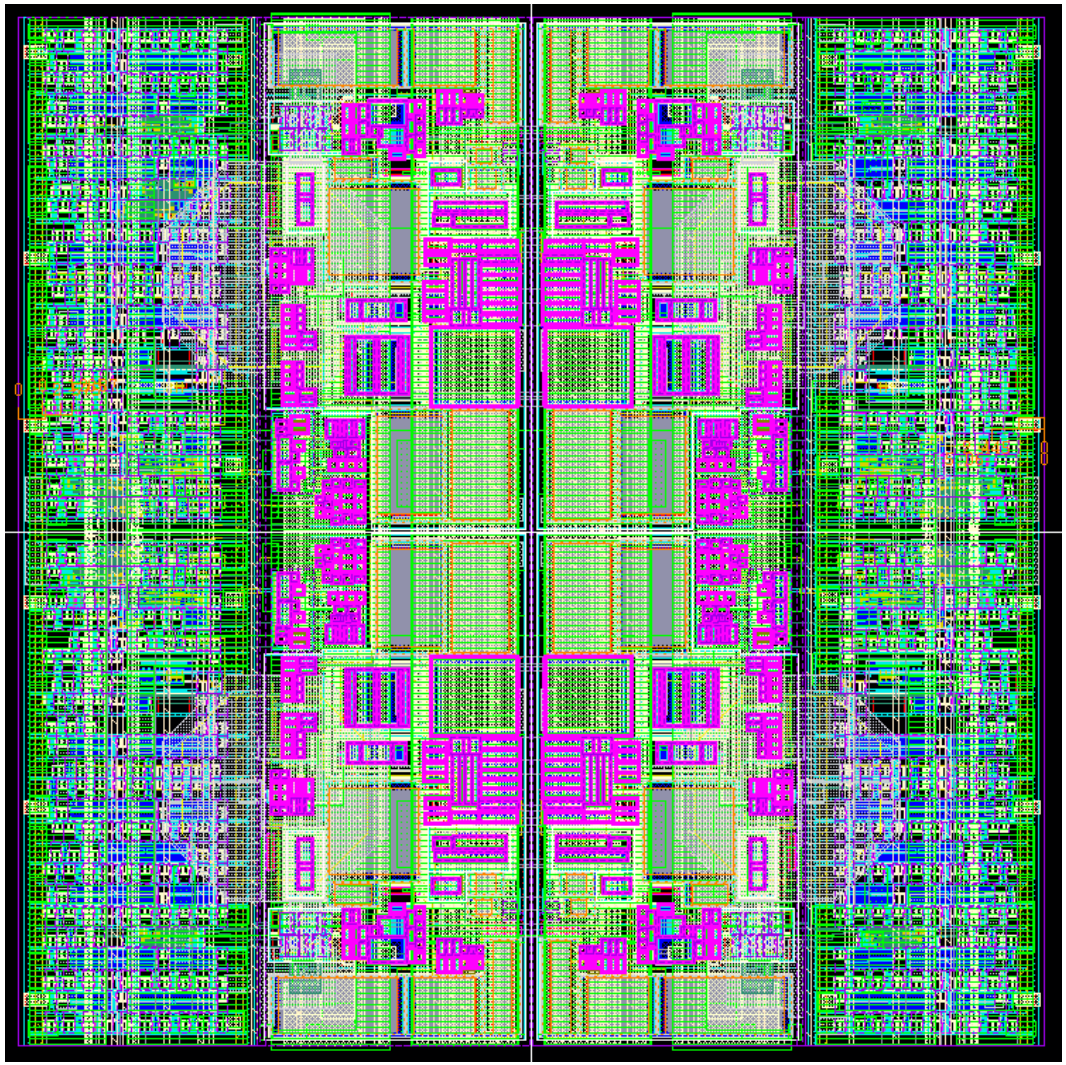
- its contribution can be evaluated only from positive feedback transients !
- register the relative number of latch outputs across transient MC simulations for different input voltages
- fit simulated points with an effor function

Pixel Unit Cell (PUC) layout



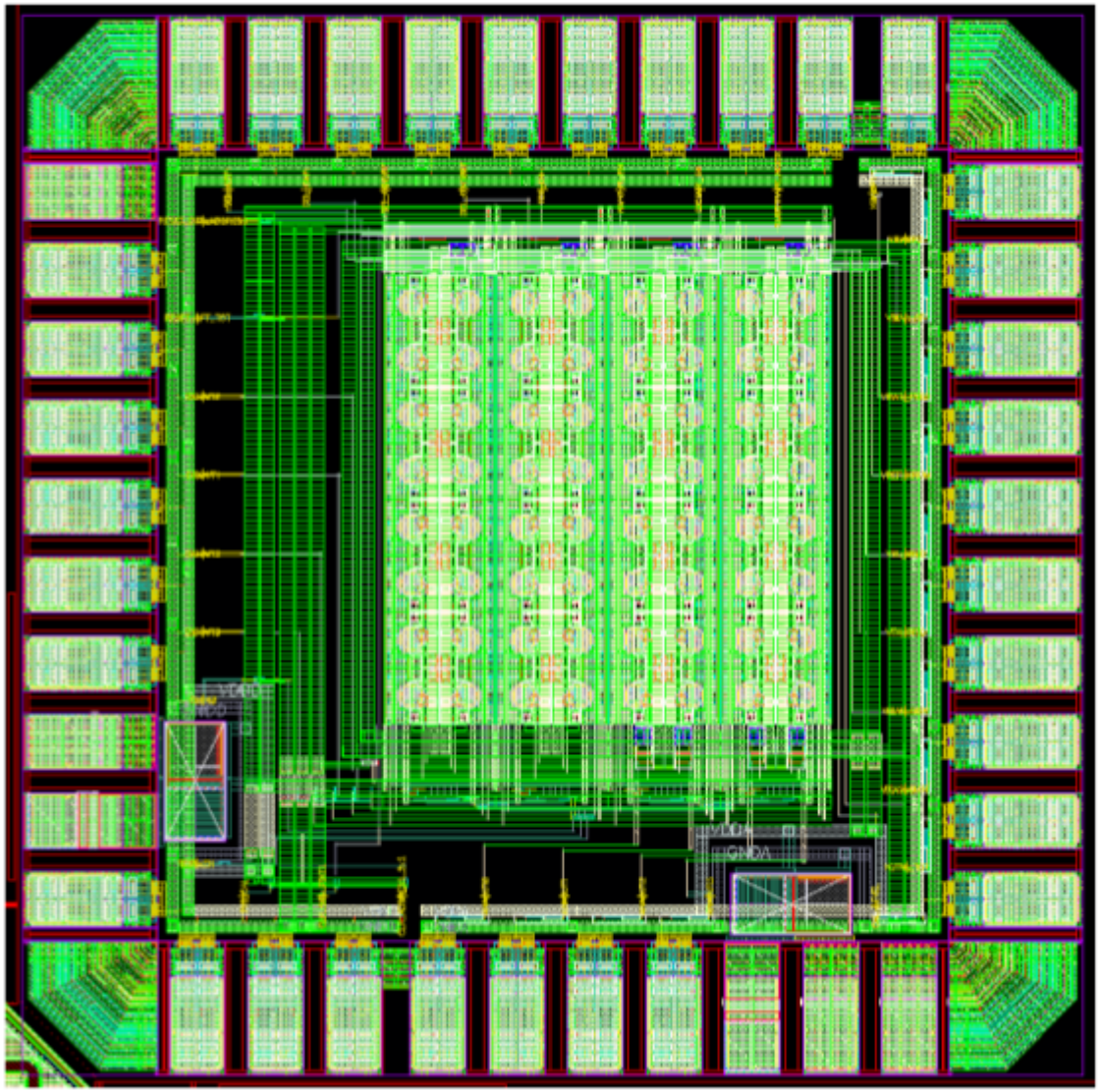
- 50 µm x 50 µm (A+D)
- ~26 µm x 50 µm A
- bump-bonding pad included
- selectable 2 GHz ring oscillator for noise studies
- most of the area is occupied by MOM capacitors
- significant reduction in the analogue area if MIM cap are use (but larger mask cost)
- full-custom STD cells !!! (all logic gates designed from scratch...)

2x2 Pixel region



- 100 µm x 100 µm
- left-right + upside-down symmetry
- ' *analogue island* '
- empty STD cell rows filled with DECAPs, dummies, buffers and pixel addressing logic

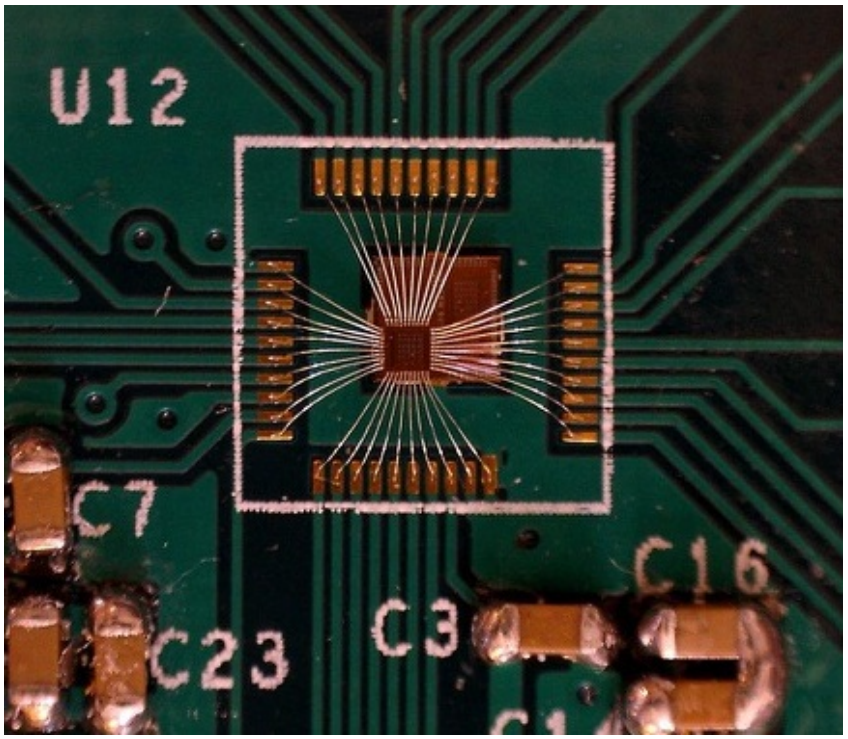
CHIPIX_VFE1/TO



- 945 µm x 945 µm
- 8 x 8 pixels cells with synchronous FE
- 16 pixel regions
- **full-analogue readout** of all 64 pixels, 4 outputs for each selectable pixel region (CSA output + hit or fast clock)
- validation of synchronous FE performance at the oscilloscope
- **100% CMS Torino !**
- part of a larger silicon die hosting two additional chips

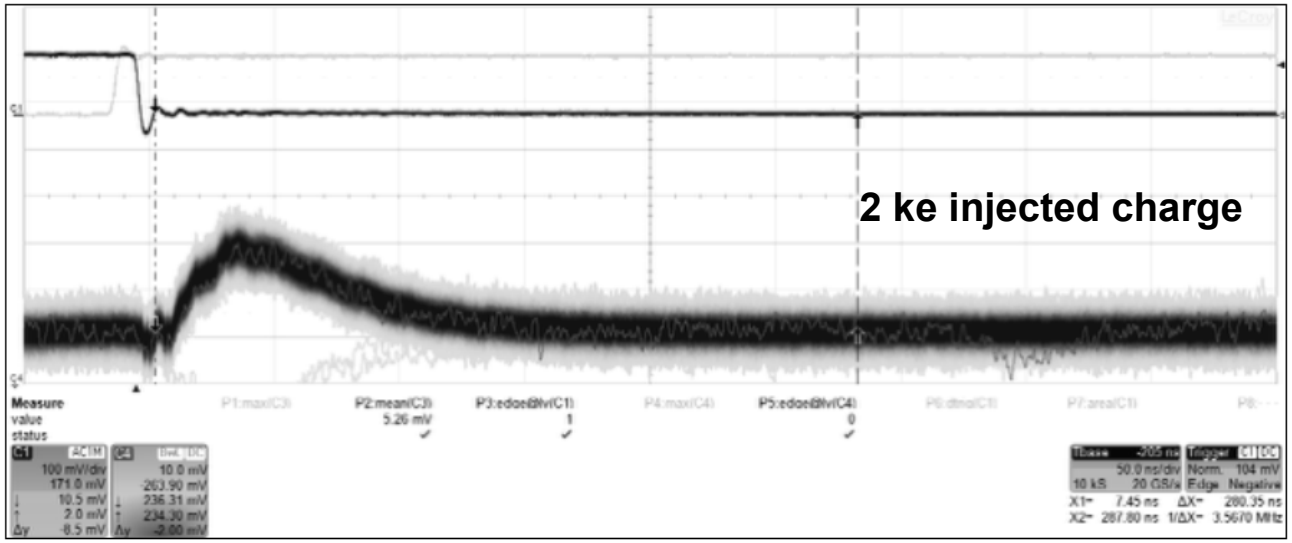
Experimental setup and measurements

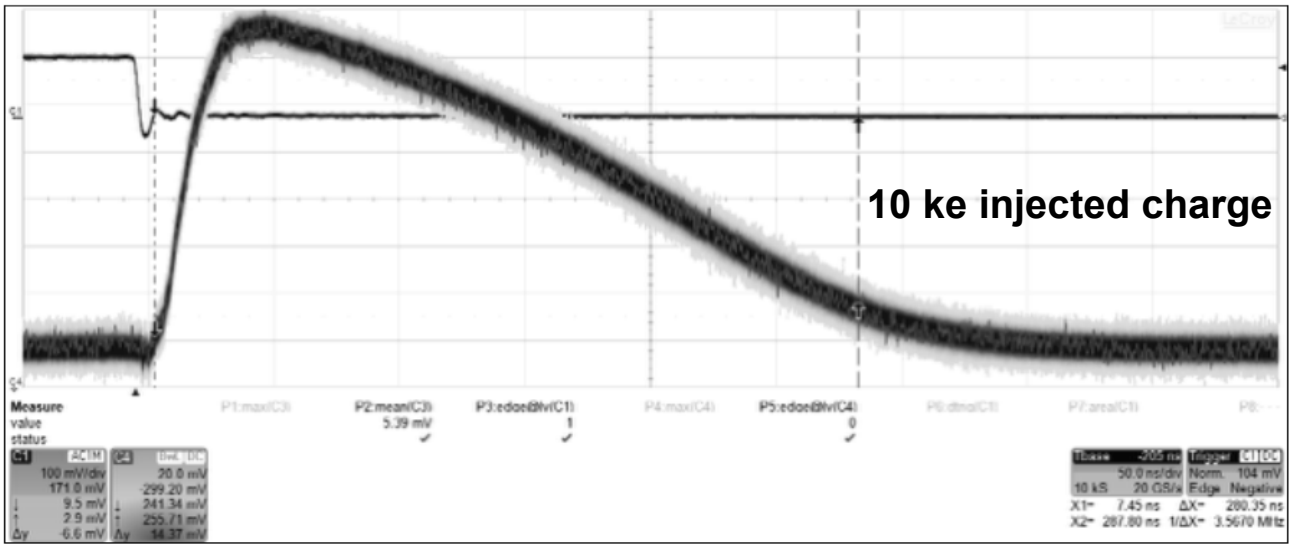
Experimental setup in Torino



- CHIPIX_VFE1/TO wire-bonded on a custom test board
- all digital signals are provided by a LSA/test pattern generator
- full-analogue characterizations at the oscilloscope with active probes

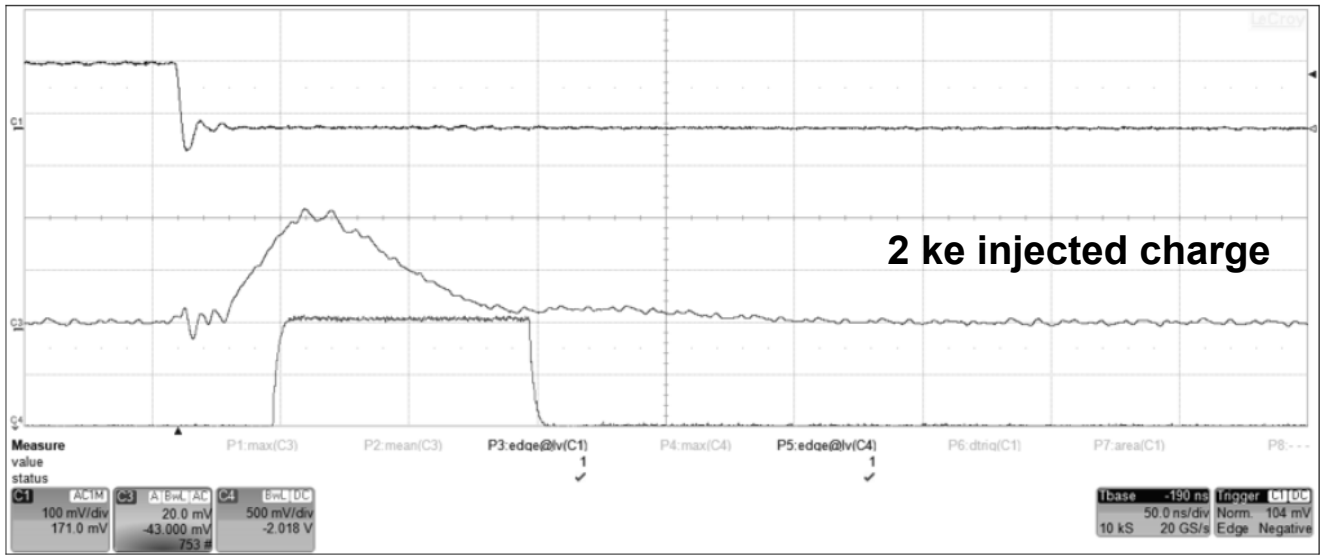
Basic electrical functionality /1

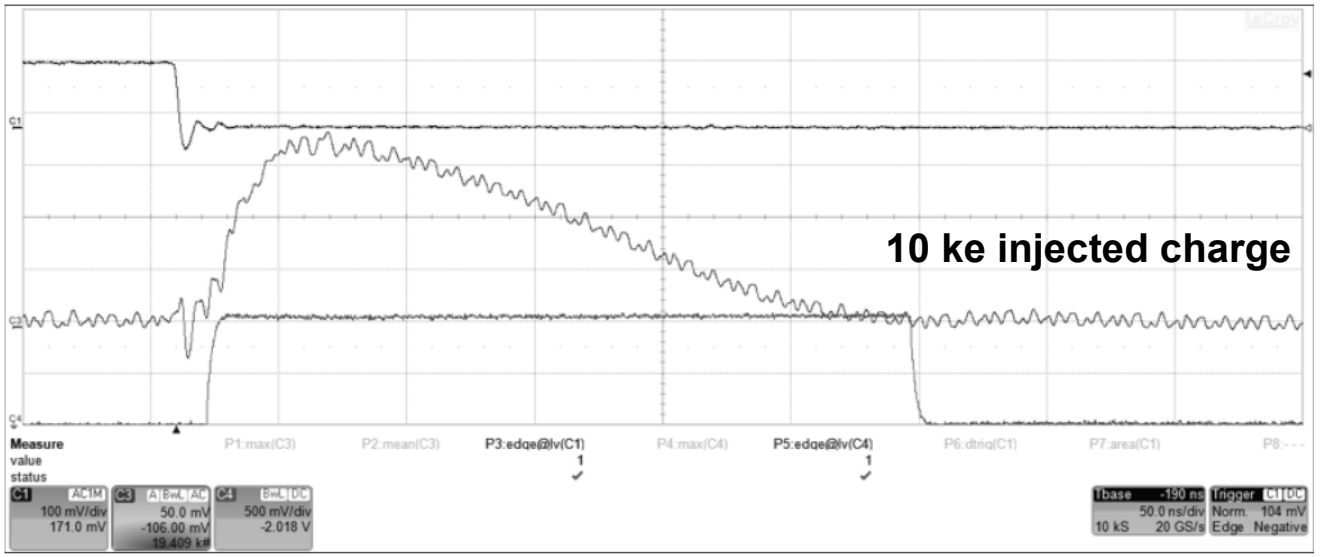




- 100 fF input capacitance
- 10 nA feedback current
- NO 40 MHz clock distributed to pixels

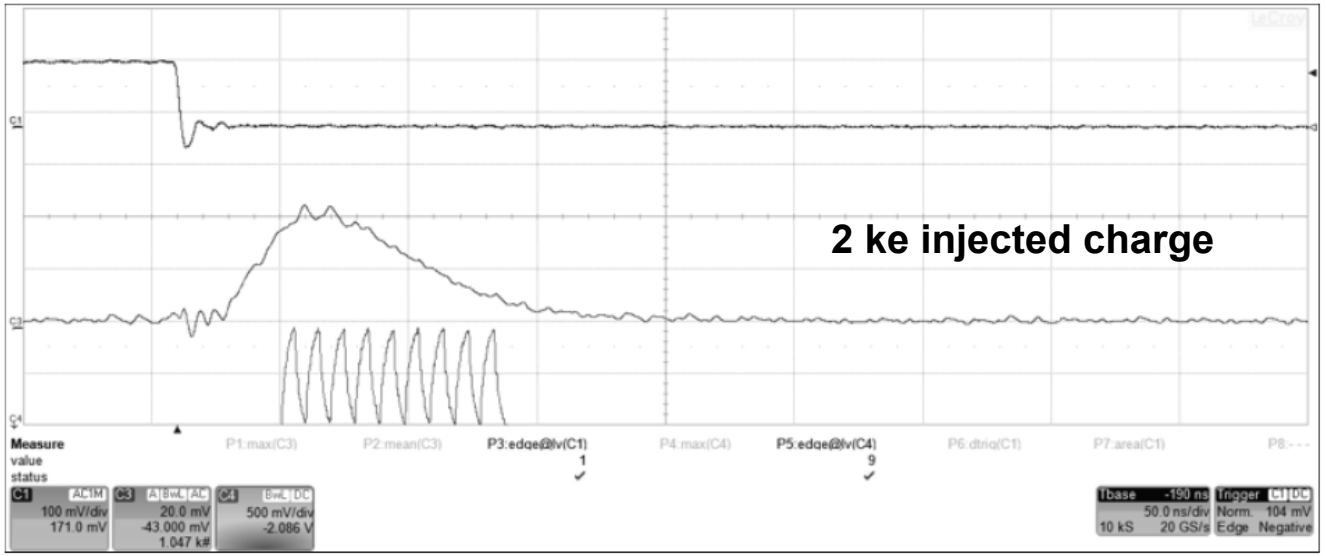
Basic electrical functionality /2

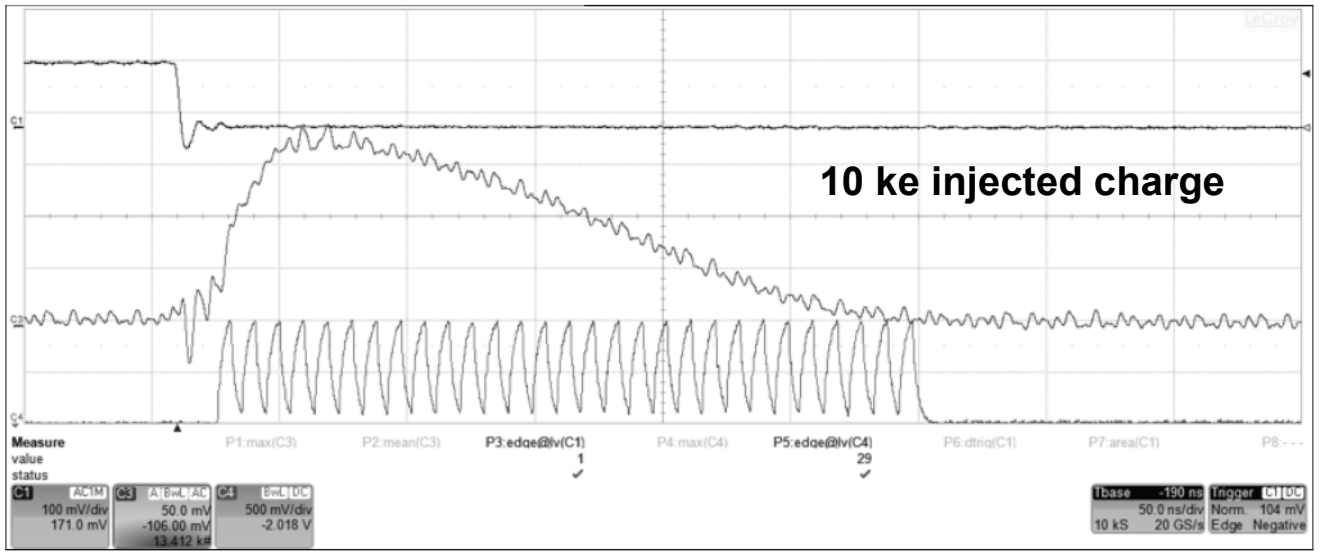




- 100 fF input capacitance
- 10 nA feedback current
- 40 MHz clock distributed to pixels
- **simple latch operations**

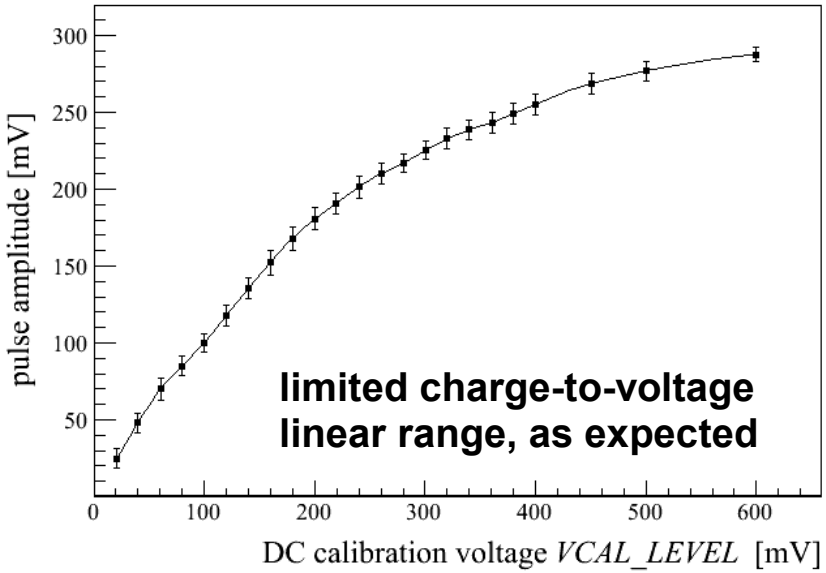
Basic electrical functionality /3

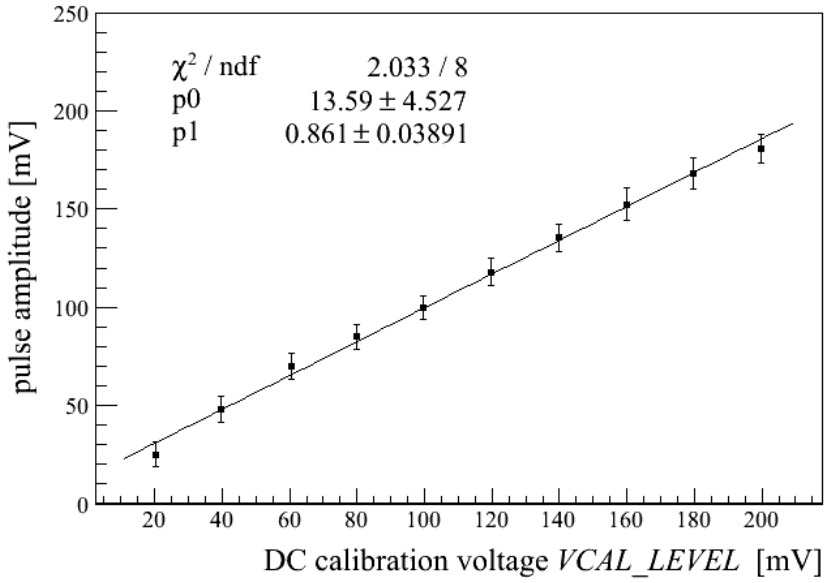


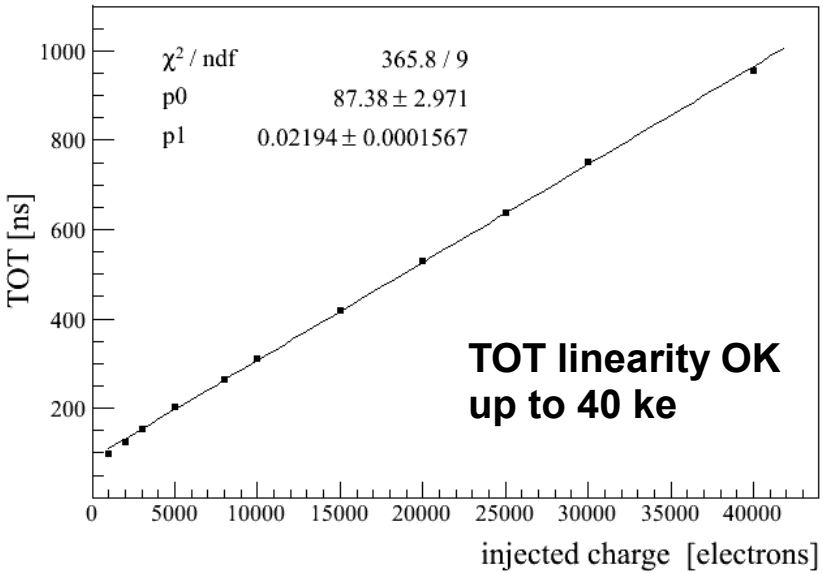


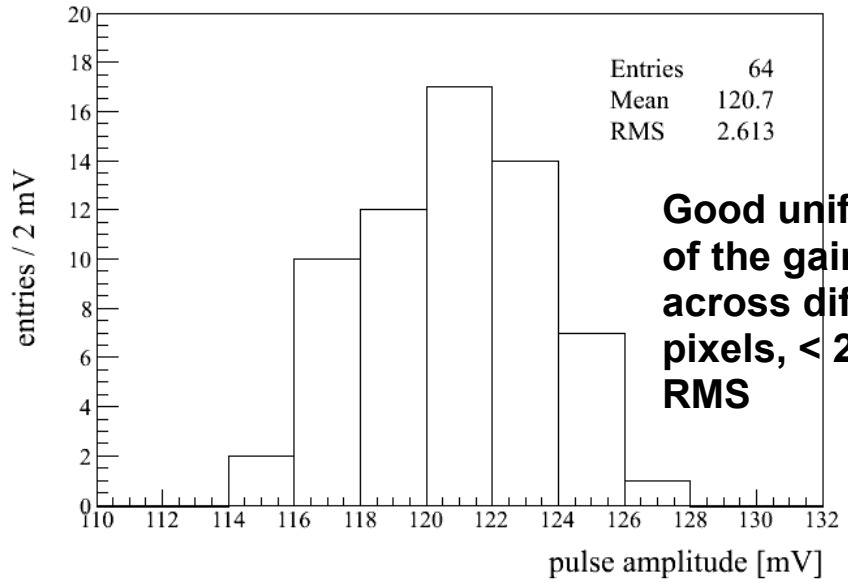
- 100 fF input capacitance
- 10 nA feedback current
- 40 MHz clock distributed to pixels
- **turning the latch into a VCO !**
- 100 MHz self-generated clock

Front-End linearity



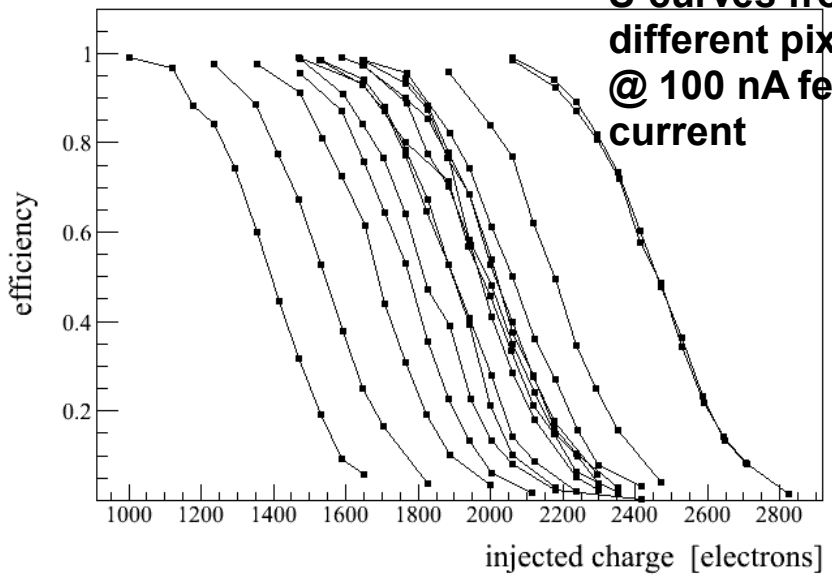


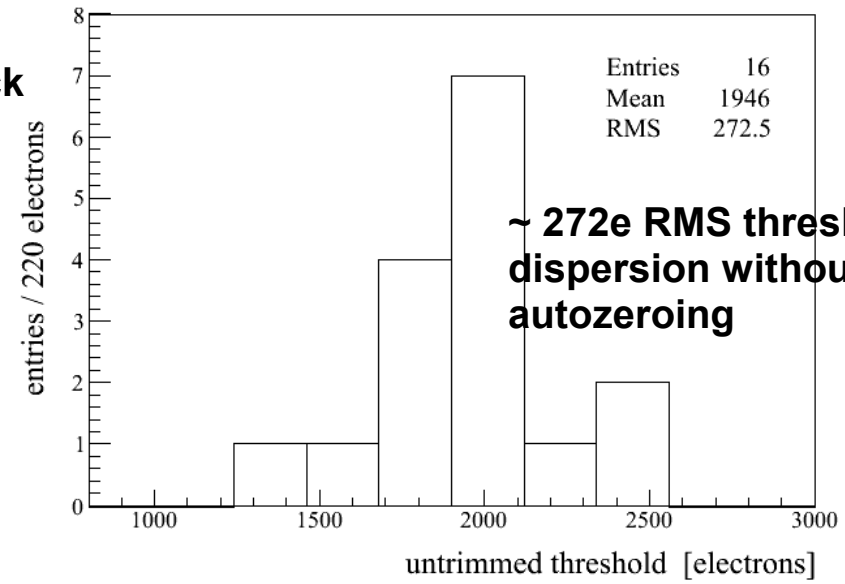




Threshold scan ad noise

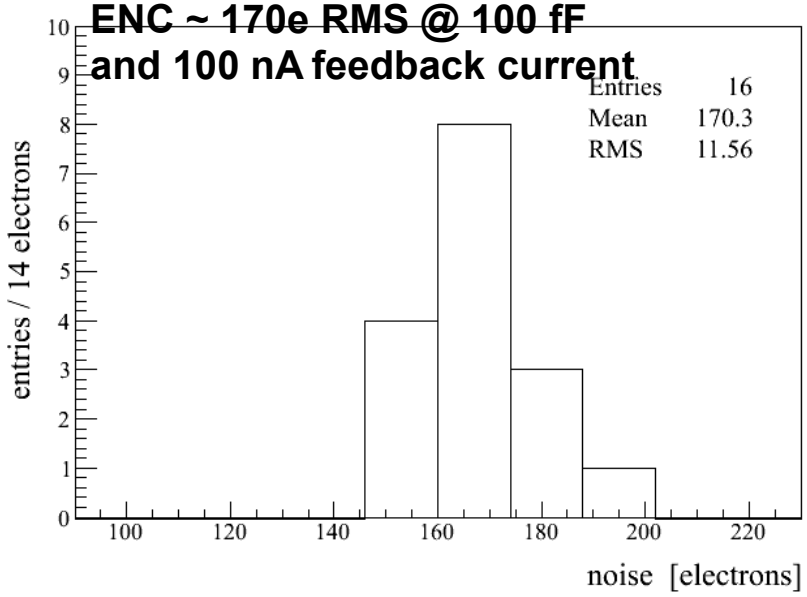
S-curves from 16 different pixels @ 100 nA feedback current



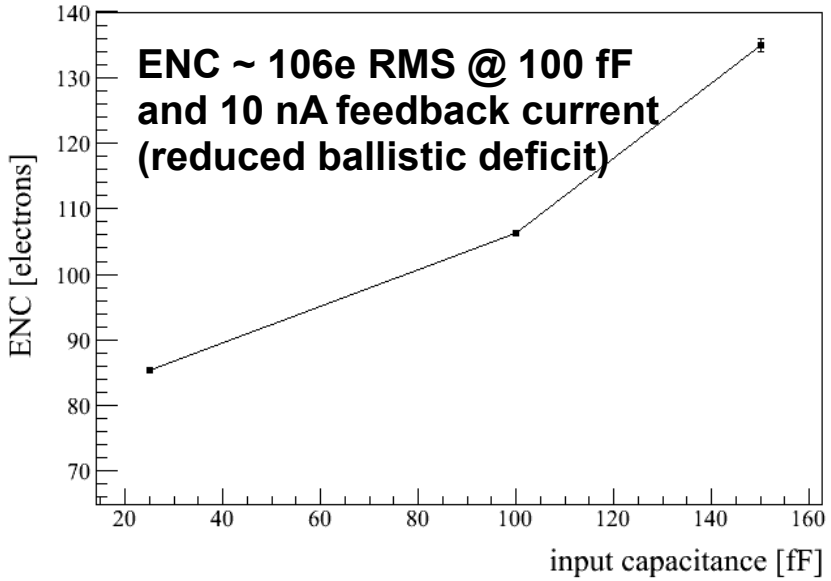


~ 272e RMS threshold dispersion without autozeroing

ENC ~ 170e RMS @ 100 fF and 100 nA feedback current



ENC ~ 106e RMS @ 100 fF and 10 nA feedback current (reduced ballistic deficit)



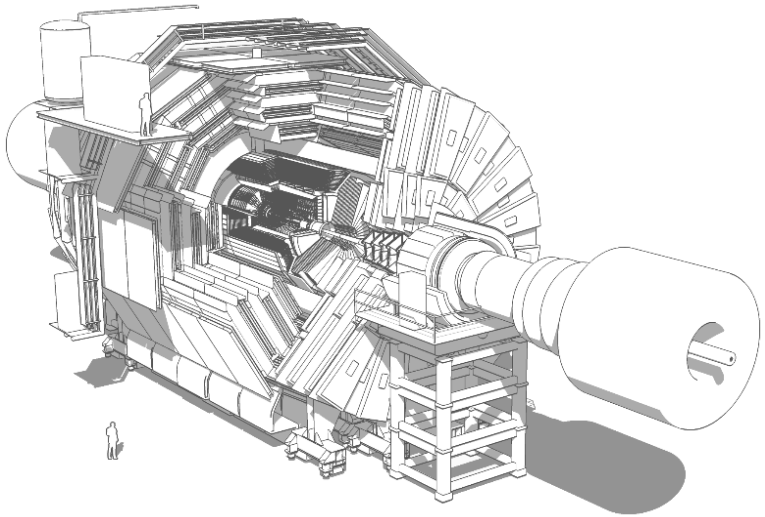
Conclusions and outlook

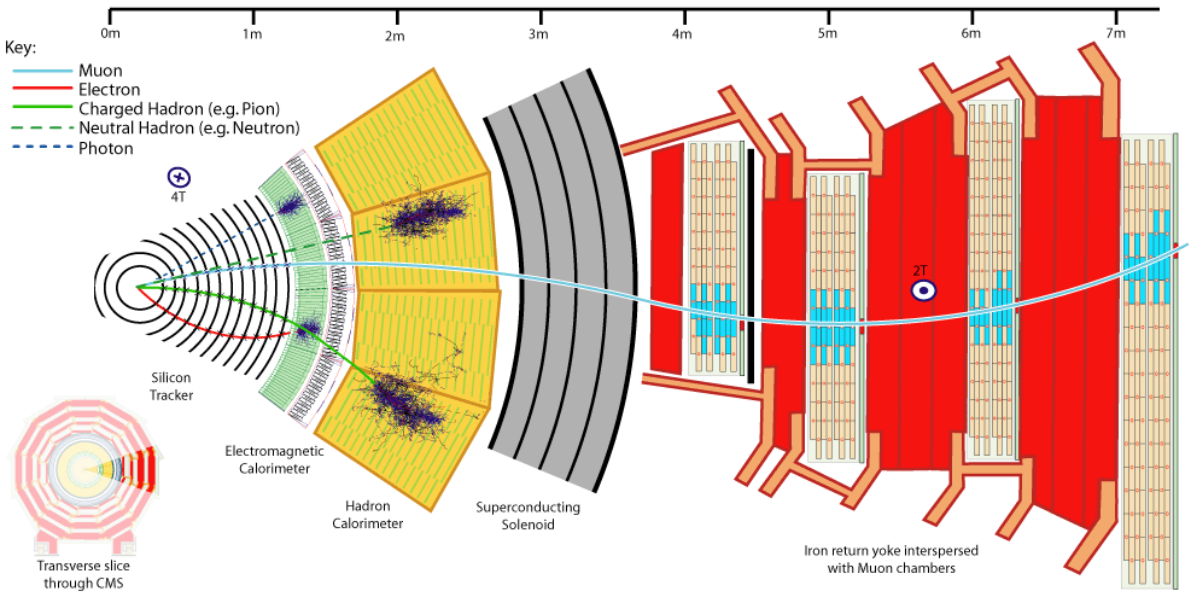
Summary

- HL-LHC operating conditions very challenging (PU, radiation levels, data rates)
- a commercial **65 nm CMOS** has been chosen by the HEP pixel community as a promising fabrication technology for the next generation of pixel ASICs
- new 3-years joint ATLAS/CMS collaborations **RD53** and **CHIPIX65** are devoted to investigate 65 nm technology capabilities and radiation tolerance
- Ph.D. research activity mainly focused on the design of an **innovative solution** for a **pixel analog Front-End chain** suitable for the foreseen Phase2 CMS pixel upgrade
- charge encoding scheme based on a latch coupled to **asyncronous control logic** for fast ToT measurements (up to ~GHz frequencies!)
- offset compensation with an **autozeroing technique**
- **first test-prototypes** have been put on silicon in October 2014
- **preliminary test results** from CHIPIX_VFE1/TO are very encouraging !

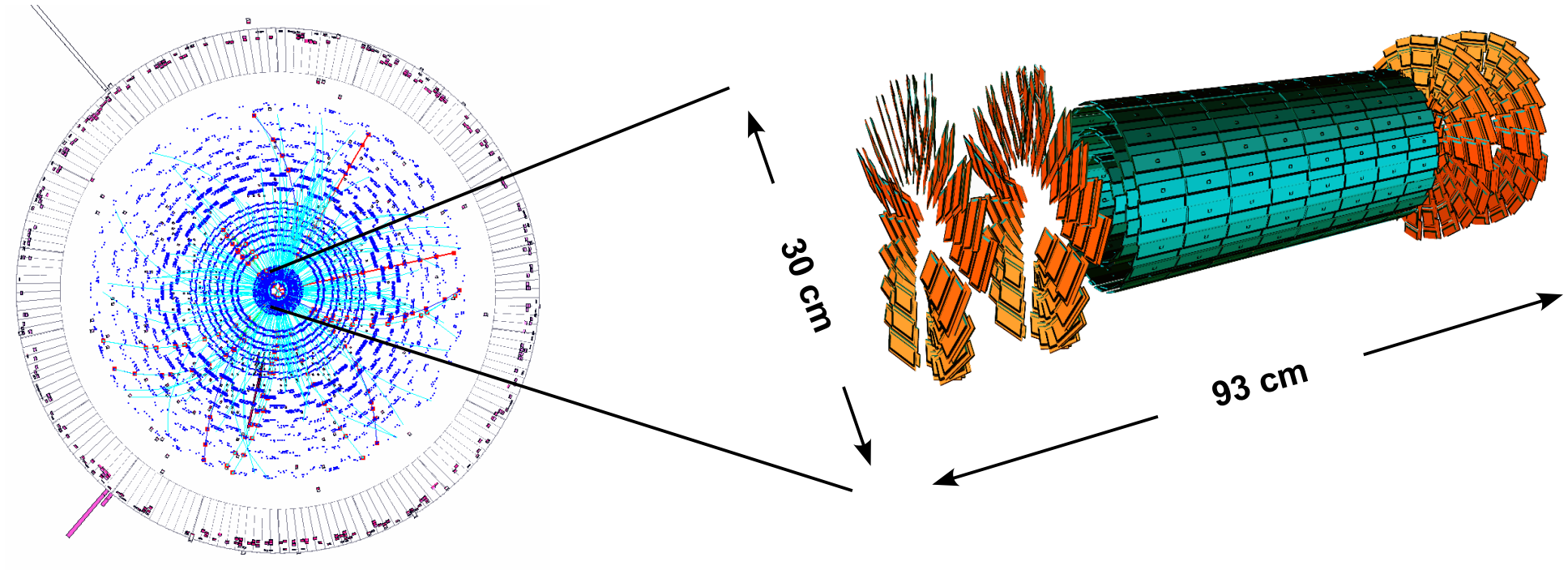
Backup slides

The CMS experiment at LHC





Silicon Pixel Tracker

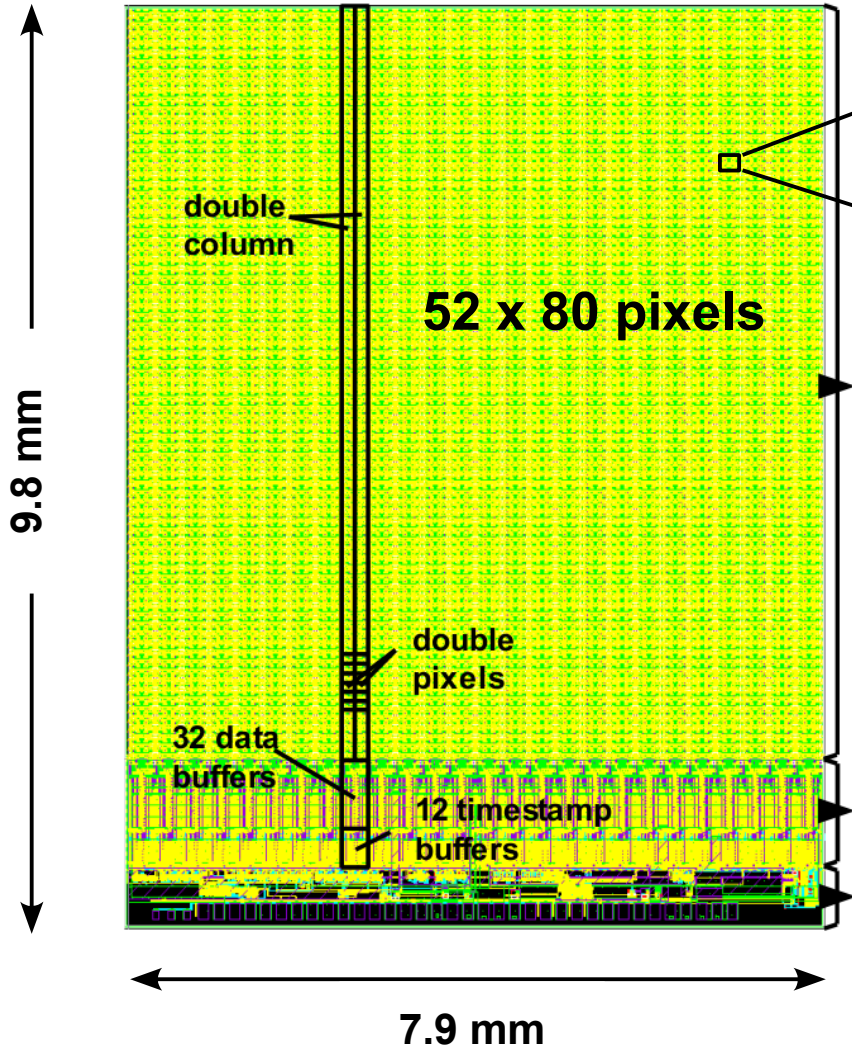


Current CMS silicon pixel detector layout:

- 3 barrel layers (BPIX) + 2 forward disks each side (FPIX)
- coverage $|\eta| < 2.5$, ~ 1 m^2, 66 Mpixels
- track seeding, IP resolution, SV reconstruction
- **hybrid pixel detectors**

CMS pixel Read-Out Chip (ROC)

0.25 µm 5M CMOS technology (PSI46v2)

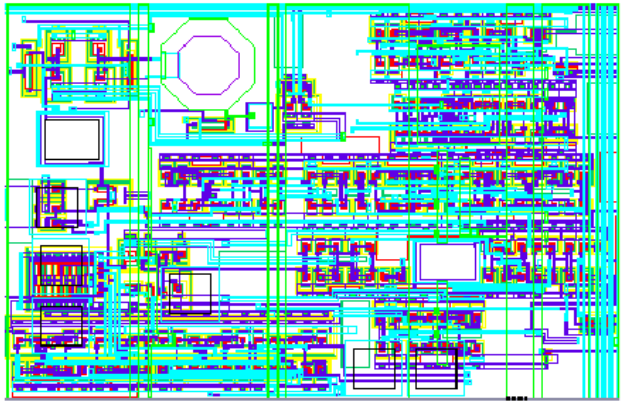


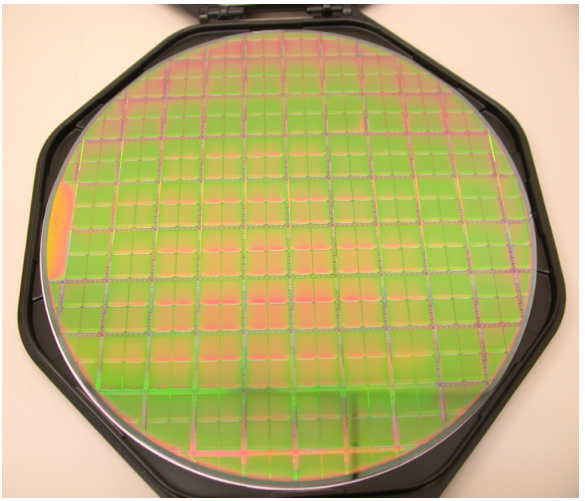
pixel array:
52 columns x 80 rows =
4160 pixels
(26 double columns)

double column periphery
(data buffers, timestamp buffers)

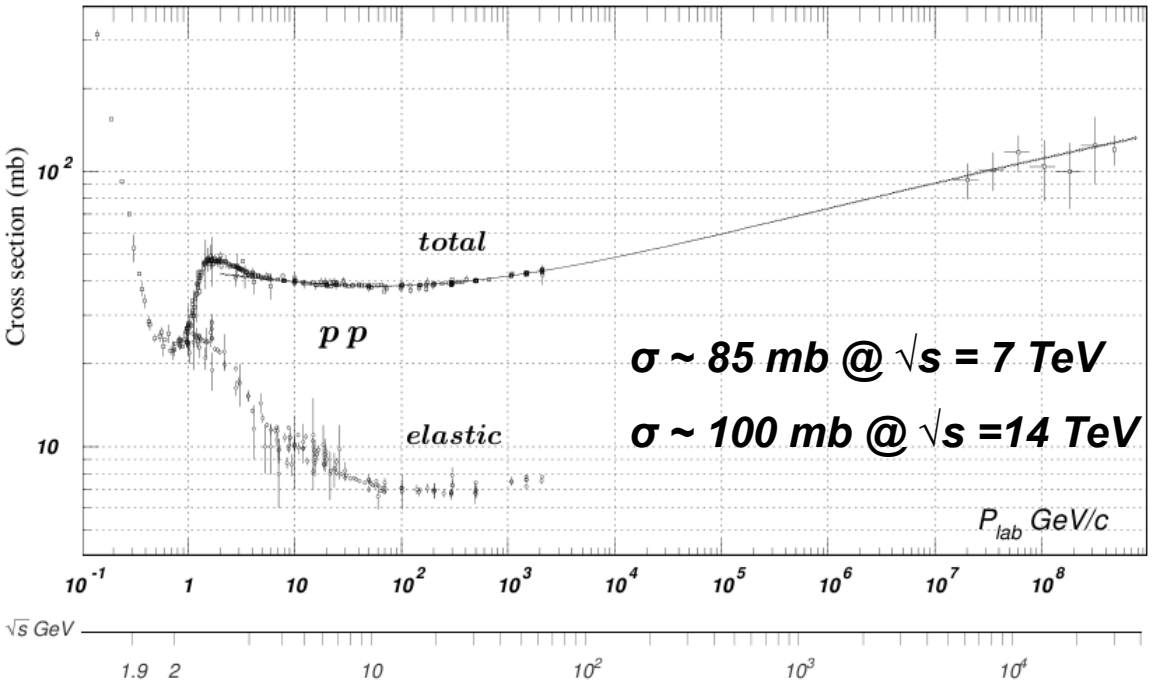
control interface block &
supply pads

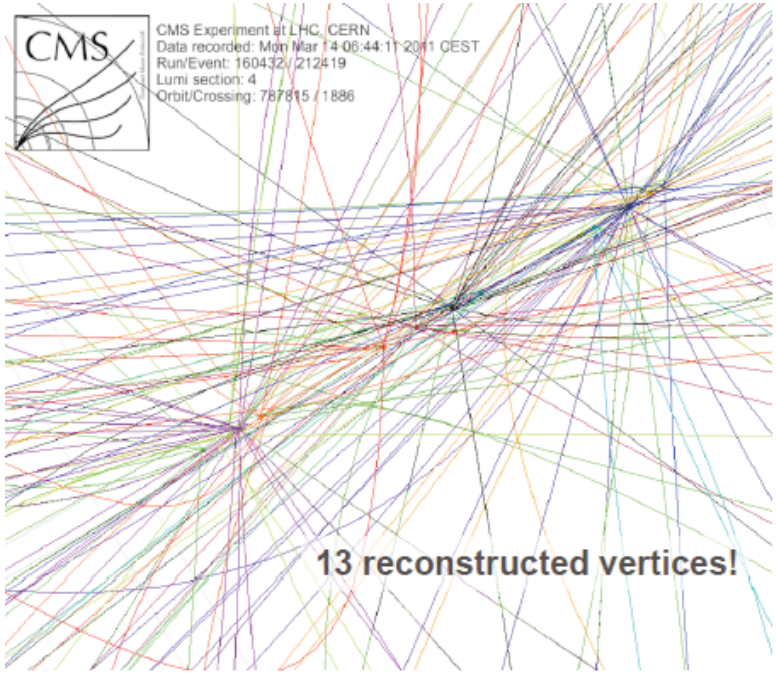
Pixel Unit Cell (PUC)





Luminosity and Pile-Up (PU)

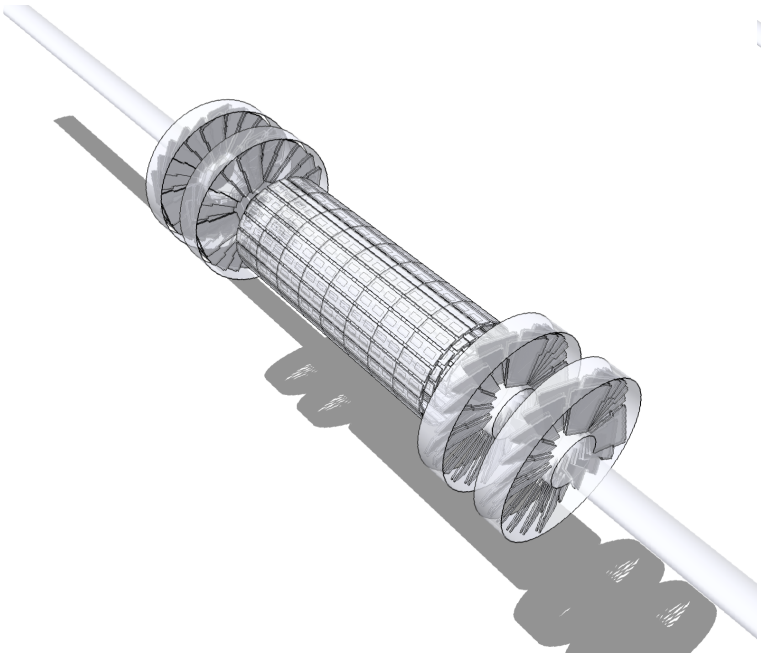


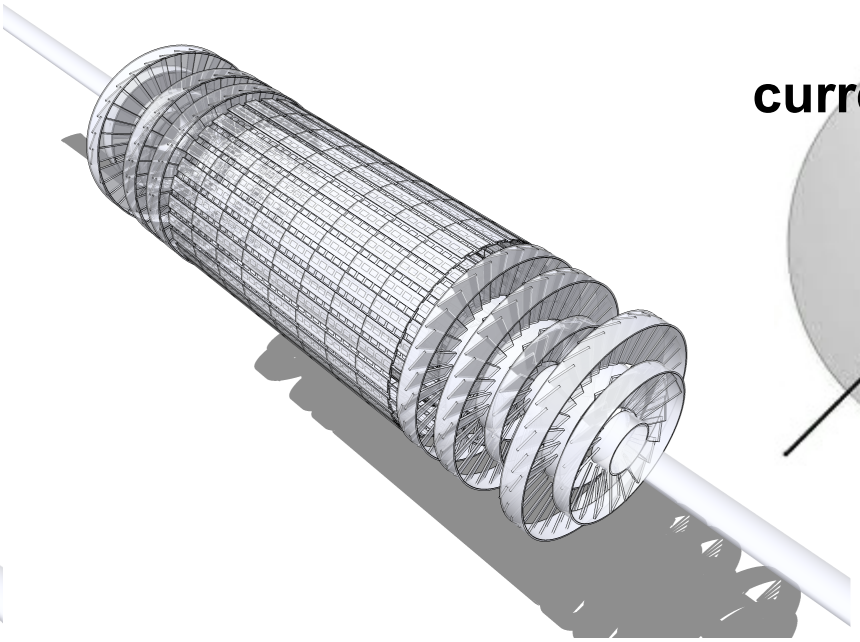


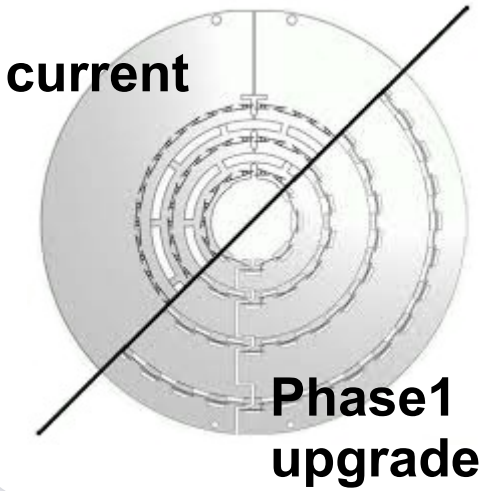
#interactions per BX = (total cross section x instantaneous luminosity) / bunch collision rate

<u>Ex.</u> 100 mb x 10^{35} cm^{-2} s^{-1} x 25 ns = 250 ! [1b = 10 fm x 10 fm = 10^{-24} cm^2]

CMS Phase 1 pixel upgrade



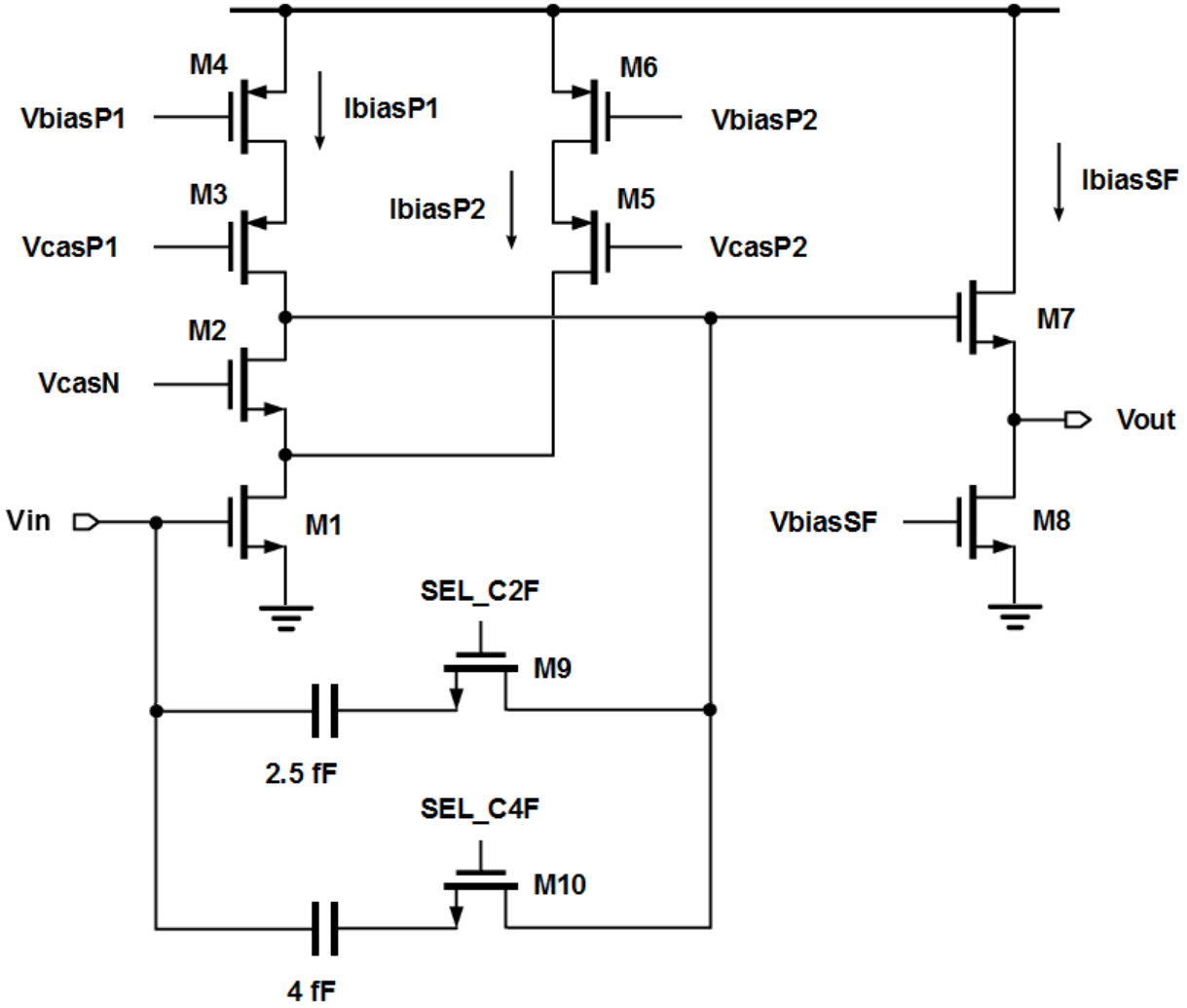




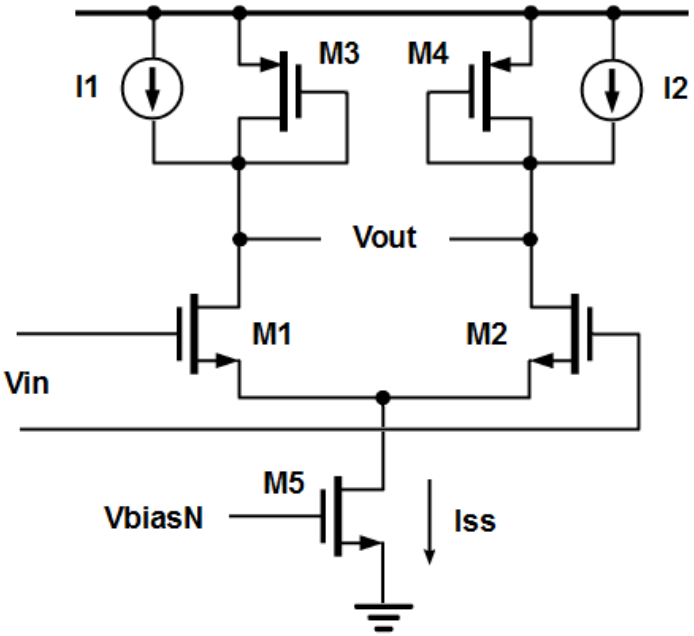
CMS **Phase1** pixel detector upgrade (end of 2016)

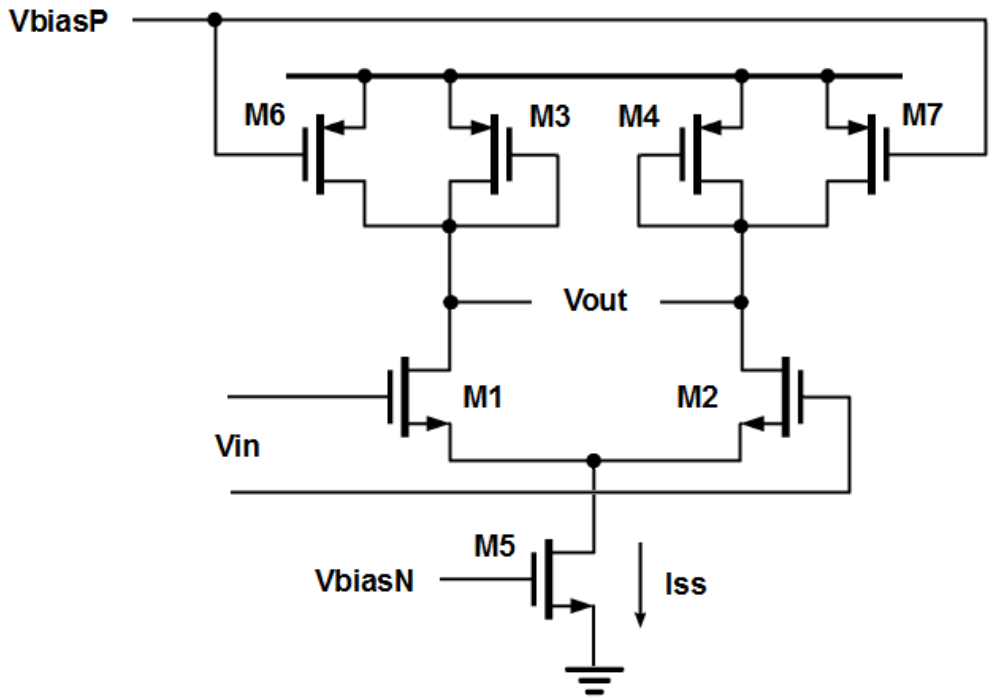
- BPIX: 3 → 4 layers
- FPIX: 2 → 4 disks
- pixel ASIC: improved version of the current PSI46v2 chip (PSI46v2DIG) to reduce data loss due to electronics readout

CSA core amplifier



Low-gain preamplifier





Class AB vs dynamic operations