Design and Test of Sensors and Front-End Electronics for Fast Timing in High Energy Physics

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XXX Cycle

Outline

Introduction

- Timing in high energy physics
- Timing with silicon detectors

Research activity

- Ultra-Fast Silicon Detectors
- TOFFEE ASIC
- Measurements on TOFFEE+UFSD

Conclusions

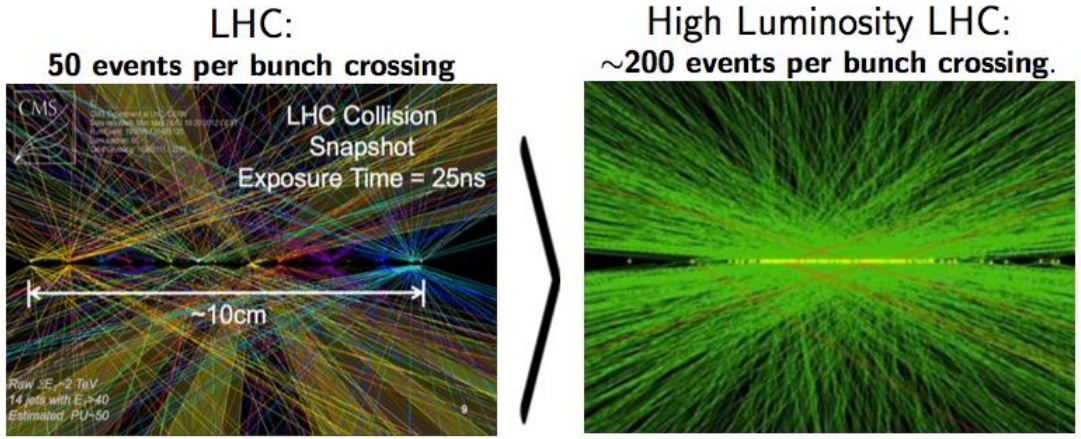
Timing in high energy physics

Fundamental in particle physics, from particle identification to determination of spatial coordinates

HL-LHC environment:

- **pileup of events** (~ 150-200 /bunch crossing, ~ 150 ps RMS time)
- **fake jets** and reduced accuracy in absence of proper reconstruction (15-20 % of the vertices merge together)

The reconstruction of time information allows to **distinguish different overlapping events**



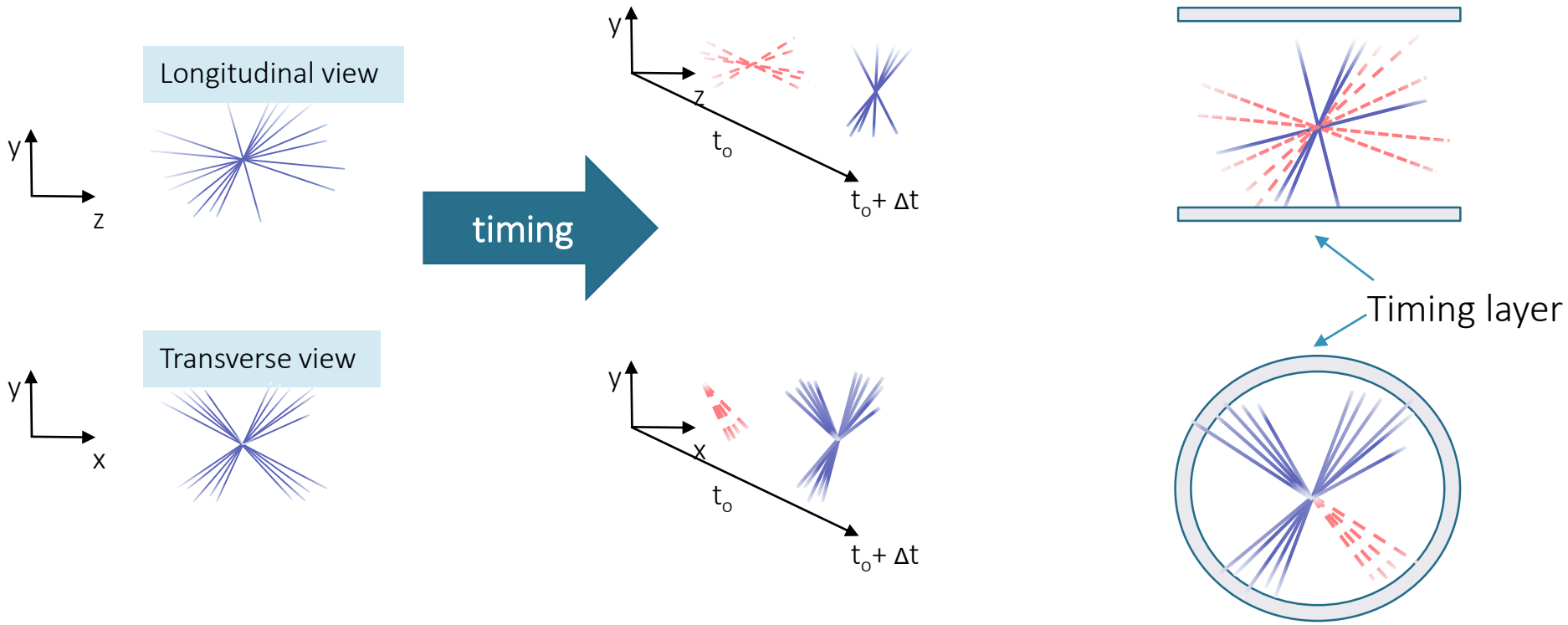
Spatial (3D) tracking is sufficient to reconstruct each vertex.

Pile-up of Vertices (15%). Timing allows distinguishing overlapping events: 4D tracking.

Timing at track reconstruction → detector should provide both track and time information
Timing at event reconstruction → can be implemented with an additional timing layer

Timing at event reconstruction

Timing allows to resolve different events otherwise undistinguishable by adding an extra dimension



CMS timing upgrade

The CMS experiment is planning to introduce a **timing layer for MIPs** (MTD) outside the tracker

The traditional 3-dimensional vertexing can be upgraded to a **4-dimensional reconstruction**

The timing layer can enhance the capability of the detector, reducing the effect of pileup of HL-LHC to the LHC levels

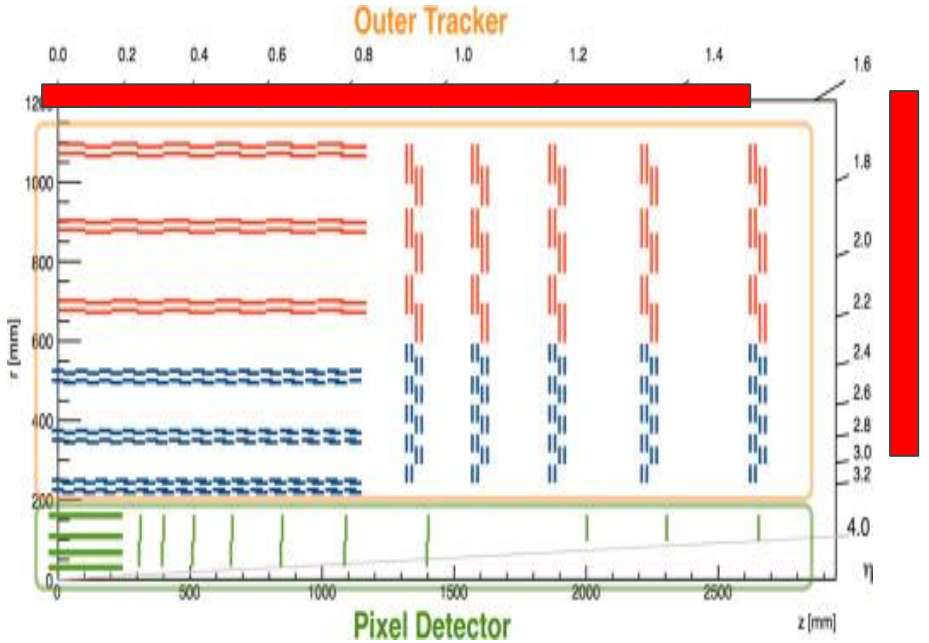
The MTD will be composed of

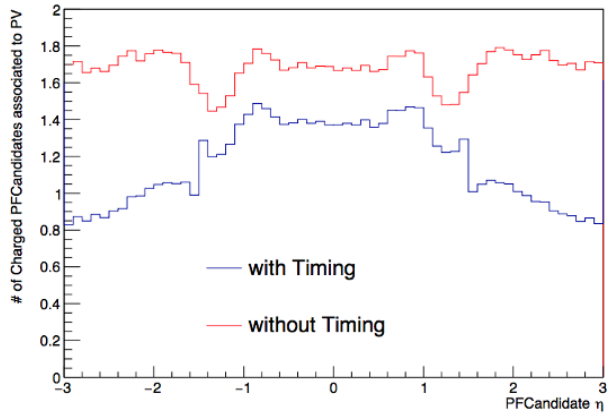
- **Endcap timing layer** → silicon detectors with gain + fast read-out

  $1.6 < |\eta| < 2.9$, $\Phi \sim 10^{15}$ n_{eq}/cm^{-2}

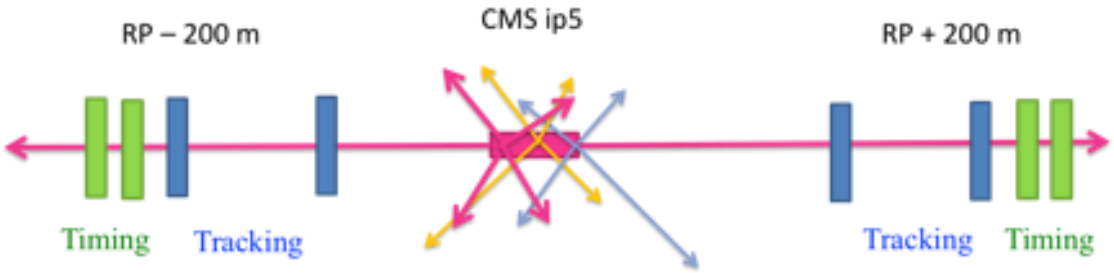
- **Barrel timing layer** → LYSO crystals + SiPMs + read-out

  $0 < |\eta| < 1.48$, $\Phi \sim 10^{14}$ n_{eq}/cm^{-2}





Timing at CT-PPS



The **CMS-TOTEM Precision Proton Spectrometer** (CT-PPS) is a **forward spectrometer** with the aim of detecting protons constituting the final state of a Central Exclusive Production (CEP): $pp \rightarrow pXp$

Protons from CEP have lost a small fraction of their initial transverse momentum and are detected by tracking and timing detectors located in detector stations (roman pots) on both arms of the spectrometer

Timing detectors: diamond (present), **silicon detectors with gain** (possible option)

Timing detectors allow to calculate the «z by timing» coordinate according to $\Delta z = c\,\Delta(t_1 - t_2)/2$

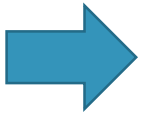
➡ **The plan is to reconstruct the time information with σ_t ~20 ps**
i.e. z position with an accuracy of ~ 4 mm

Time resolution

The timing capabilities are determined by the characteristics of the signal at the output of the preamplifier

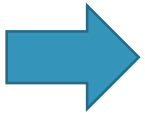
$$\sigma_t = \frac{N}{\frac{dV}{dt}}$$

Other contributions to the time resolution account for the chosen readout electronics (time walk, TDC binning)



Required:

- Noise minimization
- Large and uniform signals
- Short rise time



FAST SENSOR + PROPER READOUT

Timing with silicon detectors (I)

- Standard silicon detectors can be used in timing applications with an appropriate geometry
- Silicon detectors benefits include low material budget, low cost, good radiation tolerance, easy electrode segmentation and high rate capabilities
- Standard silicon sensors can achieve good time resolutions. However, it is difficult to reach resolutions better than $\sigma_t \sim$ 80–100 ps given their **small signal**
- The aim is to design a **silicon detector for timing**, with signals $\sim$ 10 times higher than a standard one

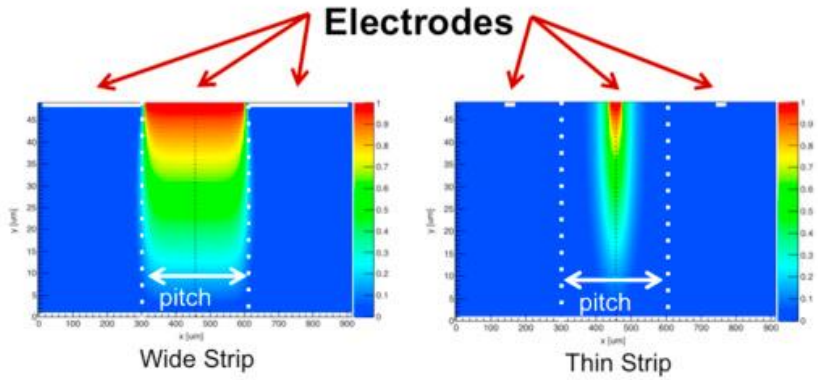
Timing with silicon detectors (II)

- A Minimum Ionizing Particle (MIP) in a standard silicon detector produces ~ 80 e-h pairs/um
- The signal of a silicon detector is produced by charge carriers drifting through the bulk and is defined as the induced current on the electrodes
- The instant induced current on a single electrode is modeled by **Shockley-Ramo's theorem**

$$I_i \propto q\, v\, E_w$$

drift velocity — Weighting field

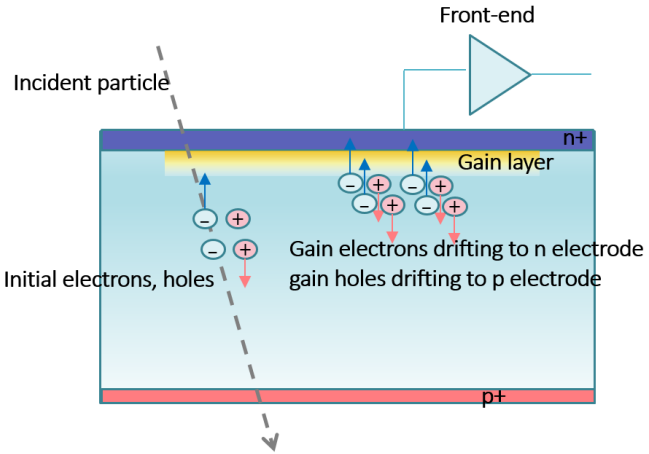
- The key for good timing is the uniformity of the signals
  → drift velocity and weighting field need to be as uniform as possible
  → parallel plate geometry: **strip implant ~ strip pitch ≫ thickness**

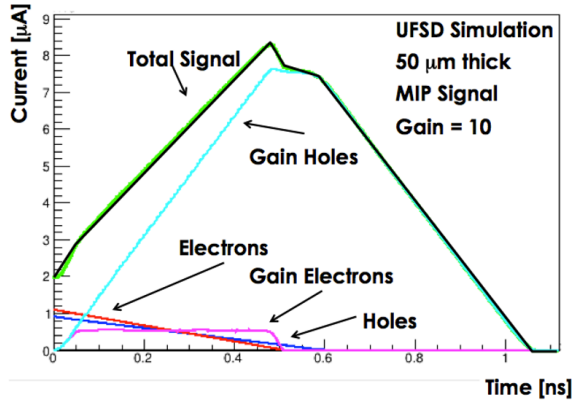


- By **reducing the sensor thickness** dt becomes short, however dV is still not large enough
  → **use avalanche multiplication to increase the amplitude**

Ultra Fast Silicon Detectors

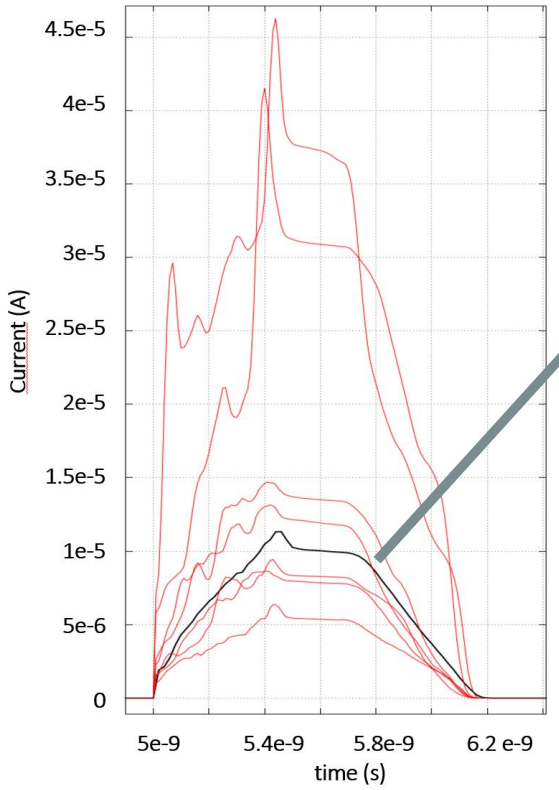
- UFSD have been designed to minimise the $N/\frac{dV}{dt}$ term
- They have a particular signal shape due to **charge multiplication**
- To achieve charge multiplication **E= 300 kV/cm** is necessary
  → possible by adding a **p doping layer** internal to the sensor: gain layer
- Electrons multiply when crossing the gain layer generating **additional electrons and holes** (electrons have higher ionization coefficient than holes)
- The main part of the signal is **produced by gain holes** drifting to p electrode
- UFSD have **low gain** (~ 10): low shot noise, milder electric fields, possible electrode segmentation, behavior similar to standard silicon detectors
- Currently produced by CNM (Barcelona), FBK (Trento) and Hamamatsu

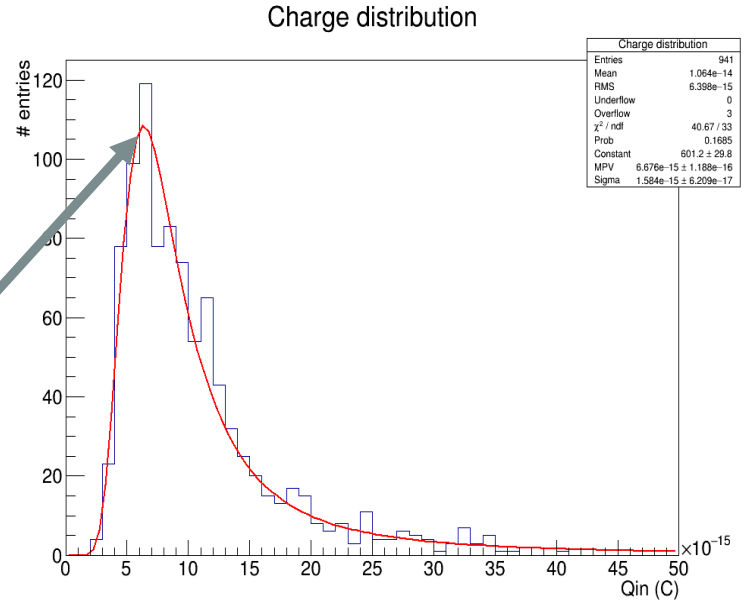




50 um UFSD signals

UFSD signals simulated with *Weightfield2*





Typical 50 um, gain 15 UFSD MIP signal
charge ~ 8 fC
signal length ~ 1.2 ns

UFSD are fast sensors providing steep signals

➡ an appropriate readout electronics is needed to reach the best time resolution

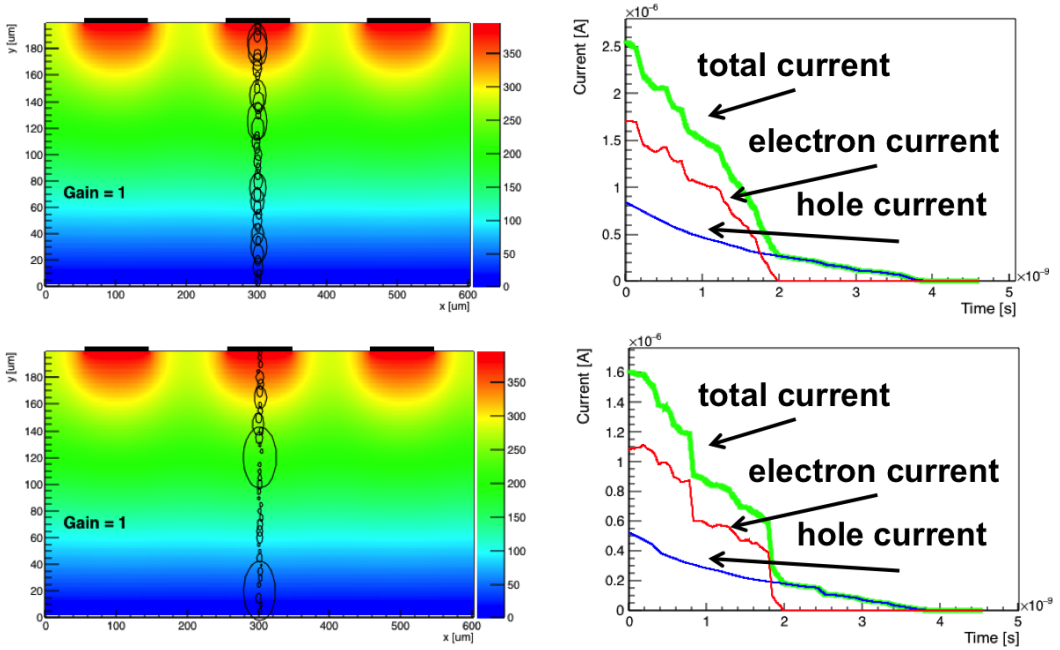
Time resolution of a UFSD-based system

Time resolution of a system composed of: UFSD sensor, amplifier, discriminator and TDC

$$\sigma_t^2 = \sigma_{Time\ Walk}^2 + \sigma_{Landau\ Noise}^2 + \sigma_{Distortion}^2 + \sigma_{Jitter}^2 + \sigma_{TDC}^2$$

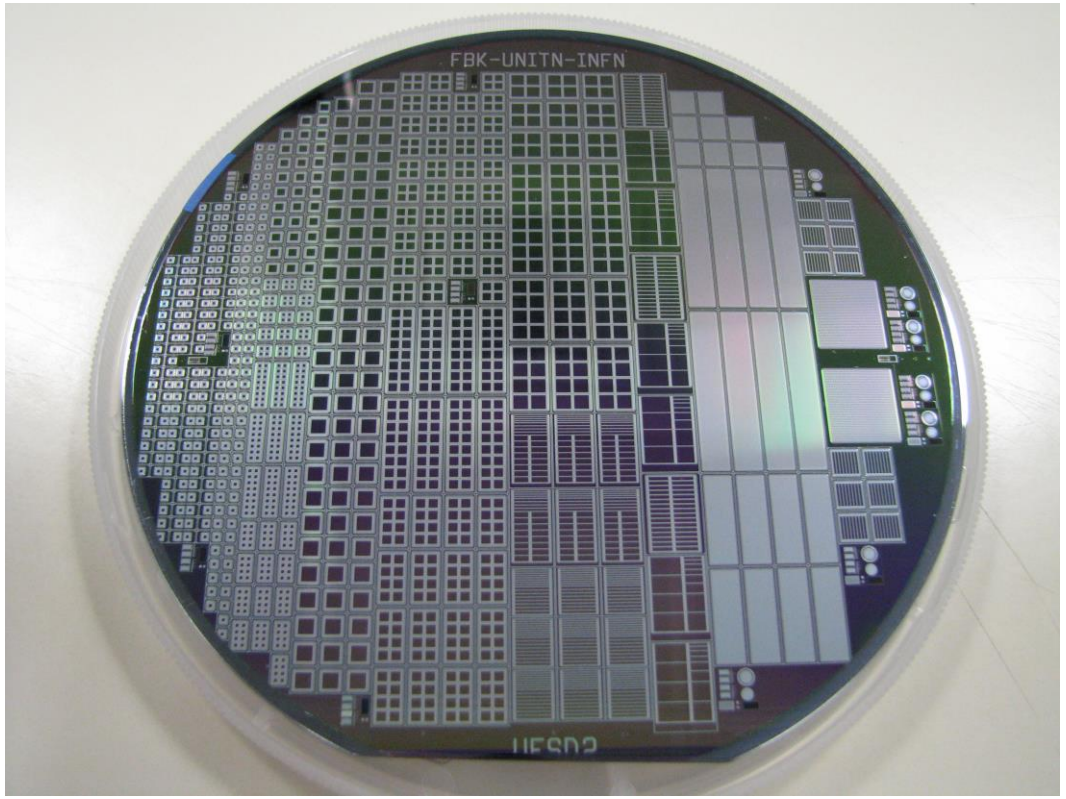
Landau noise: non uniform charge deposition

Distortion: signal variabilities due to non-uniformities in weighting field and in drift velocity
→ keep drift velocity saturated
→ uniform weighting field



Development of UFSD sensors at FBK

- UFSD design has been carried out with Fondazione Bruno Kessler (FBK) and Trento University
- Two productions
  - 275 um: double-sided
  - 50 um: with support wafer
- n-in-p devices (p-type bulk)

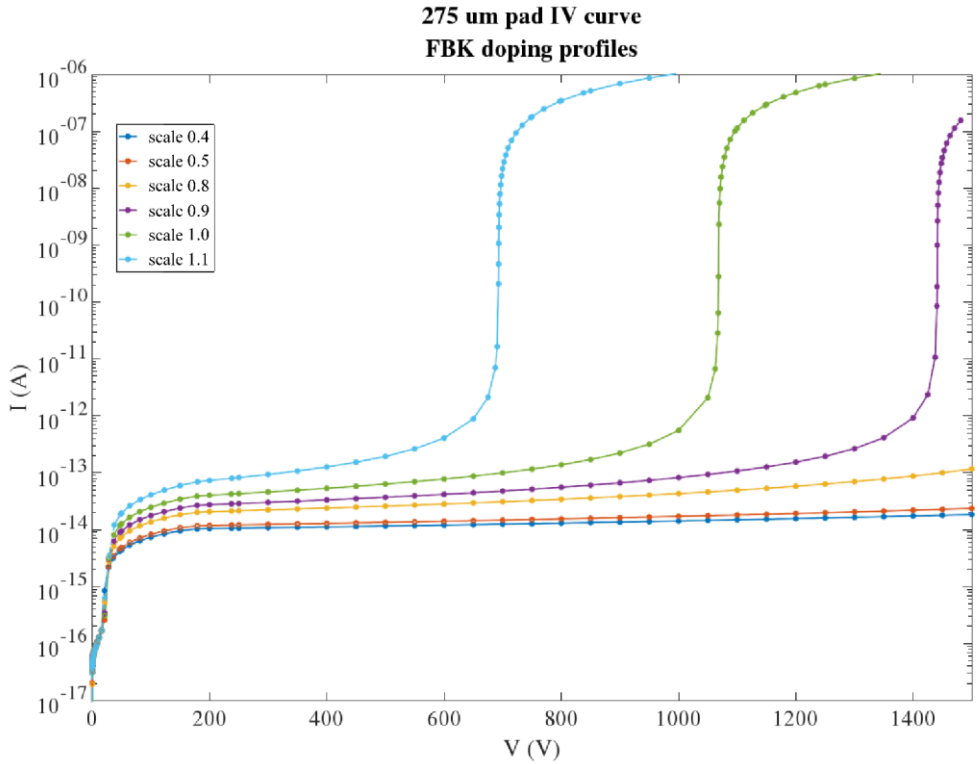


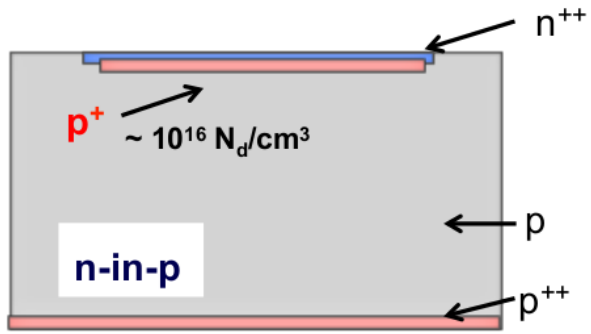
275 um production

First step: how to achieve controlled charge multiplication

Electrical simulations to predict the electrical characteristics of the devices (2D)

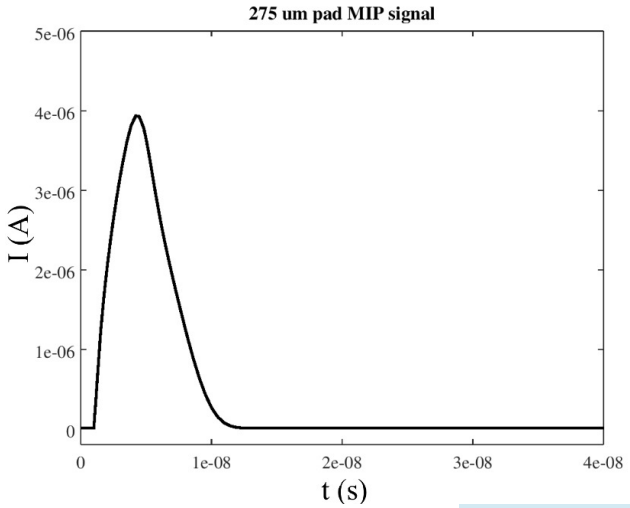
→ leakage current and breakdown voltage evaluation

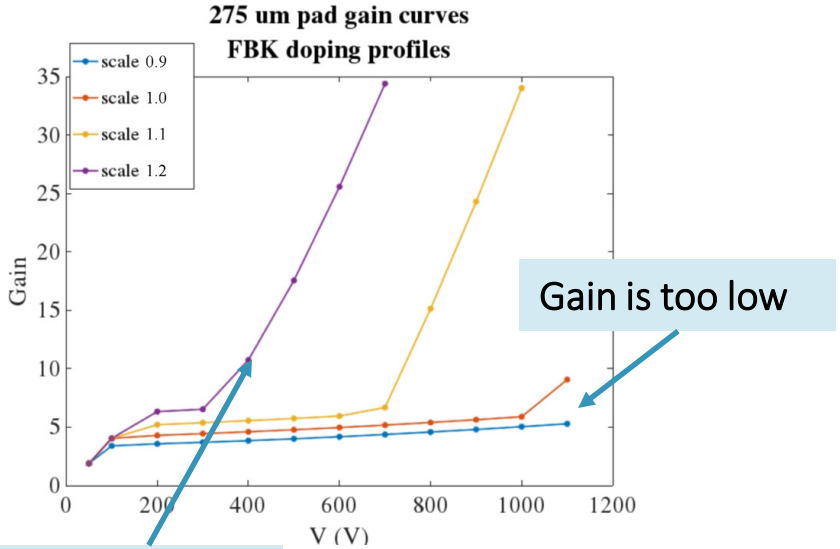




275 um - simulations

- **Dynamic simulations**, optical/heavy ion (2D with cylindrical geometry)
  → Charge collection and signal shape evaluation
  → Gain behavior with bias voltage





Gain is too low

Gain is too high:
Breakdown before drift velocity saturation

Signal shape,
~ 10 ns duration

Gain behavior with bias voltage, response to a MIP

275 um – dead area studies

The segmentation of the n electrode implies the segmentation of the gain layer

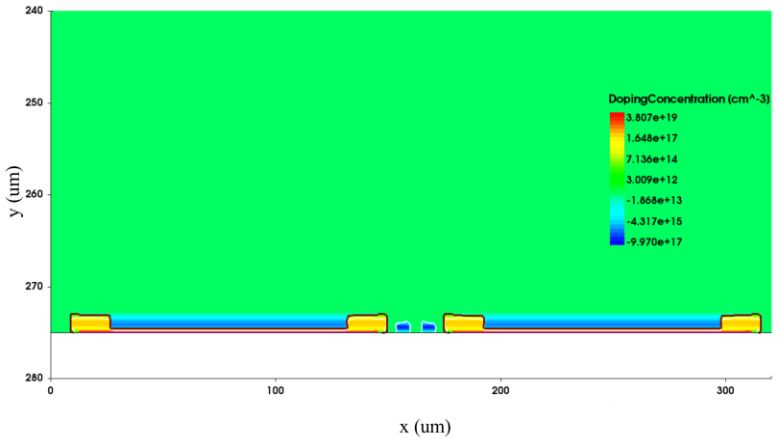
→ possible non-uniformity of electric and weighting fields, degraded timing performance

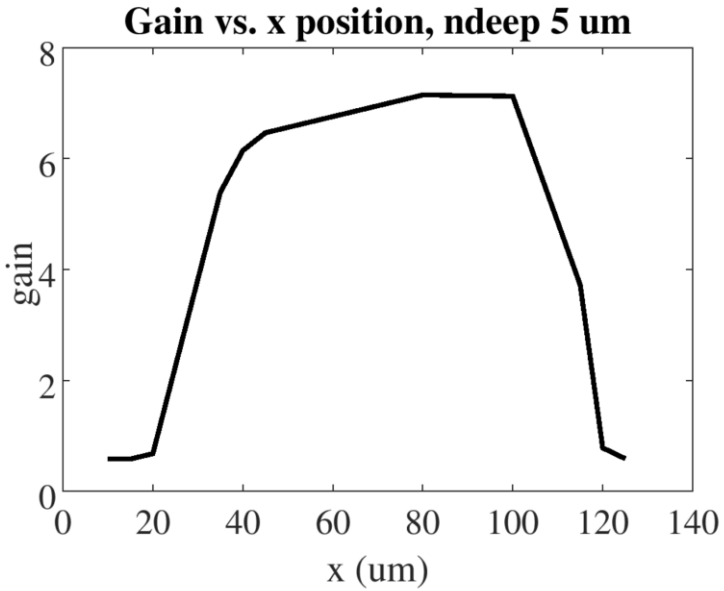
The inactive area between pixels due to the presence of the guardring can be a significant percentage of the total area

→ study of the reduction of the ndeep implant size between pads

- Simulation of 2 adjacent pixels hit by a MIP at different x positions separated by 2 pstops

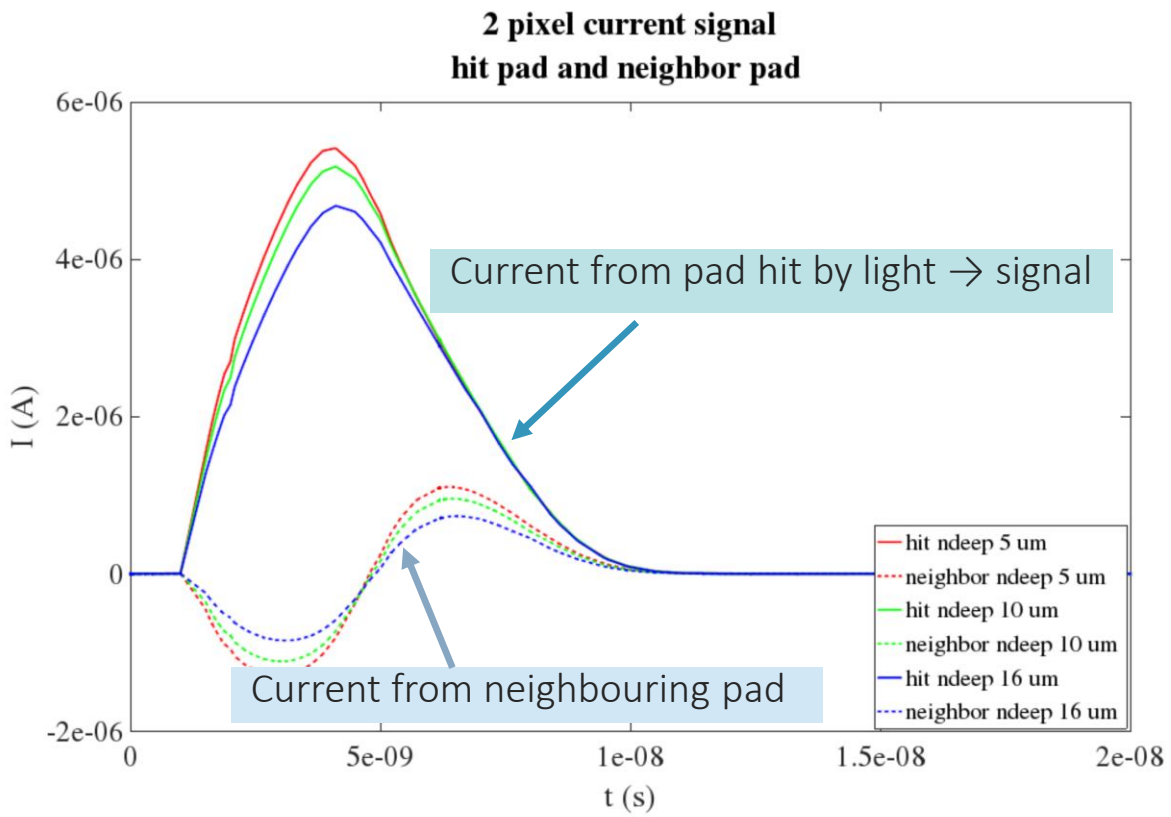
→ ndeep implant is dead area





275 um – dead area studies

The ndeep width can be reduced to 5 um without affecting the signal



275 um – AC coupling

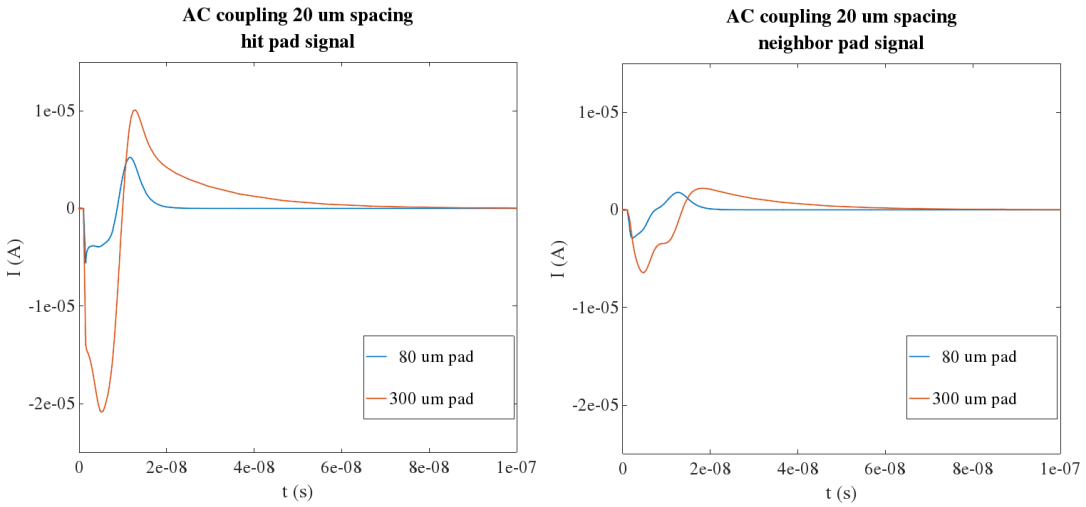
One possible way to achieve **electrode segmentation** and **dead area reduction** is the implementation of AC coupling

→ pixelated aluminum

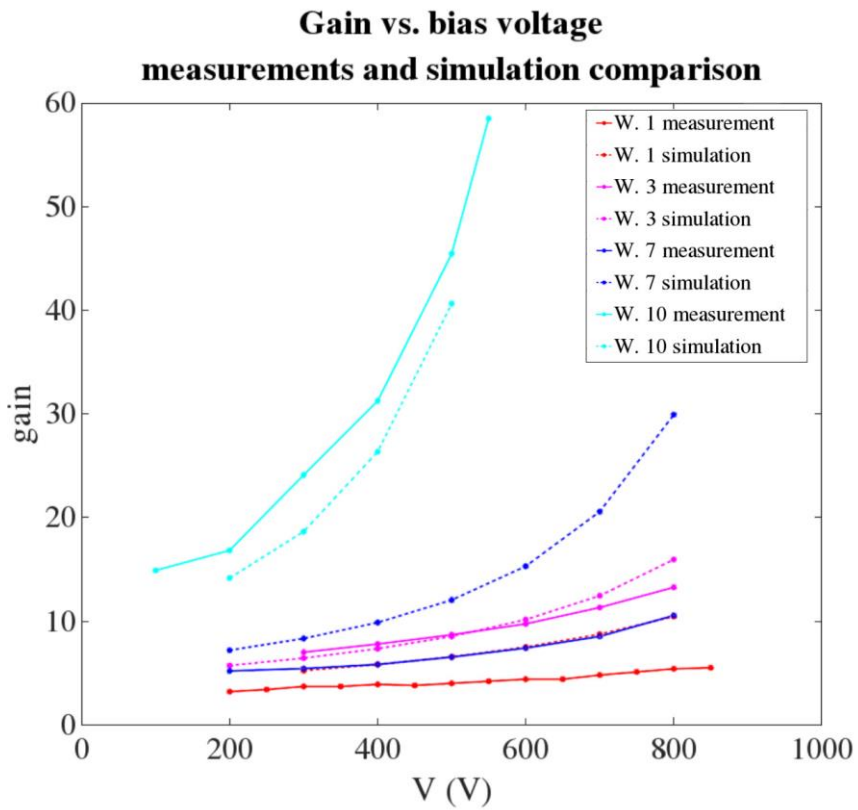
→ no gain layer segmentation

- AC pads are made of 2 conductive plates (n++, Al) and an insulator layer (SiO2 + Si3N4)
- Pads produce a bipolar signal (no net charge collection)

A device with 3 AC pads with different widths (300 um, 80 um) and spacings (20 um, 30 um) has been simulated

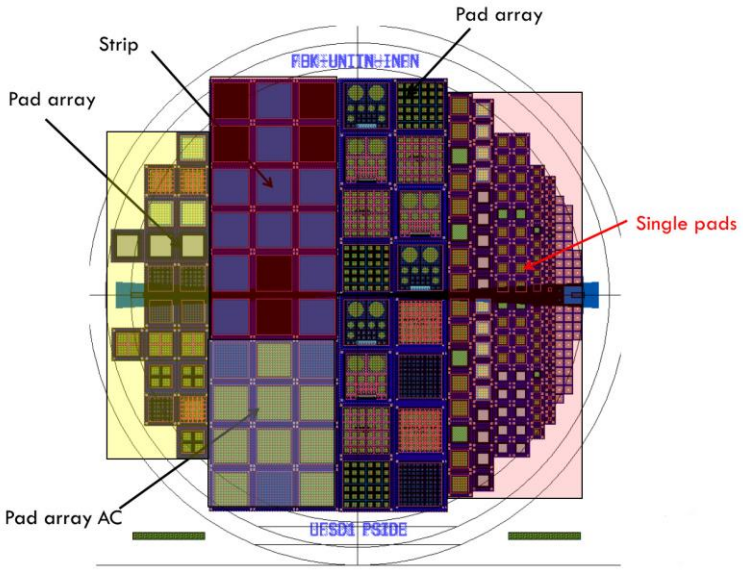


275 um – outcome



Gain measurements from laser tests:

- Good agreement between simulations and measurements for W3 and W10
- W1, W7: implanted dose slightly lower than simulated one



UFSD1 wafer layout

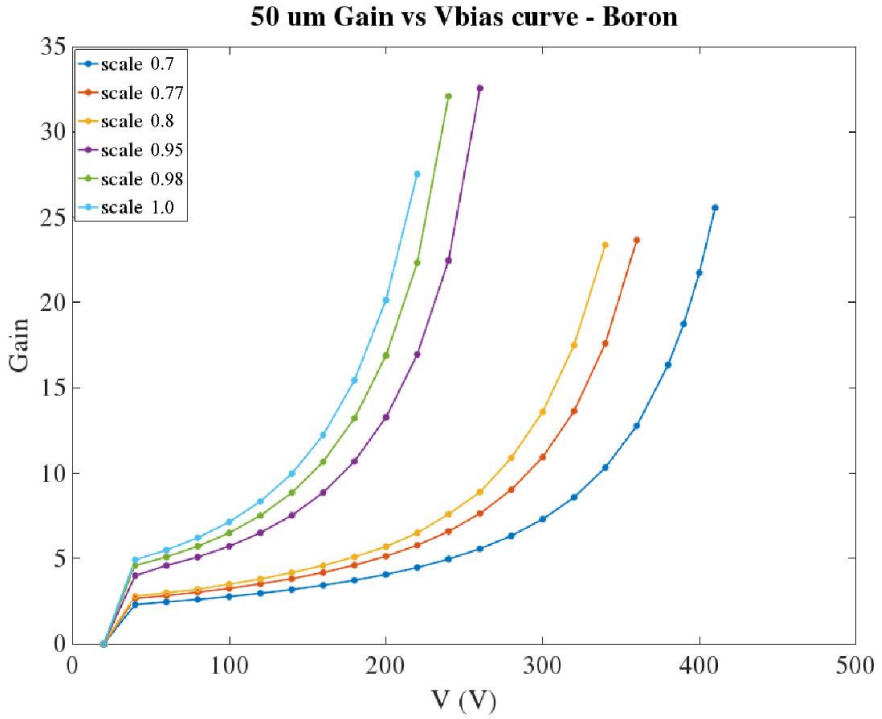
50 um production

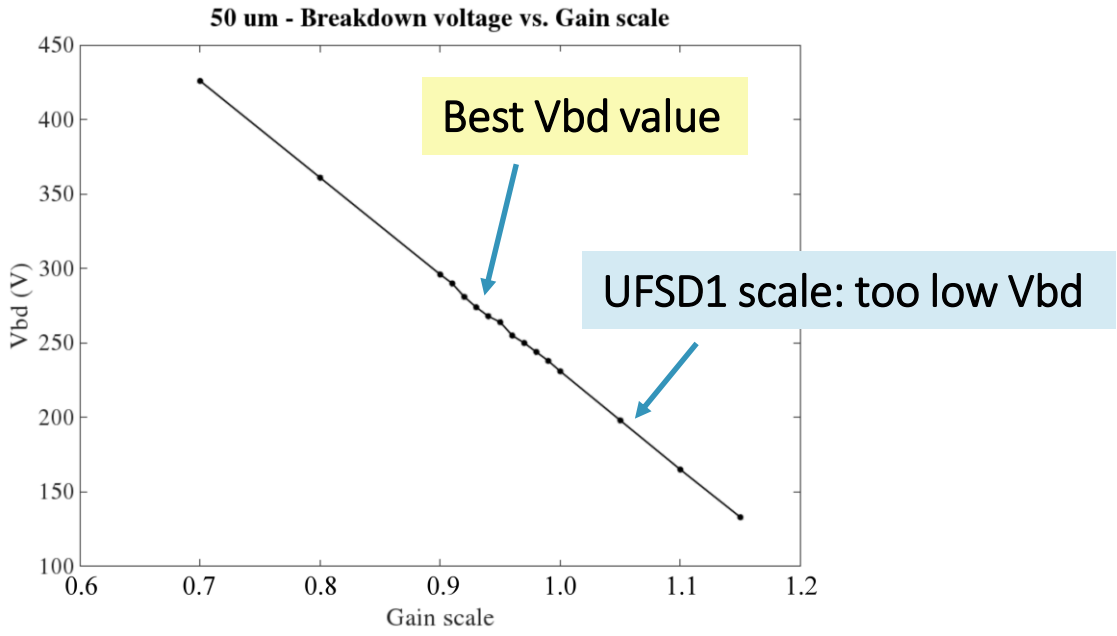
Studies on 50 um thick sensors:

- Tuning of gain layer doping for a **reduced bulk thickness**
  → breakdown voltage between 200 and 300 V, gain between 10 and 20
- Analysis on ndeep and pstop size for **dead area minimization**
  → Gain scan along x coordinate
- Study of the difference between diffused and non-diffused gain layer dopant
- Introduction of a different dopant for gain layer (Ga)

50 um – gain curves

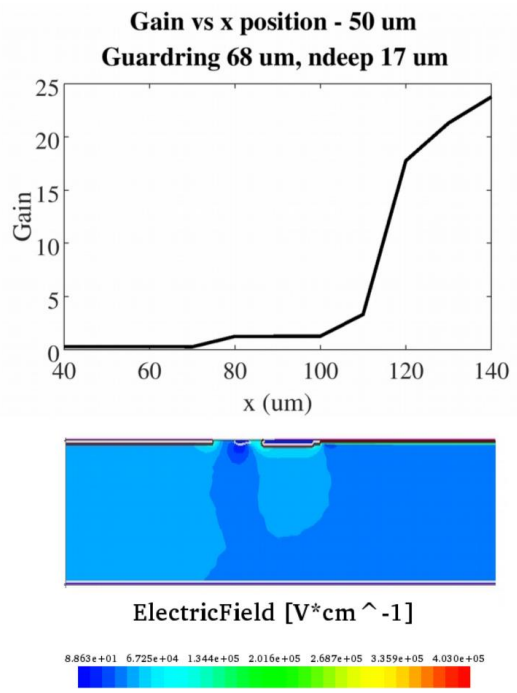
Study of the best matching between gain scale and breakdown voltage

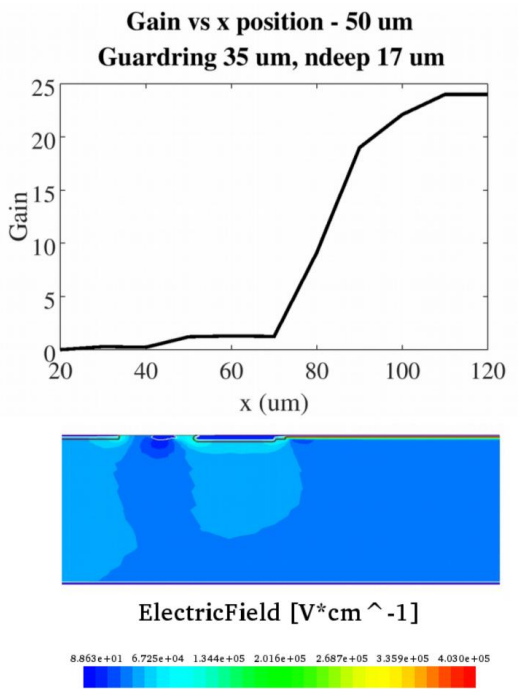


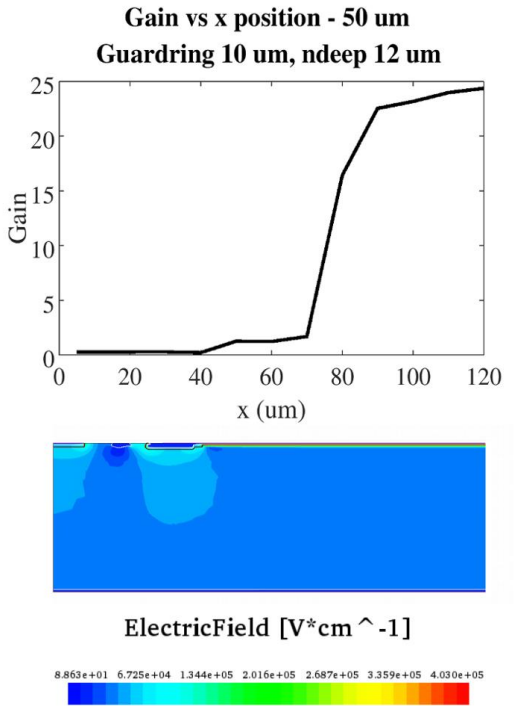


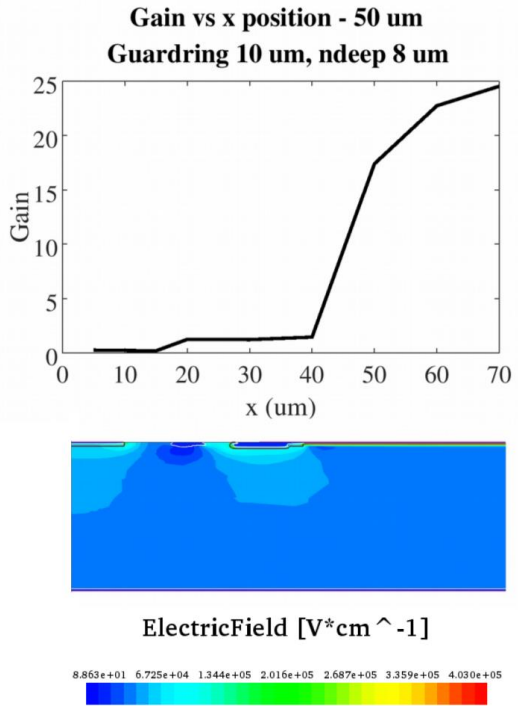
50 um – dead area studies

Extraction of gain value along x coordinate to study the effectiveness and size of ndeep/pstop implants (dead area between electrodes)





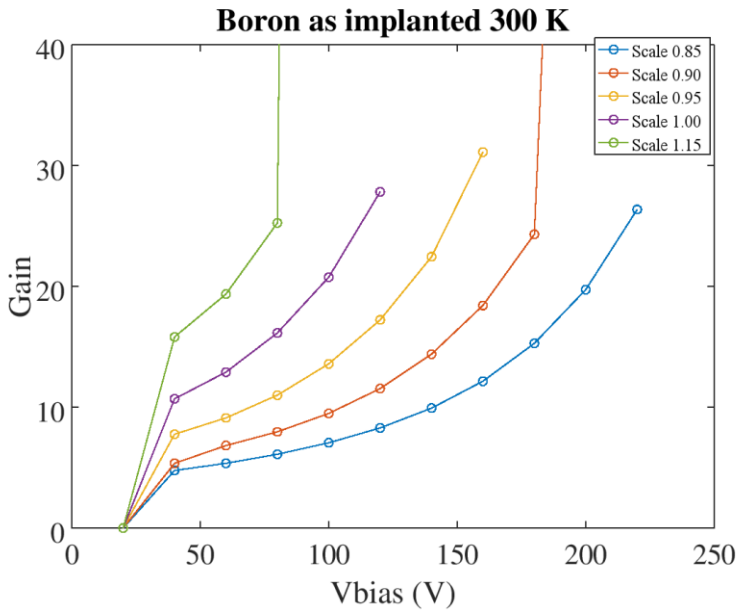


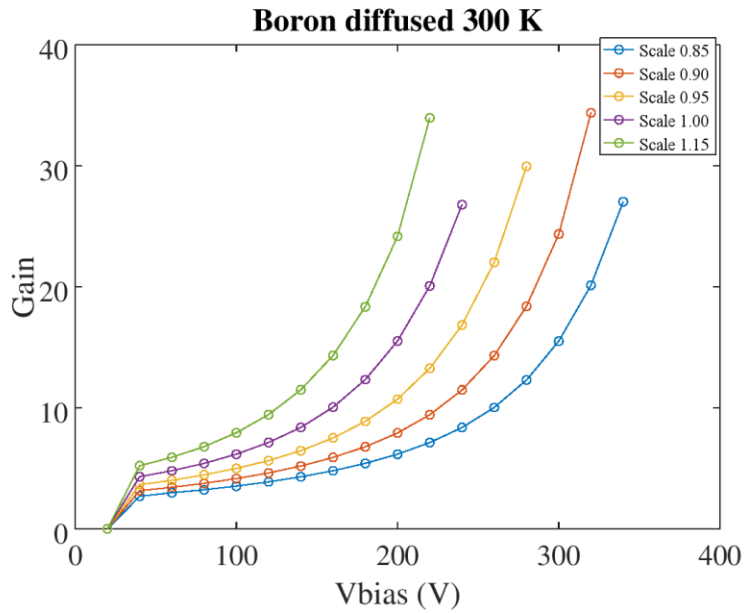


50 um – low and high diffusion

Diffusion temperature influences the gain layer width: study on low and high diffusion temperature

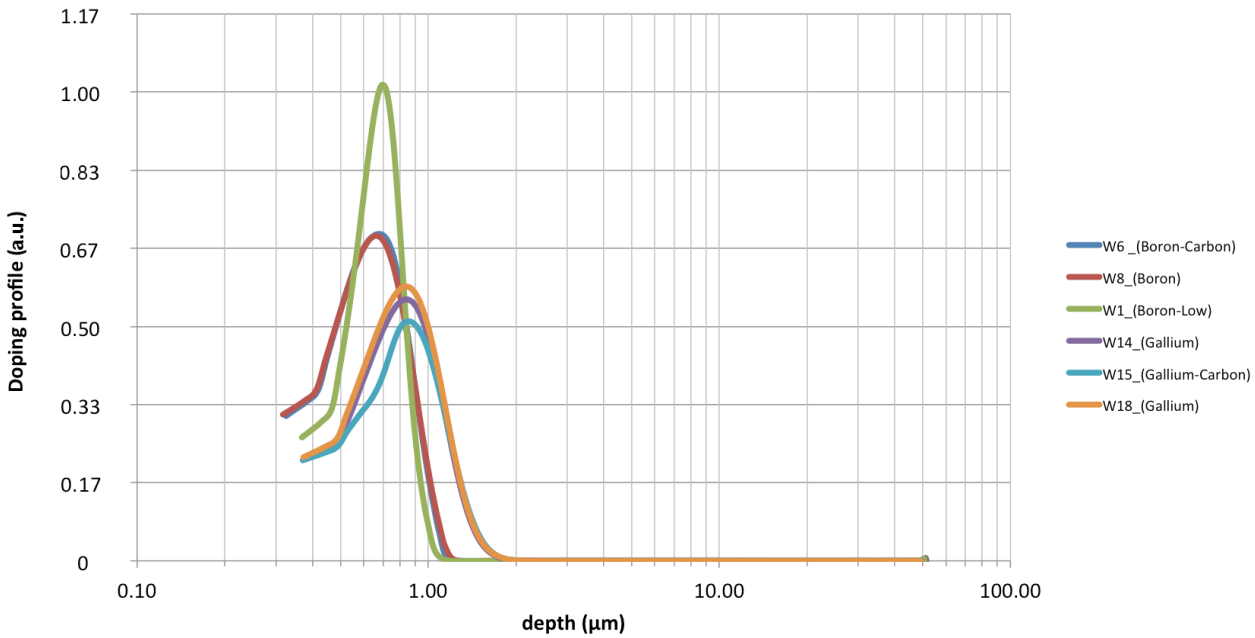
As-implanted boron (low diffusion) → steeper gain curve, only at lower doses

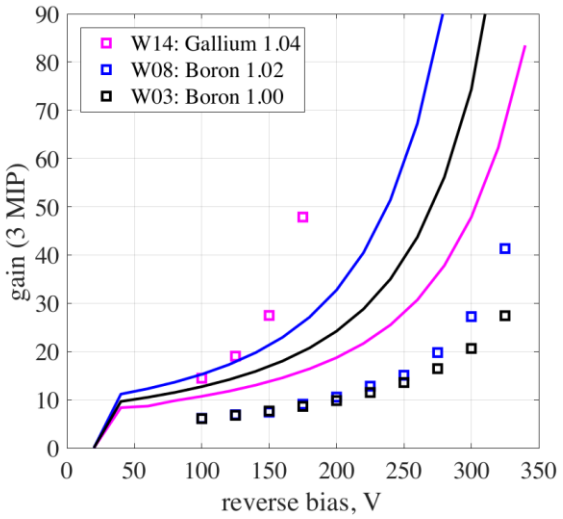


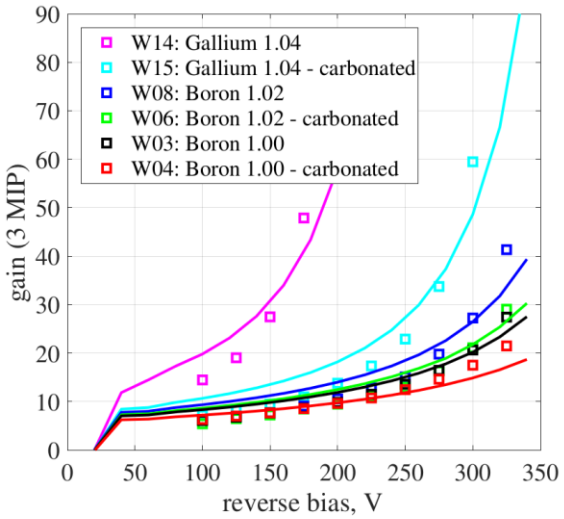


50 um – outcome

- Extraction of gain layer doping concentration from CV measurements
- Comparison between measurements and simulations





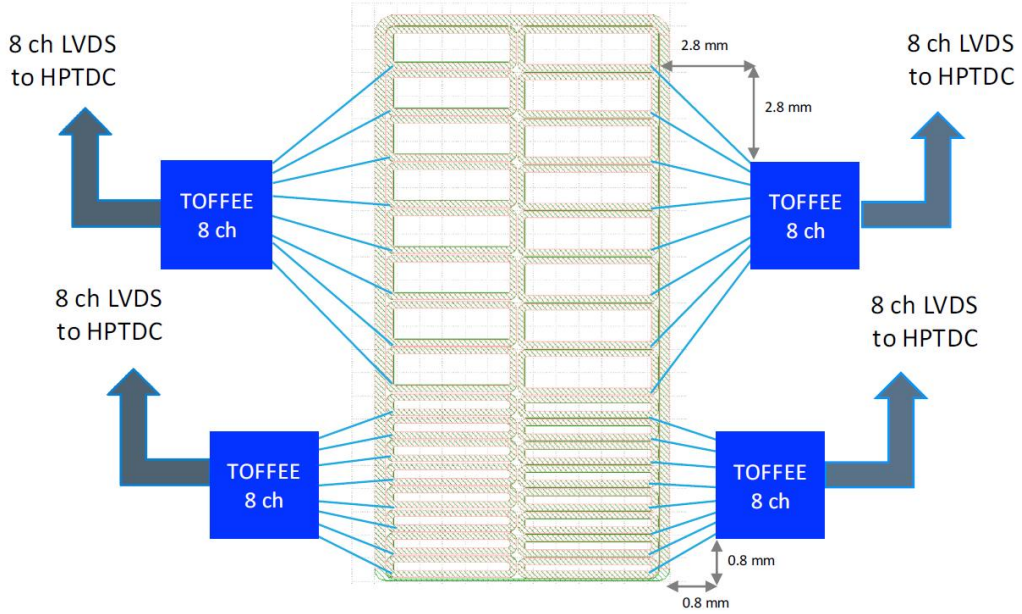


TOFFEE - overview

TOFFEE is designed in UMC 110 nm CMOS technology for CT-PPS

The ASIC has 8 channels, each channel consists of:

- Trans-Impedance Amplifier
- Single threshold discriminator
- Delay line
- LVDS driver for HPTDC interfacing



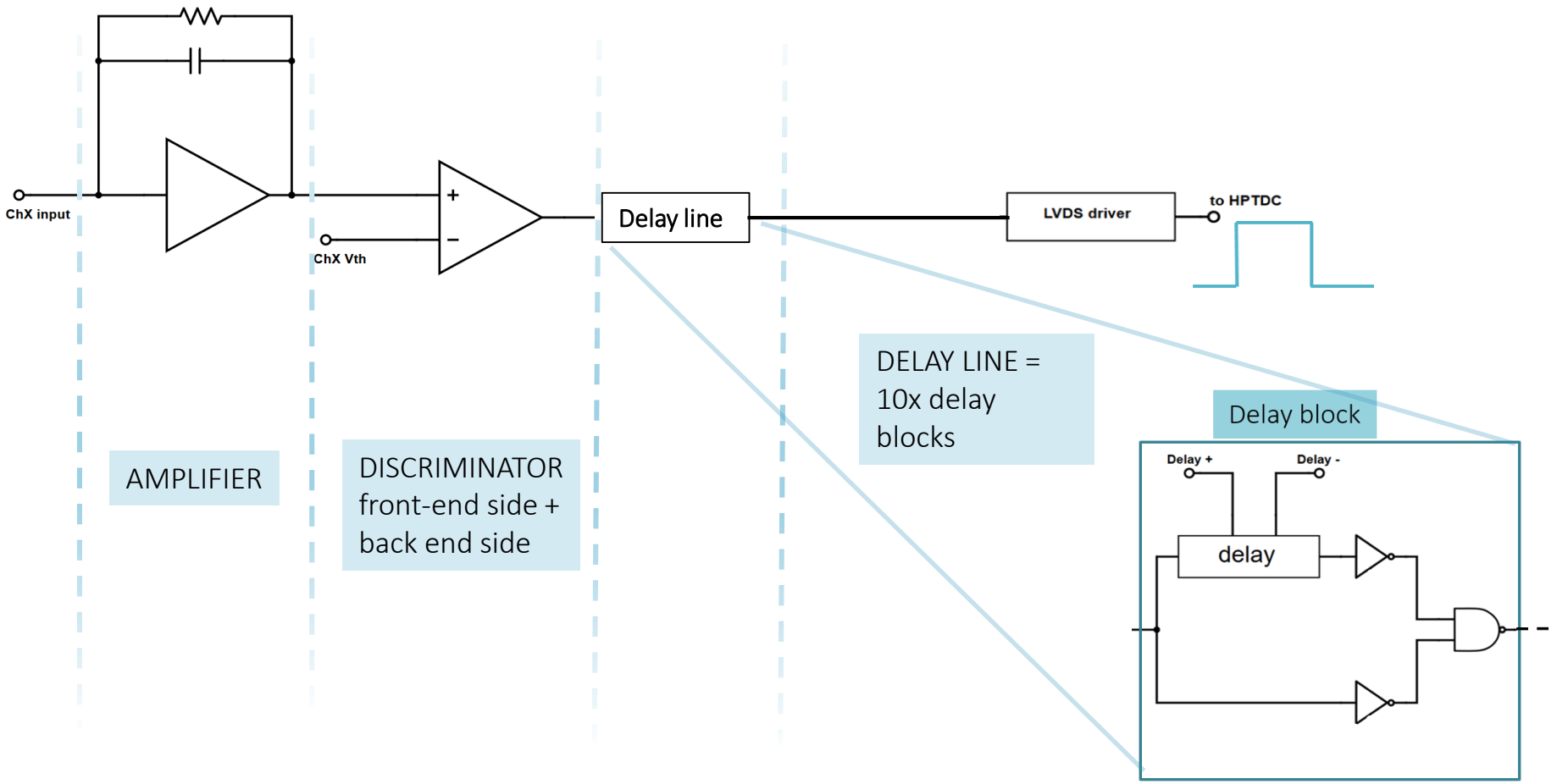
It is optimized for a sensor capacitance of 3-6 pF and an input charge between 3 fC and 30 fC

The output is sent out of the roman pot to the existing HPTDC board through LVDS links (32 pairs per detector module) for Time of Arrival (ToA) and Time Over Threshold (ToT) measurements

To read out a CT-PPS UFSD minimizing wire-bond length → 4 TOFFEEs

The chip has been submitted to foundry in May 2016, tests started in October 2016

TOFFEE – signal processing chain



TOFFEE – specifications

Linear dynamic range: 3 fC – 30 fC

Amplifier gain: ~ 7 mV/fC

GBW: 14 GHz

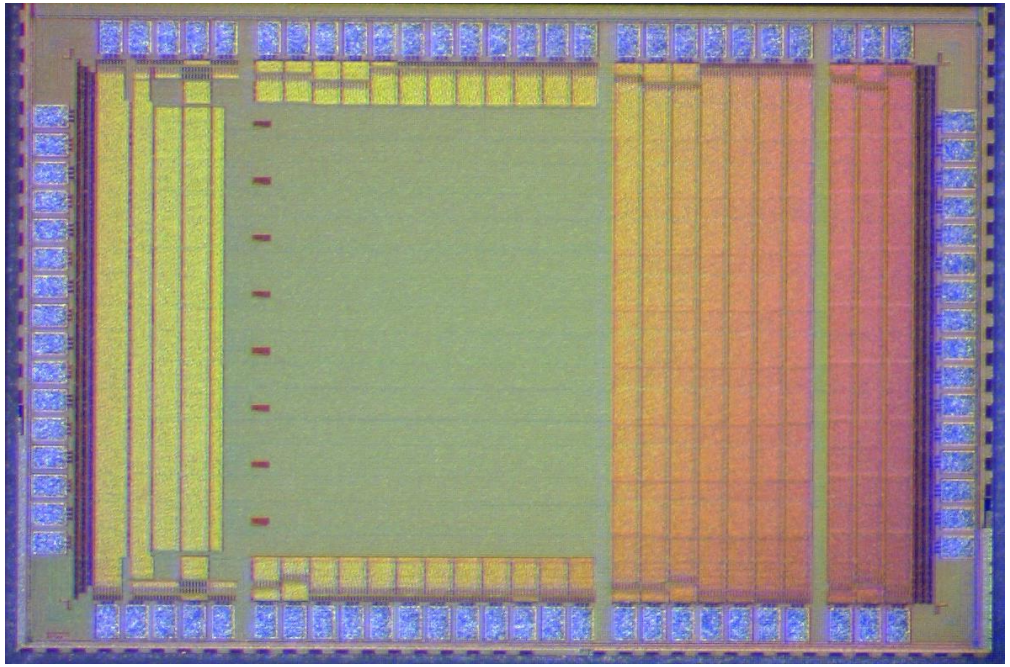
RMS noise at Cdet= 3 pF: 0.6 mV

Delay line: adds 5 ns offset to discriminator signal width (4 – 10 ns)

Power consumption: ~ 30 mW per channel

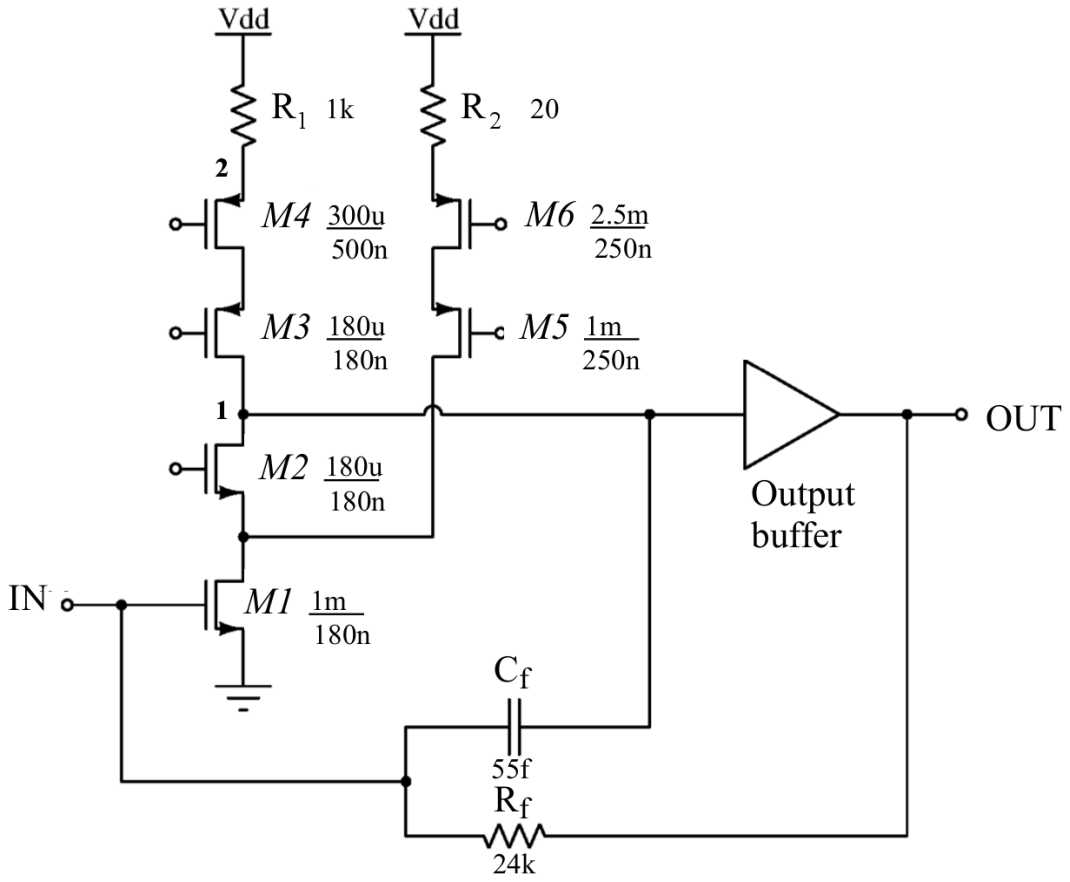
AVDD: 1.2V

DVDD IO: 2.5V

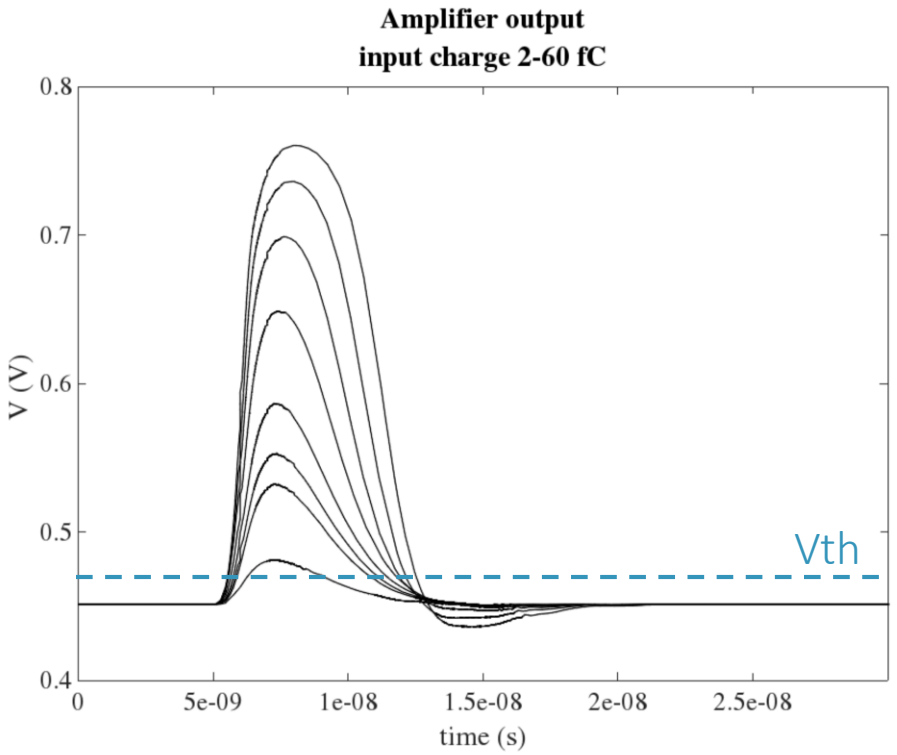


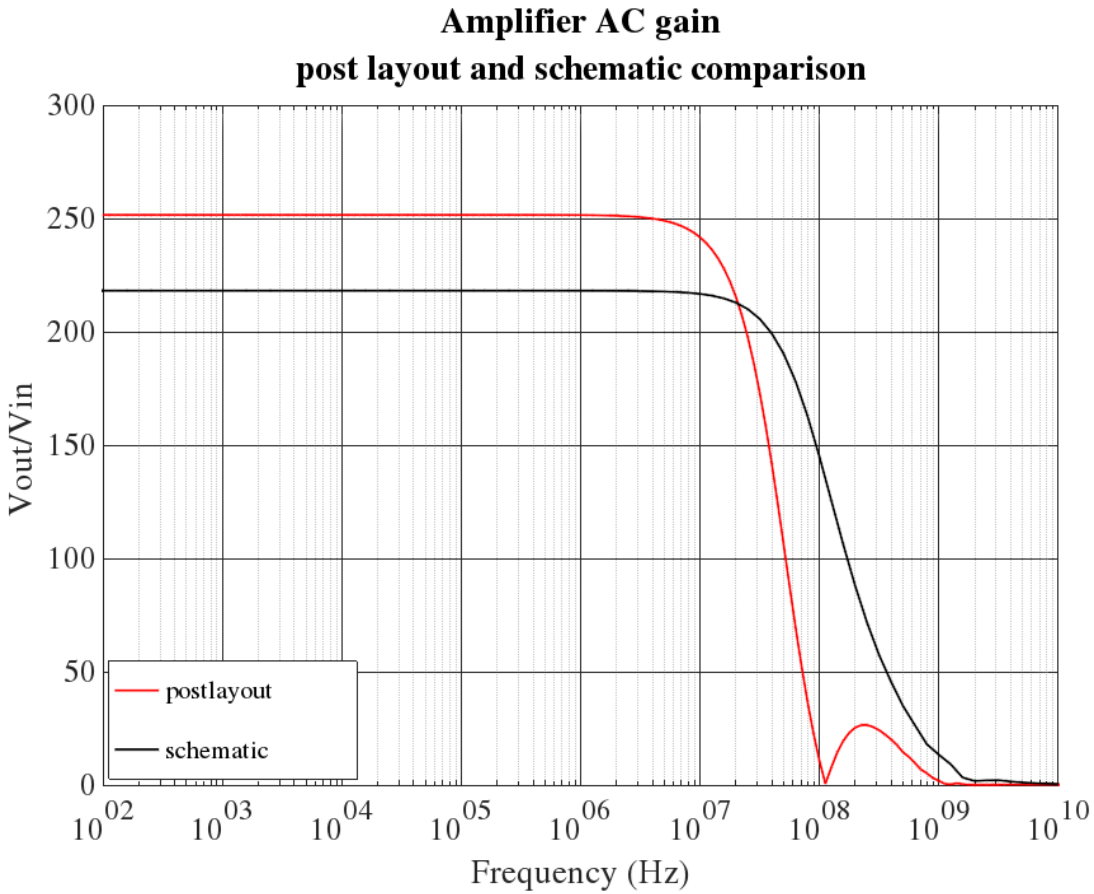
Amplifier architecture

- Telescopic cascode common source amplifier with split current source
- Right branch injects a high current (12 mA) in the input transistor and increases its transconductance
- Resistors for noise shielding
- Output buffer for load driving: increases the bandwidth of the transimpedance gain



Amplifier signal and transfer function





~ 2 ns peaking time

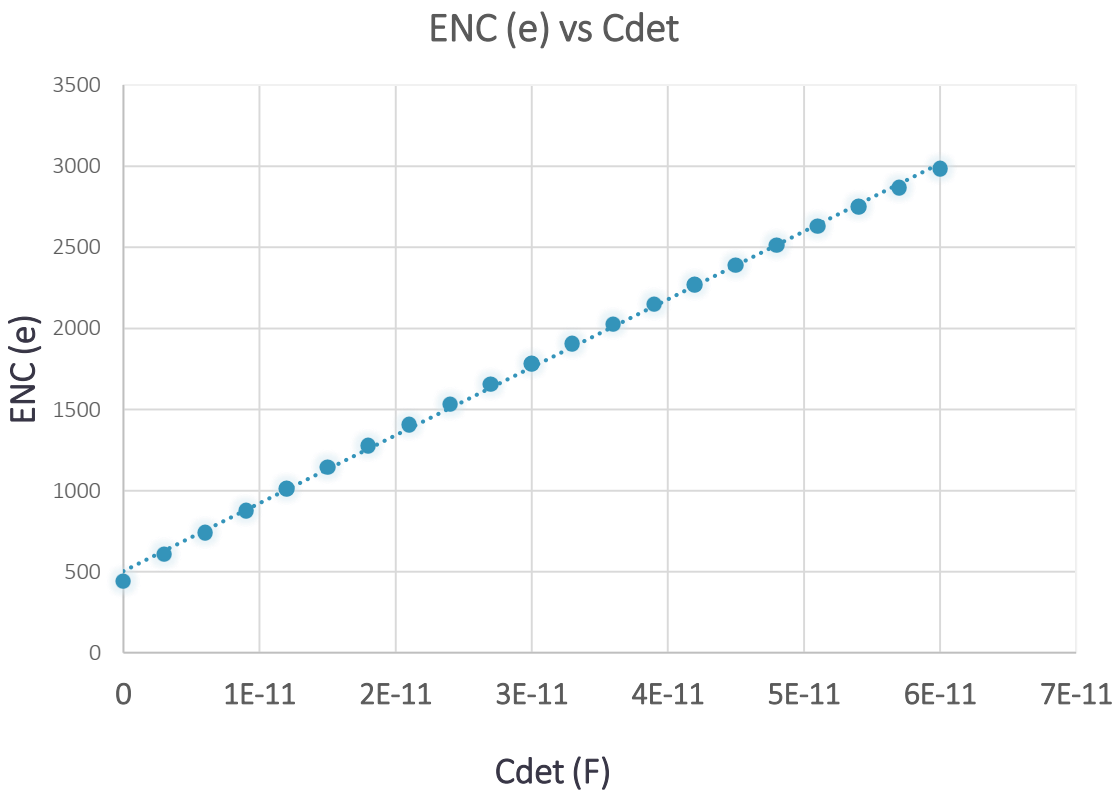
Leading edge discriminator:

→ **time walk** errors rise from signal amplitude variations

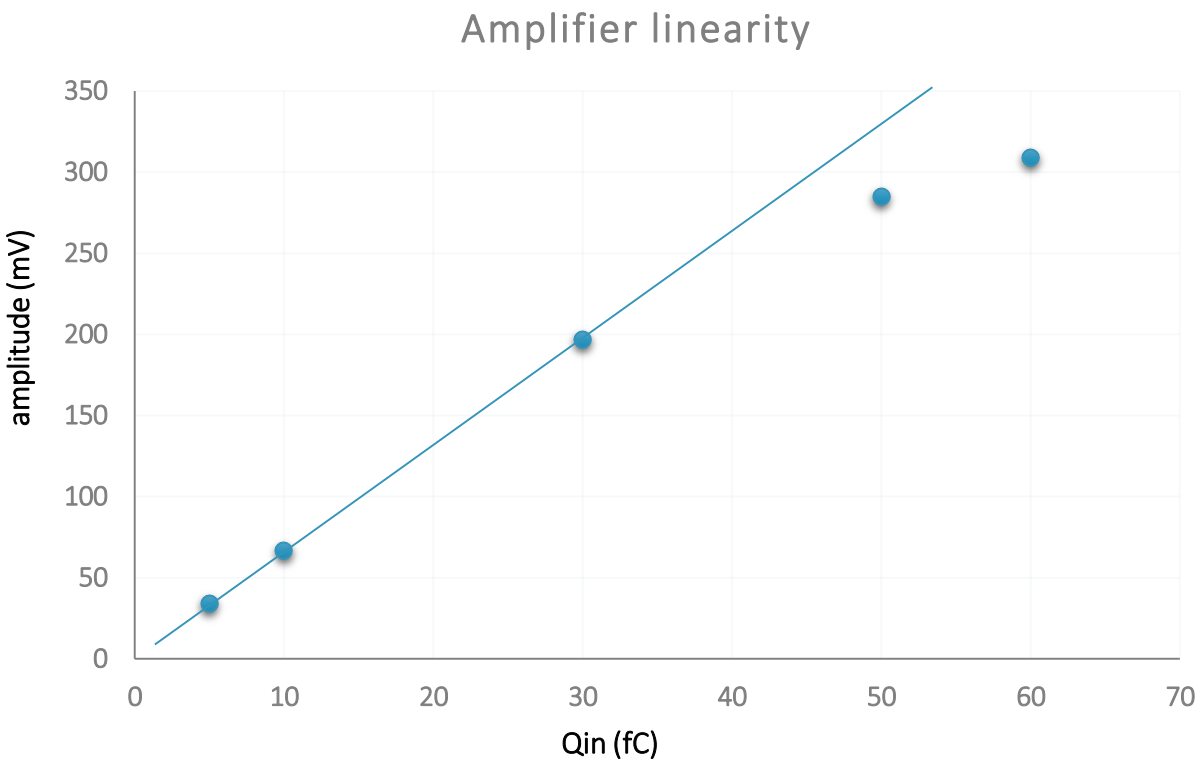
→ ToT for time walk correction

Amplifier noise curve and linearity

Simulated amplifier output noise as a function of detector capacitance



Amplifier gain linearity as a function of input charge

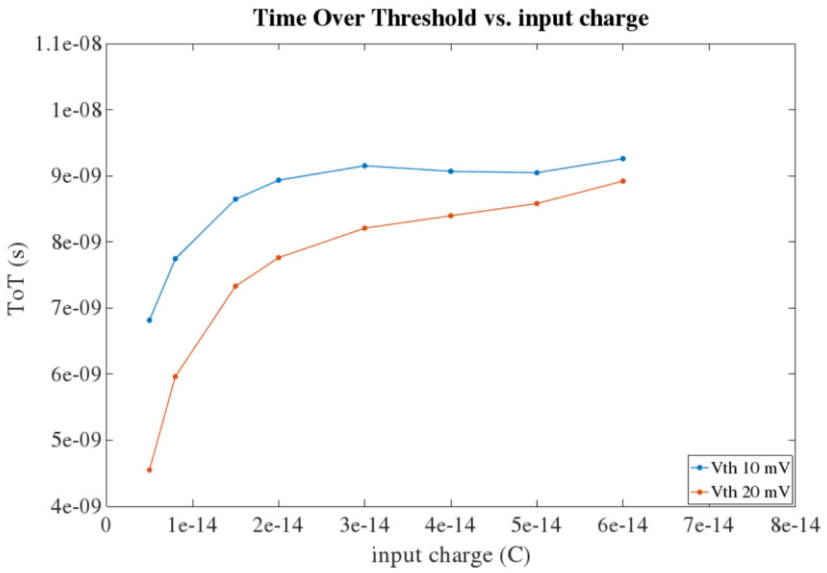


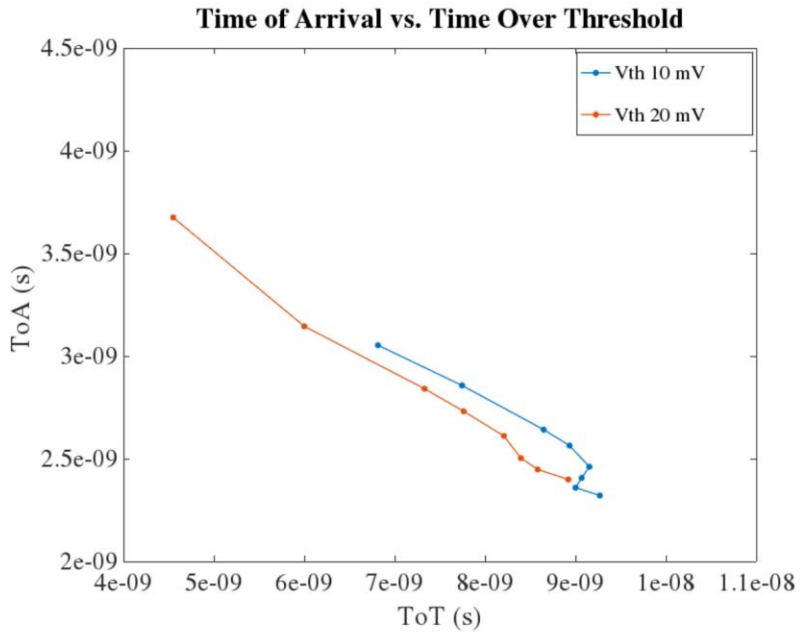
Time Over Threshold

ToT has logarithmic dependence on the input charge at nominal working conditions (3-30 fC) and before amplifier saturation

ToT vs input charge losses monotonicity at high input charges and low threshold voltages

→ time walk correction (ToA vs ToT) is limited by ToT monotonicity





Simulated time resolution

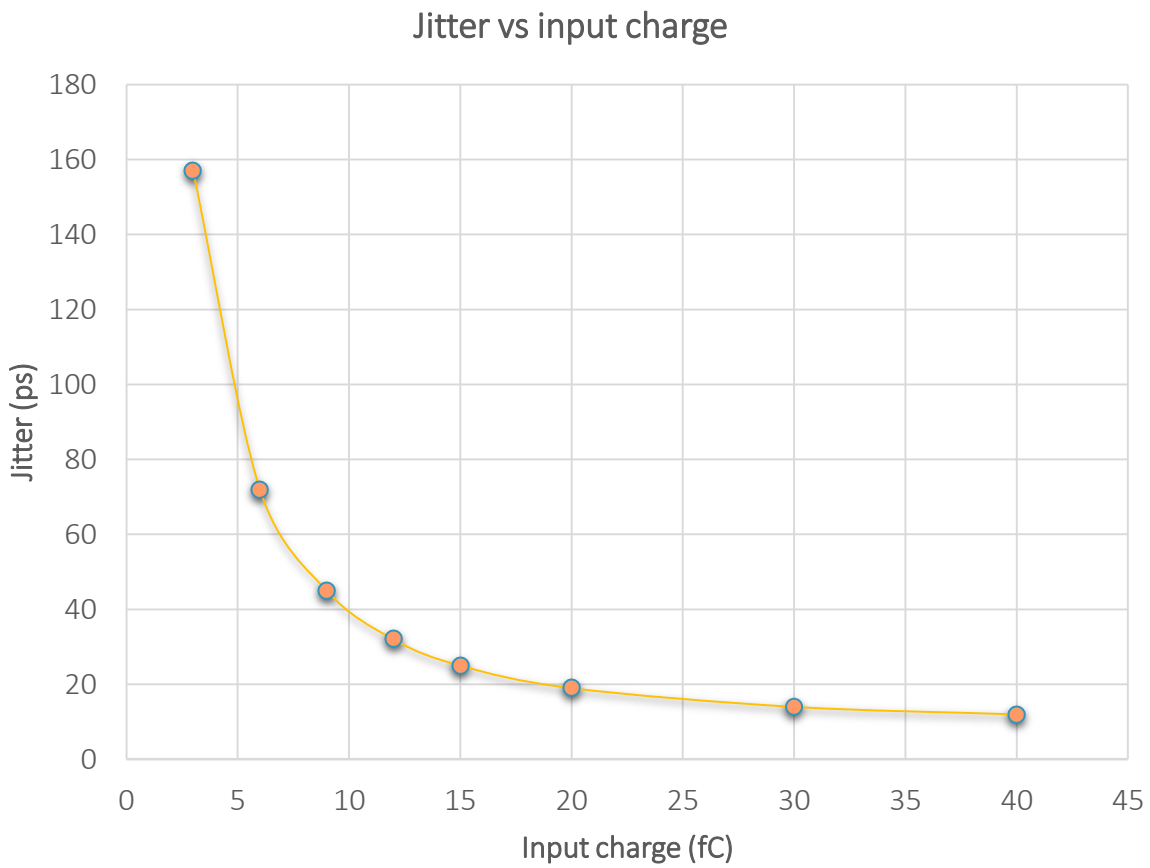
Jitter (σ_{ToA}) estimation as a function of input charge from post layout simulations

A time resolution of ~ **45 ps** is expected for **1 single detector + readout module** for a MIP signal (~ 8 fC)

Time resolution can be further improved by putting more planes in parallel, e.g. for 4 planes

$$\sigma_t = \frac{jitter}{\sqrt{N\ planes}}$$

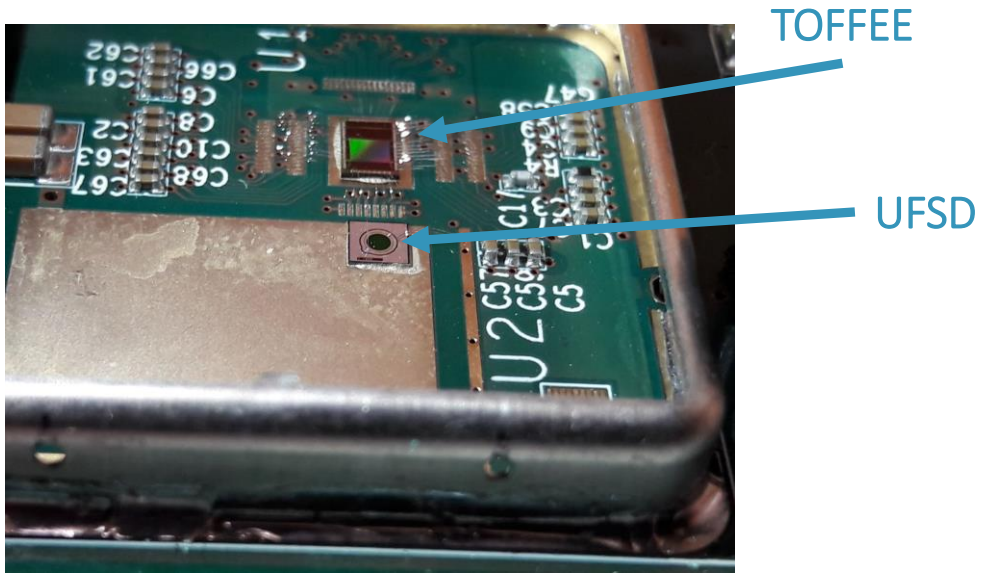
~ 22 ps

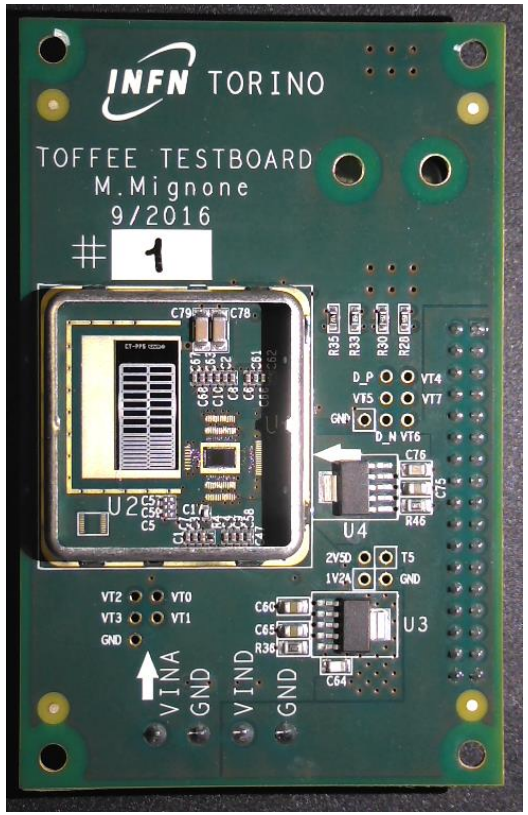


TOFFEE+UFSD: experimental results

Tests on TOFFEE + 50 um HPK UFSD (~ 3.5 pF capacitance), 2 boards

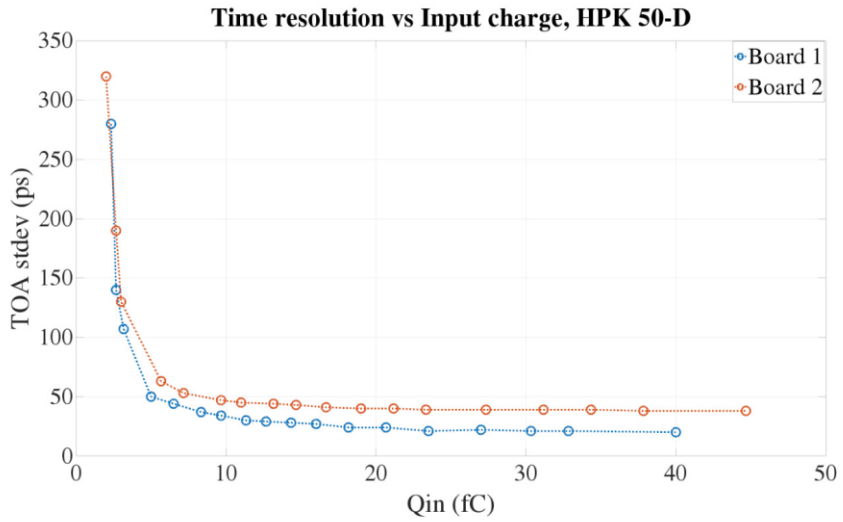
- Laboratory tests with laser (λ = 1060 nm)
  - Readout with differential probe + oscilloscope
- Beam tests (CERN SPS, 180 GeV pions)
  - Readout with differential probe + oscilloscope
  - Readout with HPTDC

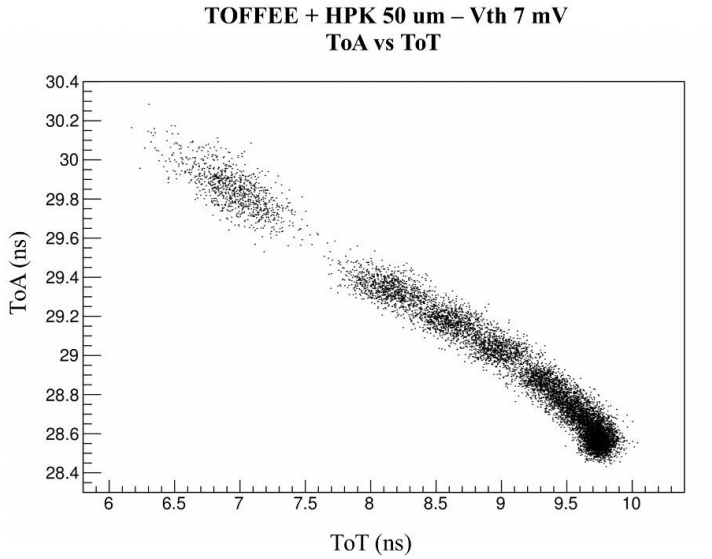




Laboratory tests

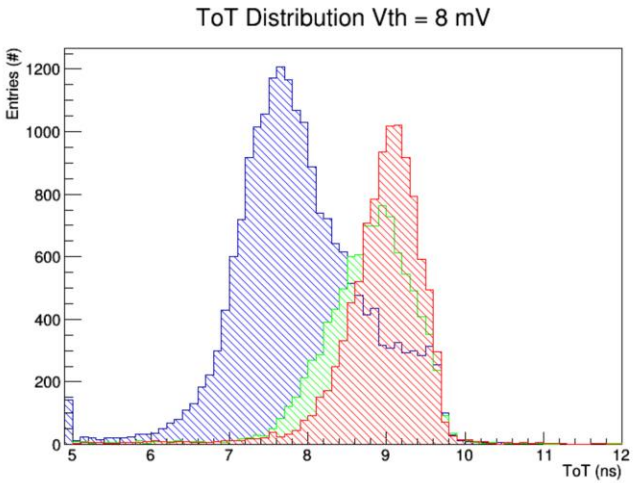
- Laser beam hits the sensor and produces the signal
- Input charge evaluated from amplifier signal amplitude (threshold scan)
- Time of Arrival = delay between trigger (from laser) and LVDS signal
- Time resolution as a function of input charge, discriminator threshold = 7 mV
  → ~ 50 ps for an input charge ~ 8fC
- Time Over Threshold = width of LVDS signal at half height



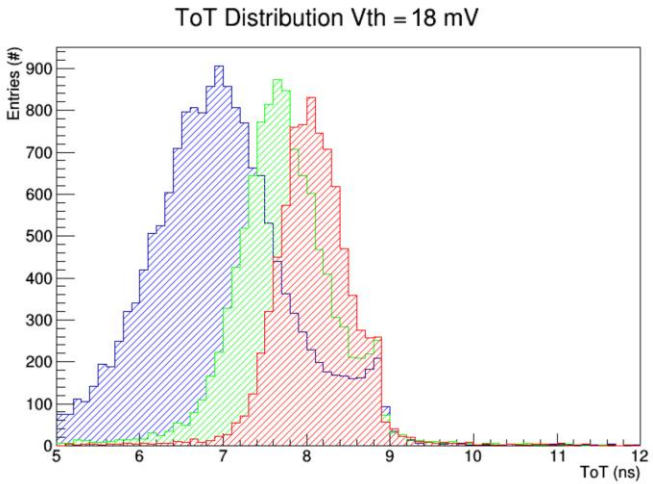


Beam tests – oscilloscope readout

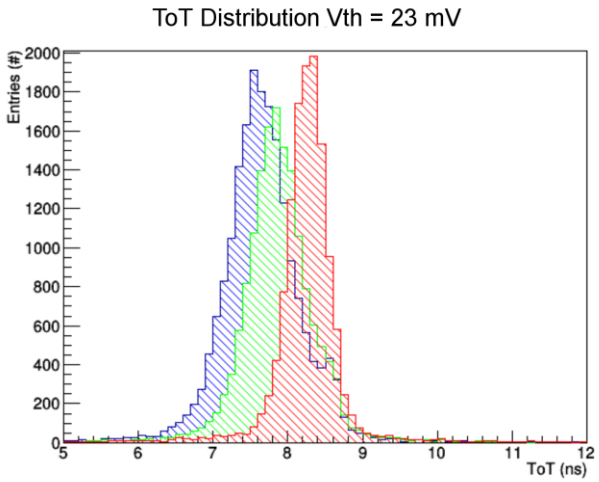
ToT distribution at different threshold values and sensor bias voltages



Vbias = 170 V, 230 V, 250 V



Vbias = 230 V, 270 V, 290 V



Vbias = 290 V, 300 V, 320 V

ToT should follow a Landau distribution, but high Vth and Vbias the energy information is lost
ToT **logarithmic behavior** with input charge confirmed: saturation at ~ 10 ns (Vth= 8mV), ~ 9 ns (Vth= 18, 23 mV)

Beam tests – oscilloscope readout

2-boards telescope, coincidence between the two sensors

Difference in time of arrival:

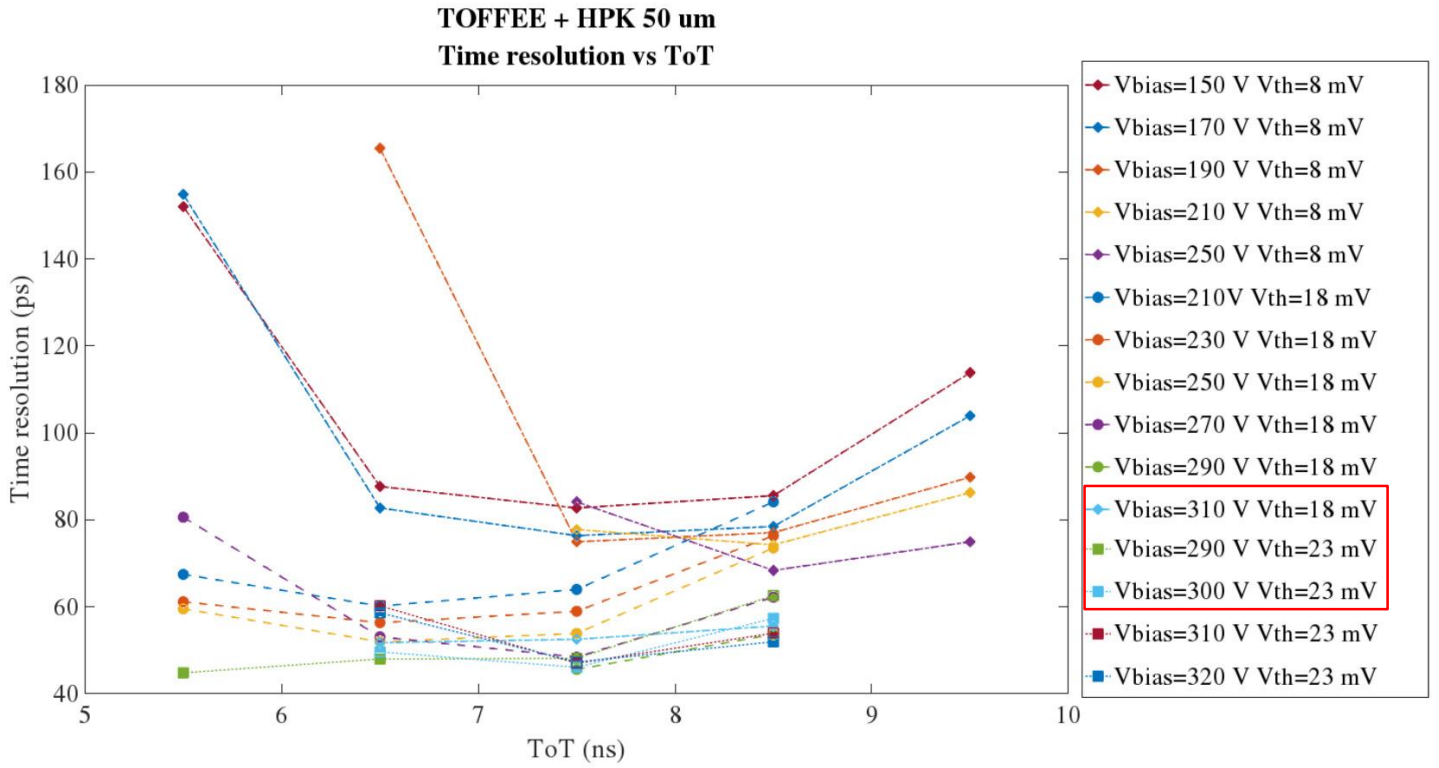
$$\Delta ToA = ToA_2 - ToA_1$$

Time resolution of a single board:

$$\sigma_{t,1\ board} = \frac{\sigma_{\Delta ToA}}{\sqrt{2}}$$

Time resolution (single channel) as a function of ToT, oscilloscope readout

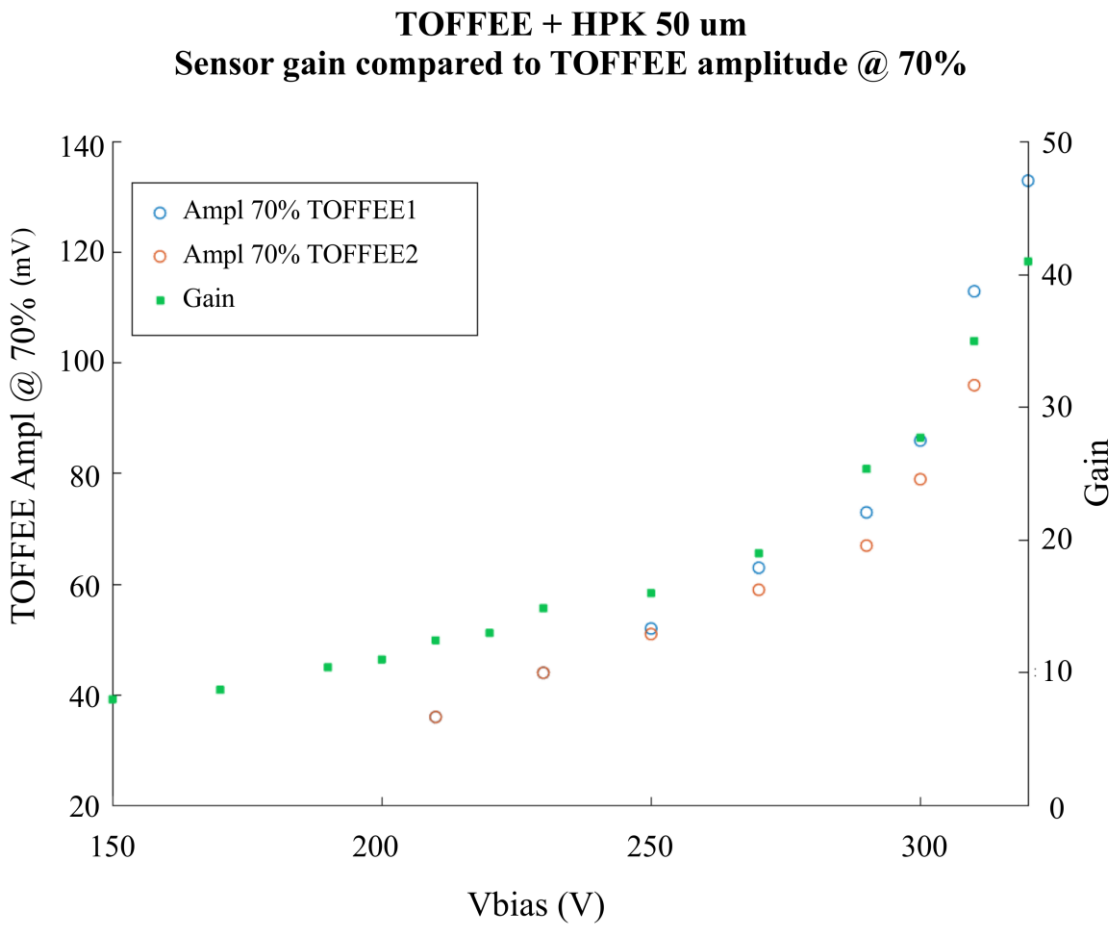
→ better time resolution at higher thresholds



Beam tests – oscilloscope readout

Estimation of amplifier gain:

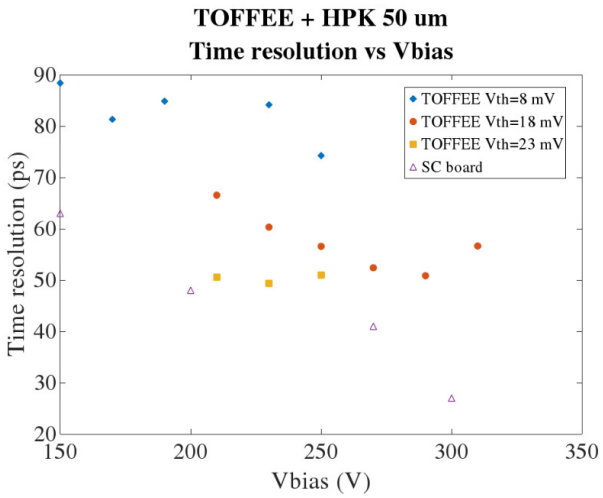
- Sensor gain is known from gain curves
- Charge deposited by a MIP in 50 um silicon = 0.46 fC
- Acquire events in Δt at low Vth
- Increase Vth to acquire 70% of the events in Δt → MIP
- Increase Vbias → gain curve

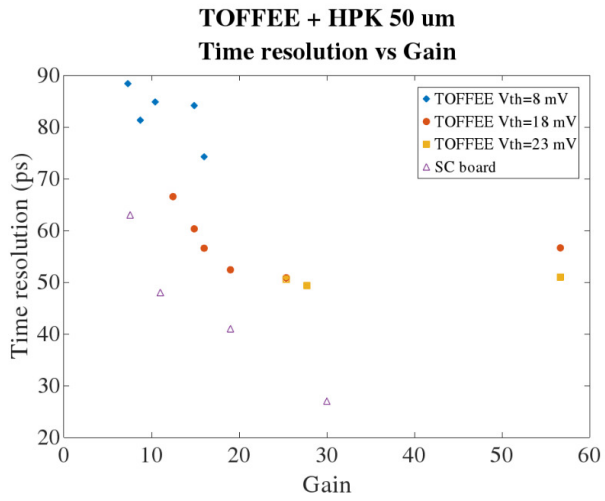


➡ TOFFEE gain ~ 6-7 mV/fC

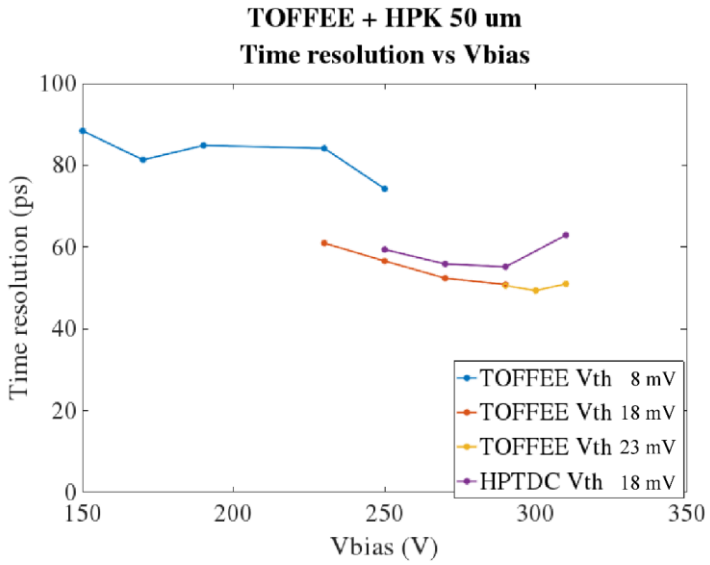
Beam tests – comparison

Comparison between UFSD + TOFFEE at different threshold values and UFSD + SC board





Comparison between UFSD + TOFFEE at different threshold values, oscilloscope and HPTDC readout



Time resolution achieved with HPTDC is compatible with expected TDC contribution: best value = **55 ps** → 27 ps for 4 planes

Conclusions

My PhD work involved the following activities:

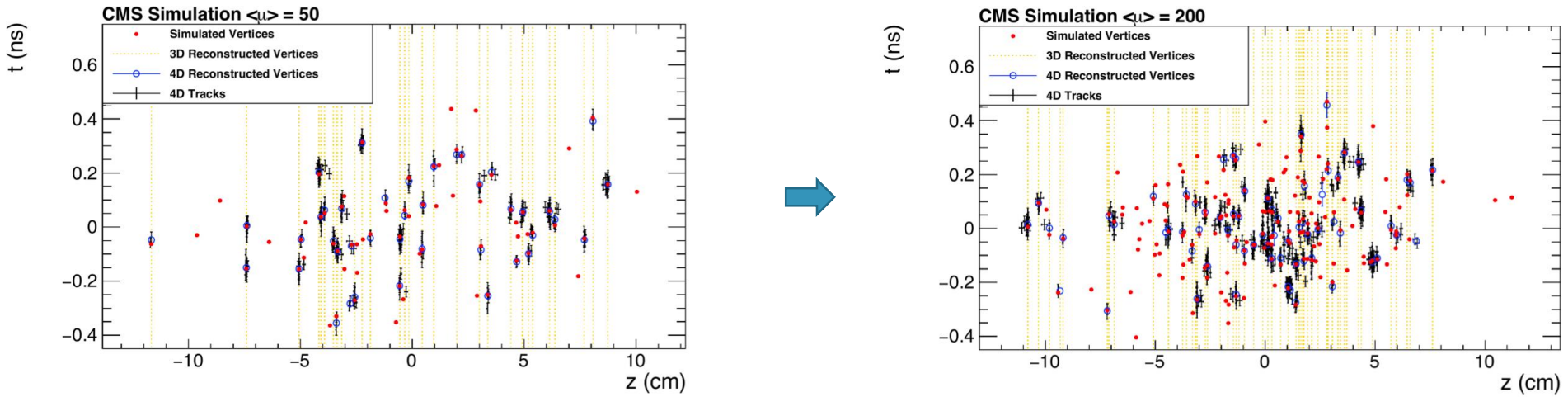
- Simulation of UFSD sensors in collaboration with FBK: 2 productions (275 um, 50 um)
- Development of an integrated readout electronics for UFSD: TOFFEE
- Characterization of sensors and electronics

- UFSD are a good option as timing detectors for modern high energy physics experiments
- The expected time resolution for a 50 um thick UFSD is ~ 30 ps (confirmed by beam tests)
- The TOFFEE ASIC coupled with UFSD reaches a time resolution of ~ 50 ps

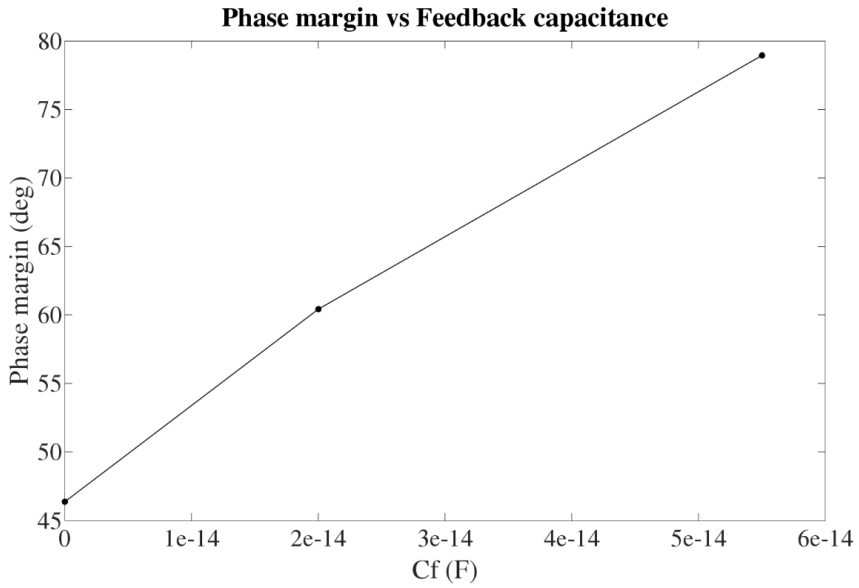
Backup

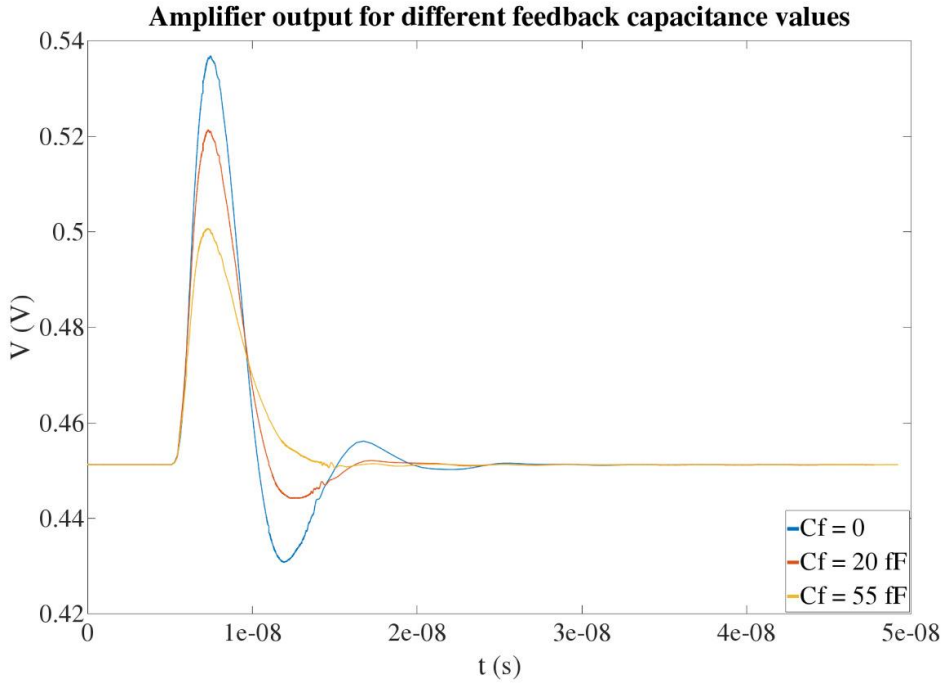
CMS timing upgrade

Reconstruction of pileup vertices in position and time within a bunch crossing



Amplifier – feedback capacitance





Amplifier – behavior at high charges

Non-monotonic ToT behavior: falling edge for high charges crosses threshold before smaller signals