Front-end electronics in 65nm CMOS technology for the HL-LHC upgrades

Torino graduate school in Physics and astrophysics - XXIX cycle

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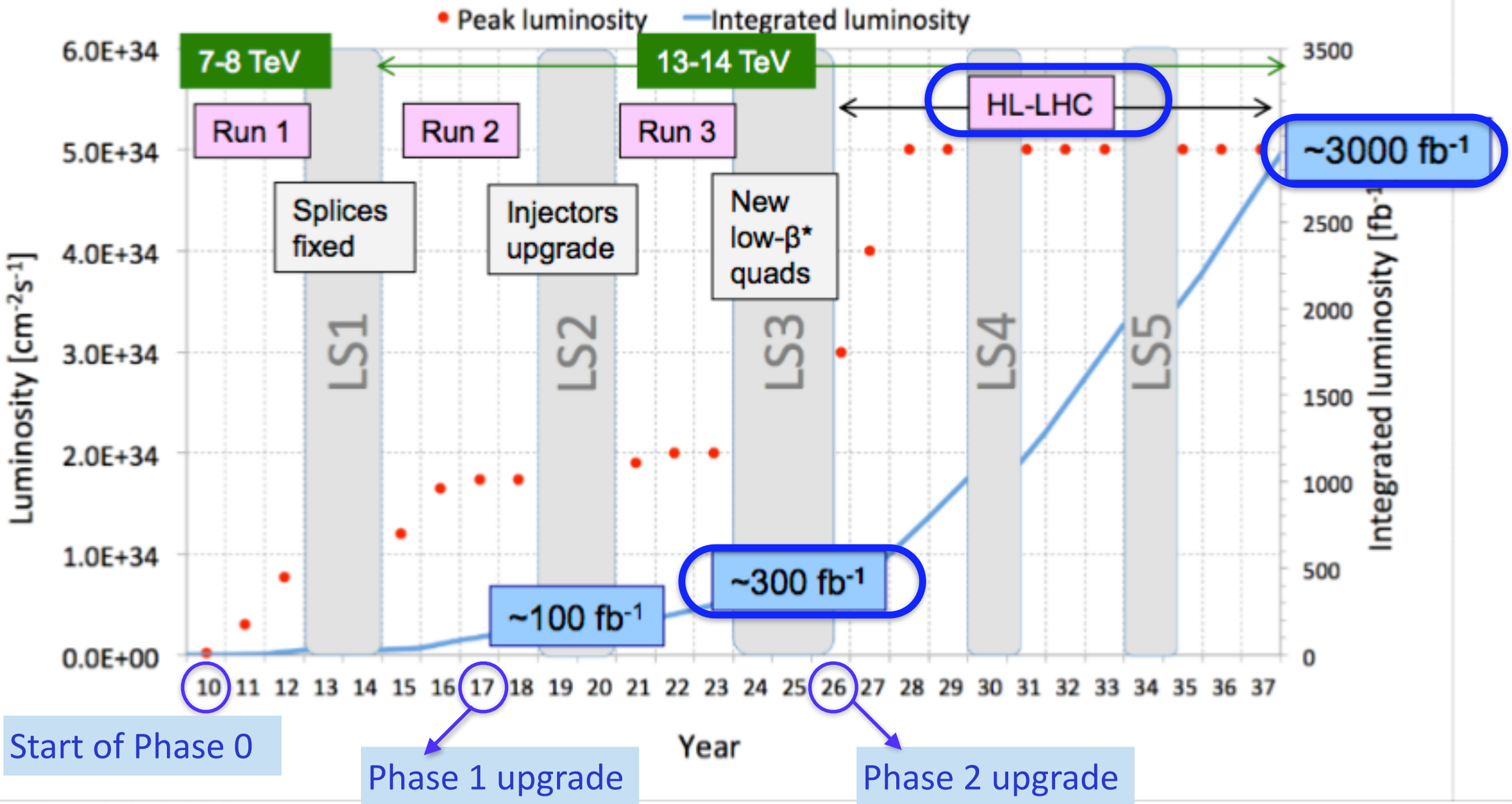
Outline

- The Phase 2 upgrade of the silicon pixel detectors of HL-LHC experiments
- Readout chip specifications
- Synchronous analog front-end architecture
- Measurements and irradiation test on small prototypes
- CHIPIX65 and RD53A demonstrator chips
- Conclusions

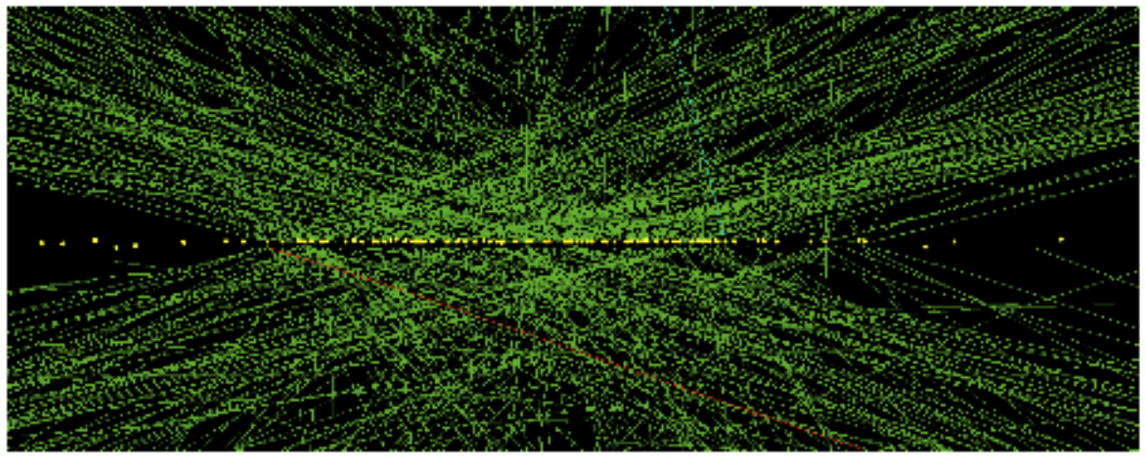
The HL-LHC upgrade



- During HL-LHC:
  - The integrated luminosity of the machine will be increased by an order of magnitude between Phase 1 and 2 (**3000 fb^{-1} foreseen**)
  - Unprecedented Pile-Up conditions (**140-200 collisions per event**)
  - Unprecedented radiation levels (around **1 Grad in 10 years** in the innermost layers)

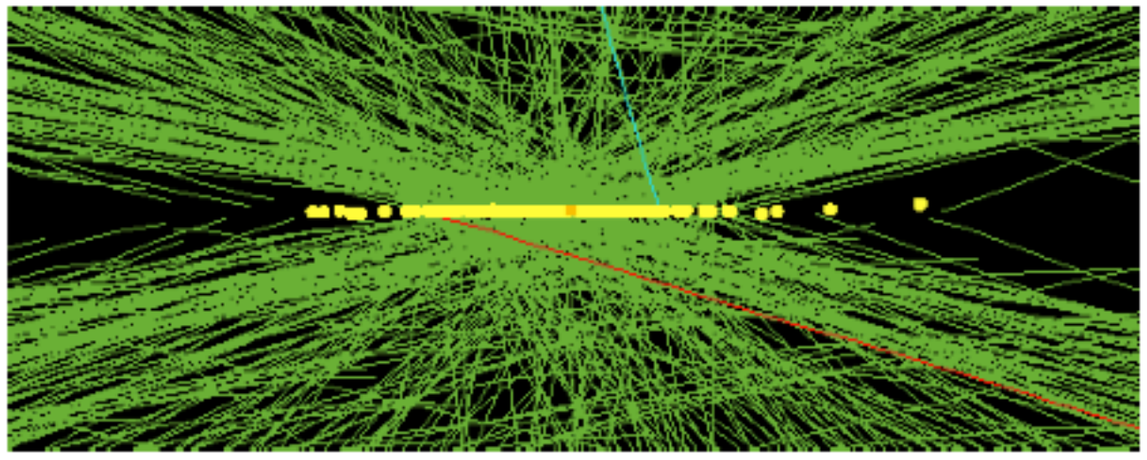
Pile-Up

LHC Phase 1



2×10^{34} cm^{-2} s^{-1}
7 TeV/beam p-p
PU 50
25 ns BX

LHC Phase 2



$5\text{-}7.5 \times 10^{34}$ cm^{-2} s^{-1}
7 TeV/beam p-p
PU 140-200
25 ns BX

- The foreseen HL-LHC upgrade will introduce unprecedented operating conditions in terms of track densities (5x Phase0) and radiation levels (10x Phase0+1)

Phase 2 physics motivations

- **2012: discovery of the Higgs boson!**

- **Now the Higgs sector must be further investigated**:
  - Higgs coupling and property measurements
  - Di-Higgs searching
  - Vector Boson Scattering (VBS)
  - Rare decays

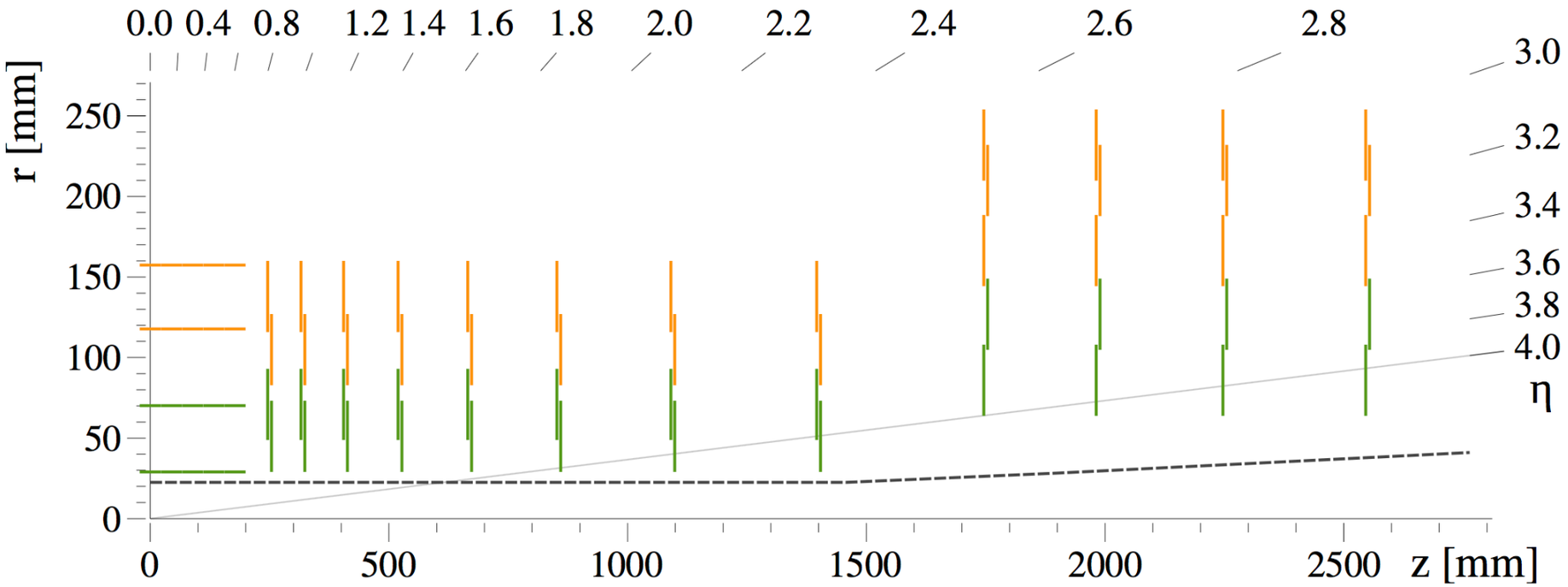
- **Exotic searches**

- **Standard Model measurements**:
  - B physics
  - Precision measurements
  - Rare processes, enhanced by Beyond Standard Model
  - Differential measurements of W, Z, di-boson, top

Phase 2 pixel detector upgrade

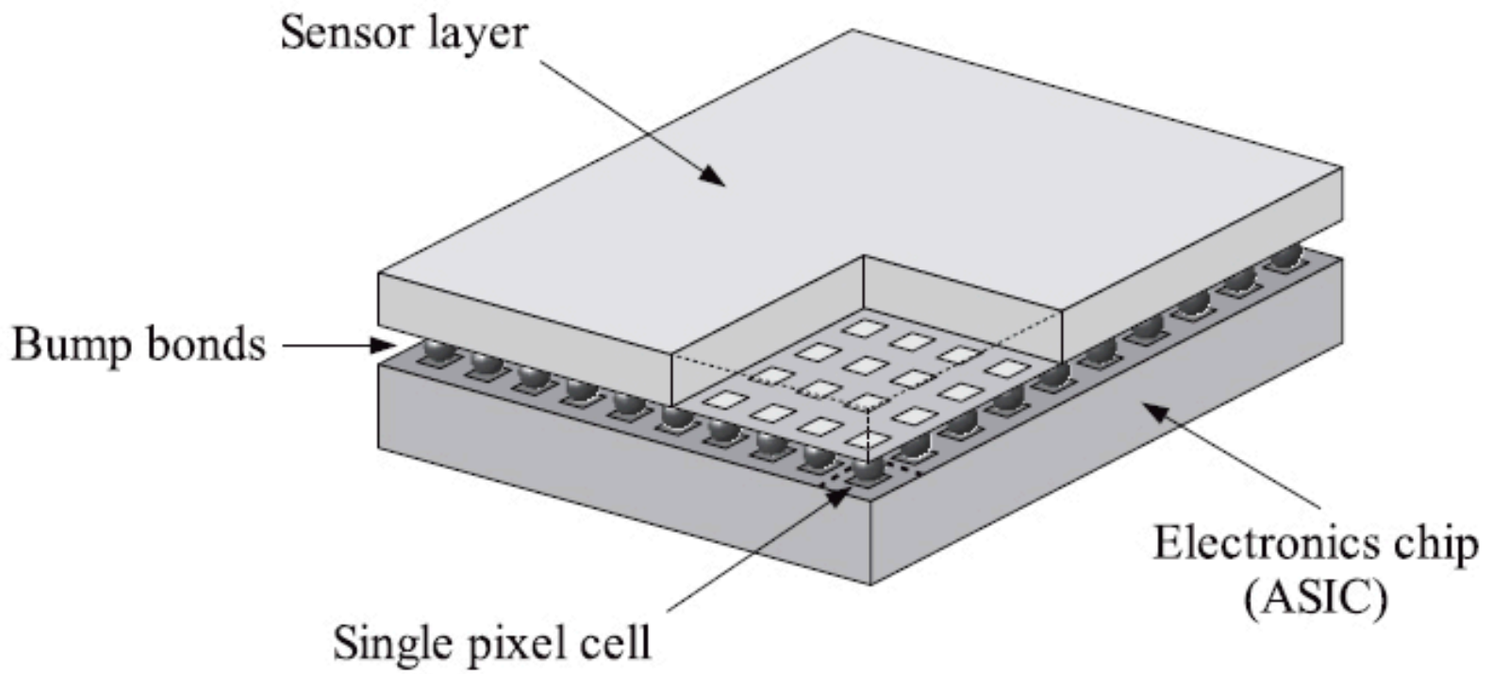
- Goal:
  - **Maintain or improve the tracking and vertexing capabilities** under the high pileup conditions of the HL-LHC
- How it is achieved:
  - **A narrower pitch** than the present pixel detector, for better transverse and longitudinal impact parameter resolution
  - Capability to withstand the **demanding hit rates and radiation environment** with negligible inefficiencies
  - **Simple installation and removal** to allow for a potential replacement of parts suffering from radiation induced effects

- CMS Phase 2 pixel detector layout
- Inner radius
  - 30 mm
  - Fluence of 2.3×10^{16} n_{eq}/cm^2



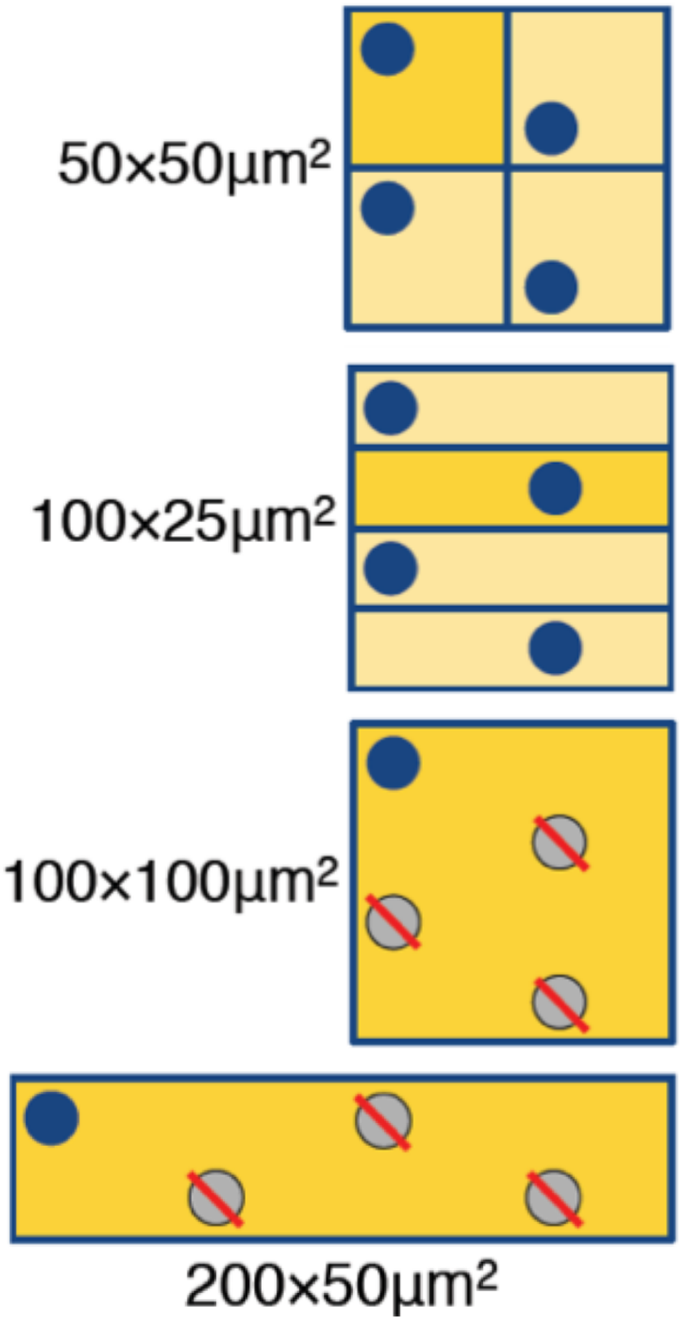
Hybrid pixel detectors

- The pixel detector will be based on the **hybrid pixel** technology
- It allows **separate production of sensors and electronics**
- The pixels on the two sides are then connected through the **bump-bonding** technique, consisting in a metal deposition between the sensor output and the electronics input



Pixel detector design

- **Improvement in granularity → Reduction of the pixel size**
  - It allows to maintain the same occupancy with respect to the present detector
  - Cell dimensions 50x50 μm^2 or 100x25 μm^2
  - Chip size 50x50 μm^2
  - Staggered bumps to make different sensor sizes (for example 100x100 μm^2 or 200x50 μm^2 which will be used for the outer layers) compatible with the same chip



Silicon sensors

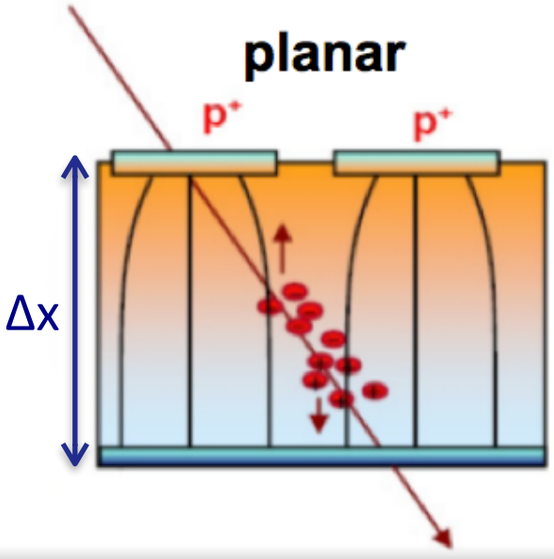
- **Radiation hardness** is a key parameter for Phase 2 sensors:
  - Particle fluence ~2×10^{16} n_{eq}/cm^2 expected in the innermost layer
  - Choice between planar and 3D has not yet been taken: important to design a front-end electronics compatible with both solutions

PLANAR

- Thinner thickness to reduce the charge loss due to trapping

  $100\ \mu m < \Delta x < 200\ \mu m$

- HV>>100 V for fluence >5×10^{15} n_{eq}/cm^2

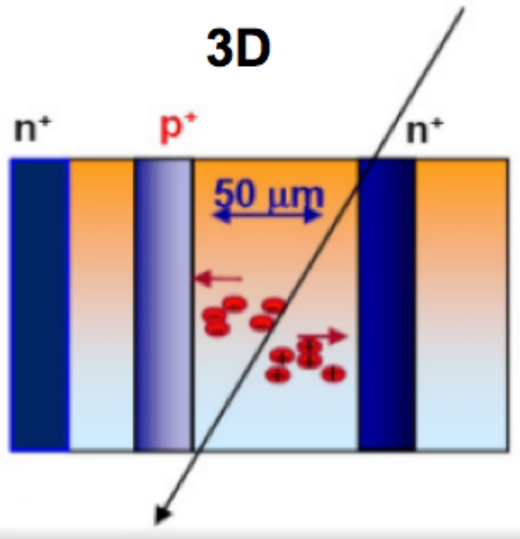


For a 50x50 μm^2 configuration:

- C ≃ 50 fF (dominated by inter-pixel contribution)
- $I_{leak} \lesssim 10$ nA @ -20 °C

3D

- Intrinsically more radiation hard
- Lower depletion voltage
- Due to higher costs usage probably limited to the inner layers



For a 50x50 μm^2 configuration:

- C ≃ 50-80 fF (dominated by p^+-n^+ capacitance)
- $I_{leak} \lesssim 10$ nA @ -20 °C

Motivations for a new readout chip

- **Radiation hardness**
  - The present chip can not survive the extreme Phase 2 conditions
- Very **high pixel hit flux** (3 GHz/cm^2 for the innermost layer)
- **Smaller pixel size** (chip → 50x50 um^2)
- **Low power architecture**
  - Required in order to maintain the material budget as low as possible
  - Around 10 μW per pixel (analog + digital)

Pixel chip specifications

PARAMETER/FEATURE	PHASE 0	PHASE 1	PHASE 2
PIXEL SIZE	100x150 μm^2	100x150 μm^2	50x50 or 100x25μm^2
SENSOR THICKNESS	2D, 285 µm	2D, 285 µm	thin 2D, 3D
PIXEL HIT RATE	100 MHz/cm^2	400 MHz/cm^2	2-3 GHz/cm^2
TRIGGER RATE	100 kHz	100 kHz	1 MHz
READOUT RATE	40 Mb/s	400 Mb/s	~2 Gb/s
RADIATION	15 Mrad	120 Mrad	1 Grad
TECHNOLOGY	250nm CMOS	250 nmCMOS	65nm CMOS
ARCHITECTURE	Analog	Digital	Digital
POWER	~0.3 W/cm^2	~0.3 W/cm^2	~0.5 W/cm^2

Why CMOS 65nm?

- **Radiation tolerance** increases with technology scaling thanks to a thinner gate oxide

- **More digital functionalities in a smaller area:**
  - Local storage during trigger latency + trigger matching

- **Improved speed** (~GHz)

- **Low power**
  - 1.2 V supply voltage (same as 130nm, halved wrt to 250nm)
  - Digital cell power consumption → 1/8 wrt to 250nm

- **Mature technology**
  - Introduced in 2006 in industry
  - Novel technology for HEP
  - Long-term availability guaranteed (OK for 2024-2025)

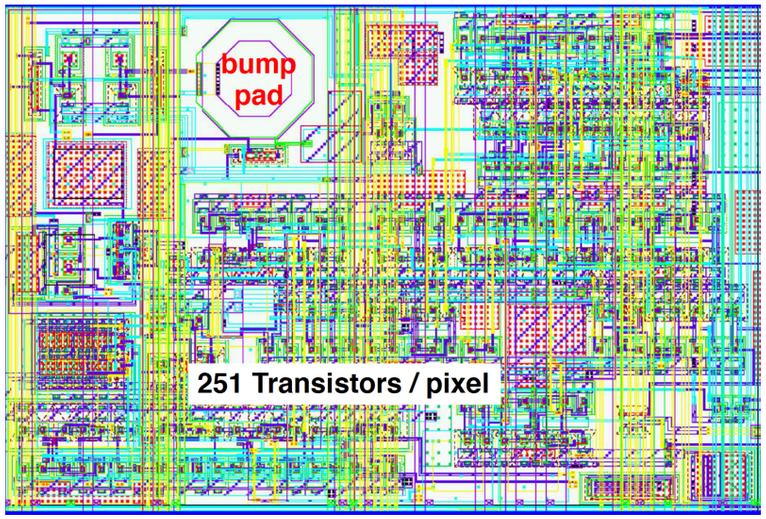
Design communities on 65nm Phase 2 pixel chip

- **RD53 collaboration** at CERN, a joint CMS-ATLAS effort approved in 2013 by LHCC
  - Common technology qualification
  - Around 20 institutes from different countries involved
  - Important INFN contribution
  - Submission of the RD53A demonstrator chip in 2017

- **CHIPIX65**: approved by CSN5 in October 2013
  - Italian CMS/ATLAS groups involved
  - 8 INFN groups (Bari, Bergamo/Pavia, Lecce, Milano, Padova, Perugia, Pisa and Torino)
  - Small prototypes submissions during 2014 and 2015
  - Demonstrator chip submission in July 2016

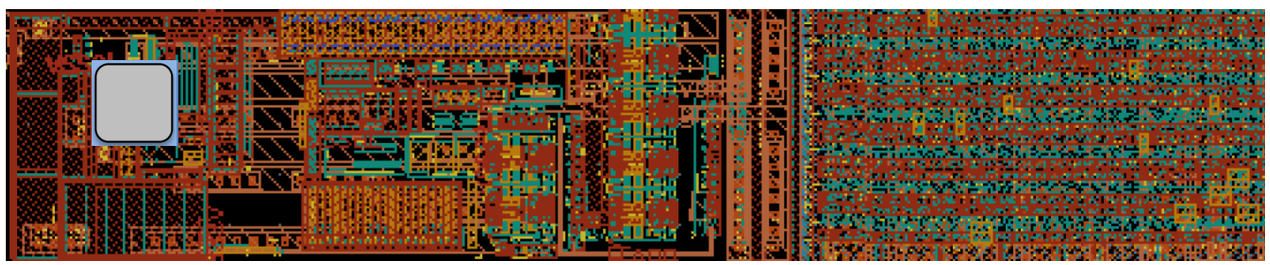
Comparison with other readout chips

PSI46 (150um x 100um)



- 250nm CMOS tech
- **251** transistors/pix

FEI4 (50um x 250um)

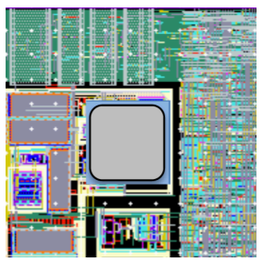


- 130nm CMOS techn
- ~**2500** transistors/pix
- ~0,5 trans/um^2

65nm technology allows to design a smaller pixel capable to sustain extreme particle fluxes and long latencies

CHIPIX65/RD53

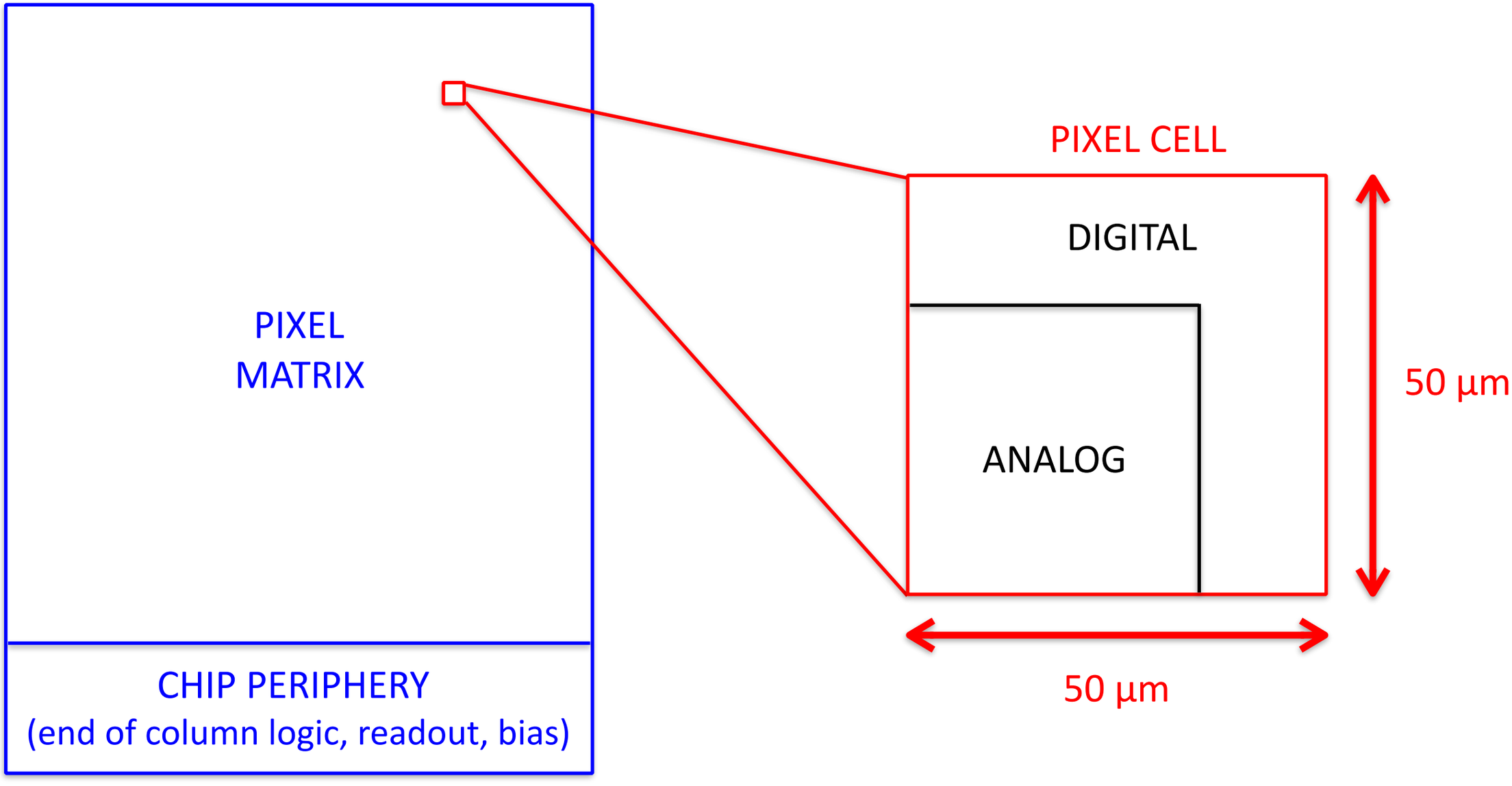
(50um x 50um).



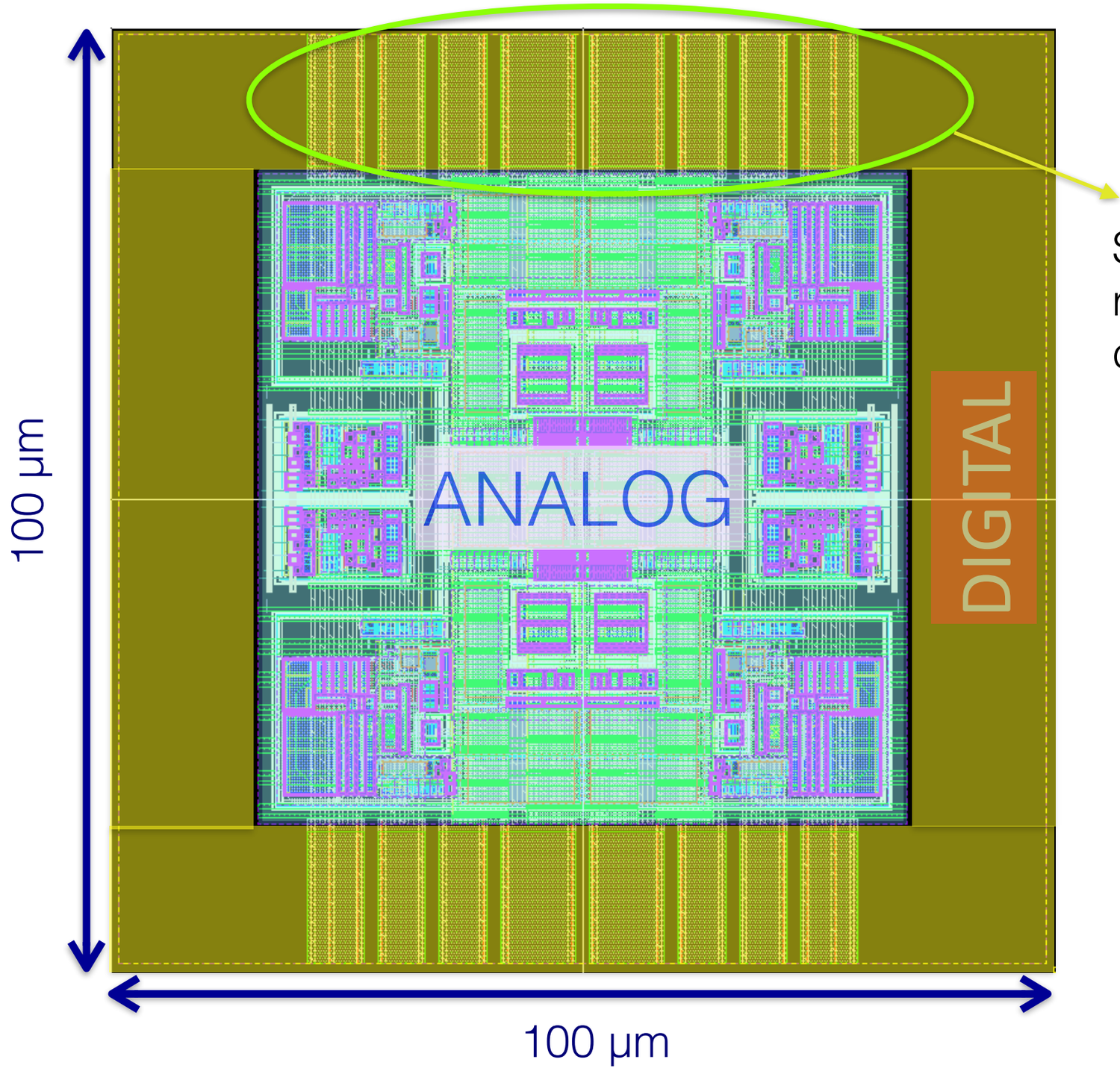
- 65nm CMOS tech
- ~**2500** transistors/pix
- ~2 trans/um^2

50% of area to digital

Pixel chip scheme

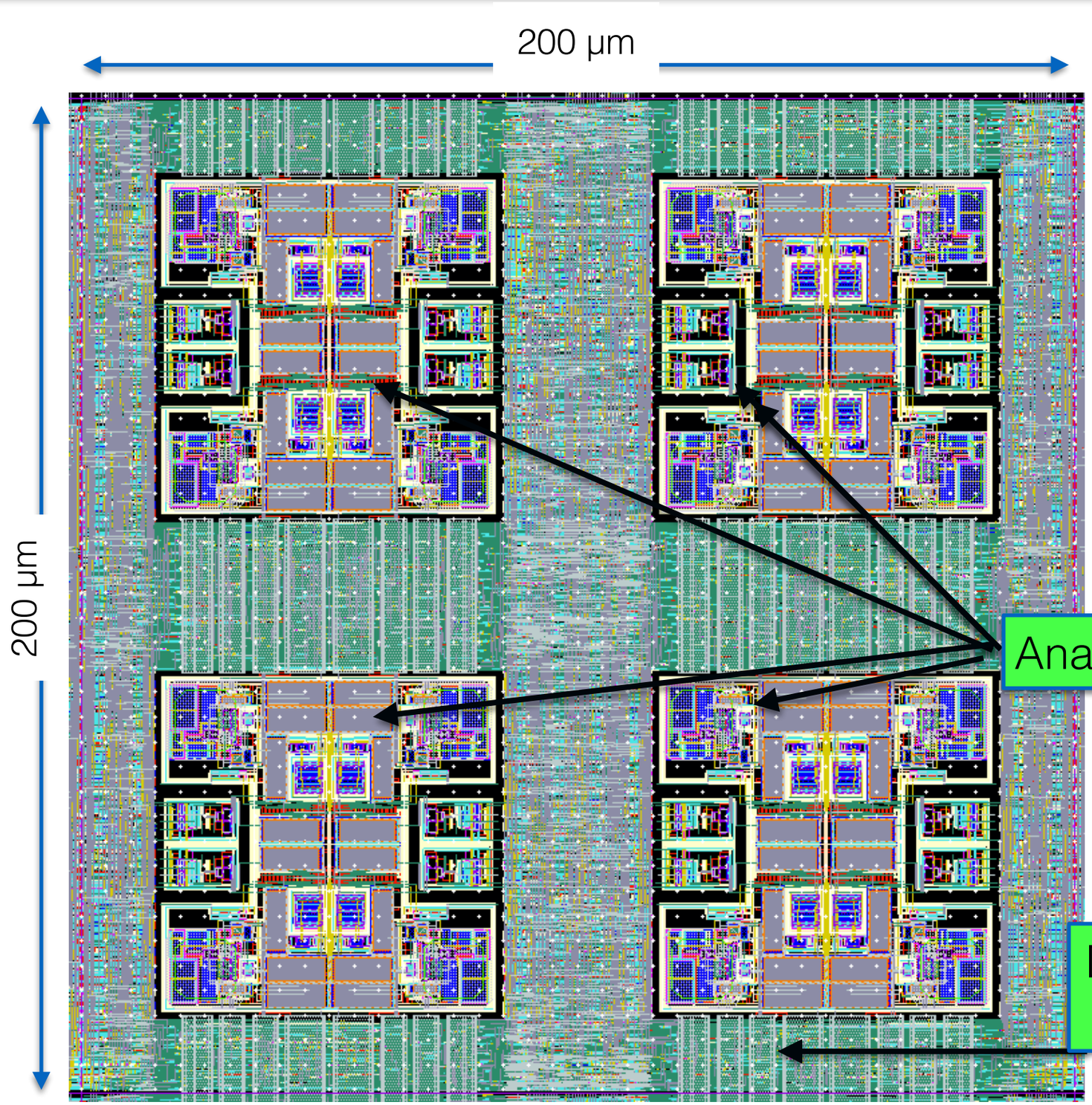


2x2 analog island



Shielding of bias lines running on top of the digital part

Pixel Regions



Area for digital is tight: the idea is to make real use of sharing digital resources among more pixel

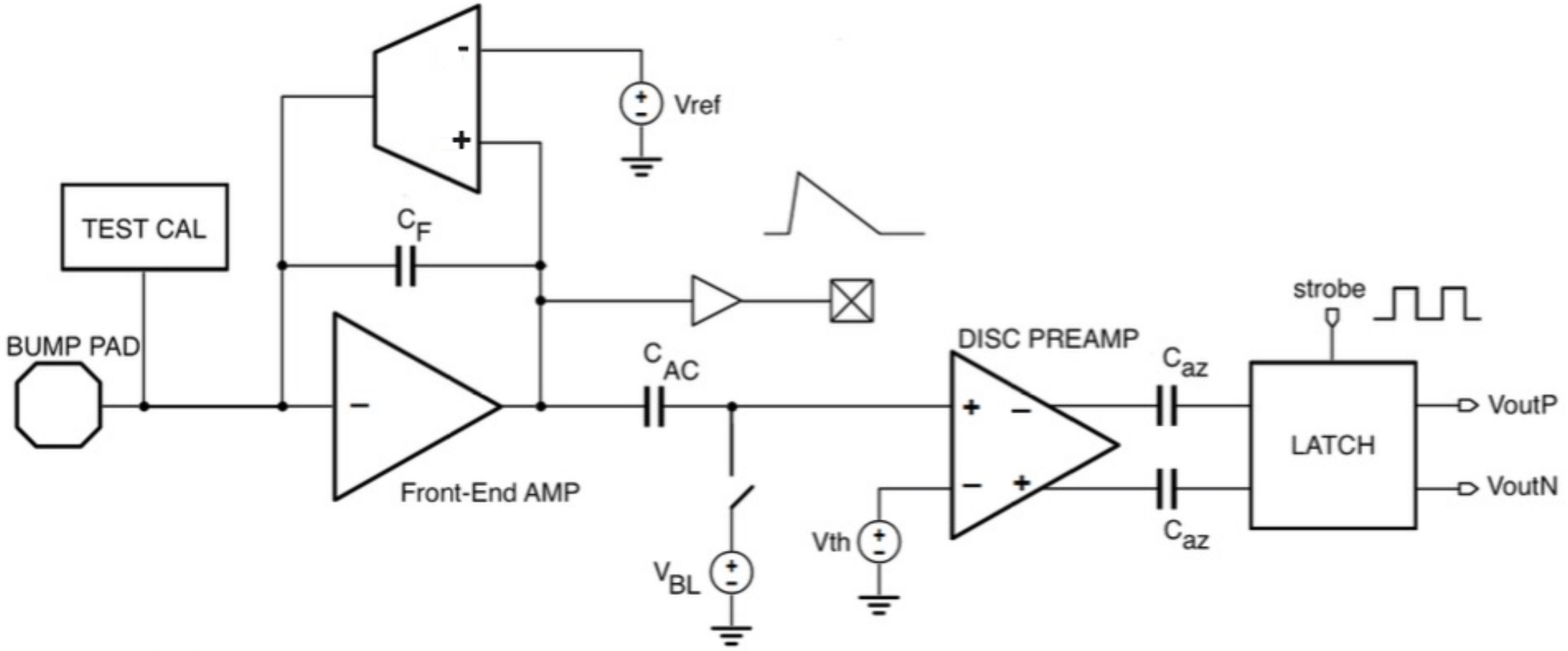
Synchronous analog front-end design

Main features

- **Innovative design**:
  - **Synchronous discriminator**: suitable for a clocked machine like LHC
  - Very **fast discrimination** using a positive feedback latch, which can be also used as a local oscillator for fast Time-over-Threshold counting
  - **Offset compensation by hardware** based on switched capacitors techniques

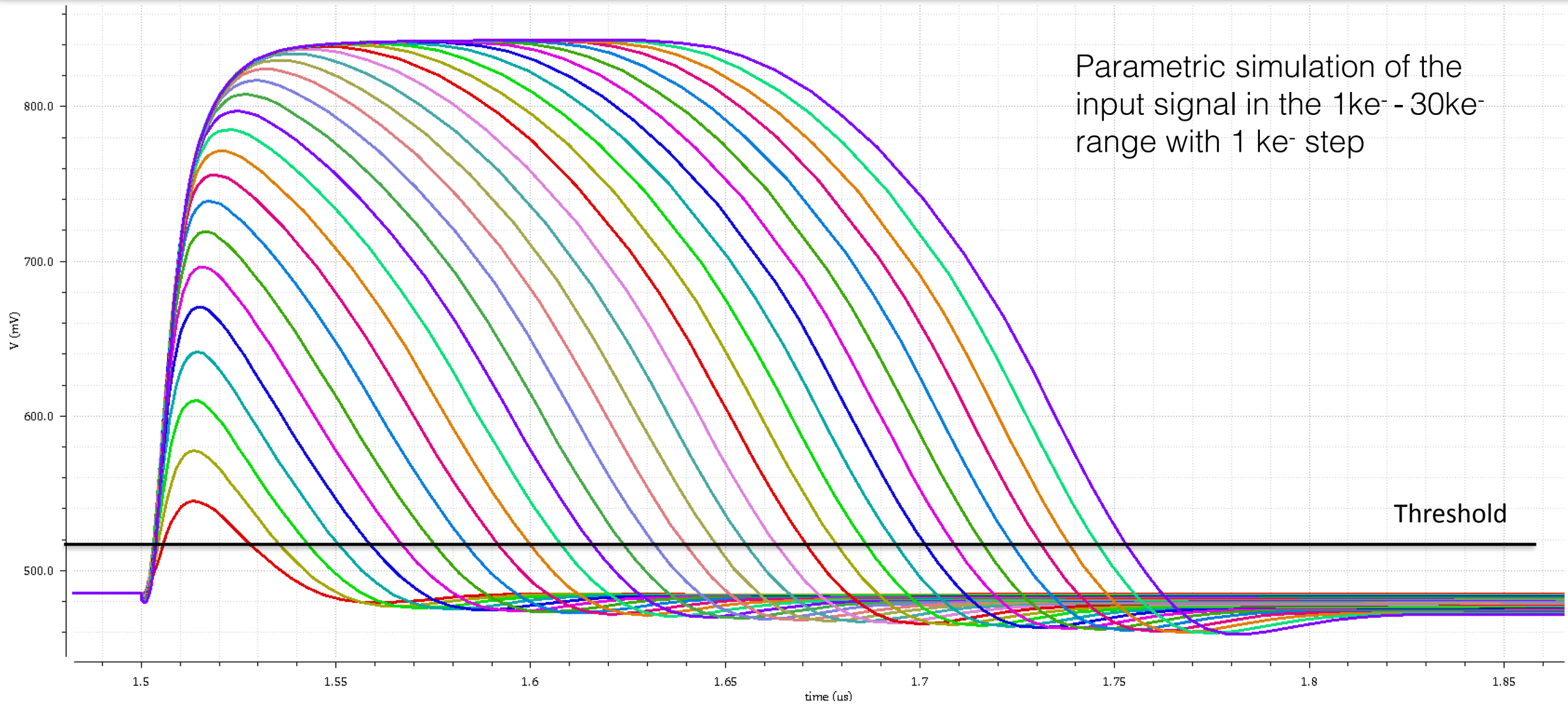
- **Small**: half of the area of a 50x50 μm^2 pixel
- **Low noise**: < 100 e^-
- **Low threshold**: ~ 600 e^-
- **Low power**: ~ 5 μW
- One of the first application of a CMOS 65nm for HEP analog design

Synchronous analog front-end



- **PREAMPLIFIER**
  - One stage Charge Sensitive Amplifier (CSA) with Krummenacher feedback
- **Synchronous DISCRIMINATOR**
  - AC coupled to CSA
  - Offset compensated differential amplifier using autozeroing
  - Fast Time-over-Threshold
    - Local oscillator strobing Latch (to 800MHz)
- **Charge injection circuit**
  - Digital signal + DC calibration level

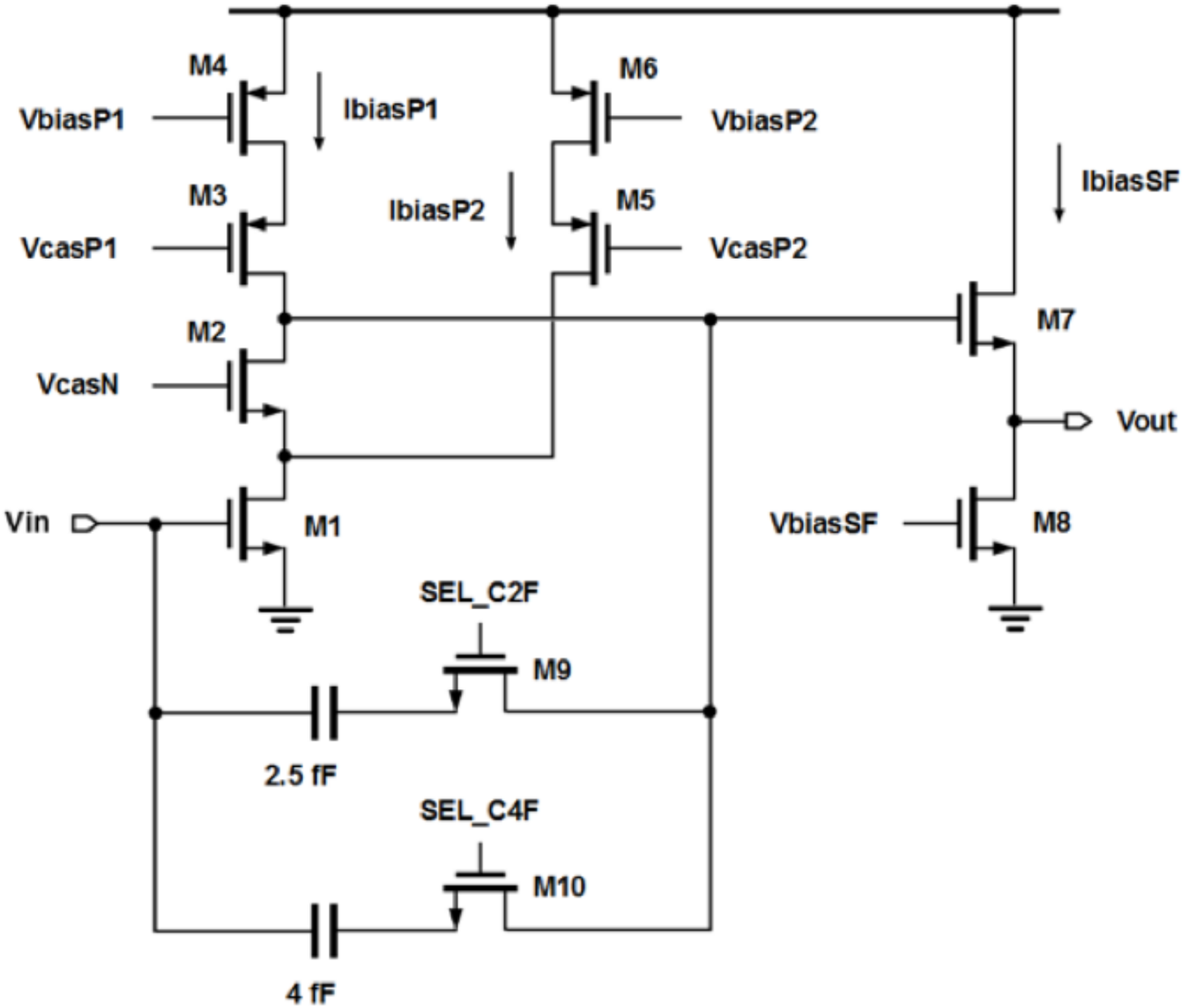
Time-over-Threshold technique



Parametric simulation of the input signal in the 1ke$^-$ - 30ke$^-$ range with 1 ke$^-$ step

- Time-over-Threshold technique:
  - The time spent by the signal over the threshold is proportional to the amplitude of the input signal
  - The time needed to remove the charge is equal to Q_{in} / $I_{discharge}$
  - Advantage: the linear digitization in amplitude is limited in the baseline-1.2 V range; the linearity of the ToT vs Qin instead is maintained even if the CSA gain saturates

Charge Sensitive Amplifier

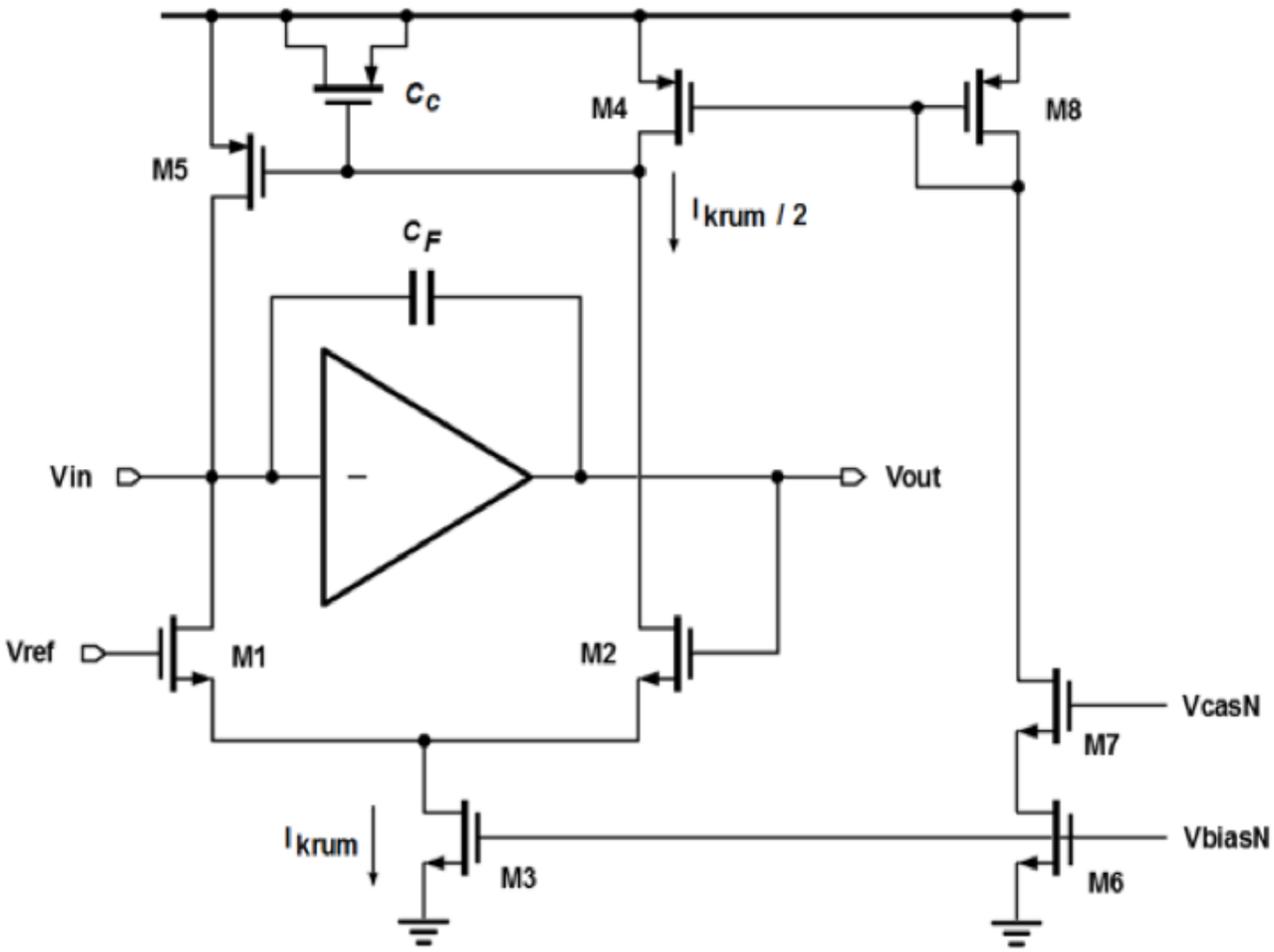


- Pixel sensors for HL-LHC will produce small signals (in the 1-30 ke^- range) → **high gain** required for proper signal processing
  - It is provided by t**elescopic cascode** amplifier (M1-M4)
  - The **current splitting** branch (M5-M6) improves the noise figure of the CSA
  - The open loop gain is 60 dB
  - **Source Follower** added at the output for impedance matching

- Two different **gain configurations**:
  - Low (C_{feed} = 2.5 fF)
  - High (C_{feed} = 4 fF)

- Total current consumption around 2.5 μA

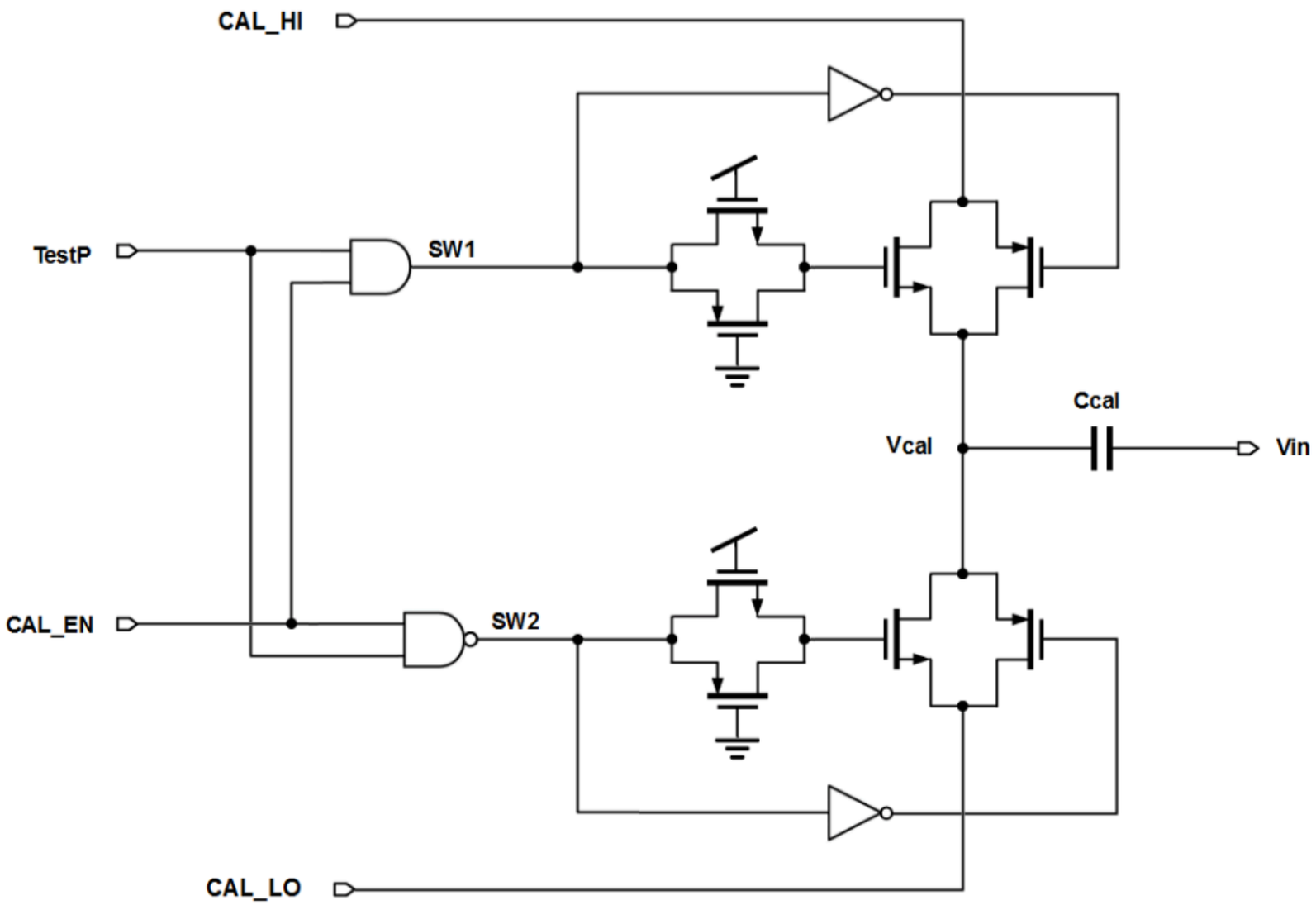
Krummenacher feedback



- Firstly presented by F. Krummenacher in 1991 (1)
- Provides the **DC level at the input of the CSA**
- Drives the speed of signal discharge (therefore the **ToT speed**)
- Implements the **sensor leakage current compensation**

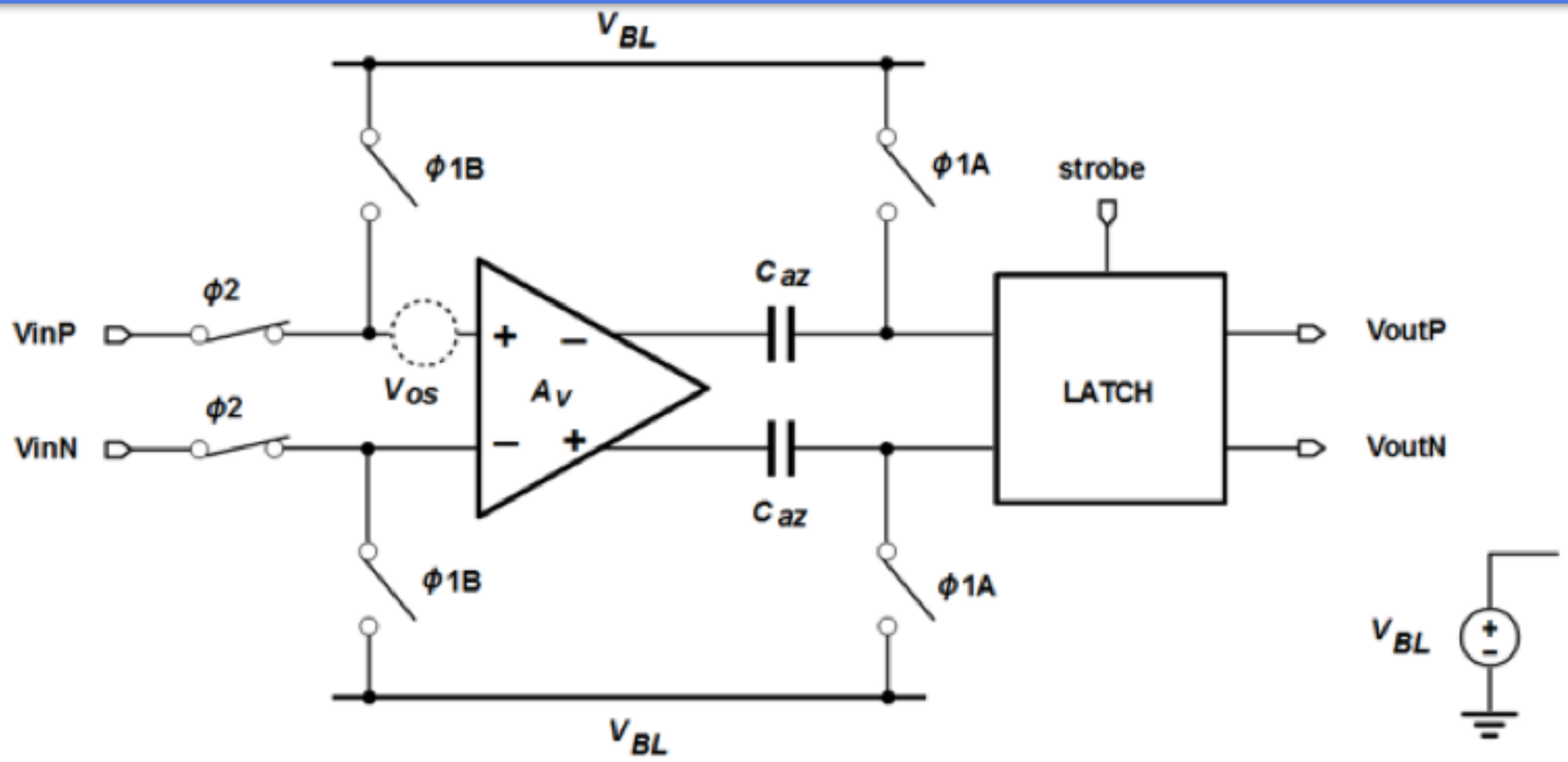
1) F. Krummenacher, “Pixel detectors with local intelligence: an IC designer point of view,” Nuclear Instruments and Methods in Physics Research, 1991

Charge injection circuit



- Local generation of the test pulse based on a DC level
- A switching digital pulse (TESTP) is used to inject the signal
- C_{cal} = 8 fF

Discriminator



- Features of the synchronous design:
  - LHC is a **40 MHz-clocked** collider: collisions take place very 25 ns (with a spread sigma equal to 0.25 ns)
  - The hit generation is synchronized with the clock, sampling the CSA output around the peak
  - In this way, the problem of **time-walk about timestamp assignment** is overcome
  - On the other hand, this synchronization has to be well optimized in order to take full advantage of this technique

Autozeroing

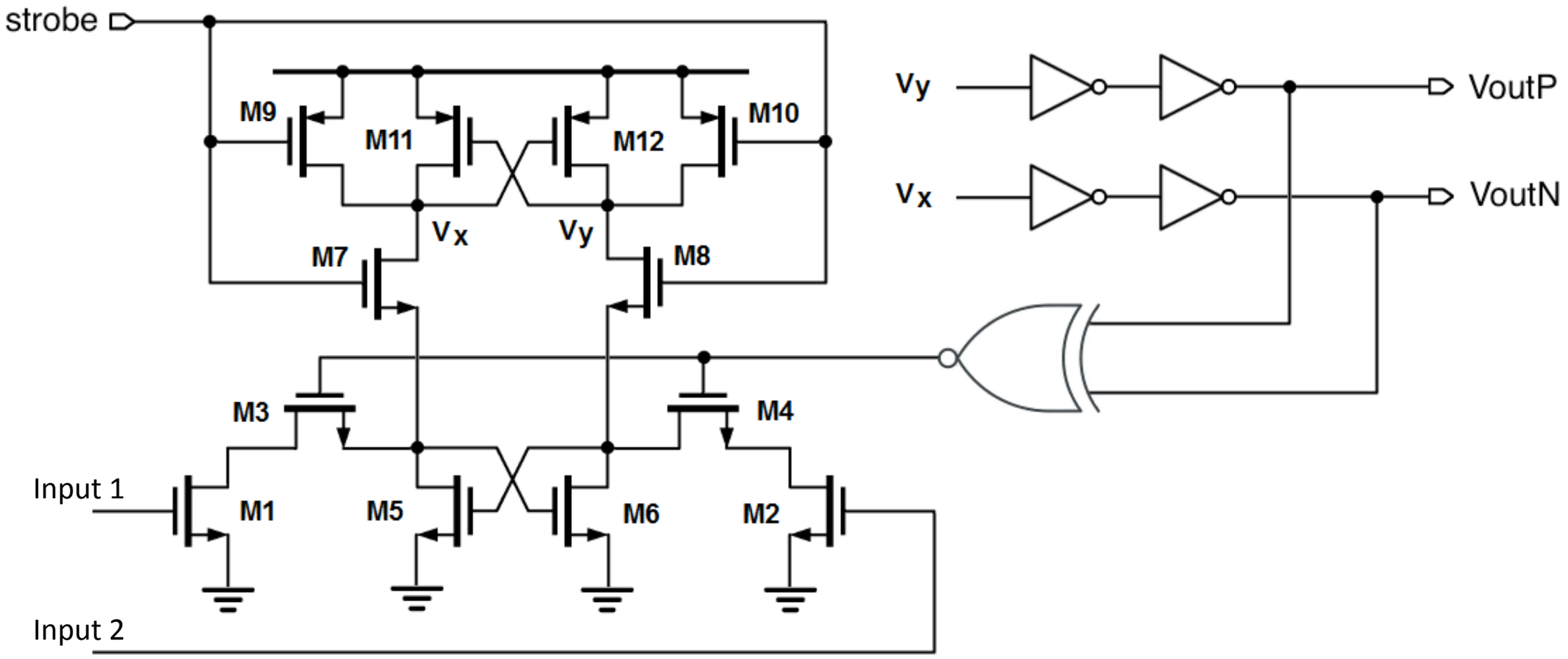
- This technique makes use of **switched capacitors for offset storage**
  - Usually front-ends for HEP have been based on continuous time design due to charge injections in the switches
  - The shrinking of the devices has progressively reduced these effects, making switched-capacitors technique again competitive for this application

- Advantages:
  - Pixel-by-pixel offset compensation by hardware
  - **No trimming local DAC needed** inside the pixel
  - No risk of SEU of local configuration registers determining a noisy pixel

- Disadvantage:
  - If the frequency of the offset compensation phase is too high it can introduce an additional dead time

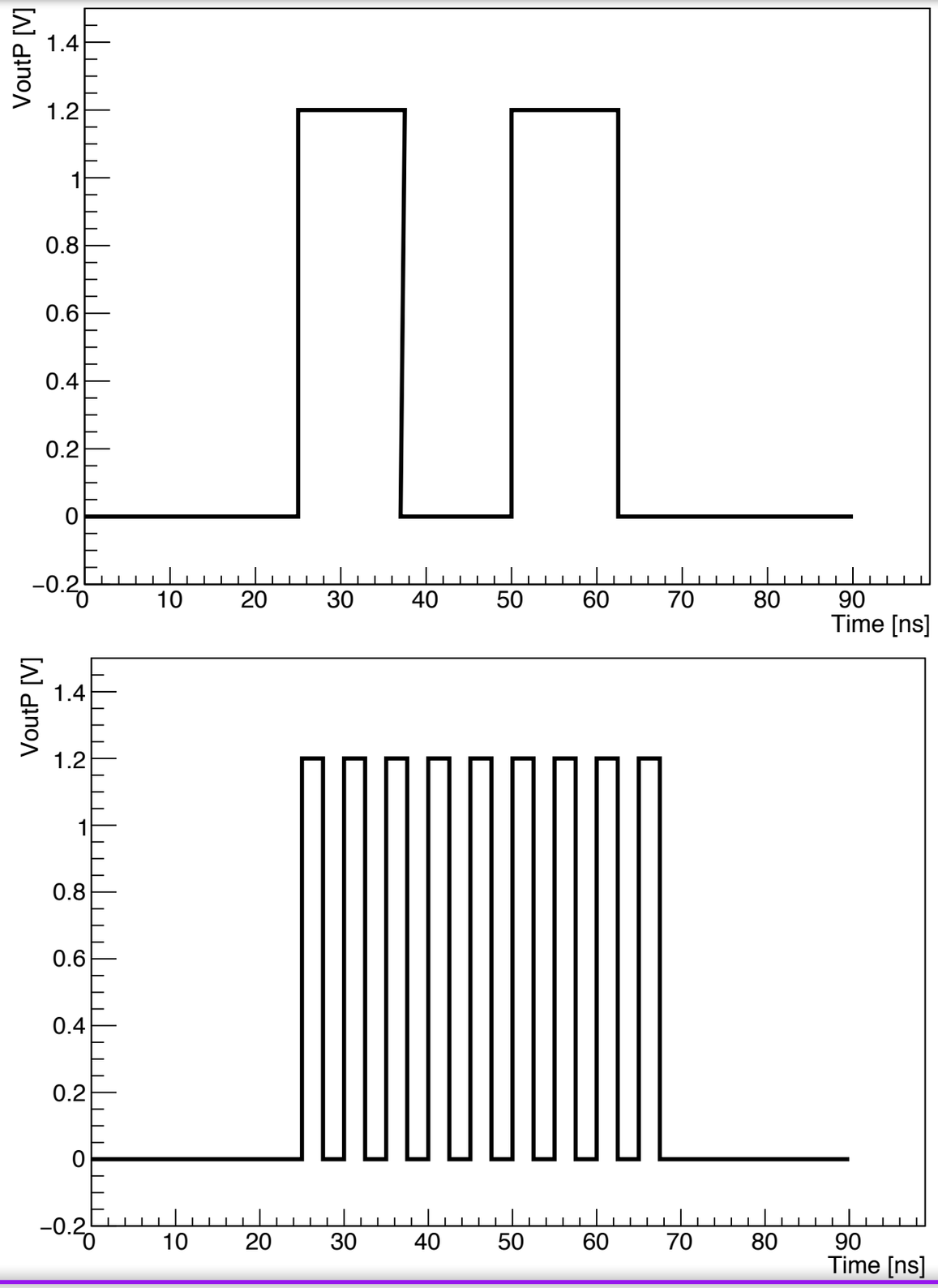
SOLVED! In this case it is enough to perform a 100 ns-long compensation every ~100 μs : taking advantage of the abort gap of the machine (which lasts around 3 μs) **no dead time is added**

Positive feedback latch



- When the 40 MHz strobe signal moves high, this stage is able to compare the two inputs in a very short time (~ 200 ps)
- The power consumption is limited to transitions thanks to the XNOR gate
- This kind of latch can be used only in a synchronous design

Latch operation simulation

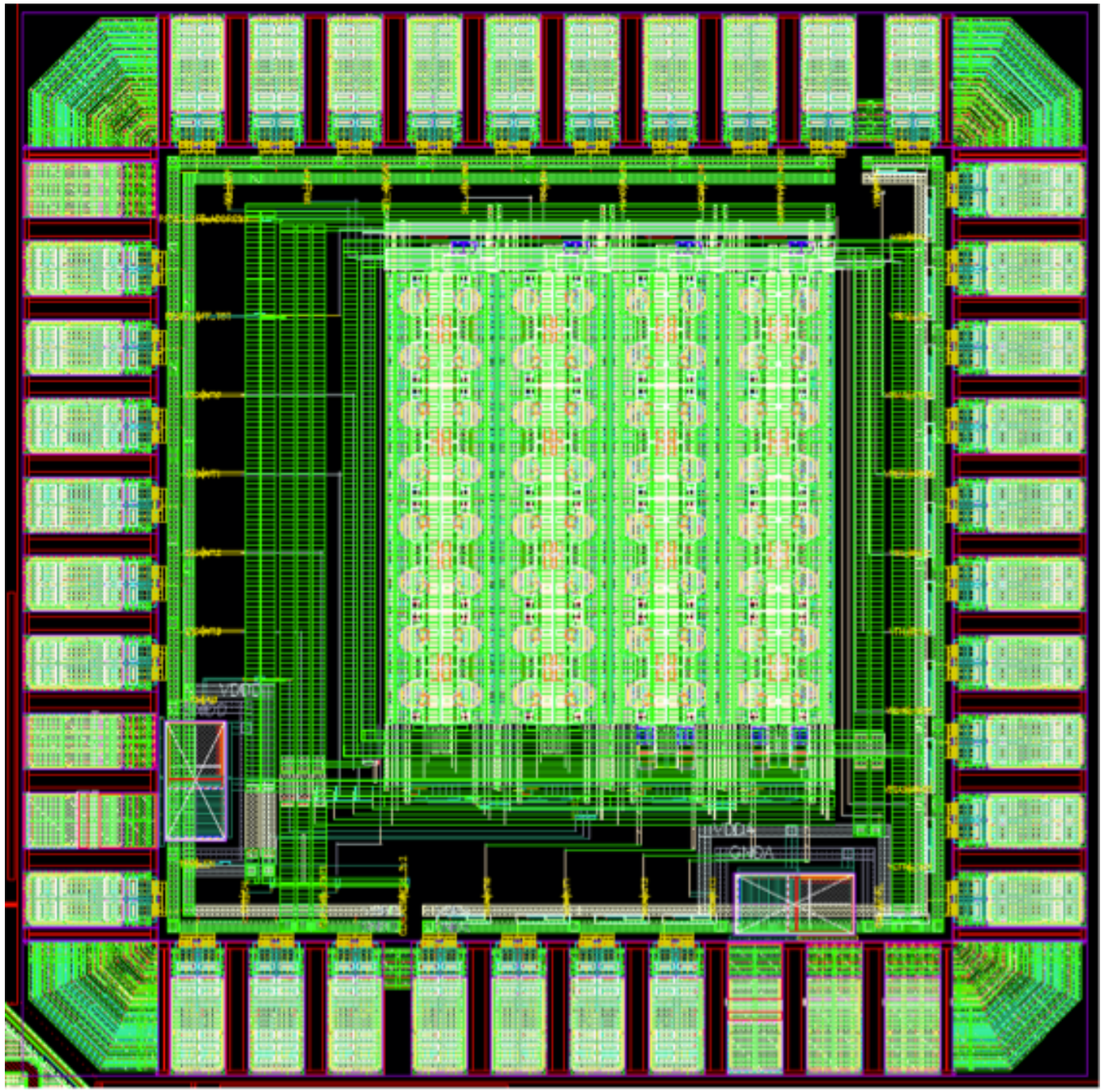


- 40 MHz operation
- ToT = 2 in this example

- Fast ToT operation
- Simulated with 200 MHz frequency
- ToT = 9 in this example

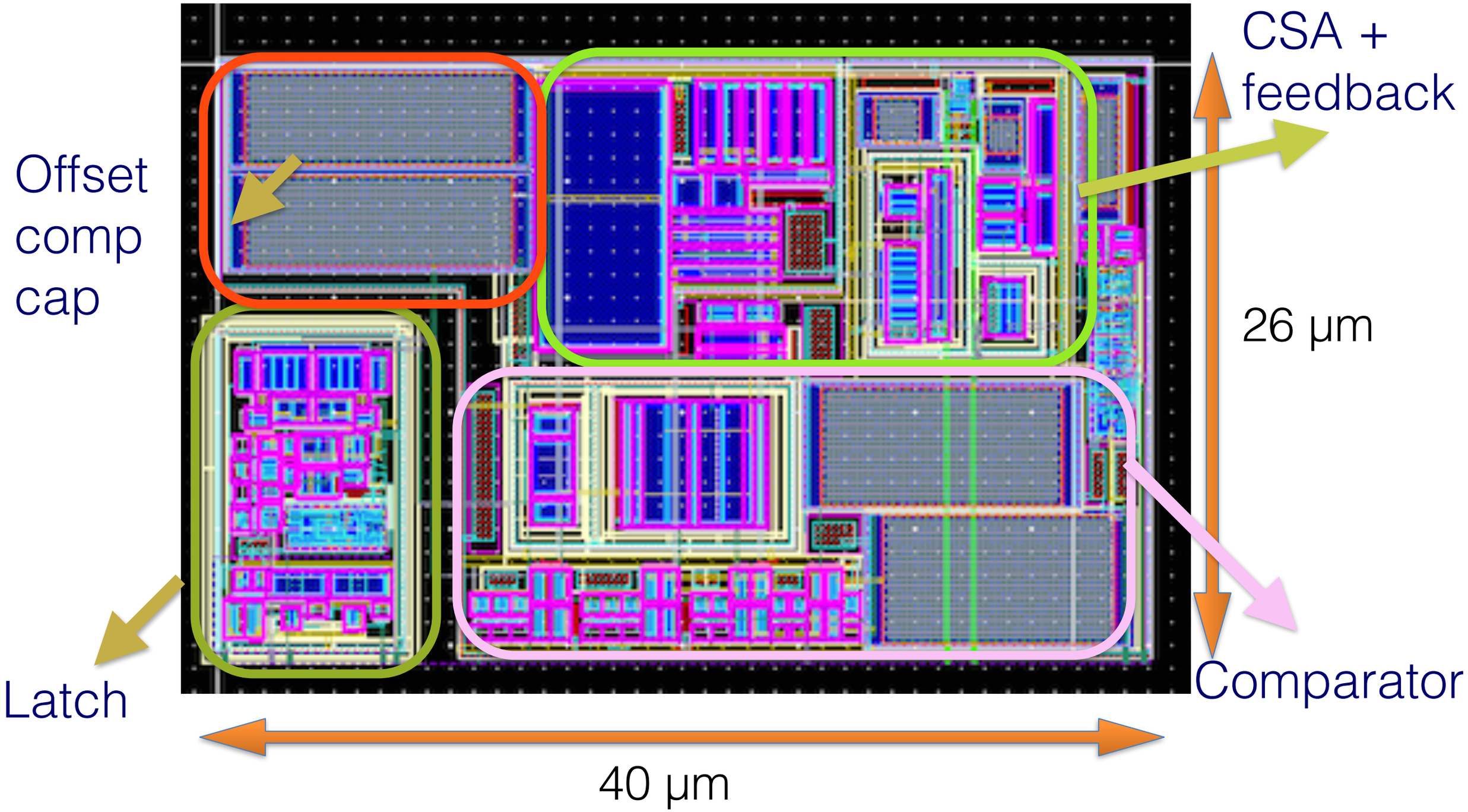
Chip submissions and test results

Small pixel matrix with analog outputs



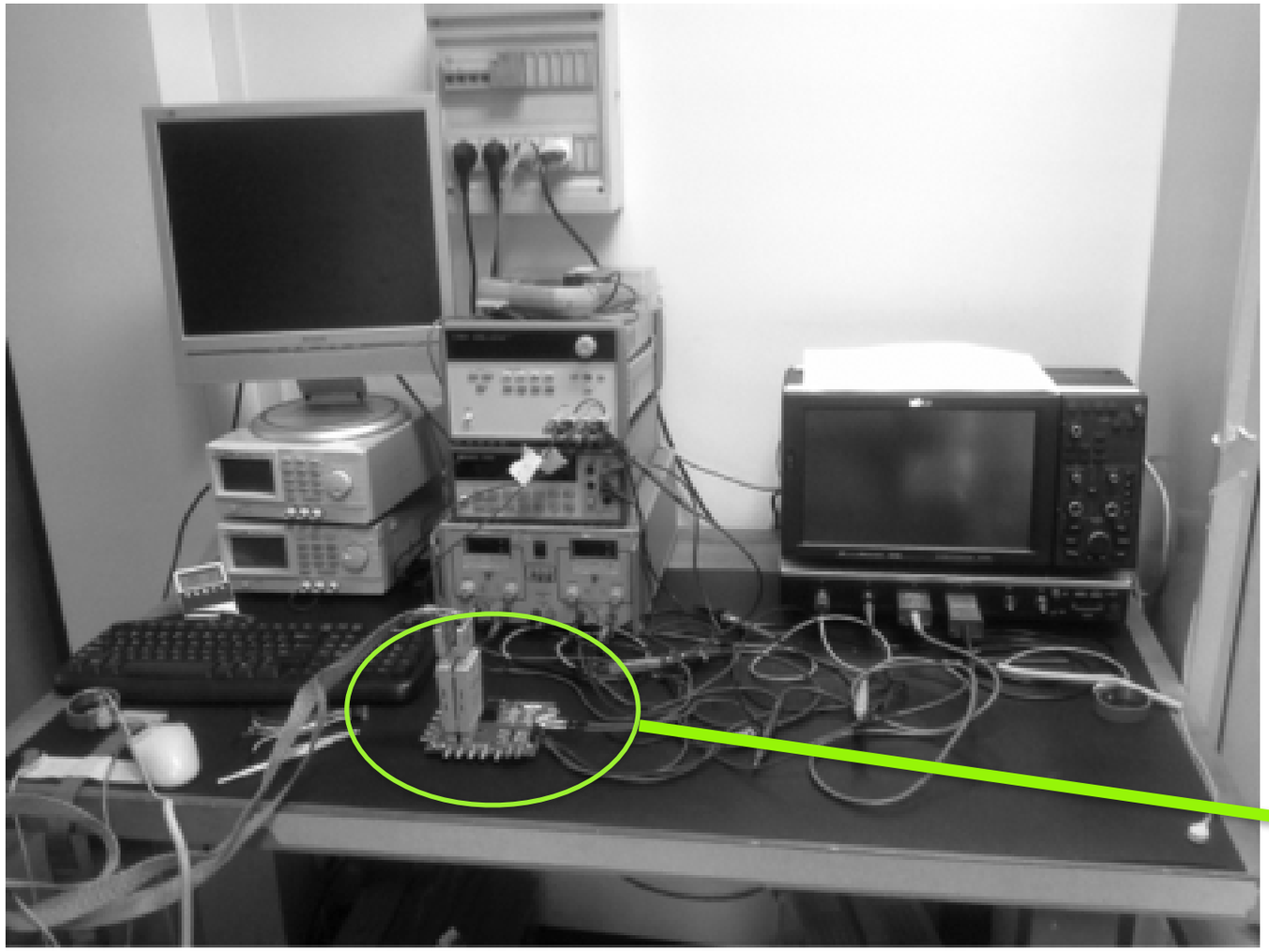
- **8x8 pixel matrix**
  - Two prototypes submitted to the foundry between **2014 and 2015** (named VFE_1 and VFE_2)
- Readout of CSA output using analog buffering
- Readout of discriminator output using a digital buffer
- 4 pixel (2x2 analog island) are readout at the same time
- VFE_2 irradiated with X-rays up to a TID = 600 Mrad at room temperature

Analog cell layout (40 x 26 μm²)



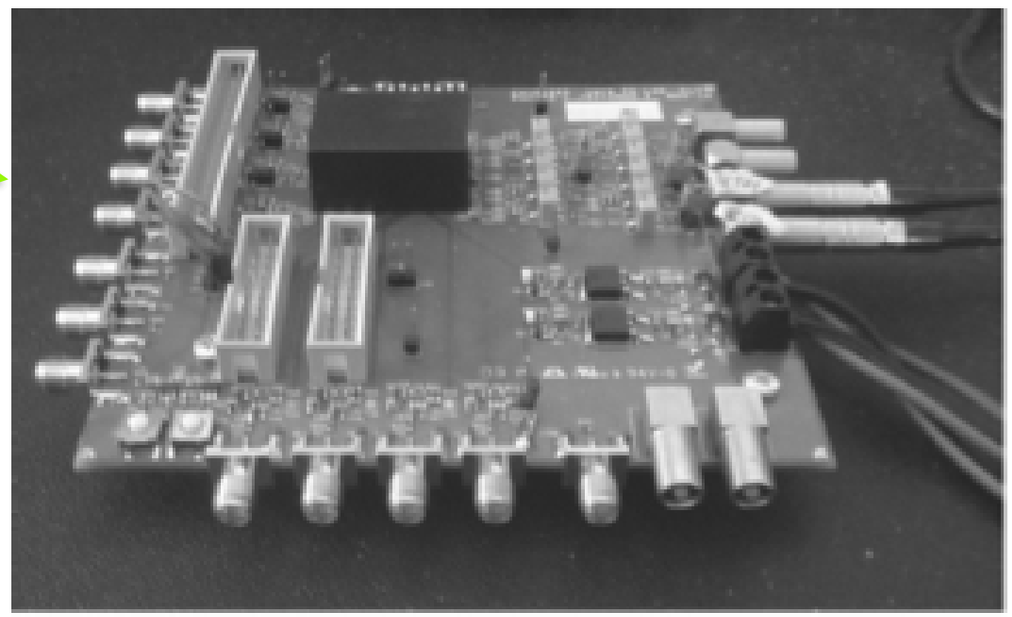
In addition three selectable input capacitances (of value 21.5, 43 and 86 fF) have been added to emulate the detector together with the analog and digital buffers

Experimental setup



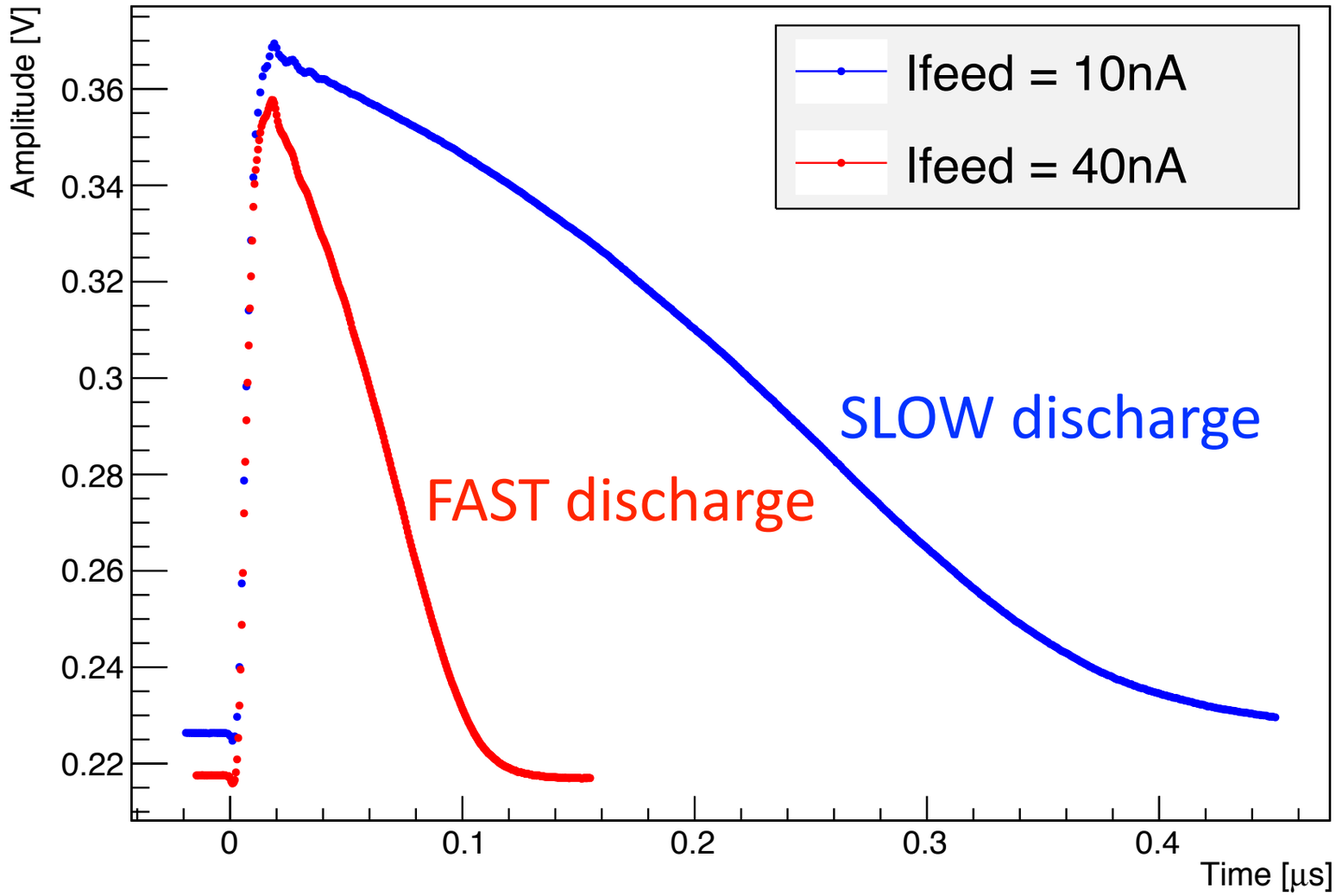
TEST BOARD

(Designed by Luca Pacher and Francesco Rotondo)



- Test board
- Power supplies
- Digital pattern generator
- Oscilloscope
- Active probe with large bandwidth

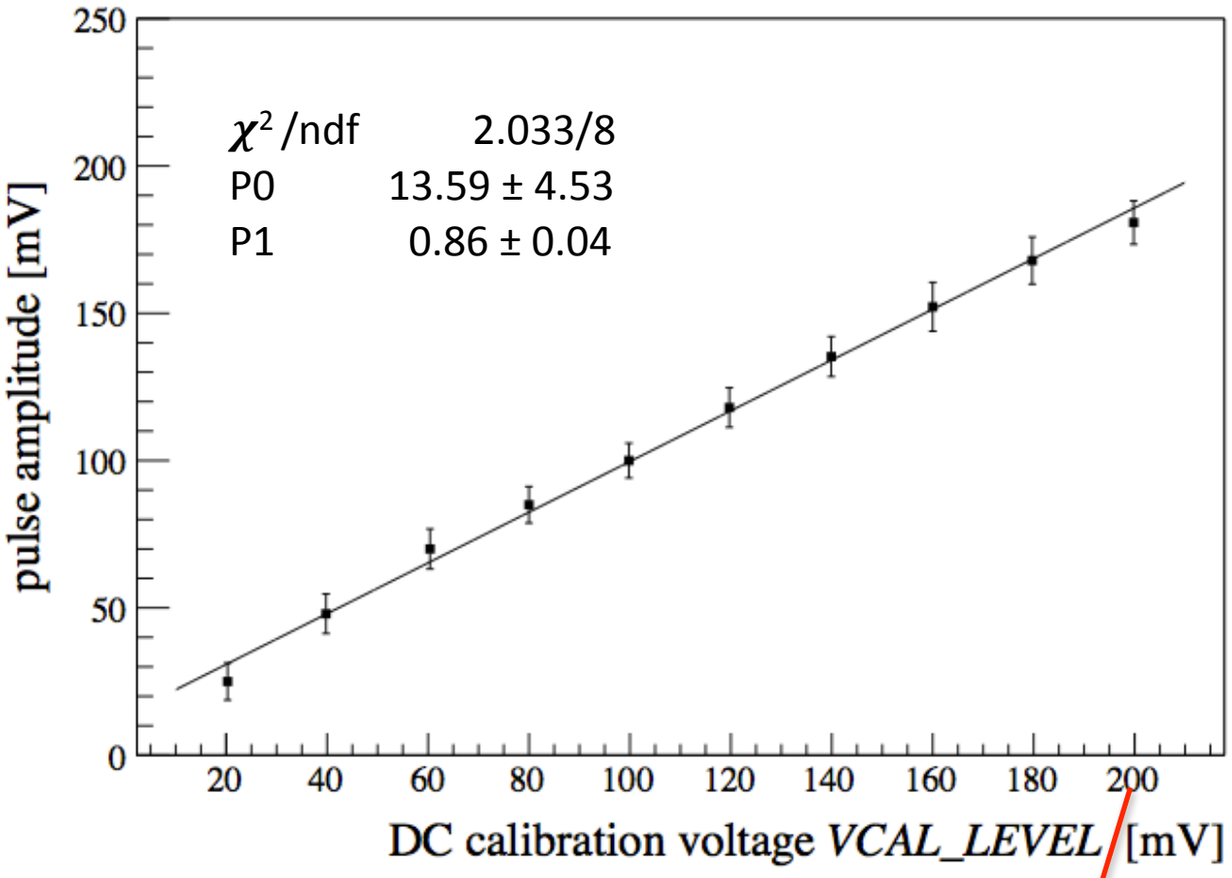
Signal shape



- C_{input} = 50 fF ⇒ T_{peak} around 25 ns
- Two different values of feedback current:
  - Slow → ToT = 400 ns for a 10 ke- input signal: 10 nA
  - Fast → ToT = 100 ns for a 10 ke- input signal: 40 nA
- At the schematic level the value of T_{peak} @ 50 fF is around 18 ns

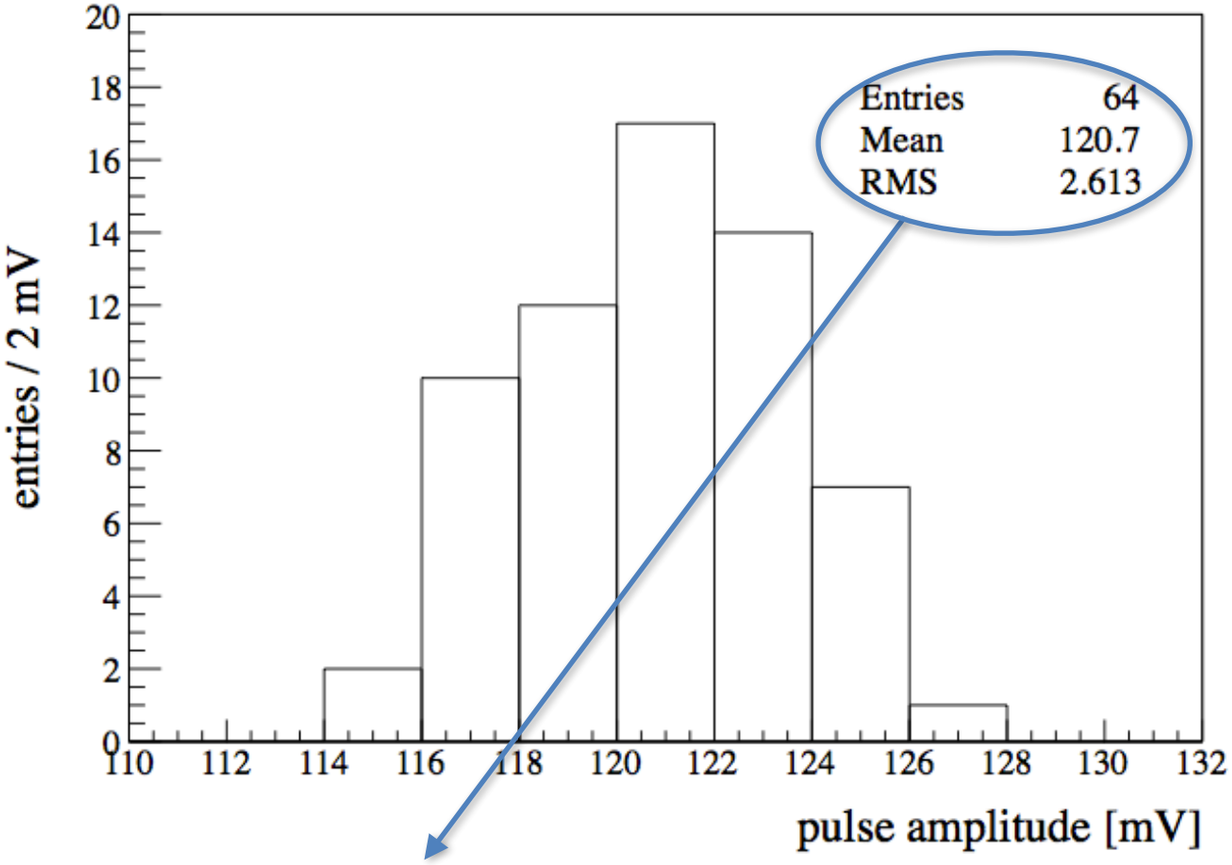
CSA gain

CSA voltage gain linearity for one pixel



10 ke$^-$

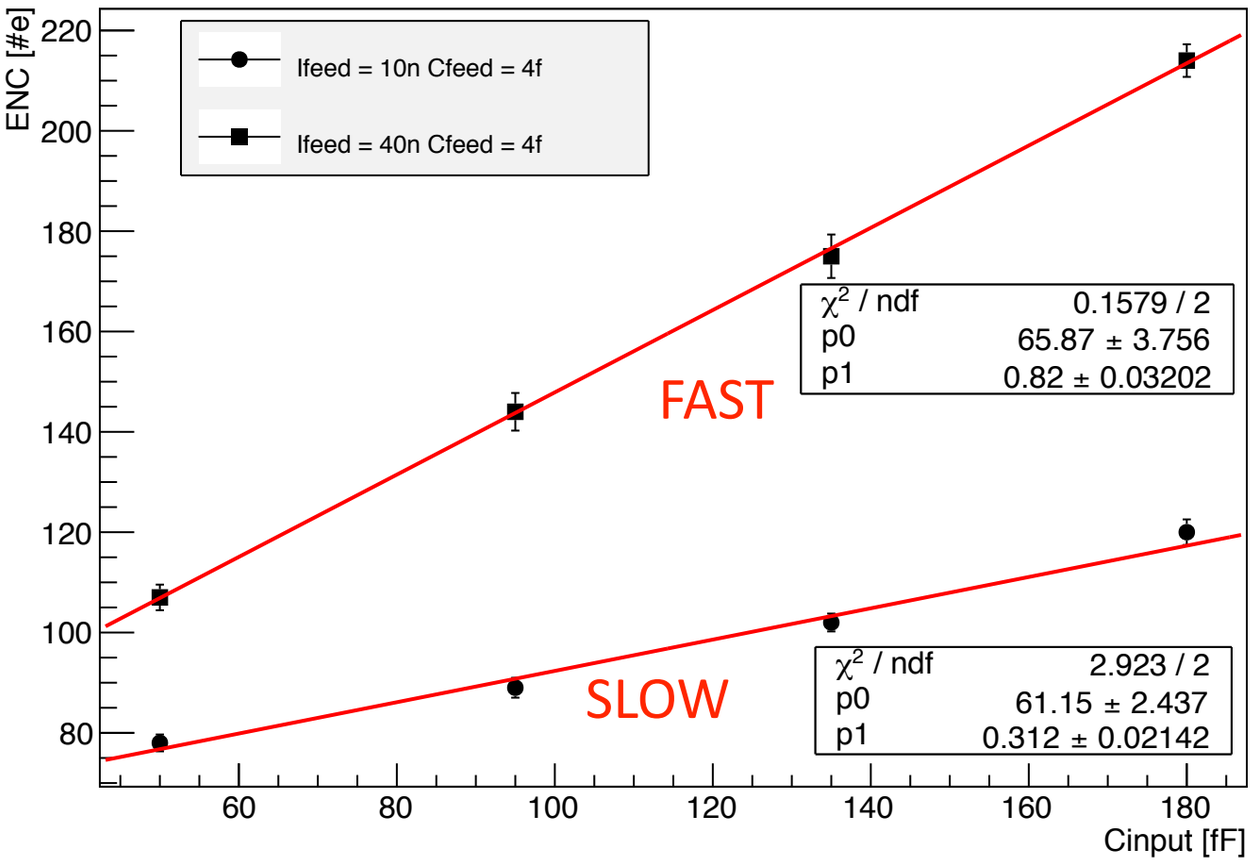
Gain distribution of the 64 pixels (Q_{in} = 6ke$^-$)

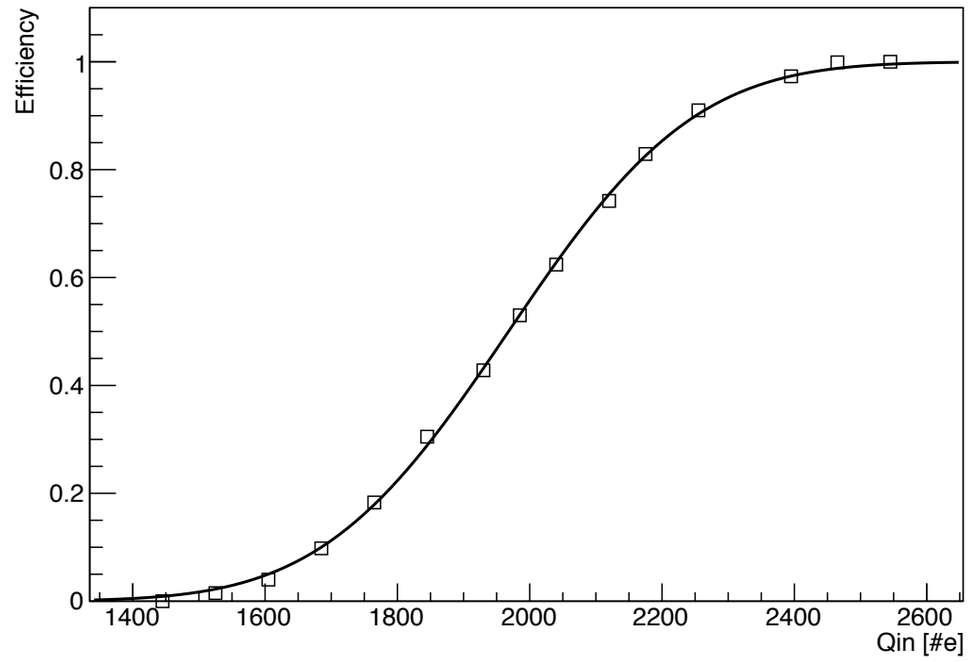


Amplitude dispersion below 2.2% RMS

Excellent gain uniformity

Noise

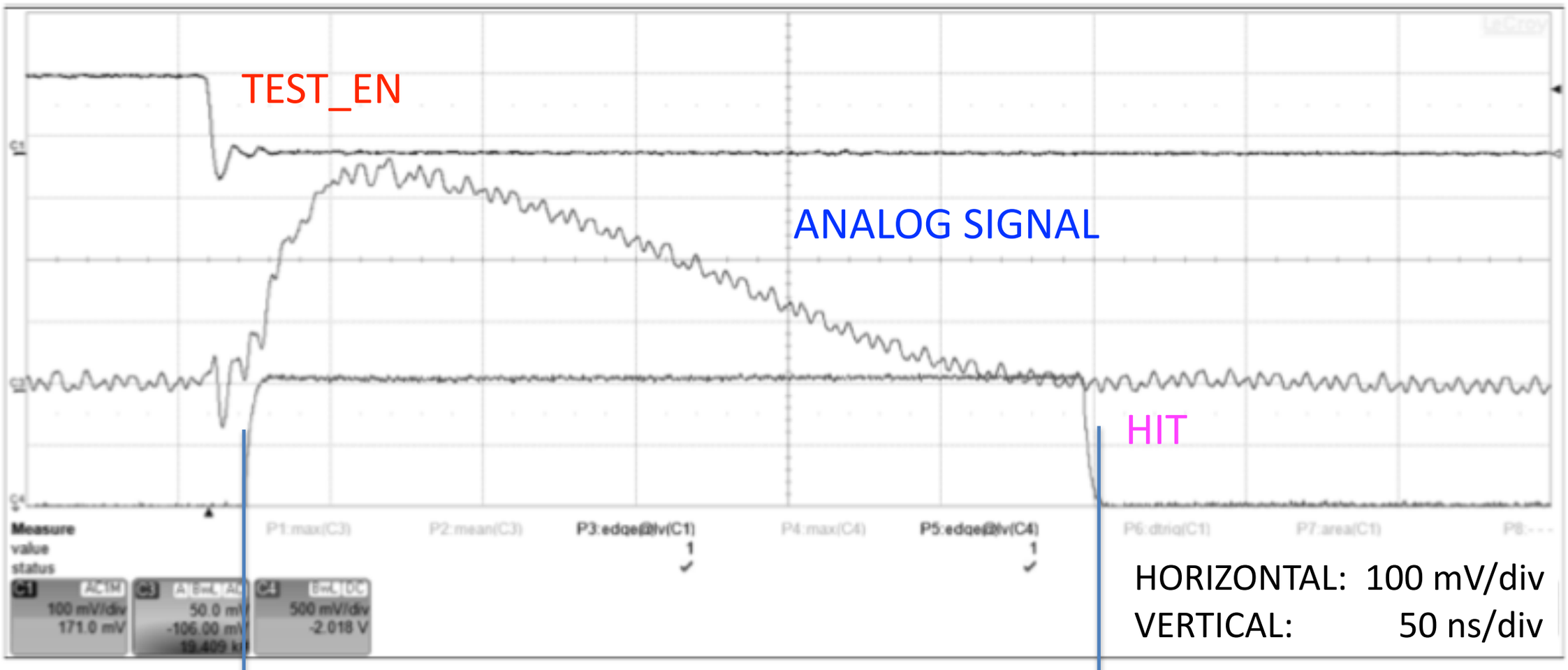




- Linear trend of the Equivalent Noise Charge vs input capacitance as expected
- Noise increases with the feedback current
- Threshold = 1000 e- ⇒ Around 7σ of the noise

Comparator output - Binary mode

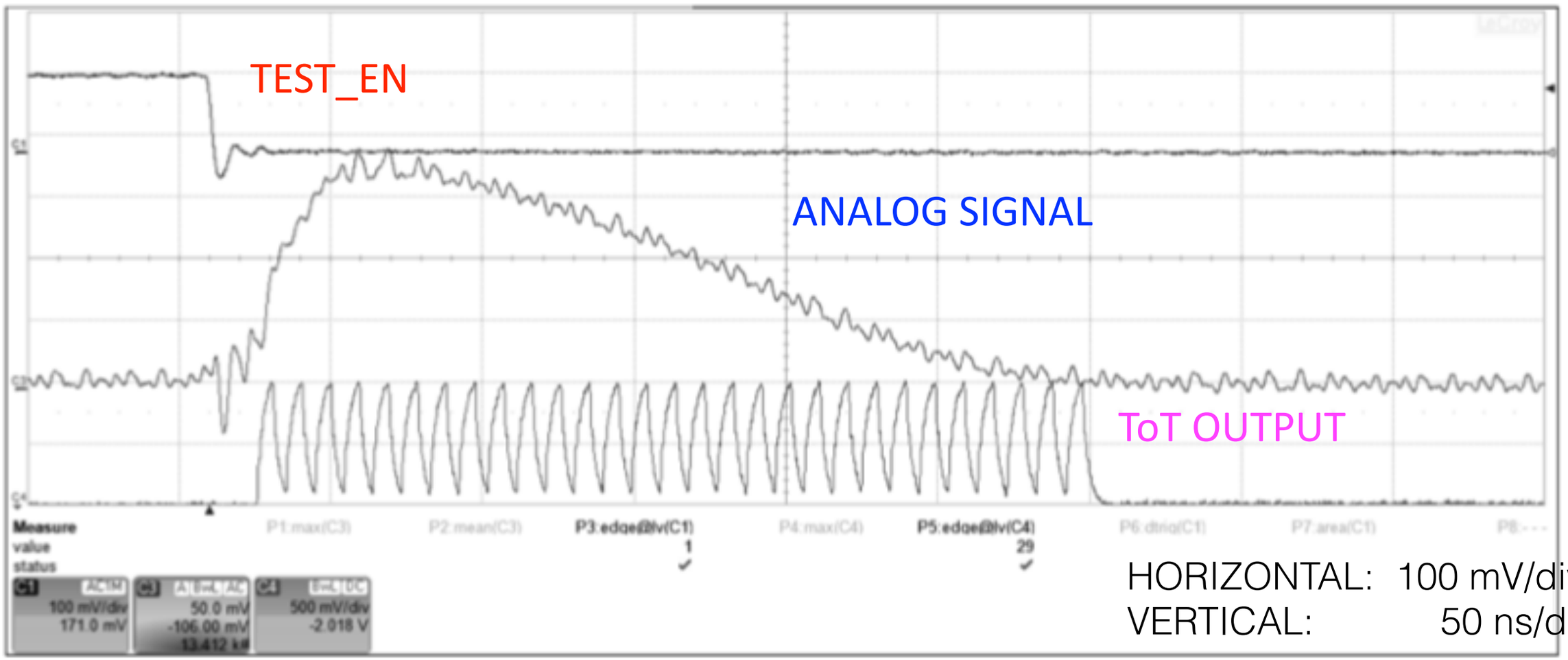
Input signal 10 ke^- Threshold ≈ 1000 e^-



Time duration of HIT multiple of 25 ns (clock period)

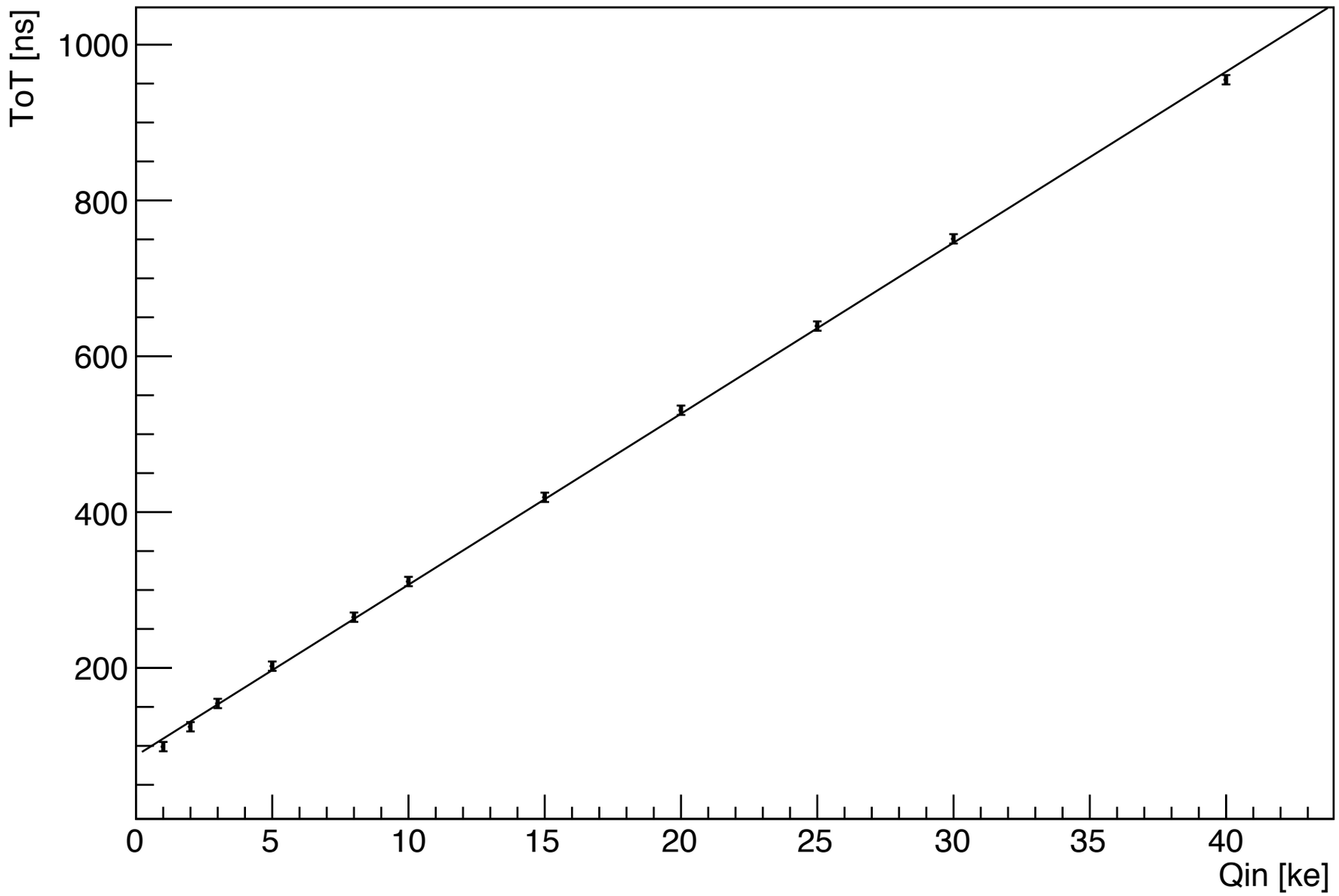
Comparator output - Fast ToT mode

Input signal 10 ke^- Threshold ≈ 1000 e^-



- Oscillator @ 100 MHz
- Time duration of the ToT output compatible with HIT in binary mode
- Oscillation speed can be tuned up to 500 MHz, but set-up bandwidth for this small prototype is limited to about 100 MHz

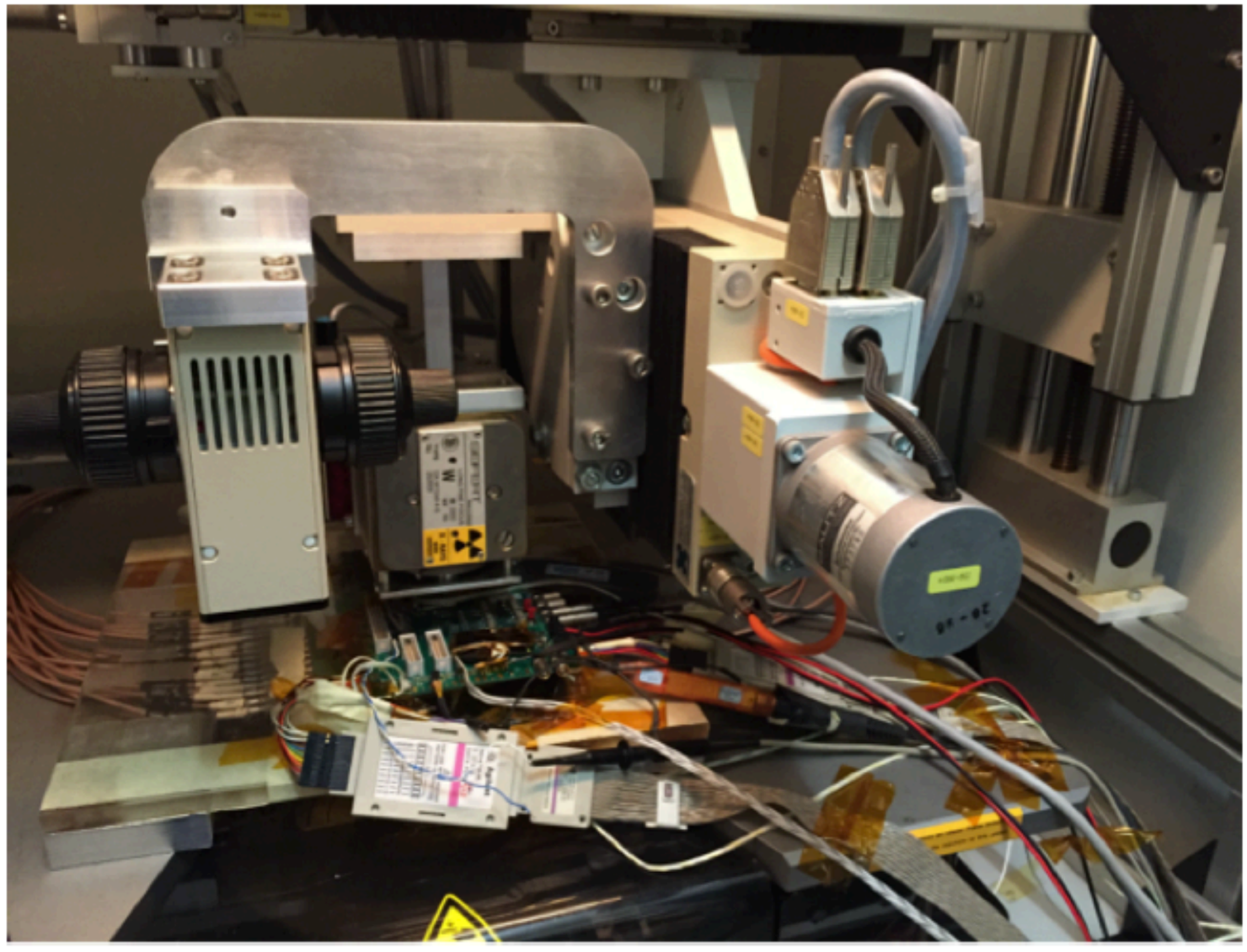
ToT linearity



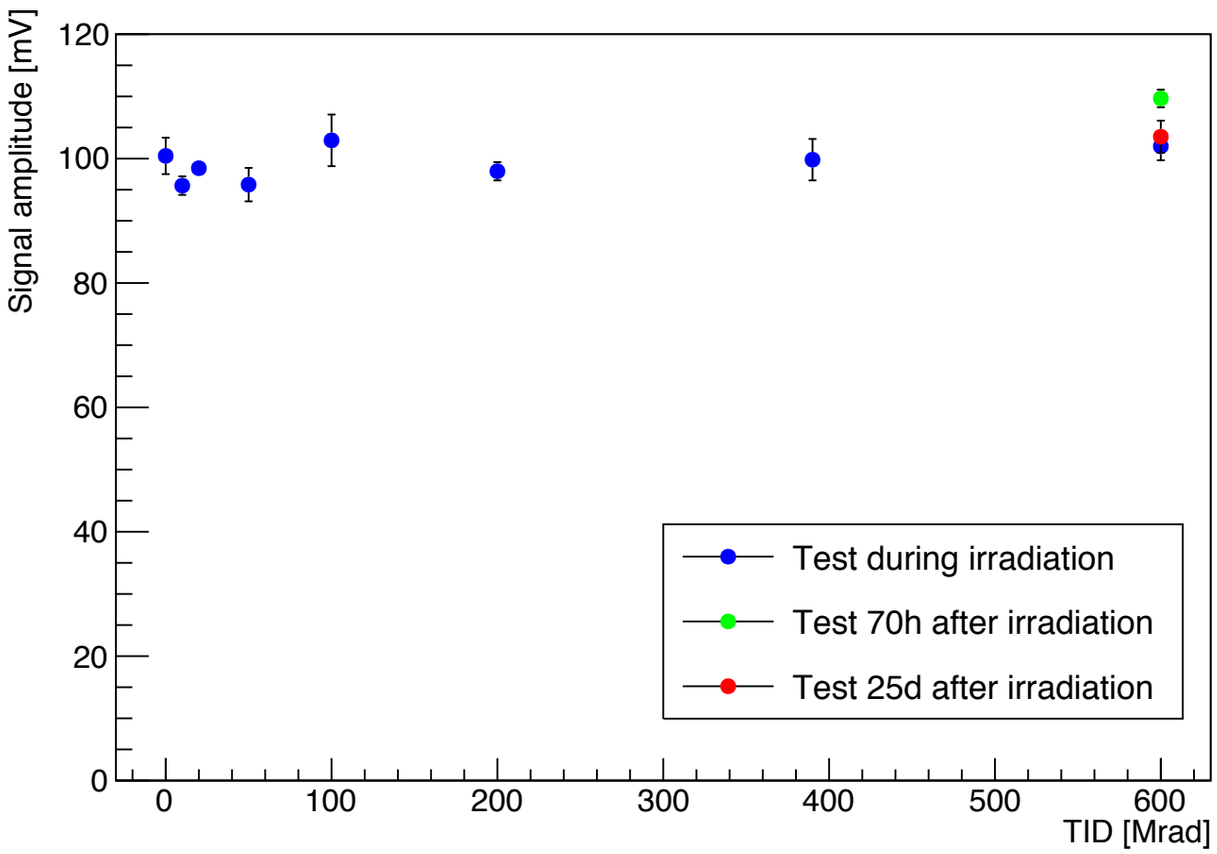
ToT is linear up to (at least) 40 ke$^-$

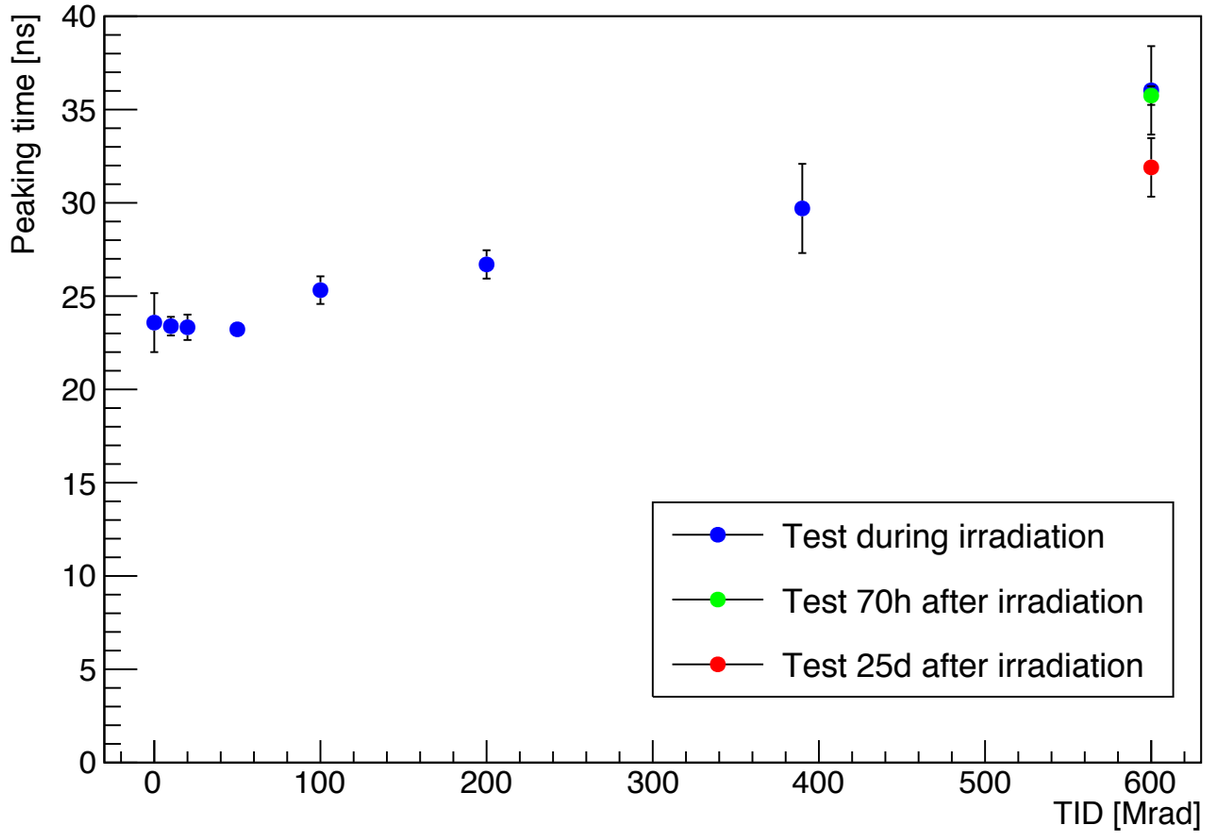
Irradiation campaign

- Made at CERN X-ray machine
- **Chip powered, biased, clocked, readout active: as during HL_LHC**
- Ambient temperature: worst case
- TID up to 600 Mrad
- In all these test
  - Medium gain (Cfeed = 4.2 fF)



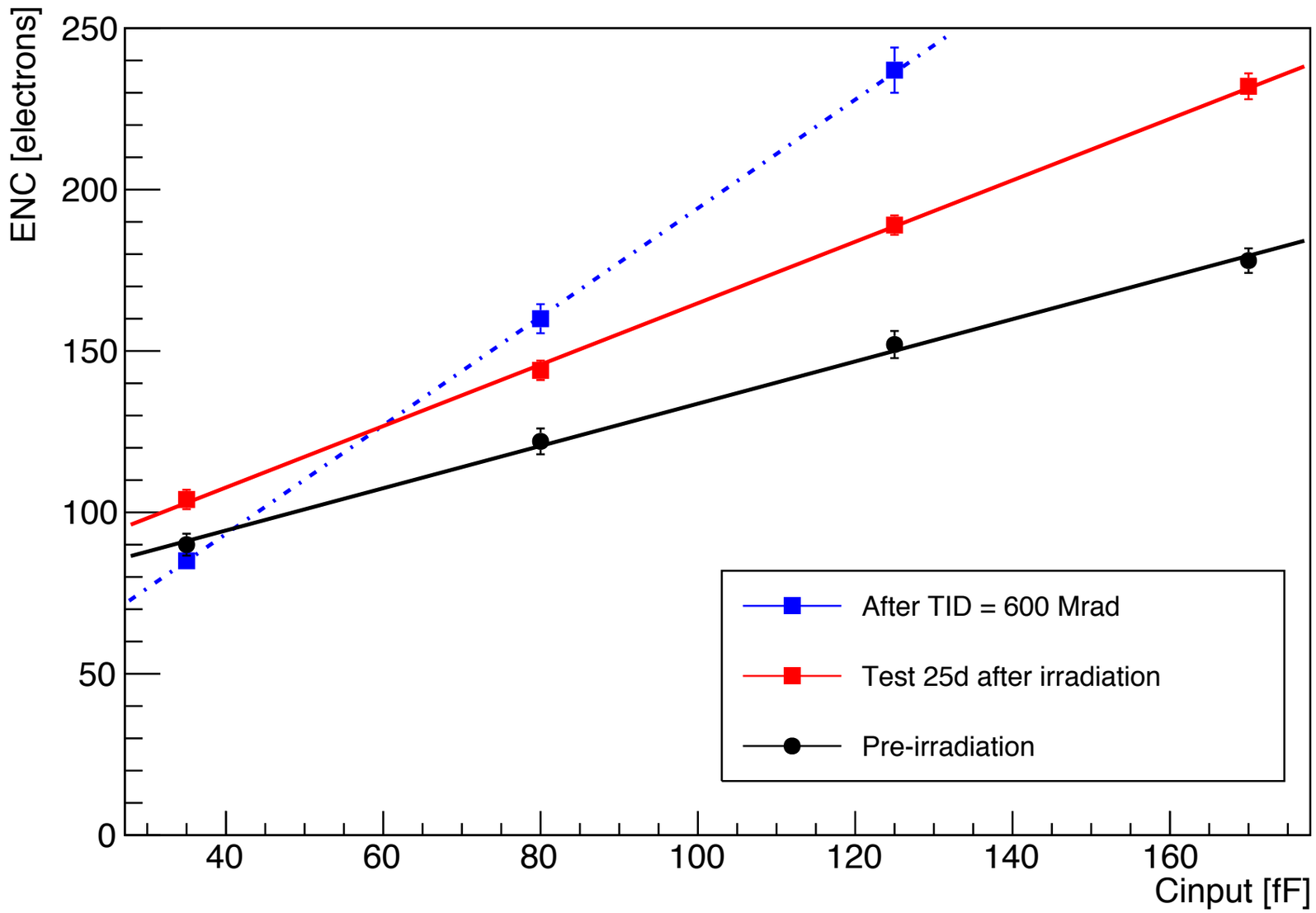
Analog parameters





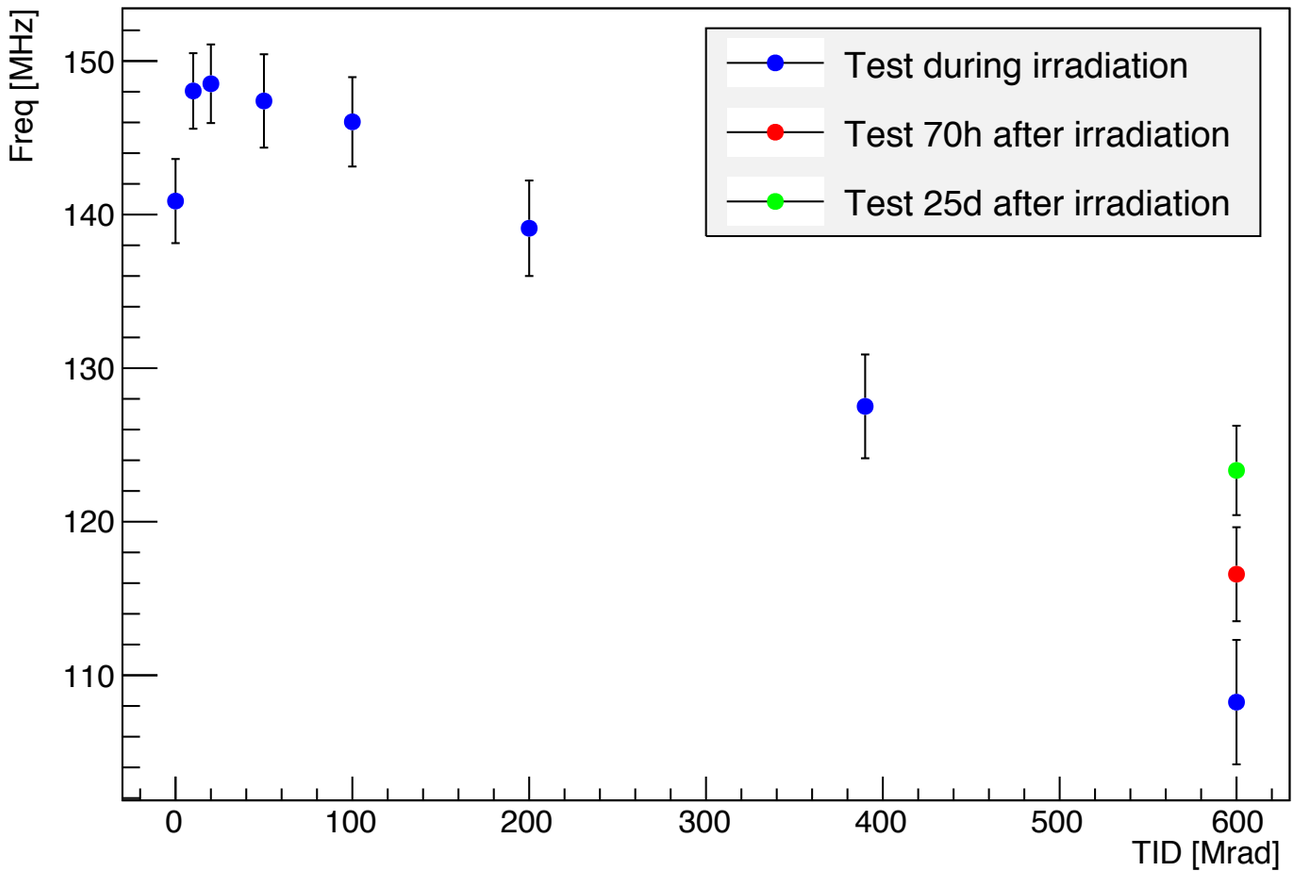
- Peak time for Cd=80fF: increase with TID then partial recovery
- Amplitude : no relevant variation seen

Noise



- Significant increase of the slope after irradiation
- Relevant recovery with annealing at room temperature
- At the typical C_{det} value (50 fF) the ENC variations are only in the order of 10%

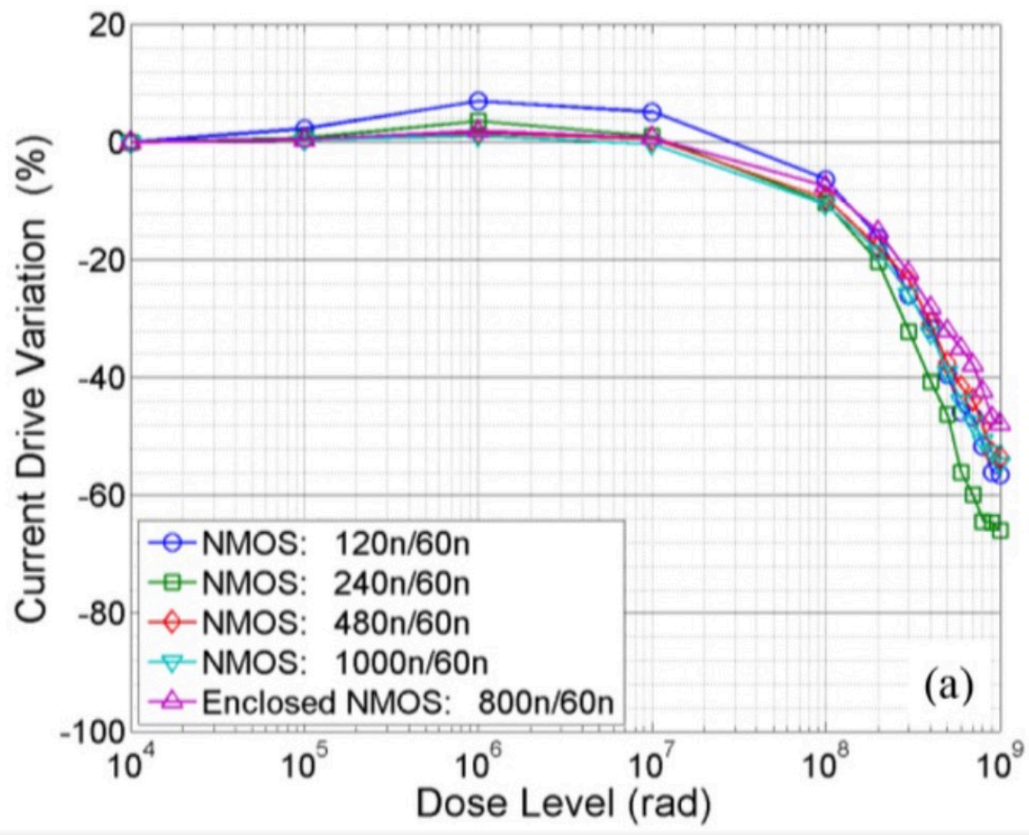
ToT frequency



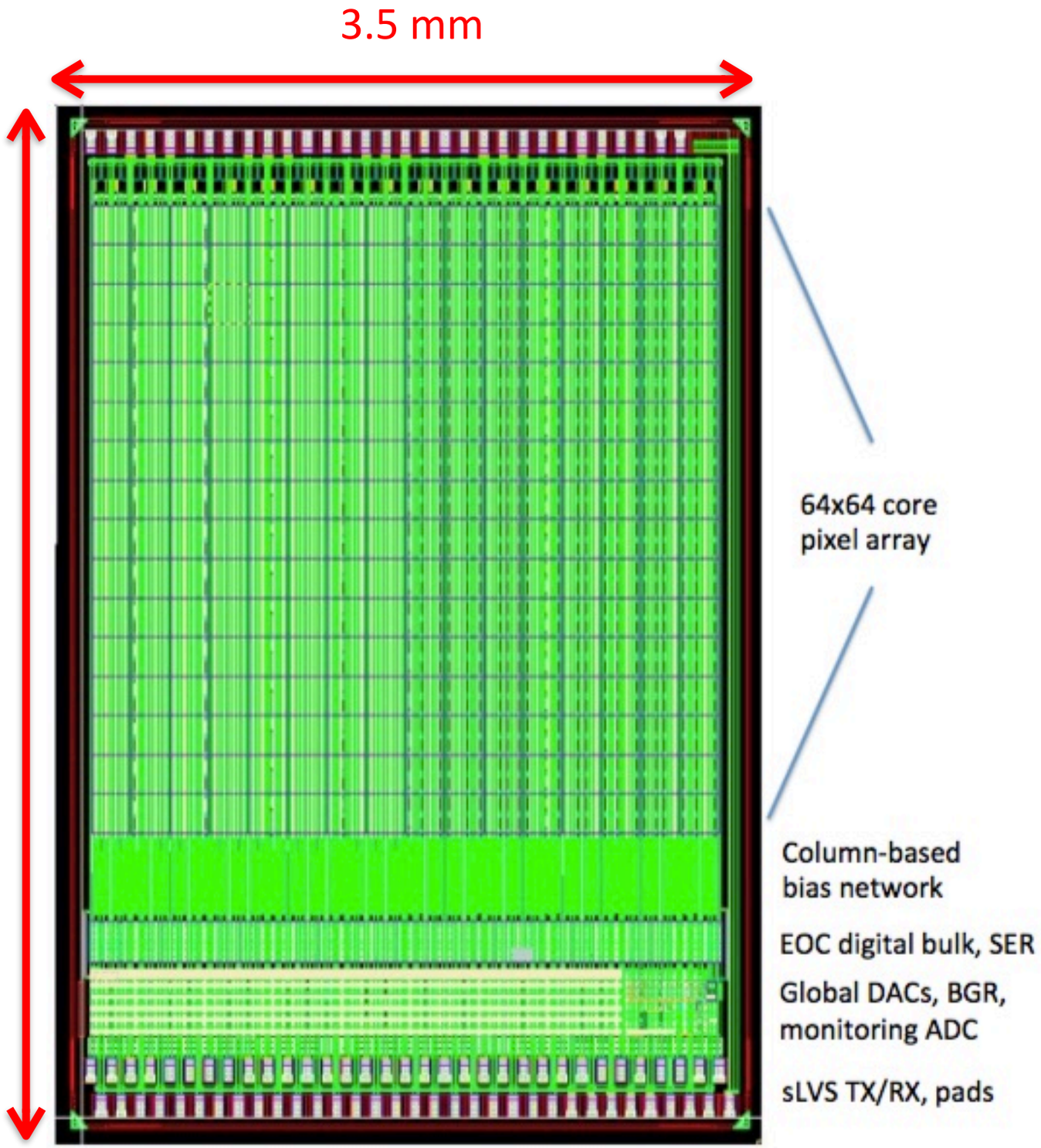
- Behavior compatible with measurements on single 65 nm devices (1)
- Increase of NMOS current at few Mrads due to charge trapping in the oxide
- Subsequent decrease due to interface states

(1) M. Menouni et al., "1-Grad total dose evaluation of 65 nm CMOS technology for the HL-LHC upgrades," Journal of Instrumentation, 2015.

- Local oscillator set to 140 MHz
- Slow down with TID with partial recovery with time (annealing)
- Frequency dispersion between pixels around 2% RMS
- This effect can be recovered by tuning the global current which control the oscillation frequency

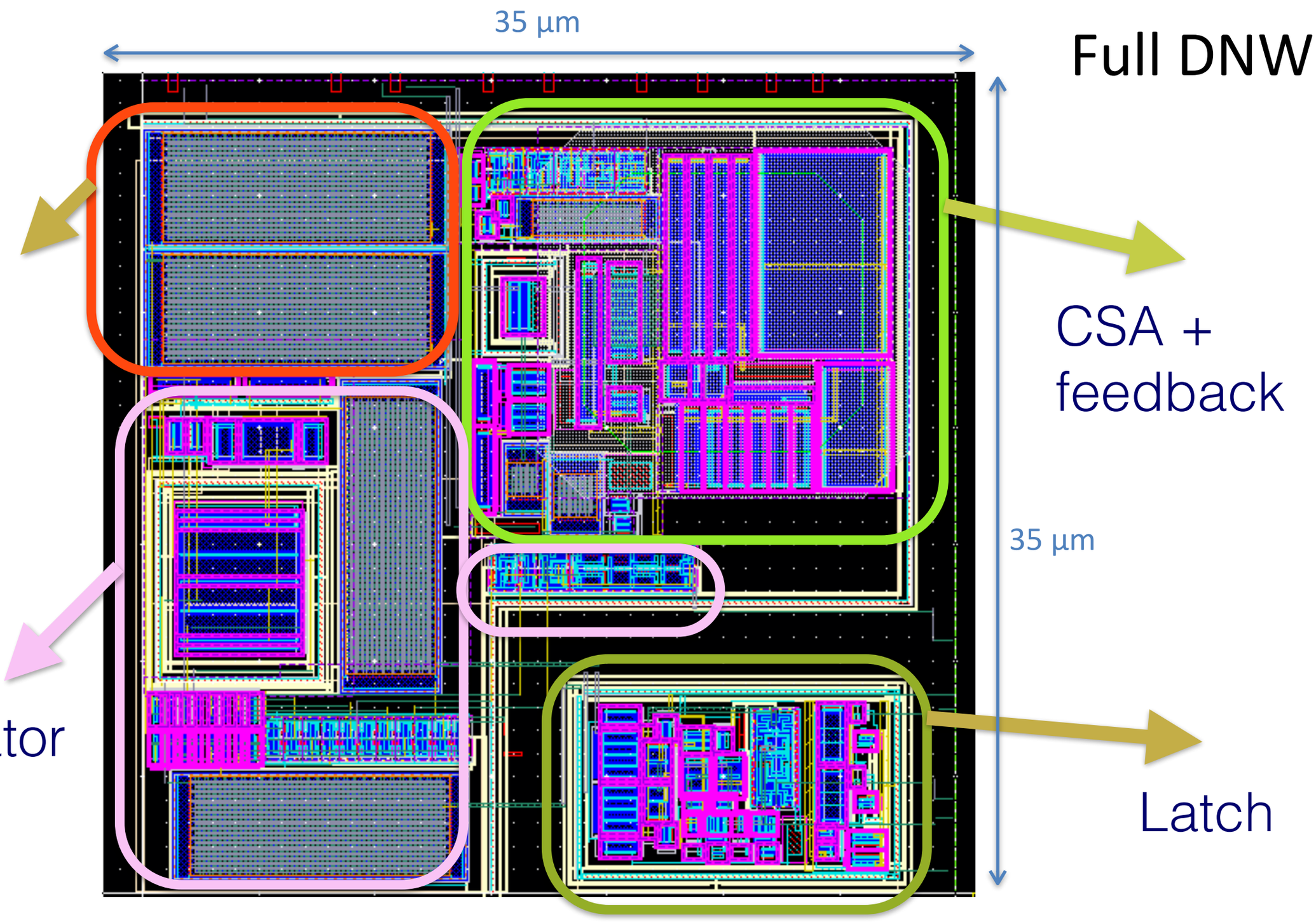


CHIPIX65 demonstrator

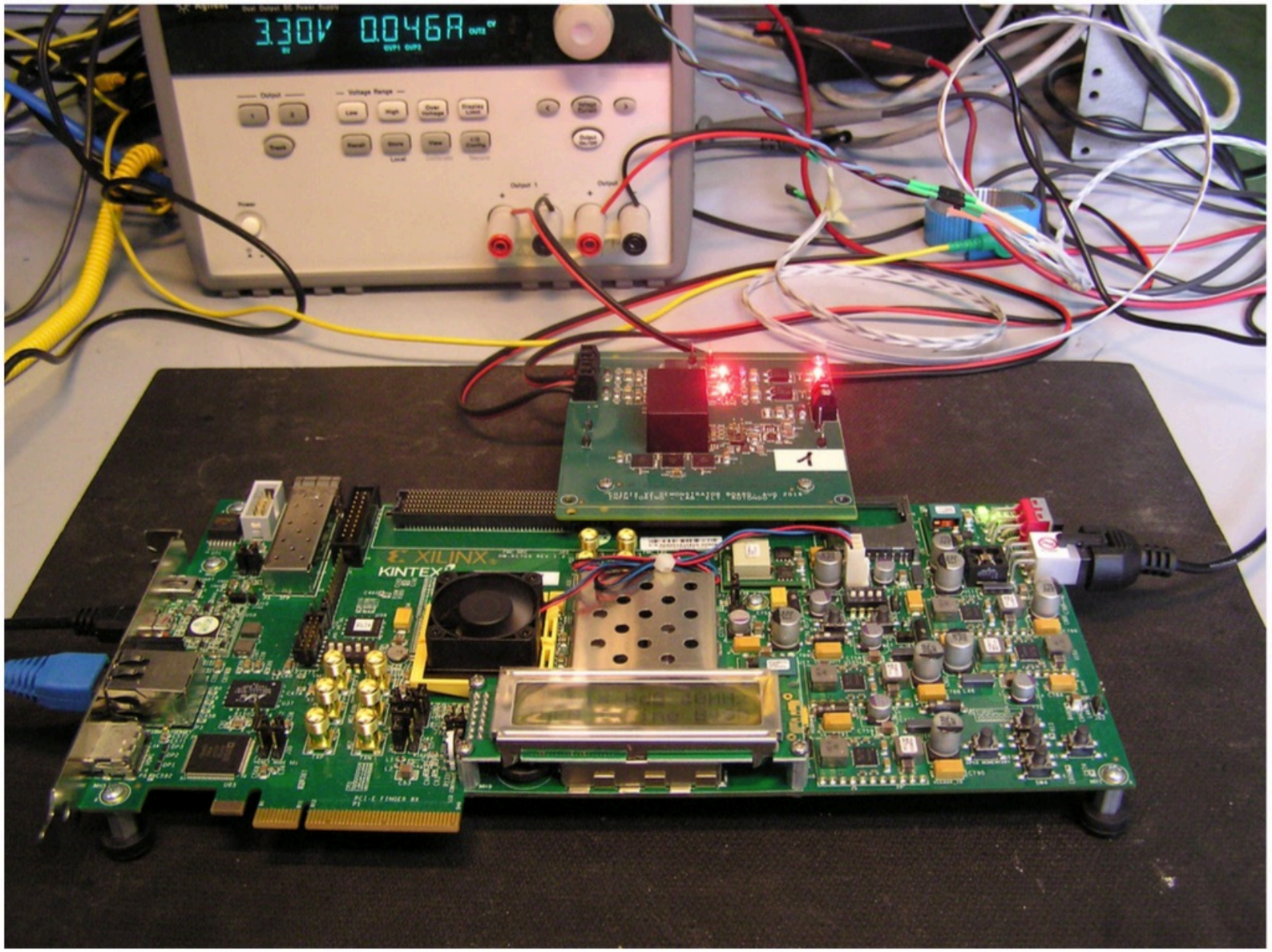


- 64x64 pixels with 50 µm x 50 µm pixel size
- Contains the building blocks designed by INFN groups in view of RD53A
- 2 different flavors of analog front-ends (Torino and Bergamo/Pavia)
- Realistic digital architecture complaint with the 3 GHz/cm^2 requirement (IO at 320 MHz)
- Complete biasing and monitoring scheme
- MPW (Multi Project Wafer) submission done in July 2016)

Analog cell layout (35x35 µm²)

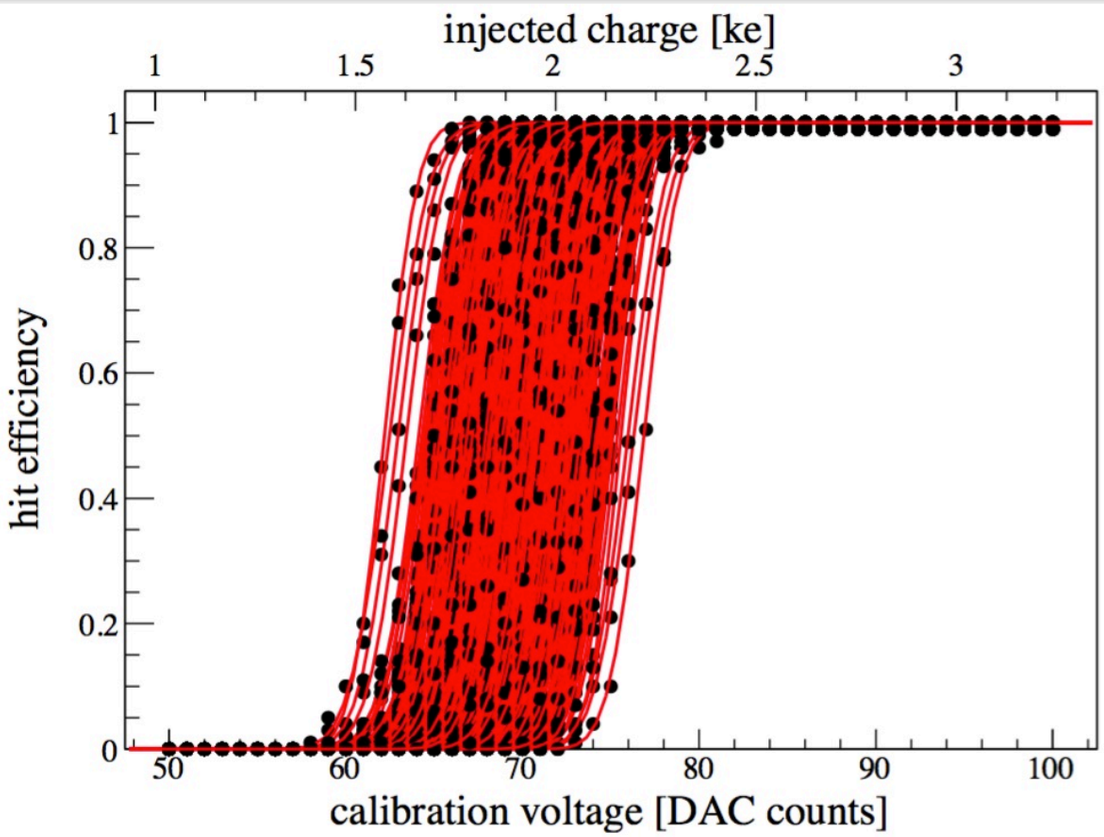


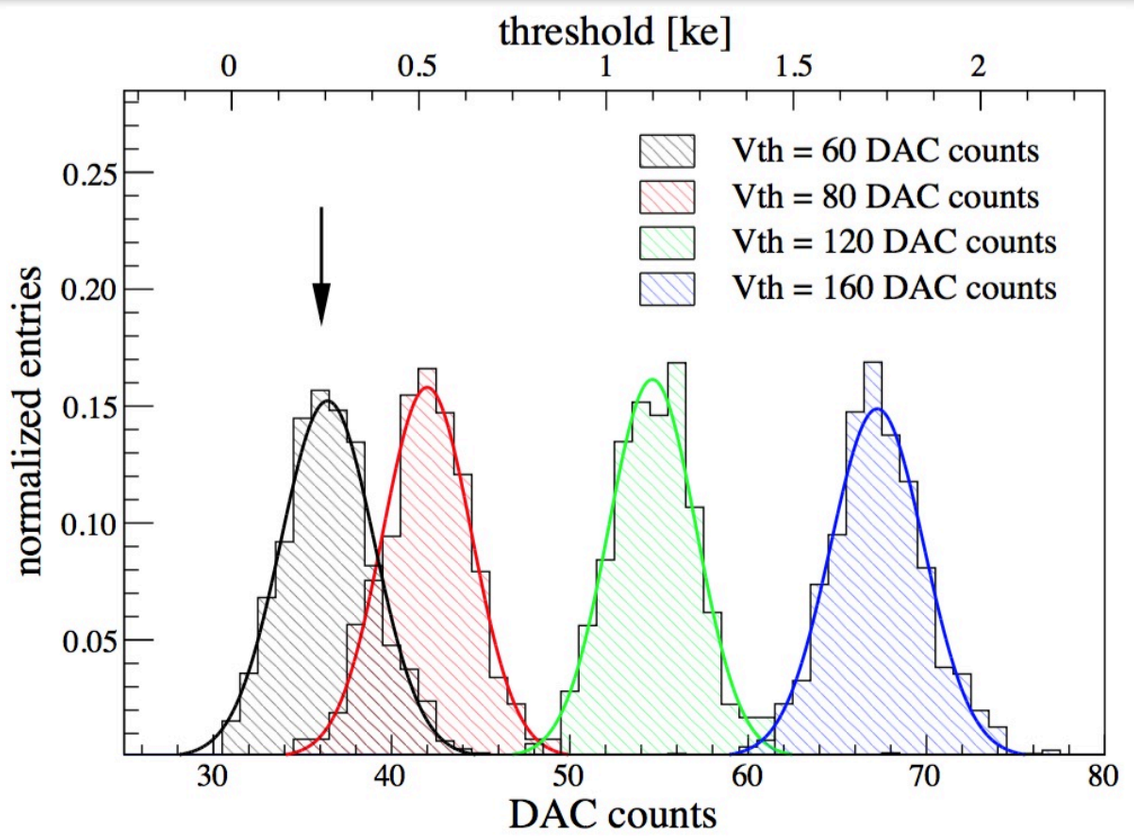
Test setup



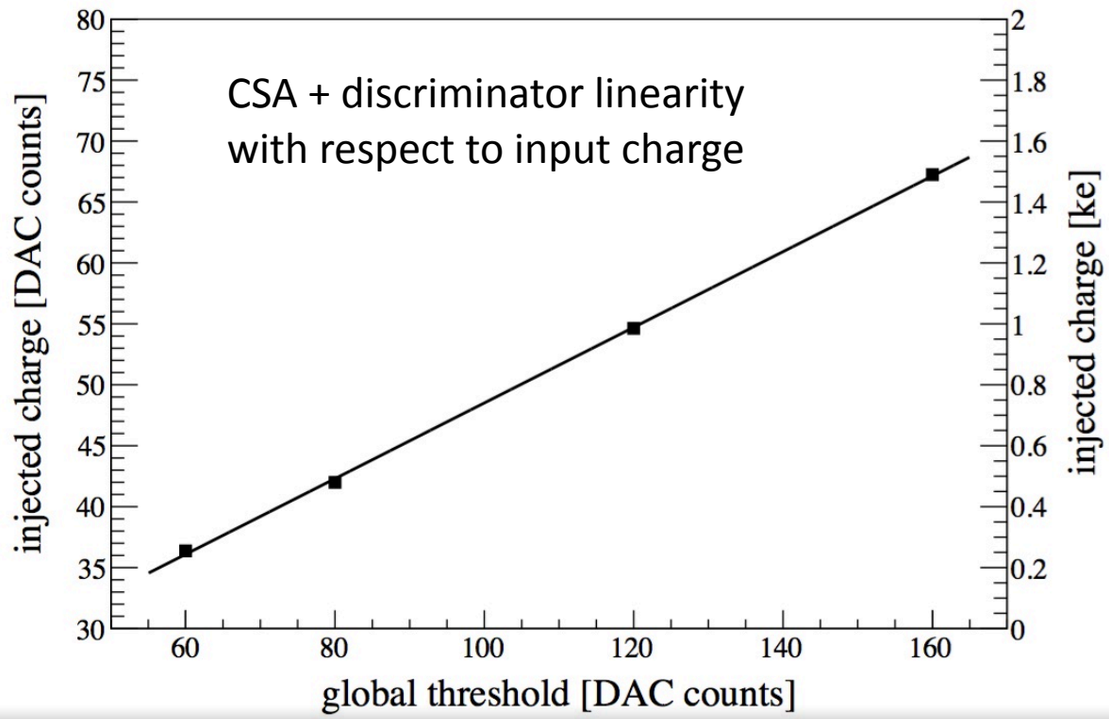
- Full digital/ASIC FPGA interface
- Chip wire-bonded to a custom test board
- FPGA Xilinx Kintex-7 evaluation board
- LabView data acquisition test interface

Threshold distribution

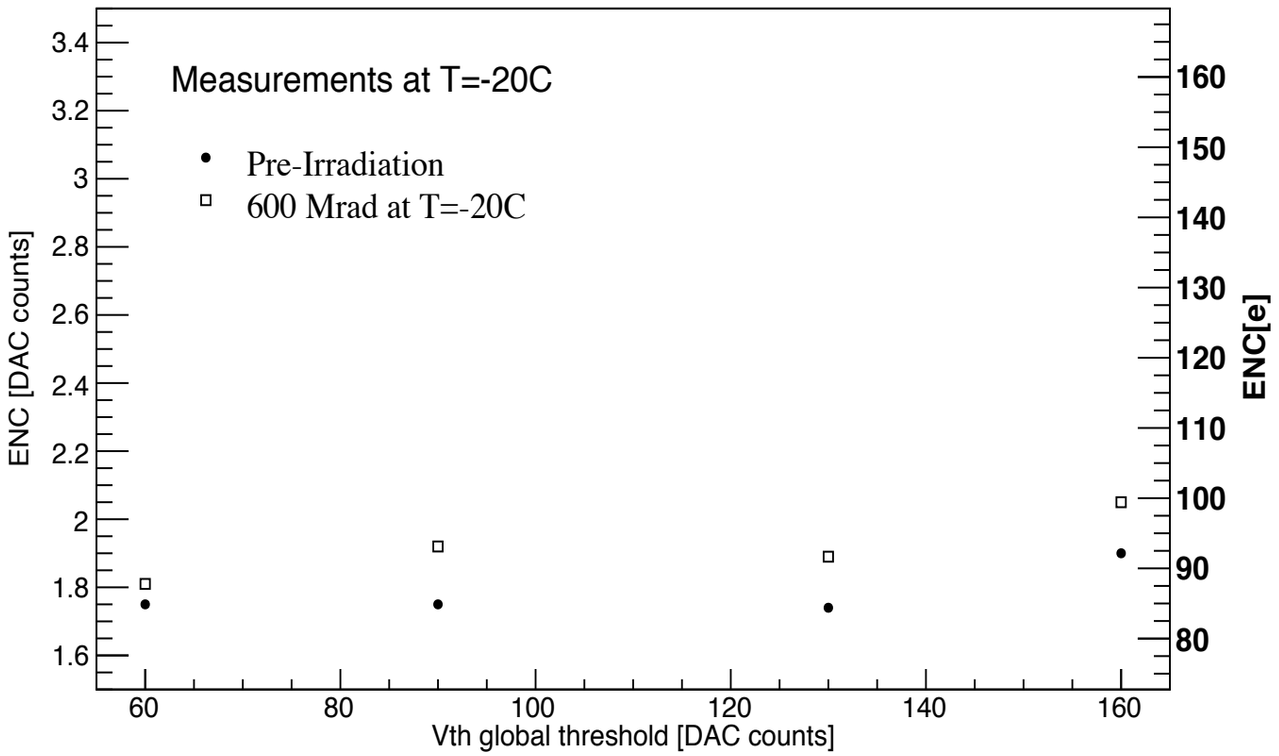


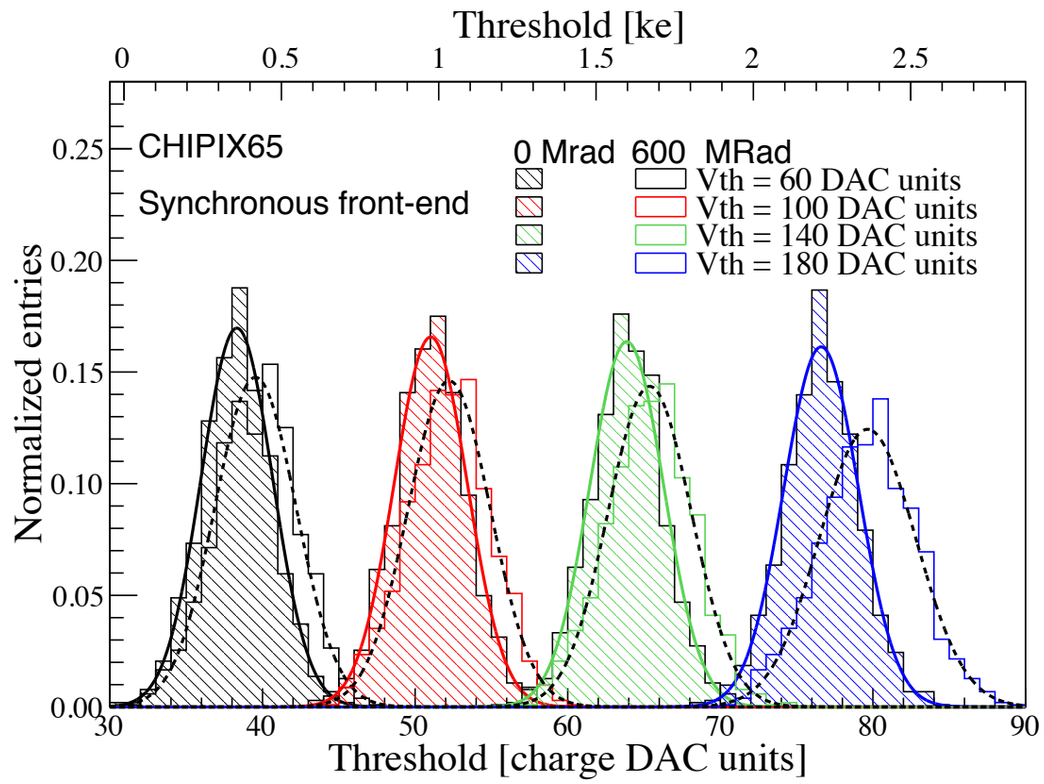


- The S-curves have been obtained for 1024 pixels (left)
- The procedure has been reproduced for different values of the global threshold
- Measurements show that the front-end can be operated at very low thresholds (around 300 electrons)
- The threshold dispersion is around 100 electrons

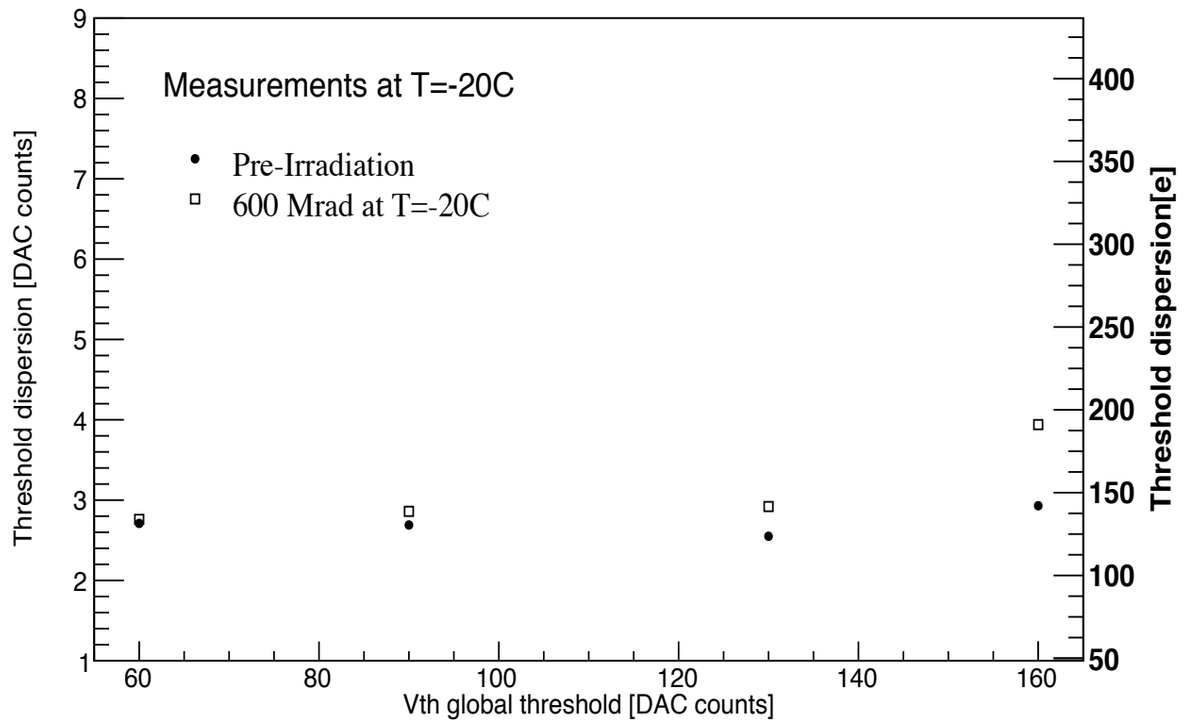


Irradiation results at -20°C

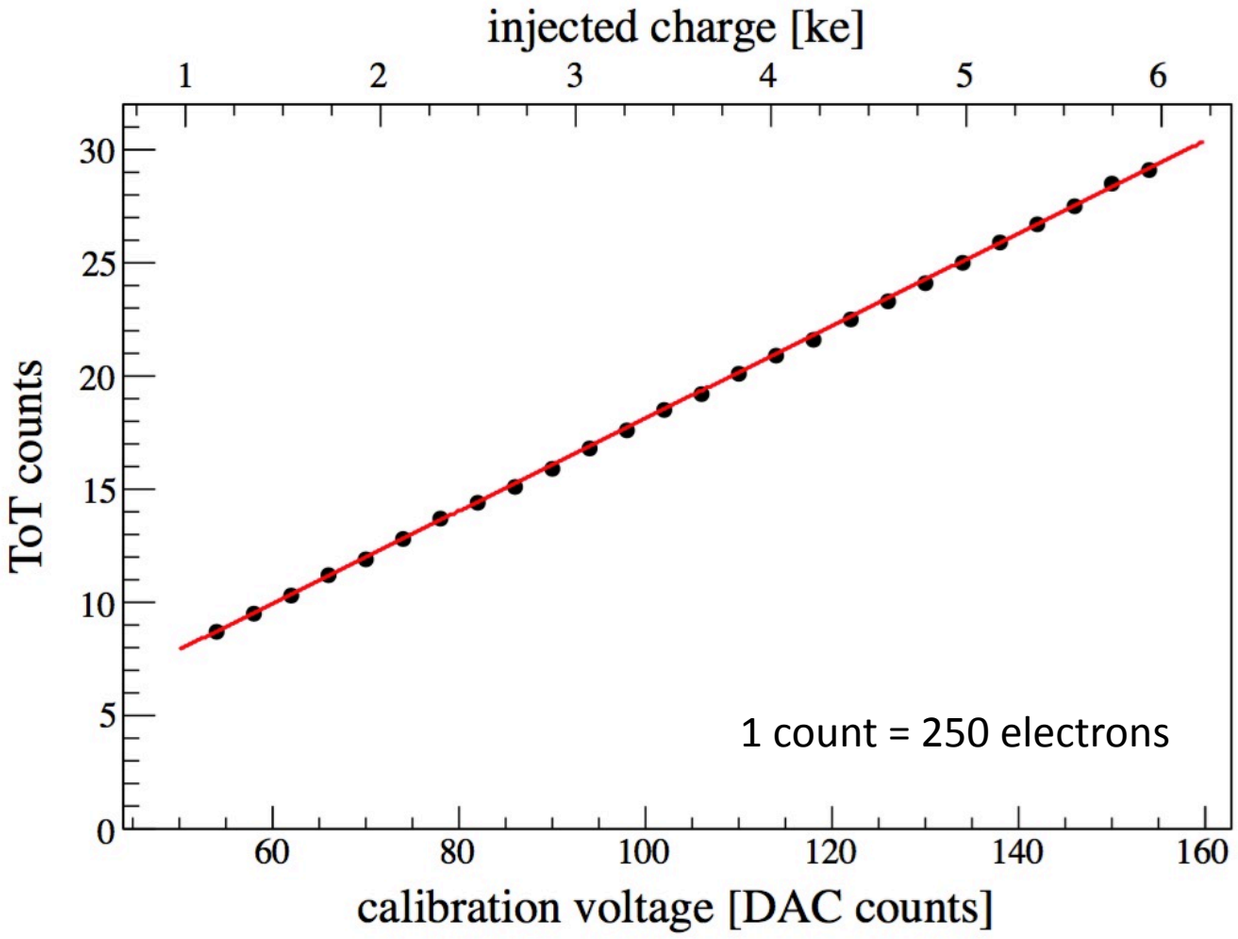


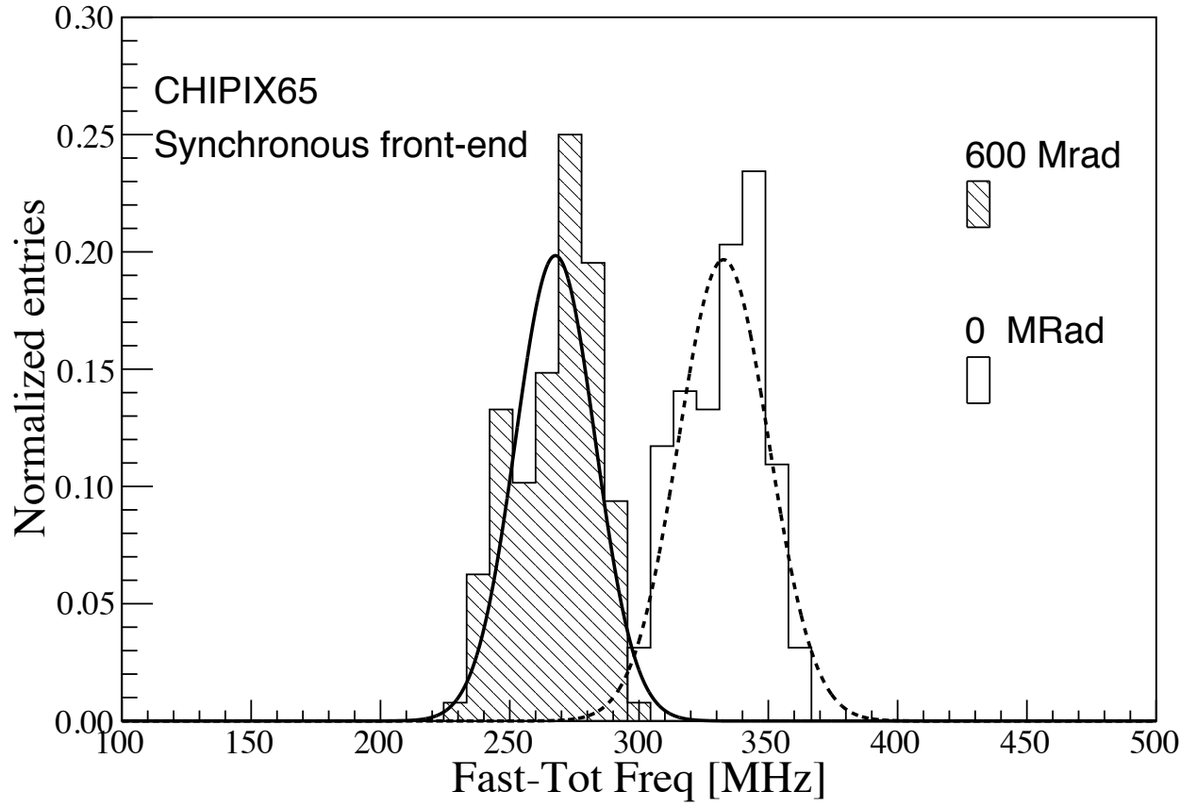


- The ENC increases of about 10% after irradiation
- The threshold dispersion increase is instead very limited at low global threshold values (< 1000 e-), which are the operating ones
- Radiation has a larger impact at higher thresholds



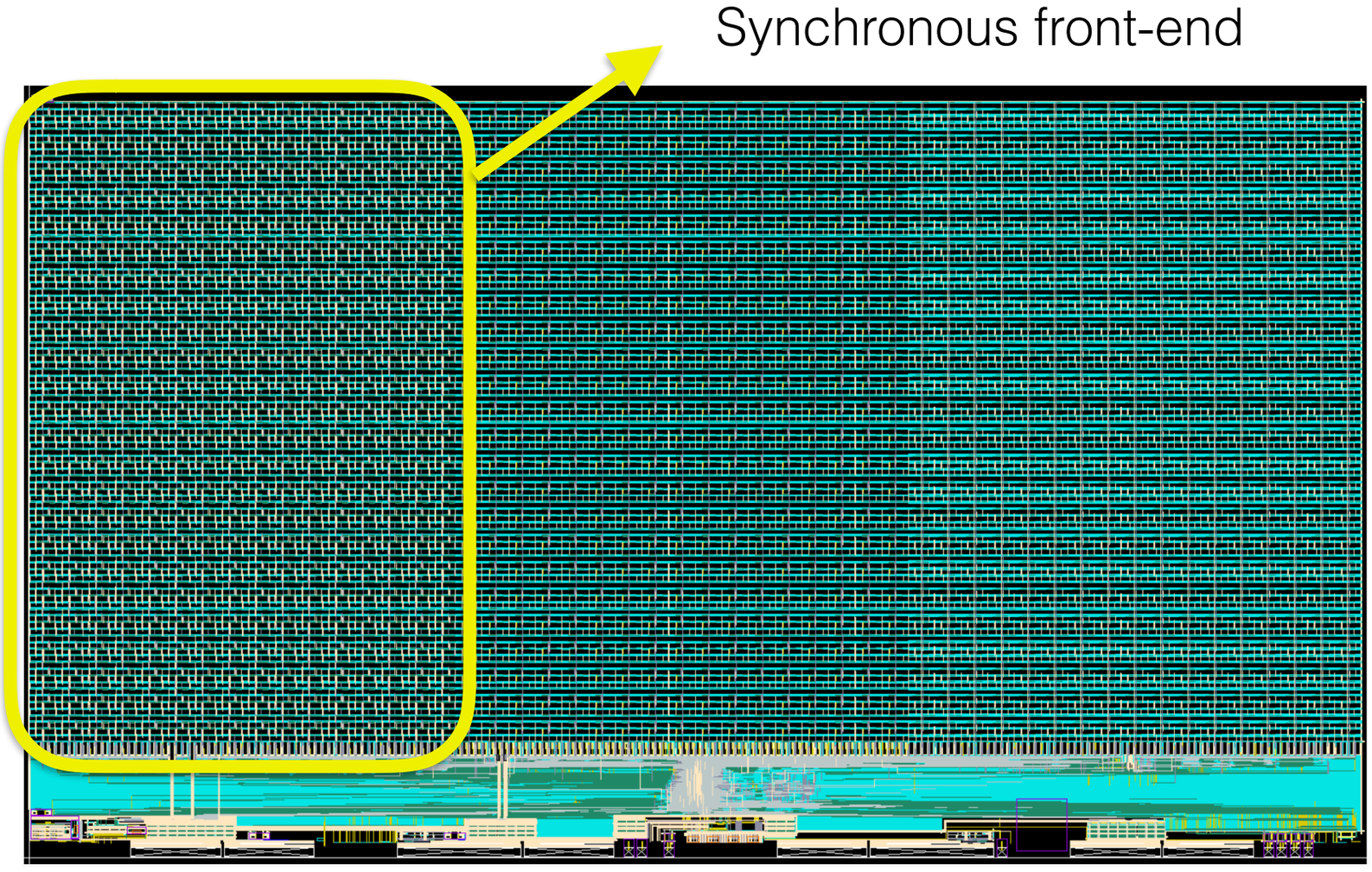
ToT





- Fast ToT oscillation enabled with a **320 MHz** frequency
- Information digitized with a 5-bit counter
- ToT linearity for the single pixel verified
- RMS of the ToT value around 13% of the mean value, in agreement with CAD simulations

RD53A demonstrator



- Matrix of 400 (cols) x192 (rows) pixels
- Three analog FEs
- Designed taking into account effects of full chip like voltage drops
- Submission planned for June 2017

- Further improvement with respect to the CHIPIX65 demonstrator based on prototype measurements:
  - Separate ground line for the Krummenacher feedback to minimize ToT variations for voltage drop compensation
  - Addition of inverters at the input of configuration bit lines for noise minimization

Simulation results for RD53A

- A full set of simulations has been performed to characterize the front-end before the submission:
  - Post-layout
  - Corners: these simulations allow to check the performance of the circuit in extreme cases of process, voltage and temperature

	Typ Ro1	Typ Ro2	Typ Ro3	Typ Op1	Typ Op2	Typ Op3	Lv_ Op1	Lv_ Op2	Lv_ Ro1	Lv_ Ro2	FF	SS
Model	TT	FS	SF	TT	FS	SF	FS	SF	FS	SF	FF	SS
VDD	1.2	1.2	1.2	1.2	1.2	1.2	1.08	1.08	1.08	1.08	1.32	1.08
T	27	27	27	-20	-20	-20	-20	-20	27	27	-40	80

Simulation results for RD53A

	Typ Ro1	Typ Ro2	Typ Ro3	Typ Op1	Typ Op2	Typ Op3	spec
Charge sensitivity [mV/ke]	42.6	42.6	41.9	42.2	42.1	41.2	-
ENC rms [e]	67	66	68	62	62	62	<<126
Threshold dispersion σ(Qth) rms [e]	93						<<126
$\sqrt{(ENC^2 + \sigma(Qth)^2)}$ [e]	122						≤126
In-time overdrive [e-]	50	50	50	50	50	50	≤ 600
Analog current consumption [μA/pixel]	3.33	3.42	3.29	3.24	3.28	3.23	≤ 4
Average digital current consumption [μA/pixel]	1.82	1.86	1.64	1.58	1.68	1.53	-
Time-walk [ns]	9.5	9.4	9.4	8.6	8.7	8.5	-
Time over threshold @ 6 ke [ns]	120.7	117.6	121.2	117.5	116.8	117.7	-
Phase Margin [deg]	64.6	65.2	63.9	62.2	63.2	60.8	-

Simulation results for RD53A

	Lv Op1	Lv Op2	Lv Ro1	Lv Ro2	FF	SS	spec
Charge sensitivity [mV/ke]	42.2	38.2	42.6	38.9	46.3	38.8	-
ENC rms [e]	63	70	60	73	60	72	<<126
Threshold dispersion σ(Qth) rms [e]							<<126
√(ENC² + σ(Qth)²) [e]							≤126
In-time overdrive [e-]	100	100	100	100	50	50	≤ 600
Analog current consumption [μA/ pixel]	2.91	2.86	3.05	2.93	4.03	2.94	≤ 4
Average digital current consumption [μA/pixel]	1.67	1.63	1.74	1.71	2.5	1.6	-
Time-walk [ns]	10.9	11.7	11.6	12.6	6.5	12.1	-
Time over threshold @ 6 ke [ns]	117.2	124.8	118.1	120.5	115	128.3	-
Phase Margin [deg]	64.5	65.9	66	66.5	58.6	66.6	-

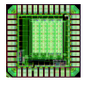
PhD activity summary

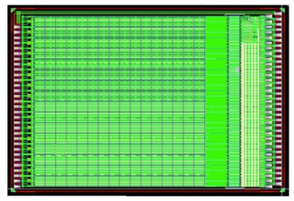
2014:

- Design and simulation of different analog blocks using the Cadence Virtuoso tool
- Layout implementation of the analog front-end and integration into a small chip (2x2 mm^2) submitted to the foundry: **VFE_1** (8x8 analog readout Pixel Matrix)

2015:

- VFE_1 test
- Design and submission of a second prototype (**VFE_2**)
- Testing and X-ray irradiation of VFE_2



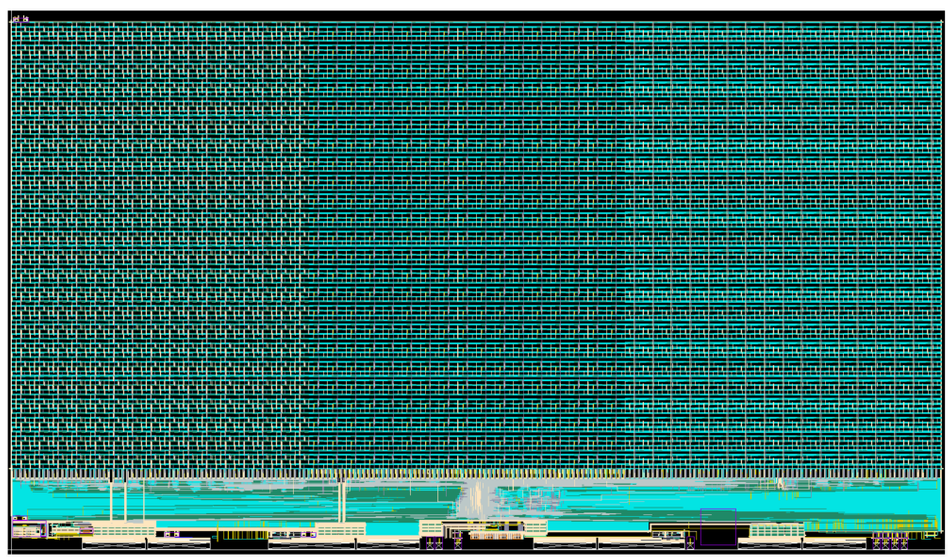


2016:

- VFE design for the **CHIPIX65 demonstrator** chip
- First measurements on this prototype

2017:

- Contribution to the **RD53A** design team for the analog front-end (AFE) design, responsible for the synchronous AFE



Conclusions

- In view of the Phase 2 upgrade of the HL-LHC experiments a new synchronous analog front-end for the readout of the silicon pixel detectors has been designed, featuring:
  - A single stage CSA with Krummenacher feedback
  - A switched capacitor offset compensated differential amplifier
  - A positive feedback latch which can be used as a local oscillator for fast ToT counting

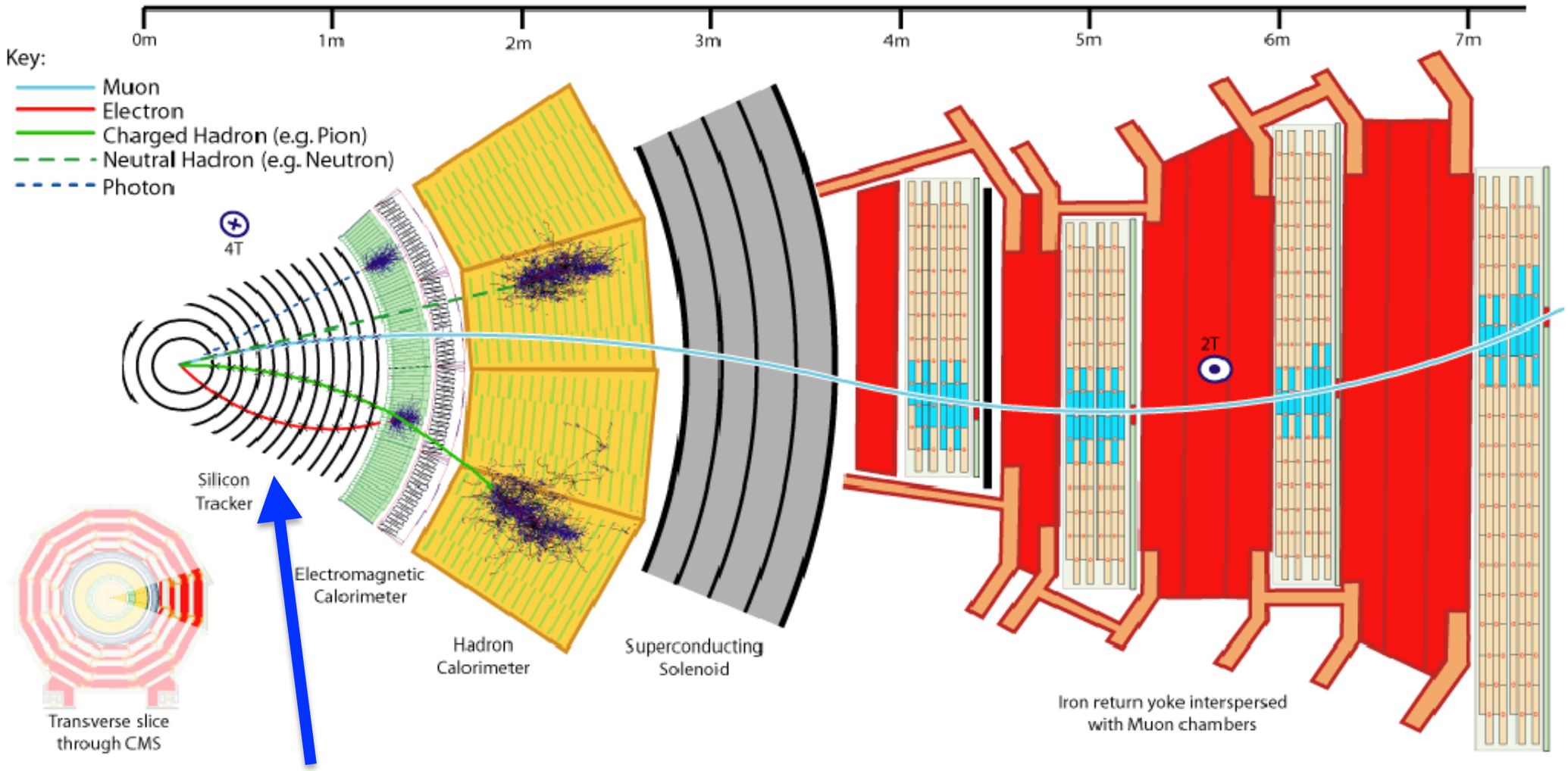
- Two small prototypes have been successfully submitted to the foundry and tested during 2015 with very promising results
  - Idea of “self-oscillating” comparator for fast ToT measurement works
  - Good ToT linearity in a wide range of input signals
  - Performance degradation after a TID = 600 Mrad is very limited

- The front-end is part of the large demonstrator chips designed by the CHIPIX65 and RD53A collaborations
  - First results on the CHIPIX65 chip are compliant with specifications
  - The chip is fully operational after a 600 Mrad irradiation at -20C
  - The RD53A chip is going to be submitted in June 2017

Thank you for your attention!

BACKUP

The CMS experiment

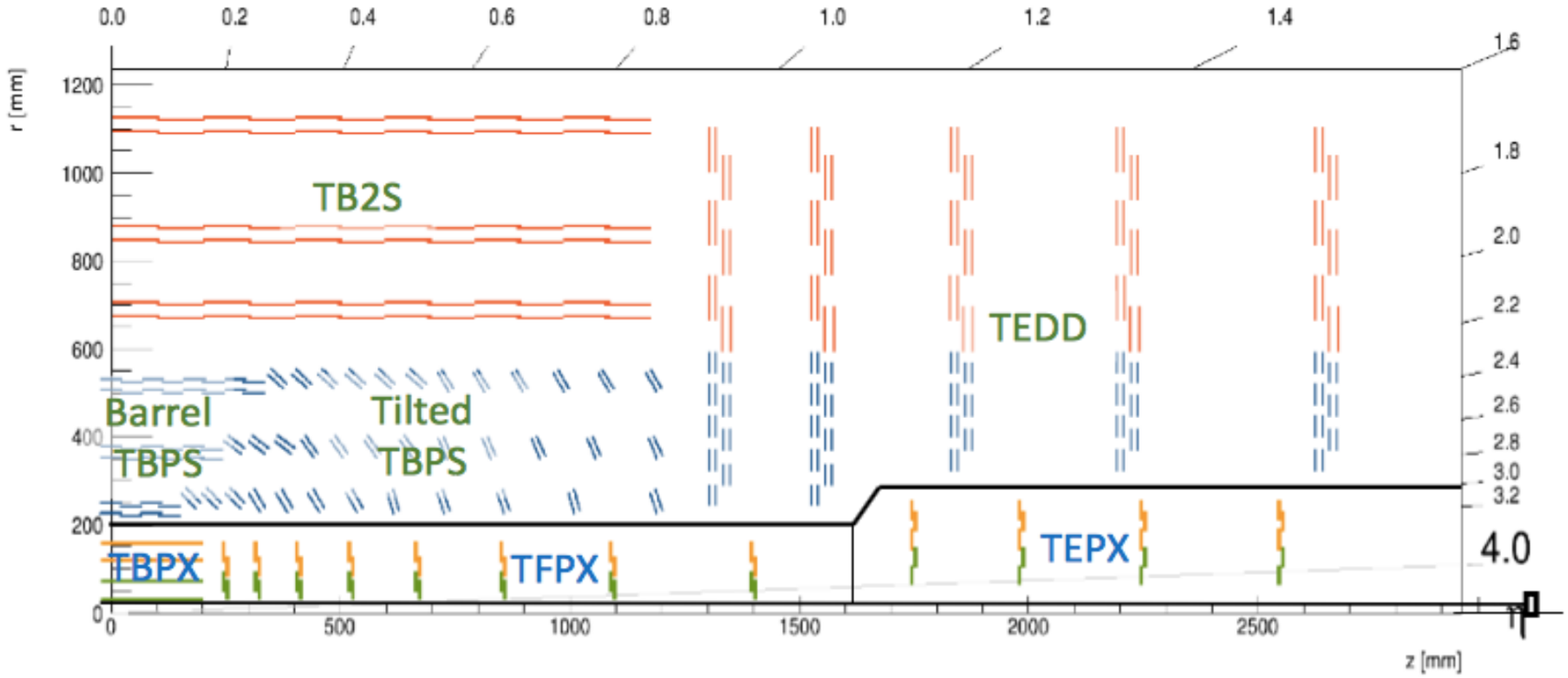


- **Silicon tracker** ⇒ Inner part of the CMS detector
  - Composed of pixels and strips layers
  - **Pixel detector** ⇒ Closest to the beam pipe

CMS tracker layout

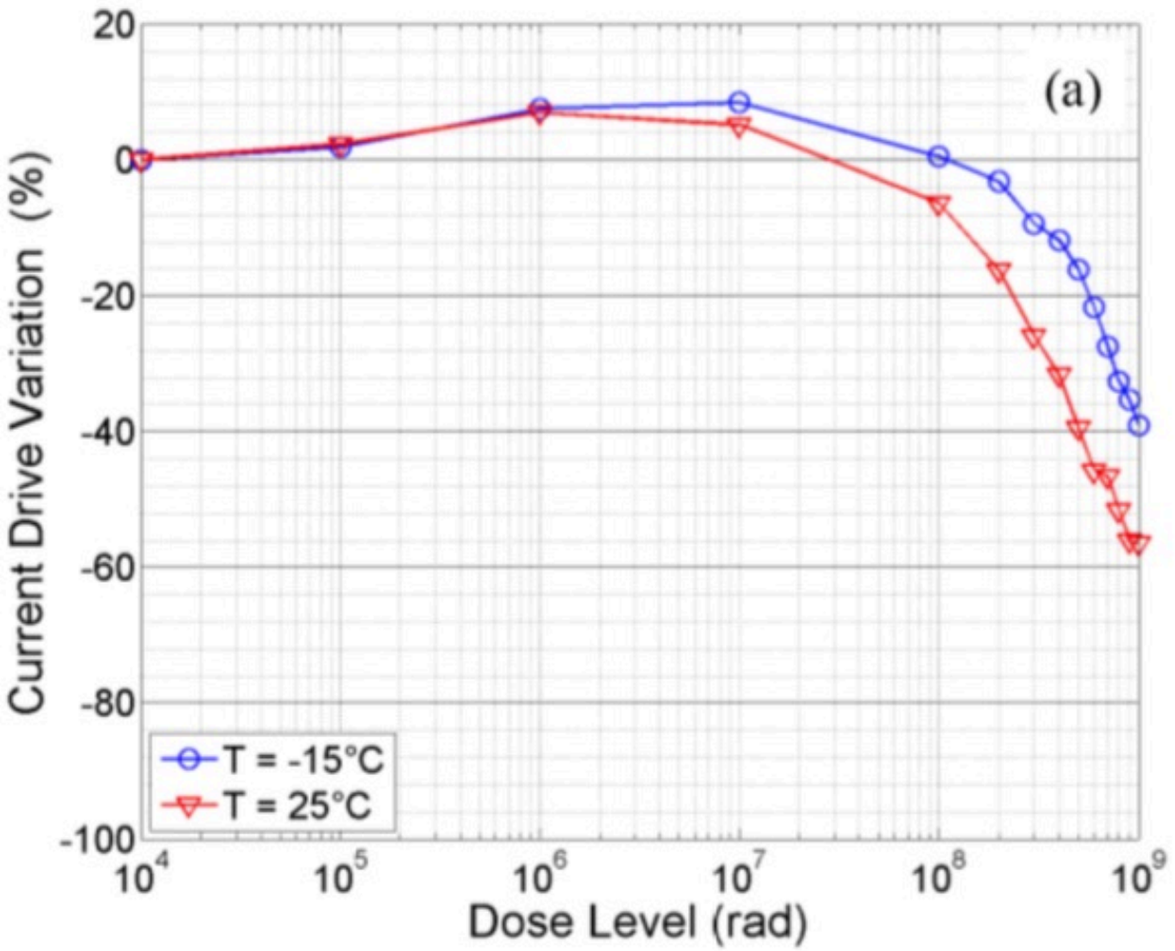
OT, Outer Tracker

IT, Inner Tracker

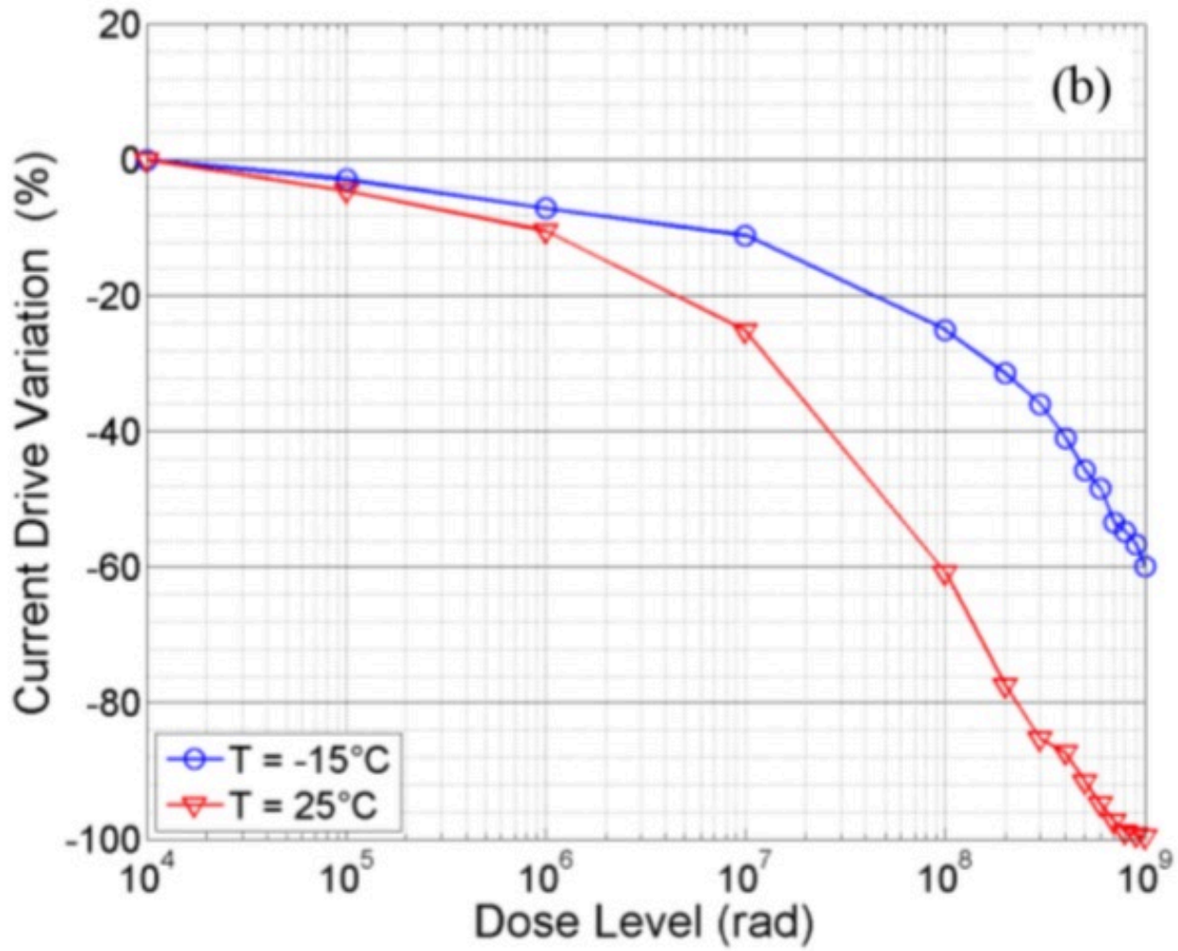


Radiation effects on 65 nm technology

NMOS



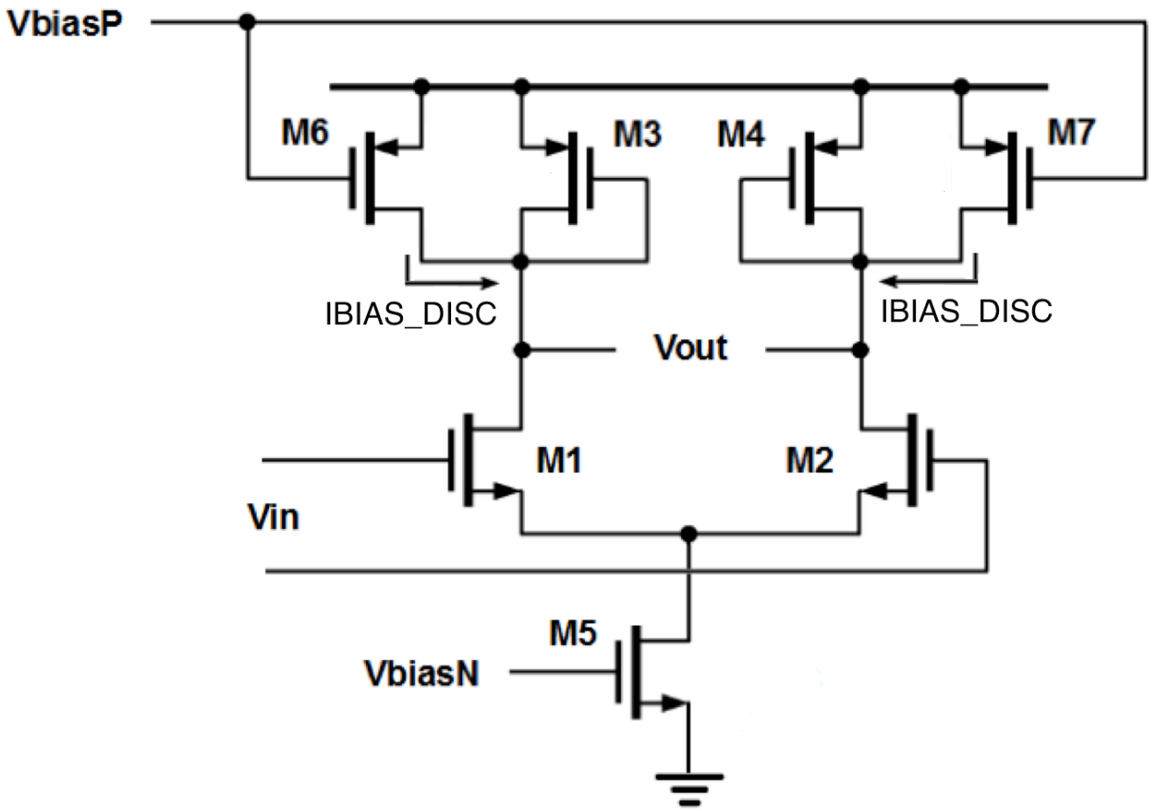
PMOS



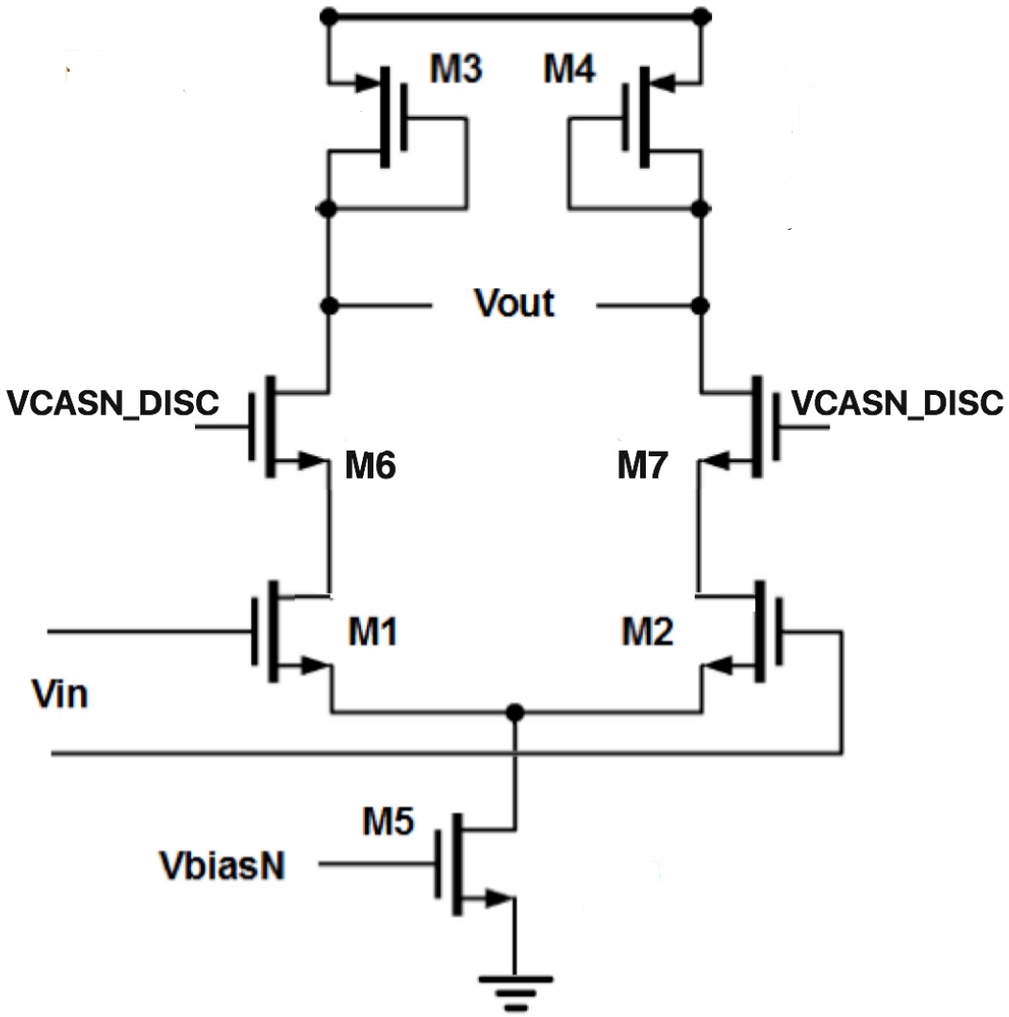
- Low temperature operation reduces the performance degradation

Differential Amplifier schematics

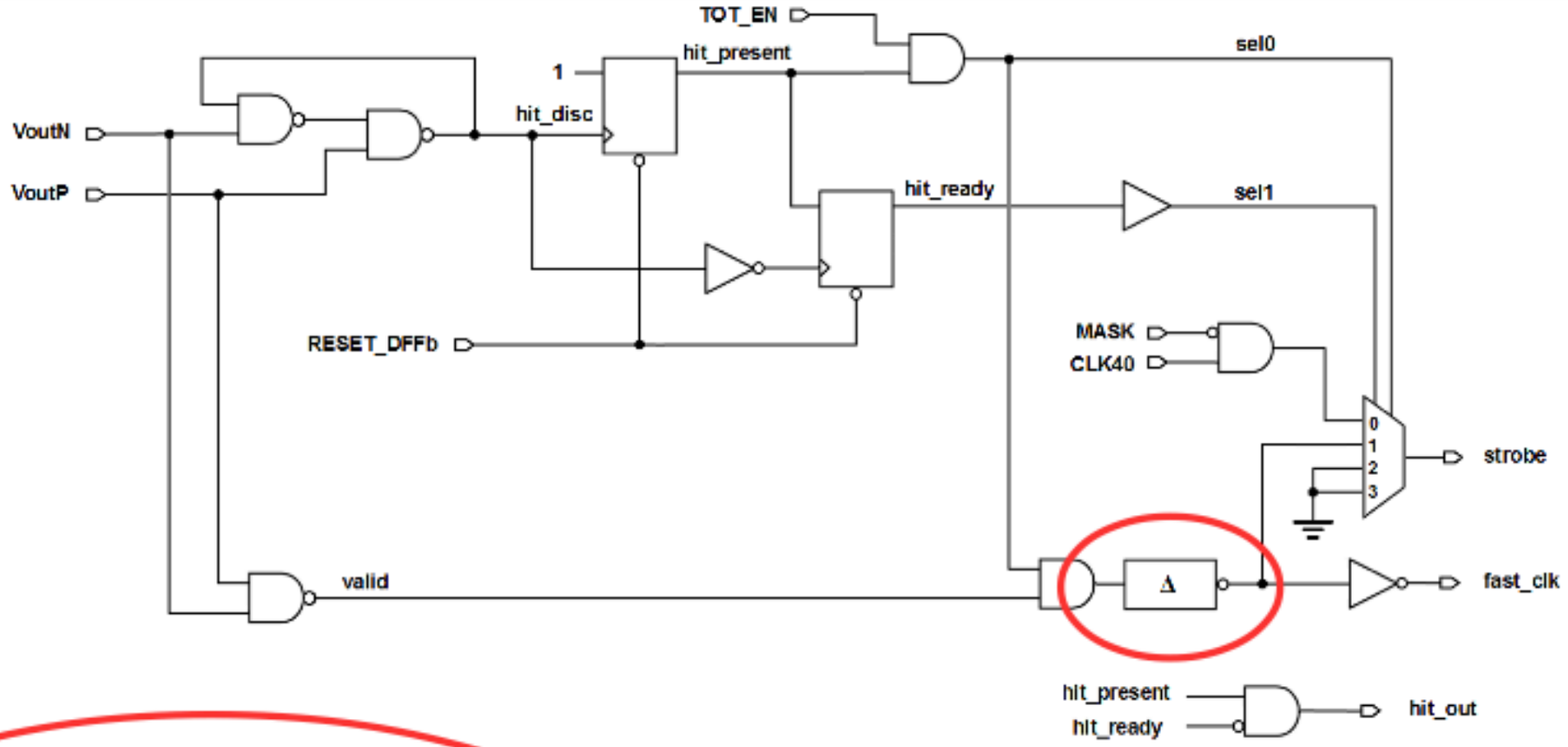
VFE_1 version

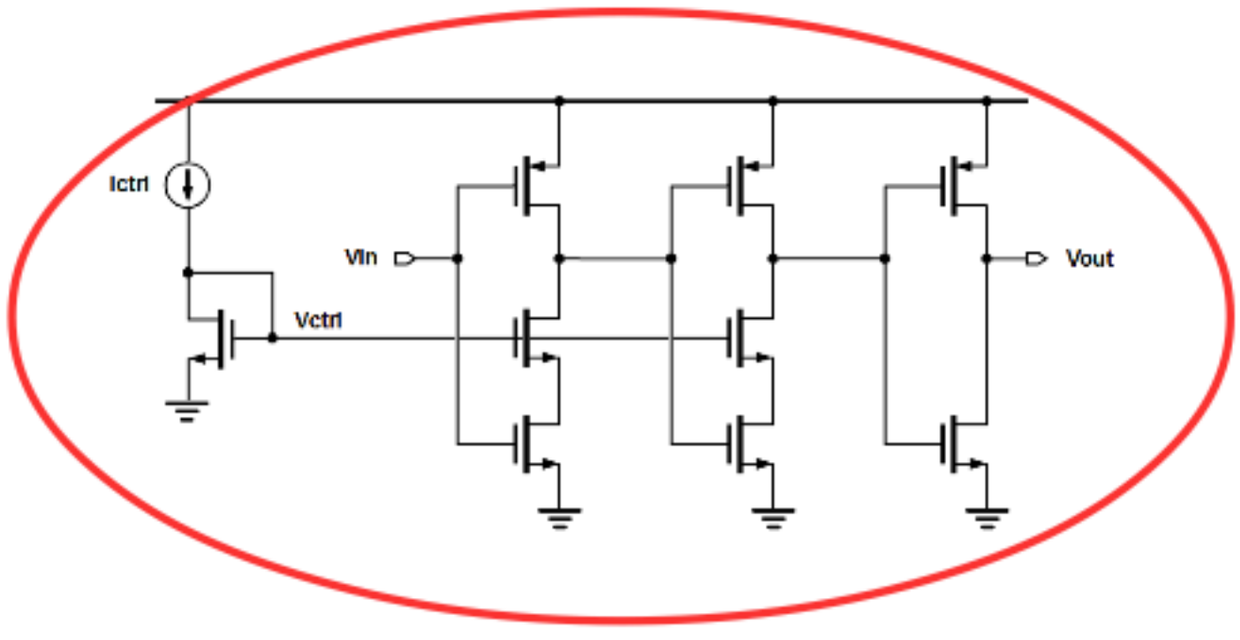


VFE_2 version



Hit logic





- This logic, inserted in the digital architecture, allows to switch between the two operating modes
  - SEL0 = 1 → Binary
  - SEL1 = 0 and SEL0 = 0 → Slow ToT
  - SEL1 = 1 and SEL0 = 0 → Fast ToT
- The delay element, based on current-starved inverters, allows to control the oscillation frequency by tuning the current value

Power consumption

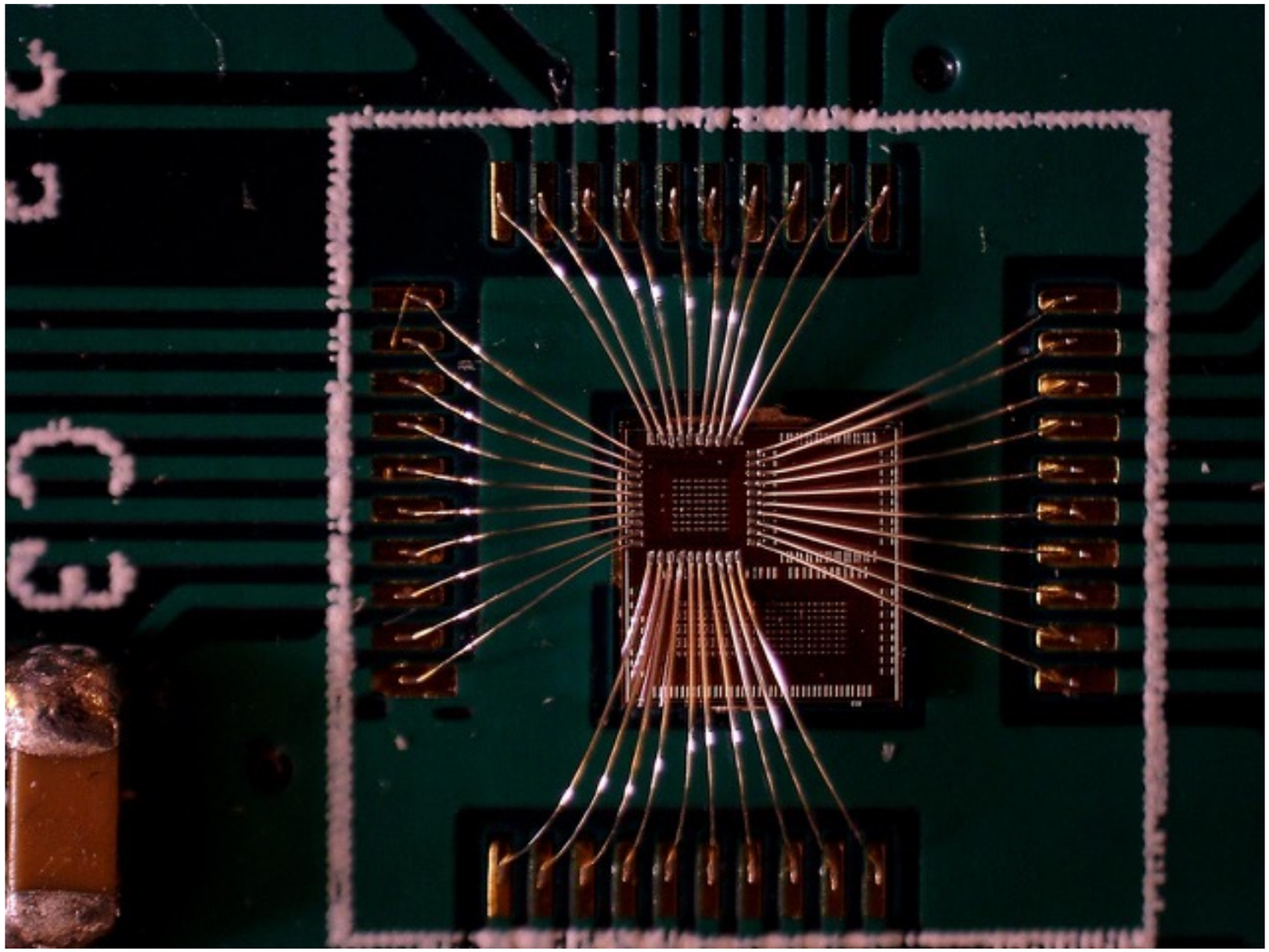
- Static current around 3.5 uA
  - Preamplifier -> 2.5 uA
  - Discriminator -> 1 uA

- Dynamic current (latch) around 0.8 uA

- The average total current is around 4.3 uA per pixel

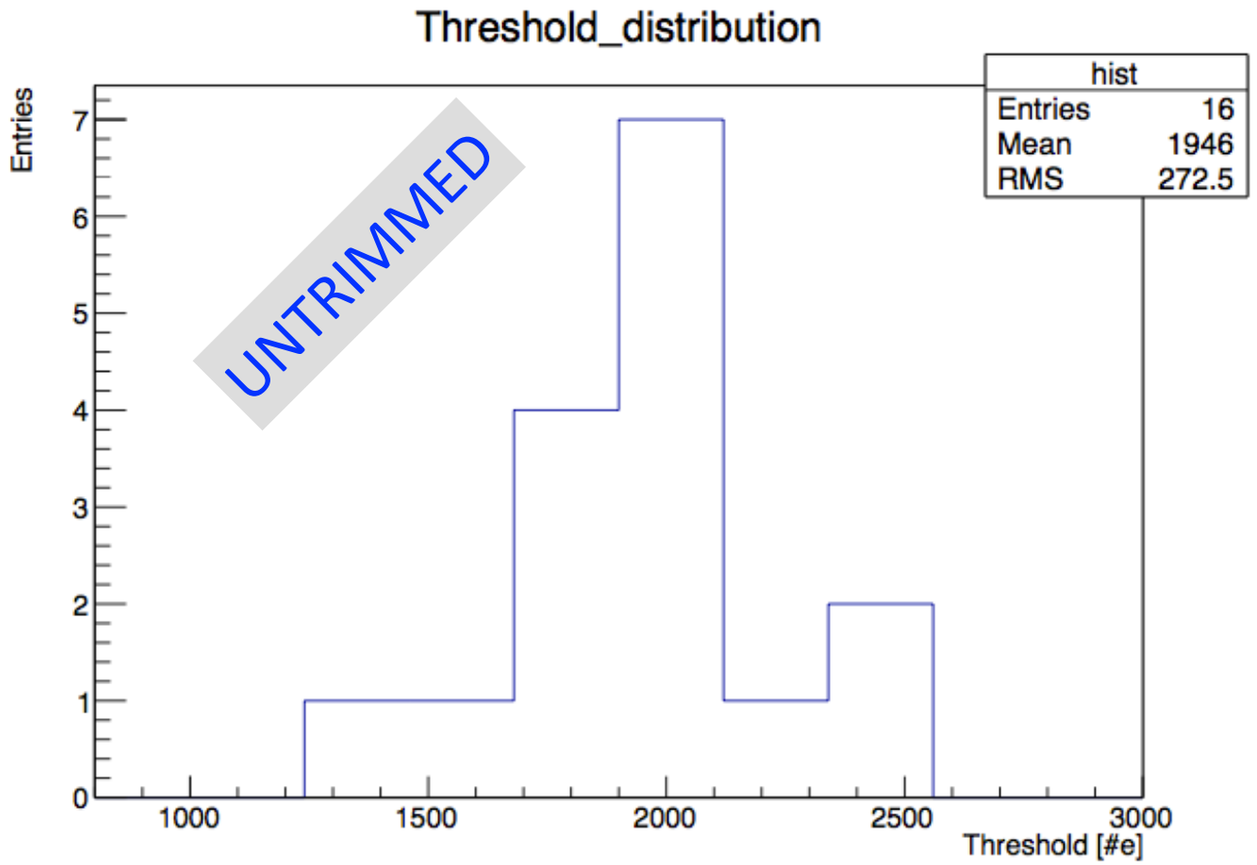
- Considering VDD = 1.2 V the total power consumption is around 5.2 uW
  - It corresponds to around 0.2 W/cm^2 considering a 50x50 um^2 pixel
  - OK ~ 50% of the 0.4 W/cm^2 required

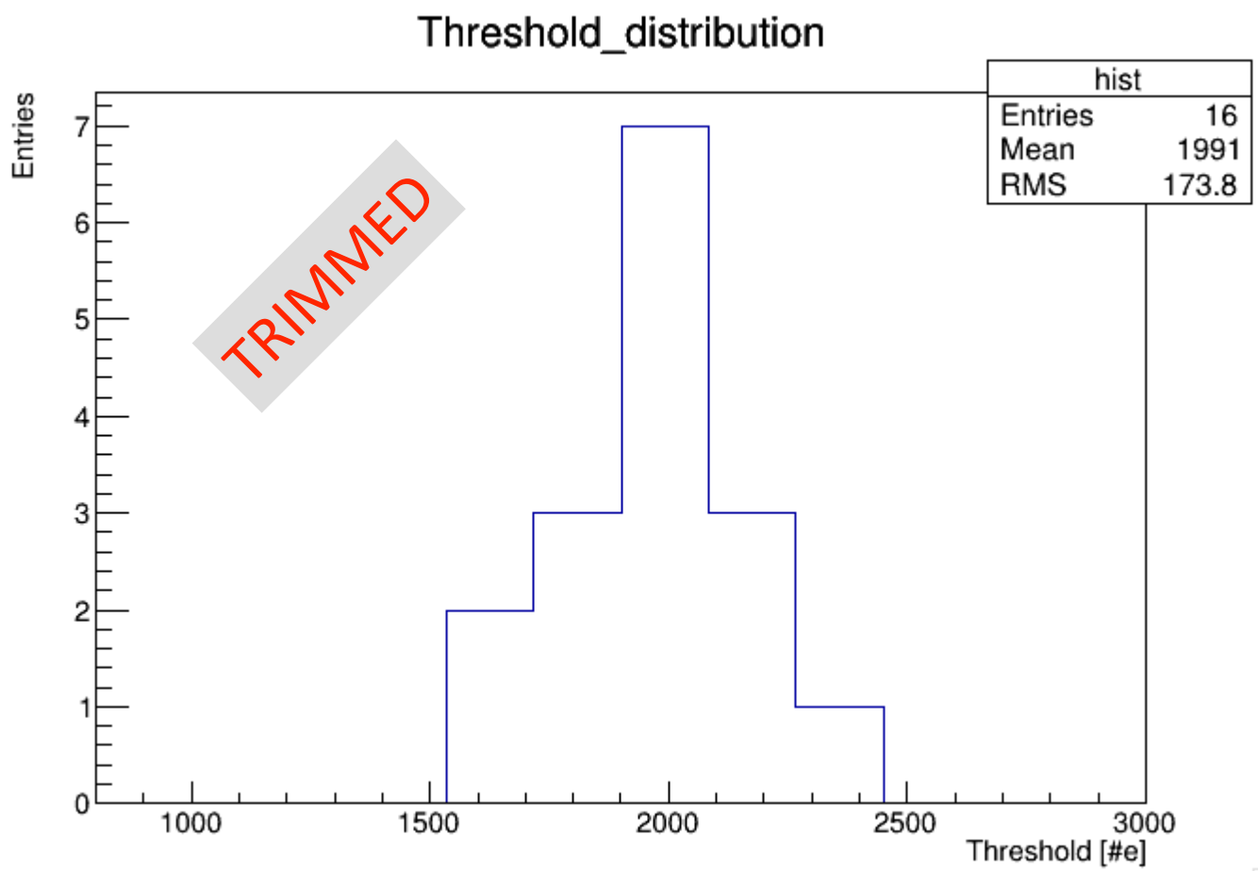
Pixel matrix wire-bonded to the PCB



Picture of the chip wire-bonded to the test board

Offset compensation - Measurement results





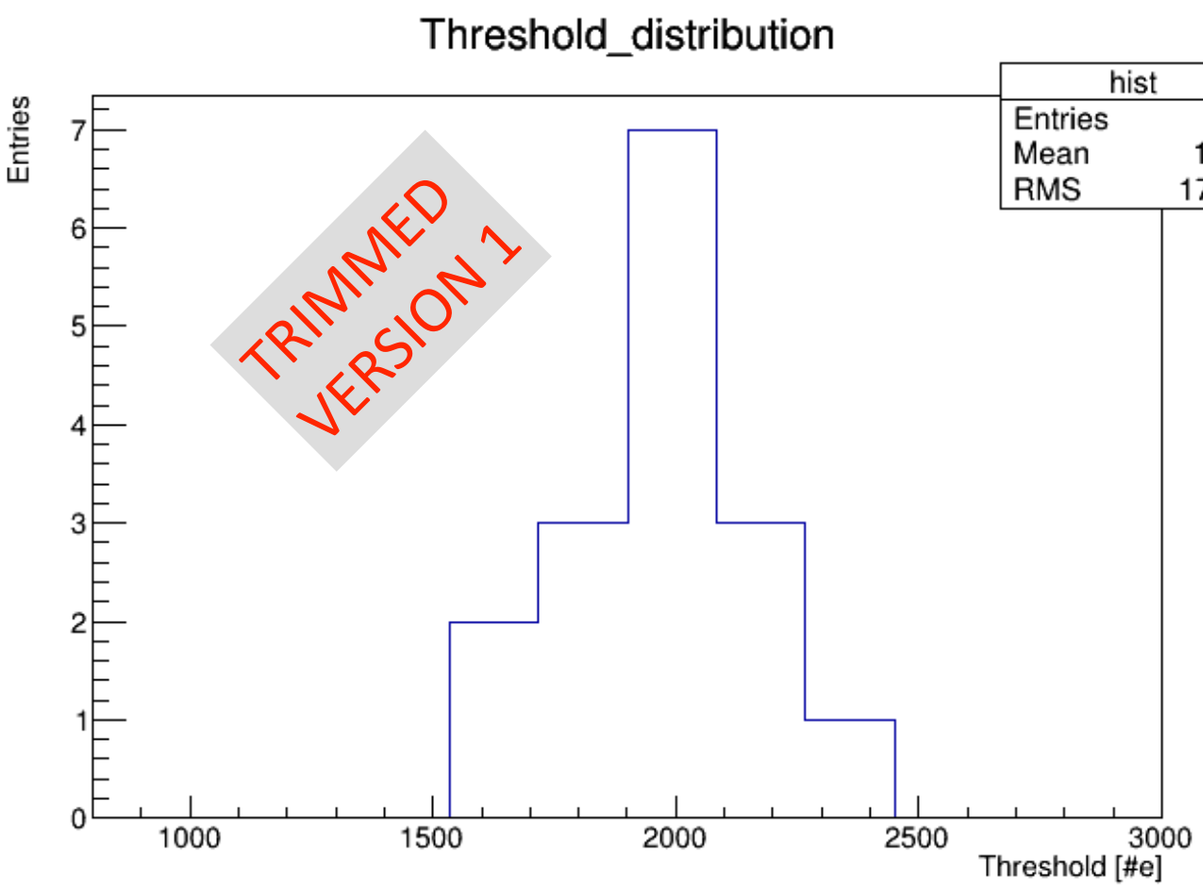
☹ It could be better

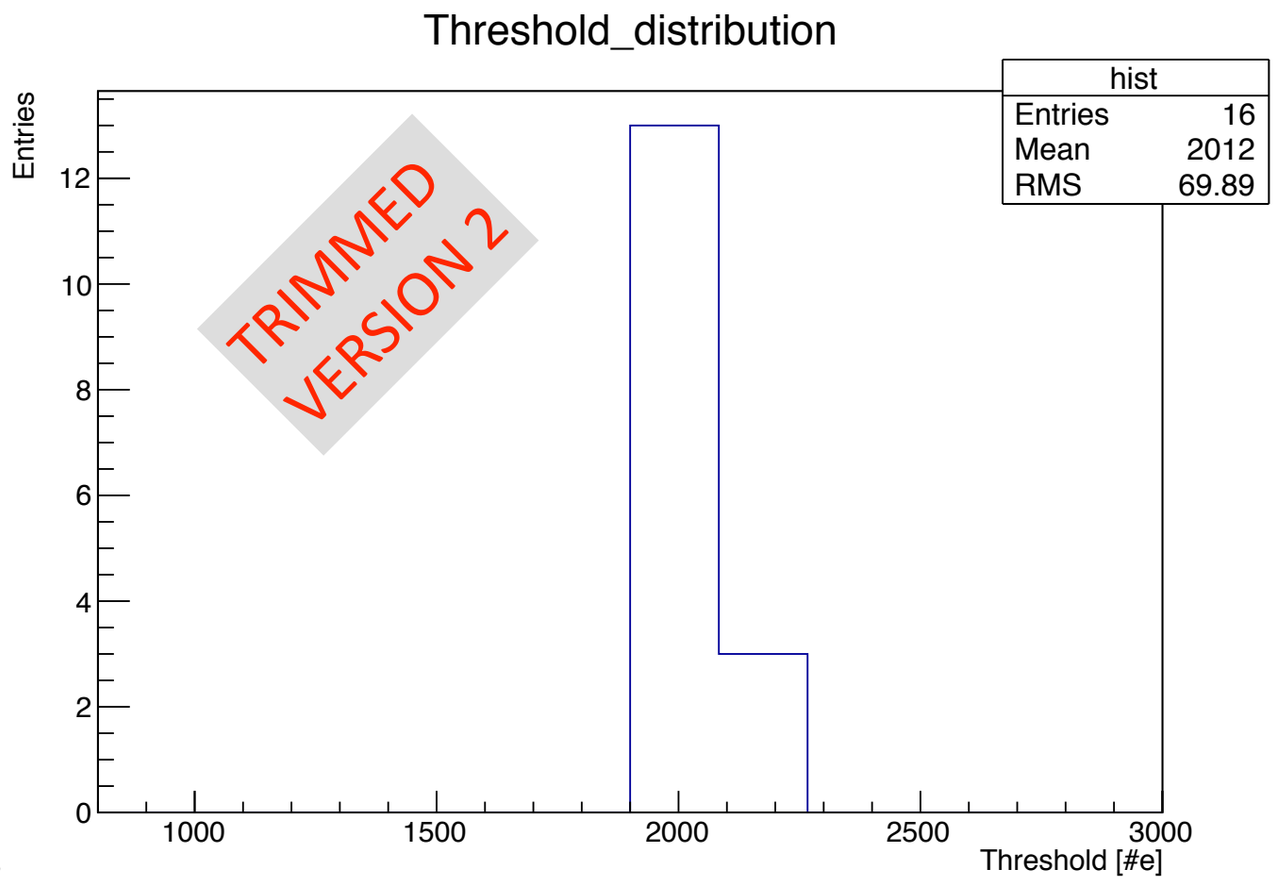
☺ We have understood the problems

- Too high gain fluctuations due to mismatch
- Underestimation of the latch dynamic offset

⇨ Solved in version 2

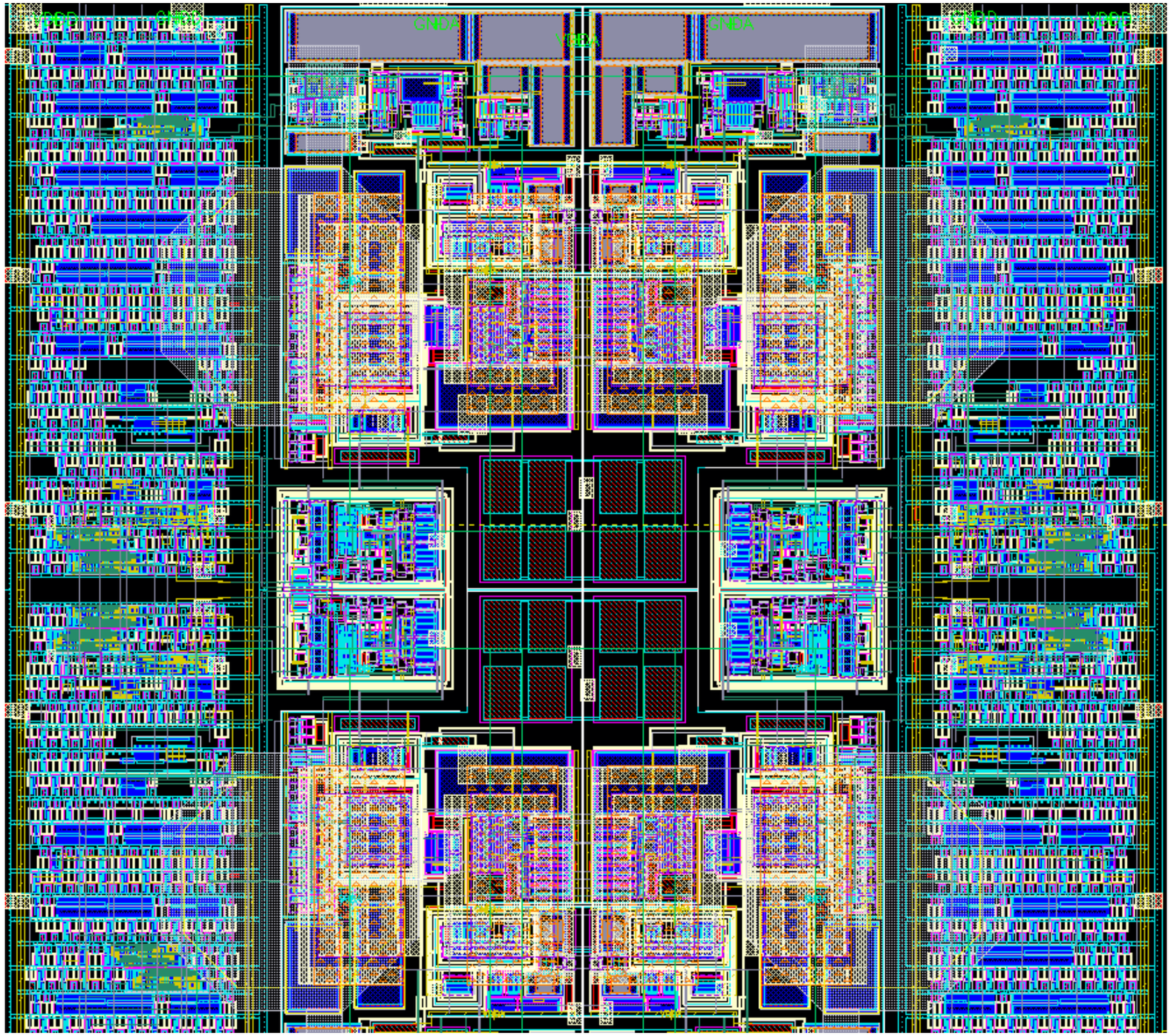
Offset compensation - Measurement results





- Significant improvement wrt the first version
  - The threshold RMS decreases from 174 e- to 70 e-

VFE_2 layout - 2x2 pixel region



List of Conferences

- RADFAC 2015, INFN Legnaro, 26/03/2015 (talk)
- TWEPP 2015 - Topical Workshop on Electronics for Particle Physics - Lisbon 28/09-2/10/2015 (poster)
- SIF 2015 - 101° Congresso Nazionale della SIF (talk)
- PIXEL 2016 - 8th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging (poster)
- TWEPP 2016 - Topical Workshop on Electronics for Particle Physics - Karlsruhe 26-30/09/2016 (talk)

List of Publications

- Authorship within the CMS Collaboration since May 2015

- N.Demaria, E. Monteil et al. “RD53 Collaboration and CHIPIX65 Project for the development of an innovative Pixel Front End Chip for HL-LHC”, PoS IFD 2014, 010 (2015).

- N.Demaria, E.Monteil - “CHIPIX65: Developments on a new generation pixel readout ASIC in CMOS 65 nm for HEP experiments” - Published in:Advances in Sensors and Interfaces (IWASI), 2015 6th IEEE International Workshop on Advances in Sensors and Interfaces

- L.Pacher, E.Monteil et al., “A Low-Power Low-Noise Synchronous Pixel Front-End Chain in 65 nm CMOS Technology with Local Fast ToT Encoding and Autozeroing for Extreme Rate and Radiation at HL-LHC” - IEEE

- E. Monteil, N. Demaria, L. Pacher, A. Rivetti, M. Da Rocha Rolo, F. Rotondo, C. Leng, “Pixel front-end with synchronous discriminator and fast charge measurement for the upgrades of HL-LHC experiments”, TWEPP 2015 - Journal of Instrumentation

- E. Monteil et al.,“A Prototype of a New Generation Readout ASIC in 65nm CMOS for Pixel Detectors at HL-LHC”, PIXEL 2016 - Journal of Instrumentation

- E. Monteil, N. Demaria, L. Pacher, A. Paterno’, A. Rivetti, M. Da Rocha Rolo, F. Rotondo, C. Leng, J.Chai, “A synchronous analog very front-end in 65 nm CMOS with local fast ToT encoding for pixel detectors at HL-LHC”, TWEPP 2016 - Journal of Instrumentation