# Design of integrated front chip in $0.35\mu m$ CMOS for cellular signal recording systems based on diamond arrays

**Candidato Sara Garbolino**
**Relatore Prof. Diego Gamba**
**Co-Relatore Dott. Angelo Rivetti**

Tesi di Laurea Magistrale in
Fisica delle Tecnologie Avanzate


FacoltÃ  di Scienze Matematiche Fisiche Naturali
UniversitÃ  degli studi di Torino
July, 2008

# Abstract

The target of this work is to study and design a layout for an Analog Front End for cellular electrical signal recording systems based on diamond microelectrodes. The diamond is the most recent material considered for microelectrode implementation. Its surface becomes conductive through the hydrogenation process. It is biocompatible and optically transparent and its noise level is lower than the conventional metal microelectrodes. For this reason it is important to minimize the noise introduced by the electronics employed in the signal processing.
The advent of the microelectrode array (MEA) makes it possible to have hundreds of recording channels. To avoid signal attenuation and minimize noise the preamplifier has to be close to the recording electrodes and if it occupies a small area the number of the channels could be increased.
To comply with noise and space requirements we choose to design an integrate circuit in CMOS AMS $0.35\mu m$ technology.
Main AFE requirements are very low noise, low power consumption, DC voltage rejection and a cut off frequency of some $kHz$.

The thesis is structured as follows:

1. **Introduction** It contains a brief description of neurons structure and their electrical activity, commonly used biosensors and experimental setup.

2. **Front End Architecture** The starting point [1] of the circuit is there described.

3. **Layout and packaging** This chapter deals with design rules and analog layout techniques.

4. **Preamplifier layout** and **Filter layout** A first layout has been designed starting from the architecture of Chapter 2. Problems related to the layout bahavior and solutions are exposed in this chapters, which contain also the study of more complex and more performant architectures.

5. **Complete chip layout** It describes the final submitted architecture layout and a summary of obtained results.

# Acknowledgements

# Contents

# List of Figures

# List of Tables

# Chapter 1

# Introduction

In order to characterize electrical signals from neurons, it is necessary to monitor their action potentials, which are variation of the transmembrane potential due to the flux of ions between cell's cytoplasm and external medium.
Results from this characterization find several applications in pharmaceutical screening, biochemical agents monitoring, drug detection, etc.

In this chapter the reader can find in the first part a short explanation of neurons electrical activity, followed by a description of cultured cell recording methods, focusing on diamond microelectrode array.
The second part of the chapter contains a list of electronic requirements for this application and a description of the chosen Front End architecture.

## 1.1 Neurons and biosensors

### 1.1.1 Neuron's structure

Neurons are cells capable of processing and transmitting informations through electrical pulses.
They are distinguished by their function in the nervous system and by the way they transmit signals. However the main structure is the same for all types (Fig. 1.1).

Neuron's main components are:

**soma** the cell body where most protein synthesis occurs. It ranges from $4\mu m$ to $25\mu m$;

**dendrites** branching fibers extending from the cell body, specialized in receiving incoming signals;

**axon** which has the function of transmitting action potentials to the dendrites of another neuron;

**axon terminal** placed at the end of the axon, its task is to electrically and chemically communicate with target neurons.

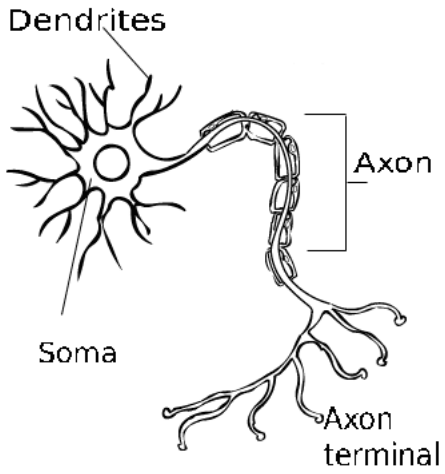



Figure 1.1: Neuron main structure

### 1.1.2 Neuron's electrical activity

#### Cellular membrane

Neural electrical activity is due to the flux of ions through a semipermeable bilayer membrane that covers the neuron itself.
The cellular membrane is composed by a double layer of molecules with fatty hydrophobic tails and charged hydrophilic heads. Layers are disposed as shown in Fig. 1.2.

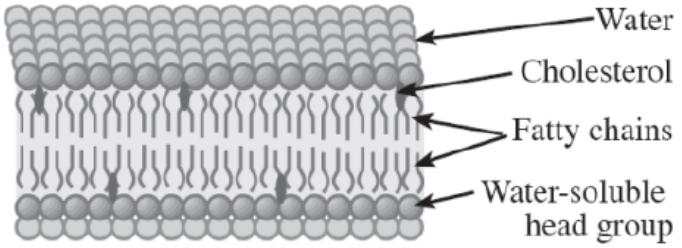



Figure 1.2: Double layer cellular membrane structure [2]

Fatty chains ($\sim 7nm$ thick) have the role of electrically insulating the external medium from the cytoplasm preventing ions, charged and uncharged molecules from passively diffusing from one region to the other and allowing the cell to control this flux through transmembrane proteins placed on the membrane. There are proteins that pump ions against their electrochemical gradient and others that form a channel through which ions can move along their electrochemical gradient.

#### Resting potential

With resting potential is meant the electrical field that rise between intracellular and extracellular surfaces because of the ions movements in equilibrium state. At

resting potential there are relatively more $Na^+$ ions outside of the neuron and more $K^+$ ions inside of it. The major contribution to the resting potential is given by $K^+$ ions and it assumes the typical value of $-70mV$ (negative charge inside the cell relative to the outside).

### Action potential

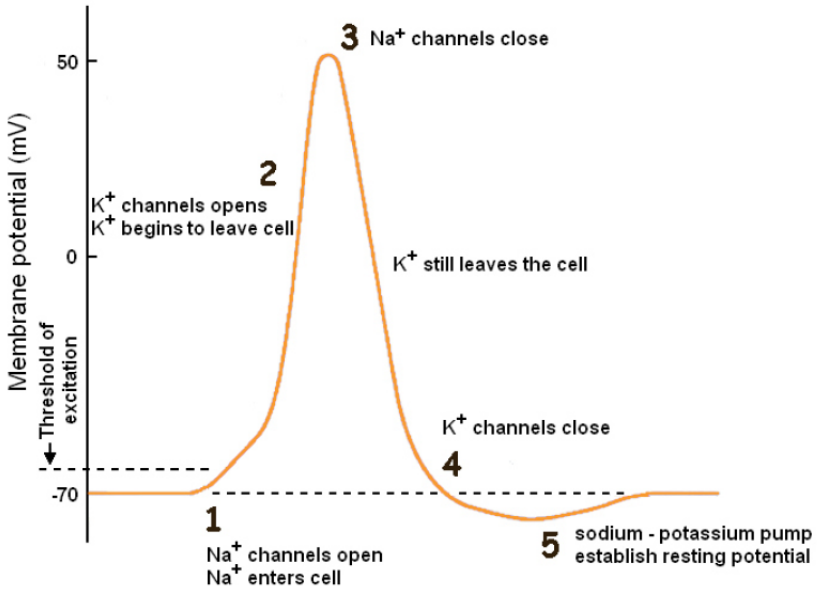



Figure 1.3: Action potential progress

Action potential carries out in five steps (Fig. 1.3).

**Stimulation** If transmembrane potential reaches about $-50mV$, sodium channels are opened for a short period allowing the flux of $Na^+$ ions into the cell and causing the membrane potential to become positive.

**Depolarization ("Rising phase")** At some positive membrane potential the $K^+$ channels are opened too, therefore $K^+$ ions can flow outside of the neuron.

**Peak** When $+50mV$ potential is reached $Na^+$ channels close stopping the inflow of positive charges.

**Repolarization ("Falling phase")** Since $K^+$ channels are still open, the membrane potential begin to decrease.

**Undershoot** When the resting potential is reached, $K^+$ channels close. Equilibrium ion transport starts again and the cell is ready for the next action potential.

The entire membrane doesn't depolarize at once, depolarization starts in one area and spreads by diffusion to contiguous regions. The process of depolarization and repolarization takes about $0.5ms$-$1.5ms$.

### 1.1.3 Recording methods

Testing on cultured cells, that means *in vitro*, rather than on *in vivo* cells is more suitable in order to study their behavior and activity. In this section some cultured cell recording method will be exposed.

#### Patch clamping

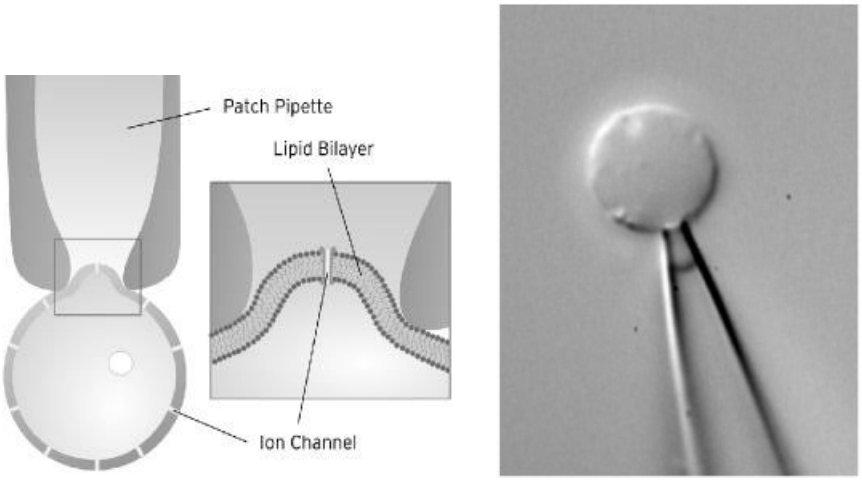



Figure 1.4: Patch clamping

This is an invasive method that consist on patching the tip of a glass electrolyte-filled pipette of about $1\mu m$ diameter to the membrane of a cell, calmping it to a preset voltage and measuring the resulting current (Fig. 1.4).
The advantage is the possibility to record directly action potentials of about $100mV$ wide and to study individual ion channels. As a drawback, it has a mechanically fragile connection which makes long term recording difficult.

#### Microelectrode

This is a non-invasive solution which estimates the transmembrane potential variation measuring the ion concentration change in extracellular medium surrounding the cell.
Two electrodes $10\mu m$ large are placed, the first near the cellular membrane and the second far from it, as a reference electrode.
Advantages are given by the possibility of monitoring and stimulating the electrochemical activity of several cells independently and simultaneously for a long time, but signals recorded are on the order of $100\mu V$ against $100mV$ of patch clamping.
It's simple to implement a microelectrode array (MEA), That is an arrangement of several electrodes (typically 60 placed at a distance of some hundreds micrometers). This solution allows recording and stimulation of more sites in parallel, moreover the sample can be placed directly on the recording area.
Typical detection distances are lower than $100\mu m$.
The impedance of a flat, round titanium nitride electrode ranges from $30\Omega$ and

$400k\Omega$. The smaller the electrode diameter and interelectrode distance, the higher the spacial resolution. However, small electrode results in higher noise: the average noise level of $30\mu m$ microelectrode is lower than $10\mu V$, while for a $15\mu m$ diameter microelectrode it's lower than $15\mu V$.

### Diamond microelectrode

A new material for microelecrode arrays, still in testing phase, is given by diamond. Diamond has a bandgap of about $5.5eV$ and is considered an insulator, but, with its surface hydrogenated, it becomes conductive. Hydrogenating diamond, dangling bonds on the surface are saturated by hydrogen atoms creating hole accumulation layers in the bandgap that act as acceptors (Fig. 1.5).

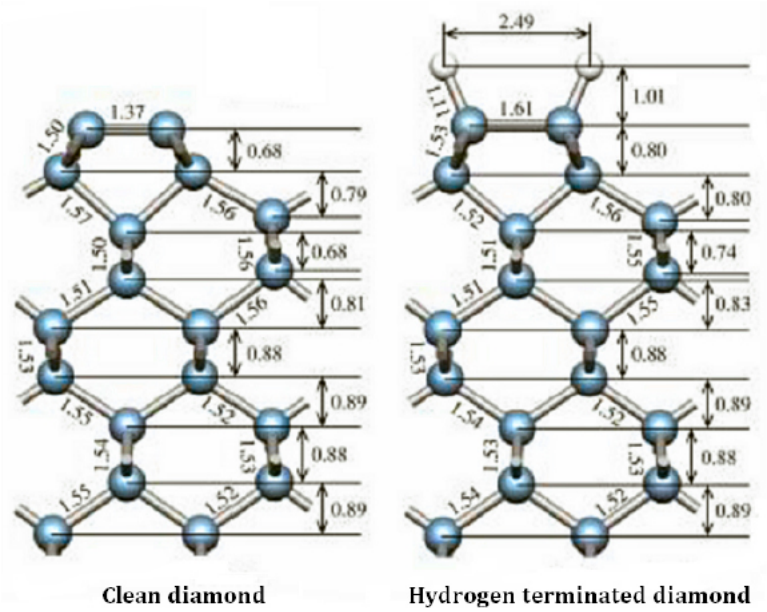



Figure 1.5: pure and hydrogenated diamond (001) surfaces

Moreover, when exposed to atmosphere, a thin water layer forms on the surface acting as an acceptor surface for the diamond exchanging electrons with hydrogen terminations.
The result is an areal hole density of $\rho_{surface} \approx 10^{13} cm^{-2}$ and a superficial sheet resistance of $R_{\square} \approx 10^4 \Omega/\square$ at room temperature.

Diamond is preferred to conventional electrode materials because of some favorable properties.
First of all it is biocompatible, having an inert surface that assure a long term stability with weak adsorption of polar molecules.
Furthermore, having a transmittance grater than 50% in the visible wavelength region upon $500nm$, it can be considered optically transparent. This property allows first to position the cell on the microelectrodes through a microscope, and second to record optical signals of cells by using fluorescent dyes.

Besides it gives the possibility of modulating its surface characteristics, such as resistivity, with oxygen or hydrogen terminations.

### Experimental setup

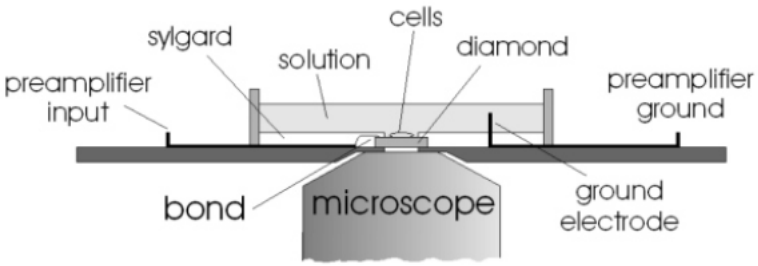



Figure 1.6: Diamond macroelectrode experimental setup

For the testing measurements a diamond microelectrode of $3mm^2$ was used. The borders of the macroelectrodes are fixed to a high resistivity printed circuit board. A microscope positioned under the macroelectrode allows to see the cells immersed in the electrolyte medium and directly coupled with the macroelectrode. In order to insulate the electrolyte from conductors, bond wires and interconnections a sylgard passivation layer is used. The preamplifier input signal is taken through a gold wire of $20\mu m$ diameter connected to diamond with a silver paste, while ground electrode is connected to a silver chloride reference electrode immersed in the cultured media.
It is possible to measure the diamond electrode noise level, and it is expected being lower than the one of metallic electrodes ($\leq 5\mu V$). To amplify the signal without increasing the noise floor and to prevent from amplification of the relatively small extracellular signals, a low noise, high input impedance preamplifier is required.

Extracellular signals are $10^3$ times smaller than transmembrane potentials. Signal amplitude and wave shape depends on many factors, such as the diameter of the neuron, the proximity of the electrode to the neuron, the angle between the electrode surface and the neuron, the portion of the neuron to which the electrode is closest. There are small regions of close adhesion ($< 15nm$) between membrane and electrode, while other regions are more loosely coupled and separation reaches $100nm$. Thanks to low pass filtering properties of the extracellular medium, the more the neuron-electrode distance increases, the more the extracellular signal amplitude decreases; than, neurons placed beyond $140nm$ from the electrode are indistinguishable from noise. In this regard, high spatial resolution of the electrode and close interface between electrode and cell are very important to obtain a good signal-to-noise ratio.

## 1.2 AFE basic requirements

AFE basic requirements are imposed by the characteristics of the signal coming from the sensor:

- Amplitude: $150\mu V$
- Frequency domain: $10Hz$-$3kHz$
- Biological noise: $10\mu Vrms$
- DC component: $\pm 50mV$

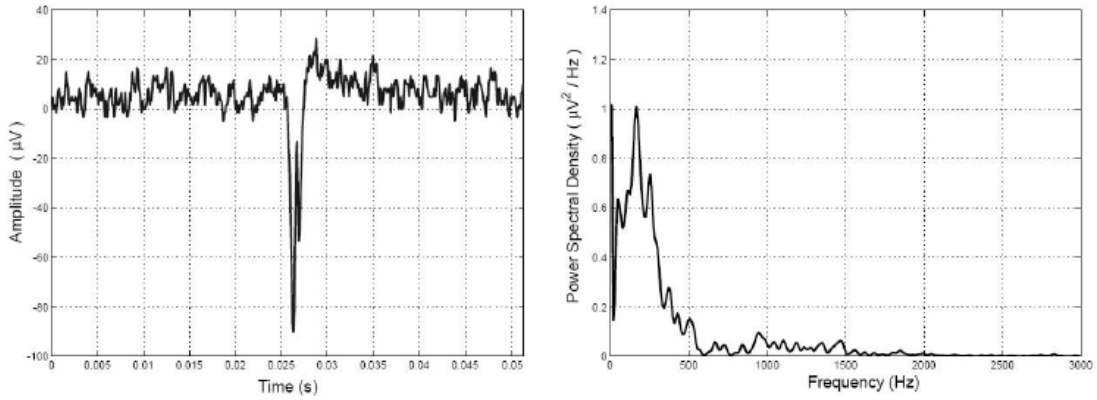



Figure 1.7: Time and frequency domain analysis of neuron spontaneous electrophysiological activity [3]

First important feature of the preamplifier is the frequency band. It has to cut the DC component without cutting the signal. A typical band is between $f_L \approx 10Hz$ and $f_H \approx 10kHz$.
Moreover the differential input must have a high input resistance in order to have a negligible voltage drop on the microelectrode ($R_{electrode} \leq 400K\Omega$). Low power consumption is required too not to damage by heating biological tissues and to have many recording channels on the same chip in a small silicon area. Furthermore, most important features are low noise and high gain (to minimize following stages noise contribution) [1].

# Chapter 2

# Front End Architecture

This chapter deals with the description of the chosen Front End Architecture for neural signal recording coming from diamond MEA biosensors together with the reasons for this choice.
A block diagram of single channel is shown in fig. 2.1.

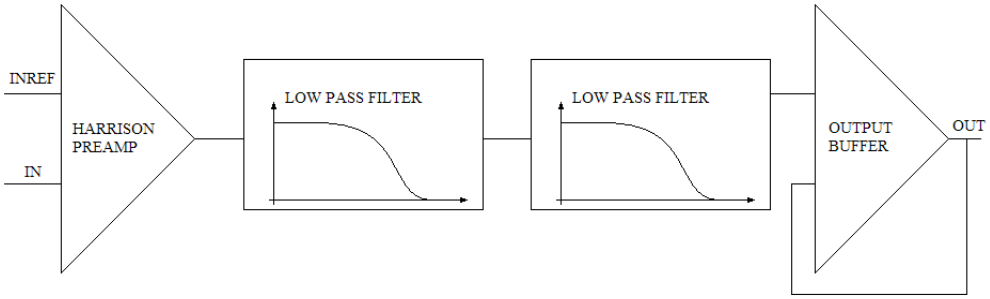



Figure 2.1: Block diagram of a single channel

## 2.1 Harrison preamplifier

As exposed above, mainly features of the preamplifier stage are low noise, low power consumption, high gain and offset rejection with a frequency band of $\sim 10Hz$-$10kHz$.

Low power consumption requirement derives from the necessity of fully implanting large quantities of them in a small area. Since power dissipation should not exceed a few hundreds $mW$, for a 1000-electrode system, this results in a maximum power dissipation much less than $1mW$ per amplifier.

With Harrison's feedback network [4] (Fig. 2.2), the preamplifier transfer function is:

$$A_{VM}(s) = \frac{A_{V0}^{OTA}(sC_1R)}{(A_{V0}^{OTA}+1)(sC_2R+1)+sC_1R}$$

where $A_{V0}^{OTA}$ is the OTA open loop gain.
If $A_{V0}^{OTA}$ is assumed infinite, the mid band gain tends to the ratio $C_1/C_2$. The amplifier has been designed for a gain of 100, setting $C_1$ to $20pF$ and $C_2$ to $200fF$. Both $C_1$ and $C_2$ were designed as poly-poly capacitors for maximum linearity.

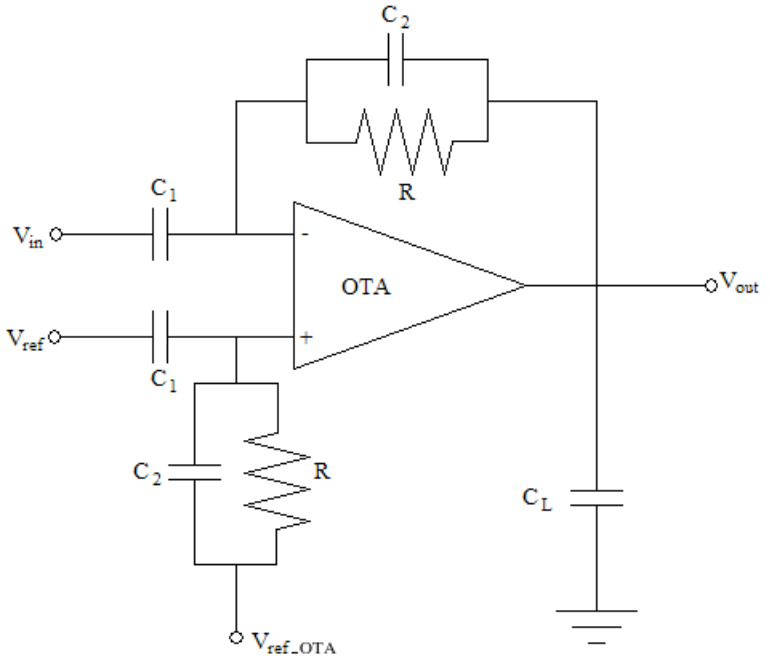



Figure 2.2: Schematic of Harrison's bandpass preamplifier

The low cutoff frequency $f_L$ is given by $1/(2\pi RC_2)$, while the high one is $f_H = g_m^{OTA}/(2\pi A_V C_L)$. To set $f_L \approx 10Hz$, the product $RC_2$ must be $\approx 10^{-2}$. This means that, using a large resistor (than a MOS-bipolar pseudoresistor), capacitor can be small enough to occupy a not too large silicon area.

Moreover, in the case where $C_1$, $C_L \gg C_2$ the bandwidth is approximately $g_m/(A_{VM}C_L)$, where $g_m$ is the transconductance of the OTA and $C_L$ is $13pF$ compensation capacitor.

### 2.1.1 MOS-bipolar pseudoresistor

The peculiarity of this circuit consists in the use of a MOS-bipolar pseudoresistor element to amplify low frequency signals down to the $mHz$ range while rejecting DC offsets. With negative $V_{GS}$, each device functions as a diode-connected pMOS

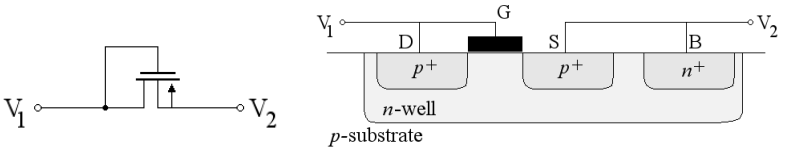



Figure 2.3: MOS-bipolar pseudoresistor

transistor, while with positive $V_{GS}$, the parasitic source-well-drain p-n-p bipolar junction transistor (BJT) is activated, and the device acts as a diode-connected BJT (Fig. 2.4).

For small voltages across this device, its incremental resistance $r_{inc}$ is extremely high: for $|V_{GS}| < 0.2V$, $\frac{dV}{dI} > 10^{11}\Omega$ has been measured. A large change in the input

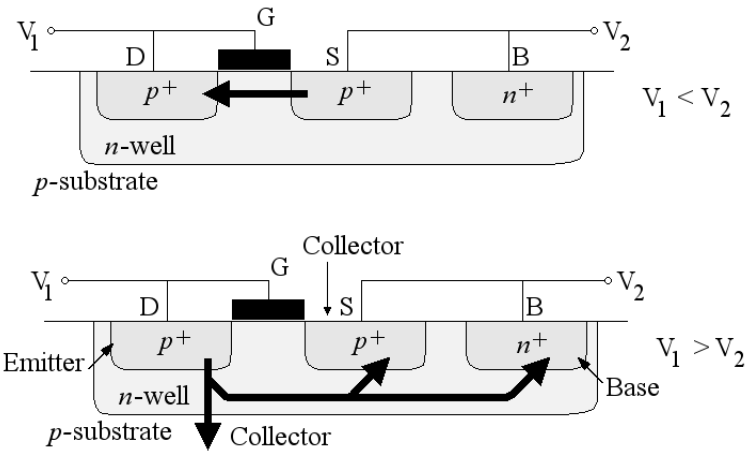



Figure 2.4: MOS-bipolar pseudoresistor working

causes a large voltage across the MOS-bipolar elements, reducing their incremental resistance and giving fast settling time.

Another design uses diode-connected nMOS transistors as pseudoresistors to achieve an equivalent resistance of grater than $10^{10}\Omega$, though it is not stated whether a body-source connection is used to create a diode-connected bipolar transistor.

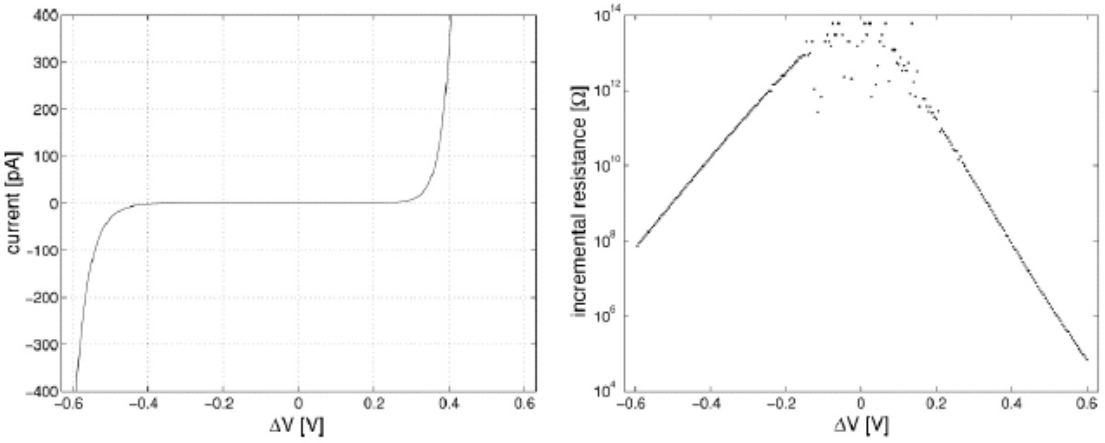



Figure 2.5: I-V relationship and incremental resistance of single MOS-bipolar element

Using two MOS-bipolar devices in series it is possible to reduce distortion for large output signals.

### 2.1.2 Low-noise, high gain and low-power OTA design

As told before, the ideal gain of preamplifier is:

$$A_{VM}^{ideal} = \lim_{A_{V0}^{OTA}\to+\infty} A_{VM} = \lim_{A_{V0}^{OTA}\to+\infty} \frac{A_{V0}^{OTA}(sC_1R)}{(A_{V0}^{OTA}+1)(sC_2R+1)+sC_1R} = \frac{C_1}{C_2} \quad (2.1)$$

Actually $A_{VM}$ differs from the ideal value $A_{VM}^{ideal}$ because of the finite value of $A_{V0}^{OTA}$. The error on the total gain is:

$$err(A_{VM}) = \frac{A_{VM}^{ideal} - A_{VM}}{A_{VM}^{ideal}} \tag{2.2}$$

In the bandwith of interest $R \approx 10^{12}\Omega$, than Equation 2.1 can be rewritten as:

$$A_{VM} \approx \frac{A_{V0}^{OTA} C_1}{(A_{V0}^{OTA} + 1)C_2 + C_1} \tag{2.3}$$

Than, using definition 2.2, the gain error results:

$$err(A_{VM}) \approx \frac{\frac{A_{V0}^{OTA} C_1}{(A_{V0}^{OTA}+1)C_2+C_1} - \frac{C_1}{C_2}}{\frac{C_1}{C_2}} = \frac{A_{V0}^{OTA} C_2}{(A_{V0}^{OTA} + 1)C_2 + C_1} - 1 \tag{2.4}$$

In table 2.1 errors for different values of $A_{VM}^{OTA}$ are reported (using $C_1 = 20pF$ and $C_2 = 200fF$).

| $A_{V0}^{OTA}[V/V]$ | $err(A_{VM})[\%]$ |
|---|---|
| $10^2$ | $-50$ |
| $10^3$ | $-9.1$ |
| $10^4$ | $-0.99$ |
| $10^5$ | $-0.10$ |

Table 2.1: Influence of $A_{VM}^{OTA}$ on the $A_{VM}$ precision

The typical extracellular neural background noise is of about 5-10 $\mu Vrms$ over the bandwidth, therefore, in order to avoid increasing the noise floor, the preamplifier *rms* noise must be at least a factor two smaller. It means that in the choice of OTA architecture the noise is the most critical parameter since a gain of $10^4$ is easily achieved by most CMOS OTA architectures [4].
As a solution, symmetrical OTA has been chosen (Fig 2.6) [5].

In Fig. 2.6 a pMOS input stage configuration is shown. In M10 flows current mirrored by M9. This current symmetrically splits in M1 and M2 and is mirrored by M3 and M4 respectively in M5 and M6. Finally the same current of M6 is mirrored in M8 by M7.

Equation 2.5 reports the total input referred noise:

$$V_{irn}^2 = 2V_{n1}^2 + \frac{2V_{n3}^2 + 2V_{n6}^2 + 2V_{n8}^2}{g_{m1}^2 r_{0,1}^2} \tag{2.5}$$

where transistors M1-M2, M3-M4, M5-M6 and M7-M8 are matched in pairs. The contribution given by thermal noise is:

$$V_{irn,th}^2 = [\frac{16k_bT}{3g_{m1}}(1 + 2\frac{g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}})]\Delta f \tag{2.6}$$

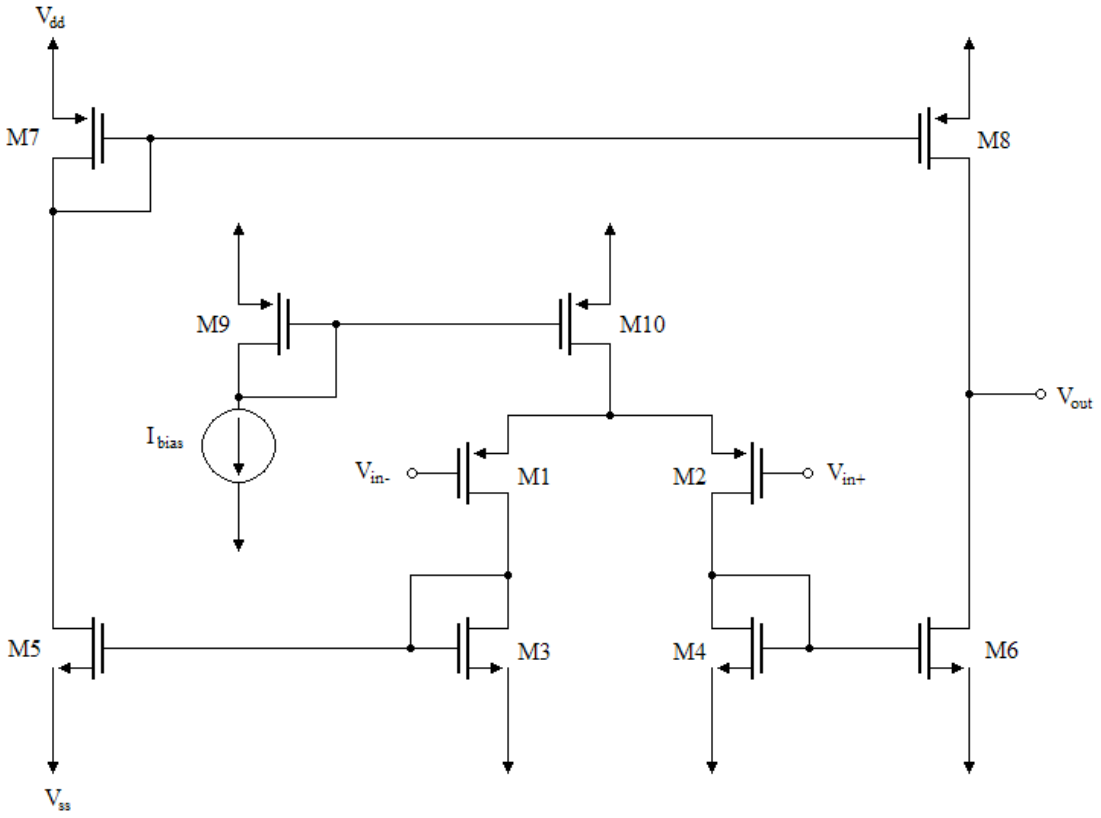



Figure 2.6: Schematic of OTA used in Harrison preamplifier

Sizing devices such that $g_{m3}$, $g_{m7} \ll g_{m1}$the noise contributions of devices M3-M8 can be minimized. This can be accomplished by making $(W/L)_3$, $(W/L)_7 \ll (W/L)_1$. Moreover, to minimize flicker noise, M1 and M2 are set with a high $(W/L)$ ratio.
Nevertheless, $g_{m3}$ and $g_{m7}$ cannot be arbitrarily decreased without danger of instability. If the total capacitance seen by the gate of M3 (or M4) is $C_3$, than the OTA has two poles at $\omega_p = g_{m3}/C_3$. Similarly there is a pole at $g_{m7}/C_7$ caused by the pMOS mirror. To ensure stability, these pole frequencies must be several times greater than the dominant pole $\omega_D = g_{m1}C_L$. As a trade off, $C_L$ cannot be too large, area limitations and bandwith requirements have to be considered.
On the other hand, the input referred noise of the bioamplifier can be related to the OTA input referred noise by:

$$V^2_{irn,amp} = (\frac{C_1 + C_2 + C_{in}}{C_1})V^2_{irn} \tag{2.7}$$

where $C_{in}$ is the OTA input capacitance. Than, as M1 and M2 are made larger, $C_{in}$ increases and consequently the noise becomes higher.

In table 2.2 are reported the values which were chosen after some simulations.

The OTA open loop gain is given by the product of the OTA transconductance $(g_m^{OTA})$ with the output resistance $(R_{out})$:

$$g_m^{OTA} = \frac{g_{m1}}{g_{m3}} g_{m6} \tag{2.8}$$

| MOS | W/L |
|---|---|
| M1, M2 | $1000\mu m/2\mu m$ |
| M3, M4 | $2\mu m/20\mu m$ |
| M5, M6 | $2\mu m/20\mu m$ |
| M7, M8 | $6\mu m/20\mu m$ |
| M9, M10 | $20\mu m/20\mu m$ |

Table 2.2: OTA's MOS dimensions

$$R_{out} = \frac{1}{g_{ds6} + g_{ds8}} \tag{2.9}$$

$$A_v^{OTA} = g_m^{OTA} R_{out} \tag{2.10}$$

## 2.2 Filter stage

[1] Harrison preamplifier is followed by a two filter stage which amplifies the signal once again in the bandwidth of interest and increases the slope of the transfer function after the cut off frequency, producing a clearer cut of the signal components with a frequency greater than the one desired.

The input signal of the filter comes from the preamplifier. Since the maximum amplitude of peak-to-peak neural signal is nearly $V_{pp} = 150\mu V$and the preamplifier gain is $\approx 100$, the maximum peak-to-peak value of filter input signal results of about $15mV$. This means that the filter stage have to amplify without distortions signals smaller than $15mV$, this results in a large output swing requirement.
Moreover, the filter stage should exhibit a low pass behavior with a cut off frequency nearly of $10kHz$, with the possibility of externally tuning this value.

It has been decided to implement the filter stage as two single pole OP-AMP filters in non inverting configuration in cascade.
In Fig. 2.7 is shown the OP-AMP architecture chosen for the filter.

It is a two stage differential input single ended amplifier with Miller compensation.

### 2.2.1 First OP-AMP stage

The first stage is composed by a differential pair with NMOS input transistors (M1, M2) with degeneration resistance $R_s$, a cascoded current mirror load (M5, M6, M7, M8) and current source transistors (M3, M4) which mirror the $I_{bias}$ current.
The use of wide swing cascode increases the output resistance, also reducing the systematic mismatch between the currents that flow in the differential branches.
Cascode transistors are biased with $V_{cas}$, which has to satisfy the following conditions in order to keep M5 and M6 in saturation region:

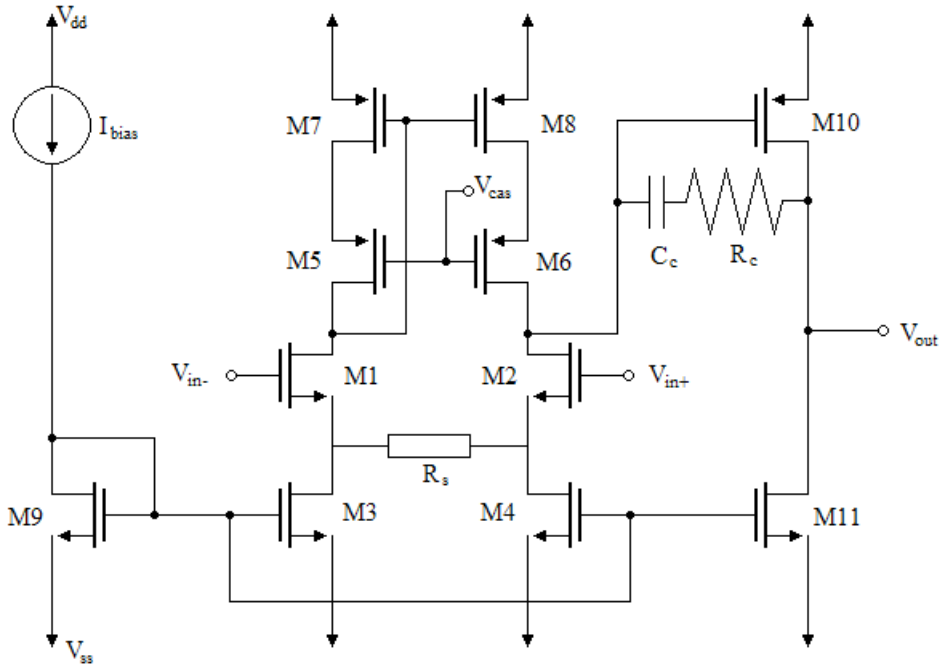



Figure 2.7: Schematic of filter OP-AMP

$$\begin{aligned} V_{dd} - V_{DS8sat} &> V_{cas} + V_{GS6} \\ V_{cas} + V_{GS6} - V_{DS6sat} &> V_{out1}^{DC} + S_{swing} \\ \Rightarrow V_{out1}^{DC} + S_{swing} - V_{GS6} + V_{DS6sat} &< V_{cas} < V_{dd} - V_{DS8sat} - V_{GS6} \end{aligned} \quad (2.11)$$

where $V_{out1}^{DC}$ and $S_{swing}$ are the DC voltage level and the signal swing at the output of the first stage.
After some simulations $V_{cas} = 2.0V$ was chosen.output buffer

The source degeneration resistance $R_s$ is composed by four NMOS transistors connected in series as shown in Fig. 2.8

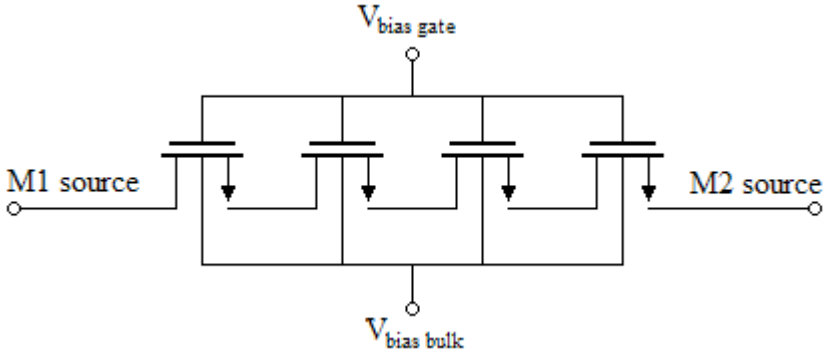



Figure 2.8: Source degeneration resistance scheme

All transistor gates are biased by $V_{biasgate}$, with their bulks connected to the negative supply.
The value of $R_s$ is given by the sum of the resistance of each transistor:

$$R_s = \sum_{transistor M_i} \frac{1}{g_{ds_i}} \approx 1M\Omega \tag{2.12}$$

By changing the value of $R_s$ it is possible to tune the cut off frequency of the filter stage. This could be desirable to serve different applications once the circuit has been fabricated. Decreasing the value of $V_{biasgate}$ the channel conductance $g_{ds}$ of the four transistors that compose the degeneration resistance is decreased, leading to higher values of $R_s$ and lower values of cut off frequency.

Load resistance value is given by the cascode equivalent resistance:

$$R_d = (g_{m6} + g_{mb6})r_{o8}r_{o6} + r_{o8} + r_{o6} \approx 500M\Omega \tag{2.13}$$

finally, first stage gain is:

$$A_{V1} = \frac{g_{m2}r_{o2}R_d}{R_d + \frac{R_s}{2} + r_{o2} + (g_{m2} + g_{mb2})\frac{R_s}{2}r_{o2}} \approx 500 \tag{2.14}$$

### 2.2.2 Second OP-AMP stage

The second stage is a PMOS (M10) common source with NMOS (M11) active load, which gain is given by:

$$A_{V2} = g_{m10}(r_{o10}//r_{o11}) = g_{m10}\frac{1}{g_{ds10} + g_{ds11}} \approx 500 \tag{2.15}$$

than total open loop gain results $\approx 2500$.

### 2.2.3 Miller compensation

Miller compensation has the role to increase the phase margin through $C_c = 5pF$ capacitance regulating the unity gain frequency:

$$G_{meq} = \frac{g_{m2}}{1 + (g_{m2} + g_{mb2})\frac{R_s}{2}} \tag{2.16}$$

$$f_{UG} = \frac{G_{meq}}{2\pi C_c} \tag{2.17}$$

Besides the $R_c$ compensation resistance regulates the transfer function zero:

$$z_1 = -\frac{1}{R_c C_c - C_c/g_{m10}} \tag{2.18}$$

To avoid instability issues, the zero must be pushed to $\infty$, than:

$$R_c = \frac{1}{g_{m10}} \tag{2.19}$$

### 2.2.4 Two filters in cascade

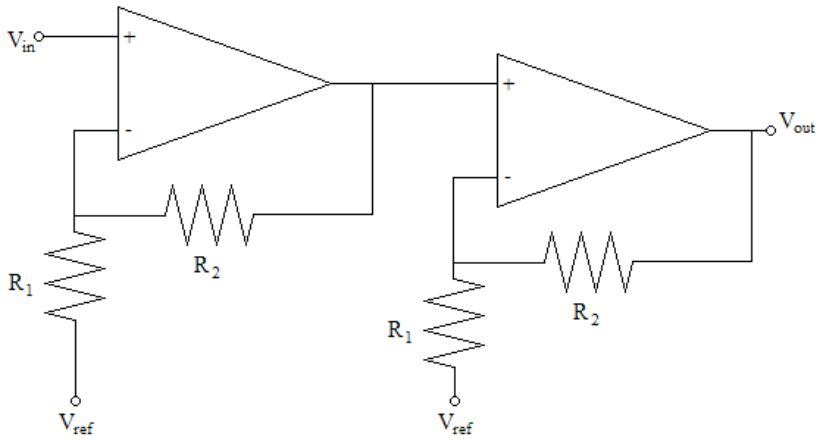



Figure 2.9: Schematic of filter stage

Each OP-AMP is used in non inverting condition and the closed loop gain is:

$$A_V^{closedloop} = \frac{A_V^{openloop}}{1 + A_V^{openloop} \frac{R_1}{R_1+R_2}} \tag{2.20}$$

$$\lim_{A_V^{openloop} \to \infty} A_V^{closedloop} = 1 + \frac{R_2}{R_1} \tag{2.21}$$

In order to haw a total gain of 25, each filter must have a gain of 5 and $R_2$ must be four time greater than $R_1$.
$R_1 = 100k\Omega$ and $R_2 = 400k\Omega$ have been chosen.

### 2.2.5 Channel-to-channel mismatch

To work correctly, the circuit has to balance the current in the branches of the differential pair creating an output offset:

$$G_{meq} = \frac{\delta I_{branch}}{\delta V_{out1}} \Rightarrow \Delta I_{branch} = \Delta V_{out1} G_{meq} \tag{2.22}$$

Mismatch between circuit components affects the circuit DC working point and the current symmetry in the branches. For example, a mismatch between mirror transistors leads to different mirrored current values in the different branches of the circuit, a mismatch in the input transistor is responsible for the broken symmetry if the differential pair, and a mismatch in the feedback resistors causes a variation of the OP-AMP closed loop gain.
In a multichannel recording system, there may be differences between the different channel DC output levels because of transistor mismatches, and, if the DC output level is too far from the reference value, the output linear range decreases.
To decrease the channel-to-channel difference mismatches have to be reduced. With this target following solutions have been adopted during OP-AMP design:

- increase the length of PMOS load transistors in order to increase the cascode resistance and consequently the gain of the first stage: with high gain value, the effects of mismatch are compensated with little variation of the output DC level.
- increasing the length of NMOS current source transistors to reduce the mismatch effects in the current mirrored in the two branches of differential pair
- increasing length of NMOS input transistors to reduce mismatch on $g_m$ values.
- splitting the transistors gates, making more accurate the transistors size in the chip fabrication process.

Increasing $G_{meq}$ means to reduce the output offset. Nevertheless, to hold steady the unity gain frequency, the compensation capacitance has to be increased. This involves the use of a larger silicon area.
To avoid this, a $5pF$ capacitance and an offset compensation system have been used.

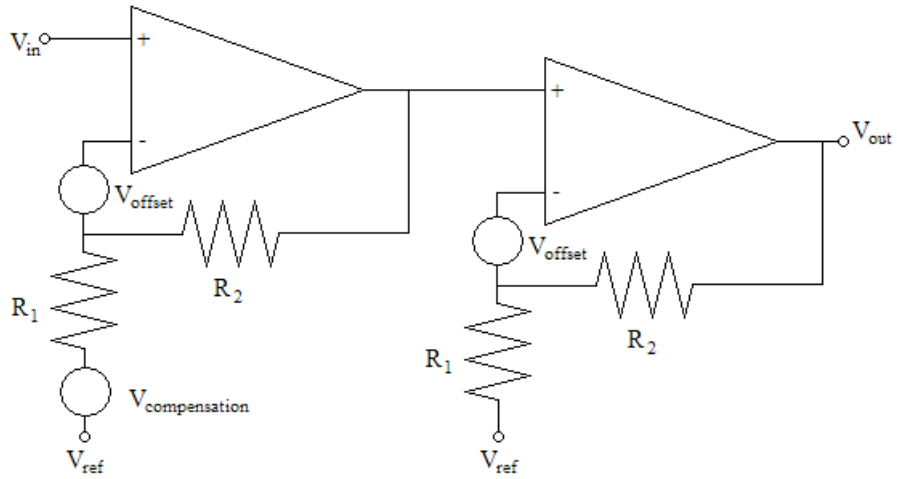



Figure 2.10: Filter stage offset compensation system

In Fig 2.10 a scheme of a possible offset compensation system is shown. The DC voltages $V_{offset}$ represent the offset o the circuit, while $V_{compensation}$ is a DC reference voltage which could vary the DC output level of the filter stage changing the DC level of the negative input of the first OP-AMP.

## 2.3 Output buffer

[1] The role of the unity gain output buffer is to interface the AFE to the recording hardware.
After the filter stage the gain reached is $\approx 2500$, which is sufficiently high for our purpose, so the output buffer is not required to amplify further on.
The maximum input signal of the filter stage is $15mV$ large, this means that the maximum signal in input to the buffer reaches $15mV \cdot 25V/V = 375mV$. This

implies that the buffer linear output range must be at least of $375mV$.
Of course it is also required a cut off frequency higher than $10kHz$.

For the implementation of the output buffer a standard configuration in class AB with two stages and Miller compensation has been chosen (Fig 2.11).

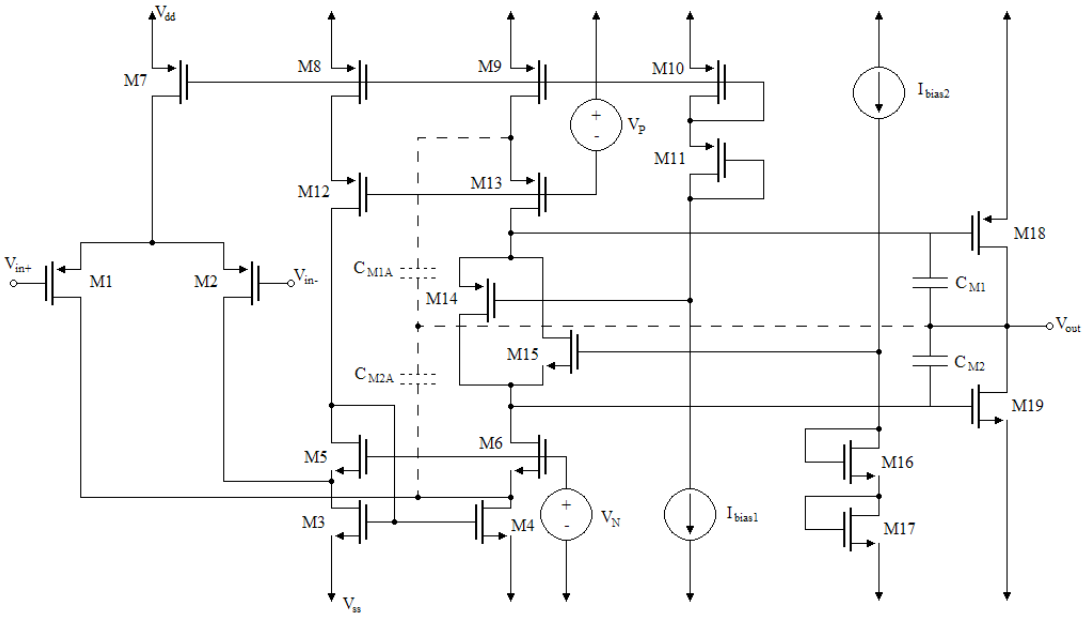



Figure 2.11: Schematic of output buffer OP-AMP

The output buffer is connected to the oscilloscope with a load resistance of $50\Omega$ and a load capacitance of $20pF$ (Fig 2.12).

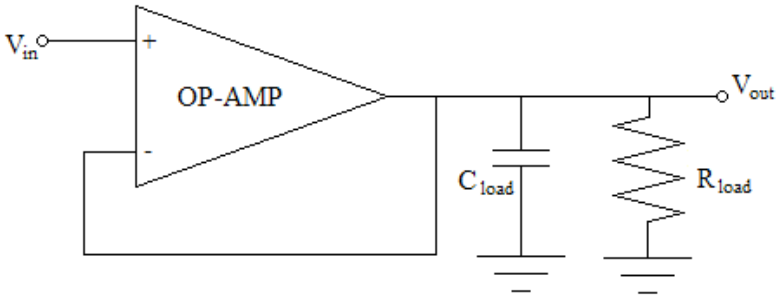



Figure 2.12: Output buffer scheme

If a supply voltage between $0V$ and $3.3V$ is used, the DC output level is $\approx 1.65V$, this means that a current of $33mA$ will flow in the load resistance. To avoid this large current flow at the output, there are two possible solutions:

- using a high load resistance of about $1M\Omega$ in order to have a current flow of few $\mu A$
- using a dual power supply with $\pm 1.65V$ in order to have a DC output level of $\approx V$

# Chapter 3

# Layout and packaging

[6] In the last 20 years analog CMOS circuits have evolved towards increasingly small dimensions. While device scaling has enhanced transistors speed, it has also led to unwanted interactions between different sections of integrated circuit as well as nonidealities in the layout and packaging, limiting speed and precision of such systems and influencing heavily their functioning.

## 3.1 Design rules

To prevent such troubles some design rules have been set concerning $n$-well and polysilicon geometries, $n^+$ and $p^-$ implants, interlayer contact windows and metal layers.

### 3.1.1 Minimum allowable rules

These are a set of rules which ensures the proper fabrication of devices despite tolerances in each step of processing.

#### Minimum width

This value is set both by lithography and processing capabilities of the technology. In general, the thicker a layer (the smaller technology), the greater its minimum allowable width.

#### Minimum spacing

To prevent geometries built on the same or on different masks to be shorted, they have to be separated by a minimum space.

#### Minimum enclosure

Each active area, such as $n$-wells and $p^+$ implants, must be surrounded by a proper implant geometry with enough margin to guarantee that the device is contained by these geometries despite tolerances.

#### Minimum extension

Some geometries must extend beyond the edge of others by a minimum value. This is the case of the gate polysilicon beyond the active area to ensure proper transistor action at the edge.

### 3.1.2 Maximum allowable rules

Some maximum allowable rules have been dictated too, e.g. a major metal width for longest wires to prevent *litoff* problems or rules related to the *antenna effect* described in next section.

#### Antenna effect

The antenna effect is an effect that can potentially cause reliability problems during the manufacture of MOS integrated circuits. Since the gate dielectric is so thin, only a few molecules thick, a big worry is breakdown of the this layer. This can happen if the net somehow acquires a voltage higher than the normal operating voltage of the chip. During the construction of the chip, the oxide may not be protected by any diffusion.
Suppose the gate of a small MOSFET is tied to a *metal 1* interconnect having a large area (Fig 3.1(a)).

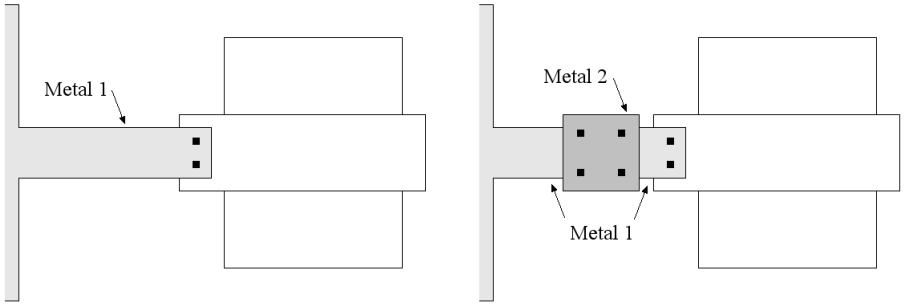



Figure 3.1: (a) Layout susceptible to antenna effect. (b) Discontinuity in *metal 1* layer to avoid antenna effect

During the etching of *metal 1*, the metal acts as an "antenna" collecting ions and rising potential. It is than possible than gate voltage of the MOS device increases so much that the gate oxide breaks down irreversibly during fabrication.

The antenna effect may occur for any large piece of conductive material tied to the gate of a transistor including polysilicon itself. For that reason such geometry areas are limited by design rules. Antenna rules are normally expressed as an allowable ratio of metal area to gate area. If large areas can't be avoided, than a discontinuity is created (Fig. 3.1(b)) so that when *metal 1* is being etched the large area is not connected to the gate.

## 3.2 Analog layout techniques

While design rules aim to guarantee the functioning of devices in IC, these techniques are meant to minimize effects such as crosstalks, mismatches, noise, etc.

### 3.2.1 Multifinger transistors

While for wide transistor a folded structure, as shown in Fig. 3.2(a), can be used in order to minimize both the source/drain junction area and the gate resistance, for very wide devices such a solution may prove inadequate. That's the reason for using a multiple fingers structure (Fig. 3.2(b)).
Moreover, in low noise applications, the gate resistance must be one-fifth or one-tenth of $1/g_m$.

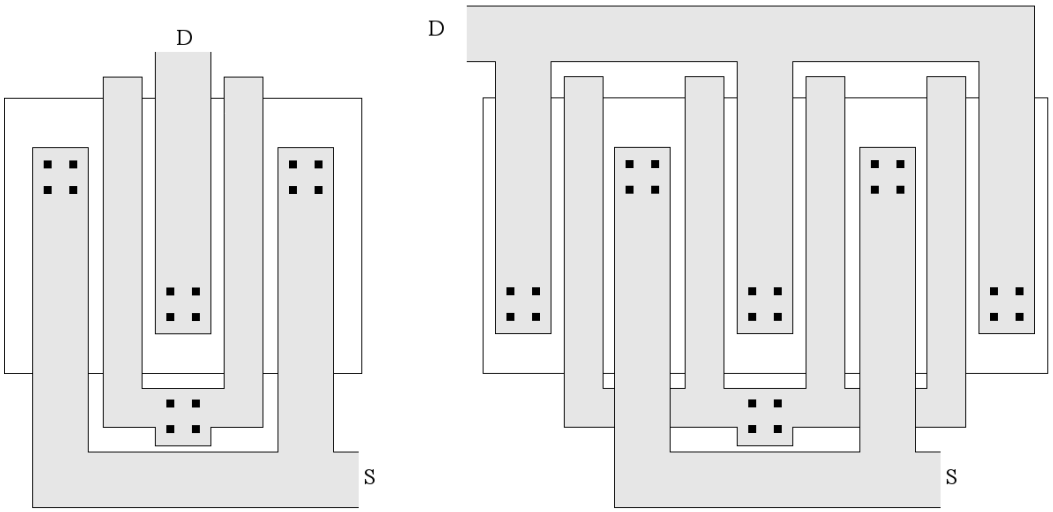


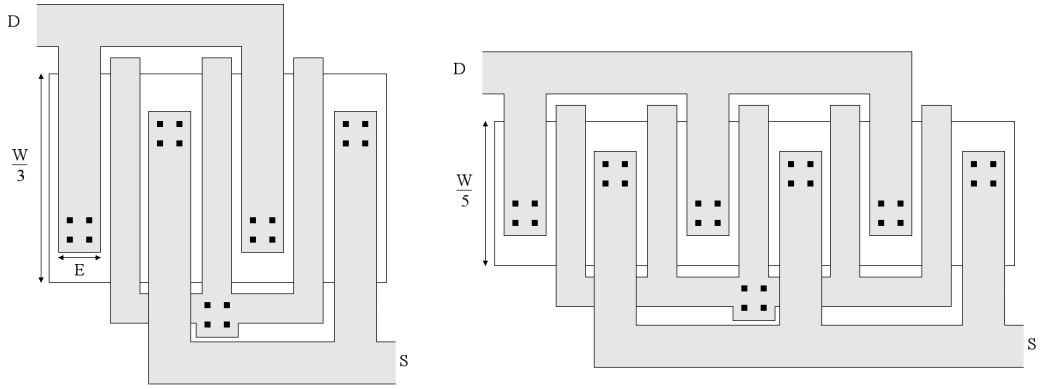

Figure 3.2: (a) Simple folded transistor. (b) Multifinger structure of a MOSFET

Decomposing the transistor into more parallel fingers takes to the trade-off between reducing the gate resistance (i.e. minimizing the gate resistance noise) and increasing the capacitance associated with the perimeter of source/drain areas (i.e. degrading the circuit high-frequency performance).
An example is shown in Fig. 3.3.

With three fingers the total perimeter of source/drain area is equal to $2(2E + 2W/3) = 4E + 4W/3$, whereas in five fingers structure it is given by $3(2E + 2W/5) = 6E + 6W/5$. In general, for an unspecific number of fingers $N$, the source/drain perimeter capacitance is:

$$C_P = \frac{N+1}{2}(2E + \frac{2W}{N})C_u = [(N+1)E + \frac{N+1}{N}W]C_u \tag{3.1}$$

Where $C_u$ is the capacitance per perimeter unit.
Therefore the number of fingers multiplied by $E$ must by much less than $W$ as to minimize the source/drain perimeter capacitance contribution.




(a) (b)

Figure 3.3: Layout of a transistor using (a) three fingers, (b) five fingers

A compromise may be reached by contacting the gate on both ends to reduce its resistance without increasing the number of fingers.

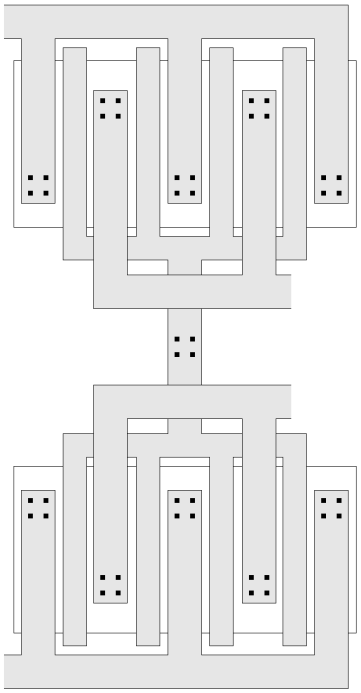


Figure 3.4: Layout of a transistor with many fingers

For transistors having a large number of fingers, the structure may modified as shown in Fig. 3.4 avoiding long uncomfortable geometries in the layout of overall circuit.

### 3.2.2 Symmetry

Symmetry is a very important item especially in the design of differential circuits, in which asymmetries introduce input referred offsets limiting the minimum signal

level that can be detected. A symmetric layout also yields to the suppression of common-mode noise and even-order nonlinearity.

For example, in the design of a pair (Fig. 3.5(a)) disparate solutions may be adopted. If the two transistors are laid out with different orientations as in Fig 3.5(b), the matching greatly suffers because of the variable behavior along different axes of many steps in lithography and wafer processing. Thus some more adequate solutions are provided by geometries in Fig. 3.5(c) and (d)

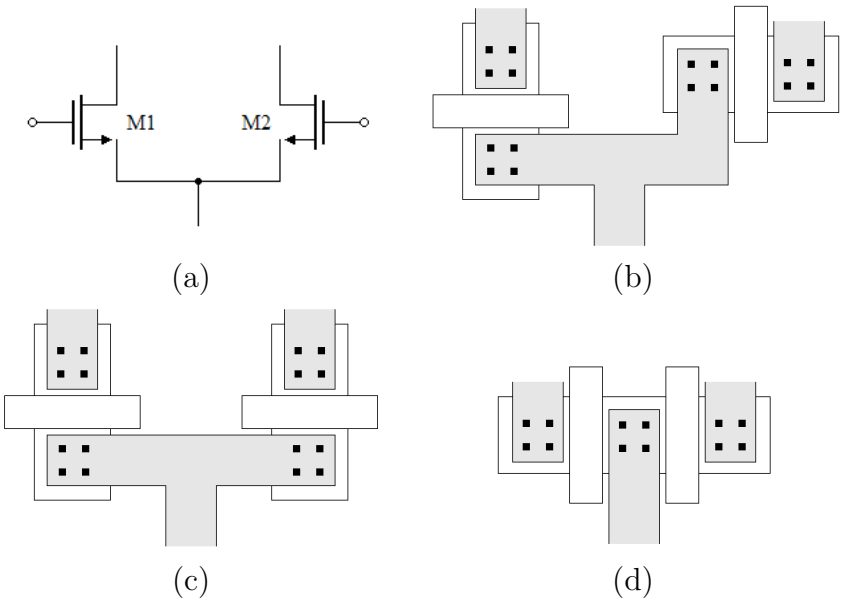



Figure 3.5: (a) Differential pair. (b) An example of an asymmetric layout and (c), (d) two symmetric layouts of the differential pair

Another issue that must be taken into account is the gate shadowing effect. Since during source/drain implantation the wafer is tilted by about 7° to avoid channeling, the gate polysilicon shadows a narrow strip in the source or drain region which receives less implantation than the other, creating a small asymmetry between source and drain side diffusions (Fig. 3.6).

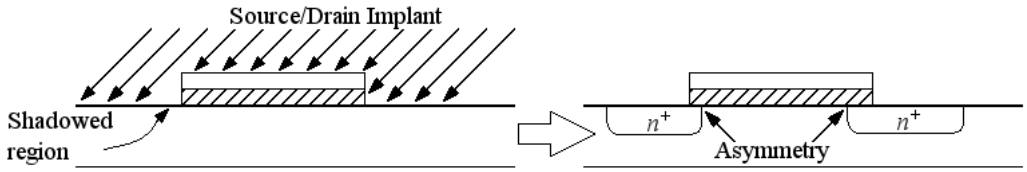



Figure 3.6: Gate shadowing effect

In order to reduce effects due to this kind of asymmetries, dummy structures are used (Fig. 3.7). They reproduce the same environment around the working devices.

Furthermore, if the geometry to be laid out requires a large area occupation (that's the case of large transistors composing a differential pair), appreciable mismatches due to gradients along the axes may arise. To reduce the error, a "common-centroid" configuration is used limiting the first order effects of gradients along both

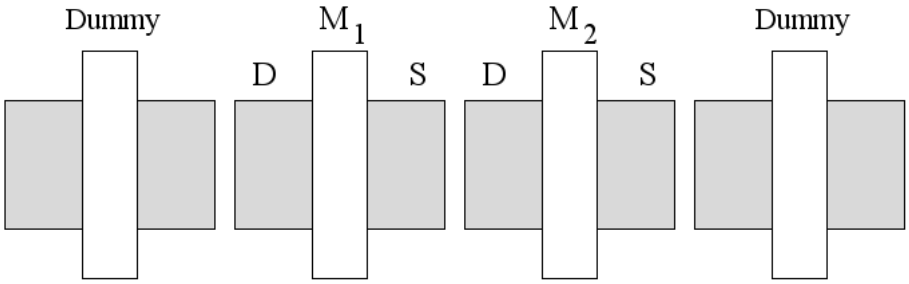
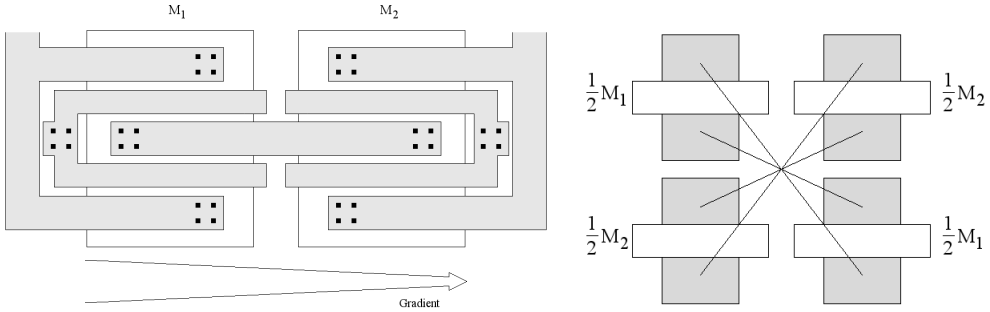



Figure 3.7: Addition of dummy devices to improve symmetry

axes (Fig. 3.8). However, the routing of interconnects in this kind of layouts is quite difficult, often leading to systematic asymmetries and to the introduction of parasitic capacitances between wires and from wires to ground.




(a) (b)

Figure 3.8: (a) Effect of gradient on a differential pair. (b) Common centroid layout

Another solution to this issue which is not affected by routing difficulties is provided by the one-dimensional cross coupling. Let's consider Fig. 3.9 and let us assume that, for example, the gate oxide capacitance varies by $\Delta C_{ox}$ from each half transistor to the next. In the first configuration it results:

$$\begin{aligned} I_{DS1a} + I_{DS4a} &= \frac{1}{2}\mu_n(C_{ox} + C_{ox} + 3\Delta C_{ox})\frac{W}{L}(V_{GS} - V_{th})^2 \\ I_{DS2a} + I_{DS3a} &= \frac{1}{2}\mu_n(C_{ox} + \Delta C_{ox} + C_{ox} + 2\Delta C_{ox})\frac{W}{L}(V_{GS} - V_{th})^2 \end{aligned} \tag{3.2}$$

This configuration than cancels the effect of the gradient, while the same does not happens in the second configuration, where:

$$\begin{aligned} I_{DS1b} + I_{DS3b} &= \frac{1}{2}\mu_n(C_{ox} + C_{ox} + 2\Delta C_{ox})\frac{W}{L}(V_{GS} - V_{th})^2 \\ I_{DS2b} + I_{DS4a} &= \frac{1}{2}\mu_n(C_{ox} + \Delta C_{ox} + C_{ox} + 3\Delta C_{ox})\frac{W}{L}(V_{GS} - V_{th})^2 \end{aligned} \tag{3.3}$$

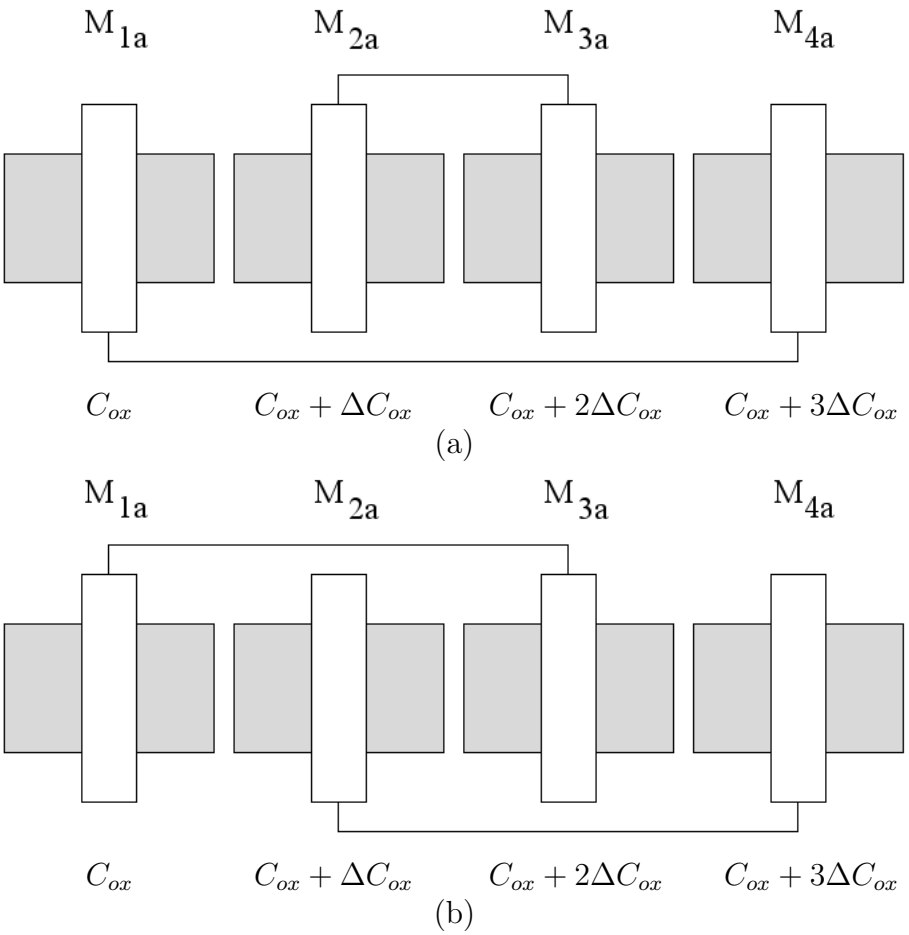



Figure 3.9: One-dimensional cross coupling

### 3.2.3 Reference distribution

In analog systems, the distribution across the chip of bandgap reference generators which bias the various building blocks gives rise to a number of issues.
Consider for example Fig. 3.10(a) where current $I_{REF}$ is mirrored in current sources $M_1$-$M_n$ which bias the different building blocks. If the matching between $I_1$-$I_n$ is critical and if transistors $M_1$-$M_n$ are located far from $M_{REF}$, than the voltage drop along the ground line must be taken into account. to prevent such problems, the reference can be distributed in the current domain rather than in the voltage one, as shown in Fig. 3.10(b). the idea is to route the reference current in the neighborhood of he interested building block and to perform the mirroring locally.
This solution ameliorate the match between references, however further errors are introduced by the mismatch between $I_{REF1}$ and $I_{REF1}$ and between $M_{REF1}$ and $M_{REF1}$.

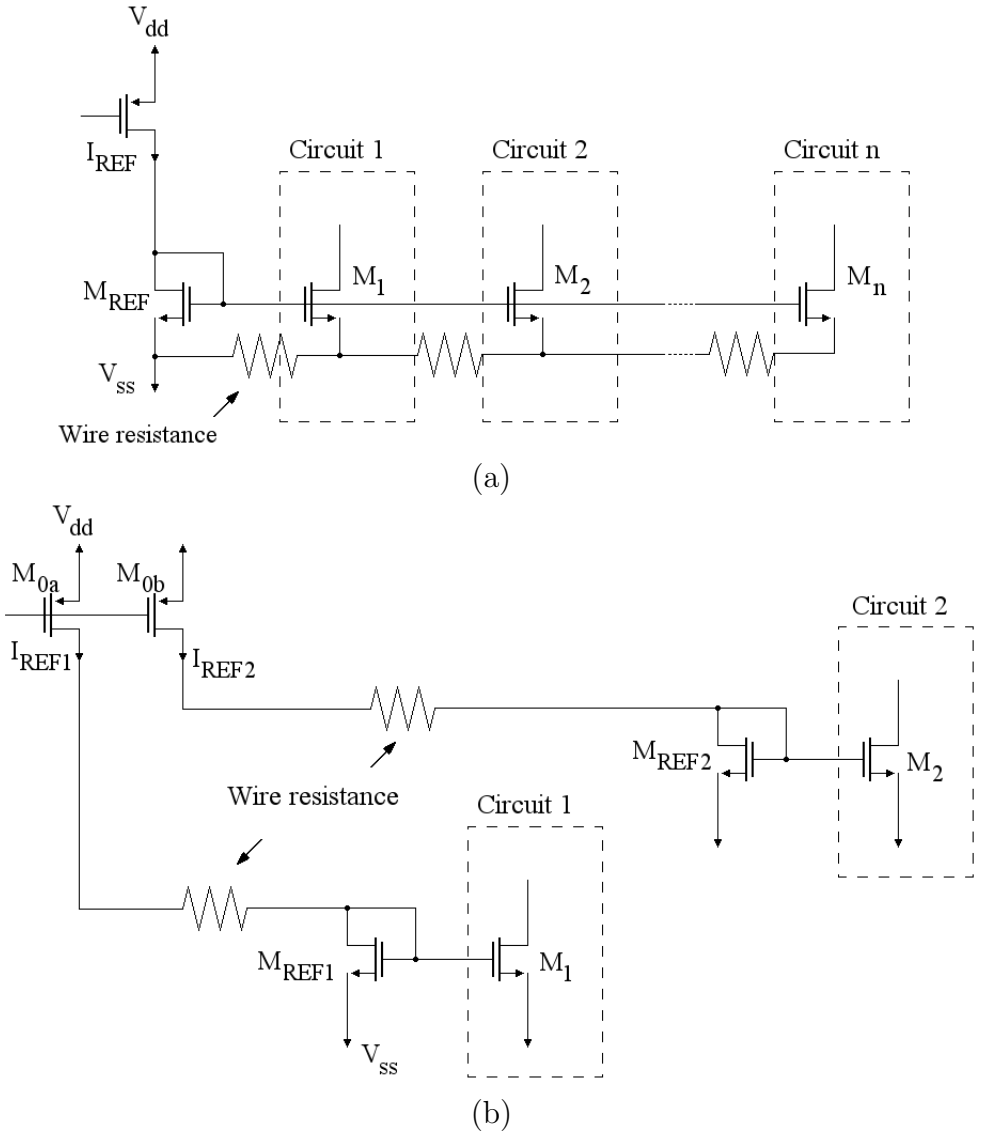



Figure 3.10: (a) Distribution of a reference voltage for current mirror biasing. (b) Distribution of current to reduce the effect of interconnect resistance

Finally, the scaling of currents demands careful choice of device dimensions and layout. Since the transistor channel length is a poorly controlled quantity, due to the side diffusion of source/drain regions, to ensure the maximum match, the length of transistor must be equaland the current must be scaled by proper choice of widths.

### 3.2.4 Passive devices

In this section problems related to the integration of resistors, capacitors and diodes are discussed. Main issues are area occupation, linearity, process variation, precision, etc.

#### Resistors

An important feature of integrated resistors is the sheet resistance $R_{\square}$, which depends on temperature, expressed by the temperature coefficient, and process.

Polysilicon resistors using a silicide block are characterized by high linearity and low capacitance to the substrate. Since their linearity depends on their dimensions, applying symmetry rules described for MOS devices layout, it is possible to obtain resistors which exhibit relatively small mismatches.

In order to improve the matching, large value resistors are usually laid out as the parallel of shorter units, which structure is preferable to the serpentine topology because of the absence of corners (Fig. 3.11).

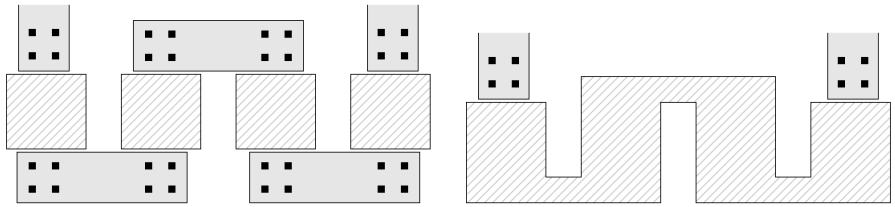



Figure 3.11: (a) Layout of large resistor. (b) Serpentine topology

The temperature coefficient varies with the doping type and level, typical values are $+0.1\%/°\text{C}$ and $-0.1\%/°\text{C}$ for $p^+$ and $n^+$ doping respectively. The sheet resistance variation with process is usually less than $\pm 20\%$.

In technologies lacking a silicide block mask, resistors may be implemented with $n$-well, source /drain $p^-$ $n^+$ material, silicided polysilicon or metal, with $R_{\square}$ decreasing in this order.

Typically, $n$-well resistors display a temperature coefficient of $+(0.2-0.5)\%/°\text{C}$, while their sheet resistance is of about $1k\Omega/\square$, but subject to large variations with process ($\approx \pm 40\%$). Moreover, since, with the depth of several microns, $n$-well regions exhibit width dependent diffusion at the edges, $R_{\square}$ also decreases with the width of the resistor. However the most serious problem is given by the dependence of $R_{\square}$ upon $n$-well-substrate voltage difference, which causes non-linearity andpoor definition of resistor value.

The $p^+$ and $n^+$ source/drain regions exhibit a sheet resistance of $3-5\Omega/\square$, thus they are suitable only for low value resistors. Despite they exhibit a higher linearity

with respect to $n$-well resistors, their variation with process may reach 50% and the junctions between these areas and the bulk introduces substantial capacitance and voltage dependence and their variation with process may reach 50%.

Silicided polysilicon has the same sheet resistance of $p^+$ and $n^+$ source/drain regions, but suffers from less capacitance to the substrate. These resistors are particularly suitable in applications in which the absolute value of $R_\square$ is not critical, since their variation with process is as high as 60% to 70%.
Its temperature coefficient varies between 0.2%/°C and 0.4%/°C.

Finally, a very low resistor value may be provided by a metal layer, which temperature coefficient for alluminium is 0.3%/°C. However, if the width of the metal resistor is small, the match suffers.

### Capacitors

High density linear capacitors are made using polysilicon over diffusion, polysilicon over polysilicon or polysilicon over metal, with a layer of oxide between the two plates. The first structure is largely used owing to its simplicity, while others exhibit higher linearity. If it is not possible to use such structures, available conductive layers are used (Fig. 3.12).

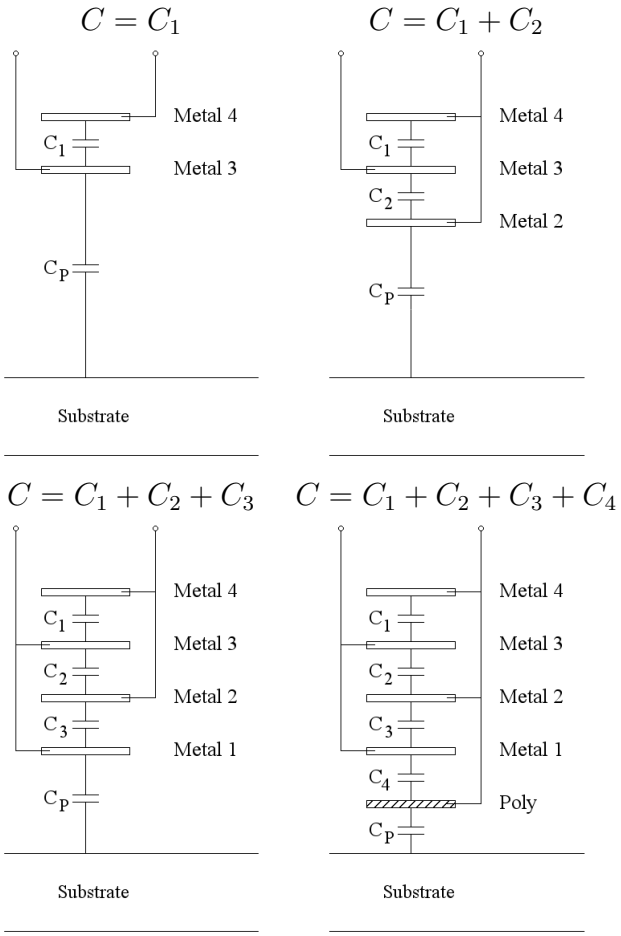



Figure 3.12: Capacitors made using allowable conductive layers

The choice of the topology is driven by area constraint and by the ratio of the bottom-plate parasitic capacitance to the inter-plate one, $C_P/C$. The capacitance of consecutive metal layers is of $35 - 40aF/\mu m^2$, while the one between *metal 1* and polysilicon is as high as $60aF/\mu m^2$, leading to a higher density. Nonetheless, the ratio $C_P/C$ increases from $0.2 - 0.25$ for the structure in Fig. 3.12(a) to 0.5 in Fig. 3.12(d). Moreover, since the interlayer capacitance value is poorly controlled, these topologies may experience process variations as high as 20%, while the gate oxide capacitance is controlled by less than 5% error.

Besides, a MOS transistor with source and drain tied together can be used as a capacitance as well if the gate-source potential is sufficiently high to establish an inversion layer, but this voltage dependence limits the linearity of this structure.

As for MOS and resistor devices, capacitors used in high precision applications have to be laid out following the rules described, such as using dummy structures, avoiding gradients, etc. However capacitors are quite more sensitive to wiring parasitic capacitance due to interconnections.

### Diodes

As shown in Fig. 3.13, two types of *p*-*n* junctions can be fabricated, in the *p*-substrate or in a *n*-well. The former must be used in reversed bias, than is useful only as a varactor (voltage-dependent capacitor).
The second has some problems too if forward biased because of a parasitic bipolar *pnp* transistor composed by the $p^+$ region, the *n*-well and the *p*-substrate. than this structure must not be viewed as a merely two-terminal floating diode.

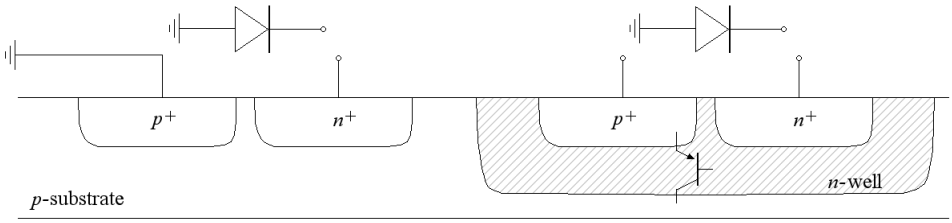



Figure 3.13: Diodes in CMOS technology

## 3.2.5 Interconnects

Modern CMOS technology offers five metal layers. This introduces a number of parasitic capacitors between the different levels of metal and fringe capacitance of wires, which may degrade the speed of the circuit. Furthermore, the capacitance between the wires produces unwanted coupling of signals. In order to reduce crosstalk, two solutions can be adopted. The use of differential signals, which convert the coupling into common-mode disturbance. Otherwise sensitive signals can be shielded placing ground lines on the two sides of the signal line as exemplified in Fig. 3.14(a), forcing most of electric field lines emanating form the noisy lines to terminate on ground rather than on the signal, at the cost of more complex wiring and greater

capacitance between the signal and ground. Note that this solutions proves more effective than just increasing the space between the different lines as in Fig. 3.14(b).

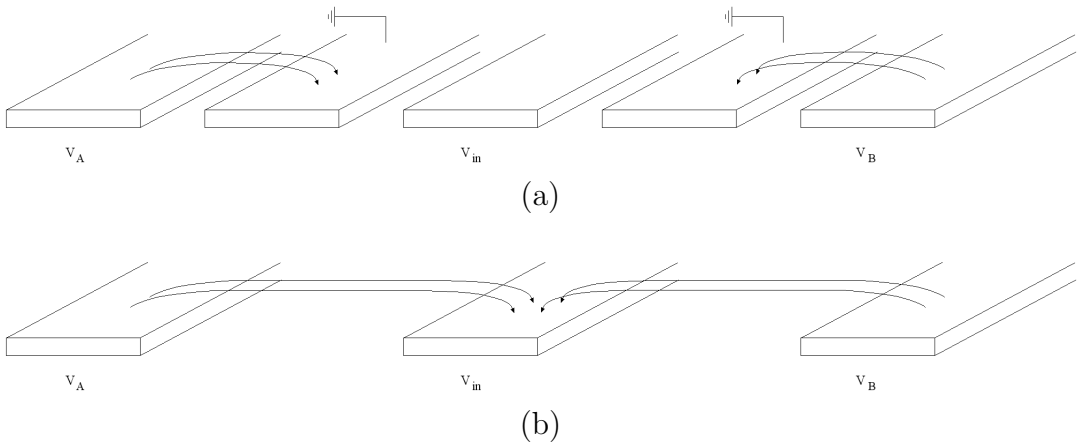



Figure 3.14: (a) Shielding sensitive signals by additional ground lines. (b) Allowing greater space between lines to reduce coupling

Another important issue is the resistance of interconnects. In low noise applications, thermal noise introduced by long interconnects may become remarkable. Moreover vias and contacts also suffer from high resistance.

The design of power and ground busses requires a particular attention too. In large chips, the voltage drop across the busses may become significant, affecting the functioning of different circuits supplied by them.Moreover, electromigration forces a minimum line width to ensure long term reliability. In order to reduce electromigration and busses resistance, it is possible to connect more metal layers in parallel.

### 3.2.6 Pads and ESD protection

Once the chip has been fabricated, it needs to be interfaced with the external environment. At this scope, bond wires are connected to large pads placed on the perimeter of the chip and connected to the corresponding nodes in the circuit. The pad dimensions and structure are dictated by the reliability issues and by tolerances in the bonding process.

The area of the pads must be minimized in order to reduce the parasitic capacitance of the pad to the substrate and to minimize the total dye area.

Since a pad made of simply a square of top metal may suffer of lit-off issues, a structure composed by two topmost metal layers connected to each other by many small vias on the perimeter is used. Of course, this structure suffers from a larger capacitance to the substrate.

The interface between the IC and the external world also entails the problem of electrostatic discharge (ESD). This effect occurs when an external object having a high potential touches the connections of the circuit. Since the capacitance seen at each input or output is quite small, the ESD produces a large voltage, possibly damaging the devices fabricated on the chip. As a result of the ESD, two possible

damages can affect MOS devices. First, the gate oxide may break down if the electric field exceeds roughly $10^7 V/cm$ (e.g. $10V$ for an oxide 100 $\overset{A}{\circ}$ thick). Second, the source/drain junction diodes may melt if a large current in forward or reverse bias flows.
To alleviate this risk, CMOS circuits incorporate EDS protection devices, like the one illustrated in Fig. 3.15. Such device clamps the external discharge to ground or $V_{dd}$ limiting the potential applied to the circuit. Resistor $R_1$ is necessary to avoid damage to $D_1$ and $D_2$ due to large currents that would otherwise flow from the external source.

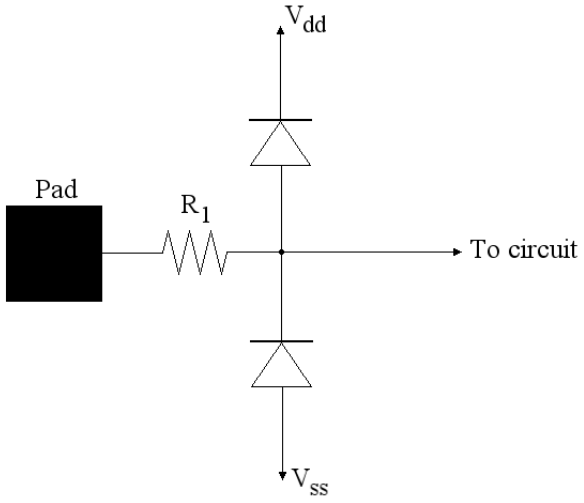



Figure 3.15: Simple EDS protection circuit

Obviously, the use of EDS protection circuits involves some problems.
The devices introduce substantial capacitance from the node to ground and $V_{dd}$, degrading the speed and the matching of impedances at the input and output ports of the circuit. Since the devices must be large enough so as the chip sustains a large EDS without damage, their capacitance may reach several picofarads. Moreover, $R_1$ introduces thermal noise which may become significant.
The capacitance introduced by ESD devices may couple noise on $V_{dd}$ and ground lines to the input of the circuit, corrupting the signal.
If not properly designed, ESD structures may lead to latch-up in CMOS circuits when electrostatic discharge occurs.

## 3.3 Substrate coupling

Most modern CMOS use a heavily-doped $p^+$ substrate to minimize latchup susceptibility. However, the low resistivity of the substrate created unwanted paths between various devices in the circuit, thereby corrupting sensitive signals. In order to reduce the effects of this phenomenon, called substrate coupling or substrate noise, the use of differential operation is suggested, making the circuit less sensitive to common-mode noise. Also, op amps using a PMOS differential input are preferred

because the well of the transistor can be tied to their common source, reducing the effect of substrate noise.

In circuits fabricated on lightly-doped substates, guard rings can be employed to isolate the sensitive sections. A guard ring may be simply a continuous ring made of substrate ties that surrounds the circuit, providing a low-impedance path to ground for the charge carriers produced in the substrate.

## 3.4 Packaging

Finally, integrated circuits are packaged. In simple dual-in-line package, the die is mounted in the center cavity and bonded to the pads on the perimeter of the cavity. These pads are the tip of each trace that ends in each package pin. Such a structure exhibits several parasitics, e.g. bond wire self-inductance, trace self-inductance, trace-to-ground capacitance, trace-to-trace mutual inductance and trace-to-trace capacitance.

While, owing to both circuit innovations and device scaling, the speed and accuracy of integrated circuits have steadily increased, the performance of packages, especially for low-cost applications, has not improved significantly. This limitation originates from the unscalable nature of packages and the environment in which they are used. As a result, packaging continue to limit the achievable performance of today's high-performance ICs.

# Chapter 4

# Preamplifier layout

Once the layout of the circuit was designed, a certain number of simulations were performed in order to ensure the right functioning.
Generally a first simulation of the layout in comparison with the result of the schematic simulation is performed. If both views give a consistent result, a second simulation is performed considering the parasitic capacitances of the extracted view. As a third step, worst cases and Montecarlo simulations are run.

## 4.1 Parasitic diodes

The first block to simulate is the Harrison preamplifier, which is also the most critical one.
A first simulation is shown in Fig. 4.1. It was performed biasing the circuit between $-1.65V$ and $1.65V$, than the output DC voltage is supposed to adjust at $0V$. However the result highlights the presence of a noteworthy output offset ($-155.458mV$), together with an instability in the transient analysis.

Looking at the extracted view, these effects seem to be due to the presence of parasitic *n*-well-*p*-substrate diodes in the feedback network MOS-bipolar pseudoresistors (Fig. 4.2).

In fact, introducing the parasitic diodes in the MOS-bipolar pseudoresistors and simulating the schematic, the result obtained is the same as the previous (Fig. 4.3).

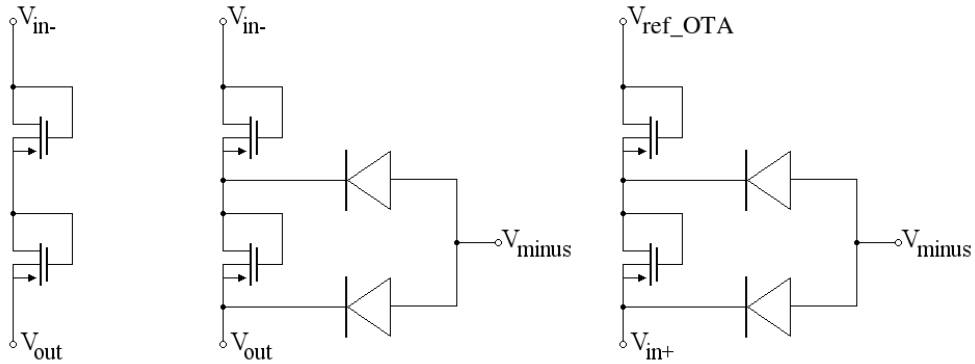
To study this phenomenon, the schematic was simulated with the parasite diodes first only on the feedback pseudoresistor and than only on the other.
The first simulation (Fig. 4.4(a)) gave a great positive output offset of $\approx 380mV$ and transient instability.

On the other hand, the second simulation (Fig. 4.4(b)) resulted in a negative output offset of $\approx -530mV$, without any instability effect. This means that the instability is due to the diodes on the feedback pseudoresistor. The total output offset agrees with the partial ones ($380mV - 530mV = -150mV$) and is the consequence of an asymmetry in the OTA's input transistors caused by the diodes.

As a test, we tried to turn the pseudoresistor at the positive input as it was in [4]. A negative output offset of $\approx -380mV$ was found, which cancels out the one found in the first simulation. Than in this configuration the problem of the offset is solved, probably thanks to a higher symmetry, since both OTA's inputs see the gate

Transient response

Figure 4.1: Harrison preamplifier layout transient simulation




(a) (b) (c)

Figure 4.2: (a) Ideal scheme of MOS-bipolar pseudoresistor. (b), (c) Presence of parasitic *n*-well diodes in the feedback network MOS-bipolar pseudoresistors

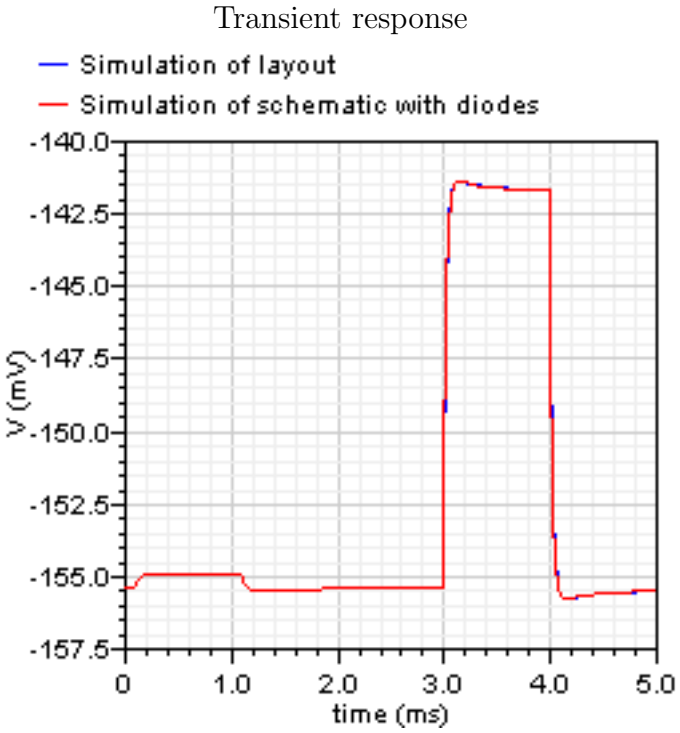
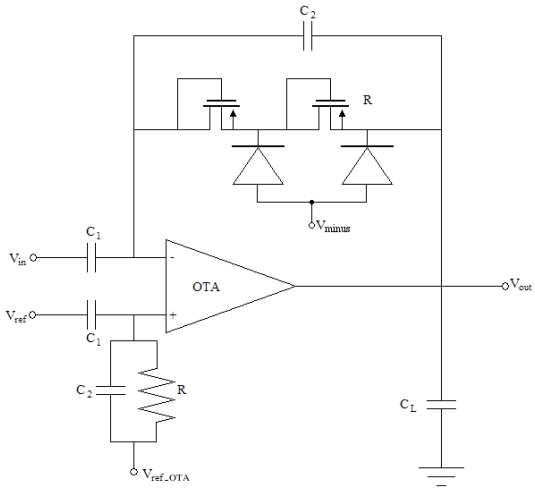
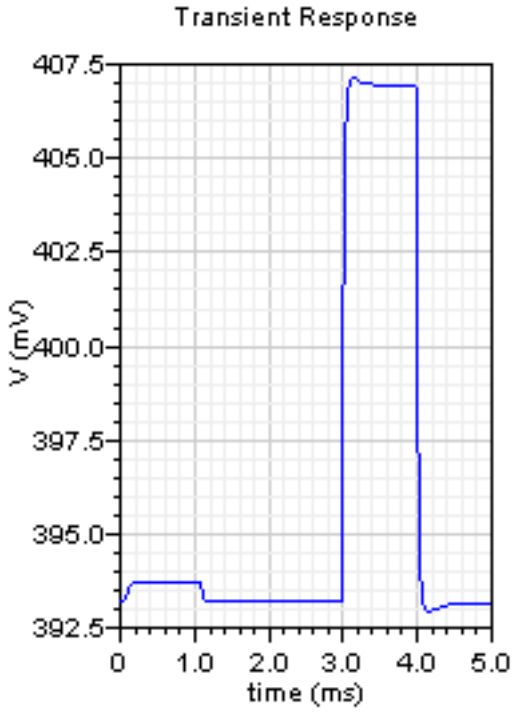


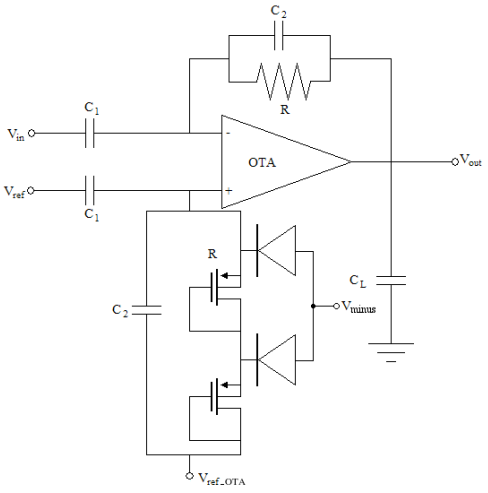

Figure 4.3: Introduction of parasitic diodes in the schematic transient simulation

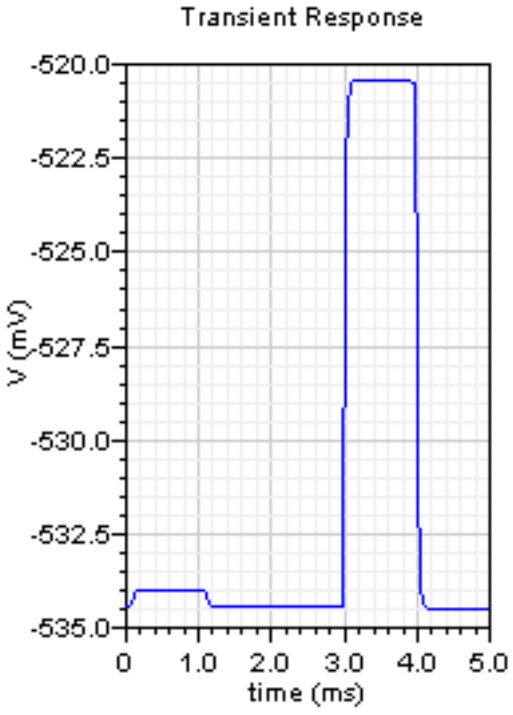
of the MOS-bipolar pseudoresistor, while in configuration 4.4(b) there's a current flowing through the diode in the positive input. This current throws off balance the inputs, than the OTA finds a new equilibrium introducing an output offset.




(a)




(b)

Figure 4.4: Simulation of schematic with parasitic diodes on the feedback pseudoresistor (a) and on the pseudoresistor at the positive input (b)

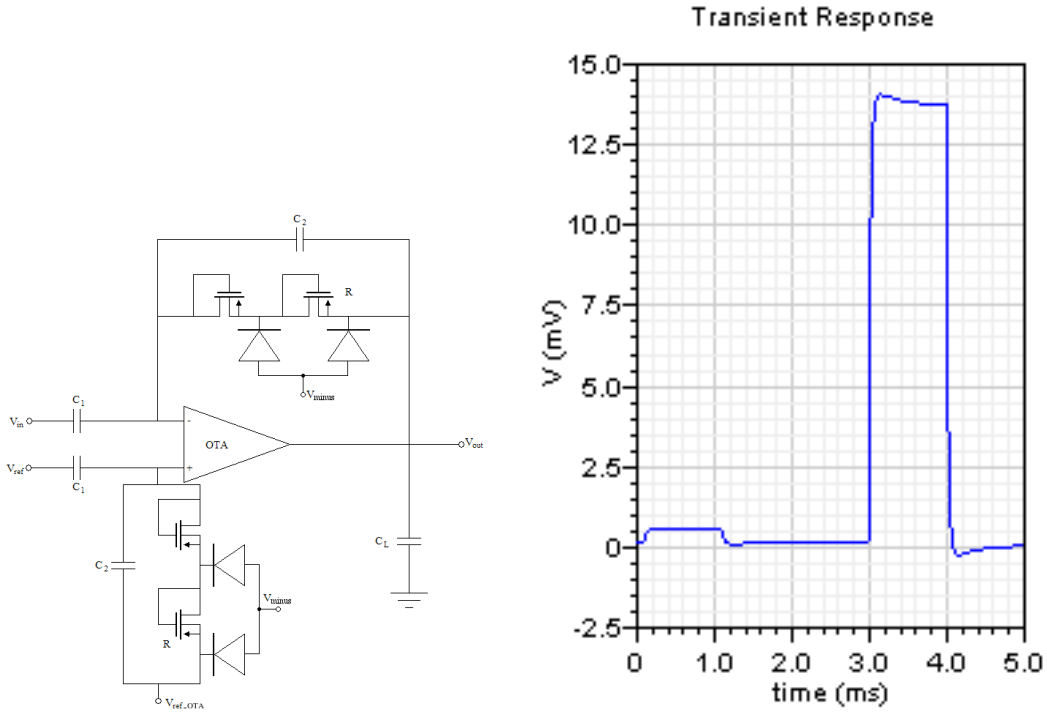



Figure 4.5: Simulation with reversed pseudoresistor

Reducing the output offset, also the stability improves. To understand why, let's consider the model of the feedback MOS-bipolar pseudoresistor depicted in Fig. 4.6:

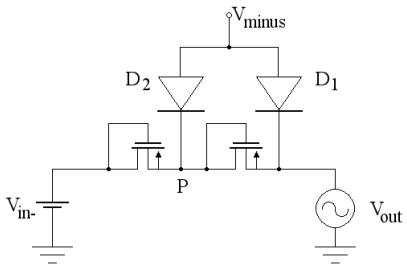



Figure 4.6: feedback MOS-bipolar pseudoresistor model

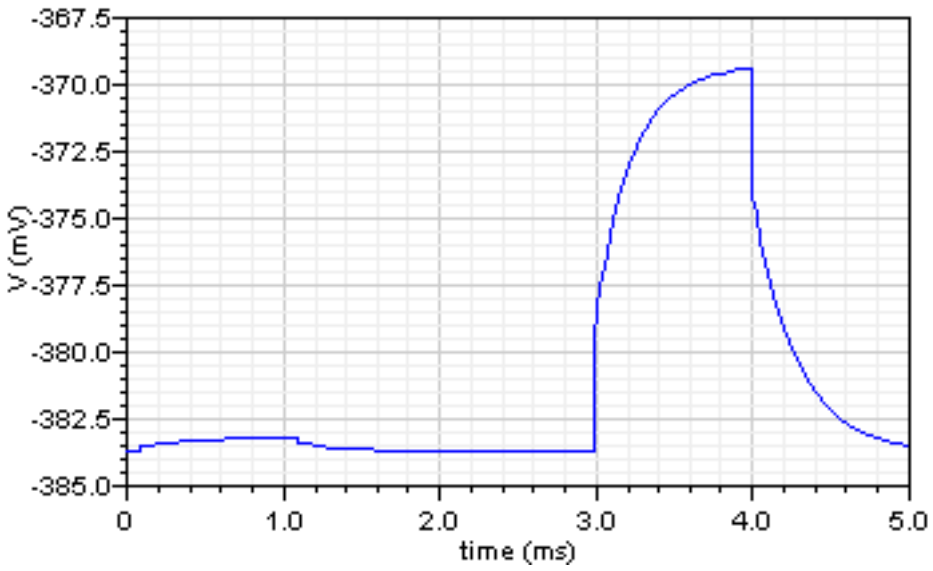
where $V_{in-}$ is the DC tension level present in the circuit on the negative input, and $V_{out}$ reproduces the output of the preamplifier when an input signal is applied.

Since a greater overshoot manifests on larger signals, it seemed to be caused by a non-linearity of the diodes parameters. To study the dependence of these parameters against the amplitude of the measured signal, the idea is, first of all to verify the trustworthiness of the model, than to study the DC operating points of the diodes varying the output DC level.

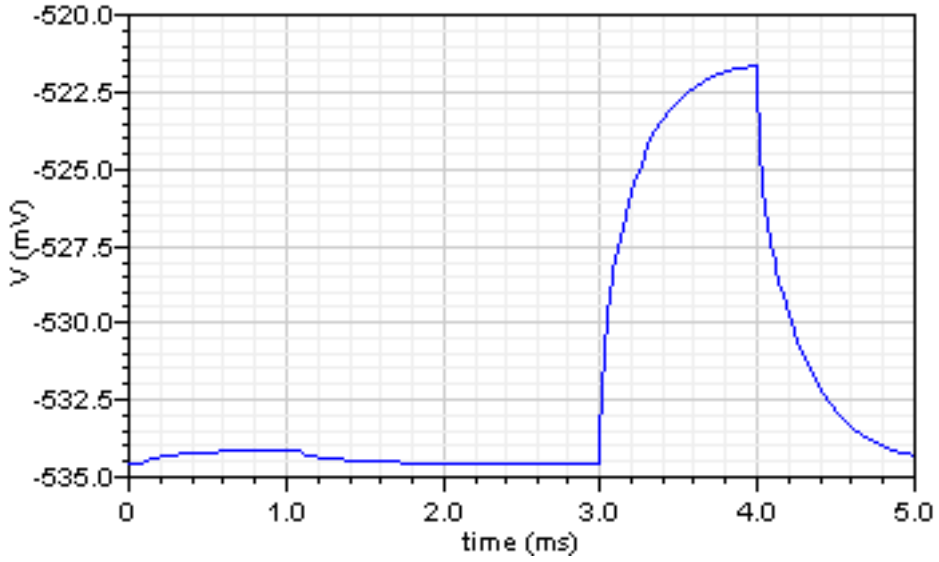
To verify the reliability of the model, the transient response of point P was studied and compared with the same point in the preamplifier. As shown in Fig. 4.7 the comparison demonstrates the good concordance of the model with the real situation.

It is than possible to study the diodes parameters when the output voltage level

moves, looking for a parameter which varies a lot. The maximum input signal from neurons is $150\mu V$ large, than the maximum output swing reaches $15mV$.




(a)

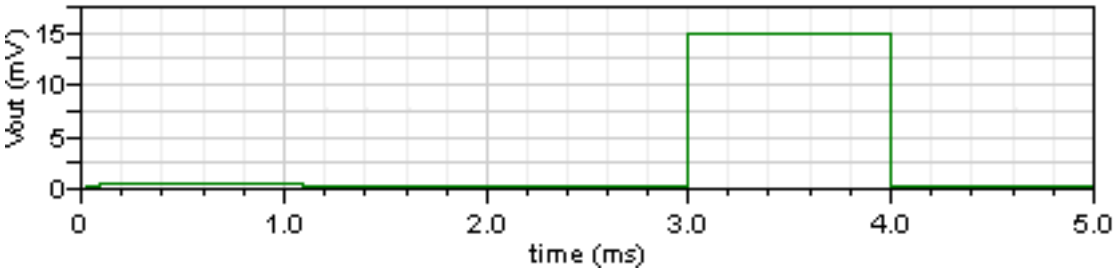



(b)

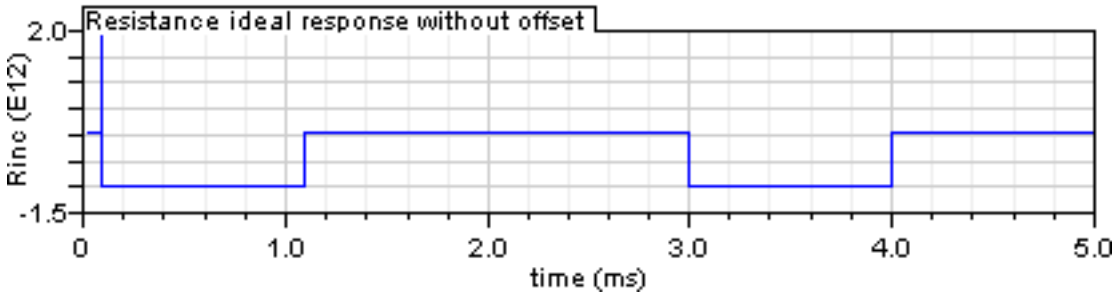
Figure 4.7: Transient response of point P on the model (a) and on the preamplifier (b)

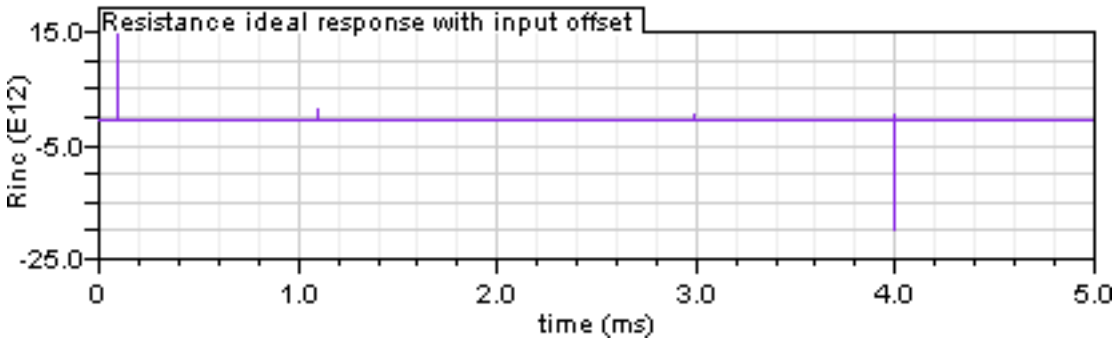
The behavior of diodes parameters for negative values of $V_{out}$ was not studied since in previous simulations the comparison between the output transient for positive and negative signals showed the independence of the overshoot effect from the signal sign[1].

[1]Varying the output voltage level, the polarization of the feedback diode is modified. The fact that the instability proves independent from this variation implies also that it is not due to the diode capacitance.

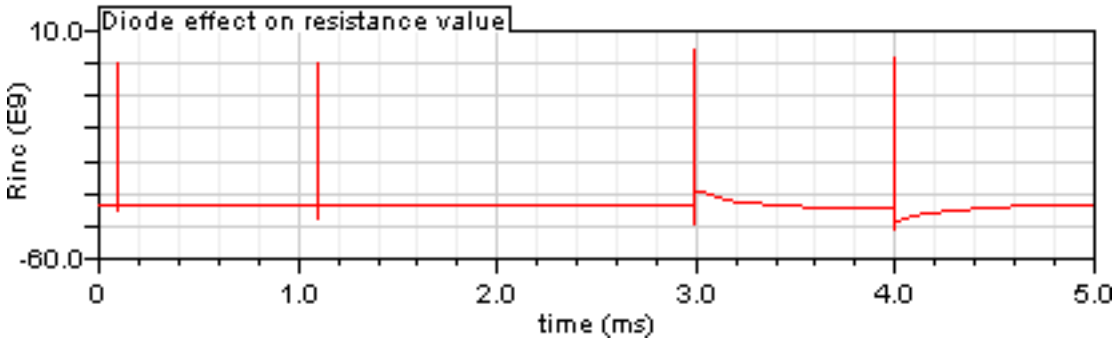



(a)




(b)




(c)

Figure 4.8: (a) Output signal applied. Incremental resistance behavior (b) without and (c) with parasitic diodes

No parameter which value varies remarkably has been found, suggesting that the problem is not tied to a DC parameter, but to the transient response itself. This evidence becomes much more pronounced if the incremental resistance transient is studied. The ideal transition of $R_{inc} = \frac{dV}{dI}$ at the edges of the MOS-bipolar pseudoresistor is depicted in Fig. 4.8(b).

The presence of the input offset ($\approx 383.7mV$) causes the incremental resistance to be always different from zero except in transitions when it shows large spikes. In fact, if the situation is compared with the characterization of the MOS-bipolar pseudoresistor (Fig 2.5), it is clear that if the voltage at the edges of it is greater than $0.2V$ the incremental resistance assumes values of the order of $\approx 10^{12}$.
Moreover, the presence of diodes on feedback resistance is responsible for a large current flowing through the transistor composing the pseudoresistor. The larger they are, the higher is their gate capacitance, the longer the settling time of the incremental resistance. This phenomenon is highlighted in Fig. 4.8(c) and is at the origin of the overshoots and undershoots on the preamplifier transient response.
To confirm this theory the same measurements have been repeated using smaller transistor to make the pseudoresistors, $\frac{W}{L} = \frac{1\mu m}{1\mu m}$ instead of $\frac{W}{L} = \frac{2\mu m}{2\mu m}$. Owing to their lower gate capacitance, they are expected to be affected by shorter settling time, what actually happens, as shown in Fig 4.9

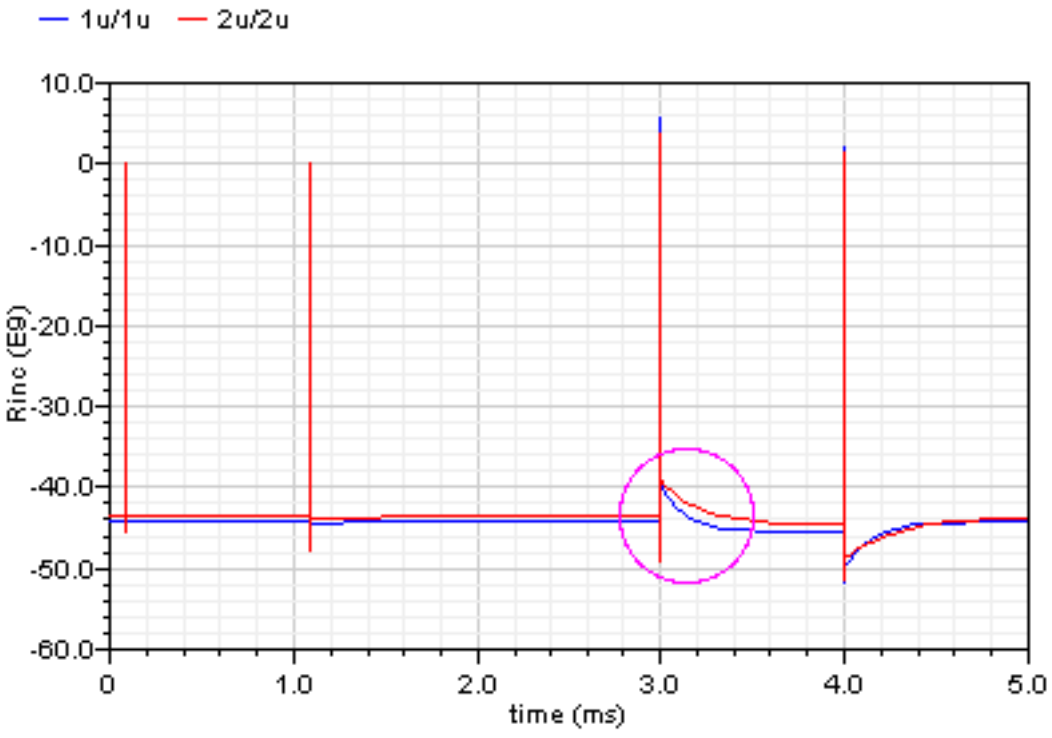
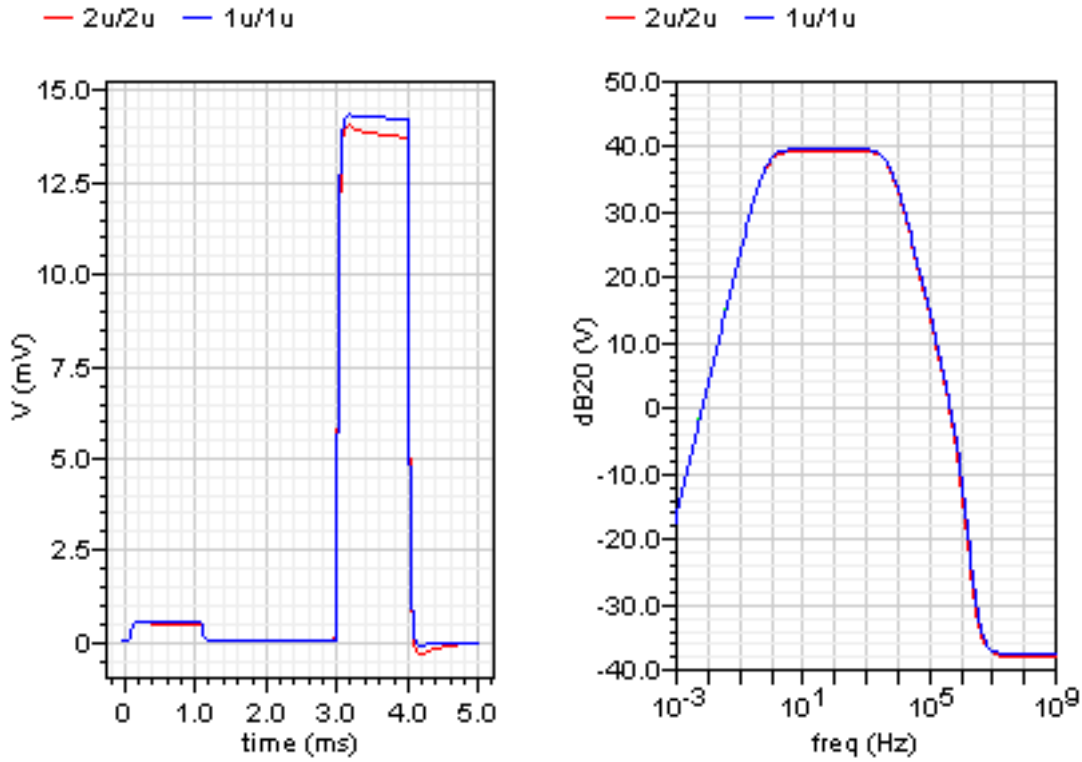
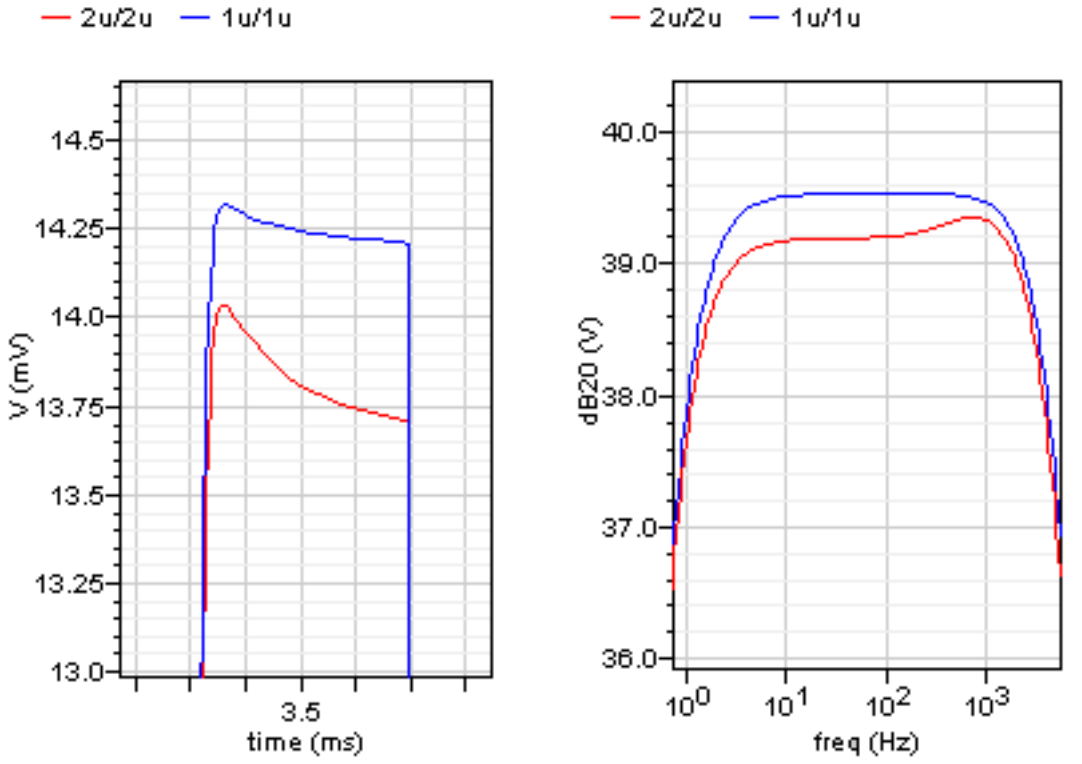



Figure 4.9: Shorter MOS-bipolar pseudoresistor settling time using smaller transistors

As a consequence both the transient and the AC responses of the preamplifier get better (Fig. 4.10) even if the offset on the OTA's inputs does not ameliorate.




(a) (b)




(c)

Figure 4.10: Preamplifier transient (a) and AC (b) responses. (c) Zoom on more affected regions

## 4.2 Noise issues

### 4.2.1 Single stage OTA

As discussed before, an important issue of the preamplifier is low noise. A first simulation of the Harrison preamplifier composed with $p$-type symmetrical OTA (see Fig. 2.6) shows that the flicker noise of nMOS M5 and M6 transistors prevails. For $I_{bias} \simeq 5\mu A$ an input referred noise of $\simeq 3.88\mu V$ in a $5.05kHz$ bandwidth was found, which is too high for the scope. New simulations were performed increasing the $W/L$ ratio in M3-M6 transistor, thus reducing their $1/f$ noise. Results are reported in table 4.1.

| $(W/L)_{nMOS}$ | $V_{irn}(\mu V)$ | Prevailing noise |
|---|---|---|
| $2\mu m/20\mu m$ | 3.88 | $1/f$ noise of M5 and M6 |
| $3\mu m/30\mu m$ | 3.52 | $1/f$ noise of M5 and M6 |
| $4\mu m/40\mu m$ | 3.39 | Thermal noise of M5 and M6 |
| $4\mu m/60\mu m$ | 3.24 | Thermal noise of M5 and M6 |

Table 4.1: $p$-type symmetrical OTA Harrison preamplifier noise

Using a $n$-type symmetrical OTA (Fig. 4.11), the noise decreases of $\approx 15\%$, but the thermal noise of nMOS transistors (M7 and M8) is prevailing.

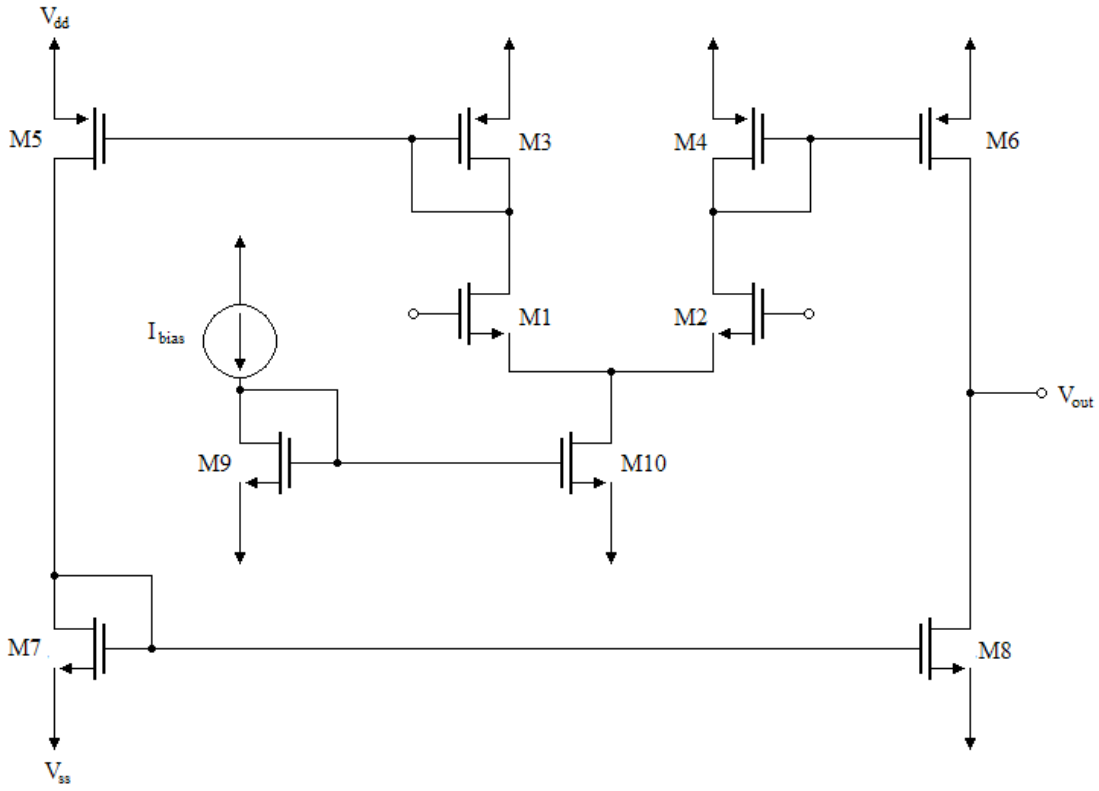



Figure 4.11: $n$-type symmetrical OTA

With $I_{bias} = 5\mu A$ and an input referred noise of $\simeq 3.26\mu V$ in a $5.72kHz$ bandwidth was measured, against the $3.88\mu V$ of the pMOS OTA analogous case (note that the noise is inferior in comparison with the *p*-type configuration even if the bandwith is larger).

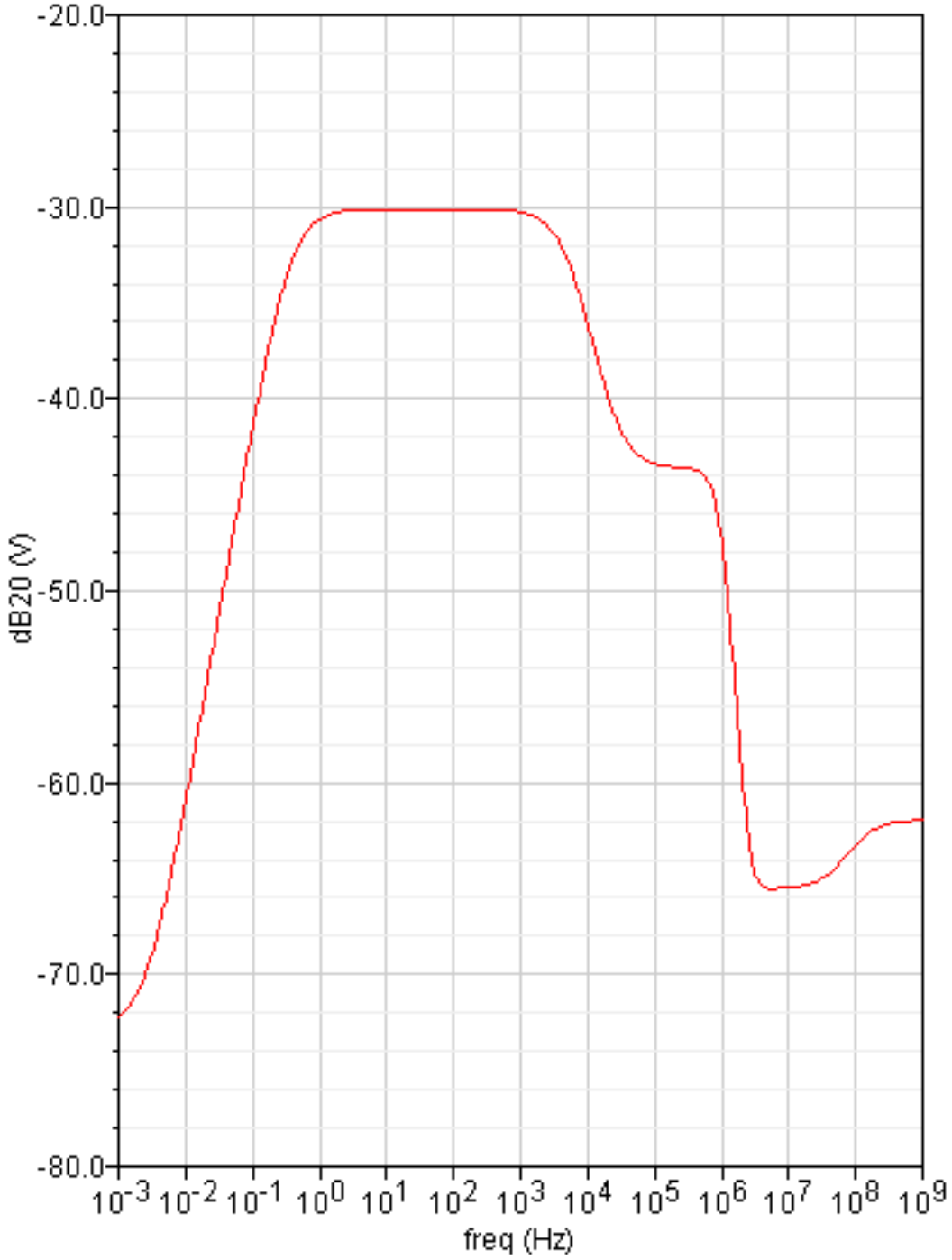
Nevertheless it is essential to pay attention to the PSRR (Power Supply Rejection Ratio), in fact, even if the nMOS OTA exhibit a lower noise, the *p*-type configuration is supposed to be less sensible to the noise on the supply lines since the input transistors have their bulk connected to the source.
The PSR study on each supply line takes three steps:

Small signal analysis Applying a $1mV$ pulse on the supply line the AC response for small signals is studied;

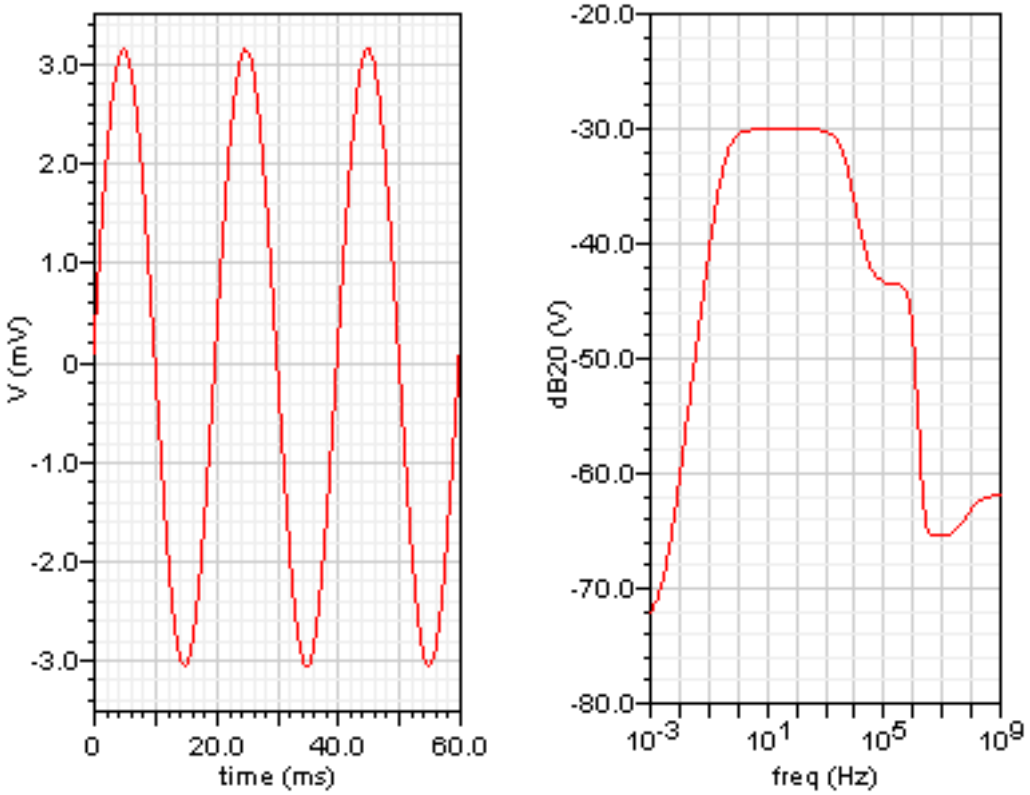
First large signal analysis A $100mV$ sinusoid at $50Hz$ is used to study the large signal response at the electric network typical frequency;

Second large signal analysis A $100mV$ square wave at $200kHz$ permits to analyze the response at the second typical disturbance frequency (the one in which, for example DC-DC converters operate).

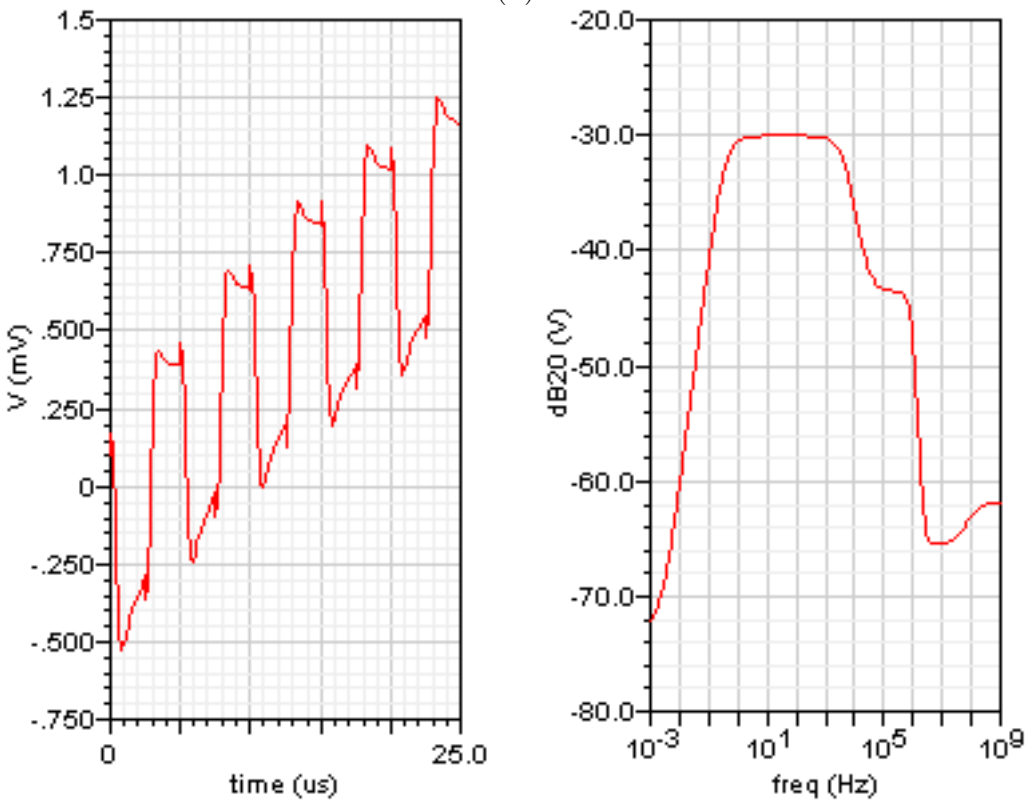
Results are shown in Fig.4.12 to Fig. 4.15.
First of all, the analysis of small and large signal show that the response for small and large signals is the same in all cases, involving that there are is not non-linearities in the circuit.
On the other hand, comparing the transfer functions of the two OTA configurations it is clearly visible that the pMOS configurations slightly more tolerant to disturbs on the power supply than the nMOS one, as expected.


-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
dB20 (V)
10-3 10-2 10-1 100 101 102 103 104 105 106 107 108 109
freq (Hz)

(a)

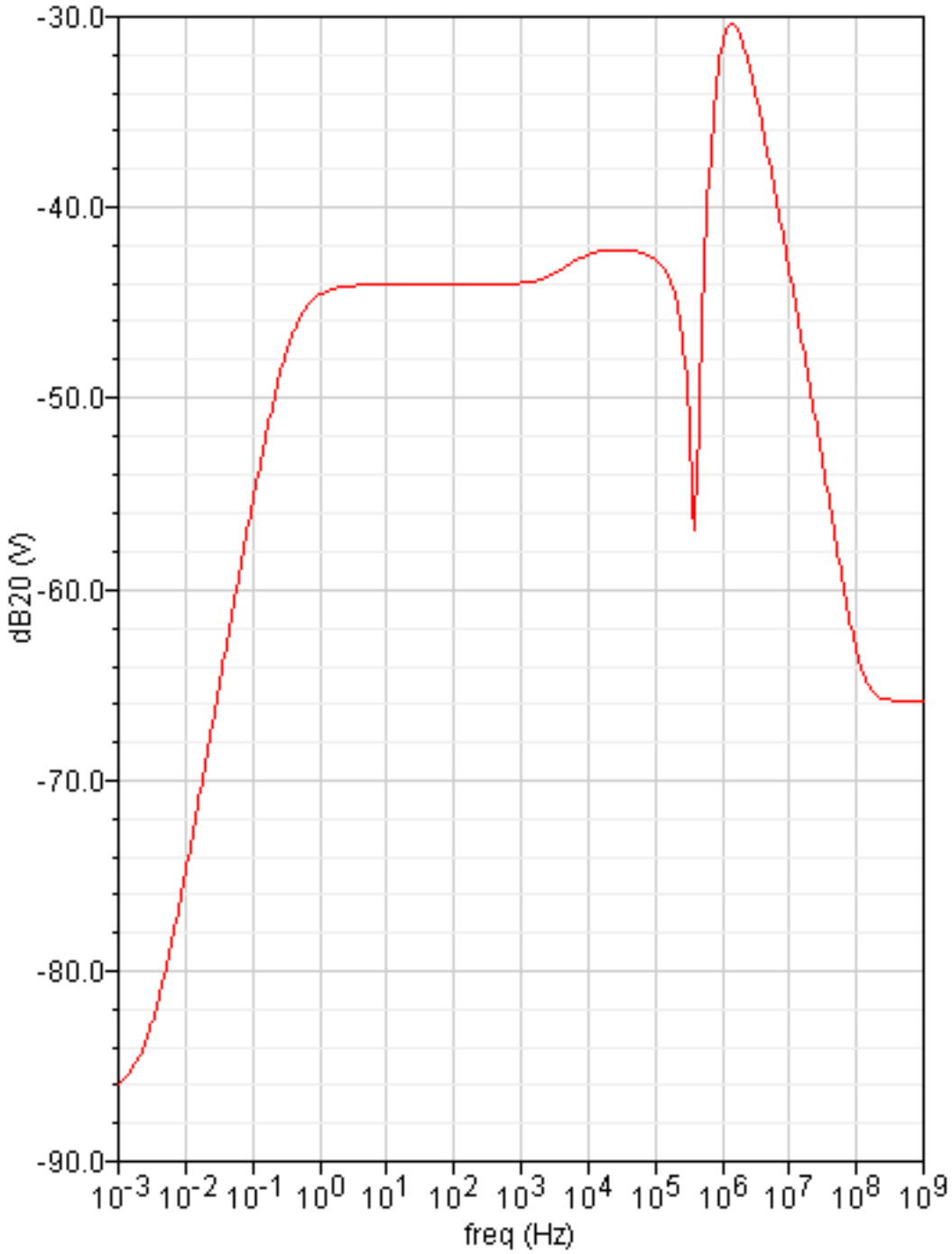



(b)

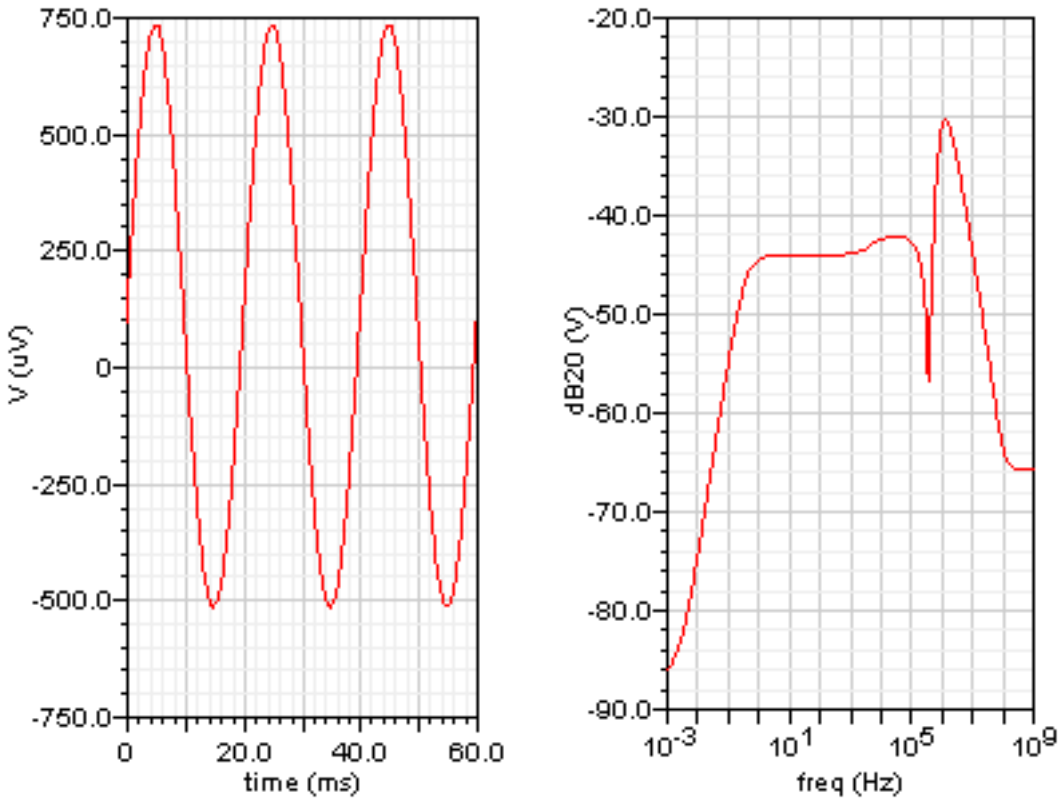



(c)

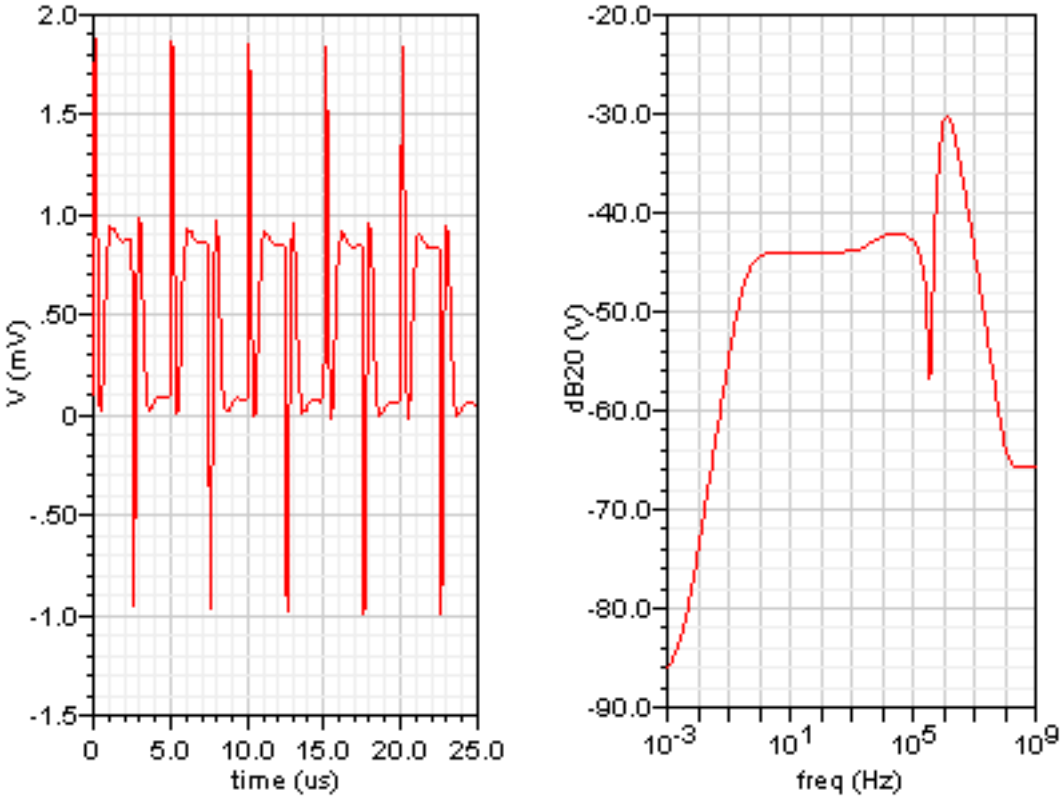
Figure 4.12: PSR of pMOS OTA on $V_{dd}$. (a) Small signal analysis. (b) First large signal analysis. (c) Second large signal analysis


-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
dB20 (V)
10-3 10-2 10-1 100 101 102 103 104 105 106 107 108 109
freq (Hz)

(a)

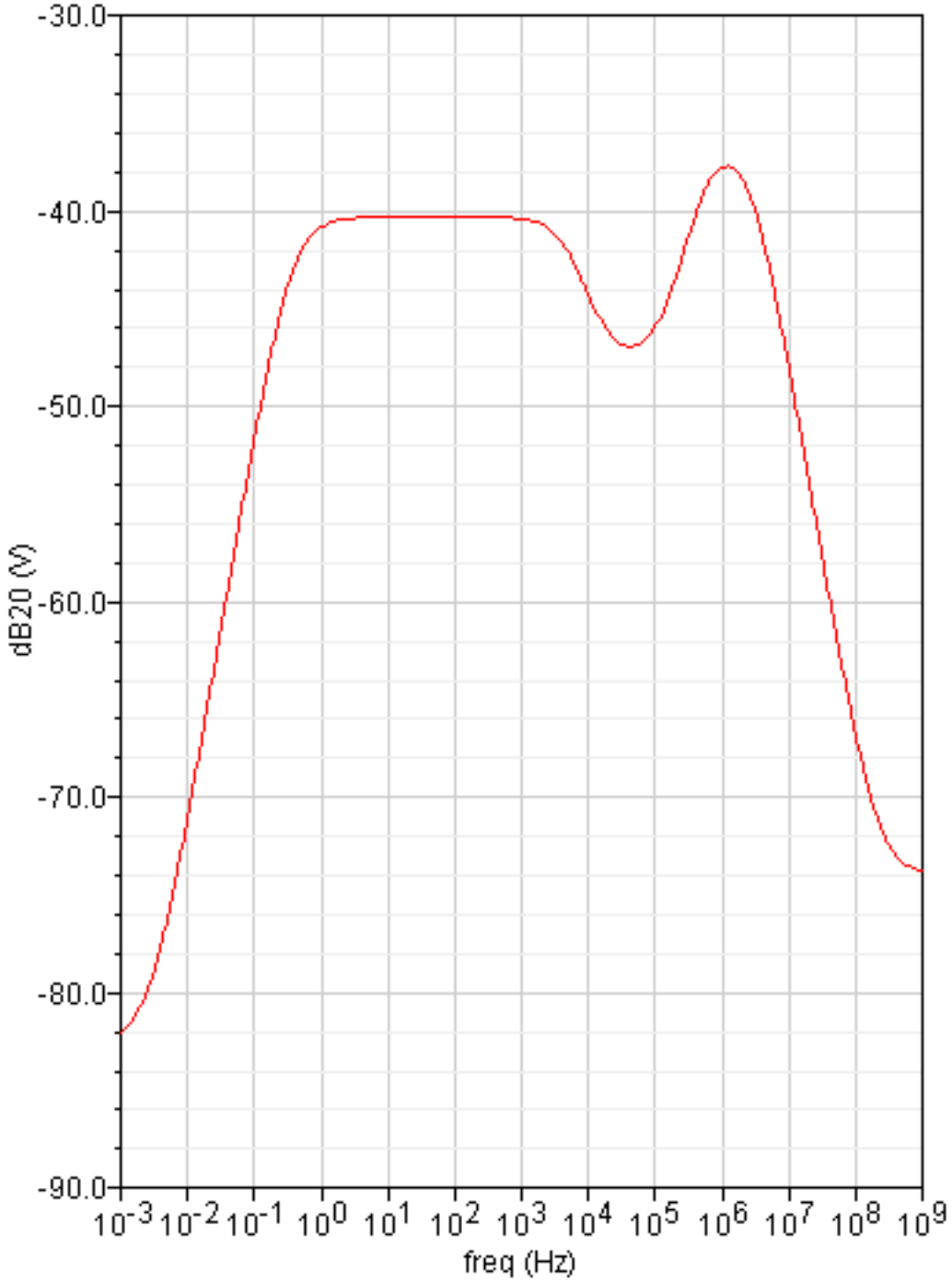



(b)

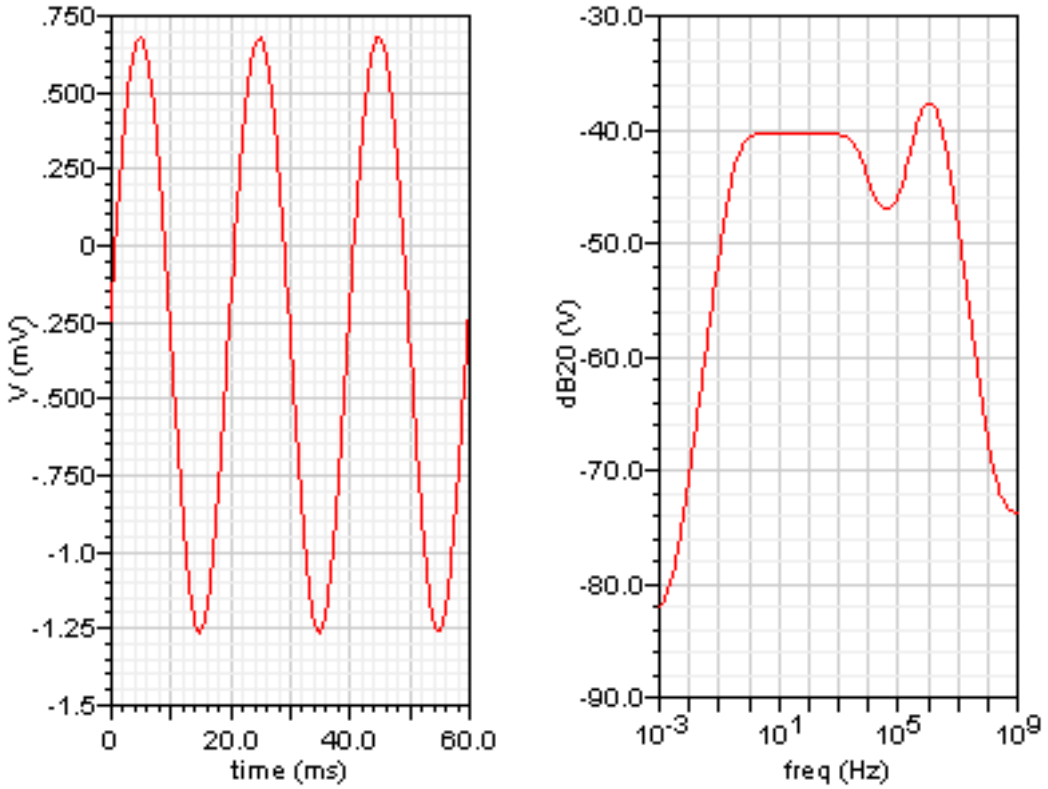



(c)

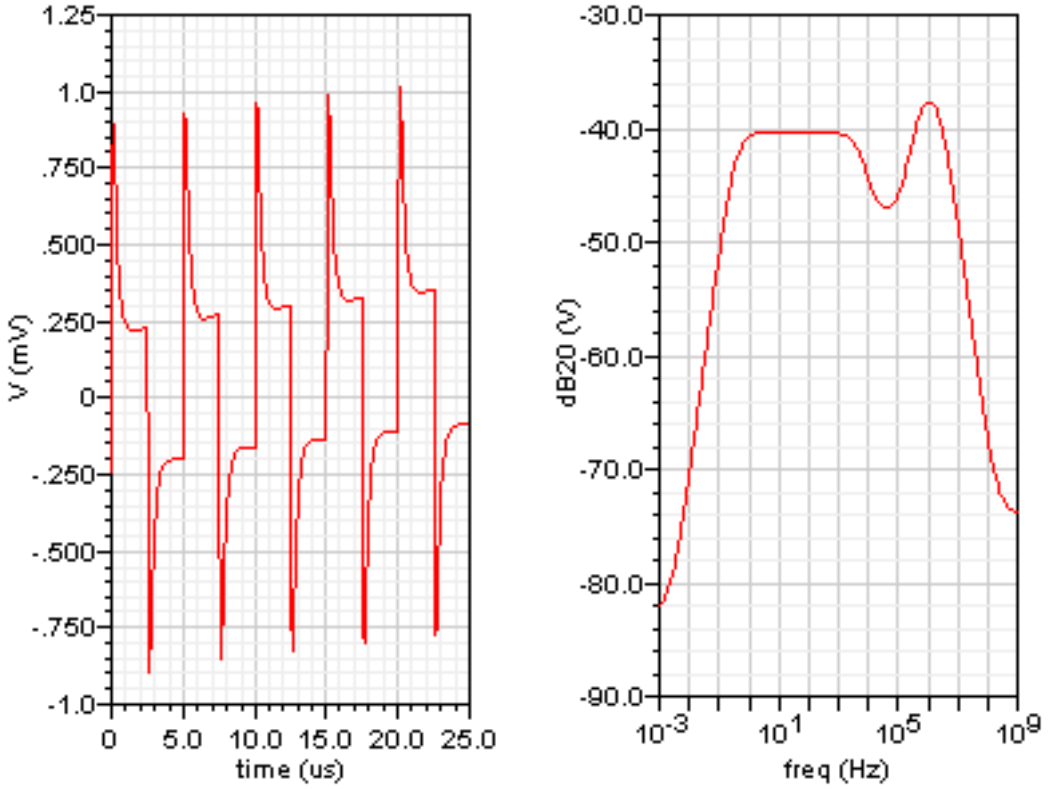
Figure 4.13: PSR of pMOS OTA on $V_{ss}$. (a) Small signal analysis. (b) First large signal analysis. (c) Second large signal analysis


-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
dB20 (V)
10-3 10-2 10-1 100 101 102 103 104 105 106 107 108 109
freq (Hz)

(a)

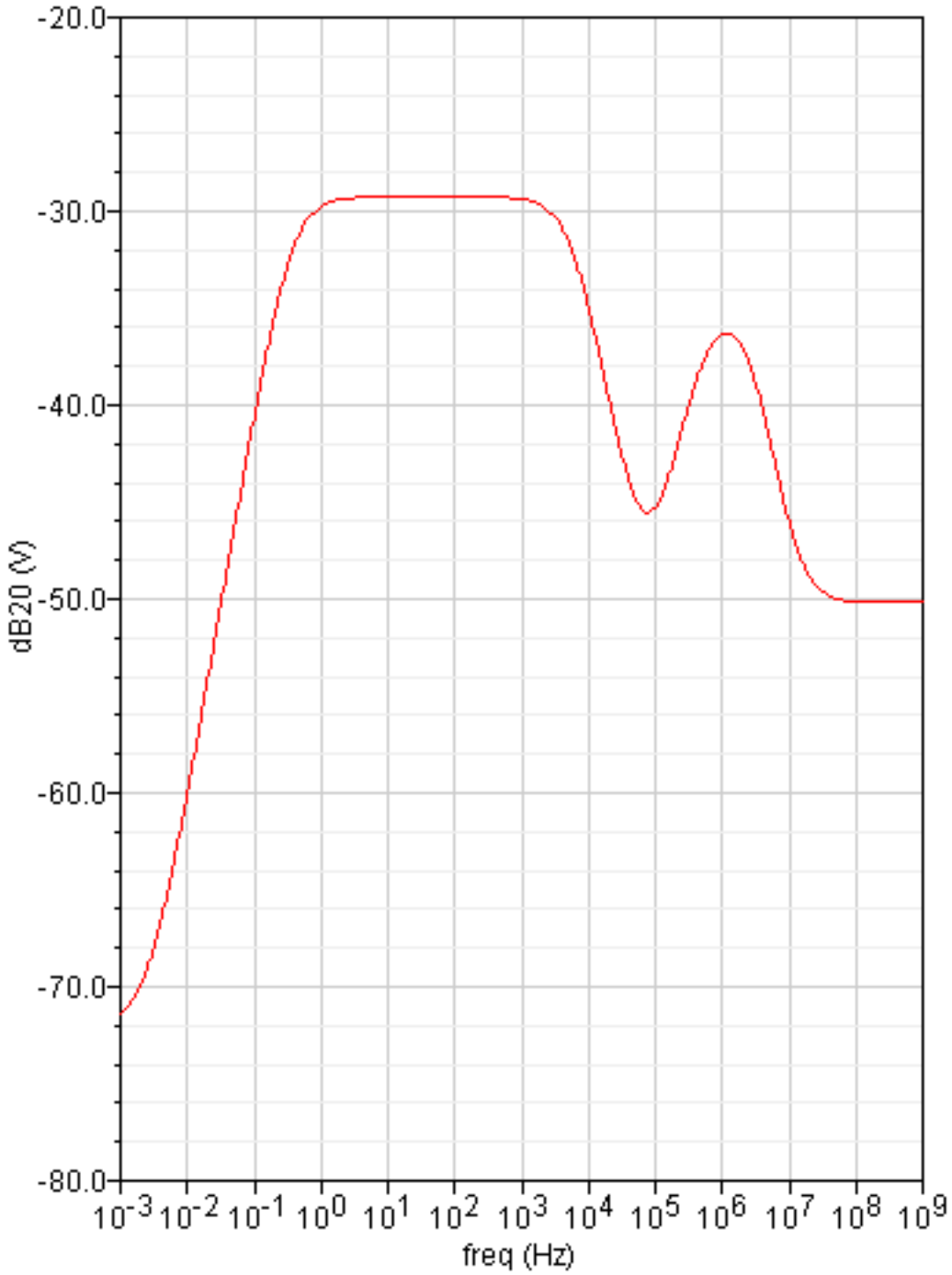



(b)

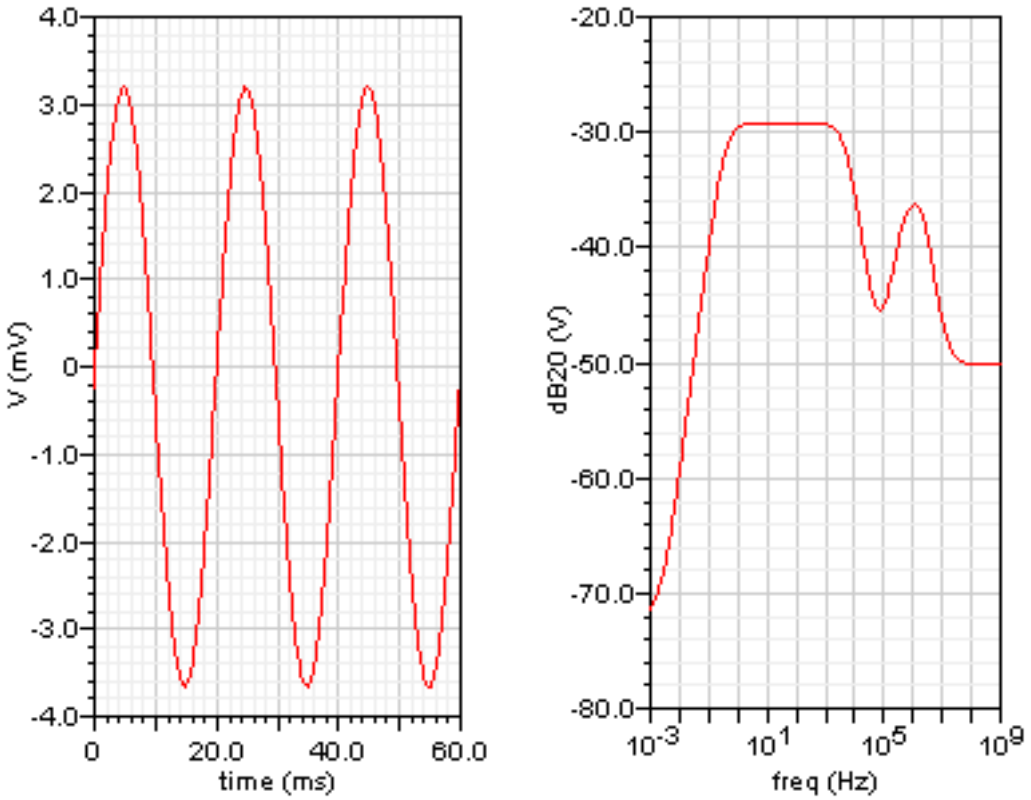



(c)

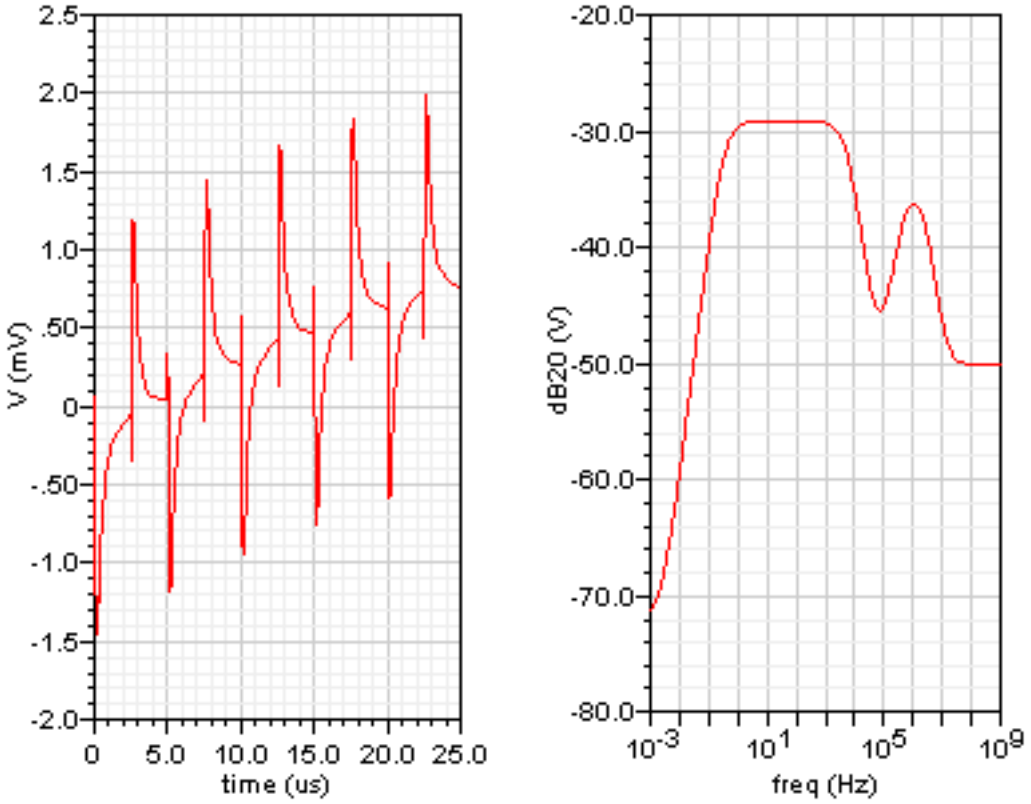
Figure 4.14: PSR of nMOS OTA on $V_{dd}$. (a) Small signal analysis. (b) First large signal analysis. (c) Second large signal analysis


-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
dB20 (V)
10-3 10-2 10-1 100 101 102 103 104 105 106 107 108 109
freq (Hz)

(a)




(b)

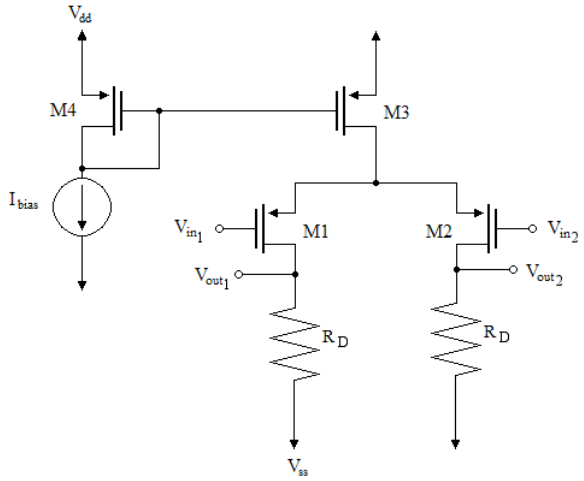



(c)

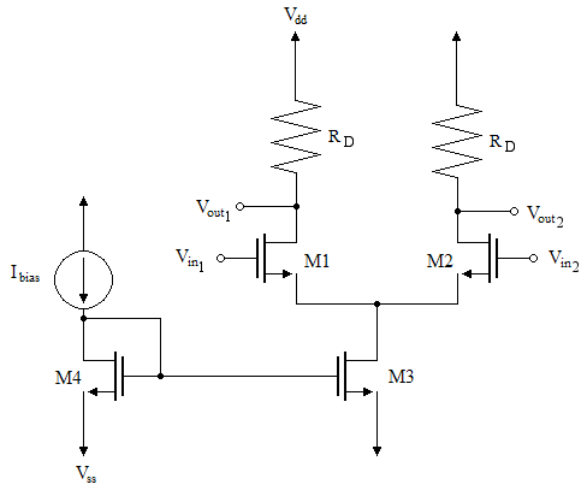
Figure 4.15: PSR of nMOS OTA on $V_{ss}$. (a) Small signal analysis. (b) First large signal analysis. (c) Second large signal analysis

### 4.2.2 Two stage OTA

It would be suitable having the input transistors (M1 and M2) thermal noise prevailing. If so, it would be possible to reduce considerably the noise increasing $I_{bias}$ (thus the power dissipation), and than optimizing the channel.
To achieve this result a double stage OTA can be used instead of a single symmetrical OTA. Introducing a fully differential stage, with a gain of at least $10V/V$, in front of the symmetrical OTA, the first stage noise becomes dominant, thus it would be feasible to reduce the noise operating only on the first stage.
The first stage has been realized as a fully differential symmetrical OTA with resistive loads[2] (Fig. 4.16).




(a)




(b)

Figure 4.16: Fully differential OTA with resistive loads with (a) pMOS and (b) nMOS input transistors

[2]Note that the use of resistive loads yields to a lower flexibility in biasing current changes.

It is than possible to study the behavior of four configurations:

- ***p-p* configuration:** first and second stages with pMOS input transistors
- ***p-n* configuration:** first stage *p*-type and second stage *n*-type
- ***n-p* configuration:** first stage with nMOS input transistors and second stage with pMOS input transistors
- ***n-n* configuration:** both stages using nMOS input transistors

Maintaining the input transistors with $\frac{W}{L} = \frac{1000}{5}$ their flicker noise is kept low. Forcing $I_{bias} = 5\mu A$ and using a mirroring coefficient of $(\frac{W}{L})_3/(\frac{W}{L})_4 = \frac{40}{20}/\frac{20}{20} = 2$, the current which flows in M1 and M2 is given by $\frac{2 \cdot I_{bias}}{2} = 5\mu A$.
Since M1 and M2 work in weak inversion, it results:

$$I_{DS1,2} \simeq I_0 e^{\frac{V_{GS1,2}}{\zeta V_T}} \tag{4.1}$$

$$g_{m1,2} = \frac{\delta I_{DS1,2}}{\delta V_{GS1,2}} \simeq \frac{I_{DS1,2}}{\zeta V_T} = \frac{5\mu A}{1.3 \cdot 26mV} = -147.93\mu S \tag{4.2}$$

where $\zeta \sim 1.3$ is a non-ideality factor and $V_T = \frac{K_B T}{q} \simeq 26mV$.
Using a supply of $-1.65V$-$1.65V$, the output DC level must arrange to $0V$. Thereby $R_D$ has to be sized accordingly:

$$R_D = \frac{1.65V}{5\mu V} = 330k\Omega \tag{4.3}$$

The gain is equal to:

$$A_V = -g_{m1,2} R_D // \frac{1}{g_{DS1,2}} \simeq -g_{m1,2} R_D \simeq -147.93 \cdot 10^{-6} S \cdot 330 \cdot 10^3 \Omega \simeq -49 \tag{4.4}$$

which is sufficiently high for our scope.

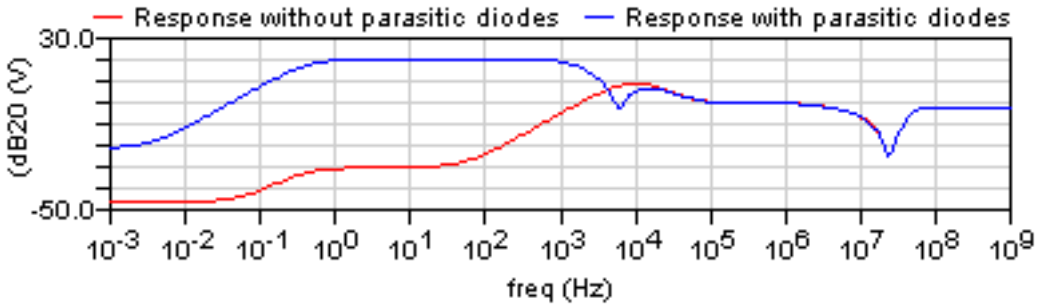
Using the two stage OTA, the second stage noise is no more critical, it is than convenient to reduce the second stage transistors dimensions and decreasing its bias current. As a first optimization, the symmetrical OTA input transistors and its mirroring coefficient have been halved resulting in $\frac{W}{L} = \frac{500}{5}$ and $I_{DS} = 1.25\mu A$. Than the four configurations have been simulated, results are reported in table 4.2.

| Configuration type | $V_{irn}(\mu V)$ |
|---|---|
| *p*-*p* | 2.11 |
| *p*-*n* | 2.11 |
| *n*-*p* | 1.96 |
| *n*-*n* | 1.96 |

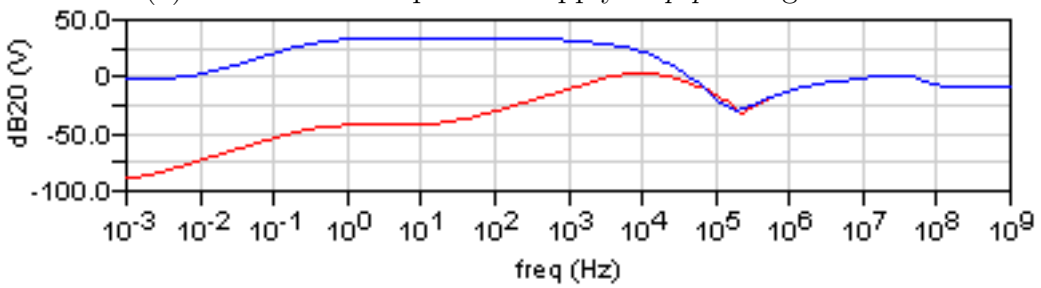
Table 4.2: Noise response of the complete channel amplifying $67.83dB$ in a bandwith $6kHz$ large using a two stage OTA Harrison preamplifier

The noise is abundantly dominated by the thermal noise of the first stage input transistors ($30\% - 40\%$ of the total output noise).

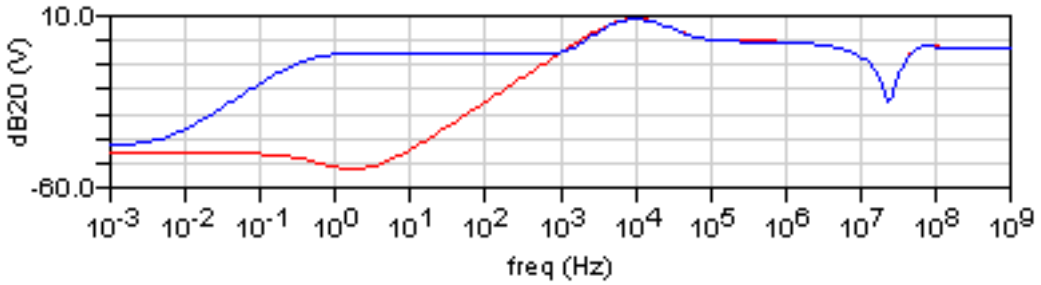
As in the single stage case, *n-p* and *n-n* configurations exhibit lower noise, but the experience a slightly rougher PSSR. However, introducing the parasitic diodes on the MOS-bipolar pseudoresistors, something happens, the PSRR degrades considerably for the configurations using pMOS input transistor. It is clearly visible in Fig. 4.17



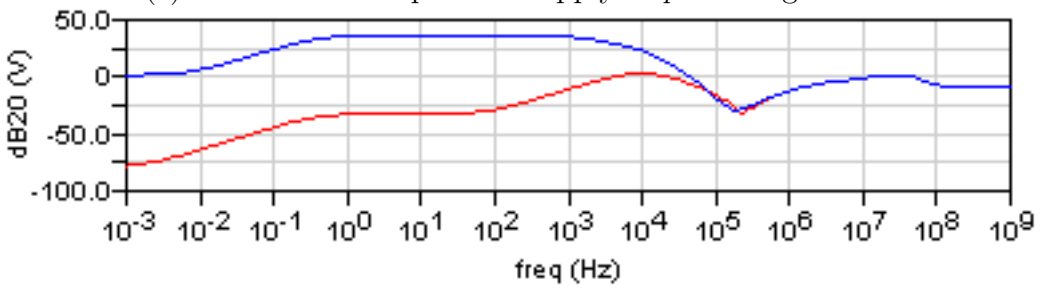

(a) Disturbance on positive supply in *p-p* configuration



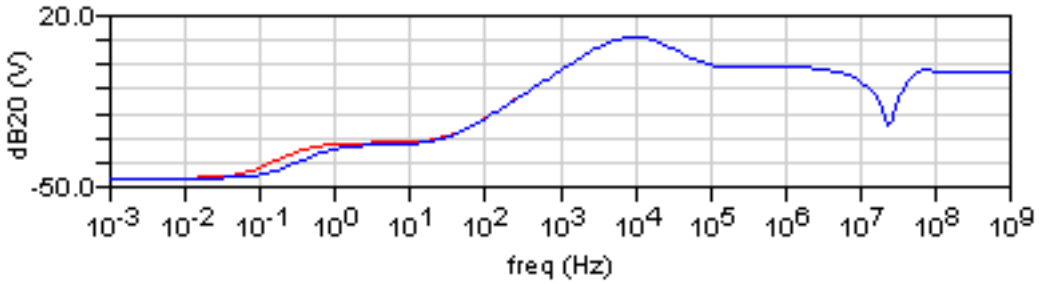

(b) Disturbance on negative supply in *p-p* configuration



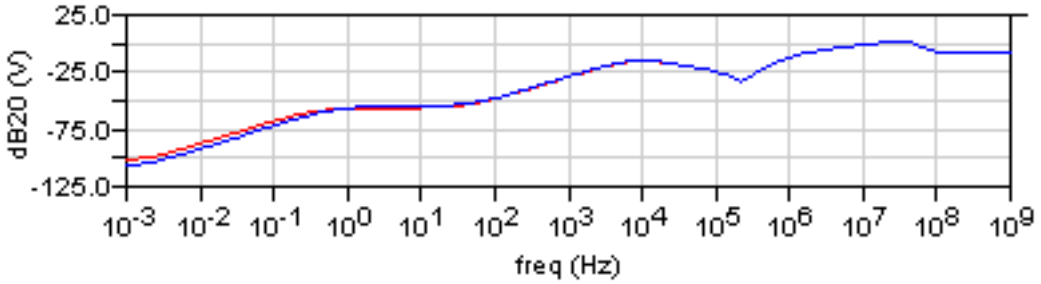

(c) Disturbance on positive supply in *p-n* configuration



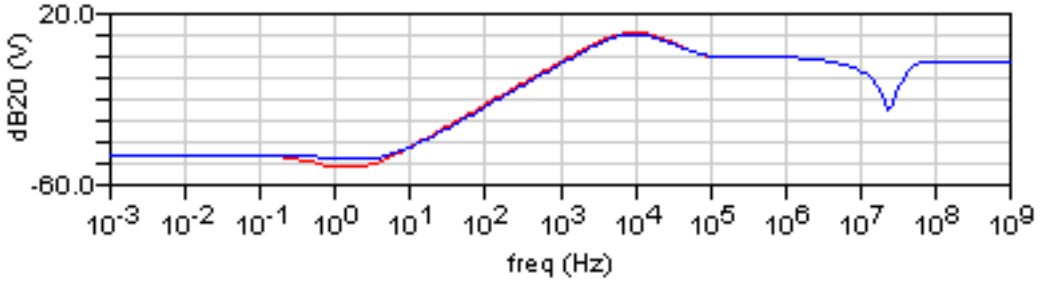

(d) Disturbance on negative supply in *p-n* configuration



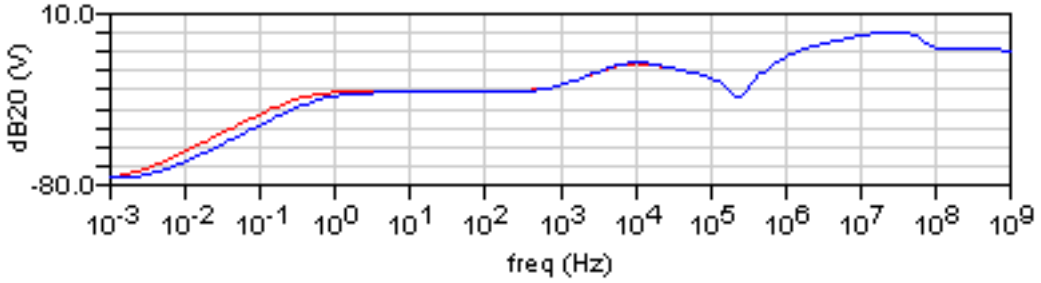

(e) Disturbance on positive supply in *n*-*p* configuration




(f) Disturbance on negative supply in *n*-*p* configuration




(g) Disturbance on positive supply in *n*-*n* configuration




(h) Disturbance on negative supply in *n*-*n* configuration

Figure 4.17: Degrading of power supply rejection at low frequencies due to parasitic diodes in MOS-bipolar pseudoresistors

Due to its higher tolerance to power supply disturbs, the *n*-*n* configurations has been optimized. In order to reduce furthermore the noise it is possible to increase once again the biasing current in the first stage (degrading the power consumption). Note that increasing the current in the input transistors they move away from the weak inversion working zone, than their $g_m$ becomes proportional to $\sqrt{I_{DS}}$ rather than to $I_{DS}$, thus increasing anymore the current may become profitless.
Moreover, to dampen the area occupation, the input transistors of the second stage are made smaller as much as allowed by their noise.
Result of simulations performed with $20\mu A$[3] flowing in the first stage (mirroring coefficient: $(\frac{W}{L})_3/(\frac{W}{L})_4 = (\frac{80}{20})/(\frac{20}{20}) = 4$) are shown in table 4.3.

| Second stage input transistors $W/L$ | $V_{irn}(\mu V)$ |
|---|---|
| $500\mu m/5\mu m$ | 1.646 |
| $120\mu m/5\mu m$ | 1.647 |
| $60\mu m/5\mu m$ | 1.648 |
| $20\mu m/5\mu m$ | 1.655 |

Table 4.3: Complete channel input referred noise variation with second stage input transistors dimensions

The power dissipation of the complete channel results in $82.52\mu W$. If the current in the second stage is changed from $2.5\mu A$ to $5\mu A$, the noise lower to $V_{irn} = 1.650\mu V$, while the power consumption raise to $99.14\mu W$.
At the end, $(W/L) = 120\mu m/5\mu m$ have been chosen not to introduce mismatches which could degrade too much the output offset.

### CMIR

The introduction of the fully differential stage produces the necessity to pay attention to CMIR (Common Mode Input Range) of he second stage. Referring to Fig. 4.18, it is required:

$$\begin{aligned} V_{DS13} &\geq V_{DS,sat13} \\ V_{CM} - V_{GS5} = V_P &\text{ and } V_{DS13} = V_{ss} - V_P \\ \Rightarrow V_{CM} \geq V_{DS,sat13} + V_{GS5} + V_{ss} &= (199.4 + 599.2)mV - 1.65V = -851.4mV \end{aligned} \tag{4.5}$$

and:

[3]Note that the input transistors of the first stage are still working in weak inversion, in fact from simulations it results $g_m = 263\mu S$, which is similar to the theoretical value.

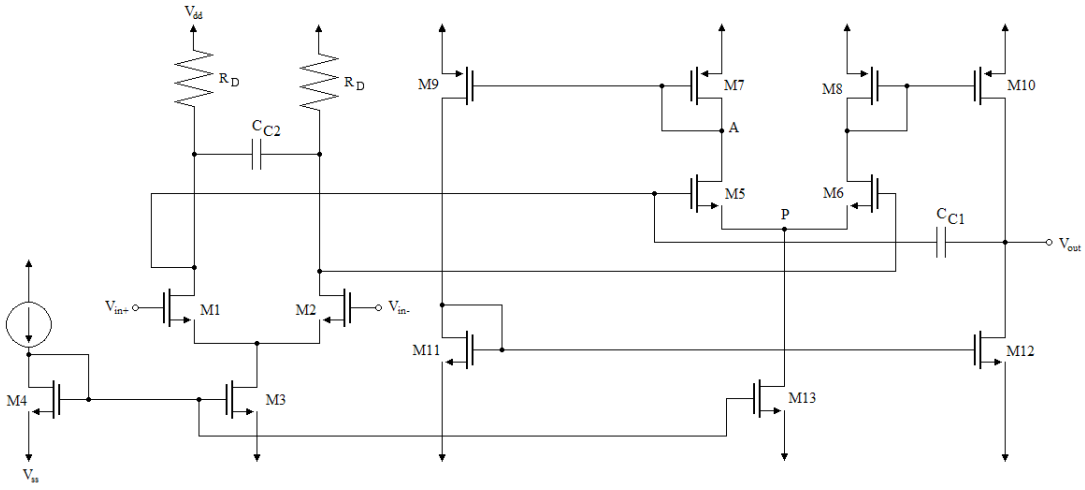



Figure 4.18: Complete two stage ota used for Harrison preamplifier

$$\begin{aligned} V_{DS5} &\geq V_{DS,sat5} \\ V_{DS5} &= V_A - V_P \\ \Rightarrow V_{CM} \leq V_A + V_{GS5} - V_{DS,sat5} &= (619.3 + 599.2 - 36.58)mV = 1.182V \end{aligned} \tag{4.6}$$

which results in a small input dynamics of $852.6mV$ for the second stage. Using a $20pA$ bias current in the first stage, than a load resistance of $175k\Omega$, the current flowing in the loads may vary from a minimum of $\frac{1.65V+851.4mV}{175k\Omega} = 15.160\mu A$ to a maximum of $\frac{(1.65-1.182)V}{175k\Omega} = 2.836\mu A$. This means that ideally the bias current in the first stage can be tuned in an interval in between $5.672\mu A$ and $30.320\mu A$, which is a sufficiently high range. Howewer this topic introduces the need of an AC coupling between the preamplifier and the filter stage or of an offset compensation.

### Two stage OTA Miller compensation

The use of the two stage OTA causes the presence of non-dominant poles in the OTA transfer function, thus the necessity of a Miller compensation. Since the OTA is used with a 40dB gain (which means an amplification of $100V/V$), a phase margin of 90° at $34dB$ ($50V/V$) is sufficient to ensure stability.
The first stage (Fig. 4.16) introduces a dominant pole at the frequency of

$$\omega_D \simeq \frac{1}{R_D c_L} \tag{4.7}$$

where $c_L$ is the input capacitance of second stage.
The second stage (Fig. 4.11) introduces, in order of importance, a single pole at

$$\omega_{ND1} = \frac{g_{DS10} + g_{ds12}}{c_L} \tag{4.8}$$

with $c_L$ input capacitance of the following stage, a double pole in

$$\omega_{ND2} = \frac{g_{m7}}{c_{gs7} + c_{gs9}} = \frac{g_{m8}}{c_{gs8} + c_{gs10}} \tag{4.9}$$

and another single pole in

$$\omega_{ND3} = \frac{g_{m11}}{c_{gs11} + c_{gs12}} \tag{4.10}$$

Using a two poles model the non-dominant pole is $\omega_{ND1}$, and the dominant pole

$$\omega_D = \frac{1}{R_D g_{mII} R_{II} c_{C1}} \tag{4.11}$$

where

$$g_{mII} R_{II} = \frac{g_{m5} g_{m10}}{g_{m7}} \frac{1}{g_{ds10} + g_{ds12}} \tag{4.12}$$

is the second stage gain.
The frequency at $34dB$ is $2.68MHz$, thus, since before the second pole the transfer functions increases of 20dB per decade and since the mid band open loop gain is 84dB, the dominant pole have to operate at $8.475kHz$, which implies

$$c_{C1} = \frac{1}{175k\Omega \cdot 58.65\mu S \cdot 6.15M\Omega \cdot 8.475kHz} = 1.87pF \tag{4.13}$$

Moreover, also a zero is introduced in the transfer function at a frequency of

$$f_Z = \frac{g_{mII}}{2\pi c_{C1}} = \frac{58.65\mu S}{2\pi \cdot 1.87pF} \simeq 5MHz \tag{4.14}$$

thus no Miller resistance is required to push the zero to infinity.

Looking at the transfer function after compensation (Fig. 4.19) it is clearly visible that the circuit is not completely compensated. This effect is due to the absence of a fully differential-single ended conversion in the OTA, than using $c_{C1}$ only one output of the first stage is compensated. The problem would be resolved introducing a second compensation capacitance between the other fully differential output and ground of the value of $g_{mII} R_{II} c_{C1} = 674.5pF$, which is absolutely non-integrable. Than a $7pF$ capacitance have been introduced between the two outputs of the first stage which behave like a short circuit at high frequency, permitting to $c_{C1}$ to compensate both outputs, as shown in Fig. 4.20.

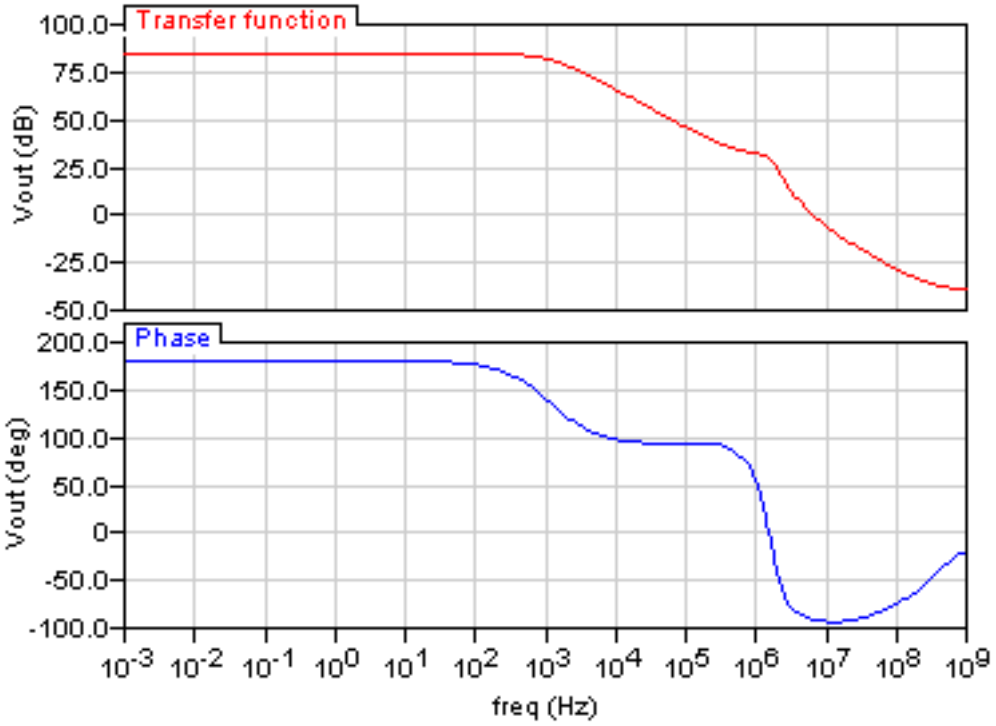



Figure 4.19: Two stage transfer function after Miller compensation ($c_{C1}$)

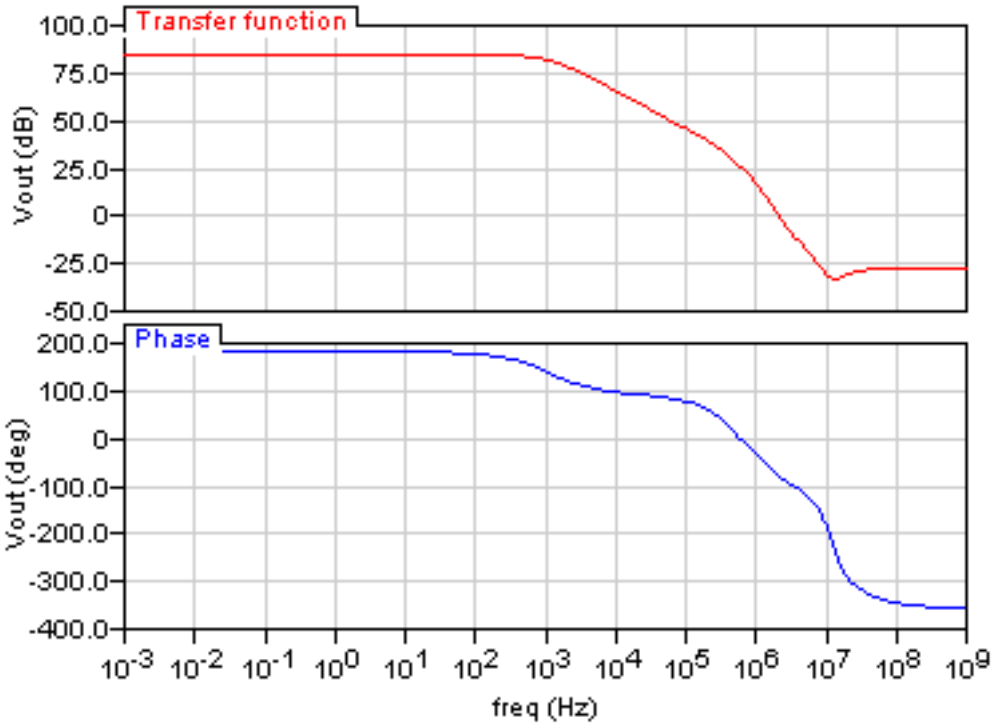
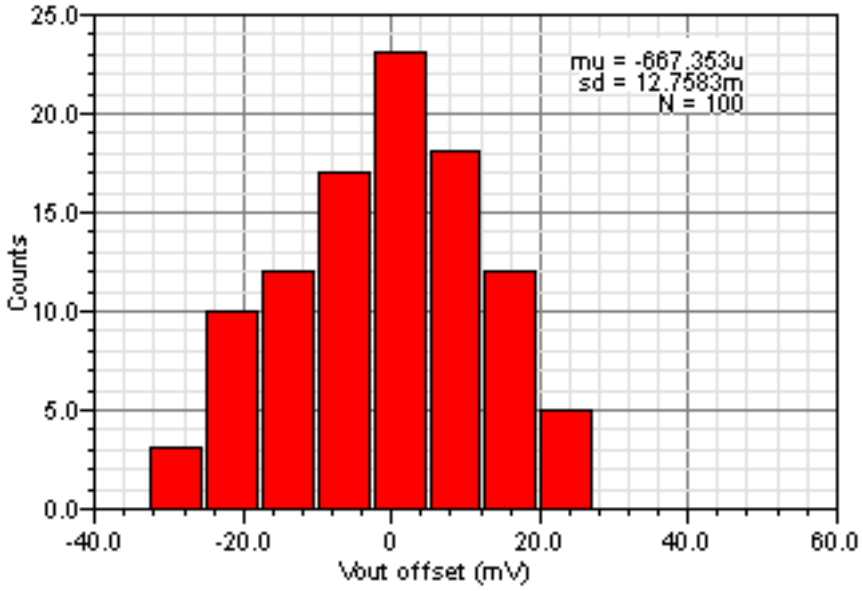


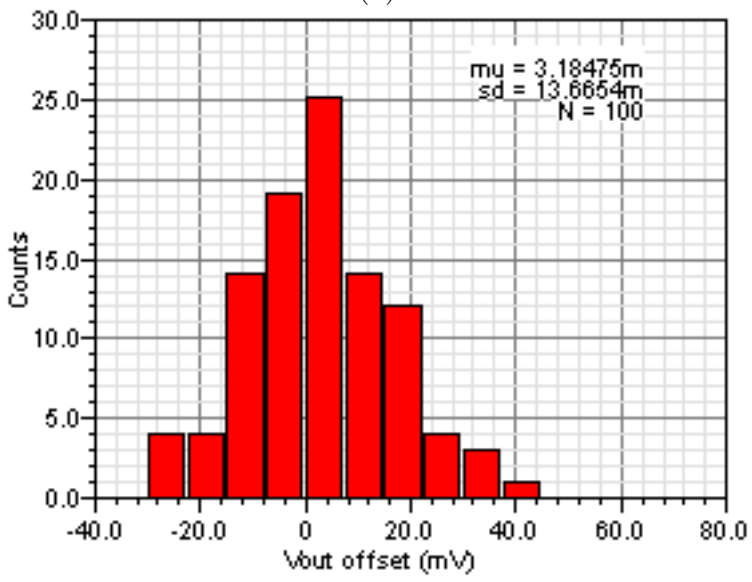

Figure 4.20: Two stage transfer function after second output compensation ($c_{C2}$)

### 4.2.3 Output offset

An important topic in the study of the preamplifier is the output offset. In fact a high offset can push out of working region the following stages, mainly because it is amplified of a factor 25 by the filter stage. Montecarlo simulation have been performed on both Harrison preamplifier using single and double stage OTAs (Fig. 4.21).




(a)




(b)

Figure 4.21: Montecarlo simulations of Harrison preamplifier layout using (a) single stage OTA with pMOS inputs and (b) double stage OTA in *n*-*n* configuration

At the input of the filter stage a random offset of 60-75$mV$, depending on case, can be found because of process variations and mismatches and it is amplified at

each step of the circuit chain.

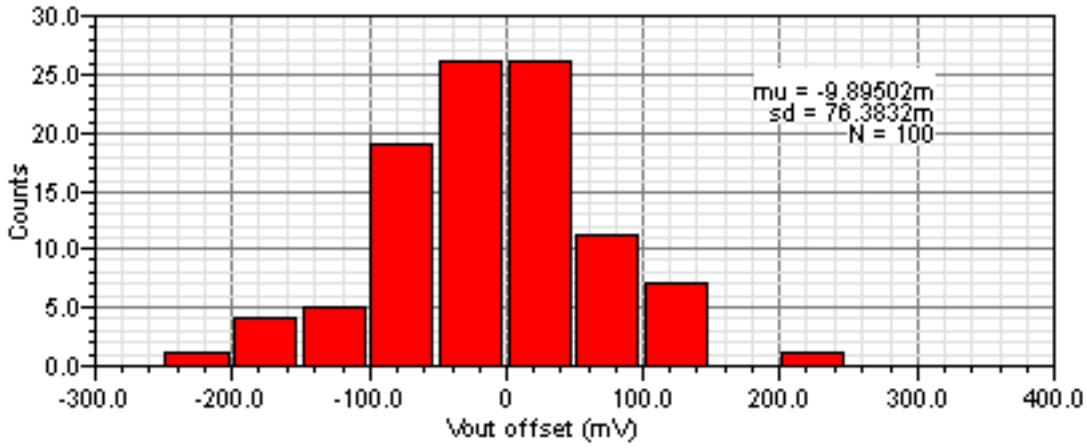
# Chapter 5

# Filter layout

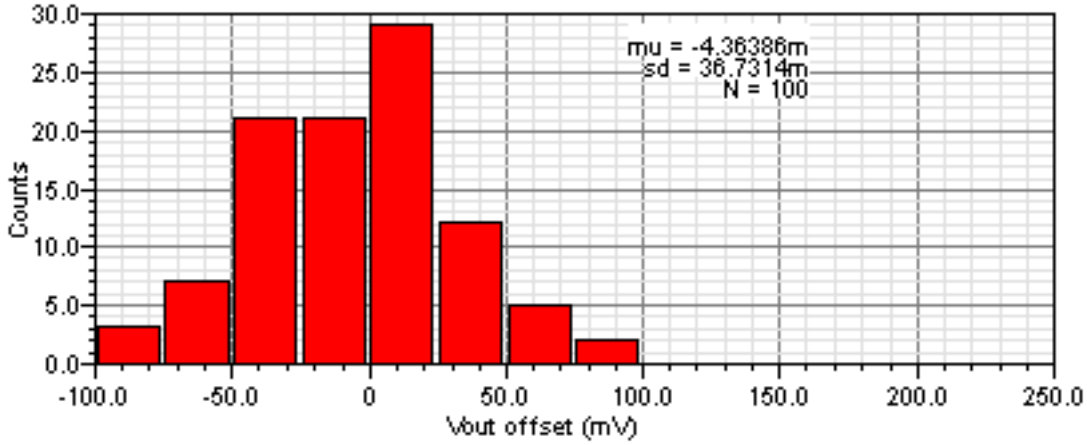
Main problems linked to filter layout concern its random offset introduced because of process variations and mismatches. It has been estimated through Monte Carlo simulations leading to the discovery of an interesting behavior.

## 5.1 Random offset dependence on source degeneration resistance

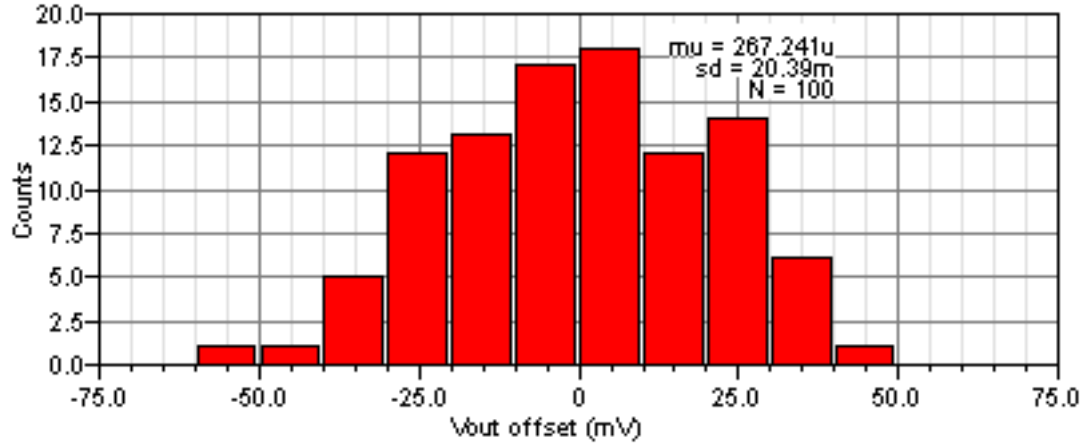
The first Monte Carlo simulation was performed using a load resistance of $R_S \sim 1M\Omega$ (see Fig. 2.7). The resulting random offset proved as high as $\sim 500mV_{pp}$. By decreasing the value of $R_S$, the offset reduces proportionally as shown in Fig. 5.1. The reason is that the source degeneration resistance decreases the open loop gain of the filter OTA, yielding to a higher sensitivity to random offsets introduced by mismatches.




(a)




(b)




(c)

Figure 5.1: Variation of random offset depending on $R_S$ value. (a) A $500mV_{pp}$ offset was found using $R_S \sim 1M\Omega$. (b) Halving $R_S$ it reduces to $\sim 200mV_{pp}$ and (c) a $\sim 110mV_{pp}$ offset was estimated reducing once again $R_S$ of a factor 2

## 5.2 AC coupling

Offset issues lead to the introduction of an AC coupling block which, introduced after each stage (see Fig. 5.2), keeps the random offset under control, preventing it from being amplified [7].

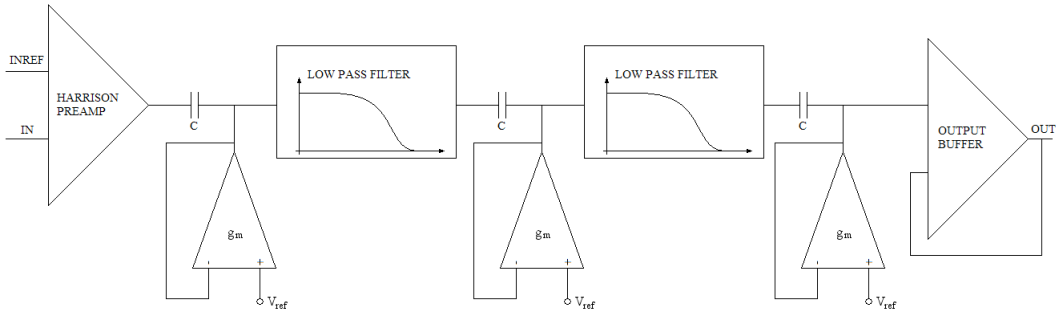
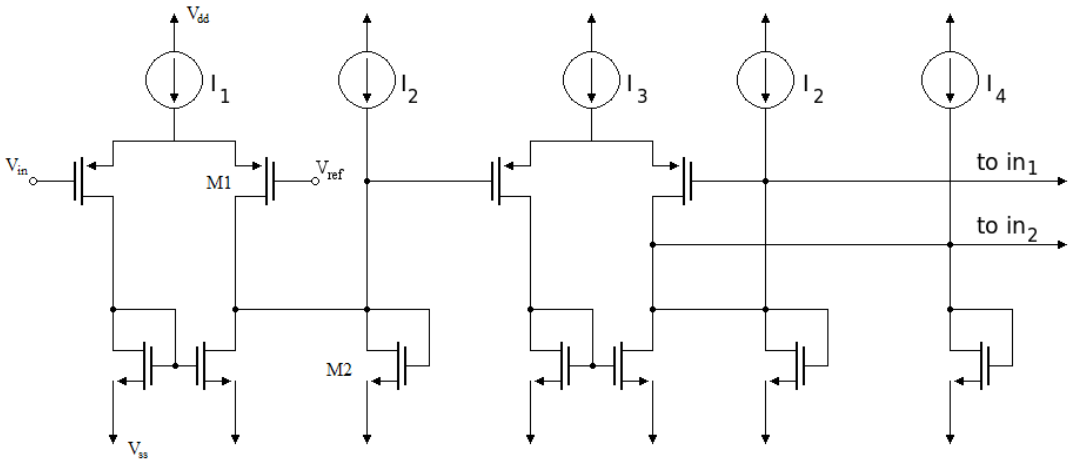



Figure 5.2: Channel block scheme with AC coupling circuits

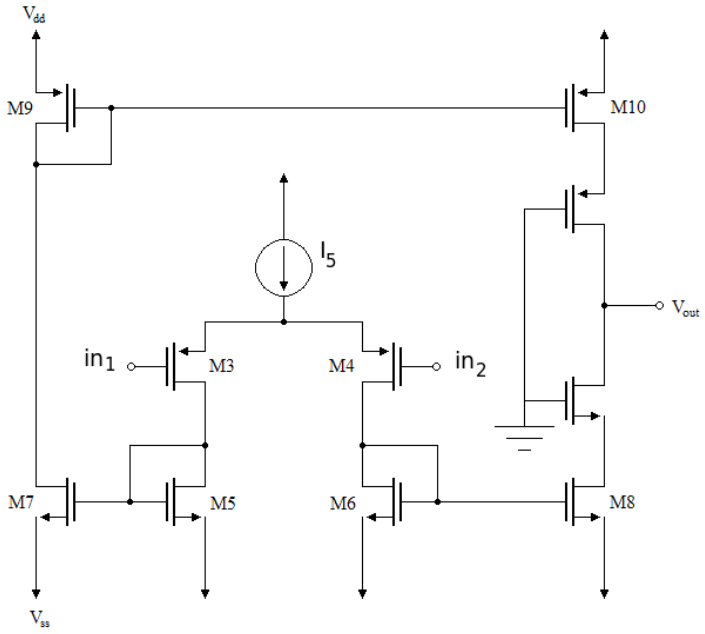
### 5.2.1 $g_m$-$\frac{1}{g_m}$ AC coupling block

[8] An alternative to implement a long time constant integrator is given by the $g_m$-$\frac{1}{g_m}$ chain approach. The time constant of this circuit is tunable and any offset voltages at the output terminal may be trimmed.

In the design of the integrator each $g_m$ stage was realized by a simple CMOS OTA with *p*-MOS inputs and each $\frac{1}{g_m}$ stage with a diode-connected *n*-MOS transistor, all stages biased to work in weak inversion. A total of three $g_m$ and two $\frac{1}{g_m}$ stages were cascaded.




(a)




(b)

Figure 5.3: (a) First and (b) second stage of $g_m$-$\frac{1}{g_m}$ chain

In weak inversion the transconductance of an OTA and the resistance of a diode-connected transistors are

$$g_m = \frac{I_i}{\zeta V_T} \tag{5.1}$$

$$r = \frac{1}{g_m} = \frac{\zeta V_T}{I_i} \tag{5.2}$$

$$\tag{5.3}$$

respectively. The resulting total transconductance of $g_m$-$\frac{1}{g_m}$ chain is given by

$$A_{V,1st} = (\frac{g_{m1}}{g_{m2}})^2 \frac{V}{V} \tag{5.4}$$

$$\tag{5.5}$$

where $\zeta \sim 1.3$ is a non-ideality factor and $V_T = \frac{K_B T}{q} \simeq 26mV$ is the thermal voltage, $g_{m1}$ is the transconductance of the $g_m$ stages and $g_{m2}$ of the $\frac{1}{g_m}$ ones (Fig 5.3 (a)).

Currents $I_1$ to $I_5$ are all in the $nA$ range. To achieve better balanced DC conditions, an extra diode-connected $n$-MOS transistor is connected at the non-inverting input of the second OTA.
The last stage shown in Fig. 5.3 (b) is an asymmetrical OTA with cascoded output.

Bias currents of two different values are used ($I_1 = I_3 = I_5$ and $I_2 = I_4$) , which are generated by dividing an external current source ($I_{bias}$) using simple current mirrors. If the mirroring factors of $I_1$ and $I_2$ are respectively $x$ and $y$, the equivalent transconductance of the entire circuit for all transistors working in weak inversion is

$$G_{m,eq} \sim (\frac{xI_{bias}}{yI_{bias}})^2 xI_{bias} = \frac{x^3}{y^2} I_{bias} \tag{5.6}$$

$$\tag{5.7}$$

where the ratio $\frac{x^3}{y^2}$ is fixed. Thus $I_{bias}$ can be used to tune the time constant of the integrator. For an integrator connected in a unity gain feedback loop the time constant is

$$\tau = \frac{C}{G_{m,eq}} \sim \frac{1}{I_{bias}} \tag{5.8}$$

$$\tag{5.9}$$

Using $I_1 = 10nA$ and $I_2 = 100nA$, the transconductance of each $g_m$ and $\frac{1}{g_m}$ are respectively $g_{m1} = 106.7nS$ and $g_{m2} = 1.364\mu S$, thus

$$A_{V,1st} = (\frac{g_{m1}}{g_{m2}})^2 = 6.12 \cdot 10^{-3} \frac{V}{V} \tag{5.10}$$

while the transconductance of the second stage is $g_{m,2nd} = g_{m3} = 108nS$. The resulting equivalent transconductance and cutoff frequency are given by

$$G_{m,eq} = A_{V,1st} \cdot g_{m,2nd} = 661pS \tag{5.11}$$

$$f_L = \frac{G_{m,eq}}{2\pi C} = \frac{661pS}{2\pi \cdot 5\mu F} \tag{5.12}$$

However there are problems with this approach due to the reintroduction of offset issues. In fact, since the first stage attenuates the input signal of some hundreds factor, closing the loop in unity gain feedback, transistors are pulled out of saturation. Let's consider the situation in which the second stage needs a $1mV$ voltage difference between the inputs because of asymmetries or mismatches (which is exactly the voltage found by the simulator). Since the first stage attenuates of a factor

$$\frac{1}{A_{V,1st}} = \frac{1}{6.12 \cdot 10^{-3}} = 163.4\frac{V}{V} \tag{5.13}$$

closing the loop, at the inputs of the first stage a voltage difference of $1mV \cdot 163.4 = 163.4mV$ is generated throwing out of saturation the input transistors. This problem can be solved by introducing a compensation current at the input of the second stage, as shown in Fig. 5.4, reintroducing the same compensation terminal we were trying to suppress.

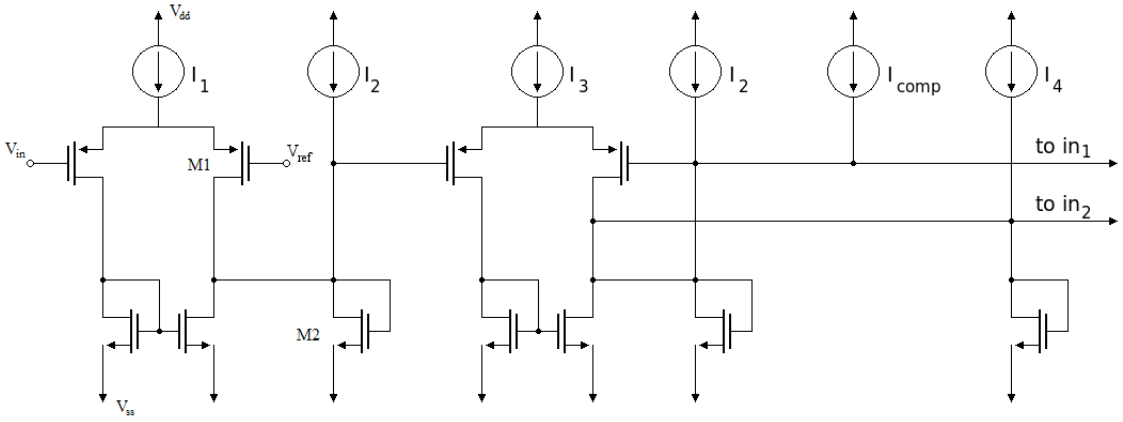



Figure 5.4: Introduction of a compensation current at one input of the second stage in order to balance offsets in the second stage

For that reason it was chosen to change architecture to realize the AC coupling block.

### 5.2.2 Current controlled AC coupling block

The AC coupling block is a high pass filter where the transconductance amplifier acts as a high resistance. Using a $5pF$ capacitance a resistance of the order of $10^{10}$

is required in order to have a low cut frequency of few $Hz$. This implies the use of an OTA biased with a very low current ($\sim pA$) to minimize $g_m$. Initially the circuit in Fig 5.5 was used, where the second load transistor has been removed because of stability issues. In fact it introduces a pole at high frequencies which may became dominant when a low bias current is used.

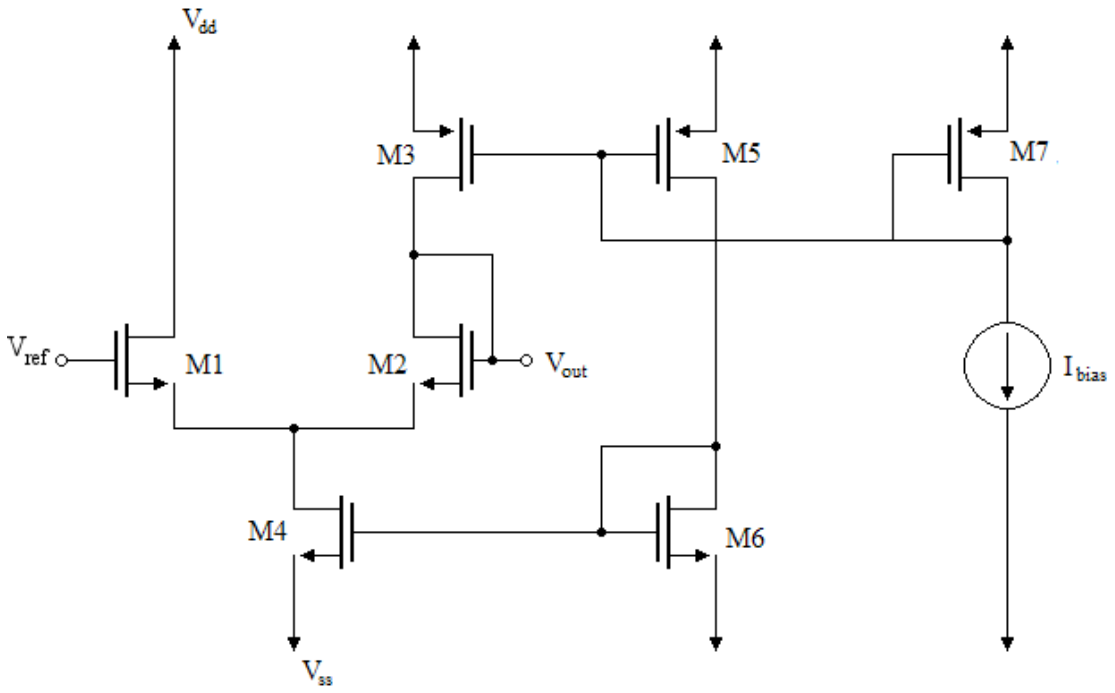



Figure 5.5: OTA used for the AC coupling block

The equivalent transconductance and the cut frequency are given by:

$$G_{meq} = \frac{g_{m1}}{2} \tag{5.14}$$

$$f_L = \frac{G_{meq}}{2\pi C} \tag{5.15}$$

Simulations have been run varying $I_{M4}$, to ensure the circuit behaves as expected. Results are reported in Table 5.1

Random offset of the AC coupling circuit was simulated too resulting in $\sim 45mV_{pp}$ (Fig. 5.6).

A simulation of the entire channel with AC coupling current controlled circuit was performed and the gain of each block was calculated (Table 5.2). It highlighted the presence of an important attenuation after the AC coupling blocks preceding the filters, causing a total gain of about $1469V/V$ instead of $2400V/V$.

This problem is due to the fact that the AC coupling circuit, having a high output impedance, is unable to pilot small loads. Since the input capacitance of the filter stage using input transistors with dimensions $\frac{W}{L} = 400/4$ is about $c_{gs} = 969fF$, while the buffer one is $54.82fF$, this attenuation phenomenon is much more evedent

| $I_{M4}$ | $g_m$ | $f_L$ |
|---|---|---|
| $2nA$ | $29.05nS$ | $925Hz$ |
| $200pA$ | $3.137nS$ | $50Hz$ |
| $100pA$ | $1.669nS$ | $25Hz$ |
| $50pA$ | $814.1pS$ | $12.5Hz$ |
| $20pA$ | $340.4pS$ | $4.3Hz$ |
| $2pA$ | $70.18pS$ | $941mHz$ |

Table 5.1: Low cut frequency dependence on bias current

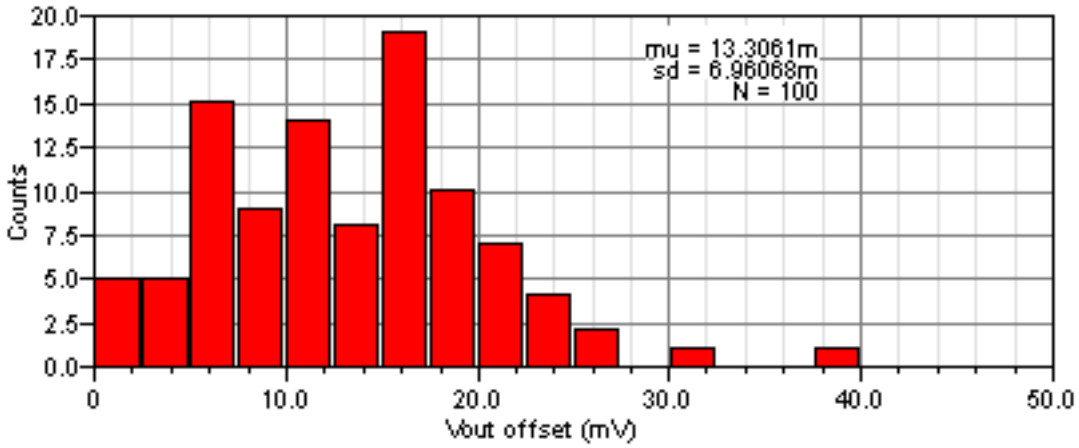



Figure 5.6: Monte Carlo random offset simulation of the AC coupling block

| Block output | gain (V/V) |
|---|---|
| Preamplifier | 96.28 |
| First AC coupling block | 0.79 |
| First filter | 4.99 |
| Second AC coupling block | 0.79 |
| Second filter | 4.99 |
| Third AC coupling block | 0.98 |
| Buffer | 1 |

Table 5.2: Gain of each stage of the channel using the current controlled AC coupling circuit

when the output of the AC coupling block is connected to the filter input. The foregone solution is to reduce the dimensions of the input transistors of the filter in order of decreasing the value of the gate capacitances and than increasing their impedance. In Table 5.3 is shown the dependence of the gain on these transistors dimensions.

| $W/L$ ($\mu m/\mu m$) | AC coupling block gain ($V/V$) | Total output gain ($V/V$) |
|---|---|---|
| 400/4 | 0.79 | 1469 |
| 100/4 | 0.93 | 2025 |
| 50/4 | 0.96 | 2148 |
| 50/2 | 0.97 | 2205 |

Table 5.3: Dependence of the gain on filter input transistors dimensions

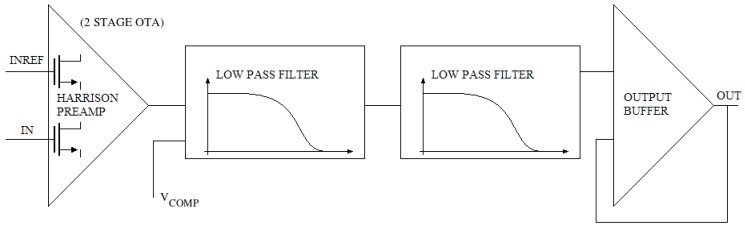
Finally it was decided to use $\frac{W}{L} = \frac{50\mu m}{2\mu m}$ since the filter is slightly more sensible to offsets, while the gain is maximized.

The main problem of this architecture lies in the difficulty of generating a current of few $pA$ to bias the OTA. Since we can arrive with generators to some tens $nA$, a mirroring factor of some thousand is needed, implying the use of a large silicon area to realize the diode-connected transistor of the mirror.

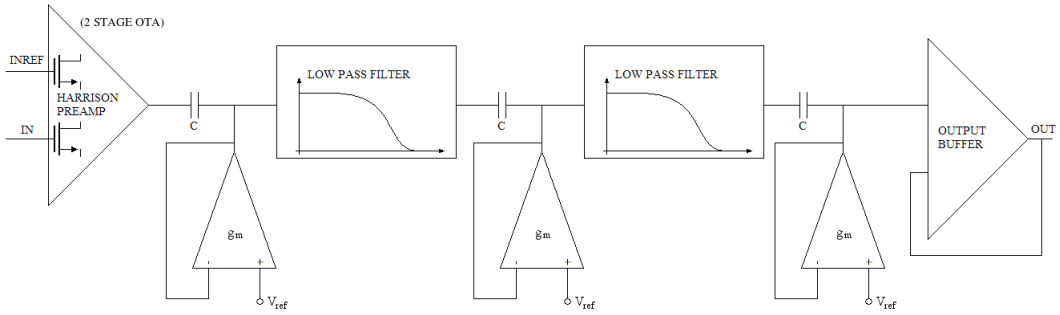
# Chapter 6

# Complete chip layout

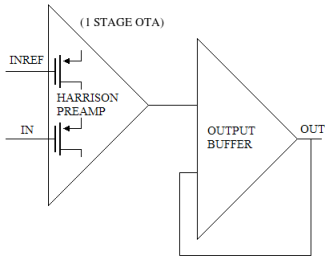
In this chapter results of post layout simulations are exposed together with the main features of the chip.




(a)




(b)




(c)

The chip is nearly square and has an area of $4.32mm^2$. It contains three channels.

Two of them use the Harrison preamplifier with two stage low noise *n*-type OTA examined in chapter 4, the first (Fig. 6.1 (a), 6.2 (1)) uses a voltage compensation terminal at the input of the first filter, the second (Fig. 6.1 (b), 6.2 (2)) has different blocks coupled with the AC coupling circuit studied in chapter 5. The third channel (Fig. 6.1 (c), 6.2 (3)) contains only a standard single stage *p*-type preamplifier directly coupled with the output buffer and is supposed to be a point of reference for the testing of the first two channels.

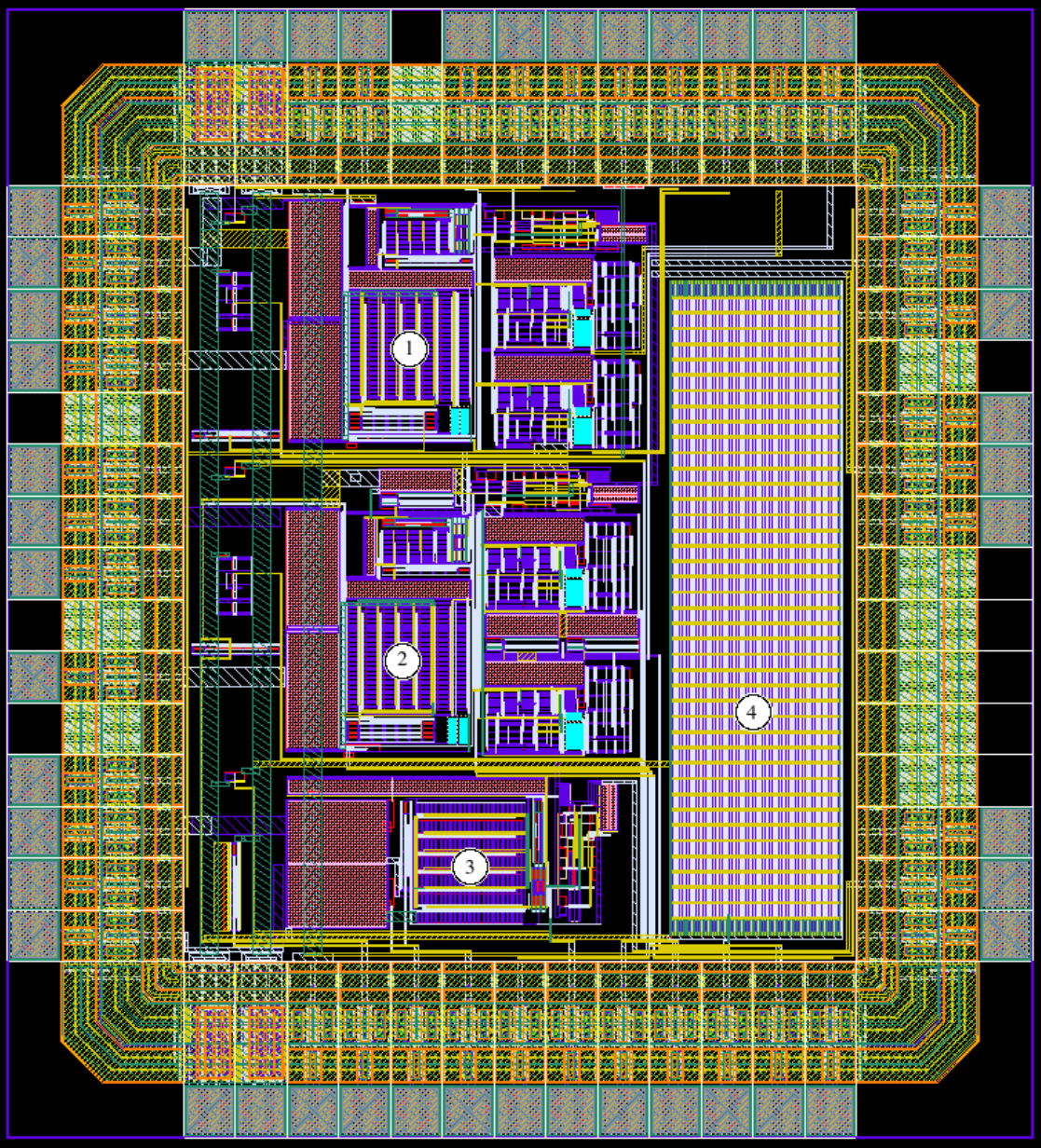



Figure 6.2: Complete chip layout. (1, 2, 3) Each channel is enlarged in Fig. from 6.3 to 6.7. (4) AC coupling circuit current mirror

## 6.1 External offset compensation voltage channel layout

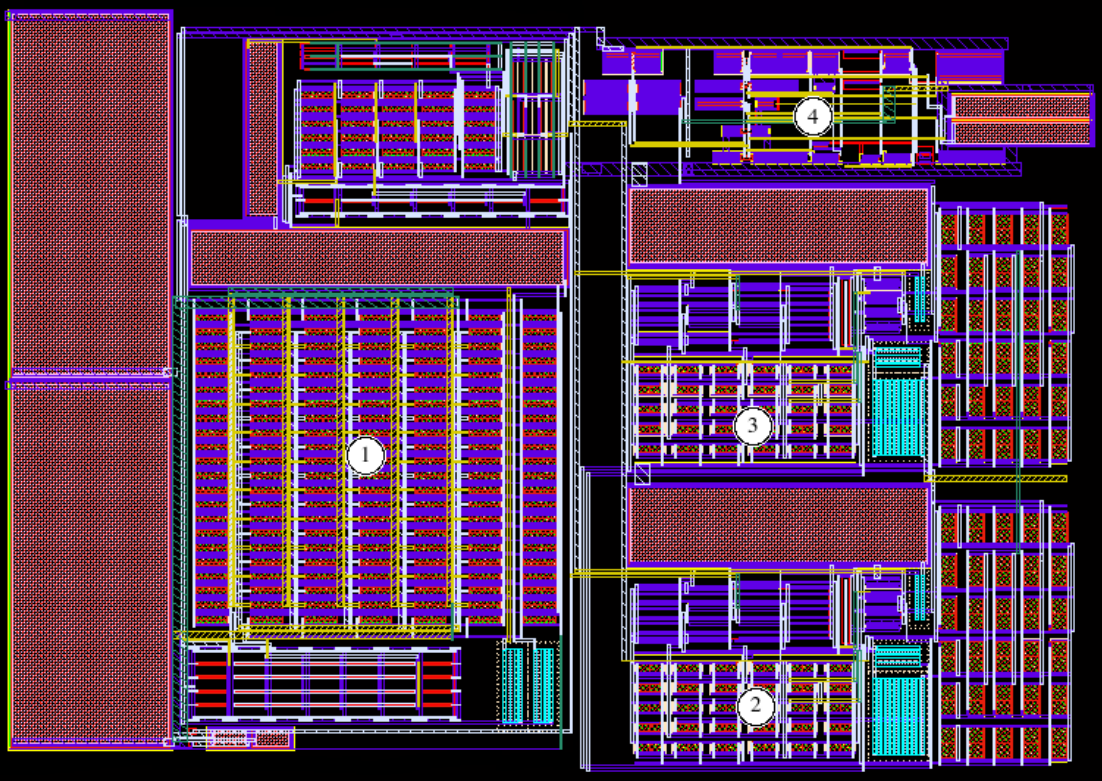



Figure 6.3: Layout of the channel using external voltage offset compensation. (1) Harrison preamplifier using two stage OTA, (2) first filter, (3) second filter and (4) output buffer

For the first two channels worst cases simulations and temperature analysis have been performed, in order to ensure the absence of parasitics effects. In the following tables and graphics results are reported.

**Worst cases simulations**

| case | $f_L(mHz)$ | $f_H(kHz)$ | $A_V(dB)$ | $V_{irn}(\mu V_{rms})$ |
|---|---|---|---|---|
| typical mean | 768.7 | 8.654 | 67.58 | 1.686 |
| worst power | 864.2 | 11.8 | 67.58 | 2.516 |
| worst speed | 690.3 | 6.192 | 67.58 | 1.643 |

Table 6.1: Worst cases analysis results on first channel layout

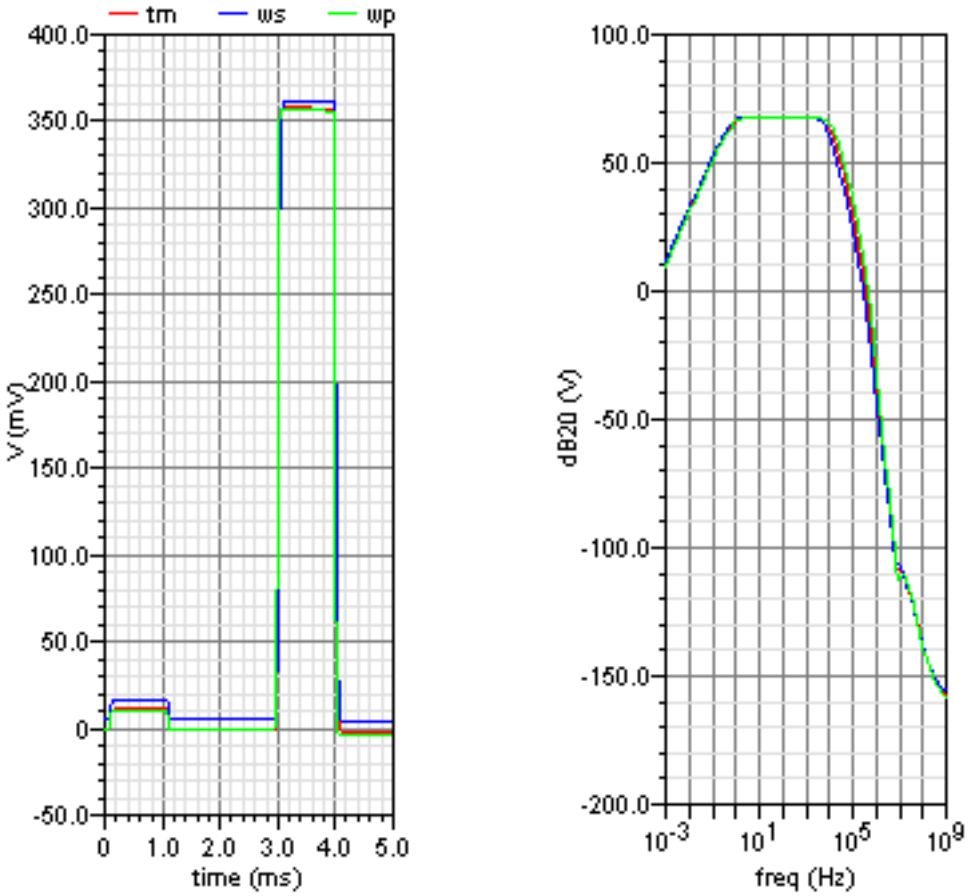



Figure 6.4: Transient and AC response in worst cases of the first channel layout

**temperature analysis**

| Temperature | $f_L$ | $f_H$ |
|---|---|---|
| $-25°C$ | $765.9mHz$ | $11.88kHz$ |
| $0°C$ | $766.0mHz$ | $10.12kHz$ |
| $25°C$ | $768.0mHz$ | $8.75kHz$ |
| $50°C$ | $841.7mHz$ | $7.66kHz$ |
| $100°C$ | $31.96Hz$ | $7.66kHz$ |

Table 6.2: Results of temperature analysis on first channel layout

## 6.2 AC coupled channel

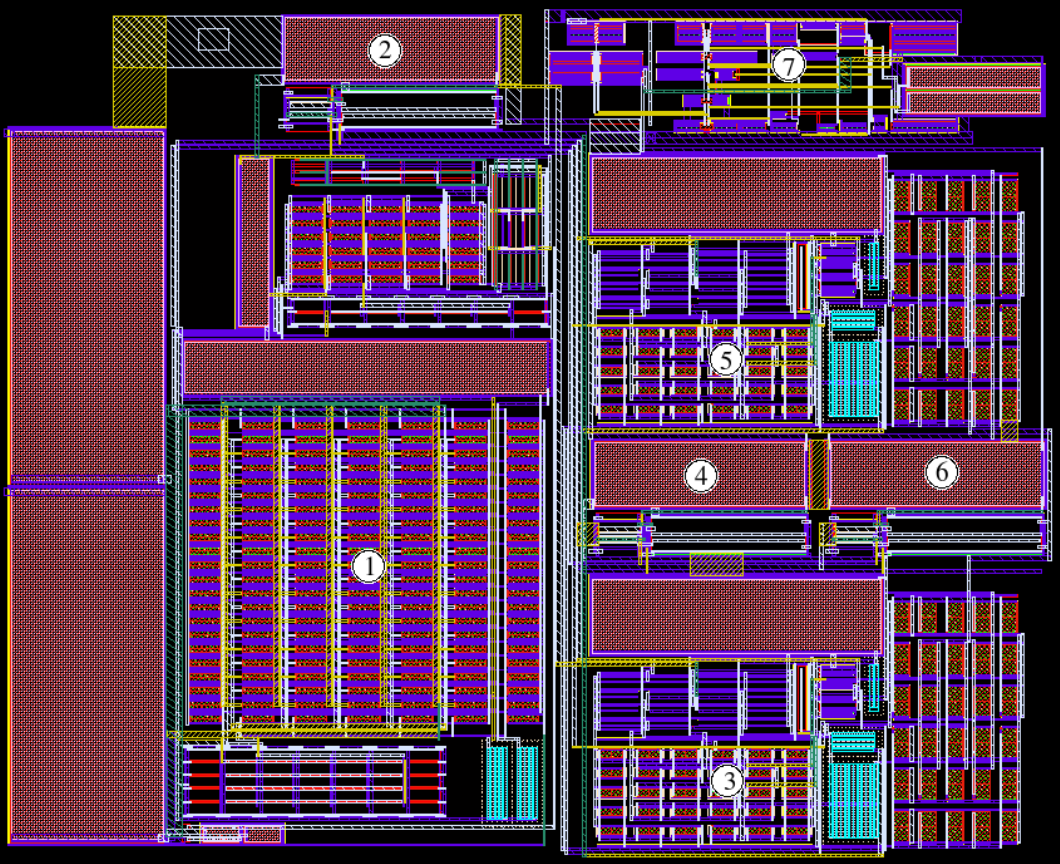



Figure 6.5: Layout of the channel using AC coupling circuits. (1) Harrison preamplifier using two stage OTA, (2) first AC coupling block, (3) first filter, (4) second AC coupling block, (5) second filter, (6) third AC coupling block and (7) output buffer

### Worst cases simulations

| case | $f_L(Hz)$ | $f_H(kHz)$ | $A_V(dB)$ | $V_{irn}(\mu V_{rms})$ |
|---|---|---|---|---|
| typical mean | 2.419 | 8.814 | 66.14 | 1.721 |
| worst power | 3.168 | 12.04 | 66.14 | 1.855 |
| worst speed | 1.938 | 6.302 | 66.18 | 1.567 |

Table 6.3: Worst cases analysis results on second channel layout

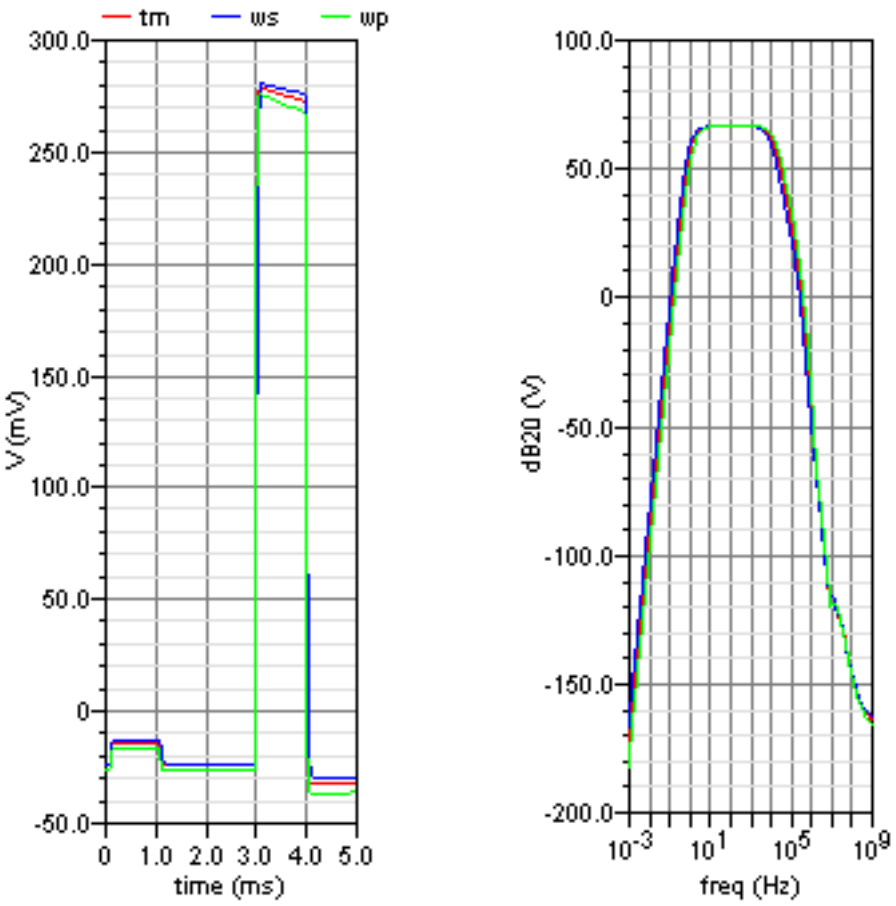



Figure 6.6: Transient and AC response in worst cases of the second channel layout

**temperature analysis**

| Temperature | $f_L(Hz)$ | $f_H(kHz)$ |
|---|---|---|
| $-25°C$ | 2.513 | 12.08 |
| $0°C$ | 2.465 | 10.30 |
| $25°C$ | 2.422 | 8.91 |
| $50°C$ | 2.420 | 7.80 |
| $100°C$ | 32.26 | 6.21 |

Table 6.4: Results of temperature analysis on second channel layout

## 6.3 Standard preamplifier OTA architecture

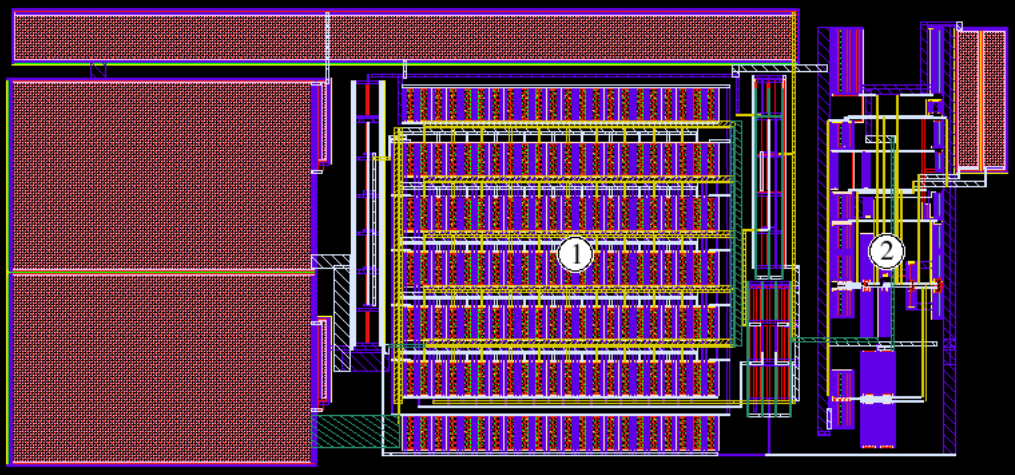



Figure 6.7: Layout of channel using standard preamplifier configuration. (1) Harrison preamplifier using single stage OTA with $p$-MOS inputs and (2) output buffer

## 6.4 Complete chip layout simulations

### Interconnections noise

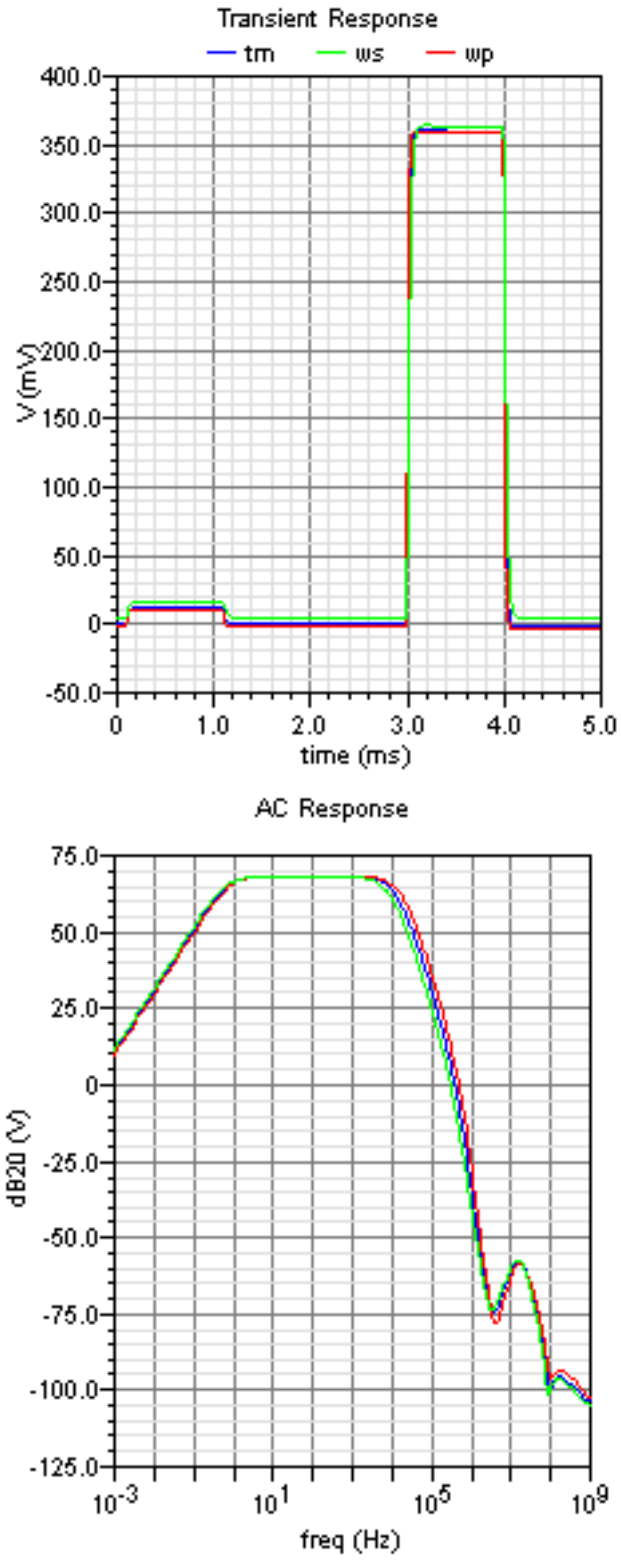
Note that the simulator doesn't take into account the thermal noise of the interconnections. Their resistance at the inputs of channels have been estimated of nearly $100\Omega$ which gives a negligible contribution ($\sim 10nV_{rms}$) to total channel input referred noise.
By the way, the thermal noise of a $100\Omega$ resitance is expected to be

$$N_{rms} = \sqrt{4K_BTR\Delta f} = \sqrt{4 \cdot 1.68 \cdot 10^{-23}\frac{J}{K} \cdot 300K \cdot 100\Omega \cdot 8.6 \cdot 10^3 Hz} \simeq 130nV_{rms} \tag{6.1}$$

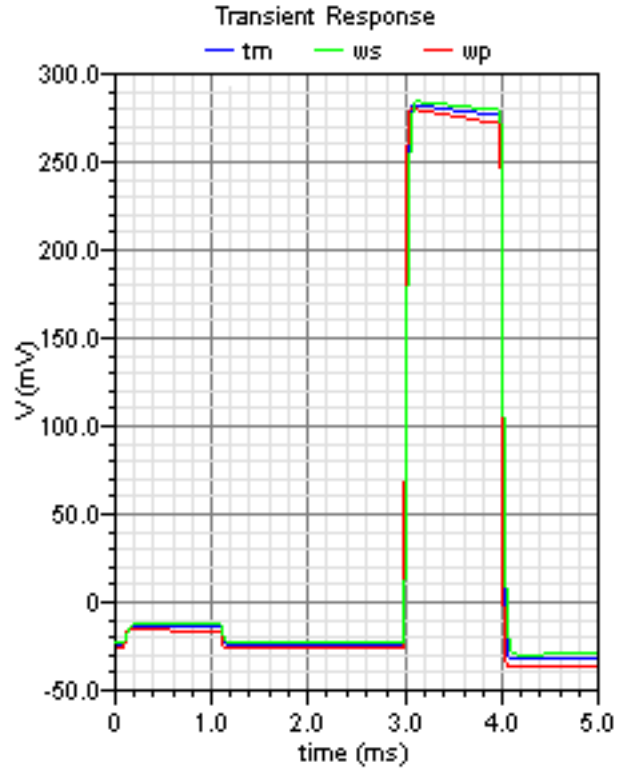
which is one order lower than the total noise of the circuit.

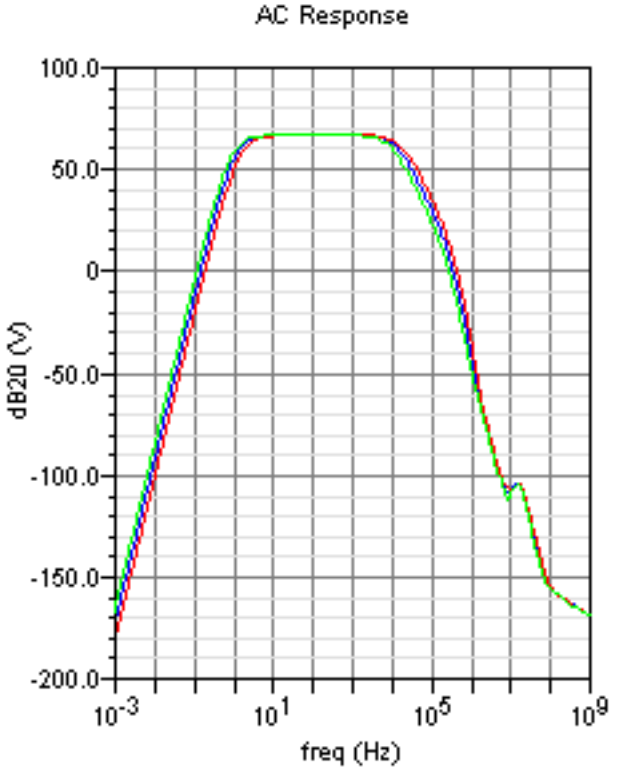
### Worst cases simulations

As a final confirm of the right functioning of the circuits, worsts cases simulations of the entire chip have been performed and results for each channel are shown in the following graphs. Note that for the inputs and outputs, as well as for the biases, pins with only diode ESD protection have been used. Moreover input and output pins are surrounded by ground pins in order to shield them.

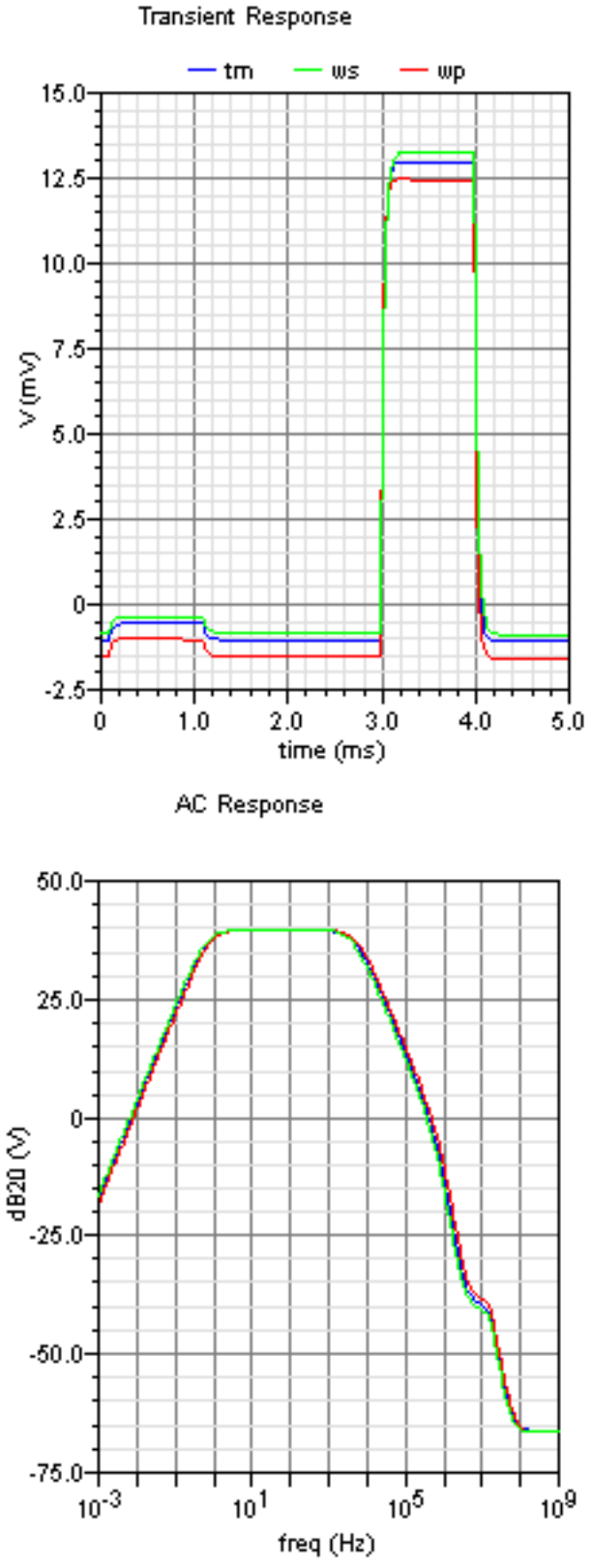

Transient Response
tm
ws
wp
400.0
350.0
300.0
250.0
200.0
150.0
100.0
50.0
0
-50.0
V (mV)
0
1.0
2.0
3.0
4.0
5.0
time (ms)
AC Response
75.0
50.0
25.0
0
-25.0
-50.0
-75.0
-100.0
-125.0
dB20 (V)
10-3
101
105
109
freq (Hz)

(a)


Transient Response
tm
ws
wp
300.0
250.0
200.0
150.0
100.0
50.0
0
-50.0
V (mV)
0
1.0
2.0
3.0
4.0
5.0
time (ms)


AC Response
100.0
50.0
0
-50.0
-100.0
-150.0
-200.0
dB20 (V)
10-3
101
105
109
freq (Hz)

(b)




(c)

Figure 6.8: Worst cases simulations of the complete chip layout. Transient and AC responses of (a) the channel using external compensation voltage, (b) the AC coupled one and (c) of standard preamplifier

# Chapter 7

# Conclusions and future work

The aim of this work was to do a study and design the layout of an Analog Front End for neural signal recording systems based on diamond microelectrode arrays in 0.35 $\mu m$ CMOS.
The diamond is a new electrode material. Its surface becomes conductive through the hydrogenation process, and it shows many interesting properties; the most important are tunable surface conductivity, biocompatibility and optical transparency. Being the noise level of the diamond microelectrodes is lower than the metal ones, low noise of electronic amplifying chain becomes an important aim.
CMOS AMS 0.35$\mu m$ technology has been chosen to comply with noise requirements and small area occupation.
Starting from a complete processing channel for neural signal recording and simulating the first layout version, improvements in noise level,area occupation and signal distortion have been made.

Each channel is composed by three stages:

- Preamplifier, with differential input and single ended output. It has a gain of 100 with pass band behavior with few $Hz$ low cut frequency. To achieve this very low cut off frequency with integrated component a mos-bipolar pseudoresistance is exploited($\approx 10^{12}\Omega$).
  Particular attention is given in the design of the OTA to minimize the noise and the power consumption ($59.4\mu W$).

- Filter Stage, composed by two OP-AMP filter designed with $g_m/C$ technique. It has a gain of 25 with a high cut off frequency tunable in the range $\approx 3kHz$ and $\approx 13kHz$. Since the offset is a critical factor in this stage it has been provided with two different techniques of offset control.

- Output Buffer, in a standard configuration in class AB with two stage and Miller compensation.

The supply voltage is selectable among 0-3.3$V$ or $-1.65$-1.65$V$, in the first case the output load resistance can be 50$\Omega$, in the second case of 1$M\Omega$.
The complete circuit has a bandpass between 380$mHz$-2$Hz$ and 8$kHz$ with a gain of $\approx 2400$.

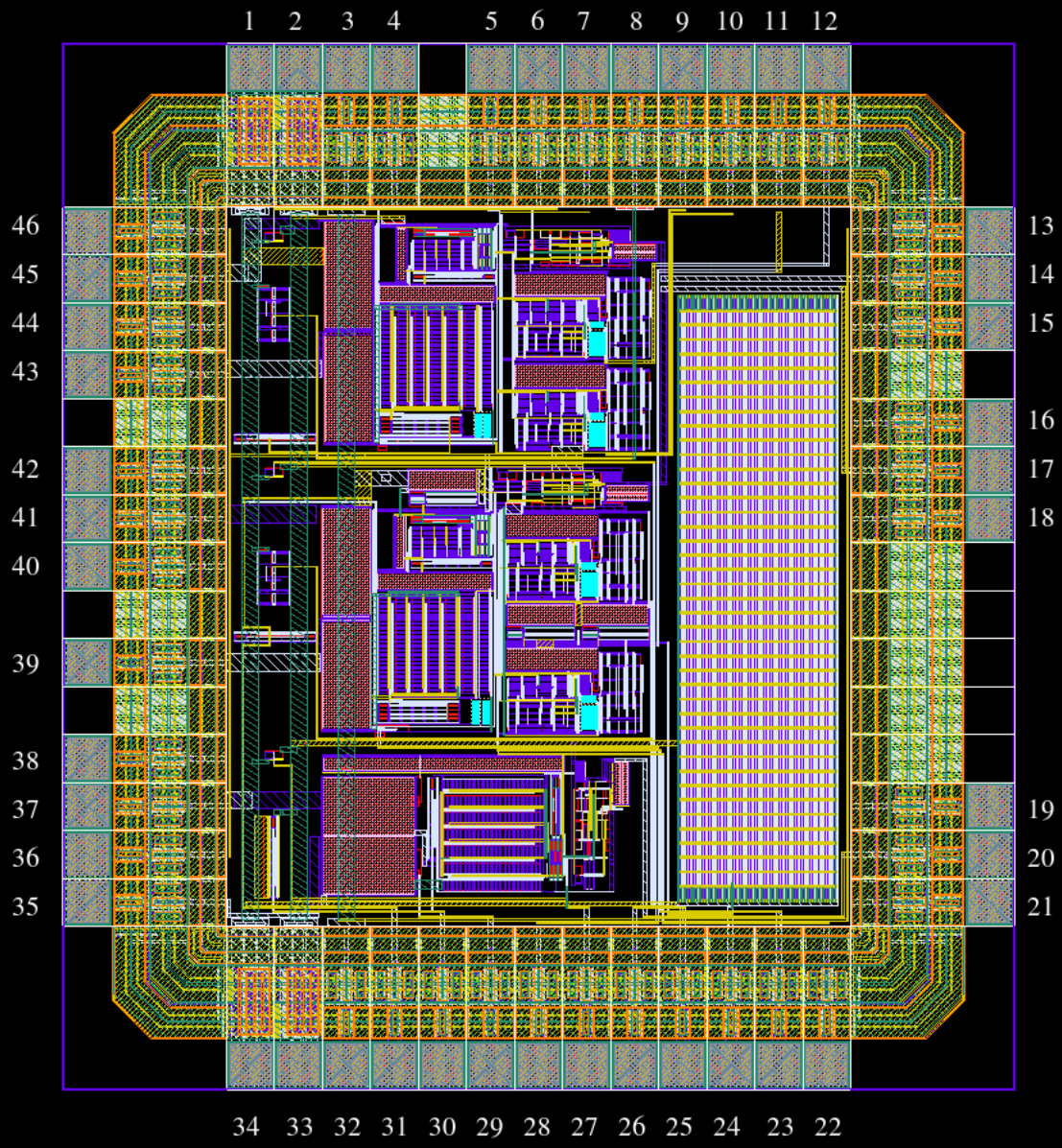
Three different channels have been designed. Two of them use a preamplifier's two stage OTA characterized by very low noise ($V_{irn} = 1.67\mu V_{rms}$). The difference

between them lies in the offset compensation method. First channel uses an external compensation tension on the input of the first filter, while the second has each block AC coupled with the following.
The AC coupling circuit is $g_m - C$ filter using very long time constant OTA.
Finally, third channel is composed only by a preamplifier using a standard single stage symmetrical OTA with $p$-MOS inputs, followed by the output buffer.

Next step of this work is to test the chip which has already been sent in foundry. First of all it is necessary to study a testing experimental setup and, more critical aim, a way to reproduce signals of the same type of the ones coming from micro-electrode arrays (with an amplitude of 10-150$\mu V$ in a frequency band going from few $Hz$ to some $kHz$)

# Appendix A

# Chip data sheet



| pin number | pin name | pin function | tension value (referred to ground) | |
|---|---|---|---|---|
| 1, 34 | $V_{ss}$ | Negative supply | $0V$ | $-1.65V$ |
| 2, 33 | $V_{dd}$ | Positive supply | $3.3V$ | $1.65V$ |
| 3, 13, 15, 16, 18, 19, 21, 32, 36, 38, 40, 42, 44, 46 | gnd | Ground supply. Lines 36, 38, 40, 42, 44, 46 shield the inputs lines, lines 13, 15, 16, 18, 19, 21 the output lines. | $0V$ | |
| 4<br>30<br>31 | bias_OTA_VC[1]<br>bias_OTA_1P[3]<br>bias_OTA_AC[2] | Preamplifier bias. In simulations 5 $\mu A$ in the weak side of the mirror have been used (which means 20$\mu A$ in the first stage and 5$\mu A$ in the second, or 5$\mu A$ in the single stage OTA) | – | |
| 5<br>23 | Vcas_VC<br>Vcas_AC | Cascode tension of filter's OTA | $2V$ | $350mV$ |
| 6<br>25<br>27 | ibias_OTA_VC<br>ibias_OTA_AC<br>ibias_OTA_1P | Buffer bias. In simulations 5 $\mu A$ in the weak side of the mirror (thus 5$\mu A$ in the buffer OTA) have been used | – | |

[1] "VC" refers to the first channel, the one using external offset compensation tension on the first filter input

[2] "AC" refers to the second channel, the AC coupled one

[3] "1P" refers to the third channel, the one with preamplifier in standard configuration

| pin number | pin name | pin function | tension value (referred to ground) | |
|---|---|---|---|---|
| 7<br>22 | Vgatebias_VC<br>Vgatebias_AC | Gate control tension through which high cut frequency of filters is tuned | $2.95V$ | $1.3V$ |
| 8<br>26 | Ibias_VC<br>Ibias_AC | Filter bias. In simulations 5 $\mu A$ in the weak side of the mirror (thus $5\mu A$ in each filter OTA) have been used | – | |
| 9<br>28<br>29 | Vref_OTA_VC<br>Vref_OTA_AC<br>Vref_OTA_1P | Preamplifier feedback tension reference | $1.65V$ | $0V$ |
| 10 | Vcomp | External offset control tension for first channel | $1.65V$ | $0V$ |
| 11<br>12 | Vref_filter_AC<br>Vref_filter_VC | Filter OTAs reference tension | $1.65V$ | $0V$ |
| 14<br>17<br>20 | Vout_VC<br>Vout_AC<br>Vout_1P | Channels outputs | – | |
| 24 | ACbias | AC coupling blocks bias. In simulations 2 $nA$ in the weak side of the mirror (thus $2pA$ in each block OTA) have been used | – | |
| 35<br>39<br>43 | Vref_1P<br>Vref_AC<br>Vref_VC | Channels reference input tensions | $1.65V$ | $0V$ |
| 37<br>41<br>45 | Vin_1P<br>Vin_AC<br>Vin_VC | Channels inputs | – | |

# Bibliography


[1] Thanushan Kugathasan. *Integrated front end electronics for cellular signal recording system based on diamond microelectrode arrays*. PhD. Thesis 2007.

[2] David A. Borkholder. *Cell based biosensors using microelectrodes*. PhD. Thesis 1998.

[3] Emanuele Bottino, Sergio Martinoia, Maurizio Valle. *Integrated low noise low power interface for neural bio–potentials recording and conditioning*. In Proc. European Symposium on Artificial Neural Network (ESANN '04), pp. 513–518, Apr 2004.

[4] Reid R. Harrison, Cameron Charles. *A low–power low–noise CMOS amplifier for neural recording applications*. IEEE Journal of Solid-State Circuits, vol. 38, no. 6, pp. 958-965, June 2003.

[5] Emanuele Bottino, Maurizio Valle. *Integrated low noise preamplifier for biologic-electronics interfaces*. In Proc. European Conference on Circuit Theory and Design (ECCTD), 2005.

[6] Behzad Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, 1999.

[7] Reid R. Harrison, Paul T. Watkins, Ryan J.Kier, Robert O. Lovejoy, Daniel J. Black, B. G. Grager, Florian Solzbacher. *A low power integrated circuit for a wireless 100-electrode neural recording system*. IEEE Journal of Solid-State Circuits, vol. 42, no. 1, pp. 123-133, January 1997.

[8] Robert Reiger, Andreas Demosthenous, John Taylor. *Continuosly tunable, very long time constant CMOS Integrator for a neural recording implant*. IEEE International Solid-State Circuits Conference, 2003, pp. 441-444, September 2003.