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Tesi di laurea

Analysis and Design of a Fast Binary Front-End Chip for the COMPASS Experiment at CERN

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Contents

Preface

The topic of this thesis is the design of the final version of the integrated circuit CMAD developed for the COMPASS experiment at CERN.

The project has been carried out at the VLSI Laboratory of the INFN of Turin.

As a first step, the limitations of an existing prototype of the circuit have been identified in order to improve the circuit performance especially from the counting rate point of view.

In fact a higher counting rate is one of the major requirements for the new front-end circuit and the improvement of the counting rate capability is a demanding specification.

Thus to obtain an understanding of the factors affecting the circuit response, a thorough study of the existing architecture has been carried out and an accurate mathematical model has been analytically derived.

The blocks critical for the circuit performance have been pointed out and a new design of these blocks has been achieved.

In particular the BLH (baseline holder) block has been modelled and redesigned and the design and the optimisation of the whole analog chain consisting of the preamplifier, the pulse shaper and the BLH (buffer + transconductor block) have been accomplished.

An outline of each chapter will be presented now in order to give a general idea of the thesis structure and the specific topics covered throughout this work.

Chapter 1 contains an overview of the COMPASS experiment for which the front-end chip is designed. A brief description of the COMPASS spectrometer behavior as well as the RICH particle detectors is given. The basics of Cherenkov effect, the fundamental principle that the RICH detectors are founded on, are also covered. The general behavior of the PMTs is presented. Finally a comparison between the main features and performance of the new front-end

circuit and those of the old one is performed.

Chapter 2 deals with the general characteristics of front-end circuits. The main purpose of this chapter is to give an insight into the architecture and the behavior of the stages making up a detector readout system, namely a CSA and a pulse shaper. Thus, the analysis performed is fairly qualitative and it is founded on a set of general relationships allowing an approximate understanding of the circuit behavior.

Chapter 3 contains a detailed analysis of the first two stages of our detector readout system. The models used for representing the main characteristics of each of the circuit building blocks are presented. The small-signal transfer function as well as the input and output impedance of each stage are analytically derived in the frequency domain and described. The time-domain pulse response of each stage is also given graphically and discussed. Moreover, a lot of other graphical outputs are presented in order to check the accuracy of the results obtained through our models.

Chapter 4 deals with the modelling and analysis of the slew-rate limited non-linear buffer making up (together with a transconductor block) the BLH (baseline holder). The BLH is a particularly important block because it provides the circuit output baseline stabilisation both at low frequency and at a high counting rate. Furthermore all the computer simulations performed to set important design parameters are given.

Chapter 5 is concerned with the design of the non-linear buffer modelled in chapter 4. Several SPICE simulations of the actual circuit are performed in order to check it works properly especially when processing large and fast signals. A detailed analysis of the large-signal buffer basic circuit is carried out to identify circuit limitations and drawbacks. An alternative circuit for solving these problems is presented and analysed.

Chapter 6 deals with the single-pulse characterisation and the actual-circuit response to various sequences of pulses to show the efficient baseline stabilisation occurring for fast and large signals and performed by the new BLH block. The performance of a circuit version producing narrower output pulses and thus able to provide a higher counting rate is discussed.

Finally, we add that all the calculations presented throughout this thesis have been performed by using *Mathematica*, a general computer software system and language. In fact, although SPICE simulations could be performed to obtain the same numerical results, *Mathematica*'s symbolic computation capabilities allowed us to obtain symbolic relationships which proved to be very useful in understanding the circuit behavior. In fact the circuits considered are simple enough to allow an analytical approach.

Chapter 1

Introduction

The topics covered in this thesis concern the front-end electronics of particle detectors. The purpose of such a detector is the acquisition of data allowing us to collect information about the energies and trajectories of subatomic particles.

In particular, the circuit studied throughout the thesis will be used for a specific high-energy physics experiment called COMPASS (Common Muon Proton Apparatus for Structure and Spectroscopy) taking place at CERN in Geneva.

1.1 The COMPASS Experiment

The COMPASS experiment is a fixed target experiment at the CERN Super Proton Synchrotron (SPS). The purpose of this experiment is the study of hadron structure and spectroscopy with high intensity muon and hadron beams.

The physics programme includes measurements of semi-inclusive and inclusive polarized deep inelastic scattering, charm production, search for exotics in high quark spectroscopy and Primakov reactions. One of the main goals of the experiment is the measurement of the contribution of the gluon spins to the angular momentum of the nucleon.

The COMPASS experiment was constructed in 1998-2000 and was commissioned during a technical run in 2001. The experiment set-up is made up of two spectrometers, a large-angle spectrometer followed by a small-angle spectrometer both provided with a gas RICH detector (RICH-1 and RICH-2) for hadron identification. A three-dimensional view of the COMPASS spectrometer is shown in Fig. 1.1.

The first physics run took place in 2002 and continued until the end of 2004.

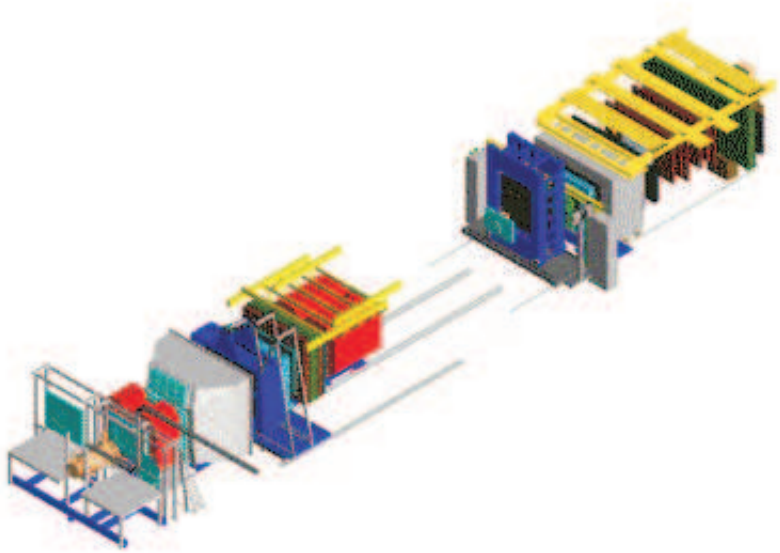


Figure 1.1: Three-dimensional view of the COMPASS spectrometer at CERN.

After a year shutdown in 2005, data taking should continue in 2006. Nearly 240 physicists from 12 countries and 28 institutions are working on COMPASS.

One of the main new features of COMPASS with respect to previous experiments is its powerful data acquisition. The read-out architecture is based on custom electronics and operated with a 40 MHz clock. A trigger rate of 5 kHz was used for the muon experiments but the real DAQ capabilities will be exploited by the hadron beam experiments, even if the full rate of 50-100 kHz can be only used with a very efficient event reduction.

The total amount of data recorded in 2002 is very large and amounts to 9 billion events or 260 TByte.

1.1.1 The COMPASS Spectrometer

To obtain a general understanding of the concept and performance of the COMPASS spectrometer, which is at the heart of the COMPASS experiment, we will give a brief description of its behavior.

A schematic view of the COMPASS spectrometer is shown in Fig. 1.2. The spectrometer is made up of two stages, the large-angle spectrometer (LAS) covering an

aperture of ±180 mrad and the small-angle spectrometer (SAS) detecting particles within the inner ±30 mrad.

Both sections comprise tracking and particle identification detectors grouped around the spectrometer dipole magnets SM1 and SM2 which provide field integrals of 1 and 4.4 Tm. Tracking in the beam region is provided by scintillating fibre and silicon detectors and in the intermediate region by MicroMeGas (Micro Mesh Gaseous structure) and Gem (Gaseous Electron Multiplier) detectors. Large area outer tracking is covered by drift chambers, multi-wire proportional chambers and straw tubes. Both LAS and SAS comprise a hadron calorimeter.

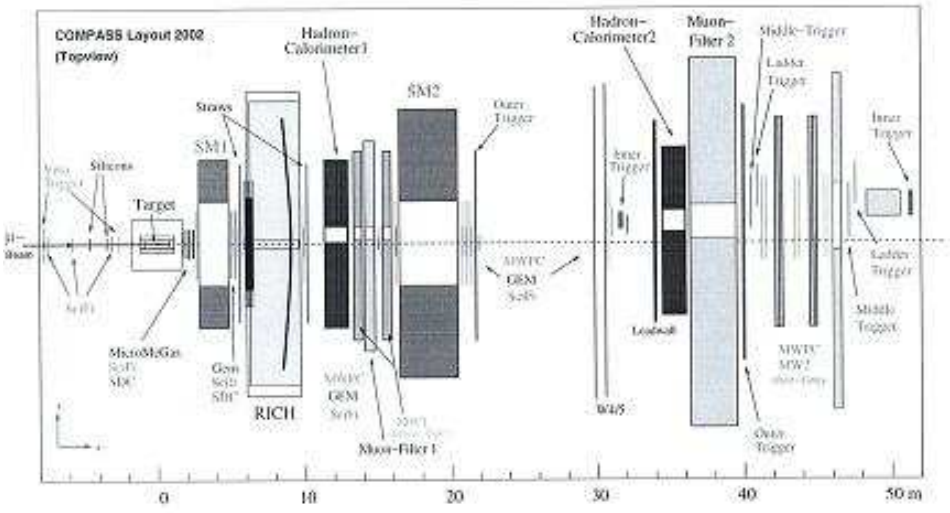


Figure 1.2: Top view of the COMPASS spectrometer in 2002.

The muon beam has a large momentum spread and a considerable size and hence a measurement of each single incoming particle is essential. The momentum is measured by four scintillator hodoscopes. Upstream of the target the beam particle trajectory is determined by a scintillating fibre hodoscope consisting of seven layers of fibres and read out by multi-anode photomultiplier tubes. The association of track and momentum is based on the time correlation.

The polarised target system consists of a superconducting target solenoid providing a field of 2.5 T and an additional dipole which can provide a transverse magnetic field. The incoming muon beam traverses two 60 cm long target cells containing oppositely longitudinally polarised deuterons.

Finally it should be pointed out that the central apparatus for particle identification is the RICH-1 in the LAS. Before giving some additional information about the RICH-1, it is useful to recall that a RICH (Ring Imaging CHerenkov) detector is a particle detector that can determine the velocity v of a particle by an indirect measurement of the Cherenkov angle θ_c, namely the angle between the emitted Cherenkov radiation and the particle path (a more detailed explanation of Cherenkov radiation will be given later).

In a RICH detector a cone of Cherenkov light is produced when a high speed particle traverses a suitable medium, often called radiator, with a velocity greater than the speed of light in that medium.

This light cone is detected on a position sensitive planar photon detector, which allows reconstructing a ring or disc, whose radius is a measure for the Cherenkov emission angle.

Both focusing and proximity-focusing detectors are in use. In a focusing RICH detector the photons are collected by a spherical mirror with focal length f and focused onto the photon detector placed at the focal plane. The result is a circle with a radius $r = f\,\theta_c$, independent of the emission point along the particle track. This scheme is suitable for low refractive index radiators, i.e. gases, due to the larger radiator length needed to create enough photons.

In the more compact proximity-focusing design a thin radiator volume emits a cone of Cherenkov light which traverses a small distance – the proximity gap – and is detected on the photon detector plane. The image is a ring of light whose radius is defined by the Cherenkov emission angle and the proximity gap. The ring thickness is determined by the thickness of the radiator.

1.1.2 The COMPASS RICH Detectors

As mentioned previously the COMPASS spectrometer used in the muon program is a two stage spectrometer.

Hadrons produced in DIS (Deep Inelastic Scattering) are detected in the first stage and scattered muons in the second stage.

Two RICH detectors termed RICH-1 and RICH-2 are at the heart of the two stages respectively.

The RICH-1 is the fundamental tool for particle identification. Thus we will try to summarise the most important technical aspects characterising its behavior.

The fundamental requirements for RICH-1 design related to the general design of the experiment are:

- the capability to separate π and K with momenta up to $\sim 60\,\mathrm{GeV}/c$ in a high-intensity environment
- the full acceptance of the LAS (horizontal: $\pm 250\,\mathrm{mrad}$; vertical: $\pm 200\,\mathrm{mrad}$)
- the minimisation of the total amount of material, to preserve the tracking resolution of the SAS as well as the energy resolution of the downstream electromagnetic and hadronic calorimeters
- the capability to register and handle high data fluxes.

An artistic view of COMPASS RICH-1 is shown in Fig. 1.3 which displays the position of some important detector components such as the mirror wall and the photon detector and also allows us to realise the real size of the whole device.

From a qualitative point of view the RICH 1 is a gas RICH with a 3 meter-long C_4F_{10} radiator at atmospheric pressure, mantained at the temperature of 25°C.

The mirror set-up consists of spherical mirrors having a radius of 6.6 m and segmented in 120 hexagonal pieces covering a total area greater than $20\,\mathrm{m}^2$ forming two spherical surfaces with different centres of curvature.

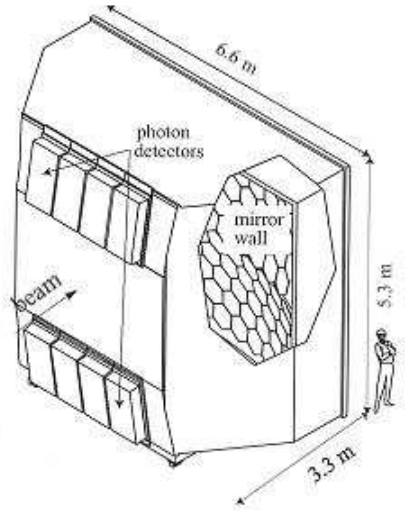


Figure 1.3: Artistic view of COMPASS RICH-1.

This solution allows the focalisation of the Cherenkov photons onto two sets of photon detectors placed above and below the acceptance region.

The photon detectors are equipped with CsI photocathodes for a total active surface of $5.3\,\mathrm{m}^2$.

The pixel segmentation of the photocathodes (pixel size: $8 \times 8\,\mathrm{mm}^2$) results in approximately 80 000 channels equipped with analog read-out electronics.

In addition to the information stated above on the main design parameters, we can add that the gas radiator must be as pure as possible in order to limit the

contamination from impurity able to absorb UV photons. The goal is water vapour and oxygen traces smaller than 5ppm.

For the vessel, leakages $< 10^{-2}$ mbar l/s as well as nonpolluting materials are required. Moreover the vessel must be thermalised to reduce the refractive index dispersion and designed to be the support for the mirror wall as well as the photon detector.

Thus, the gas purity, the rigidity and the stability required to guarantee the relative alignement of mirrors and photon detector have been important design criteria.

For the mirrors the main requests concern good performance in the UV region, surface shape and amount of material. In practice a good reflectance in the far UV region is obtained by using a reflective coating of Al (80 nm) protected by a layer of MgF_2 (30 nm).

The local deviation from the spherical shape must not exceed 0.2 mrad and the radius deviation from its nominal value must be in the order of 0.5 % for each single mirror.

The RICH-2 installed in the second stage is used for particle identification in the high energy region, namely up to 120 GeV.

The structure of RICH-2 is similar to RICH-1. The thickness of the radiator gas is 8 m. The radiator gas is a mixture of 50% C_2F_6 and 50% Ne. The photon-detector is the same type as that of RICH-1 and it has 23 K cathode pads.

1.2 Cherenkov Radiation

As mentioned in the previous section the Cherenkov effect is the fundamental principle that the RICH detectors are founded on.

It is known that the speed of light *in vacuum* is a universal constant c whereas the speed of light in a material may be significantly less than c (e.g. the speed of light in water is 0.75 c).

Cherenkov radiation results when a charged particle, most commonly an electron, exceeds the speed of light in a dielectric medium through which it passes.

Moreover, the velocity of light that must be exceeded is the phase velocity rather than the group velocity.

The phase velocity can be altered dramatically by employing a periodic medium or a complex periodic medium, such as a photonic crystal. In that case a variety

of anomalous Cherenkov effects, such as radiation in a backward direction, can be observed (let us recall that ordinary Cherenkov radiation forms an acute angle with the particle velocity).

As a charged particle travels, it disrupts the local electromagnetic field in its medium. Electrons in the atoms of the medium will be displaced and polarized by the passing EM field of the charged particle.

Photons are emitted as the insulator electrons restore themselves to equilibrium after the disruption has passed (in a conductor, the EM disruption can be restored without emitting a photon).

In normal circumstances, these photons destructively interfere with each other and no radiation is detected. However, when the disruption travels faster than the photons themselves, the photons constructively interfere with and intensify the observed radiation.

A common analogy is the sonic boom of a supersonic aircraft. The sound waves generated by the supersonic body do not move fast enough to get out of the way of the body itself. Hence, the waves stack up and form a shock front.

Similarly, a speed boat generates a large bow shock because it travels faster than waves can move on the surface of the water.

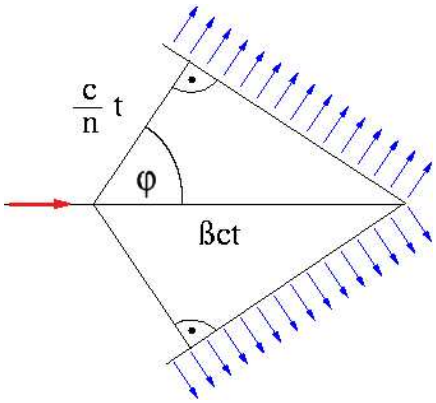


Figure 1.4: The geometry of the Cherenkov radiation.

In the same way, a charged particle generates a photonic shockwave as it travels through an insulator faster than the speed of light in that medium.

It should also be pointed out that Cherenkov radiation is entirely unrelated to the *bremsstrahlung*, which is emitted by the moving electron itself when it collides with atomic nuclei in the medium.

In contrast, the Cherenkov effect involves radiation emitted by the medium under the action of the field of the particle moving in it.

The distinction between the two types of radiation appears with particular clarity when the particle has a very large mass since *bremsstrahlung* disappears whereas Cherenkov radiation is unaffected.

Figure 1.4 shows graphically what we stated above. The red arrow represents the charged particle moving in the medium whereas the blue arrows represent the

photons emitted after the particle has passed.

From the figure it is apparent that this radiation is only observed at a particular angle called Cherenkov angle φ, with respect to the track of the particle.

This angle represents the position in which waves from arbitrary points over the particle track are coherent and combine to form a plane wave front.

If the velocity of the particle is $v = \beta\, c$ where c is the velocity of light *in vacuum* and c/n is the velocity of the Cherenkov light in the medium, then by taking into account only geometrical considerations we can write the Cherenkov angle as

$$\cos\varphi = \frac{\dfrac{c}{n\,(\lambda)}\,\Delta t}{\beta\, c\, \Delta t} \tag{1.1}$$

from which

$$\cos\varphi = \frac{1}{\beta\, n\,(\lambda)} \tag{1.2}$$

where n is the refractive index of the medium and Δt is the time interval considered in Fig. 1.4.

Let us now consider equation (1.2) in order to analyse some particular implication, namely:

- ▷ for a medium of a given refractive index n, there is a threshold velocity $\beta_{\min} = 1/n$, below which no radiation takes place. At this critical velocity the direction of radiation coincides with that of the particle. Thus the process can be used in the construction of threshold detectors in which Cherenkov radiation is only emitted if the particle has velocity greater than c/n.

- ▷ For an ultra-relativistic particle, for which $\beta = 1$, there is a maximum angle of emission given by $\cos\varphi = 1/n$.

- ▷ The radiation occurs in the visible and near visible regions of the spectrum, for which $n > 1$. A real medium is always dispersive, so actually radiation is restricted to those frequency bands for which $n\,(\omega) > 1/\beta$. In the x-ray region it is always $n\,(\omega) < 1$ and radiation is forbidden. Thus, emission in the x-ray region is impossible because n is less than unity and the equation $\cos\varphi = 1/n$ cannot be satisfied.

There are two further conditions to be fulfilled to achieve coherence. First, the length l of the track of the particle in the medium should be large compared with the wavelength of the radiation in question, otherwise diffraction effects will become dominant. Secondly, the velocity of the particle must be constant during its passage through the medium, or, to be more specific, the differences in the times for the particle to traverse successive distances λ should be small compared with the period λ/c of the emitted light.

1.3 Photomultiplier Tubes

Since the signal to be read out by the front-end electronics comes from photomultiplier tubes, it is interesting to obtain an insight into the main features of these devices.

The photomultiplier tubes (PMTs) are used for light detecting of very weak signals. They are photoemissive devices in which the absorption of a photon results in the emission of an electron.

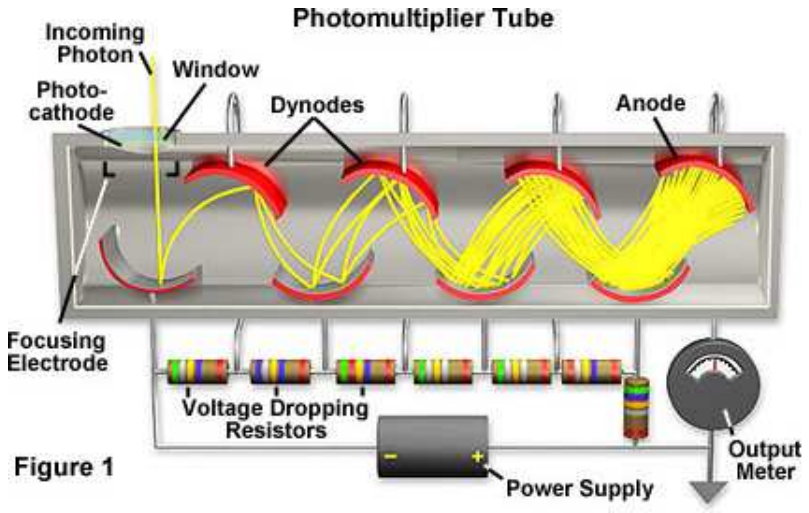


Figure 1.5: Three-dimensional schematic representation of a conventional PMT.

These detectors work by amplifying the electrons generated by a photocathode exposed to a photon flux. A three-dimensional schematic representation of such a device is shown in Fig. 1.5.

Photomultipliers acquire light through a glass or quartz window that covers a photosensitive surface, called the photocathode, which then releases electrons that are multiplied by electrodes known as metal channel dynodes.

At the end of the dynode chain there is an anode or collection electrode. Over a very large range, the current flowing from the anode to ground is directly proportional to the photoelectron flux generated by the photocathode.

The spectral response, quantum efficiency, sensitivity, and dark current of a photomultiplier tube are determined by the composition of the photocathode.

The best photocathodes capable of responding to visible light are less than 30% quantum efficient, meaning that 70% of the photons impacting on the photocathode do not produce a photoelectron and are therefore not detected.

Photocathode thickness is an important variable that must be monitored to ensure the proper response from absorbed photons.

If the photocathode is too thick, more photons will be absorbed but fewer electrons will be emitted from the back surface, but if it is too thin, too many photons will pass through without being absorbed.

The elecrons emitted by the photocathode are accelerated toward the dynode chain, which may contain up to 14 elements.

Focusing electrodes are usually present to ensure that photoelectrons emitted near the edges of the photocathode are likely to land on the first dynode.

Upon impacting the first dynode, a photoelectron will invoke the release of additional electrons that are accelerated toward the next dynode, and so on.

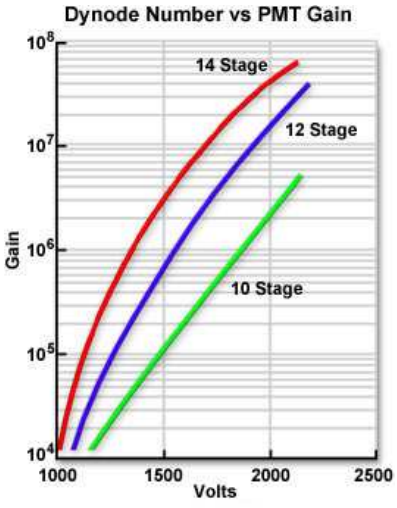


Figure 1.6: Dynode number versus PMT gain.

The surface composition and geometry of the dynodes determines their ability to serve as electron multipliers. Because the gain varies with the voltage across the dynodes and the total number of dynodes, electron gains of 10 million are possible if 12–14 dynode stages are employed, as shown in Fig. 1.6.

Photomultipliers produce a signal even in the absence of light due to the dark current arising from thermal emissions of electrons from the photocathode, leakage

current between dynodes, as well as stray high-energy radiation.

Electronic noise also contributes to the dark current and is often included in the dark-current value.

1.3.1 Channel Photomultipliers

Channel photomultipliers represent a new design that incorporates a detector having a semitransparent photocathode deposited onto the inner surface of the entrance window.

Photoelectrons released by the photocathode enter a narrow and curved semiconductive channel that performs the same functions as a classical dynode chain.

Each time an electron impacts the inner wall of the channel, multiple secondary electrons are emitted. These ejected photoelectrons have trajectories angled at the next bend in the channel wall (simulating a dynode chain), which in turn emits a larger quantity of electrons angled at the next bend in the channel.

The effect occurs repeatedly, leading to an avalanche effect with a gain exceeding 100 million.

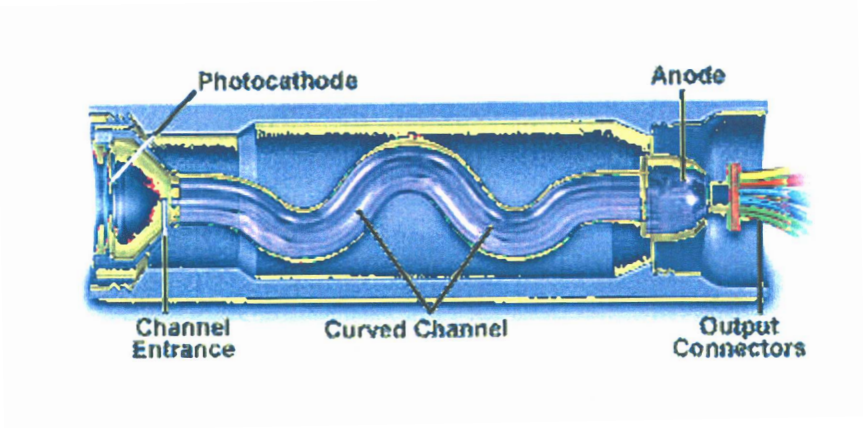


Figure 1.7: Three-dimensional schematic representation of a channel PMT.

Thus, the channel photomultiplier is a design that eliminates the hundreds of elements necessary to construct a conventional dynode chain.

The advantages of this design are lower dark current (pA range), increased sensitivity, wider bandwidth, and an extended dynamic range.

The monolithic structure provides a fairly high efficiency. Secondary emission of electrons occurs identically on any portion of the photomultiplier sidewalls, thus optimizing performance.

Because photomultipliers do not store charge and respond to changes in input light fluxes within a few nanoseconds, they can be used for the detection and recording of extremely fast events.

Finally, the signal to noise ratio is very high in scientific grade photomultipliers because the dark current is extremely low (it can be further reduced by cooling).

1.4 Front-End Electronics for the RICH

In this section we will consider the main reasons which have led to the development of a new design for the detector front-end circuit.

In fact, these new requirements have motivated the modelling and the analysis performed throughout this thesis on the front-end circuit, to give the basis for the improvement of the circuit performance, especially at a high counting rate.

An overview of the old circuit, called MAD, will be presented as well as a brief description of the features of the new circuit.

1.4.1 The MAD

The MAD is a full custom ASIC in which the analog front-end electronics for the muon chambers of CMS barrel has been integrated.

This chip has been realised in 0.8 μm BiCMOS technology and provides 4 identical chains of amplification, discrimination and cable driving circuitry.

It also integrates a flexible channel enabling/disabling feature and a temperature probe.

Figure 1.8 shows the block diagram of the MAD.

By inspecting the figure we are able to identify the four identical analog chains mentioned above.

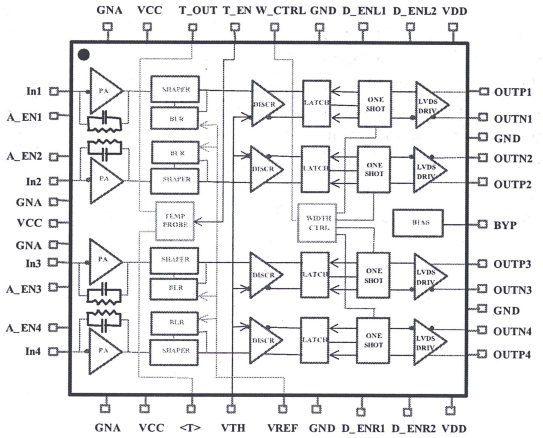


Figure 1.8: Block diagram of the MAD.

Each chain consists of a charge preamplifier (PA) followed by a pulse shaper with its baseline restorer (BLR), a latched discriminator (DISCR + LATCH) comparing the analog output of the shaper with an external reference voltage value (VTH) and issuing a standard logic signal, a programmable one-shot stretching the output logic pulses and finally an output stage able to drive long twisted pair cables with LVDS compatible levels (LVDS DRIV).

As far as the channel output section operation is concerned, we can add that the buffered output of the discriminator is capacitively coupled to the one-shot and that the discriminator differential output, when active, stores the comparator status in the latch producing a non retriggerable pulse whose width is inversely proportional to the current sunk from the W_CTRL pin, shared by all the channels.

The ASIC also includes some control and monitoring features, namely

- ▷ each channel can be disabled at the shaper input resulting in little crosstalk to neighbours,
- ▷ a fast enable/disable feature allows the simulation of tracks perpendicular to the detector,
- ▷ an absolute temperature probe is able to detect electronics failures and monitor environmental changes.

1.4.2 The CMAD

The new readout front-end circuit will be used in the COMPASS RICH upgrade to read out the signals coming from multi-anode photomultiplier tubes.

There are several important reasons which suggested the changes that characterise the new project and now some of them will be dealt with briefly here to obtain a general idea of the new circuit features.

From the fabrication process point of view the MAD was realized in $0.8\,\mu$m BiCMOS technology whereas the CMAD is realised in $0.35\,\mu$m CMOS technology. The key point here is that the $0.8\,\mu$m BiCMOS technology is obsolete and new samples of the circuit can no longer be produced in such a technology.

Also the modularity of the circuit is enhanced since the new circuit is provided with eight channels whereas the old one had only four channels.

Another important new requirement for the circuit is the gain value.

The MAD was designed to give a gain of 4 mV/fC while the CMAD allows us to choose between two gain values, the old value of 4 mV/fC, for compatibility with the old circuit, and the new value of 1.1 mV/fC, optimised for COMPASS.

In fact the signals coming from the new detector will not be as weak as those the old circuit had been conceived for. For this reason the new circuit has been designed to give a gain value smaller than the preceding one.

Finally, another demanding design specification concerns the maximum counting rate.

The new circuit is able to work correctly up to 5 MHz and an enhanced version of this circuit, capable of working properly up to a rate in the order of 10 MHz, has already been designed.

On the other hand the old circuit allowed a maximum counting rate approximately equal to 2 MHz.

Chapter 2

The Basics of Front-End Circuits

Signals delivered by particle detectors are normally fairly weak.

The first element of the electronics acquisition chain is therefore a front-end amplifier whose task is to amplify and filter the incoming signal.

In this chapter we will perform a general analysis of the stages making up a typical front-end amplifier, namely a CSA and a pulse shaper.

The purpose of this preliminary analysis is to obtain a general understanding of the behavior of these blocks.

The small-signal behavior of these stages will be dealt with in detail in the following chapters by performing a detailed analysis of their small-signal equivalent circuits.

2.1 First Stage Behavior

2.1.1 Collecting Charge

The first stage of a detector readout system consists of a preamplifier mounted as close as possible to the detector to reduce cable length as well as cable capacitance which tends to decrease the signal to noise ratio. We know three main categories of such preamplifiers according to what they are sensitive to, namely current, voltage or charge.

For our applications a CSA (Charge Sensitive Amplifier) is required because of its low noise performance and insensitivity to changes in the detector capacitance. In fact a voltage sensitive amplifier would amplify any voltage proportional to the

charge produced by the detector and appearing at its input terminals as a voltage drop across the total input capacitance. The latter consists of circuit input capacitances plus the intrinsic detector capacitance which is quite sensitive to temperature changes. As a consequence we may observe different input voltage signals even if the charge produced by the detector is the same, since $V_{\text{in}} = Q/C_{\text{tot}}$.

To overcome this problem a CSA is used and its schematic diagram is shown in Fig. 2.1.

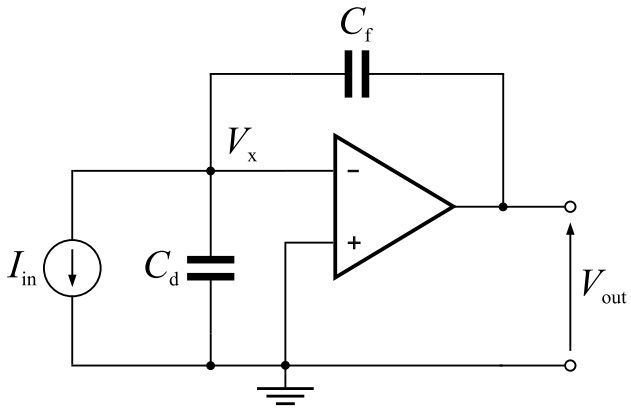


Figure 2.1: Schematic diagram of a charge-sensitive preamplifier.

By inspecting the Figure we can note that a purely capacitive negative feedback is applied to the basic amplifier causing the stage to act as an integrator. In fact the basic idea is to integrate the current carried by the incoming pulse on the capacitor C_{f}.

To find the relationship between V_{out} and I_{in}, Kirchoff's current law (KCL) can be applied. Thus from KCL at the input node,

$$I_{\text{in}} + V_{\text{x}}\, s\, C_{\text{d}} + (V_{\text{x}} - V_{\text{out}})\; s\, C_{\text{f}} = 0 \tag{2.1}$$

Assuming that the core amplifier has a finite low-frequency voltage gain of A together with a very large bandwidth, an infinite input resistance and a zero output resistance gives

$$V_{\text{out}} = A\; (V_{+} - V_{-}) \;\Rightarrow\; V_{\text{x}} = -\frac{V_{\text{out}}}{A} \tag{2.2}$$

Substituting (2.2) into (2.1) and rearranging gives

$$\frac{V_{\text{out}}}{I_{\text{in}}}\,(s) = \frac{A}{s\;(C_{\text{d}} + C_{\text{f}}) + A\, s\, C_{\text{f}}} \tag{2.3}$$

When

$$A\,s\,C_{\mathrm{f}} \gg s\,(C_{\mathrm{d}} + C_{\mathrm{f}}) \;\Rightarrow\; A \gg \frac{C_{\mathrm{d}} + C_{\mathrm{f}}}{C_{\mathrm{f}}} \tag{2.4}$$

equation (2.3) can be approximated as

$$\frac{V_{\mathrm{out}}}{I_{\mathrm{in}}}(s) \simeq \frac{1}{s\,C_{\mathrm{f}}} \tag{2.5}$$

From (2.5)

$$V_{\mathrm{out}}(s) \simeq \frac{1}{C_{\mathrm{f}}}\,\frac{I_{\mathrm{in}}(s)}{s} \tag{2.6}$$

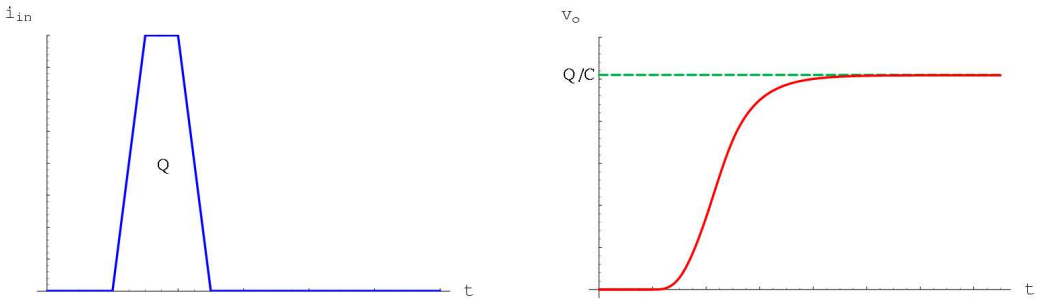
Thus, taking the inverse Laplace transform of equation (2.6) gives

$$v_{\mathrm{out}}(t) \simeq \frac{Q(t)}{C_{\mathrm{f}}} \tag{2.7}$$

which yields in the time domain the approximated output voltage of the CSA.

Let us now suppose that a small input current pulse $i_{\mathrm{in}}(t)$ carrying a total charge Q, as shown in Fig. 2.2(a), is applied to our circuit.

In agreement with equation (2.7) the output voltage of the CSA has the shape shown in Fig. 2.2(b).



(a) Input current pulse $i_{in}(t)$ carrying a charge Q.

(b) Output voltage $v_{out}(t)$ (red line) and its limiting value Q/C_{f} (green dashed line).

Figure 2.2: Current pulse response of the circuit shown in Fig. 2.1.

Moreover, by inspection of Fig. 2.2 it can be observed that the input current pulse is similar to a Dirac delta function $\delta(t)$ and the output voltage to a step function $u(t)$.

This consideration is once again in exact agreement with the fact that the stage, acting as an integrator, performs the integral of its input signal.

In fact,

$$\delta(t) = \frac{d}{dt}(u(t)) \tag{2.8}$$

2.1.2 Resetting Device

The analysis performed in the previous section has pointed out that in a CSA the incoming charge is collected by a feedback capacitor C_f.

That charge must be removed to allow the capacitor to collect the charge carried by the next current pulse, if possible avoiding the new charge being added to the previous one.

For this purpose a resistive feedback network is required. The feedback network only consists of a resistance R_f connected in parallel with the capacitance C_f as shown in Fig. 2.3 and providing a slow discharge of the capacitor.

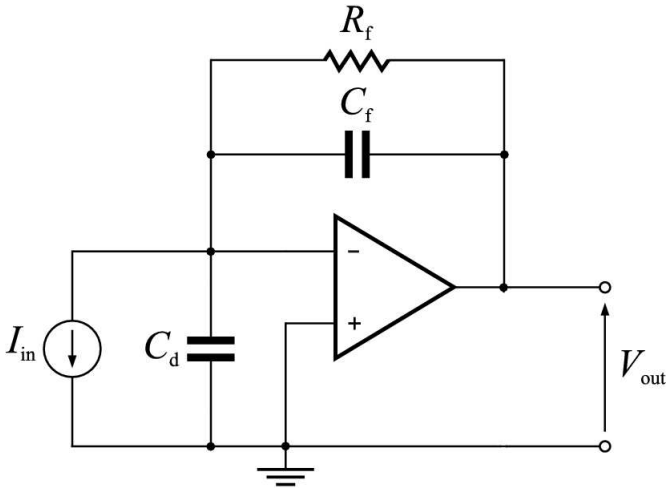
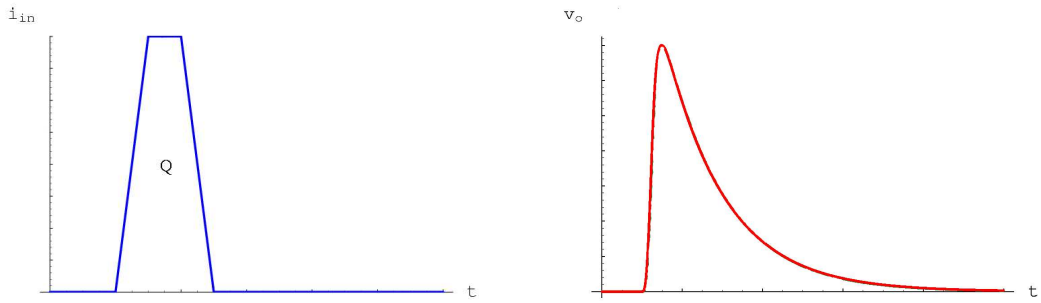


Figure 2.3: Schematic diagram of a CSA including a feedback resistance R_f.

Figure 2.4(b) shows the typical response of a CSA including a feedback resistance R_f. From a qualitative point of view we can observe that the voltage peak value will be smaller than the value Q/C_f because the capacitor discharge occurs at the same time as its charge.

Thus, the larger the resistance value, the slower the capacitor discharge and the larger the votage peak value. It approaches Q/C_{f} only in the limit as $R_{\mathrm{f}} \to \infty$.



(a) Input current pulse $i_{in}\,(t)$ carrying a charge Q.

(b) Circuit response $v_{out}\,(t)$.

Figure 2.4: Pulse response of the circuit shown in Fig. 2.3.

2.2 The Second Stage

In this section we will consider the second stage of our detector front-end circuit.

As shown in the schematic diagram of Fig. 2.5, the second stage can be thought of as consisting of two main blocks, namely a basic amplifier (OTA, Operational Transconductance Amplifier) with its feedback network (R_{sh}, C_{sh}) and a gain stage assumed to have a high output resistance so that it can be represented by a transconductor block.

This block feeds back a signal to the input and represents an active feedback network having a frequency-dependent transfer function $f\,(s)$. The purpose of this active feedback is to keep the DC output voltage of the circuit V_{OUT} (the *baseline*) approximately equal to the DC reference value V_{ref}.

In fact, the first block too keeps the DC input voltage of the second stage approximately equal to the DC value $V_{\mathrm{ref}}^{\mathrm{OTA}}$. As a result, performing this function would cause V_{OUT} to change if the second block was not there.

Furthermore, it should be pointed out that the bandwidth of the feedback block must be very narrow in order to guarantee that it has essentially zero response to each pulse. In addition, from a small-signal standpoint this block involves some

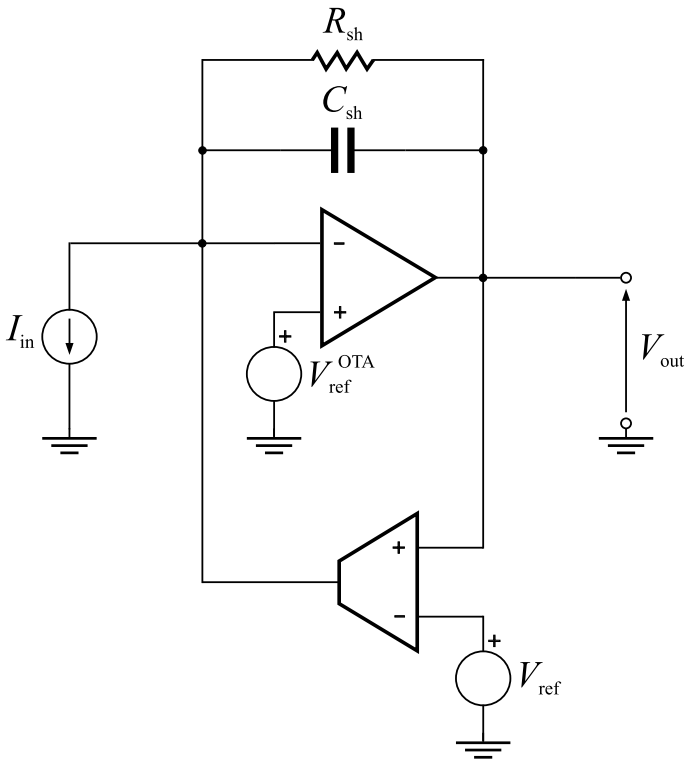


Figure 2.5: Schematic diagram of the second stage.

drawbacks as the rate of the incoming pulses increases. They will be analysed in detail in the next chapter.

An interesting way of investigating the small-signal behavior of the stage with regard to the small-signal transfer functions of the two blocks making up the stage, is to apply the feedback theory to our circuit.

Figure 2.6 displays an ideal feedback configuration consisting of two main blocks assumed to be *unilateral*, i. e. the block chacterized by $a(s)$ (the basic amplifier) can only transmit the signal from the input to the output whereas the block chacterized by $f(s)$ (the feedback network) can only transmit the signal from the output to the input and ideally does not load the basic amplifier.

It can be shown that under the above assumptions we obtain

$$\frac{S_{\text{out}}}{S_{\text{in}}} = \frac{a(s)}{1 + a(s)\ f(s)} \tag{2.9}$$

It should be pointed out that in practical feedback configurations the division into basic amplifier and feedback network is not so easy to perform due to the

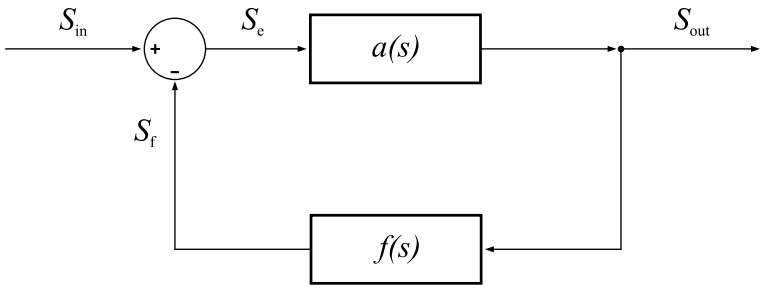


Figure 2.6: Ideal feedback configuration.

bilaterality of the actual amplifiers and the loading effect of the feedback network.

However, by assuming that in the case under examination the ideal feedback equation applies, we have

$$T^{\mathrm{II}}(s) = \frac{a(s)}{1 + a(s)\ f(s)} \tag{2.10}$$

where $T^{\mathrm{II}}(s)$ is the transfer function of the second stage, $a(s)$ represents the transfer function of the amplifier block (OTA with its feedback network) and $f(s)$ of the feedback block (transconductor block).

Thus, by considering the transfer function in the form given by (2.10) we can see that at low frequencies, where it seems reasonable to assume $|a(s)\ f(s)| \gg 1$, we have

$$T^{\mathrm{II}}(s) \sim \frac{1}{f(s)} \tag{2.11}$$

whereas at high frequencies, where we can assume $|a(s)\ f(s)| \ll 1$ due to the very narrow bandwidth of the transconductor block, we have

$$T^{\mathrm{II}}(s) \sim a(s) \tag{2.12}$$

Equation (2.11) shows that the low-pass transfer function $f(s)$ of the transconductor block achieves an approximated high-pass filter which guarantees output baseline stabilisation at low frequencies providing a lower gain at these frequencies.

However when the rate of the unipolar incoming pulses increases, a drift of the output baseline is observed due to the presence of this high-pass filter.

In order to overcome this problem a slew-rate limited non-linear buffer is inserted before the transconductor block to form a new block which is referred to as BLH (baseline holder).

This buffer performs the function of dynamically clipping the pulses to be processed by the transconductor block (the low-pass filter) in order to strongly reduce their area.

However, this dynamic attenuation only occurs for fast and large signals, thus allowing the feedback network to perform its function properly stabilising the low-frequency baseline fluctuations.

2.3 The Full Circuit

The schematic diagram of the full circuit is shown in Fig. 2.8.

An approximated small-signal analysis of the complete circuit can be performed by assuming that the output impedance of the first stage as well as the input impedance of the second stage are negligible.

In fact in this almost ideal case, we have

$$V_{\text{out}}^{\text{I}} \simeq T^{\text{I}}(s)\ I_{\text{in}} \tag{2.13}$$

$$-I_{\text{in}}^{\text{II}} \simeq \frac{V_{\text{out}}^{\text{I}}}{R} \tag{2.14}$$

$$V_{\text{out}} \simeq T^{\text{II}}(s)\ I_{\text{in}}^{\text{II}} \tag{2.15}$$

so that

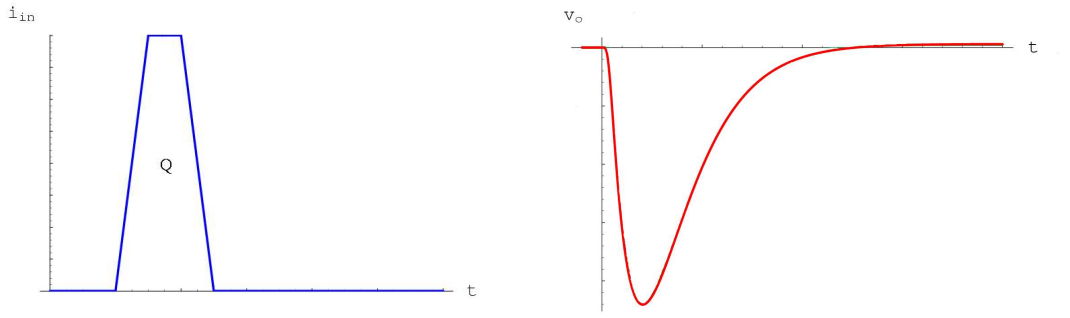
$$T(s) \simeq -\frac{T^{\text{I}}(s)\ T^{\text{II}}(s)}{R} \tag{2.16}$$

where R here can represent either R_1 or R_2. These two resistors allow us to set the gain of the complete circuit as well as to current drive the second stage.

The pulse response of the full circuit will have the shape shown in Fig. 2.7(b).

Finally let us note that Fig. 2.8 also shows a further block (comparator) giving a digital output signal.

The analysis of this block will not be performed in this thesis. However we can add that it is essentially a comparator block which compares the analog output of the full circuit (the circuit consisting of the first and the second stage) with a given reference value and outputs a binary signal based on the comparison.



(a) Input current pulse $i_{in}\,(t)$.

(b) Circuit response $v_{out}\,(t)$.

Figure 2.7: Pulse response of the complete circuit.

For binary signal we mean a signal which can have only one of two given values at any point in time, even if this concept turns out to be too ideal in practice due to the presence of a transition region between the two binary states.

Thus, due to the presence of this comparator stage, we can say that our circuit performs a binary read-out, namely it allows us to know only whether an event of a certain intensity occurred, without giving direct information on its energy.

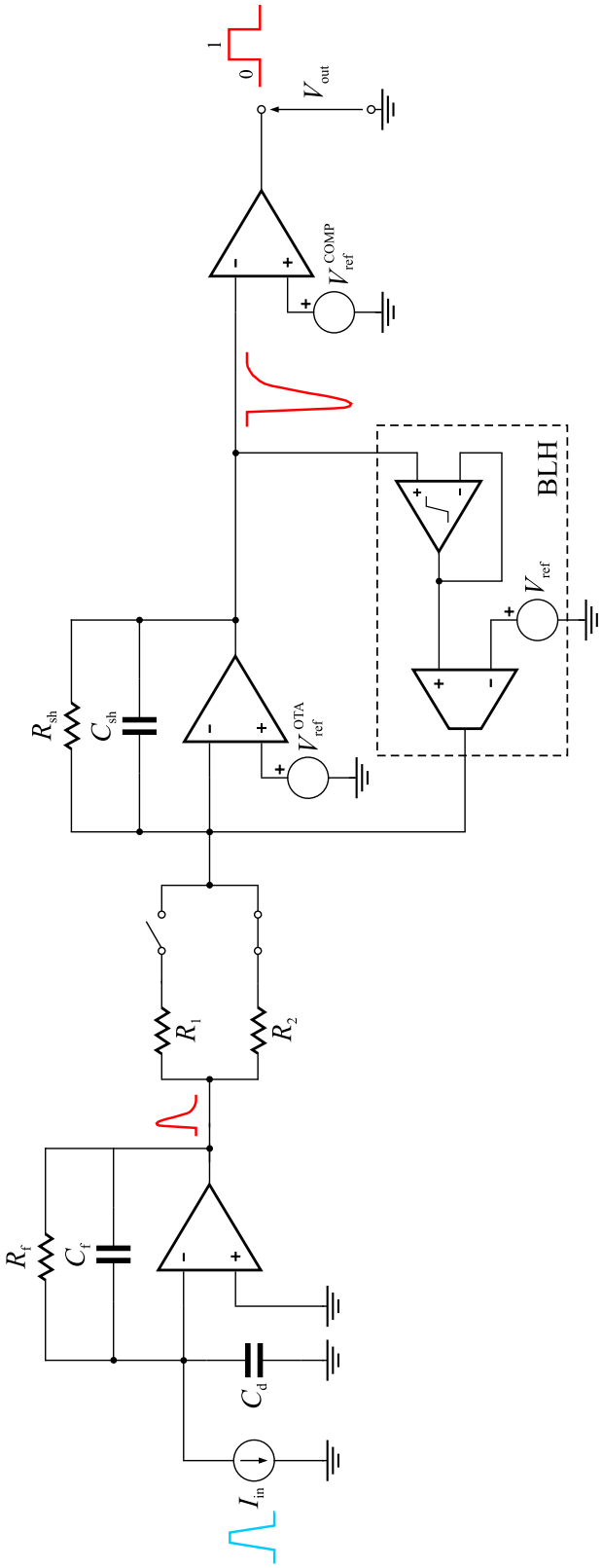


Figure 2.8: Schematic diagram of the full circuit.

Chapter 3

Modelling and Analysis of the CMAD Architecture

In this chapter we will perform from a small signal point of view a detailed analysis of the first two stages making up a detector readout system, namely a CSA and a pulse shaper. In order to obtain an understanding of factors and parameters affecting circuit behavior, a useful set of relationships stemming from opportunely simplified analytical models will be derived, in order to check our theoretical hypotheses and to perform a fast optimisation of the circuit.

Furthermore, the results obtained by using the analytical models will be compared to transistor-level SPICE simulations. Such simulations use the BSIM3V3 models and take into account the complex physics of the devices involved.

Finally, the parameter values required to obtain the several graphs shown in this chapter were estimated by small signal computer analysis of the actual circuit. This topic will be dealt with in detail in a specific section of this chapter where will be shown explicitly the relationships used for setting the parameters involved in our transfer functions.

3.1 First Stage Analysis

3.1.1 The CSA Model and Behavior

First let us consider the CSA schematic diagram illustrated in Fig. 3.1(a).

Let us observe that in our case the current signal to be processed by the CSA

comes from a single-ended detector so that the generic op amp displayed in Fig. 3.1(a) should be replaced for purposes of our analysis with a single-input amplifier block.

In fact a high-gain common-source amplifier configuration with active load is used in the actual circuit. Figure 3.1(b) shows a circuit diagram of this configuration.

Finally let us note that the schematic diagram of Fig. 3.1(a) also includes a capacitor C_{L} into which all output capacitive loads are lumped.

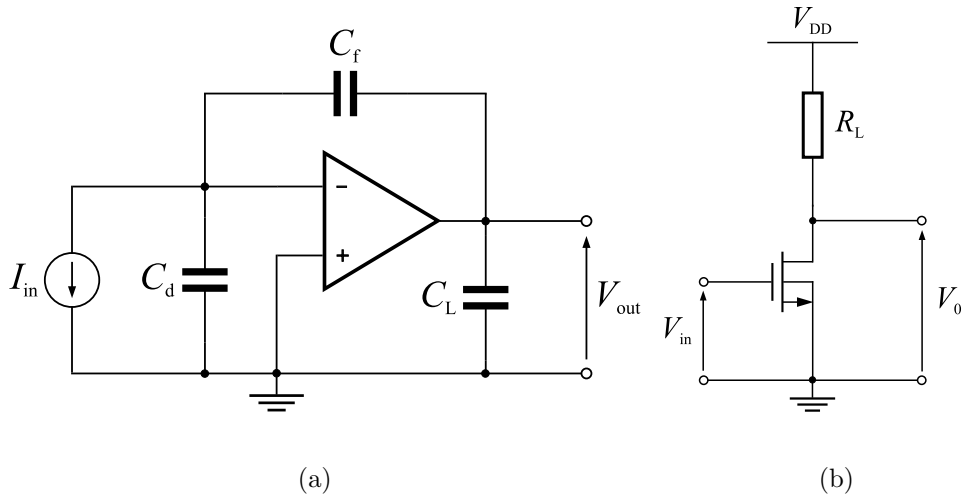


Figure 3.1: (a) Schematic diagram of a CSA including capacitive load and (b) CS configuration achieving the real single-input core amplifier.

Thus, in agreement with the above assumptions, the corresponding small-signal equivalent circuit shown in Fig. 3.2 is obtained.

From KCL at the input node,

$$I_{\mathrm{in}} + V_{\mathrm{in}}\, s\, C_{\mathrm{d}} + (V_{\mathrm{in}} - V_{\mathrm{out}})\; s\, C_{\mathrm{f}} = 0 \tag{3.1}$$

From KCL at the output node, assuming $I_{\mathrm{out}} = 0$,

$$g_{\mathrm{m}}\, V_{\mathrm{in}} + \frac{V_{\mathrm{out}}}{R_{\mathrm{L}}} + V_{\mathrm{out}}\, s\, C_{\mathrm{L}} + (V_{\mathrm{out}} - V_{\mathrm{in}})\; s\, C_{\mathrm{f}} = 0 \tag{3.2}$$

The equations (3.1) and (3.2) are a system of linear equations which can also be stated in matrix form as

$$\mathbf{Y} \cdot \mathbf{V} = \mathbf{I} \tag{3.3}$$

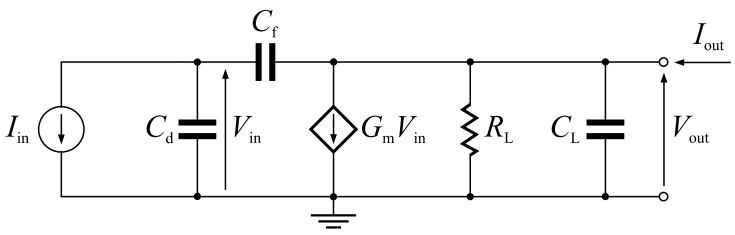


Figure 3.2: Small-signal equivalent circuit of the CSA including capacitive load.

where $\mathbf{V}$ is the vector of variables.

Matrix form can often be convenient for solving linear systems by means of computer programs.

Thus, writing the system down in this form gives

$$\begin{bmatrix} s\,(C_\mathrm{d}+C_\mathrm{f}) & -s\,C_\mathrm{f} \\ g_\mathrm{m}-s\,C_\mathrm{f} & \dfrac{1}{R_\mathrm{L}}+s\,(C_\mathrm{L}+C_\mathrm{f}) \end{bmatrix} \begin{bmatrix} V_\mathrm{in} \\ V_\mathrm{out} \end{bmatrix} = \begin{bmatrix} -I_\mathrm{in} \\ 0 \end{bmatrix} \tag{3.4}$$

Solving (3.4) for V_out and rearranging gives

$$\frac{V_\mathrm{out}}{I_\mathrm{in}}(s) = \frac{R_\mathrm{L}\,(g_\mathrm{m}-s\,C_\mathrm{f})}{s\,[C_\mathrm{d}+C_\mathrm{f}\,(1+g_\mathrm{m}\,R_\mathrm{L})+s\,R_\mathrm{L}\,(C_\mathrm{d}\,C_\mathrm{f}+C_\mathrm{d}\,C_\mathrm{L}+C_\mathrm{f}\,C_\mathrm{L})]} \tag{3.5}$$

The transfer function (3.5) can be used now for calculating the pulse response of the circit under consideration.

It can be shown that by assuming initial conditions equal to zero, the response $y\,(t)$ of a linear system to an input excitation $e\,(t)$ can be written in the time domain as

$$y\,(t) = \int_0^\infty h(t-\tau)\,e(\tau)\,\mathrm{d}\tau \tag{3.6}$$

where h is the system transfer function.

The same result as in (3.6) can be given in the frequency domain by using the Laplace transform technique and applying the properties of Laplace transform to obtain

$$Y\,(s) = H\,(s)\;E\,(s) \tag{3.7}$$

where $Y\,(s)$ and $E\,(s)$ represent the Laplace transforms of the response and the excitation respectively and $H\,(s)$ is the Laplace transform of the system transfer

function. All these functions are expressed in the domain of the complex frequency $s = \sigma + j\,\omega$.

We note that letting $e\,(t) = \delta\,(t)$ implies $E\,(s) = 1$, so that

$$Y\,(s) = H\,(s) \tag{3.8}$$

From (3.8) we deduce that $H\,(s)$ represents the pulse response transform as well.

Let us now suppose that a small input current pulse $i_{\rm in}\,(t)$ carrying a charge $Q = 4\,\mathrm{fC}$, as shown in Fig. 3.3(a), is applied to our circuit and let $I_{\rm in}\,(s)$ represent its Laplace transform.

Thus, from (3.7),

$$V_{\rm out}\,(s) = H\,(s)\;I_{\rm in}\,(s) \tag{3.9}$$

where

$$H\,(s) = \frac{V_{\rm out}}{I_{\rm in}}\,(s) \tag{3.10}$$

Setting the model parameters as listed below and performing the inverse Laplace transform of (3.9) gives the output voltage plotted in Fig. 3.3(b).

- $G_{\rm m} = 14.54\,\mathrm{mS}$
- $R_{\rm L} = 903.7\,\mathrm{k\Omega}$
- $C_{\rm d} = 10\,\mathrm{pF}\,,\;\; C_{\rm f} = 784.32\,\mathrm{fF}\,,\;\; C_{\rm L} = 382\,\mathrm{fF}$

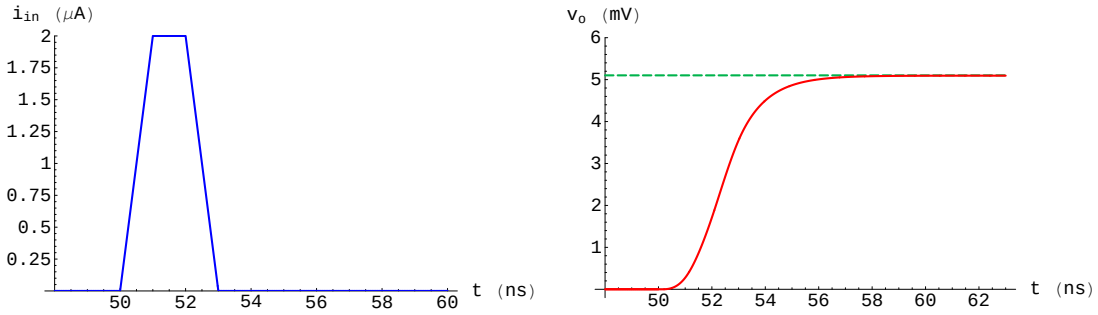
Referring to Fig. 3.3(b) we can finally note that the output voltage approaches the constant value $v = 5.1\,\mathrm{mV}$ in exact agreement with what (2.7) predicts, i.e.

$$v_{\rm out} \simeq \frac{Q}{C_{\rm f}} = \frac{4\,\mathrm{fC}}{784.32\,\mathrm{fF}} \simeq 5.099\,\mathrm{mV}$$

which means that all the charge carried by the pulse has been integrated onto the feedback capacitance $C_{\rm f}$.

3.1.2 Resetting Device

The behavior of a charge-sensitive amplifier was described through the analysis performed in the previous section, pointing out that the incoming charge is collected



(a) Input current pulse $i_{in}\,(t)$.

(b) Output voltage $v_{out}\,(t)$ (red line) and its limiting value (green dashed line).

Figure 3.3: Current pulse response of the circuit shown in Fig. 3.1(a).

by the feedback capacitor C_f. Now that charge must be removed to allow the capacitor to collect the charge carried by the next current pulse, if possible avoiding the new charge being added to the previous one. For this purpose a resistive feedback network is required. The feedback network only consists of a resistance R_f assumed at first to be connected in parallel with the capacitance C_f as shown in Fig. 3.4 and providing a fairly slow discharge of the capacitor.

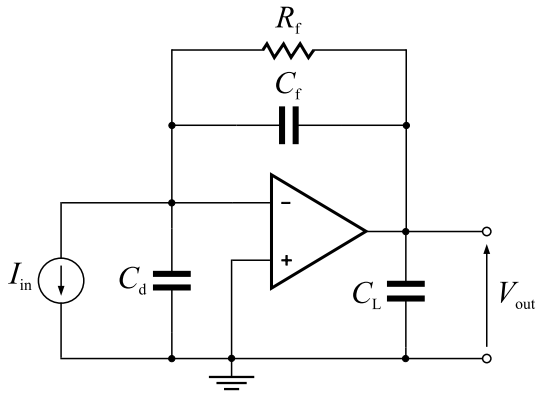


Figure 3.4: Schematic diagram of a CSA including a feedback resistance R_f.

However, we will show that the above assumption about the way to connect R_f to the rest of the circuit involves some drawbacks affecting important aspects of circuit performance.

Thus, let us consider the small-signal equivalent circuit illustrated in Fig. 3.5 and referred to the schematic diagram of Fig. 3.4.

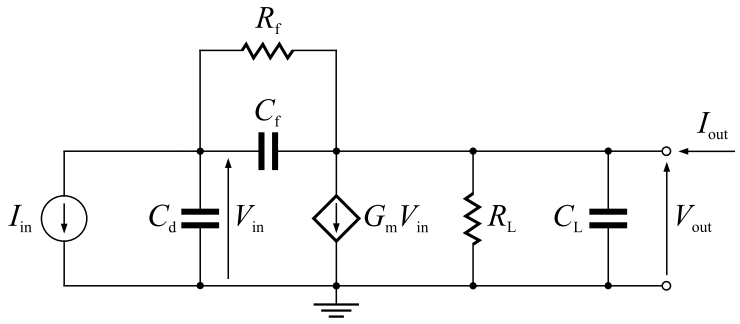
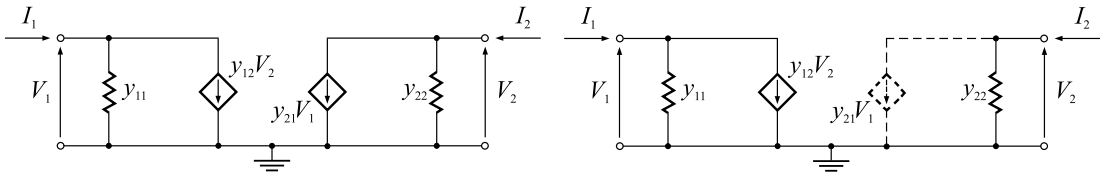


Figure 3.5: Small-signal equivalent circuit of a CSA including a feedback resistance R_f.

As stated above the feedback network is represented by R_f and this kind of feedback amplifier connection is called *shunt-shunt* feedback because the feedback network shunts the output of the basic amplifier sampling V_{out} and also shunts the input feeding back a proportional current. One possible way to analyse the feedback network behavior is to model it as a two-port equivalent network having four terminals and four port variables as shown in Fig. 3.6(a). We can set one independent variable at each port whereas the other variables will depend on the network and on the independent variables.



(a) Complete circuit.

(b) Simplified circuit ($y_{21} = 0$).

Figure 3.6: y-parameter two-port equivalent circuits for representing the feedback network.

Setting the terminal voltages as independent variables gives

$$I_1 = y_{11}\, V_1 + y_{12}\, V_2 \tag{3.11}$$

$$I_2 = y_{21}\, V_1 + y_{22}\, V_2 \tag{3.12}$$

where

$$y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0} \qquad y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0} \tag{3.13}$$

$$y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} \qquad y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0} \tag{3.14}$$

It is interesting to note that an ideal feedback network should shunt the output with $y_{22} = 0$ and the input with $y_{22} = 0$. In practice it causes loading at the input and at the output of the basic amplifier. Even y_{21} should be equal to zero, assuming the network is only able to feed back the signal from the output to the input. However, we can almost always assume that y_{21} of the feedback network is negligible compared to the analogous parameter of the basic amplifier. As a result we can use the model shown in Fig. 3.6(b).

Let us now calculate the y-parameters for the case under consideration. By inspecting Fig. 3.7 and using (3.13) and (3.14) we find

$$y_{11} = \frac{1}{R_\mathrm{f}} \qquad y_{22} = \frac{1}{R_\mathrm{f}} \tag{3.15}$$

$$y_{12} = -\frac{1}{R_\mathrm{f}} \tag{3.16}$$

Thus, the small-signal equivalent circuit illustrated in Fig. 3.5 can be redrawn as shown in Fig. 3.8. The whole circuit can be thought of as consisting of a new basic amplifier allowing for loading of the non-ideal feedback network and an ideal feedback network which does not load it.

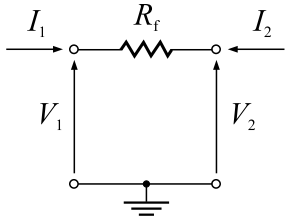


Figure 3.7: Feedback network for y parameters calculation.

As a result we can see by direct inspection that the low-frequency open loop voltage gain of the basic amplifier has been decreased by the feedback resistance due to its loading effect. In fact, before connecting R_f, we had

$$A_\mathrm{v} = \left.\frac{V_\mathrm{out}}{V_\mathrm{in}}\right|_{I_\mathrm{out}=0} = -G_\mathrm{m}\, R_\mathrm{L} \tag{3.17}$$

at low-frequency, while we now have

$$A_\mathrm{v} = \left.\frac{V_\mathrm{out}}{V_\mathrm{in}}\right|_{I_\mathrm{out}=0} = -G_\mathrm{m}\ (R_\mathrm{L} \parallel R_\mathrm{f}) \lesssim -G_\mathrm{m}\, R_\mathrm{f} \ll -G_\mathrm{m}\, R_\mathrm{L} \tag{3.18}$$

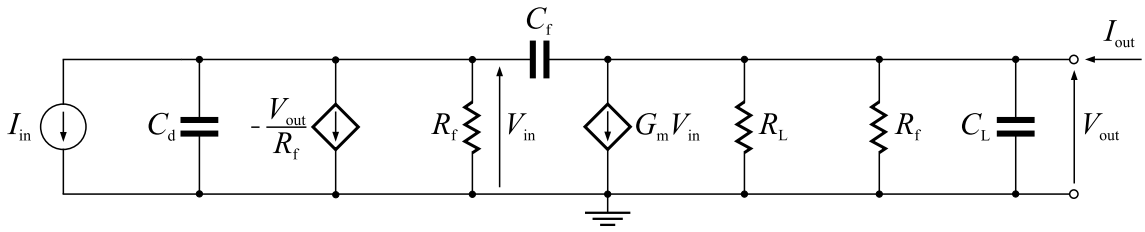


Figure 3.8: Small-signal equivalent circuit of Fig. 3.5 redrawn from a feedback network two-port equivalent circuit standpoint.

assuming $R_L \gg R_f$.

In order to overcome the problem we have just pointed out, we can modify the circuit schematic diagram of Fig. 3.4 by using a voltage buffer as shown in Fig. 3.9. Furthermore this solution allows us to avoid a direct coupling between C_f and other input capacitances of the following stage.

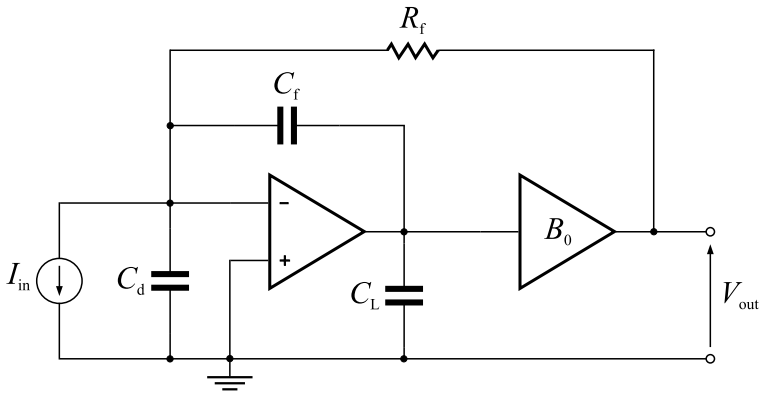


Figure 3.9: Schematic diagram of a CSA including a feedback resistance R_f and a voltage buffer B_0.

From a small-signal standpoint the corresponding equivalent circuit is shown in Fig. 3.10.

From KCL at the input node,

$$I_{in} + V_{in}\, s\, C_d + (V_{in} - V_0)\; s\, C_f + \frac{(V_{in} - V_{out})}{R_f} = 0 \tag{3.19}$$

From KCL at the internal node (node 1),

$$(V_0 - V_{in})\; s\, C_f + G_m\, V_{in} + V_0 \left(s\, C_L + \frac{1}{R_L} \right) = 0 \tag{3.20}$$

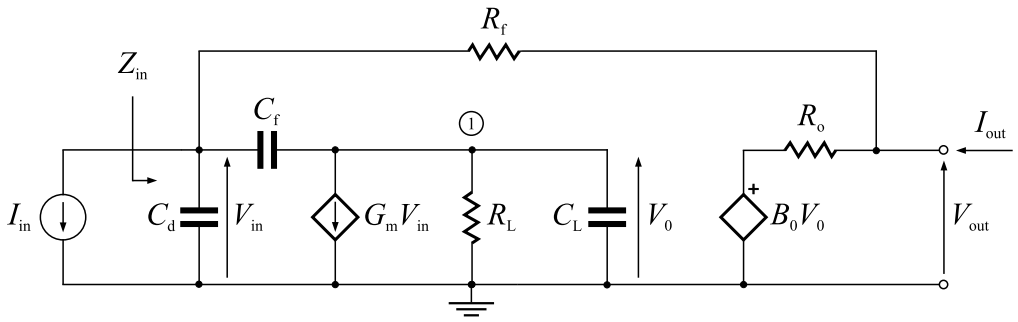


Figure 3.10: Small-signal equivalent circuit of a CSA including a feedback resistance R_f and a voltage buffer B_0.

From KCL at the output node,

$$\frac{(V_{out} - V_{in})}{R_f} + \frac{(V_{out} - B_0\, V_0)}{R_o} - I_{out} = 0 \tag{3.21}$$

Writing down in matrix form the system consisting of the simultaneous equations (3.19), (3.20), (3.21), yields

$$\begin{bmatrix} \frac{1}{R_f} + s\ (C_d + C_f) & -s\, C_f & -\frac{1}{R_f} \\ G_m - s\, C_f & \frac{1}{R_L} + s\ (C_f + C_L) & 0 \\ -\frac{1}{R_f} & -\frac{B_0}{R_o} & \frac{1}{R_f} + \frac{1}{R_o} \end{bmatrix} \begin{bmatrix} V_{in} \\ V_0 \\ V_{out} \end{bmatrix} = \begin{bmatrix} -I_{in} \\ 0 \\ I_{out} \end{bmatrix} \tag{3.22}$$

Assuming $I_{out} = 0$, solving (3.22) for V_{out} and rearranging gives

$$T^{I}(s) = \frac{V_{out}}{I_{in}}(s) = \frac{(B_0\, G_m\, R_f\, R_L - R_o) - R_L\ [B_0\, C_f\, R_f + R_o\ (C_f + C_L)]\ s}{d_0 + d_1\, s + d_2\, s^2} \tag{3.23}$$

where

$$\begin{cases} d_0 = 1 + B_0\, G_m\, R_L \\ d_1 = R_f\ [C_f\ (1 + G_m\, R_L) + C_d] + R_L\ [C_f\ (1 - B_0 + G_m\, R_o) + C_L] + \\ \qquad + R_o\ (C_d + C_f) \\ d_2 = (R_f + R_o)\ R_L\ (C_d\, C_f + C_d\, C_L + C_f\, C_L) \end{cases} \tag{3.24}$$

3.1.3 Pole Splitting

As we have seen earlier by studying the behavior of the CSA, the capacitor C_f performs the important function of collecting the incoming charge carried by the signal current. Although this is undoubtedly its primary function, we will show that it contributes in a significant way to the phenomenon of *pole splitting* as well. In general, performing the splitting of the two low-frequency poles of a circuit can play an important role in solving the problem of its compensation.

In order to illustrate the pole splitting performed by C_f, we will plot a locus of the poles of the transfer function given by (3.23) as the value C_f of the feedback capacitance changes.

To carry out a hand analysis that allows us to obtain some useful expressions for pole position, let us examine the transfer function $T^\mathrm{I}(s)$. Since it can be written in the form

$$T^\mathrm{I}(s) = \frac{C(s)}{A(s) + C_\mathrm{f}\, B(s)} \tag{3.25}$$

the poles of $T^\mathrm{I}(s)$ can be found by solving

$$A(s) = 0 \tag{3.26}$$

when $C_\mathrm{f} = 0$, and

$$B(s) = 0 \tag{3.27}$$

in the limit as $C_\mathrm{f} \to \infty$.

Thus, by collecting the terms involving C_f in the denominator of $T^\mathrm{I}(s)$ we find

$$\begin{aligned} A(s) &= (1 + B_0\, G_\mathrm{m}\, R_\mathrm{L}) + (R_\mathrm{f}\, C_\mathrm{d} + R_\mathrm{L}\, C_\mathrm{L} + R_\mathrm{o}\, C_\mathrm{d})\ s + \\ &\quad + [(R_\mathrm{f} + R_\mathrm{o})\ R_\mathrm{L}\, C_\mathrm{d}\, C_\mathrm{L}]\ s^2 \\ &= a_0 + a_1\, s + a_2\, s^2 \end{aligned} \tag{3.28}$$

and

$$\begin{aligned} B(s) &= [(R_\mathrm{f} + R_\mathrm{o})\ (1 + G_\mathrm{m}\, R_\mathrm{L}) + R_\mathrm{L}\ (1 - B_0)]\ s + \\ &\quad + [(R_\mathrm{f} + R_\mathrm{o})\ R_\mathrm{L}\ (C_\mathrm{d} + C_\mathrm{L})]\ s^2 \\ &= b_1\, s + b_2\, s^2 \\ &= s\ (b_1 + b_2 s) \end{aligned} \tag{3.29}$$

Substituting (3.29) in (3.27) and solving the equation for the poles p_1, p_2 yields

$$p_1 = 0 \tag{3.30}$$

and

$$p_2 = -\frac{b_1}{b_2} = -\frac{(R_\mathrm{f} + R_\mathrm{o})\ (1 + G_\mathrm{m}\, R_\mathrm{L}) + R_\mathrm{L}\ (1 - B_0)}{(R_\mathrm{f} + R_\mathrm{o})\ R_\mathrm{L}\ (C_\mathrm{d} + C_\mathrm{L})} \tag{3.31}$$

Equations (3.30) and (3.31) give the limiting values for the poles as $C_\mathrm{f} \to \infty$. Let us point out that the poles are real in this case.

Furthermore, relationship (3.31) for the nondominant pole p_2 can be approximated by

$$p_2 \simeq -\frac{R_\mathrm{f}\, G_\mathrm{m}\, R_\mathrm{L}}{R_\mathrm{f}\, R_\mathrm{L}\ (C_\mathrm{d} + C_\mathrm{L})} = -\frac{G_\mathrm{m}}{(C_\mathrm{d} + C_\mathrm{L})} \tag{3.32}$$

assuming that $R_\mathrm{f} \gg R_\mathrm{o}$, $G_\mathrm{m}\, R_\mathrm{L} \gg 1$ and $B_0 \lesssim 1$, which is in agreement with the model parameter values referring to the actual circuit and listed below:

- $G_\mathrm{m} = 14.54\,\mathrm{mS}$
- $R_\mathrm{f} = 16.408\,\mathrm{k\Omega}\,,\ R_\mathrm{L} = 903.7\,\mathrm{k\Omega}\,,\ R_\mathrm{o} = 166.5\,\Omega$
- $C_\mathrm{d} = 10\,\mathrm{pF}\,,\ C_\mathrm{f} = 784.32\,\mathrm{fF}\,,\ C_\mathrm{L} = 382\,\mathrm{fF}$
- $B_0 = 0.81$

Let us now examine the limiting case $C_\mathrm{f} = 0$. Equation (3.26) with $A\,(s)$ given by (3.28) is to be solved to obtain the poles p_1 and p_2. However, since this poles might be complex we prefer not to give an approximated expression for the poles in this case, recalling that in general the quadratic formula must be used.

In fact, by inspecting Fig. 3.11 which shows the locus of the poles of the circuit of Fig. 3.10 calculated by *Mathematica* program as C_f is increased from zero, we can see that the poles are just complex for the C_f starting value.

Now, it could be interesting to find an approximate expression for the poles in the case when C_f is large enough to cause them to be real.

Thus, under the above assumption, we refer to the denominator of the transfer function (3.23), which is

$$D\,(s) = d_0 + d_1\, s + d_2\, s^2 = d_0 \left(1 + \frac{d_1}{d_0}\, s + \frac{d_2}{d_0}\, s^2\right) \tag{3.33}$$

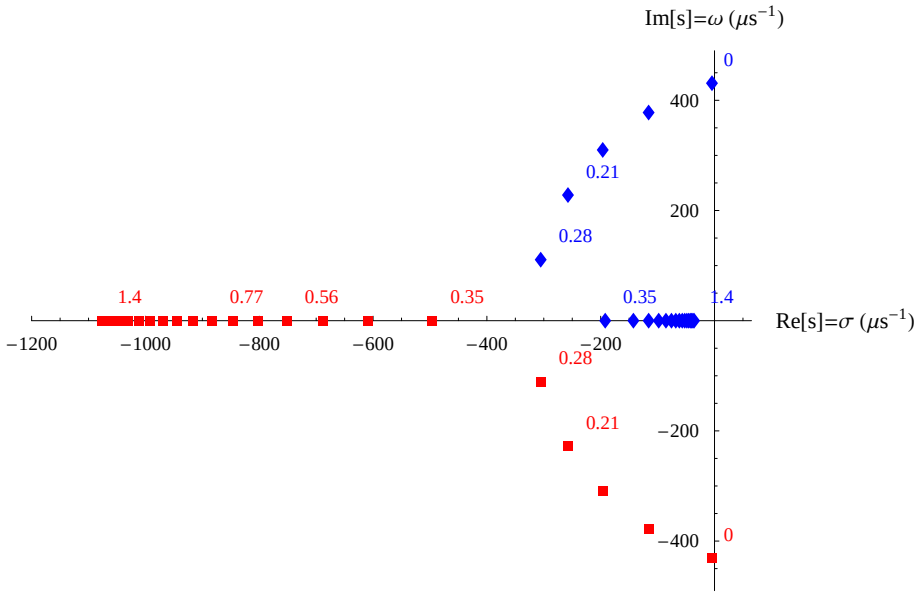


Figure 3.11: Locus of the poles of the circuit of Fig. 3.10 as C_f (pF) is increased from zero (up to $C_\mathrm{f}^{max} = 1.4\,\mathrm{pF}$ in steps of $\delta C_\mathrm{f} = 70\,\mathrm{fF}$).

with the coefficients given by (3.24). It can be written as

$$D\left(s\right) = d_0 \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = d_0 \left[1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1\, p_2}\right] \tag{3.34}$$

where p_1 and p_2 are the poles of the circuit.

They can be easily found by concentrating on the quadratic term in parenthesis in (3.33) and (3.34), if we assume they are widely separated in addition to being real. Thus, assuming p_1 is the dominant pole gives

$$1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1\, p_2} \simeq 1 - \frac{s}{p_1} + \frac{s^2}{p_1\, p_2} \tag{3.35}$$

By equating coefficients in (3.33) and (3.35), we find

$$p_1 \approx -\frac{1 + B_0 G_\mathrm{m} R_\mathrm{L}}{R_\mathrm{f}\left[C_\mathrm{f}\left(1 + G_\mathrm{m} R_\mathrm{L}\right) + C_\mathrm{d}\right] + R_\mathrm{L}\left[C_\mathrm{f}\left(1 - B_0 + G_\mathrm{m} R_\mathrm{o}\right) + C_\mathrm{L}\right] + R_\mathrm{o}\left(C_\mathrm{d} + C_\mathrm{f}\right)} \tag{3.36}$$

and

$$p_2 \approx -\frac{R_\mathrm{f}\left[C_\mathrm{f}\left(1+G_\mathrm{m}R_\mathrm{L}\right)+C_\mathrm{d}\right]+R_\mathrm{L}\left[C_\mathrm{f}\left(1-B_0+G_\mathrm{m}R_\mathrm{o}\right)+C_\mathrm{L}\right]+R_\mathrm{o}\left(C_\mathrm{d}+C_\mathrm{f}\right)}{\left(R_\mathrm{f}+R_\mathrm{o}\right)R_\mathrm{L}\left(C_\mathrm{d}C_\mathrm{f}+C_\mathrm{d}C_\mathrm{L}+C_\mathrm{f}C_\mathrm{L}\right)} \tag{3.37}$$

These expressions can be further approximated by assuming that $R_\mathrm{f} \gg R_\mathrm{o}$, $B_0 \lesssim 1$, $G_\mathrm{m}\,R_\mathrm{L} \gg 1$ and the term $R_\mathrm{f}\,C_\mathrm{f}\,G_\mathrm{m}\,R_\mathrm{L}$ due to the Miller effect is dominant compared to the other terms, which is once again in agreement with the model parameter values previously given.

Finally we can write

$$p_1 \simeq -\frac{B_0\,G_\mathrm{m}\,R_\mathrm{L}}{R_\mathrm{f}\,C_\mathrm{f}\,G_\mathrm{m}\,R_\mathrm{L}} = -\frac{B_0}{R_\mathrm{f}\,C_\mathrm{f}} \simeq -\frac{1}{R_\mathrm{f}\,C_\mathrm{f}} \tag{3.38}$$

and

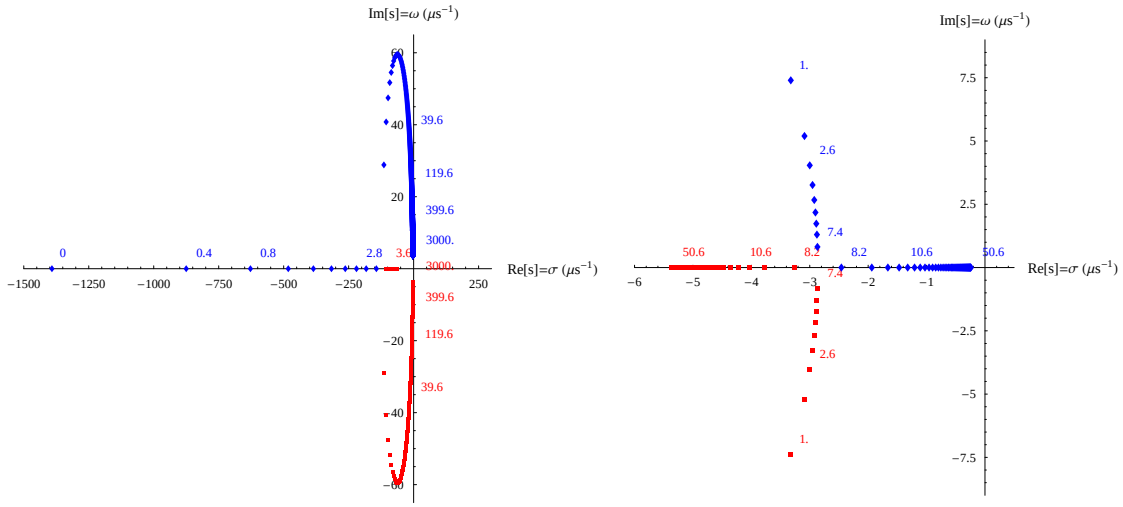
$$p_2 \simeq -\frac{R_\mathrm{f}\,C_\mathrm{f}\,G_\mathrm{m}\,R_\mathrm{L}}{R_\mathrm{f}\,R_\mathrm{L}\,\left[C_\mathrm{f}\,\left(C_\mathrm{d}+C_\mathrm{L}\right)+C_\mathrm{d}\,C_\mathrm{L}\right]} = -\frac{C_\mathrm{f}\,G_\mathrm{m}}{C_\mathrm{f}\,\left(C_\mathrm{d}+C_\mathrm{L}\right)+C_\mathrm{d}\,C_\mathrm{L}} \tag{3.39}$$

We can also note that in the limit as $C_\mathrm{f} \to \infty$ they agree exactly with the limiting values shown in (3.30) and (3.32).

After investigating what occurs to the poles of the circuit under consideration as C_f changes, it may be interesting to observe the shape of the locus of the poles for varying the load capacitance C_L and the detector capacitance C_d, given the other parameter values. Although a detailed analysis to obtain approximated expressions for the poles in the limit as $C_\mathrm{L} = 0$ and $C_\mathrm{L} \to \infty$ as well as $C_\mathrm{d} = 0$ and $C_\mathrm{d} \to \infty$ can be carried out by following the same steps which led us to the expressions (3.30) and (3.31), these steps will not be shown here. However, a numerical analysis of the roots of the denominator of the transfer function for varying C_L and C_d gives the graphical results shown in Fig. 3.12 and in Fig. 3.13, respectively.

By inspecting Fig. 3.12(a) we can see that increasing C_L causes the poles to converge till they leave the real axis to become complex. Only for large values of C_L do they become real again, splitting apart as C_L is further increased (Fig. 3.12(b)).

The same occurs as C_d is increased, which gives rise to the root-locus shown in Fig. 3.13 whose shape is similar to that of the case described earlier.



(a) Locus of the poles with C_{L} running from $C_{\mathrm{L}}^{min} = 0\,\mathrm{pF}$ to $C_{\mathrm{L}}^{max} = 3000\,\mathrm{pF}$ in steps of $\delta C_{\mathrm{L}} = 0.4\,\mathrm{pF}$.

(b) Locus of the poles with C_{L} running from $C_{\mathrm{L}}^{min} = 1\,\mathrm{nF}$ to $C_{\mathrm{L}}^{max} = 50.6\,\mathrm{nF}$ in steps of $\delta C_{\mathrm{L}} = 0.8\,\mathrm{nF}$.

Figure 3.12: Locus of the poles of the circuit of Fig. 3.10 as C_{L} is increased from zero.

3.1.4 Frequency Analysis of the First Stage

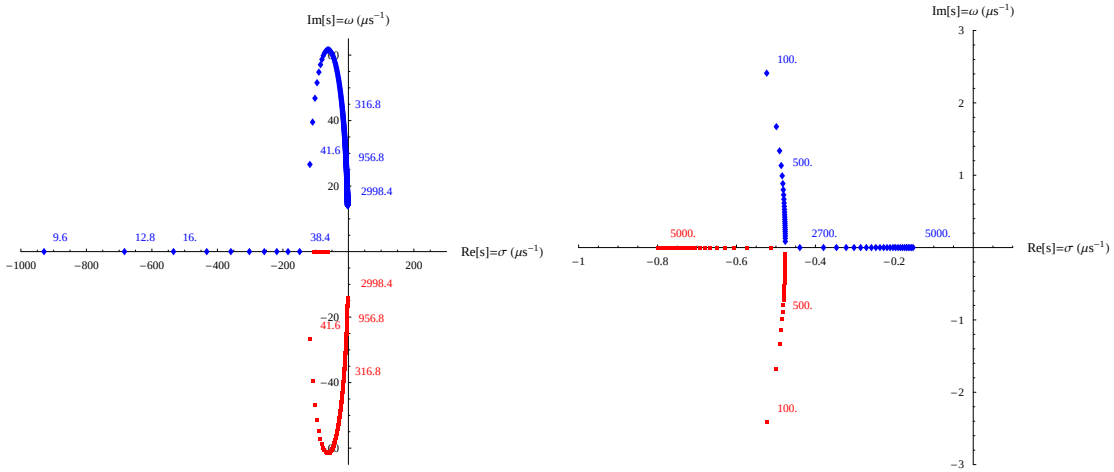
Transfer Function

The calculation of the transfer function of the first stage was already carried out in the previous section. However, for convenience we show again the results given in (3.23)

$$T^{\mathrm{I}}(s)\Big|_{I_{\mathrm{out}}=0} = \frac{(B_0\,G_{\mathrm{m}}\,R_{\mathrm{f}}\,R_{\mathrm{L}} - R_{\mathrm{o}}) - R_{\mathrm{L}}\,[B_0\,C_{\mathrm{f}}\,R_{\mathrm{f}} + R_{\mathrm{o}}\,(C_{\mathrm{f}} + C_{\mathrm{L}})]\,s}{d_0 + d_1\,s + d_2\,s^2} \tag{3.40}$$

and in (3.24)

$$\begin{cases} d_0 = 1 + B_0\,G_{\mathrm{m}}\,R_{\mathrm{L}} \\ d_1 = R_{\mathrm{f}}\,[C_{\mathrm{f}}\,(1 + G_{\mathrm{m}}\,R_{\mathrm{L}}) + C_{\mathrm{d}}] + R_{\mathrm{L}}\,[C_{\mathrm{f}}\,(1 - B_0 + G_{\mathrm{m}}\,R_{\mathrm{o}}) + C_{\mathrm{L}}] + \\ \qquad + R_{\mathrm{o}}\,(C_{\mathrm{d}} + C_{\mathrm{f}}) \\ d_2 = (R_{\mathrm{f}} + R_{\mathrm{o}})\;R_{\mathrm{L}}\;(C_{\mathrm{d}}\,C_{\mathrm{f}} + C_{\mathrm{d}}\,C_{\mathrm{L}} + C_{\mathrm{f}}\,C_{\mathrm{L}}) \end{cases} \tag{3.41}$$



(a) Locus of the poles with C_d running from $C_\mathrm{d}^{min} = 9.6\,\mathrm{pF}$ to $C_\mathrm{d}^{max} = 2998.4\,\mathrm{pF}$ in steps of $\delta C_\mathrm{d} = 3.2\,\mathrm{pF}$.

(b) Locus of the poles with C_d running from $C_\mathrm{d}^{min} = 100\,\mathrm{nF}$ to $C_\mathrm{d}^{max} = 5000\,\mathrm{nF}$ in steps of $\delta C_\mathrm{d} = 100\,\mathrm{nF}$.

Figure 3.13: Locus of the poles of the circuit of Fig. 3.10 as C_d is increased.

The analysis of equation (3.40) indicates that the circuit has a positive real zero with magnitude

$$\mid z_1 \mid = \frac{B_0\, G_\mathrm{m}\, R_\mathrm{f}\, R_\mathrm{L} - R_\mathrm{o}}{R_\mathrm{L}\, \left[B_0\, C_\mathrm{f}\, R_\mathrm{f} + R_\mathrm{o}\, \left(C_\mathrm{f} + C_\mathrm{L}\right)\right]} \tag{3.42}$$

Assuming R_f and R_L are much larger than R_o allows us to approximate the above expression to obtain

$$\mid z_1 \mid \simeq \frac{B_0\, G_\mathrm{m}\, R_\mathrm{f}\, R_\mathrm{L}}{B_0\, C_\mathrm{f}\, R_\mathrm{f}\, R_\mathrm{L}} = \frac{G_\mathrm{m}}{C_\mathrm{f}} \simeq 18.54 \times 10^9\,\mathrm{s}^{-1} \;\Rightarrow\; 2.95\,\mathrm{GHz} \tag{3.43}$$

Thus, we can see that the effect of this zero is negligible except at very high frequencies.

Equation (3.40) also shows that the transfer function has two poles whose magnitude can be estimated by using the approximated expressions given in (3.38), (3.39) and discussed in detail in that section.

Then, using the results obtained there yields

$$\mid p_1 \mid \simeq \frac{1}{R_\mathrm{f}\, C_\mathrm{f}} \simeq 77.7 \times 10^6\,\mathrm{s}^{-1} \;\Rightarrow\; 12.37\,\mathrm{MHz} \tag{3.44}$$

and

$$| p_2 | \simeq \frac{C_\mathrm{f}\, G_\mathrm{m}}{C_\mathrm{f}\ (C_\mathrm{d} + C_\mathrm{L}) + C_\mathrm{d}\, C_\mathrm{L}} \simeq 953.3 \times 10^6\, \mathrm{s}^{-1} \ \Rightarrow\ 151.72\, \mathrm{MHz} \tag{3.45}$$

Furthermore we can calculate the low-frequency transimpedance gain by analysing (3.40) in the limit as $s \to 0$.

Assuming $G_\mathrm{m}\, R_\mathrm{L} \gg 1$ and $B_0 \simeq 1$, we obtain

$$K = \frac{B_0\, G_\mathrm{m}\, R_\mathrm{f}\, R_\mathrm{L} - R_\mathrm{o}}{1 + B_0\, G_\mathrm{m}\, R_\mathrm{L}} \approx R_\mathrm{f} = 16.408\, \mathrm{k\Omega} \tag{3.46}$$

Now, writing the transfer function down as

$$T^\mathrm{I}(s) = K\, \frac{\left(1 - \dfrac{s}{z_1}\right)}{\left(1 - \dfrac{s}{p_1}\right)\left(1 - \dfrac{s}{p_2}\right)} \tag{3.47}$$

assuming the poles to be widely separated and the zero negligible as stated above and setting $s = j\omega$ in (3.47), shows that the gain is 3 dB below its low-frequency value at a frequency $\omega_{-3\,\mathrm{dB}} = | p_1 |$, since, under these assumptions

$$T^\mathrm{I}(j\omega_{-3\,\mathrm{dB}}) \simeq K/(1 + j) \tag{3.48}$$

which affords $| T^\mathrm{I}(j\omega_{-3\,\mathrm{dB}}) | \simeq K/\sqrt{2}$ as well as $Arg\left[T^\mathrm{I}(j\omega_{-3\,\mathrm{dB}})\right] \simeq -45°$.

It can be shown that at frequencies above the dominant pole the gain falls at 20 dB/dec and, above the second most dominant pole, the gain roll-off is further increased by 20 dB/dec.

The preceding considerations are in agreement with the curves plotted in Fig. 3.14 which show the magnitude and phase of $T^\mathrm{I}(s)\,|_{s=j\omega}$ versus frequency, superimposing the graphic results from our small-signal analytical model (red and blue lines) on those from a transistor-level model (green and purple lines).

Fig. 3.14(b) shows that our circuit, at low frequency, is a good transresistance amplifier whose gain approaches the value of the feedback resistance as predicted by (3.46).

Furthermore, by inspection of the figure we can also realise that our model is able to represent accurately the circuit behavior in a fairly wide range of frequencies. However it is apparent that a lot of parasitic capacitance which we did not take into account, plays an increasingly significant role at high frequencies, thus providing in that range a larger difference between the results arising from the two models.

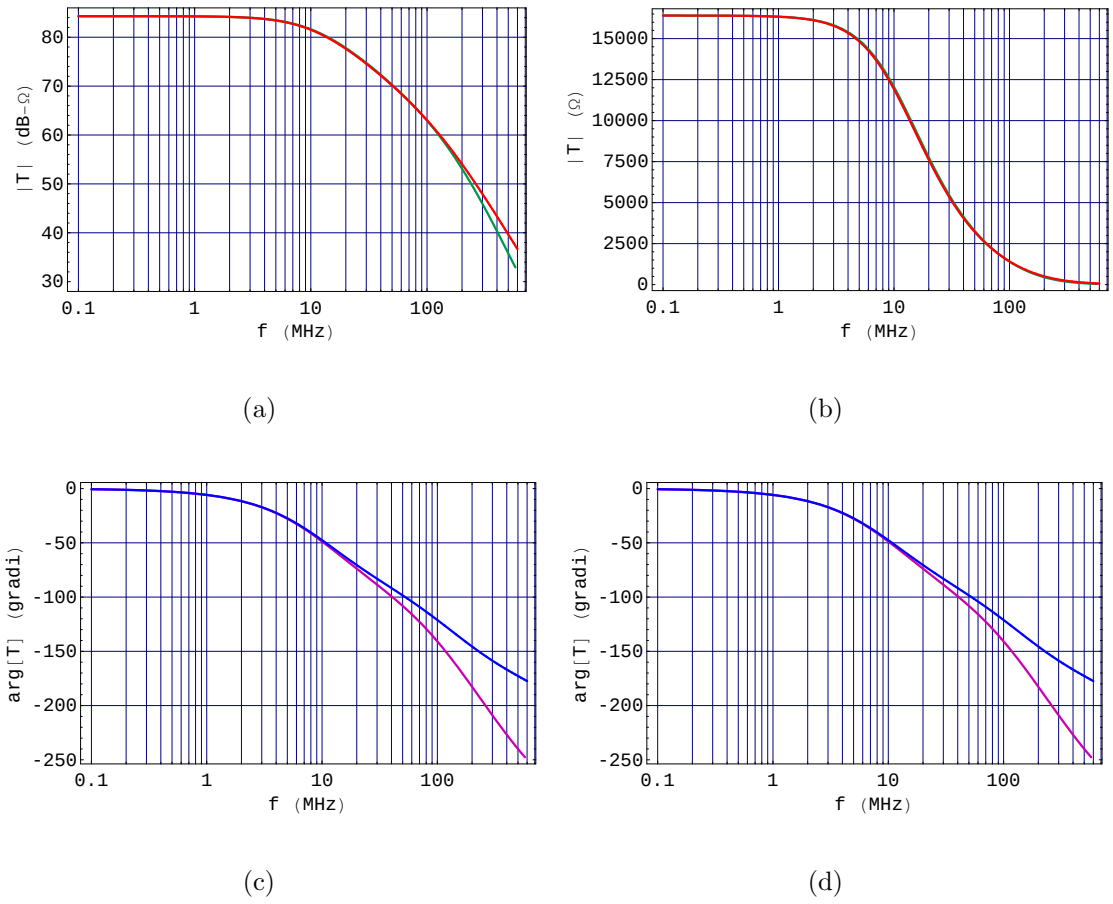


Figure 3.14: (a) Magnitude in dB-Ω, (b) magnitude in Ω and (c), (d) phase in degrees of $T^{\mathrm{I}}(j\omega)$ versus frequency (*Red* and *blue* lines: analytical model. *Green* and *purple* lines: transistor-level model).

Finally, the effect of the two negative real poles as well as the positive real zero on the magnitude of the transfer function can be understood from a graphical standpoint by inspecting Fig. 3.15 which shows the magnitude of $T^{\mathrm{I}}(s)$ as a function of σ and ω.

The two negative real poles produce two very strong peaks (approaching infinity) in the magnitude of $T^{\mathrm{I}}(s)$ at $(\sigma = p_1, Log[f] \rightarrow -\infty)$ and $(\sigma = p_2, Log[f] \rightarrow -\infty)$. Similarly the positive zero produces a peak at $(\sigma = z_1, Log[f] \rightarrow -\infty)$. These peaks give rise to the particular shape of the magnitude of $T^{\mathrm{I}}(s)$ in the range of freqencies illustrated in Fig. 3.15. We can also point out that the section obtained by setting $\sigma = 0$ agrees exactly with the curve shown in Fig. 3.14(a).

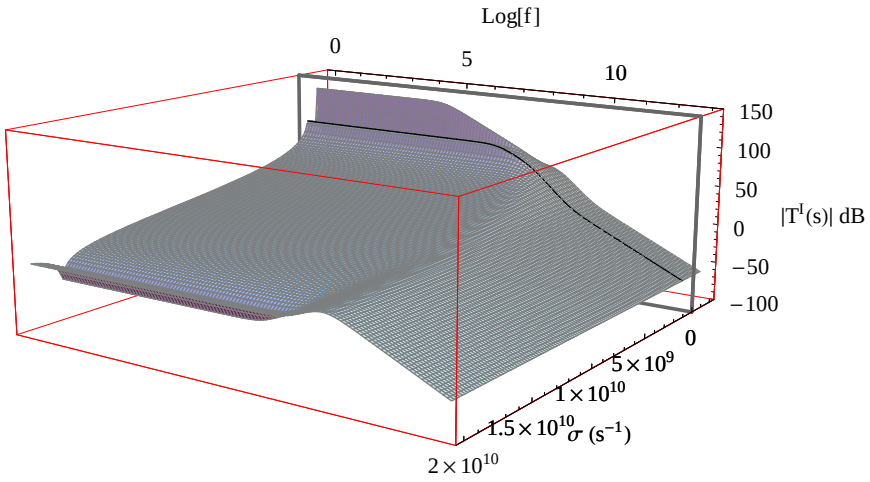


Figure 3.15: Magnitude of $T^{\mathrm{I}}(s)$ as a function of σ and ω and the section obtained by setting $\sigma = 0$ (black line).

Input Impedance

Let us refer to the small-signal equivalent circuit of Fig. 3.16 in order to find its input impedance. For purposes of our analysis the current source I_{in} can be thought of as the test current source required to perform the calculation and the voltage V_{in} as the voltage drop across it.

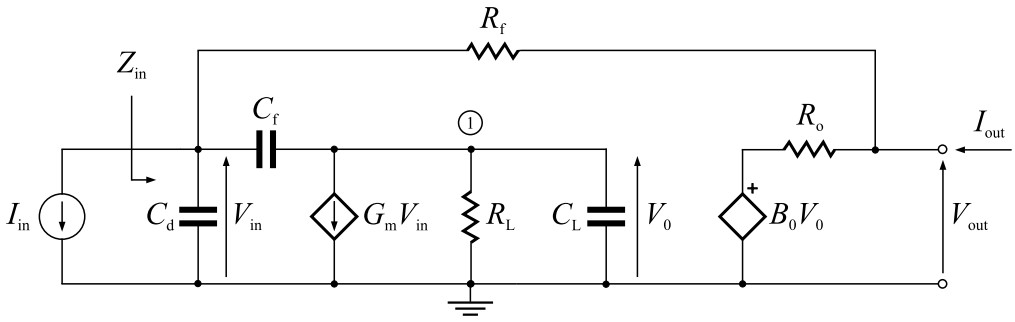


Figure 3.16: Small-signal equivalent circuit of a CSA including a feedback resistance R_{f} and a voltage buffer B_0.

Thus, solving (3.22) by assuming $I_{\mathrm{t}} = -I_{\mathrm{in}}$, $V_{\mathrm{t}} = V_{\mathrm{in}}$ and $I_{\mathrm{out}} = 0$ gives

$$Z^{\mathrm{I}}_{\mathrm{in}}(s) = \left.\frac{V_{\mathrm{in}}}{-I_{\mathrm{in}}}\right|_{I_{\mathrm{out}}=0} = \frac{V_{\mathrm{t}}}{I_{\mathrm{t}}} = \frac{(R_{\mathrm{f}} + R_{\mathrm{o}})\,[1 + R_{\mathrm{L}}\,(C_{\mathrm{f}} + C_{\mathrm{L}})\,s]}{d_0 + d_1\,s + d_2\,s^2} \tag{3.49}$$

The magnitude and phase of $Z_{\text{in}}^{\text{I}}(s)\,|_{s=j\omega}$ are shown in Fig. 3.17.

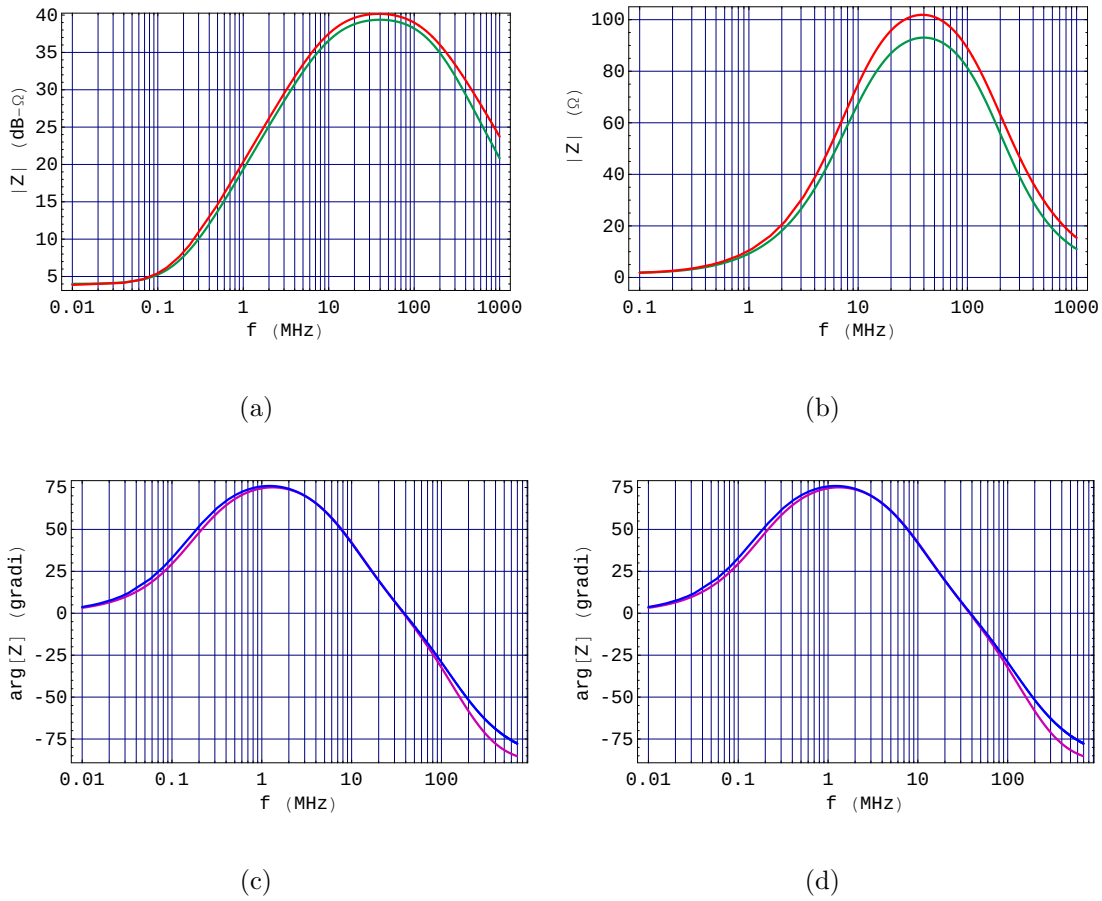


Figure 3.17: (a) Magnitude in dB-Ω, (b) magnitude in Ω and (c), (d) phase in degrees of $Z_{\text{in}}^{\text{I}}(j\omega)$ versus frequency (*Red* and *blue* lines: analytical model. *Green* and *purple* lines: transistor-level model).

The denominator of (3.49) is the same as that of the transfer function, which implies that the coefficients involved are still given by (3.41) as well as the poles by (3.44) and (3.45), as discussed in the previous paragraph.

Equation (3.49) also shows that the input impedance has a negative real zero at low frequency whose magnitude can be estimated by substituting usual parameter values, to give

$$|\, z_1 \,| = \frac{1}{R_{\text{L}}\,(C_{\text{f}} + C_{\text{L}})} \simeq 948.76 \times 10^3\,\text{s}^{-1} \;\Rightarrow\; 151\,\text{kHz} \tag{3.50}$$

In order to gain an insight into the frequency behavior of the input impedance whose value must be set with particular care as will be explained later, let us perform a simpified analysis of equation (3.49) by varying the frequency.

Assuming $R_\mathrm{o} \simeq 0$ and $B_0 \simeq 1$ (ideal voltage buffer) as well as $G_\mathrm{m}\, R_\mathrm{L} \gg 1$ gives

$$Z_\mathrm{in}^\mathrm{I}(s) \simeq \frac{R_\mathrm{f}\ [1 + R_\mathrm{L}\ (C_\mathrm{f} + C_\mathrm{L})\ s]}{\tilde{d}_0 + \tilde{d}_1\, s + \tilde{d}_2\, s^2} \tag{3.51}$$

where

$$\begin{cases} \tilde{d}_0 = G_\mathrm{m}\, R_\mathrm{L} & (\simeq 13140) \\ \tilde{d}_1 = R_\mathrm{f}\, C_\mathrm{f}\, G_\mathrm{m}\, R_\mathrm{L} + R_\mathrm{f}\, C_\mathrm{d} + R_\mathrm{L}\, C_\mathrm{L} & (\simeq 169.1\,\mu\mathrm{s} + 164.1\,\mathrm{ns} + 345.2\,\mathrm{ns}) \\ \tilde{d}_2 = R_\mathrm{f}\, R_\mathrm{L}\ (C_\mathrm{d}\, C_\mathrm{f} + C_\mathrm{d}\, C_\mathrm{L} + C_\mathrm{f}\, C_\mathrm{L}) & \left(\simeq 0.177\,(\mu\mathrm{s})^2\right) \end{cases} \tag{3.52}$$

Further assuming that $R_\mathrm{f}\, C_\mathrm{f}\, G_\mathrm{m}\, R_\mathrm{L}$ dominates in $\tilde{d}_1$ (which is true in the case under examination) leads us to write

$$Z_\mathrm{in}^\mathrm{I}(s) \simeq \frac{R_\mathrm{f}\ [1 + R_\mathrm{L}\ (C_\mathrm{f} + C_\mathrm{L})\ s]}{(G_\mathrm{m}\, R_\mathrm{L}) + (R_\mathrm{f}\, C_\mathrm{f}\, G_\mathrm{m}\, R_\mathrm{L})\ s + [R_\mathrm{f}\, R_\mathrm{L}\ (C_\mathrm{d}\, C_\mathrm{f} + C_\mathrm{d}\, C_\mathrm{L} + C_\mathrm{f}\, C_\mathrm{L})]\ s^2} \tag{3.53}$$

Thus in the limit as $s \to 0$ we have

$$Z_\mathrm{in}^\mathrm{I}(0) \simeq \frac{R_\mathrm{f}}{G_\mathrm{m}\, R_\mathrm{L}} (\simeq 1.25\,\Omega) \tag{3.54}$$

which is in exact agreement with the fact that the circuit under consideration is a transresistance amplifier at low frequency.

In fact such an amplifier can be thought of as consisting of a basic amplifier whose voltage gain is A_v and a feedback resistance R_f connected around this amplifier.

It can be shown that the input impedance of this simplified configuration is

$$R_\mathrm{in} = \frac{R_\mathrm{f}}{(1 - A_\mathrm{v})} \tag{3.55}$$

Thus, since the voltage gain of the basic amplifier is $A_\mathrm{v} = -G_\mathrm{m}\, R_\mathrm{L}$ in the case under examination, we have

$$R_\mathrm{in} = \frac{R_\mathrm{f}}{(1 + G_\mathrm{m}\, R_\mathrm{L})} \simeq \frac{R_\mathrm{f}}{G_\mathrm{m}\, R_\mathrm{L}} \tag{3.56}$$

which is the same result as in (3.54).

As $\mid s \mid$ is increased from zero, the frequency reaches a value such that

$$R_\mathrm{L}\ (C_\mathrm{f} + C_\mathrm{L})\ \mid s \mid = 1 \quad \Rightarrow \quad \mid s \mid = \frac{1}{R_\mathrm{L}\ (C_\mathrm{f} + C_\mathrm{L})} \equiv \mid z_1 \mid \tag{3.57}$$

which represents the frequency of the zero of the input impedance.

Increasing the frequency above this value allows us to approximate the numerator of (3.53) by dropping the constant "1" as well as the denominator by dropping the term $[R_f\, R_L\, (C_d\, C_f + C_d\, C_L + C_f\, C_L)]\; s^2$ to give

$$Z_{in}^{I}(s) \simeq \frac{R_f\, R_L\, (C_f + C_L)\; s}{(G_m\, R_L) + (R_f\, C_f\, G_m\, R_L)\; s} \qquad |\, z_1\, | < |\, s\, | \leq |\, p_1\, | \tag{3.58}$$

which allows us to estimate the frequency at which

$$R_f\, C_f\, G_m\, R_L\; |\, s\, | = G_m\, R_L \quad \Rightarrow \quad |\, s\, | = \frac{1}{R_f\, C_f} \equiv |\, p_1\, | \tag{3.59}$$

which represents the frequency of the dominant pole of the input impedance.

Now, further increasing the frequency above $|\, p_1\, |$ allows us to drop the term $G_m\, R_L$ and assuming that the term $[R_f\, R_L\, (C_d\, C_f + C_d\, C_L + C_f\, C_L)]\; s^2$ is still negligible gives

$$Z_{in}^{I}(s) \simeq \frac{R_f\, R_L\, (C_f + C_L)\; s}{R_f\, C_f\, G_m\, R_L\, s} = \frac{1}{G_m}\, \frac{C_f + C_L}{C_f}\, (\simeq 102.3\ \Omega) \qquad |\, s\, | > |\, p_1\, | \tag{3.60}$$

which yields the approximated amplitude of the peak shown in Fig. 3.17(b).

By further inspecting this figure we can see that the above value experiences no significant variations over a fairly wide range of frequencies corresponding to those of the signal.

Moreover equation (3.60) can be very useful from a design point of view since it allows us to set properly the value of the involved circuit components in order to obtain the desired impedance value.

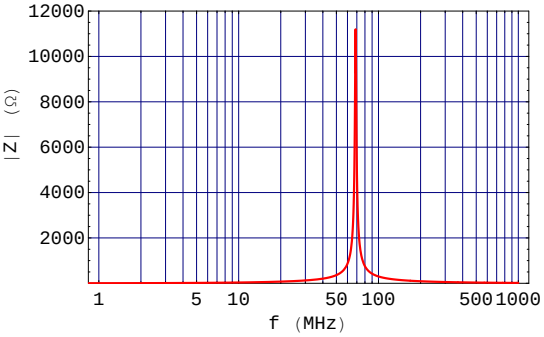


Figure 3.18: Magnitude in Ω of the input impedance when $C_f = 0$.

Finally let us note that the feedback capacitance C_f also performs the function of limiting the peak amplitude of the input impedance, as shown in Fig. 3.18 which displays the shape of the input impedance in the limit as $C_f \to 0$.

Moving on with our analysis we can write

$$Z_{in}^{I}(s) \simeq \frac{R_f\, R_L\, (C_f + C_L)\; s}{(R_f\, C_f\, G_m\, R_L)\; s + [R_f\, R_L\, (C_d\, C_f + C_d\, C_L + C_f\, C_L)]\; s^2} \qquad |\, s\, | \lesssim |\, p_2\, | \tag{3.61}$$

which allows us to estimate the frequency at which

$$(R_{\mathrm{f}}\, C_{\mathrm{f}}\, G_{\mathrm{m}}\, R_{\mathrm{L}})\; s = [R_{\mathrm{f}}\, R_{\mathrm{L}}\; (C_{\mathrm{d}}\, C_{\mathrm{f}} + C_{\mathrm{d}}\, C_{\mathrm{L}} + C_{\mathrm{f}}\, C_{\mathrm{L}})]\; s^2 \tag{3.62}$$

namely

$$\mid s \mid = \frac{C_{\mathrm{f}}\, G_{\mathrm{m}}}{C_{\mathrm{f}}\; (C_{\mathrm{d}} + C_{\mathrm{L}}) + C_{\mathrm{d}}\, C_{\mathrm{L}}} \equiv \mid p_2 \mid \tag{3.63}$$

which represents the frequency of the non-dominant pole of the input impedance. Finally in the limit as $\mid s \mid \rightarrow \infty$ we can write

$$Z^{\mathrm{I}}_{\mathrm{in}}\,(s) \simeq \frac{R_{\mathrm{f}}\, R_{\mathrm{L}}\; (C_{\mathrm{f}} + C_{\mathrm{L}})\; s}{[R_{\mathrm{f}}\, R_{\mathrm{L}}\; (C_{\mathrm{d}}\, C_{\mathrm{f}} + C_{\mathrm{d}}\, C_{\mathrm{L}} + C_{\mathrm{f}}\, C_{\mathrm{L}})]\; s^2} \simeq \frac{1}{s\, C_{\mathrm{d}}} \qquad \mid s \mid \rightarrow \infty \tag{3.64}$$

by assuming $C_{\mathrm{f}}\, C_{\mathrm{L}}$ $\left(\simeq 0.3\,(\mathrm{pF})^2\right)$ negligible with respect to $C_{\mathrm{d}}\, C_{\mathrm{f}}$ $\left(\simeq 7.8\,(\mathrm{pF})^2\right)$ and $C_{\mathrm{d}}\, C_{\mathrm{L}}$ $\left(\simeq 3.82\,(\mathrm{pF})^2\right)$.

Let us note that all the foregoing results agrees exactly with those obtained in the previous sections by following a different approach.

As mentioned earlier, the value of the input impedance turns out to be particularly significant in order to design the first stage of the full circuit since it must collect the fast current signal coming from the PMTs and travelling down a transmission line exhibiting its own characteristic impedance (whose value is $100\,\Omega$).

In addition, the low value of the input impedance strongly reduces the circuit sensitivity to pick-up phenomenon.

Thus, it is apparent that the signal transmission can be greatly improved avoiding the impedance mismatch between the line and the load which is just represented by the input impedance of the first stage. This mismatch may cause reflection of part of the incident wave at the receiving ends of the line.

To obtain a quantitative understanding of the preceding considerations we will present some interesting relationships related to the transmission lines.

Some common types of transmission lines can be a two-wire line, a parallel-strip line or a coaxial cable.

Let us consider for simplicity two parallel conductors connecting a generator to a load. The signal travelling down the line cannot reach the load immediately because it propagates at a finite velocity depending on the medium surrounding the conductors.

For signals varying sinusoidally with time, the distance covered in a cycle is

$$\lambda = v\,T = \frac{v}{f} \tag{3.65}$$

where we can assume that v is nearly the velocity of light in free space for air-insulated lines, namely $3 \times 10^8\,\mathrm{m\,s^{-1}}$.

The key point here is that transmission-line theory must be used when the length of the line is comparable to $\lambda/4$.

It should be pointed out that also the distance between conductors plays an important role in the allowable transmission modes of the travelling wave. The most important mode is termed *principal mode* which means that the electric and magnetic fields are perpendicular to each other and to the direction of the conductors. Higher modes can exist when the frequency is so high that $\lambda/4$ is comparable to the distance between conductors.

The most important constants of a transmission line are its distributed inductance ($\tilde{L}$) and capacitance ($\tilde{C}$) as well as its conductor resistance per unit length ($\tilde{R}$) and insulator conductance per unit length ($\tilde{G}$) which model the non-ideal behavior of conductors and insulators. Although these line constants are distributed along the line, we can approximately allow for their effect by applying lumped-constant theory to the several short sections of length Δz that the line can be thought to consist of.

Thus, applying KVL to the short line section shown in Fig. 3.19(a) by assuming that $v = v\,(z,t)$ and $i = i\,(z,t)$ represent the instantaneous voltage and current of the line, gives

$$v - (v + \Delta v) = -\Delta v = -\frac{\partial v}{\partial z}\,\Delta z = \left(\tilde{R}\Delta z\right) i + \left(\tilde{L}\Delta z\right)\frac{\partial i}{\partial t} \tag{3.66}$$

and applying KCL to the short line section shown in Fig. 3.19(b) gives

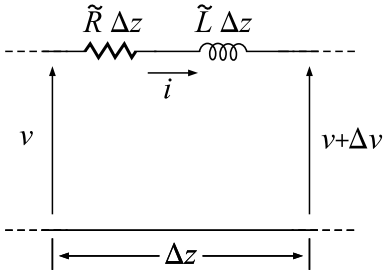
$$i - (i + \Delta i) = -\Delta i = -\frac{\partial i}{\partial z}\,\Delta z = \left(\tilde{G}\Delta z\right) v + \left(\tilde{C}\Delta z\right)\frac{\partial v}{\partial t} \tag{3.67}$$

Finally, dividing (3.66) and (3.67) by Δz yields

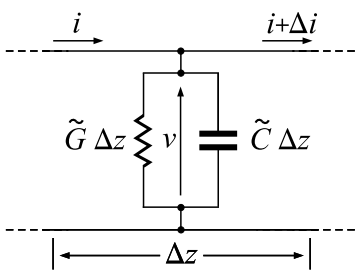
$$-\frac{\partial v}{\partial z} = \tilde{R}\,i + \tilde{L}\,\frac{\partial i}{\partial t} \tag{3.68}$$

and

$$-\frac{\partial i}{\partial z} = \tilde{G}\,v + \tilde{C}\,\frac{\partial v}{\partial t} \tag{3.69}$$



(a) Modelling of the inductive behavior of a short section Δz with loss.



(b) Modelling of the capacitive behavior of a short section Δz with loss.

Figure 3.19: Approximate representation of a short section Δz of a transmission line.

The foregoing equations have been derived under the assumption that the line is a *uniform line*, which means the constants $\tilde{R}$, $\tilde{L}$, $\tilde{G}$, $\tilde{C}$ experience no variations for varying z and t.

Now, by assuming for simplicity that the line is lossless ($\tilde{R} = \tilde{G} = 0$), deriving (3.68), (3.69) and rearranging gives

$$\frac{\partial^2 v}{\partial z^2} - \tilde{L}\,\tilde{C}\,\frac{\partial^2 v}{\partial t^2} = 0 \tag{3.70}$$

and

$$\frac{\partial^2 i}{\partial z^2} - \tilde{L}\,\tilde{C}\,\frac{\partial^2 i}{\partial t^2} = 0 \tag{3.71}$$

which are one-dimensional forms of the wave equation whose solutions, letting $c = 1/\sqrt{\tilde{L}\,\tilde{C}}$ are known to be of the form

$$v\,(z,\,t) = v^{+}\,(z - c\,t) + v^{-}\,(z + c\,t) \tag{3.72}$$

and

$$i\,(z,\,t) = i^{+}\,(z - c\,t) + i^{-}\,(z + c\,t) \tag{3.73}$$

where v^+ and i^+ represent the incident voltage and current wave whereas v^- and i^- the reflected voltage and current wave.

By considering at first only the incident wave and letting $\xi = z - c\,t$, we have from (3.68) (with $\tilde{R} = 0$)

$$\frac{d}{d\xi}\left(v^{+} - \tilde{L}\,c\,i^{+}\right) = 0 \tag{3.74}$$

and thus

$$v^+ = \tilde{L}\, c\, i^+ + \text{constant} \tag{3.75}$$

Neglecting the constant gives

$$v^+ = \tilde{L}\, c\, i^+ = \sqrt{\frac{\tilde{L}}{\tilde{C}}}\, i^+ = R_0\, i^+ \tag{3.76}$$

The important quantity

$$R_0 = \sqrt{\frac{\tilde{L}}{\tilde{C}}} \tag{3.77}$$

is termed *characteristic resistance* of the line.

In a similar way we find

$$v^- = -R_0\, i^- \tag{3.78}$$

Hence

$$v\,(z,\, t) = v^+\,(z - c\,t) + v^-\,(z + c\,t) \tag{3.79}$$

and

$$R_0\, i\,(z,\, t) = v^+\,(z - c\,t) - v^-\,(z + c\,t) \tag{3.80}$$

Finally we are able to show that a line terminated in its characteristic impedance (*correctly terminated*) is a line with no reflections. In fact, assuming $z = 0$ is the point where the load is connected to the line provides the constraint

$$v\,(0,\, t) = R_0\, i\,(0,\, t) \tag{3.81}$$

which implies

$$v\,(0,\, t) = v^+\,(0,\, t)\,, \qquad i\,(0,\, t) = i^+\,(0,\, t) \tag{3.82}$$

Thus, for all z,

$$v\,(z,\, t) = v^+\,(z - c\,t)\,, \qquad R_0\, i\,(z,\, t) = v^+\,(z - c\,t) \tag{3.83}$$

Output Impedance

Let us again refer to the small-signal equivalent circuit of Fig. 3.10 in order to find its output impedance. Let I_{out} represent the current that flows in the output node when the output is driven by a voltage V_{out}.

Thus, solving (3.22) by assuming $I_{\text{t}} = I_{\text{out}}$, $V_{\text{t}} = V_{\text{out}}$ and $I_{\text{in}} = 0$ gives

$$Z_{\text{out}}^{\text{I}}(s) = \left.\frac{V_{\text{out}}}{I_{\text{out}}}\right|_{I_{\text{in}}=0} = \frac{V_{\text{t}}}{I_{\text{t}}} = \frac{R_{\text{o}}\,(1 + n_1\,s + n_2\,s^2)}{d_0 + d_1\,s + d_2\,s^2} \tag{3.84}$$

where the coefficients of s and s^2 in the numerator are

$$\begin{cases} n_1 = R_{\text{f}}\,[C_{\text{d}} + C_{\text{f}}\,(1 + G_{\text{m}}\,R_{\text{L}})] + R_{\text{L}}\,(C_{\text{f}} + C_{\text{L}}) \\ n_2 = R_{\text{f}}\,R_{\text{L}}\,(C_{\text{d}}\,C_{\text{f}} + C_{\text{d}}\,C_{\text{L}} + C_{\text{f}}\,C_{\text{L}}) \end{cases} \tag{3.85}$$

and the coefficients in the denominator are still given by (3.41).

Hence, the poles of the output impedance are the same as those of the transfer function and the input impedance, which implies that their estimates too are still given by (3.44) and (3.45).

By concentrating now on the quadratic term in the numerator of (3.84) we can easily write it as

$$\left(1 - \frac{s}{z_1}\right)\left(1 - \frac{s}{z_2}\right) = 1 - s\left(\frac{1}{z_1} + \frac{1}{z_2}\right) + \frac{s^2}{z_1\,z_2} \tag{3.86}$$

where z_1 and z_2 are the zeros of the output impedance.

Then, assuming they are real and widely separated (which is true in the case under consideration) gives

$$1 - s\left(\frac{1}{z_1} + \frac{1}{z_2}\right) + \frac{s^2}{z_1\,z_2} \simeq 1 - \frac{s}{z_1} + \frac{s^2}{z_1\,z_2} \tag{3.87}$$

where z_2 is assumed to have the largest magnitude value.

By equating the coefficients in (3.87) and in the numerator of (3.84), we find

$$z_1 \approx -\frac{1}{R_{\text{f}}\,[C_{\text{d}} + C_{\text{f}}\,(1 + G_{\text{m}}\,R_{\text{L}})] + R_{\text{L}}\,(C_{\text{f}} + C_{\text{L}})} \tag{3.88}$$

and

$$z_2 \approx -\frac{R_{\text{f}}\,[C_{\text{d}} + C_{\text{f}}\,(1 + G_{\text{m}}\,R_{\text{L}})] + R_{\text{L}}\,(C_{\text{f}} + C_{\text{L}})}{R_{\text{f}}\,R_{\text{L}}\,(C_{\text{d}}\,C_{\text{f}} + C_{\text{d}}\,C_{\text{L}} + C_{\text{f}}\,C_{\text{L}})} \tag{3.89}$$

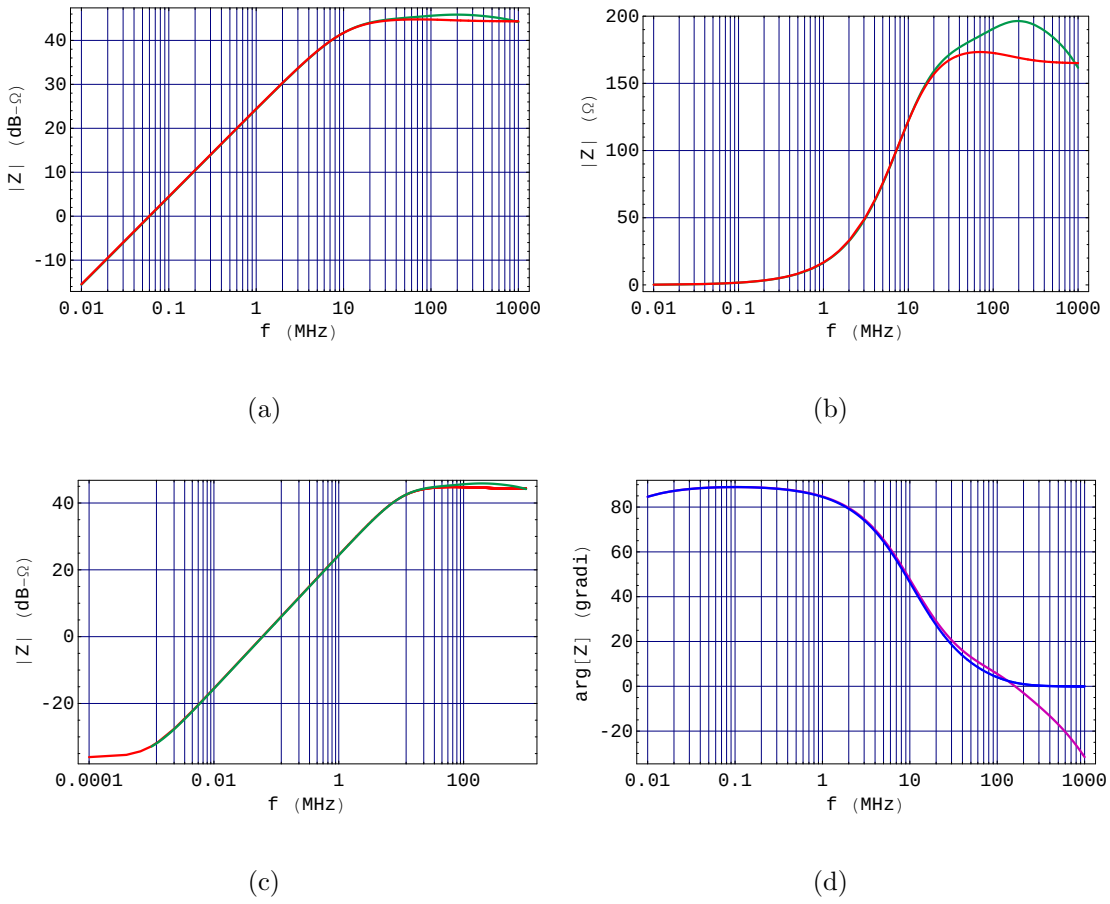


Figure 3.20: (a) Magnitude in dB-Ω, (b) magnitude in Ω, (c) magnitude in dB-Ω showing the low-frequency zero and (d) phase in degrees of $Z^{\mathrm{I}}_{\mathrm{out}}(j\omega)$ versus frequency (*Red* and *blue* lines: analytical model. *Green* and *purple* lines: transistor-level model).

from which we obtain, in our case,

$$\mid z_1 \mid \simeq 5.87 \times 10^3\,\mathrm{s}^{-1} \;\Rightarrow\; 934.4\,\mathrm{Hz} \tag{3.90}$$

and

$$\mid z_2 \mid \simeq 960.23 \times 10^6\,\mathrm{s}^{-1} \;\Rightarrow\; 152.82\,\mathrm{MHz} \tag{3.91}$$

It may also be interesting to analyse the behavior of the output impedance in the limit as $s \to 0$ and $s \to \infty$.

By referring to equation (3.84) we obtain respectively

$$Z^{\mathrm{I}}_{\mathrm{out}}(0) = \frac{R_{\mathrm{o}}}{1 + G_{\mathrm{m}}\,R_{\mathrm{L}}}\,(\simeq 0.0127\,\Omega \;\Rightarrow\; -37.9\,\mathrm{dB}\text{-}\Omega) \tag{3.92}$$

and

$$Z^{\mathrm{I}}_{\mathrm{out}}(s) = \frac{R_{\mathrm{o}}\,R_{\mathrm{f}}}{R_{\mathrm{o}}+R_{\mathrm{f}}} = R_{\mathrm{o}} \parallel R_{\mathrm{f}}\,(\simeq 164.8\,\Omega \Rightarrow 44.34\ \text{dB-}\Omega) \qquad s \to \infty \tag{3.93}$$

The preceding analysis can be verified by direct inspection of Fig. 3.20 which shows the magnitude and phase of $Z^{\mathrm{I}}_{\mathrm{out}}(s)\,|_{s=j\omega}$.

In particular, Fig. 3.20(c) displays the effect of the low-frequency zero whereas Fig. 3.20(a) and Fig. 3.20(b) allow us to see that the non-dominant real pole p_2 is so near to the real zero z_2 (as predictable by the comparison of (3.91) and (3.45)) that an almost total compensation of their effect occurs in the magnitude of $Z^{\mathrm{I}}_{\mathrm{out}}(j\omega)$ causing its shape to be very similar to that of a function having one low-frequency zero and one pole only.

Finally, it should be pointed out that at high frequencies the behavior of the output impedance predicted by our analytical model deviates from the real one because our model does not allow for all the parasitic capacitances of the circuit.

In particular, the output impedance of the buffer has been modelled by means of a resistor suitable for representing the behavior of the output impedance only over a frequency range which certainly does not include high or very high frequencies.

Reverse Transmission

By referring again to the small-signal equivalent circuit of Fig. 3.10 let us now determine the circuit reverse transimpedance which allows us to estimate whether and to what extent a current signal can propagate back from the output to the input of our amplifier.

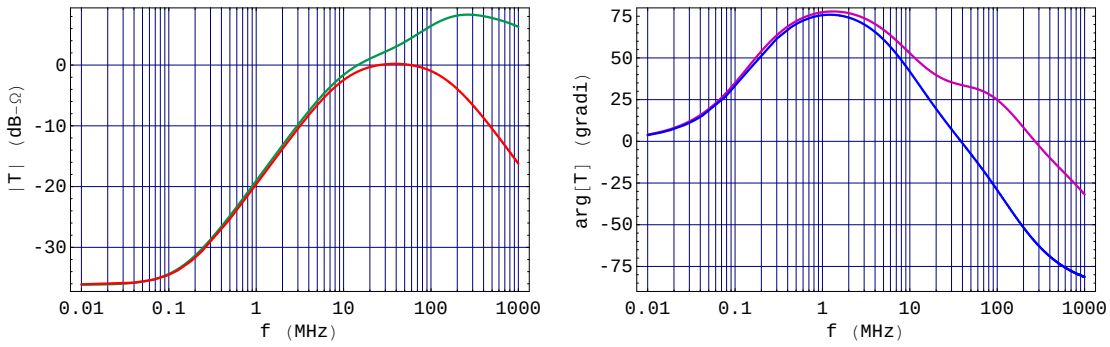
Thus, solving (3.22) for V_{in} by assuming $I_{\mathrm{in}} = 0$ and rearranging gives

$$T^{\mathrm{I}}_{\mathrm{rev}}(s) = \left.\frac{V_{\mathrm{in}}}{I_{\mathrm{out}}}\right|_{I_{\mathrm{in}}=0} = \frac{R_{\mathrm{o}}\,[1+R_{\mathrm{L}}\,(C_{\mathrm{f}}+C_{\mathrm{L}})\,s]}{d_0+d_1\,s+d_2\,s^2} \tag{3.94}$$

Equation (3.94) shows that the reverse transfer function has a negative real zero at low frequency whose magnitude is

$$|\,z_1\,| = \frac{1}{R_{\mathrm{L}}\,(C_{\mathrm{f}}+C_{\mathrm{L}})} \simeq 948.76\times 10^3\,\mathrm{s}^{-1} \Rightarrow 151\,\mathrm{kHz} \tag{3.95}$$

as well as the same two poles as the forward transfer function, still given by (3.44) and (3.45).



(a) (b)

Figure 3.21: (a) Magnitude (dB-Ω) and (b) phase (degrees) of $T^{\mathrm{I}}_{\mathrm{rev}}(j\omega)$ versus frequency.

Figure 3.21 shows the magnitude and phase of $T^{\mathrm{I}}_{\mathrm{rev}}(s)\,|_{s=j\omega}$. The considerations stated in the preceding subsection about the suitability of our model for representing the high-frequency behavior of the output impedance with adequate accuracy, still apply in this case.

However it should be highlighted that the order of magnitude of the reverse transmission is very small compared to that of the forward signal transmission, which suggests that we could consider the amplifier *unilateral*, as it often occurs in many practical cases.

3.1.5 Pulse Response

Let us consider the circuit response to a small input current pulse $i_{in}(t)$ carrying a charge $Q = 4\,\mathrm{fC}$, as shown in Fig. 3.22(a).

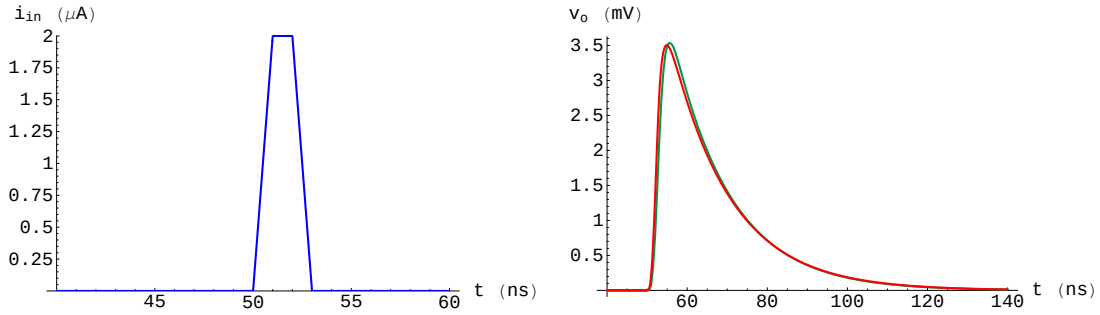
A detailed analysis of the theoretical steps which lead us to find the circuit time response by using Laplace transform has already been performed in subsection 3.1.1 and the results obtained there can be used here.

Thus, from (3.9) by letting $H(s) = T^{\mathrm{I}}(s)$ we have

$$V^{\mathrm{I}}_{\mathrm{out}}(s) = T^{\mathrm{I}}(s)\; I_{\mathrm{in}}(s) \tag{3.96}$$

where $T^{\mathrm{I}}(s)$ is given in (3.40).

Taking the inverse Laplace transform of (3.96) leads to the graphic result shown in Fig. 3.22(b). From an examination of the graph we can appreciate the exact agreement between the response that our model predicts and its real shape.



(a) Input current pulse $i_{in}\,(t)$.

(b) Circuit response $v_{out}\,(t)$ (*Red* line: analytical model. *Green* line: transistor-level model).

Figure 3.22: Pulse response of the circuit shown in Fig. 3.9.

3.1.6 The Actual Circuit and the Parameter Estimate

In this subsection the actual circuit schematic diagram of the first stage of the full front end circuit will be taken into consideration in order to obtain an understanding of its behavior in relation to the model used for representing it and widely described earlier in this chapter. In particular, the relationships used for estimating the value of the small-signal parameters involved in the equations given so far will be shown in detail.

By inspecting Fig. 3.23 we can see that a cascode amplifier (M_1, M_2) with a p-channel MOS cascode current-mirror load (M_3, M_4) is at the heart of the scheme.

This amplifier, together with the voltage buffer M_9, can be thought of as the basic amplifier involved in the feedback loop whose feedback network consists of the resistor R_f and the capacitor C_f.

The cascode configuration is made up of a common-source amplifier stage followed by a common-gate stage and is widely used because it increases the amplifier output resistance and improves its frequency behavior with respect to a single-transistor amplifier stage.

In our case the cascode connection allows us to achieve, from a small-signal standpoint, a very high load resistance. This is represented by the output resistance of the current mirror in parallel with the output resistance of the block consisting of M_1 and M_2. Hence it is apparent that M_2 performs the function of increasing

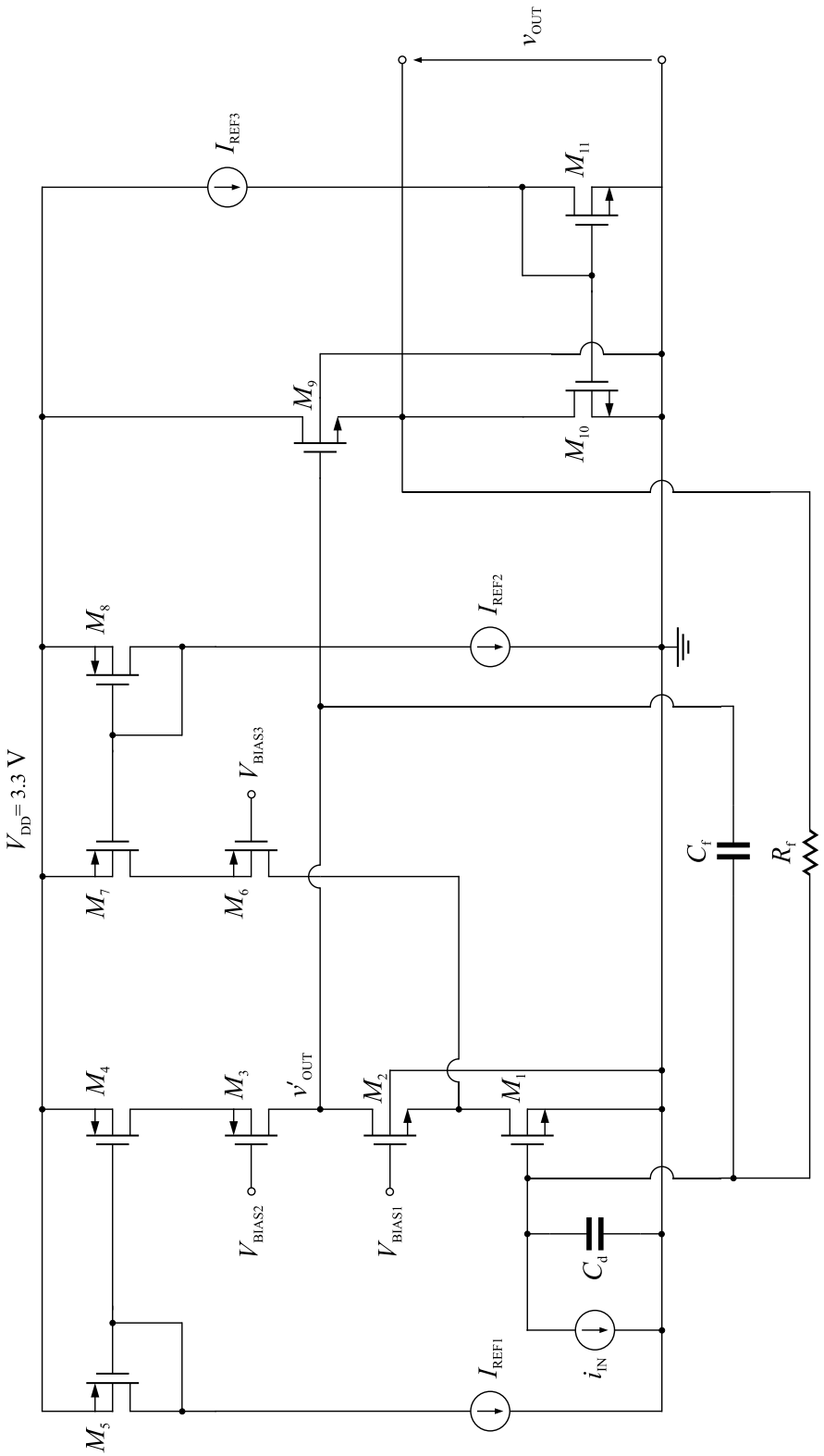


Figure 3.23: Circuit diagram of the first stage.

the output resistance of this block with the only purpose of avoiding its becoming significantly lower than that of the current mirror.

In fact the parallel combination of two resistors results in a resistor whose value is always lower than the smaller value of the two resistors.

Futhermore, cascoding M_1 provides only a small decrease in the transconductance of the basic amplifier, as we will show later.

Let us now note that an additive biasing current branch consisting of a p-channel MOS cascode current-mirror (M_6, M_7, M_8) causes an additional bias current I_{REF2} to flow in M_1 only, to increase its small-signal transconductance (which is dirctly proportional to its bias current since M_1 operates in *weak inversion*) without decreasing the output resistances of M_2, M_3 and M_4 (which are on the other hand inversely proportional to the bias current). In fact such a decrease would occur if we simply increased I_{REF1}.

It should also be pointed out that M_6, which acts as cascode for M_7, has been added in order to increase the output resistance of the simple current mirror (M_7, M_8) in order that this resistance does not decrease the output resistance of M_1 with which it turns out to be in parallel.

Finally, the transistor M_9 together with its active load M_{10} is used in the common-drain configuration and acts as a voltage buffer whose function has alredy been explained in subsection 3.1.2.

Let us now establish a connection between the small-signal parameters of the circuit model shown in Fig. 3.10 and the small-signal parameters of the transistors involved in the actual circuit diagram of Fig. 3.23.

First, let us consider the amplifier transconductance G_{m}. Let g_{mi}, g_{mbi} and r_{oi} represent the small-signal parameters of the transistor M_{i} with i running from one to eleven.

It can be shown that the cascode configuration (M_1 and M_2) gives

$$G_{\mathrm{m}} = g_{\mathrm{m1}} \left(1 - \frac{1}{1 + (g_{\mathrm{m2}} + g_{\mathrm{mb2}})\, r_{\mathrm{o1}} + \dfrac{r_{\mathrm{o1}}}{r_{\mathrm{o2}}}} \right) \simeq g_{\mathrm{m1}} \tag{3.97}$$

by assuming $(g_{\mathrm{m2}} + g_{\mathrm{mb2}})\, r_{\mathrm{o1}} \gg 1$, which is usually true.

Thus we set

$$G_{\mathrm{m}} = g_{\mathrm{m1}} \tag{3.98}$$

We now focus on the output resistance of a generic cascode amplifier (CS (M_i) – CG (M_j)), namely

$$R_\mathrm{cas}^{(\mathrm{i,j})} = r_\mathrm{oi} + r_\mathrm{oj} + (g_\mathrm{mj} + g_\mathrm{mbj})\, r_\mathrm{oi}\, r_\mathrm{oj} \tag{3.99}$$

Thus, by assuming $r_\mathrm{o1} \parallel R_\mathrm{cas}^{(7,6)} \simeq r_\mathrm{o1}$, we set

$$R_\mathrm{L} = R_\mathrm{cas}^{(1,2)} \parallel R_\mathrm{cas}^{(4,3)} \tag{3.100}$$

By continuing our analysis we find that C_L is given by the sum of some parasitic capacitance and thus we have

$$C_\mathrm{L} = (C_\mathrm{gd2} + C_\mathrm{db2}) + (C_\mathrm{gd3} + C_\mathrm{db3}) + (C_\mathrm{gs9} + C_\mathrm{gd9}) \tag{3.101}$$

Finally, we concentrate on the parameter B_0 representig the small-signal voltage gain of the buffer. In our circuit this buffer is achieved by means of the *source follower* configuration made up of M_9 and its n-channel MOS simple current-mirror load (M_{10}).

It can be shown that

$$B_0 = \frac{g_\mathrm{m9}\, r_\mathrm{o9}}{1 + (g_\mathrm{m9} + g_\mathrm{mb9})\, r_\mathrm{o9} + \dfrac{r_\mathrm{o9}}{r_\mathrm{o10}}} \simeq \frac{g_\mathrm{m9}}{g_\mathrm{m9} + g_\mathrm{mb9}} \tag{3.102}$$

in the limit as $r_\mathrm{o9} \to \infty$ and $r_\mathrm{o10} \to \infty$.

We observe that B_0 is less than unity in the case under consideration because the bulk of M_9 is connected to ground causing v_sb to be nonzero.

The parameter R_o of the buffer turns out to be the output resistance of the *source follower* and is thus given by

$$R_\mathrm{o} = \frac{1}{g_\mathrm{m9} + g_\mathrm{mb9} + \dfrac{1}{r_\mathrm{o9}} + \dfrac{1}{r_\mathrm{o10}}} \simeq \frac{1}{g_\mathrm{m9} + g_\mathrm{mb9}} \tag{3.103}$$

in the limit as $r_\mathrm{o9} \to \infty$ and $r_\mathrm{o10} \to \infty$.

Now, by setting $R_\mathrm{f} = 16.408\,\mathrm{k\Omega}$, $C_\mathrm{f} = 784.32\,\mathrm{fF}$, $C_\mathrm{d} = 10\,\mathrm{pF}$ and the nominal bias currents (I_REF1, I_REF2, I_REF3) we are able to perform a computer simulation to acquire the values of the small-signal parameters listed in Tab. 3.1. By substituting in the preceding equations the values displayed in the table we are able to obtain an adequate estimate of the parameters involved in our analytical model as well as to produce the desired graphical outputs.

	$\mathbf{g_m}$	$\mathbf{g_{mb}}$	$\mathbf{g_{ds}}$ $(\mathbf{r_o^{-1}})$	$\mathbf{C_{gd}}$	$\mathbf{C_{db}}$	$\mathbf{C_{gs}}$
$\mathbf{M_1}$	14.54 mS	4.298 mS	46.49 μS	—	—	—
$\mathbf{M_2}$	5.164 mS	1.213 mS	20.69 μS	45.36 fF	159.9 aF	—
$\mathbf{M_3}$	1.484 mS	378.1 μS	30.72 μS	8.844 fF	47.63 aF	—
$\mathbf{M_4}$	3.87 mS	997.4 μS	48.72 μS	—	—	—
$\mathbf{M_9}$	4.819 mS	1.137 mS	27.91 μS	24.59 fF	—	302.7 fF

Table 3.1: List of small-signal parameters given by computer simulation.

3.2 Second Stage Analysis

In this section we will consider the second stage of our front end circuit. However we will not perform a detailed analysis of the actual circuit which implements this stage in practice.

In fact, our purpose is to obtain a fairly simple model of the whole circuit allowing us to predict its behavior for varying some parameters as well as for introducing some additional stages.

As shown in the schematic diagram of Fig. 3.24, the second stage can be thought of as consisting of two main blocks, namely a basic amplifier (OTA) with its feedback network (R_{sh}, C_{sh}) and a gain stage assumed to have a high output resistance so that it can be represented by a transconductor block.

This block feeds back a signal to the input and represents an active feedback network having a frequency-dependent transfer function $f(s)$. The purpose of this active feedback is to keep the DC output voltage of the circuit V_{OUT} (the *baseline*) approximately equal to the DC reference value V_{ref}.

3.2.1 Frequency Analysis of the Second Stage

Transfer Function

Let us now consider the small-signal equivalent circuit shown in Fig. 3.25 in order to find the ratio $V_{\mathrm{out}}/I_{\mathrm{in}}$. In drawing this simplified equivalent circuit the input and the output impedance of the OTA as well as the input and the output impedance of the transconductor block have been neglected.

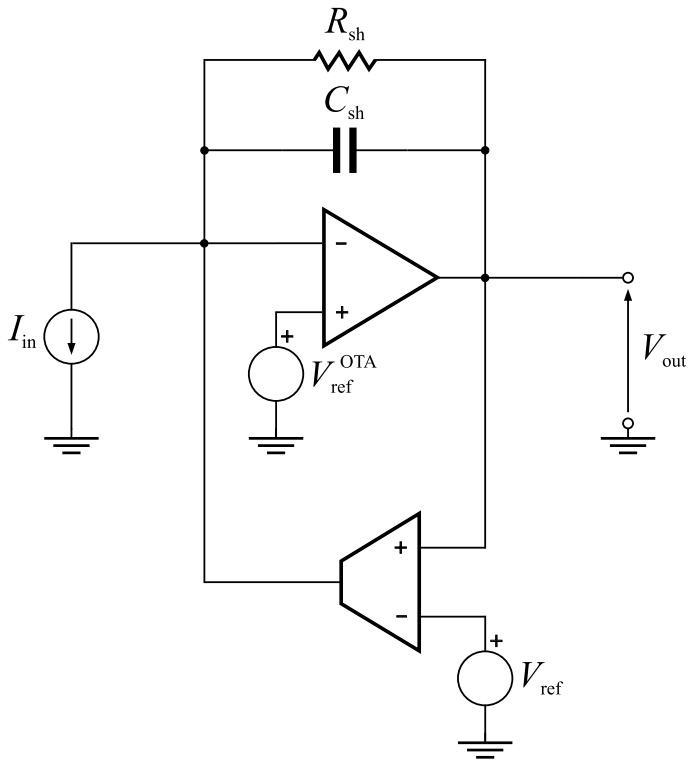


Figure 3.24: Schematic diagram of the second stage.

Thus, by assuming $I_{out} = 0$, from KCL at the input node

$$I_{in} - G_m(s)\, V_{out} + (V_{in} - V_{out}) \left(\frac{1}{R_{sh}} + s\, C_{sh} \right) = 0 \tag{3.104}$$

Since

$$V_{out} = -A_v(s)\, V_{in} \;\Rightarrow\; V_{in} = -\frac{V_{out}}{A_v(s)} \tag{3.105}$$

substituting (3.105) into (3.104) and rearranging gives

$$I_{in} = V_{out} \left[G_m(s) + \left(1 + \frac{1}{A_v(s)} \right) \left(\frac{1}{R_{sh}} + s\, C_{sh} \right) \right] \tag{3.106}$$

and further rearranging yields

$$\left. \frac{V_{out}}{I_{in}} \right|_{I_{out}=0} = \frac{A_v(s)\, R_{sh}}{G_m(s)\, A_v(s)\, R_{sh} + (1 + A_v(s))\, (1 + s\, R_{sh}\, C_{sh})} \tag{3.107}$$

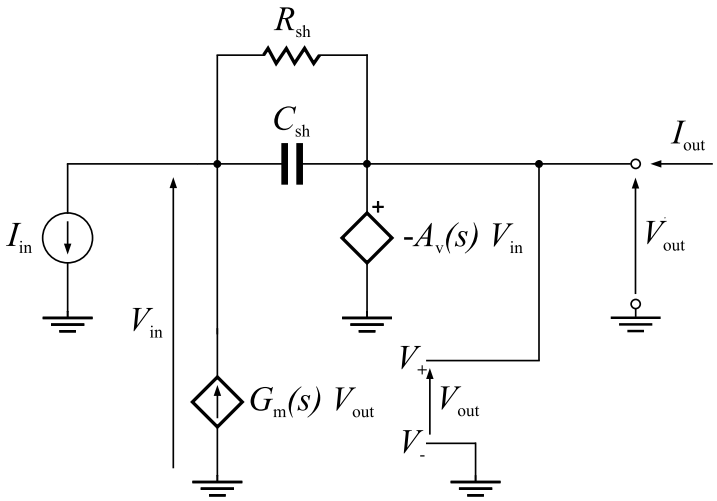


Figure 3.25: Small-signal equivalent circuit of the second stage.

Then, assuming that both $A_{\mathrm{v}}(s)$ and $G_{\mathrm{m}}(s)$ are one-pole transfer functions, namely

$$A_{\mathrm{v}}(s) = \frac{A_{\mathrm{v0}}}{1 + s\,\tau_{\mathrm{OTA}}} \tag{3.108}$$

and

$$G_{\mathrm{m}}(s) = \frac{G_{\mathrm{m0}}}{1 + s\,\tau_{\mathrm{HP}}} \tag{3.109}$$

gives

$$T^{\mathrm{II}}(s) = \left.\frac{V_{\mathrm{out}}}{I_{\mathrm{in}}}\right|_{I_{\mathrm{out}}=0} = \frac{A_{\mathrm{v0}}\,R_{\mathrm{sh}}\,(1 + s\,\tau_{\mathrm{HP}})}{\bar{d}_0 + \bar{d}_1\,s + \bar{d}_2\,s^2 + \bar{d}_3\,s^3} \tag{3.110}$$

where

$$\begin{cases} \bar{d}_0 = 1 + A_{\mathrm{v0}}\,(1 + G_{\mathrm{m0}}\,R_{\mathrm{sh}}) \\ \bar{d}_1 = \tau_{\mathrm{OTA}} + (1 + A_{\mathrm{v0}})\,(\tau_{\mathrm{HP}} + R_{\mathrm{sh}}\,C_{\mathrm{sh}}) \\ \bar{d}_2 = \tau_{\mathrm{OTA}}\,(\tau_{\mathrm{HP}} + R_{\mathrm{sh}}\,C_{\mathrm{sh}}) + (1 + A_{\mathrm{v0}})\,R_{\mathrm{sh}}\,C_{\mathrm{sh}}\,\tau_{\mathrm{HP}} \\ \bar{d}_3 = R_{\mathrm{sh}}\,C_{\mathrm{sh}}\,\tau_{\mathrm{HP}}\,\tau_{\mathrm{OTA}} \end{cases} \tag{3.111}$$

It is apparent from (3.110) that the transfer function has three poles and one zero. The magnitude of this negative real zero is given by

$$|\,z_1\,| = \frac{1}{\tau_{\mathrm{HP}}} \simeq 145.52\,\mathrm{s}^{-1} \;\Rightarrow\; 23.16\,\mathrm{Hz} \tag{3.112}$$

The zero location has been numerically estimated by using the following parameter list:

- ▷ $A_{\rm v0} = 570000\,, \qquad \tau_{\rm OTA} = 660.94\,\mu{\rm s}$
- ▷ $G_{\rm m0} = 0.11\,{\rm S}\,, \qquad \tau_{\rm HP} = 6.872\,{\rm ms}$
- ▷ $R_{\rm sh} = 19.592\,{\rm k}\Omega\,, \qquad C_{\rm sh} = 732.376\,{\rm fF}$

to which we will refer again whenever we estimate other small-signal quantities.

The parameter values listed above have been obtained by the analysis of the actual circuit that realizes the second stage.

Let us now examine the poles. The transfer function denominator (3.110), can be expressed as

$$D^{\rm II}\,(s) = \bar{d}_0 + \bar{d}_1\,s + \bar{d}_2\,s^2 + \bar{d}_3\,s^3 = \bar{d}_0\left(1 + \frac{\bar{d}_1}{\bar{d}_0}\,s + \frac{\bar{d}_2}{\bar{d}_0}\,s^2 + \frac{\bar{d}_3}{\bar{d}_0}\,s^3\right) \tag{3.113}$$

Thus the poles could be found by factoring the third-order polynomial in (3.113), a calculation that can be performed using mathematical software. However, we can obtain a fairly good estimate of these poles by assuming at first there is a dominant pole p_1, which allows us to consider

$$p_1 \approx -\frac{\bar{d}_0}{\bar{d}_1} \simeq -\frac{G_{\rm m0}\,R_{\rm sh}}{\tau_{\rm HP} + R_{\rm sh}\,C_{\rm sh}} \simeq -\frac{G_{\rm m0}\,R_{\rm sh}}{\tau_{\rm HP}} \tag{3.114}$$

by assuming $G_{\rm m0}\,R_{\rm sh} \gg 1$ as well as $A_{\rm v0}\,(\tau_{\rm HP} + R_{\rm sh}\,C_{\rm sh}) \gg \tau_{\rm OTA}$ and $\tau_{\rm HP} \gg R_{\rm sh}\,C_{\rm sh}$, which is true in our case.

Thus

$$\mid p_1 \mid \simeq 313.6 \times 10^3\,{\rm s}^{-1} \;\Rightarrow\; 49.9\,{\rm kHz} \tag{3.115}$$

As the frequency is increased well above $\mid p_1 \mid$, where $\mid s \mid \gg \mid p_1 \mid$, we have $\mid \left(\bar{d}_1/\bar{d}_0\right) s \mid \gg 1$ so that (3.113) can be approximated by neglecting the constant 1 in parenthesis, to give

$$D^{\rm II}\,(s) \simeq \bar{d}_1\,s\left(1 + \frac{\bar{d}_2}{\bar{d}_1}\,s + \frac{\bar{d}_3}{\bar{d}_1}\,s^2\right) = \bar{d}_1\,s\left(1 - \frac{s}{p_2}\right)\left(1 - \frac{s}{p_3}\right) \tag{3.116}$$

Hence, the poles at high frequencies will be the roots of the quadratic term in parenthesis in (3.116). Although they can be real or complex, assuming they are real and widely separated ($\mid p_2 \mid \ll \mid p_3 \mid$) gives

$$p_2 \approx -\frac{\bar{d}_1}{\bar{d}_2} \simeq -\frac{A_{\rm v0}\,\tau_{\rm HP}}{\tau_{\rm HP}\,(\tau_{\rm OTA} + A_{\rm v0}\,R_{\rm sh}\,C_{\rm sh})} \simeq -\frac{1}{R_{\rm sh}\,C_{\rm sh}} \tag{3.117}$$

and

$$p_3 \approx \frac{\bar{d}_1}{\bar{d}_3}\,\frac{1}{p_2} = -\frac{\bar{d}_2}{\bar{d}_3} \simeq -\frac{A_{v0}\,R_{sh}\,C_{sh}\,\tau_{HP}}{R_{sh}\,C_{sh}\,\tau_{HP}\,\tau_{OTA}} = -\frac{A_{v0}}{\tau_{OTA}} \tag{3.118}$$

under the same assumptions as (3.114) and $A_{v0}\,R_{sh}\,C_{sh} \gg \tau_{OTA}$.

From (3.117) and (3.118) we have[1]

$$|\,p_2\,| \simeq 69.69 \times 10^6\,\mathrm{s}^{-1} \;\Rightarrow\; 11.09\,\mathrm{MHz} \tag{3.119}$$

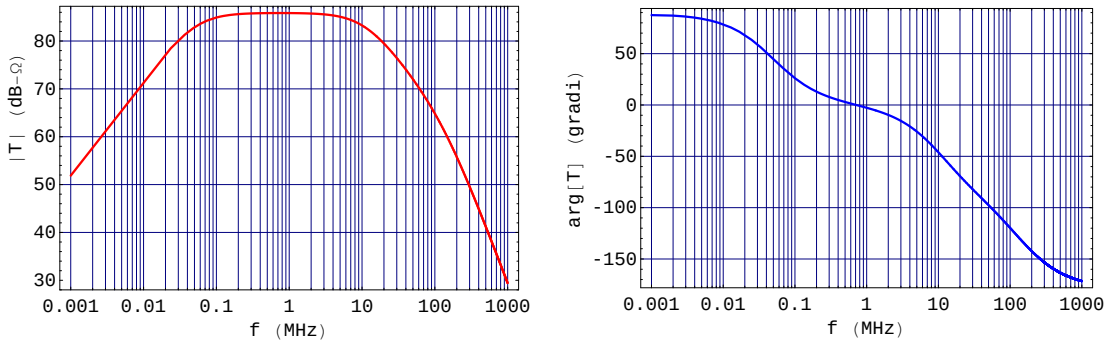
and

$$|\,p_3\,| \simeq 862.41 \times 10^6\,\mathrm{s}^{-1} \;\Rightarrow\; 137.26\,\mathrm{MHz} \tag{3.120}$$

Finally let us note that the values of the poles given by the preceding approximated analysis agree exactly with those obtained by solving (3.113) for the poles using a computer program, namely

$$\frac{|\,p_1\,|}{2\pi} \simeq 50.18\,\mathrm{kHz}\,, \quad \frac{|\,p_2\,|}{2\pi} \simeq 11.04\,\mathrm{MHz}\,, \quad \frac{|\,p_3\,|}{2\pi} \simeq 137.3\,\mathrm{MHz} \tag{3.121}$$

The magnitude and phase of $T^{II}(s)\,|_{s=j\omega}$ are shown in Fig. 3.26 that also allows us to perform a graphical check of the preceding results.



(a) (b)

Figure 3.26: (a) Magnitude in dB-Ω and (b) phase in degrees of $T^{II}(j\omega)$ versus frequency (*Red* and *blue* lines: analytical model).

[1]We recall that the pole and zero frequency values reported throughout the thesis have been obtained by dividing the pole and zero magnitudes by 2π.

Another interesting way of arriving at the same expression as in (3.110), (3.111) for the transfer function is to apply the feedback theory to our circuit, which will allow us to obtain a better understanding of the shape of the transfer function.

Figure 3.27 displays an ideal feedback configuration consisting of two main blocks assumed to be *unilateral*, i. e. the block chacterized by $a\,(s)$ (the basic amplifier) can only tansmit the signal from the input to the output whereas the block chacterized by $f\,(s)$ (the feedback network) can only transmit the signal from the output to the input and ideally does not load the basic amplifier.

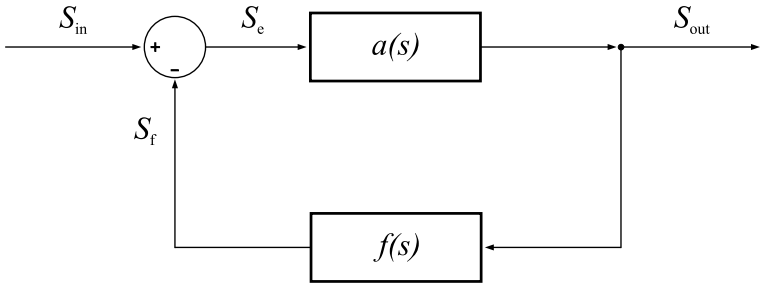


Figure 3.27: Ideal feedback configuration.

It can be shown that under the above assumptions we obtain

$$\frac{S_{\text{out}}}{S_{\text{in}}} = \frac{a\,(s)}{1 + a\,(s)\;f\,(s)} \tag{3.122}$$

It should be pointed out that in practical feedback configurations the division into basic amplifier and feedback network is not so easy to perform due to the bilaterality of the actual amplifiers and the loading effect of the feedback network.

However, in the case under examination the simplified models of the amplifier block and the feedback block allow us to apply the ideal feedback equation by simply letting

$$a\,(s) = T_{\text{bck1}}\,(s) = \frac{A_{\text{v0}}\,R_{\text{sh}}}{(1 + A_{\text{v0}}) + [R_{\text{sh}}C_{\text{sh}}\,(1 + A_{\text{v0}}) + \tau_{\text{OTA}}]\,s + \tau_{\text{OTA}}R_{\text{sh}}C_{\text{sh}}\,s^2} \tag{3.123}$$

and

$$f\,(s) = G_{\text{m}}\,(s) = \frac{G_{\text{m0}}}{1 + s\,\tau_{\text{HP}}} \tag{3.124}$$

to give

$$T^{\text{II}}\,(s) = \frac{a\,(s)}{1 + a\,(s)\;f\,(s)} \tag{3.125}$$

By considering the transfer function in the form given by (3.125) we can see that at low frequencies, where $|\,a\,(s)\;f\,(s)\,| \gg 1$, we have

$$T^{\mathrm{II}}\,(s) \sim \frac{1}{f\,(s)} \tag{3.126}$$

whereas at high frequencies, where $|\,a\,(s)\;f\,(s)\,| \ll 1$, we have

$$T^{\mathrm{II}}\,(s) \sim a\,(s) \tag{3.127}$$

By examining equation (3.126) we can observe that the pole of the transconductor block has become a zero from the overall transfer function standpoint, in agreement with what we have calculated in (3.112).

Furthermore, an analysis of equation (3.127) would give the same results as in (3.117) and (3.118) for the high-frequency poles p_2, p_3 as well as a frequency behavior in agreement with the high-frequency behavior shown in Fig. 3.26.

Input Impedance

By referring to the small-signal equivalent circuit of Fig. 3.25 we can find its input impedance by considering the current source I_{in} as a test current source and the voltage V_{in} as the voltage drop across it.

Thus, substituting $V_{\mathrm{out}} = -A_{\mathrm{v}}\,(s)\;V_{\mathrm{in}}$ into (3.106), assuming $I_{\mathrm{t}} = -I_{\mathrm{in}}$ as well as $V_{\mathrm{t}} = V_{\mathrm{in}}$ and $I_{\mathrm{out}} = 0$ and rearranging gives

$$Z^{\mathrm{II}}_{\mathrm{in}}\,(s) = \left.\frac{V_{\mathrm{in}}}{-I_{\mathrm{in}}}\right|_{I_{\mathrm{out}}=0} = \frac{V_{\mathrm{t}}}{I_{\mathrm{t}}} = \frac{R_{\mathrm{sh}}\;(1 + s\,\tau_{\mathrm{HP}})\;(1 + s\,\tau_{\mathrm{OTA}})}{\bar{d}_0 + \bar{d}_1\,s + \bar{d}_2\,s^2 + \bar{d}_3\,s^3} \tag{3.128}$$

where the coefficients of s, s^2 and s^3 in the denominator are still given by (3.111).

Since the denominator of (3.128) is the same as that of the transfer function, even the poles of the input impedance are the same as those of the transfer function and thus equations (3.114), (3.117), (3.118) still apply.

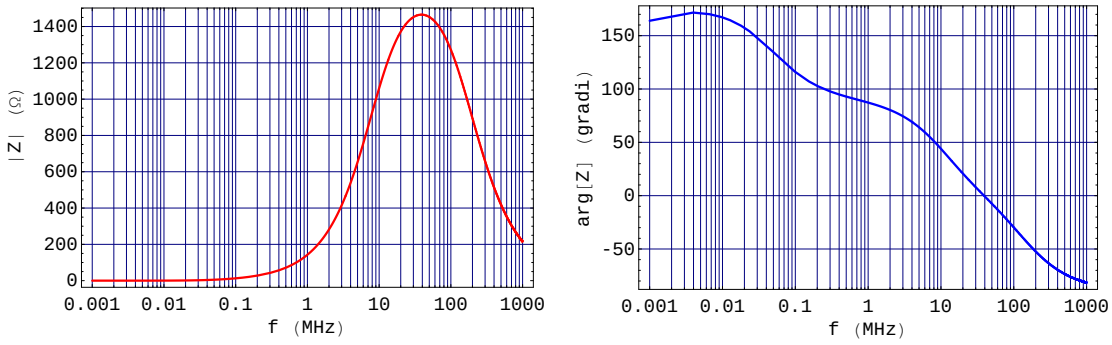
On the other hand, the numerator of equation (3.128) shows that the input impedance also has two real negative zeros whose magnitude is given by

$$|\;z_1\;| = \frac{1}{\tau_{\mathrm{HP}}} \simeq 145.52\,\mathrm{s}^{-1} \;\Rightarrow\; 23.16\,\mathrm{Hz} \tag{3.129}$$

and

$$|\;z_2\;| = \frac{1}{\tau_{\mathrm{OTA}}} \simeq 1.513 \times 10^3\,\mathrm{s}^{-1} \;\Rightarrow\; 240.8\,\mathrm{Hz} \tag{3.130}$$

The magnitude and phase of $Z_{\text{in}}^{\text{II}}(s)\,|_{s=j\omega}$ are shown in Fig. 3.28. In particular, the presence of the two low-frequency zeros can be checked by examining Fig. 3.28(b) showing a phase value of about 180° at a frequency of about 5 kHz, which is in agreement with the phase shift of 180° due to two low-frequency and fairly separated zeros.



(a) (b)

Figure 3.28: (a) Magnitude in Ω and (b) phase in degrees of $Z_{\text{in}}^{\text{II}}(j\omega)$ versus frequency (*Red* and *blue* lines: analytical model).

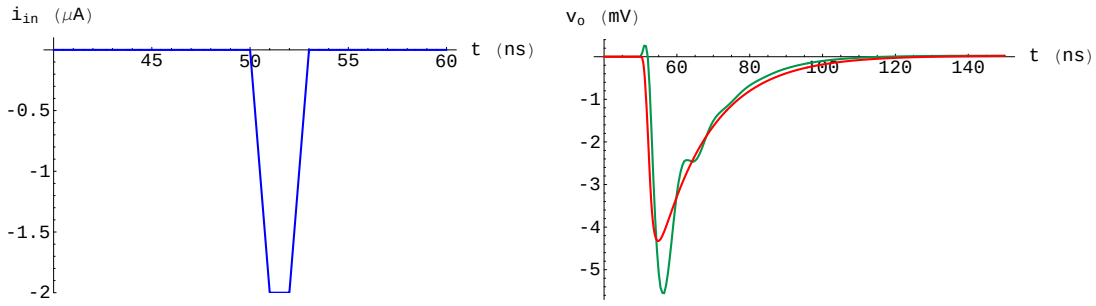
Output Impedance and Reverse Transmission

The output impedance and the reverse transmission of the second stage turns out to be equal to zero due to the ideal models which we have chosen to represent the two blocks making up the stage.

3.2.2 Pulse Response

In this section we will try to investigate the validity extent of our analytical model in adequately representing the behavior of the second stage. We will also suggest some changes suitable for improving the agreement between the predicted behavior and the real one.

Thus, let us examine the pulse response of the circuit to the usual small input current pulse $i_{in}(t)$ carrying a charge $Q = 4\,\text{fC}$. By inspecting Fig. 3.29(b) we can see that the shape of the output voltage is very different to that predicted by the

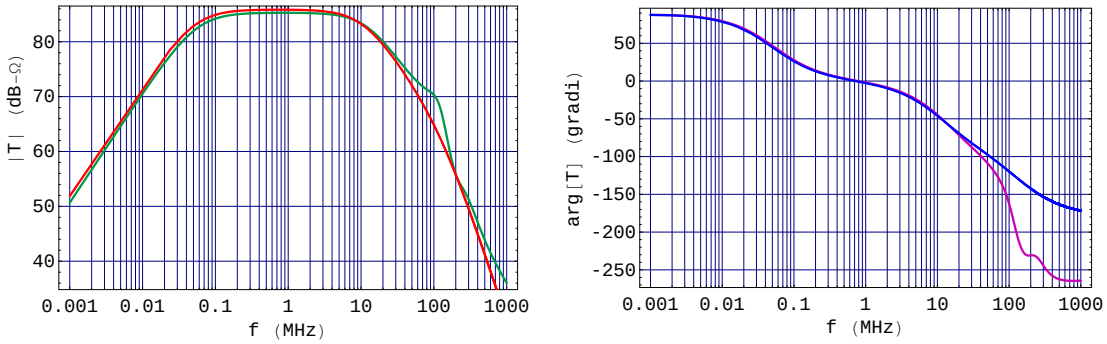


(a) Input current pulse $i_{in}\,(t)$.

(b) Circuit response $v_{out}\,(t)$ (*Red* line: analytical model. *Green* line: transistor-level model).

Figure 3.29: Pulse response of the circuit shown in Fig. 3.24.

transistor-level model. The transfer function shown in Fig. 3.30, especially at high frequencies, is also very different.



(a)

(b)

Figure 3.30: (a) Magnitude in dB-Ω and (b) phase in degrees of $T^{\mathrm{II}}\,(j\omega)$ versus frequency (*Red* and *blue* lines: analytical model. *Green* and *purple* lines: transistor-level model).

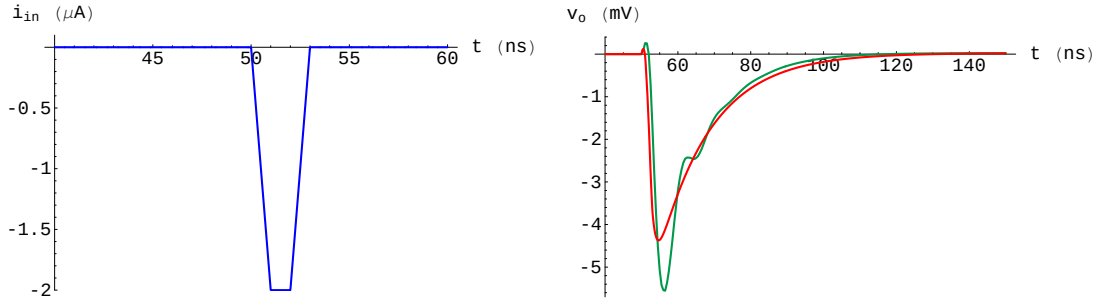
Then, let us introduce some changes in our model to check their effects on the transfer function and the resulting output voltage shape.

First, we can add to the output port of our OTA model an output resistance $R_{\mathrm{o}}^{\mathrm{OTA}}$ so that now the following system is to be solved in order to find the new circuit

response

$$\begin{bmatrix} \dfrac{1}{R_{\rm sh}} + s\,C_{\rm sh} & -\dfrac{1}{R_{\rm sh}} - s\,C_{\rm sh} - \dfrac{G_{\rm m0}}{1+s\,\tau_{\rm HP}} \\ -\dfrac{1}{R_{\rm sh}} - s\,C_{\rm sh} + \dfrac{A_{\rm v0}}{R_{\rm o}^{\rm OTA}\,(1+s\,\tau_{\rm OTA})} & \dfrac{1}{R_{\rm sh}} + \dfrac{1}{R_{\rm o}^{\rm OTA}} + s\,C_{\rm sh} \end{bmatrix} \begin{bmatrix} V_{\rm in} \\ V_{\rm out} \end{bmatrix} = \begin{bmatrix} -I_{\rm in} \\ I_{\rm out} \end{bmatrix} \tag{3.131}$$

Thus, solving it for $V_{\rm out}$ by assuming $I_{\rm out} = 0$ and following the usual steps described in the previous sections give the new $v_{out}\,(t)$ whose shape is shown in Fig. 3.31(b).



(a) Input current pulse $i_{in}\,(t)$.

(b) Circuit response $v_{out}\,(t)$ obtained by setting $R_{\rm o}^{\rm OTA} = 200\,\Omega$ (*Red* line: analytical model. *Green* line: transistor-level model).

Figure 3.31: Pulse response of the circuit shown in Fig. 3.24 after adding $R_{\rm o}^{\rm OTA}$.

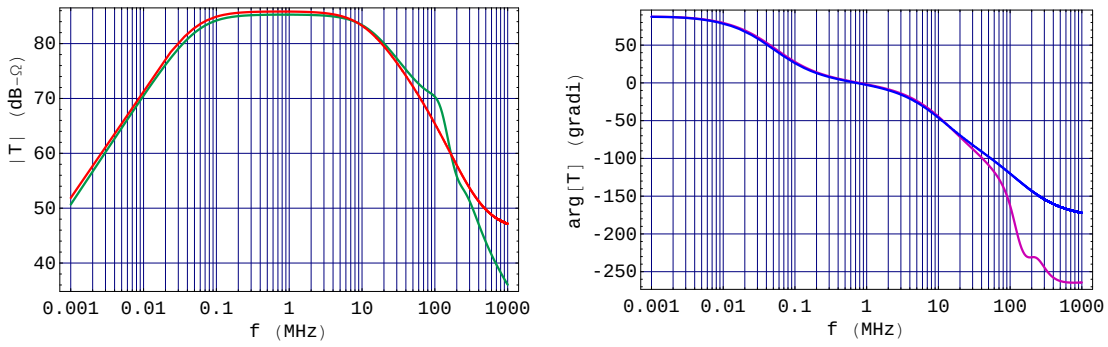
By examining the figure we can note that the addition of $R_{\rm o}^{\rm OTA}$ to the small-signal equivalent circuit of Fig. 3.25 gives rise to the initial small spike in the pulse response in accord with the real behavior.

Furthermore, an inspection of Fig. 3.32 also shows that the shape of the new transfer function fits better the real one.

Let us now try to further improve the agreement between the results obtained from the two models by adding a second pole to the function $A_{\rm v}\,(s)$ representing the voltage gain of the OTA.

Hence equation (3.108) becomes

$$A_{\rm v}\,(s) = \frac{A_{\rm v0}}{(1+s\,\tau_{\rm OTA})\,(1+s\,\tau_{\rm OTA2})} \tag{3.132}$$



(a) (b)

Figure 3.32: (a) Magnitude in dB-Ω and (b) phase in degrees of $T^{\mathrm{II}}(j\omega)$ versus frequency in the case $R_{\mathrm{o}}^{\mathrm{OTA}} = 200\,\Omega$ (*Red* and *blue* lines: analytical model. *Green* and *purple* lines: transistor-level model).

and system (3.131) also changes, becoming

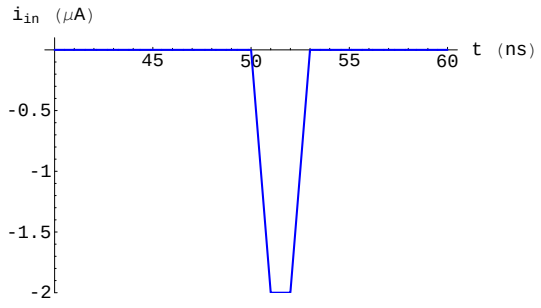
$$\begin{bmatrix} \dfrac{1}{R_{\mathrm{sh}}} + s\,C_{\mathrm{sh}} & -\dfrac{1}{R_{\mathrm{sh}}} - s\,C_{\mathrm{sh}} - \dfrac{G_{\mathrm{m0}}}{1 + s\,\tau_{\mathrm{HP}}} \\ -\dfrac{1}{R_{\mathrm{sh}}} - s\,C_{\mathrm{sh}} + \dfrac{A_{\mathrm{v0}}}{R_{\mathrm{o}}^{\mathrm{OTA}}\,(1 + s\,\tau_{\mathrm{OTA}})\,(1 + s\,\tau_{\mathrm{OTA2}})} & \dfrac{1}{R_{\mathrm{sh}}} + \dfrac{1}{R_{\mathrm{o}}^{\mathrm{OTA}}} + s\,C_{\mathrm{sh}} \end{bmatrix} \cdot \mathbf{V} = \mathbf{I} \tag{3.133}$$

Then, solving (3.133) for V_{out} leads to the pulse response shown in Fig. 3.33(b) which displays a good matching between the two models.

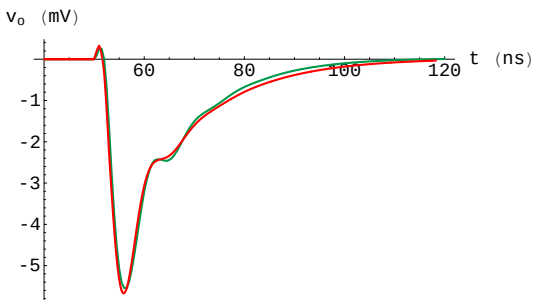
The same agreement can be appreciated by inspecting Fig. 3.34 which shows the magnitude and phase of the small-signal transfer function.

In order to understand whether the changes so far introduced reflect the real behavior of the component they model, let us concentrate on the output resistance and the voltage gain of the OTA to check our assumptions.

A computer simulation of the actual circuit has shown that our estimate of $R_{\mathrm{o}}^{\mathrm{OTA}}$ (about $200\,\Omega$) is in fairly good agreement with the value of the output impedance of the OTA over a wide range of frequencies whereas the model suggested by equation (3.132) for the voltage gain gives good results at low frequencies but only fairly good results at high frequencies, as shown in Fig. 3.35.



(a) Input current pulse $i_{in}\,(t)$.



(b) Circuit response $v_{out}\,(t)$ obtained by setting $R_{\rm o}^{\rm OTA} = 200\,\Omega$ and $\tau_{\rm OTA2} = 1.85\,{\rm ns}$ (*Red* line: analytical model. *Green* line: transistor-level model).

Figure 3.33: Pulse response of the circuit shown in Fig. 3.24 after adding $R_{\rm o}^{\rm OTA}$ and a second pole to $A_{\rm v}\,(s)$.

However a finer matching at high frequency has been found by assuming

$$A_{\rm v}\,(s) = \frac{A_{\rm v0}\,Z_{\rm cc}^{(2)}\,(s)}{(1+s\,\tau_{\rm OTA})\,(1+s\,\tilde{\tau}_{\rm OTA2})\,(1+s\,\tau_{\rm OTA3})\,P_{\rm cc}^{(2)}\,(s)} \tag{3.134}$$

where

$$\begin{cases} Z_{\rm cc}^{(2)}\,(s) = 1 + a_1\,s + a_2\,s^2 \\ P_{\rm cc}^{(2)}\,(s) = 1 + b_1\,s + b_2\,s^2 \end{cases} \tag{3.135}$$

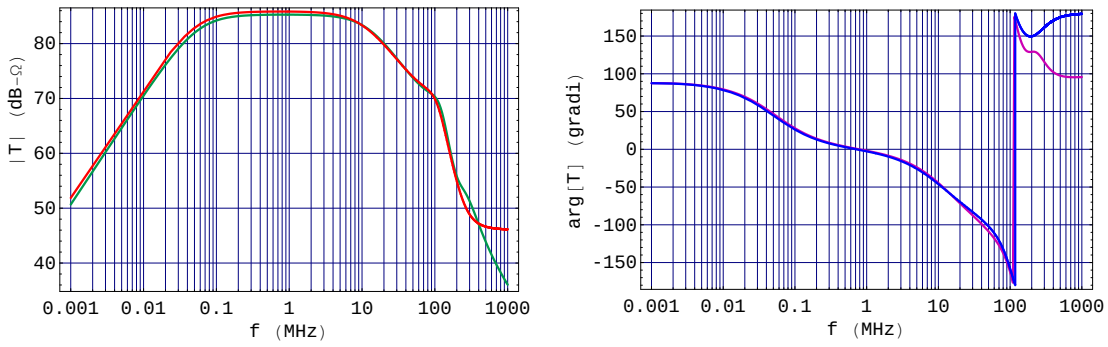
are two second order polynomials in s each of which has a pair of complex roots.

Thus by setting

- $a_1 = 1.309\,{\rm ns}\,,\ \ a_2 = 0.579\,({\rm ns})^2$
- $b_1 = 0.238\,{\rm ns}\,,\ \ b_2 = 0.105\,({\rm ns})^2$
- $\tilde{\tau}_{\rm OTA2} = 1.74\,{\rm ns} \simeq \tau_{\rm OTA2}\,,\ \ \tau_{\rm OTA3} = 0.38\,{\rm ns}$

we obtain the graphical result shown in Fig. 3.36 which allows us to see directly the improved agreement of both the magnitude and the phase of $A_{\rm v}\,(s)$.

The results so far obtained have shown that the two-poles model of $A_{\rm v}\,(s)$ gives good results when used for investigating the behavior of the whole second stage although this model does not fit very well the real shape of the OTA voltage gain.



(a) (b)

Figure 3.34: (a) Magnitude in dB-Ω and (b) phase in degrees of $T^{\mathrm{II}}(j\omega)$ versus frequency in the case $R_{\mathrm{o}}^{\mathrm{OTA}} = 200\,\Omega$ and $\tau_{\mathrm{OTA2}} = 1.85\,\mathrm{ns}$ (*Red* and *blue* lines: analytical model. *Green* and *purple* lines: transistor-level model).

This cosideration leads us to think that in practice the transconductor block performs a kind of compensation, which can be further highlighted by the comparison of Fig. 3.37 showing the magnitude only of the transfer function of the feedback OTA with Fig. 3.34 which shows the magnitude of the transfer function of the whole stage.

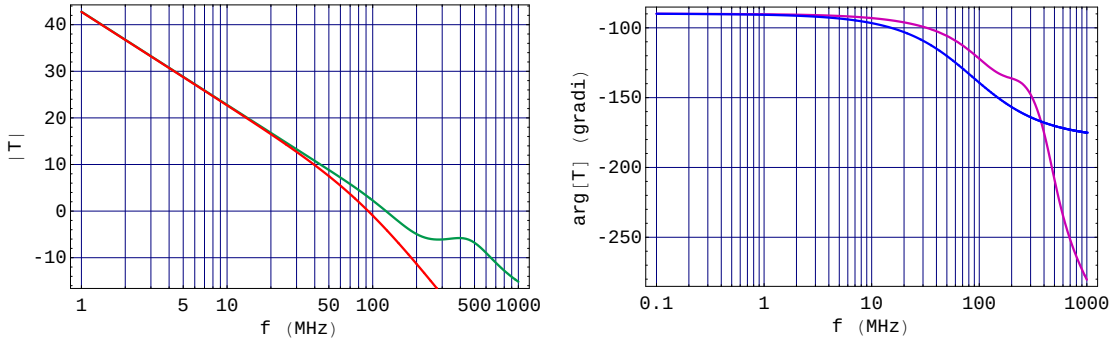
In fact, by examining Fig. 3.37 we can note a fairly important peak at high frequency which tends to disappear when the transfer function of the whole stage is considered.

However, although the previous analysis has pointed out some limitations of our initial simplified model (i.e. the model without $R_{\mathrm{o}}^{\mathrm{OTA}}$ and with $A_{\mathrm{v}}(s)$ given by (3.108)) we will still use that simple model in our analysis.

The reason for such a choice is that the stage under consideration deals with input current pulses much slower than incoming ones in the first stage. Thus we will show that the response of the second stage to such pulses can be predicted with adequate accuracy even by the simplest model.

Thus let us consider the pulse response shown in Fig. 3.39 which displays a small input current pulse having a rise time $t_{\mathrm{r}} = 3\,\mathrm{ns}$ and a fall time $t_{\mathrm{f}} = 10\,\mathrm{ns}$, unlike the one used before to test the circuit response which showed a rise time $\bar{t}_{\mathrm{r}} = 1\,\mathrm{ns}$ and a fall time $\bar{t}_{\mathrm{f}} = 1\,\mathrm{ns}$.

By comparing Fig. 3.39(b) with Fig. 3.29(b) we can see directly that the same



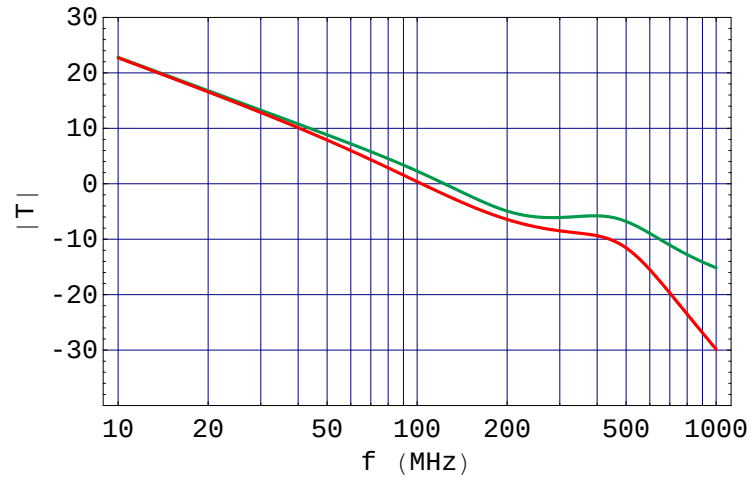
(a) (b)

Figure 3.35: (a) Magnitude in dB and (b) phase in degrees of $A_{\mathrm{v}}(j\omega)$ versus frequency (*Red* and *blue* lines: two-poles model. *Green* and *purple* lines: transistor-level model).

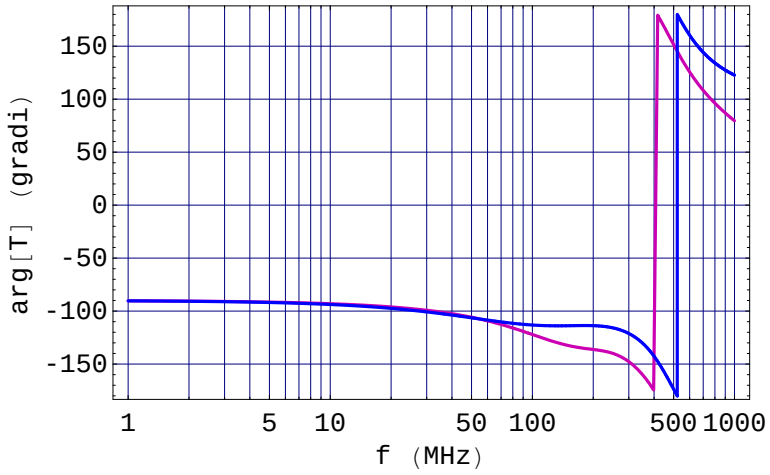
model which shows an evident disagreement with the real circuit behavior in the case of a fast pulse, on the contrary gives a fairly good result in the case of a slower pulse.

One explanation of such different results can be found by comparing the Fourier spectrum of the two pulses, as shown in Fig. 3.38. By inspecting the figure we can observe that in the range where very high frequencies still play an important role for the fast pulse, they are already much less significant for the slower pulse.

Thus it can be reasonable to expect that a fairly important disagreement at high frequency between the models results only in a slightly different circuit response, in the case of the slower pulse.



(a)



(b)

Figure 3.36: (a) Magnitude in dB and (b) phase in degrees of $A_{\mathrm{v}}(j\omega)$ versus frequency (*Red* and *blue* lines: analytical model. *Green* and *purple* lines: transistor-level model).

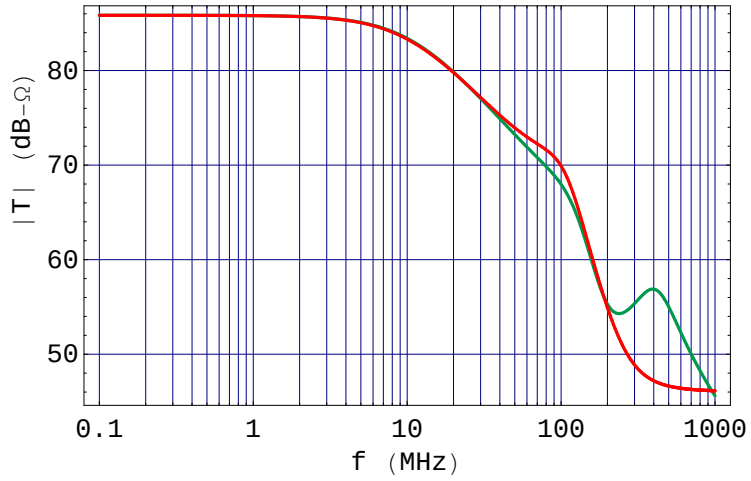


Figure 3.37: Magnitude in dB-Ω of the transfer function of the feedback OTA only.

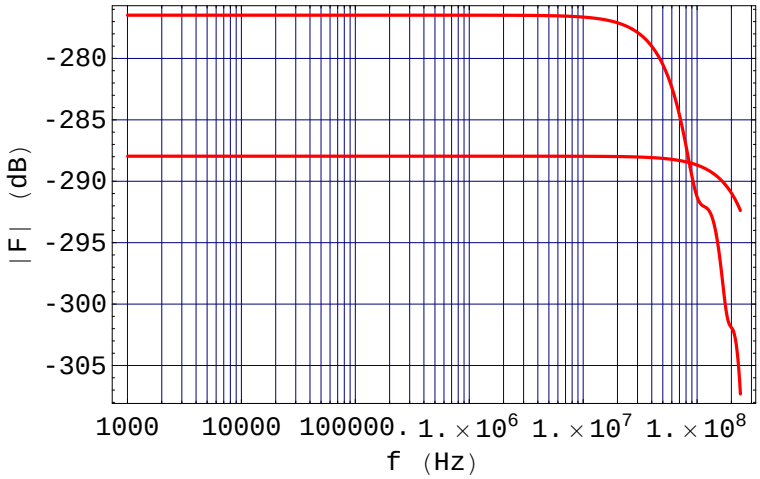
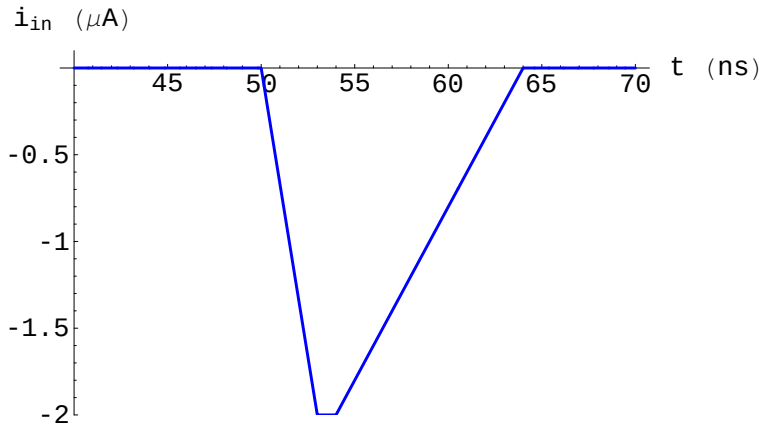
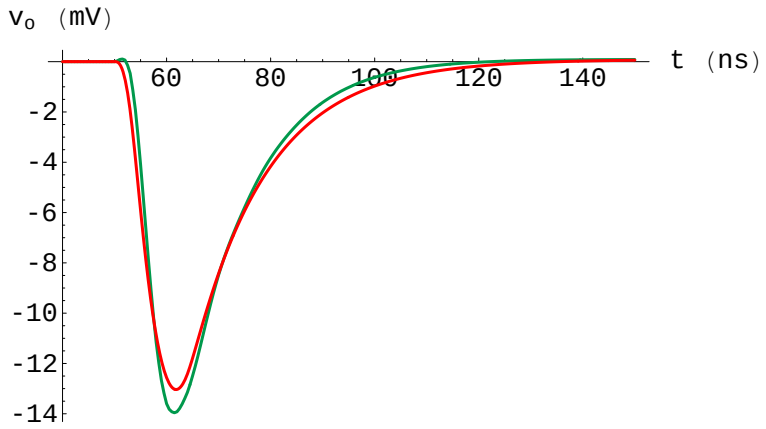


Figure 3.38: Fourier spectrum of the fast pulse and the slower pulse.



(a) Slow input current pulse $i_{in}\,(t)$.



(b) Circuit response $v_{out}\,(t)$ (*Red* line: analytical model. *Green* line: transistor-level model).

Figure 3.39: Pulse response of the circuit shown in Fig. 3.24.

3.3 Analysis of the Complete Amplifier

After the detailed analysis of the first and second stage of the front end circuit performed in the preceding sections, the behavior of the full circuit will be dealt with in this section from a small-signal standpoint.

This analysis could be performed by considering the complete small-signal equivalent circuit, writing the corresponding circuit equations and solving them for the total transfer function.

However this procedure would lead to a complex equation which would be fairly difficult to interpret. Thus we will carry out the circuit small-signal analysis through the use of two-port representations of the two stages involved.

This method also allows us to use small-signal functions such us transfer functions as well as input and output impedances already calculated earlier for each stage.

3.3.1 Two-Port Representation of the First Stage

Figure 3.40 shows the block diagram of the first stage as well as the Z-parameter two-port equivalent circuit representing it.

Focusing on the impedance-parameter equations, where the terminal currents are assumed to be the independent variables, leads to the equations

$$V_1 = Z_{11}\, I_1 + Z_{12}\, I_2 \tag{3.136}$$

$$V_2 = Z_{21}\, I_1 + Z_{22}\, I_2 \tag{3.137}$$

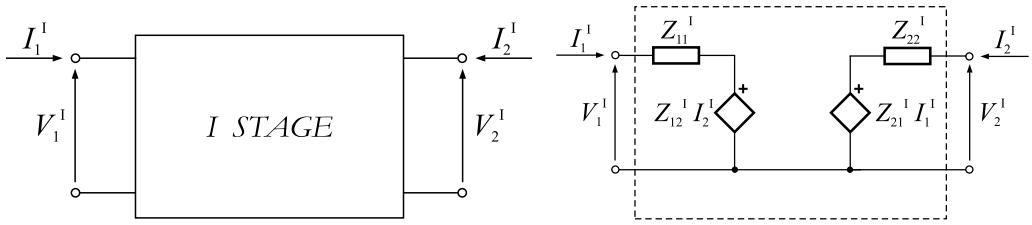
where

$$Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} \qquad Z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} \tag{3.138}$$

$$Z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} \qquad Z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} \tag{3.139}$$

Now, by referring to the small-signal equivalent circuit of the first stage shown in Fig. 3.10 and to Fig. 3.40, letting $V_1^{\mathrm{I}} = V_{\mathrm{in}}$, $V_2^{\mathrm{I}} = V_{\mathrm{out}}$, $I_1^{\mathrm{I}} = -I_{\mathrm{in}}$ and $I_2^{\mathrm{I}} = I_{\mathrm{out}}$ gives

$$Z_{11}^{\mathrm{I}} = \left.\frac{V_1^{\mathrm{I}}}{I_1^{\mathrm{I}}}\right|_{I_2^{\mathrm{I}}=0} = Z_{\mathrm{in}}^{\mathrm{I}}(s) \tag{3.140}$$



(a) Block diagram of the first stage.

(b) Z-parameter two-port equivalent circuit for representing the first stage.

Figure 3.40: Block diagram and two-port representation of the first stage.

where $Z_{\mathrm{in}}^{\mathrm{I}}(s)$ is given by (3.49),

$$Z_{12}^{\mathrm{I}} = \left.\frac{V_1^{\mathrm{I}}}{I_2^{\mathrm{I}}}\right|_{I_1^{\mathrm{I}}=0} = T_{\mathrm{rev}}^{\mathrm{I}}(s) \tag{3.141}$$

where $T_{\mathrm{rev}}^{\mathrm{I}}(s)$ is given by (3.94),

$$Z_{21}^{\mathrm{I}} = \left.\frac{V_2^{\mathrm{I}}}{I_1^{\mathrm{I}}}\right|_{I_2^{\mathrm{I}}=0} = -T^{\mathrm{I}}(s) \tag{3.142}$$

where $T^{\mathrm{I}}(s)$ is given by (3.23) and finally

$$Z_{22}^{\mathrm{I}} = \left.\frac{V_2^{\mathrm{I}}}{I_2^{\mathrm{I}}}\right|_{I_1^{\mathrm{I}}=0} = Z_{\mathrm{out}}^{\mathrm{I}}(s) \tag{3.143}$$

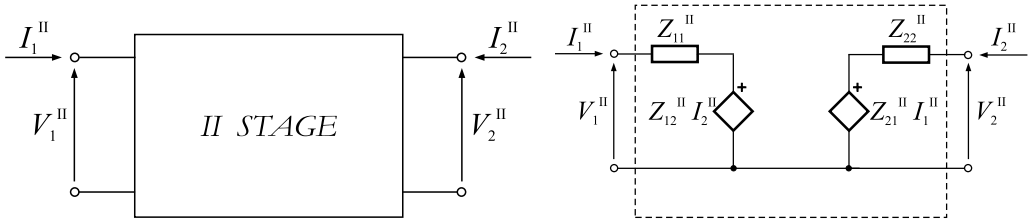
where $Z_{\mathrm{out}}^{\mathrm{I}}(s)$ is given by (3.84).

3.3.2 Two-Port Representation of the Second Stage

Figure 3.41 shows the block diagram of the second stage as well as the Z-parameter two-port equivalent circuit representing it.

The impedance-parameter equations (3.136) and (3.137) as well as equations (3.138) and (3.139) given in the previous subsection, still apply here.

Thus, by referring now to the small-signal equivalent circuit of the second stage shown in Fig. 3.25 and to Fig. 3.41, letting $V_1^{\mathrm{II}} = V_{\mathrm{in}}$, $V_2^{\mathrm{II}} = V_{\mathrm{out}}$, $I_1^{\mathrm{II}} = -I_{\mathrm{in}}$ and $I_2^{\mathrm{II}} = I_{\mathrm{out}}$ gives



(a) Block diagram of the second stage.

(b) Z-parameter two-port equivalent circuit for representing the second stage.

Figure 3.41: Block diagram and two-port representation of the second stage.

$$Z_{11}^{\mathrm{II}} = \left.\frac{V_1^{\mathrm{II}}}{I_1^{\mathrm{II}}}\right|_{I_2^{\mathrm{II}}=0} = Z_{\mathrm{in}}^{\mathrm{II}}(s) \tag{3.144}$$

where $Z_{\mathrm{in}}^{\mathrm{II}}(s)$ is given by (3.128),

$$Z_{12}^{\mathrm{II}} = \left.\frac{V_1^{\mathrm{II}}}{I_2^{\mathrm{II}}}\right|_{I_1^{\mathrm{II}}=0} = T_{\mathrm{rev}}^{\mathrm{II}}(s) = 0 \tag{3.145}$$

$$Z_{21}^{\mathrm{II}} = \left.\frac{V_2^{\mathrm{II}}}{I_1^{\mathrm{II}}}\right|_{I_2^{\mathrm{II}}=0} = -T^{\mathrm{II}}(s) \tag{3.146}$$

where $T^{\mathrm{II}}(s)$ is given by (3.110) and finally

$$Z_{22}^{\mathrm{II}} = \left.\frac{V_2^{\mathrm{II}}}{I_2^{\mathrm{II}}}\right|_{I_1^{\mathrm{II}}=0} = Z_{\mathrm{out}}^{\mathrm{II}}(s) = 0 \tag{3.147}$$

3.3.3 Two-Port Representation of the Full Circuit

The results obtained in the preceding subsections can be used now to give a close-form expression of the small-signal transfer function of the full circuit.

For this purpose let us consider Fig. 3.42 which also shows a resistor R required to drive properly the second stage with a current signal.

The value of this resistor can be externally set by choosing to connect one of the two resistors shown in Fig. 3.43 which displays the schematic diagram of the total circuit. The internal switch T allowing us to choose the desired resistance value is achieved by means of a CMOS inverter.

The values of the resistors used in the actual circuit are

▷ $R_1 = 1224.49\,\Omega\,, \quad R_2 = 6367.36\,\Omega$

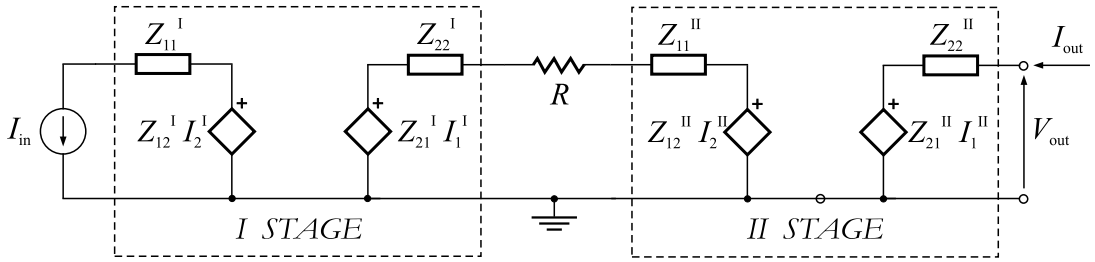


Figure 3.42: The full circuit obtained by cascading the two main stages.

Thus, by letting $V_2^{\rm II} = V_{\rm out}$, $I_2^{\rm II} = I_{\rm out}$, $I_1^{\rm I} = -I_{\rm in}$ and assuming $I_2^{\rm I}$, $I_1^{\rm II}$ have the same direction as in Fig. 3.40(b) and Fig. 3.41(b), by direct inspection of Fig. 3.42 further assuming $I_{\rm out} = 0$ we simply have

$$V_{\rm out} = Z_{21}^{\rm II}\, I_1^{\rm II} \tag{3.148}$$

Hence, since

$$I_1^{\rm II} = \frac{Z_{21}^{\rm I}\, I_1^{\rm I}}{R + Z_{22}^{\rm I} + Z_{11}^{\rm II}} = -I_{\rm in}\,\frac{Z_{21}^{\rm I}}{R + Z_{22}^{\rm I} + Z_{11}^{\rm II}} \tag{3.149}$$

substituting (3.149) into (3.148) and rearranging gives

$$\left.\frac{V_{\rm out}}{I_{\rm in}}\right|_{I_{\rm out}=0} = -\frac{Z_{21}^{\rm II}\, Z_{21}^{\rm I}}{R + Z_{22}^{\rm I} + Z_{11}^{\rm II}} \tag{3.150}$$

Finally, further substituting (3.146), (3.142), (3.143) and (3.144) into (3.150) yields

$$T\,(s) = \left.\frac{V_{\rm out}}{I_{\rm in}}\right|_{I_{\rm out}=0} = -\frac{T^{\rm I}\,(s)\; T^{\rm II}\,(s)}{R + Z_{\rm out}^{\rm I}\,(s) + Z_{\rm in}^{\rm II}\,(s)} \tag{3.151}$$

which is the small-signal transfer function of the whole circuit.

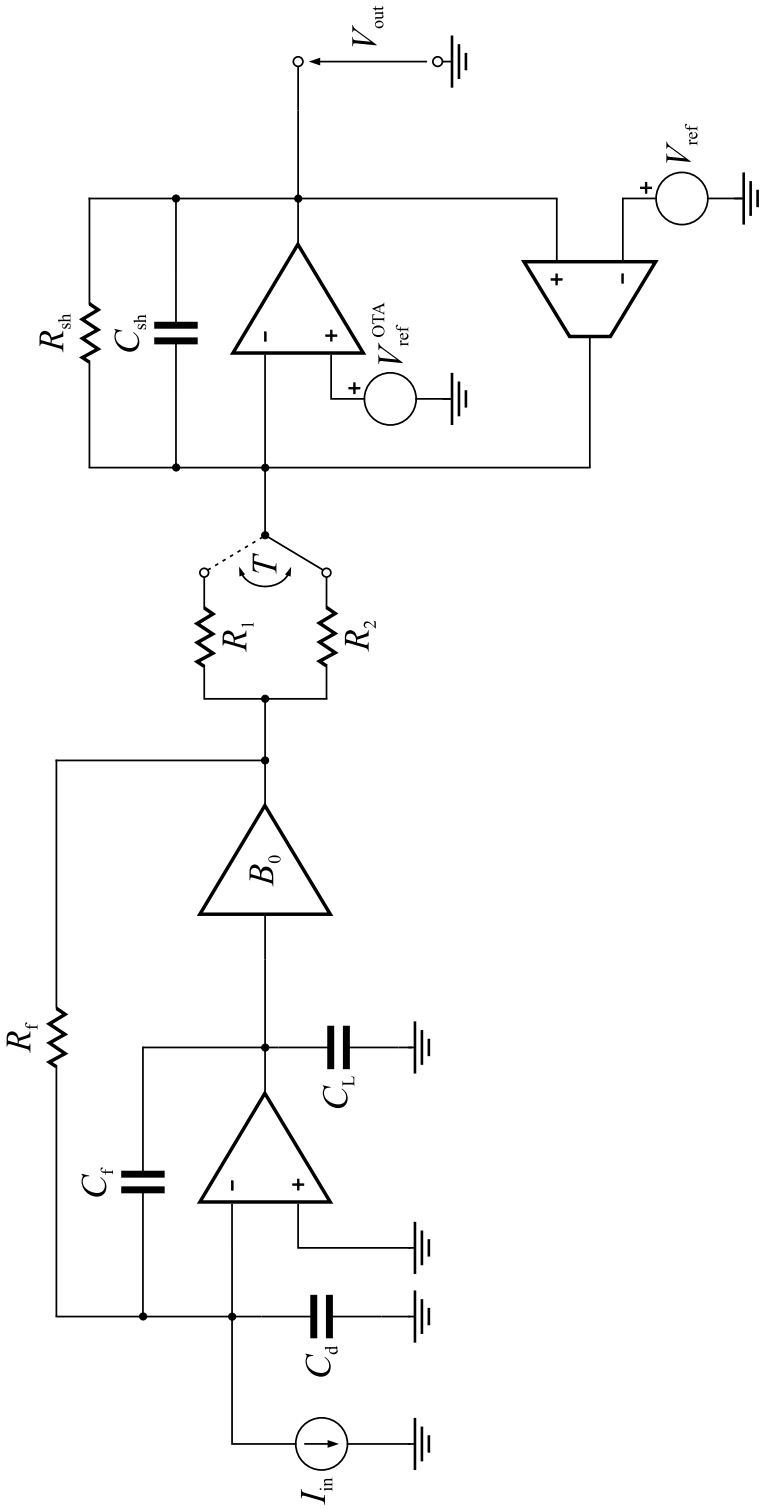


Figure 3.43: Schematic diagram of the complete circuit.

In addition it is interesting to calculate the transfer function of the first stage allowing for the loading effect of the second stage. It can be shown that

$$\left.\frac{V_2^{\mathrm{I}}}{I_{\mathrm{in}}}\right|_{I_{\mathrm{out}}=0} = T^{\mathrm{I}}(s)\left(\frac{R+Z_{\mathrm{in}}^{\mathrm{II}}(s)}{R+Z_{\mathrm{out}}^{\mathrm{I}}(s)+Z_{\mathrm{in}}^{\mathrm{II}}(s)}\right) \approx T^{\mathrm{I}}(s) \tag{3.152}$$

which shows that the second stage does not affect the behavior of the first stage provided that $|Z_{\mathrm{out}}^{\mathrm{I}}| \ll R+ |Z_{\mathrm{in}}^{\mathrm{II}}|$.

3.3.4 Frequency Analysis of the Full Circuit

Transfer Function

The calculation of the transfer function of the full circuit has been already carried out in the previous section and has led to equation (3.151).

The magnitude and phase of $T(s)\,|_{s=j\omega}$ are shown in Fig. 3.44. By inspecting the figure we can observe the presence of a very low-frequency zero followed by a low-frequency pole. They achieve an approximated high-pass filter stemming from the low-pass transfer function of the active feedback network of the second stage, as mentioned in section 3.2.1 (equation (3.126)).

This high-pass filter by providing a lower low-frequency gain, causes the output baseline to be independent of the detector leakage current which shows very slow changes. Thus the output baseline stabilization is guaranteed at low frequency.

However, when the rate of the unipolar incoming pulses becomes high or very high, a drift of the output baseline is observed due to the presence of this high-pass filter. This baseline shift mainly depending on the pulse rate and amplitude as well as the low-frequency zero location will be taken into consideration in the following subsection.

3.3.5 Pulse Response

First, let us consider the circuit response to the small single input pulse shown in Fig. 3.45(a).

The responses displayed in Fig. 3.45(b) highlight once again the adequate accuracy of the results predicted by the analytical model.

Let us now focus on the response of the full circuit to a sequence of pulses incoming at rate $r = 5\,\mathrm{MHz}$ and carrying a charge $Q = 4\,\mathrm{fC}$.

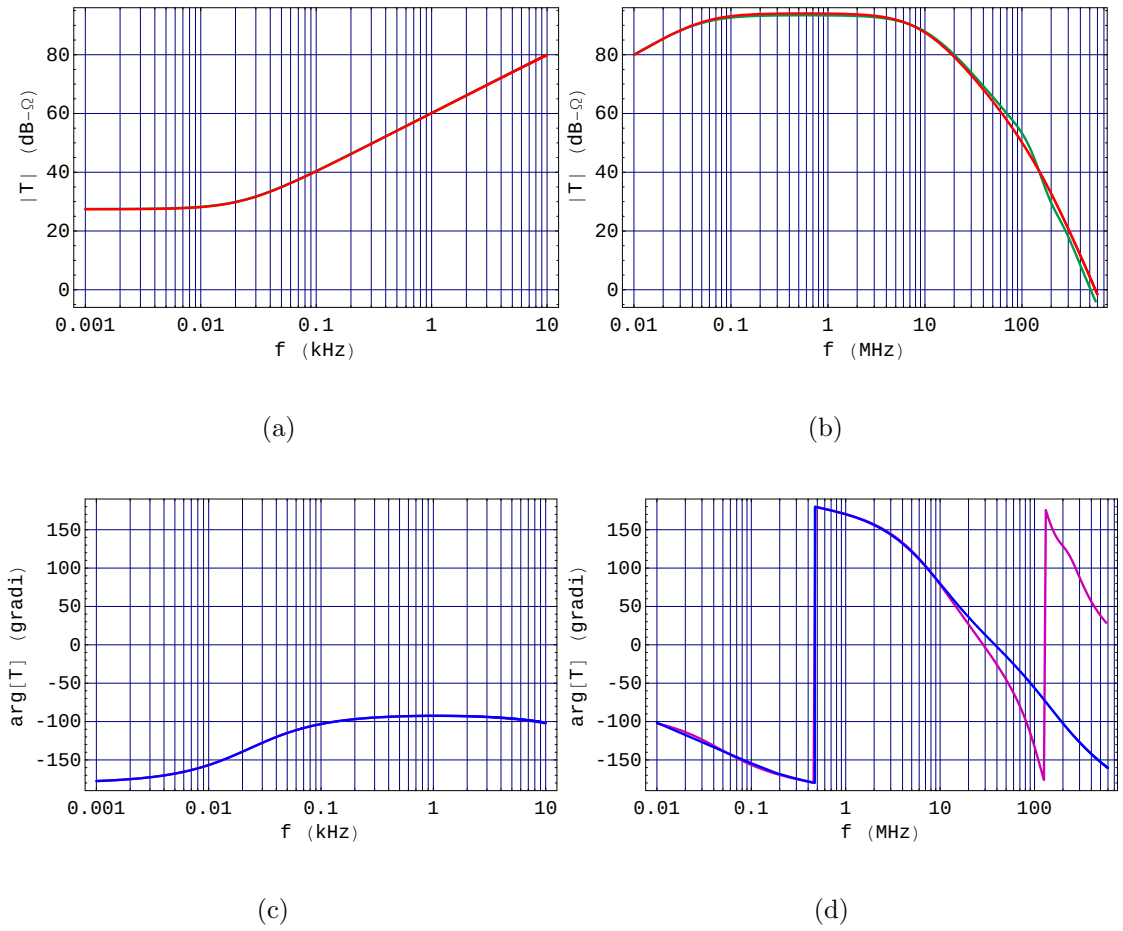


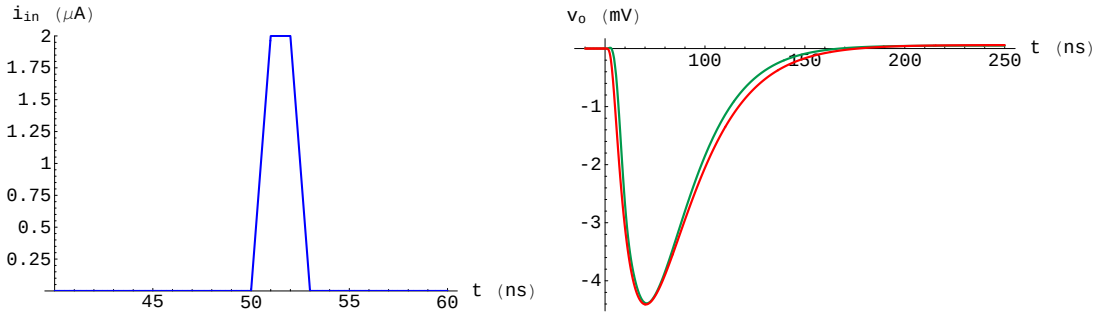
Figure 3.44: (a), (b) Magnitude in dB-Ω and (c), (d) phase in degrees of $T(j\omega)$ versus frequency (*Red* and *blue* lines: analytical model. *Green* and *purple* lines: transistor-level model).

The output voltage is shown in Fig. 3.46 which also allows us to observe the expected voltage drift mentioned in the previous subsection.

Moreover, Fig. 3.47 shows the graphical result of another analogous *Mathematica* simulation carried out by applying to the input of the circuit a train of large current pulses (incoming at $r = 5\,\text{MHz}$) each of which produces a 3-V output signal.

This simulation has been performed to point out that the output voltage drift is proportional to the area of the output signals so that it increases as these signals are increased.

In fact by direct inspection of Fig. 3.46(b) and Fig. 3.47(b) we can estimate a



(a) Input current pulse $i_{in}(t)$.

(b) Circuit response $v_{out}(t)$ (*Red* line: analytical model. *Green* line: transistor-level model).

Figure 3.45: Pulse response of the circuit shown in Fig. 3.43.

baseline shift approximately equal to 1 mV and 0.7 V respectively, in agreement with the preceding considerations.

It is also interesting to note that the baseline shift to peaking voltage ratio is nearly the same in both cases and it is approximately equal to 22.5% for the given rate $r = 5\,\text{MHz}$.

In addition, we wish to point out that the circuit under consideration produces output signals whose time length is nearly 160 ns, as shown in Fig. 3.45(b).

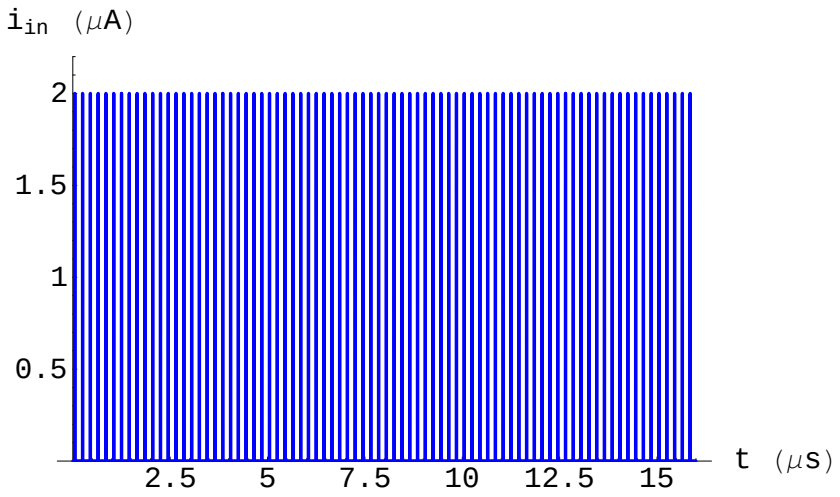
Thus the circuit so far described is unable to work properly as the pulse rate exceeds the value $r = 5\,\text{MHz}$ (corresponding to a period $T = 200\,\text{ns}$) due to the *pile-up* effect[2].

For this reason we will consider in the following chapters a circuit version able to produce narrower output signals in order to provide a counting rate in the order of 10 MHz.

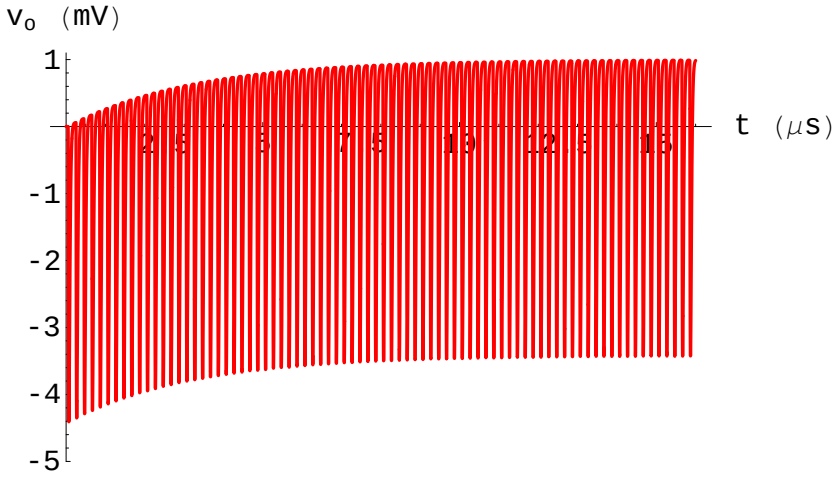
This circuit will be referred to as the "fast" circuit, unlike the old circuit which we will call the "slow" circuit.

Finally, we consider the simulation results shown in Fig. 3.48 to show the good agreement between the slow-circuit response given by the SPICE simulation (founded on a transistor-level model) and the one predicted by the *Mathematica* simulation (founded on our analytical model) when a train of pulses incoming at rate

[2] *pulse pile-up* occurs when a second pulse rides on the tail of the first.

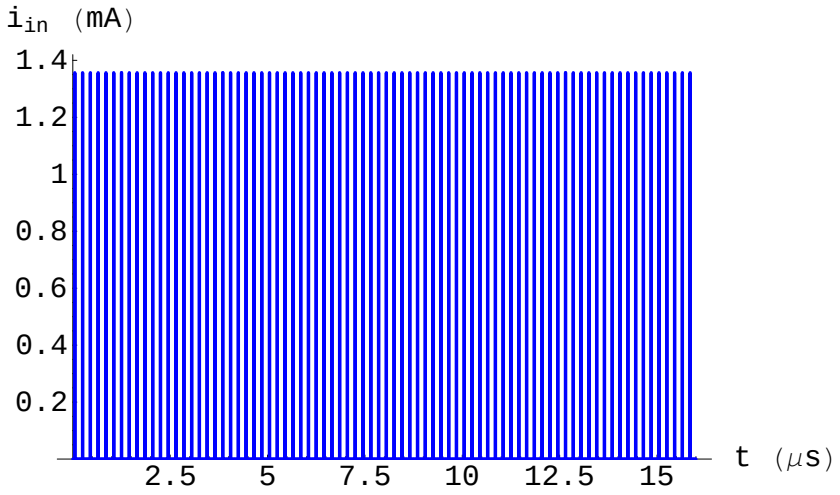


(a) Pulse train $i_{in}\,(t)$.

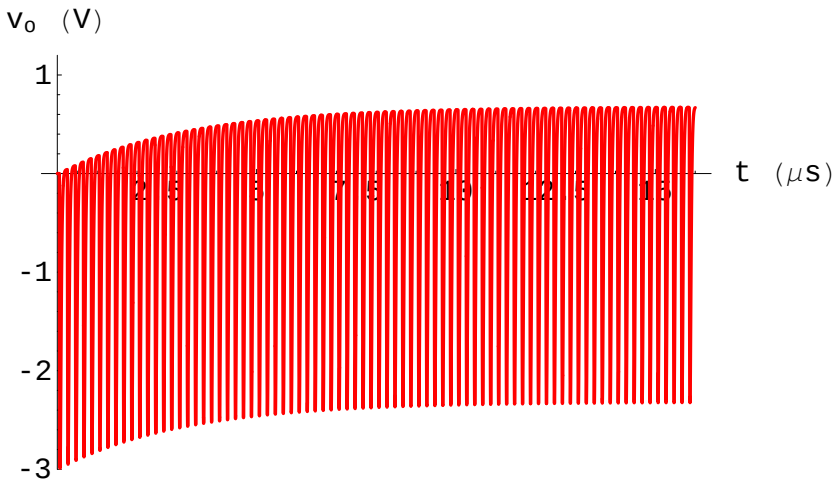


(b) Circuit response $v_{out}\,(t)$ (analytical model).

Figure 3.46: Circuit response to a train of pulses (rate $r = 5\,\mathrm{MHz}$).

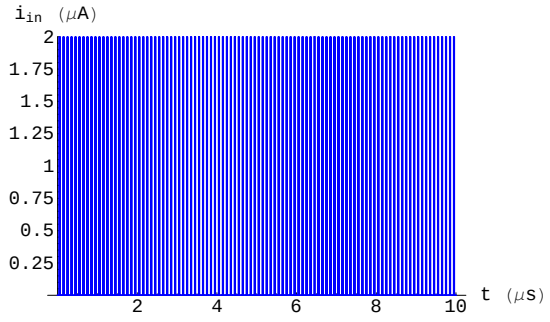


(a) Pulse train $i_{in}(t)$.

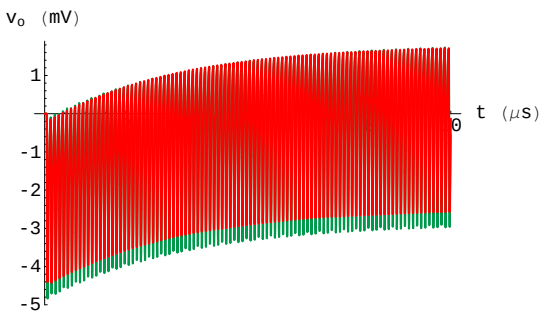


(b) Circuit response $v_{out}(t)$ (analytical model).

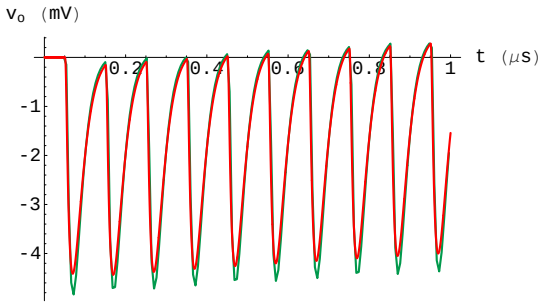
Figure 3.47: Circuit response to a train of large pulses (rate $r = 5\,\text{MHz}$).



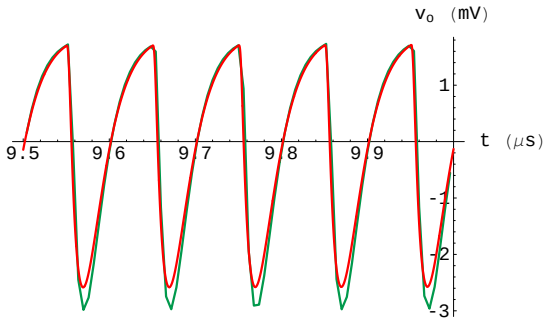
(a) Pulse train $i_{in}\,(t)$.



(b) Circuit response $v_{out}\,(t)$ (*Red* line: analytical model. *Green* line: transistor-level model).



(c) The first ten pulses.



(d) The last five pulses.

Figure 3.48: Slow-circuit response to a train of pulses (rate $r = 10\,\text{MHz}$).

$r = 10\,\text{MHz}$ is applied to the circuit input and the *pile-up* phenomenon occurs.

Let us further note that all the simulations predicting the circuit response to a pulse train have been performed by setting a constant pulse rate giving rise to an asymptotic voltage drift.

However in practice baseline fluctuations occur due to the random arrival of the pulses.

It is known that the number of events (pulse arrivals) occurring in a time interval t follows the Poisson distribution so that the time elapsing between two consecutive events follows an exponential distribution, as can be shown.

As far as the output voltage drift is concerned, a slew-rate limited non-linear

buffer will be inserted before the transconductor block to form a new block which is often referred to as BLH (baseline holder).

This buffer performs the function of dynamically clipping the pulses to be processed by the transconductor block (the low-pass filter) in order to greatly reduce their area.

However, this dynamic attenuation only occurs for fast and large signals, thus allowing the feedback network of the second stage to perform its function properly stabilising the low-frequency baseline fluctuations.

Chapter 4

Modelling the Non-Linear Buffer

The previous chapter has pointed out the need to accomplish a correct stabilisation of the circuit output baseline especially for fast and large signals.

A slew-rate limited non-linear buffer dynamically clipping the pulses has been presented as the best solution to our problem.

Thus, in this chapter this non-linear buffer will be taken into consideration and a model allowing for its non-linearity will be presented and analysed.

This model will be used for performing some useful computer simulations which will allow us to find the best values of the buffer slew-rate and bandwidth in order to design the buffer correctly at transistor level.

4.1 Time Domain Analysis of the Full Circuit

In order to predict the circuit behavior after inserting the slew-rate limited non-linear buffer, a circuit analysis in the time domain must be performed due to the non-linearity of this new component.

However we will first describe the circuit behavior without the buffer to check that our results are the same as those obtained in the previous chapter, where the whole circuit analysis in the frequency domain has been performed.

4.1.1 Time Domain Analysis of the Circuit without the Buffer

By referring to Fig. 4.4 we are able to write the equations making up the linear system describing the circuit behavior in the time domain.

Thus from KCL at the input node,

$$\frac{v_{\text{in}} - v_{\text{out}}^{\text{I}}}{R_{\text{f}}} + C_{\text{f}} \frac{\text{d}}{\text{d}t} (v_{\text{in}} - v_0) + C_{\text{d}} \frac{\text{d}v_{\text{in}}}{\text{d}t} = -i_{\text{in}} \tag{4.1}$$

From KCL at node (1),

$$C_{\text{f}} \frac{\text{d}}{\text{d}t} (v_0 - v_{\text{in}}) + \frac{v_0}{R_{\text{L}}} + C_{\text{L}} \frac{\text{d}v_0}{\text{d}t} + G_{\text{m}}\, v_{\text{in}} = 0 \tag{4.2}$$

From KCL at node (2),

$$\frac{v_{\text{out}}^{\text{I}} - v_{\text{in}}}{R_{\text{f}}} + \frac{v_{\text{out}}^{\text{I}} - v_{\text{in}}^{\text{II}}}{R} + \frac{v_{\text{out}}^{\text{I}} - B_0\, v_0}{R_{\text{o}}} = 0 \tag{4.3}$$

From KCL at node (3) by letting $A_{\text{v0}}\, \bar{v_{\text{c}}} = v_{\text{out}}$,

$$\frac{v_{\text{in}}^{\text{II}} - v_{\text{out}}^{\text{I}}}{R} - G_{\text{m0}}\, v_{\text{c}} + \frac{v_{\text{in}}^{\text{II}} - v_{\text{out}}}{R_{\text{sh}}} + C_{\text{sh}} \frac{\text{d}}{\text{d}t} \left(v_{\text{in}}^{\text{II}} - v_{\text{out}}\right) = 0 \tag{4.4}$$

From KCL at node (4) by setting $\bar{R}\,\bar{C} = \tau_{\text{OTA}}$, $\bar{g}_{\text{m}}\,\bar{R} = 1$ and $\bar{v_{\text{c}}} = v_{\text{out}}/A_{\text{v0}}$,

$$\frac{v_{\text{out}}}{\tau_{\text{OTA}}} + \frac{\text{d}v_{\text{out}}}{\text{d}t} + \frac{A_{\text{v0}}\, v_{\text{in}}^{\text{II}}}{\tau_{\text{OTA}}} = 0 \tag{4.5}$$

From KCL at node (5) by setting $R\,C = \tau_{\text{HP}}$ and $g_{\text{m}}\,R = 1$,

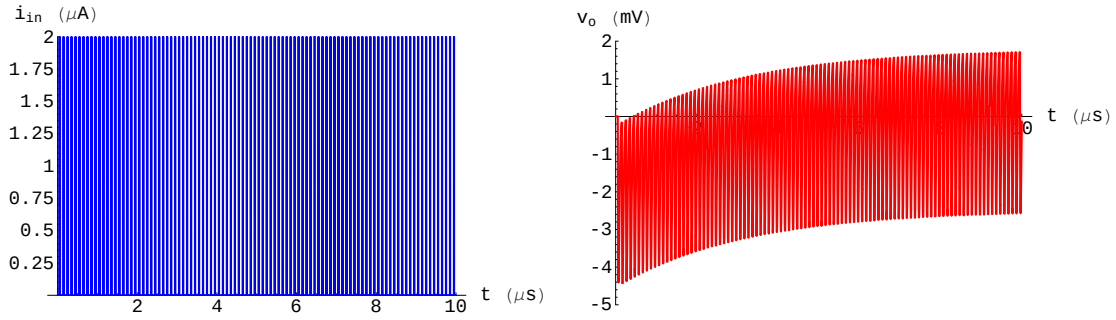
$$\frac{v_{\text{c}}}{\tau_{\text{HP}}} + \frac{\text{d}v_{\text{c}}}{\text{d}t} - \frac{v_{\text{out}}}{\tau_{\text{HP}}} = 0 \tag{4.6}$$

Numerically solving for $v_{\text{out}}\,(t)$ the system consisting of the preceding equations gives the graphical result shown in Fig. 4.1 in the case when $i_{\text{in}}\,(t)$ represents a pulse train whose rate is $r = 10\,\text{MHz}$, as shown in Fig. 4.1(a).

Then, by comparing Fig. 4.1(b) to Fig. 3.48(b) we can check graphically that the two different approaches to calculate the pulse train response of the circuit have led to the same results.

4.1.2 Modelling the Non-Linear Buffer

In order to find a model suitable for representing the non linear behavior of our buffer for large input signals, let us consider the large-signal performance of an op amp in a unity-gain feedback configuration.



(a) Pulse train $i_{in}(t)$.

(b) Circuit response $v_{out}(t)$ (analytical model).

Figure 4.1: Slow-Circuit response to a train of pulses (rate $r = 10\,\text{MHz}$).

If we really tested the performance of an op amp in such a configuration by applying a large step input voltage, we would find that the output voltage exhibits a response completely different to the one that a small-signal analysis would predict.

In fact we would see that the output voltage is a fairly slow ramp of almost constant slope instead of being an exponential curve approaching the step input voltage.

The maximum rate of change of the output voltage in the region of constant slope is called the *slew rate* (SR).

The difference between the predicted and the observed behavior is due to the fact that in our test the op amp operates completely out of its linear range, because of the large input step voltage applied at its input terminal.

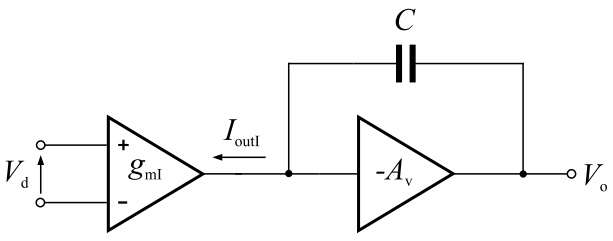


Figure 4.2: A block diagram of a two-stage op amp with Miller compensation capacitor.

To realise the origin of the slew-rate limitations characterising the op amp we can refer to the simplified block diagram shown in Fig. 4.2 representing a two-stage op

amp. The first block represents the op-amp input differential pair whereas the second block represents a high-gain output stage together with the Miller compensation capacitor C.

Since the high-gain output stage acts as an integrator, the output voltage can be expressed as

$$V_{\mathrm{o}} = \frac{1}{C} \int I_{\mathrm{outI}} \, \mathrm{d}t \tag{4.7}$$

When the op amp is forced to operate nonlinearly, it responds by charging the compensation capacitor with the maximum current available, namely the tail current of the differential input stage.

Thus, by assuming that $2\,I_1$ represents this constant current, we have

$$\mathrm{SR} = \frac{2\,I_1}{C} \tag{4.8}$$

and this equation results in the observed constant rate of change of V_{o} mentioned earlier.

A very approximate large-signal transfer characteristic which takes into account the preceding considerations is shown in Fig. 4.3.

The slope of this curve in the linear region corresponds to the small-signal transconductance of the input stage (g_{mI}).

Let us observe that the op-amp simplified representation of Fig. 4.2 contains all the main parameters concerned with the calculation of the SR and the amplifier bandwidth.

Moreover, although this model has been conceived by referring to a particular case, it is suitable for representing the behavior of most circuits operating in a similar way.

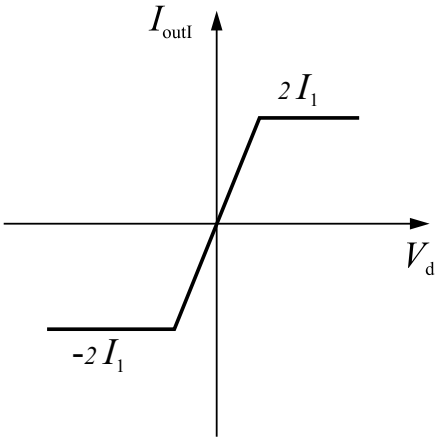


Figure 4.3: Very approximate large-signal transfer characteristic of the input stage.

Let us now calculate an approximate expression for the small-signal transfer function of our op amp when it is used in a unity-gain feedback configuration.

Referring to the model shown in Fig. 4.2 and assuming that the input stage has an infinite output resistance as well as the high-gain output stage an infinite input

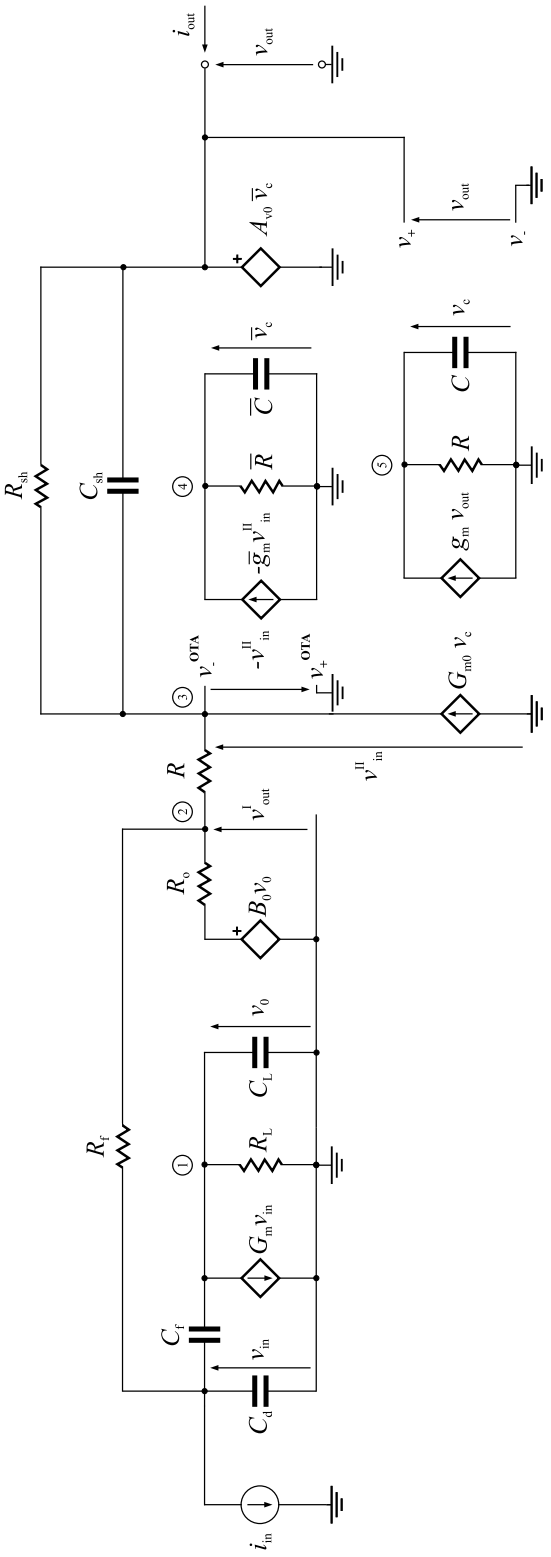


Figure 4.4: The full equivalent circuit for the time domain analysis.

resistance and a zero output resistance, gives

$$\frac{V_{\mathrm{o}}}{V_{\mathrm{d}}} = \frac{V_{\mathrm{o}}}{I_{\mathrm{outI}}} \frac{I_{\mathrm{outI}}}{V_{\mathrm{d}}} = \left(\frac{A_{\mathrm{v}}}{1 + A_{\mathrm{v}}} \right) \frac{g_{\mathrm{mI}}}{s\,C} \simeq \frac{g_{\mathrm{mI}}}{s\,C} \tag{4.9}$$

due to the high gain A_{v}.

Thus, if our op amp is used in a unity-gain feedback configuration we have $V_{+} = V_{\mathrm{in}}$, $V_{-} = V_{\mathrm{o}}$ and hence $V_d = V_{\mathrm{in}} - V_{\mathrm{o}}$, so that

$$\frac{V_{\mathrm{o}}}{V_{\mathrm{in}}} \simeq \frac{1}{1 + s\ (C/g_{\mathrm{mI}})} \tag{4.10}$$

Hence the –3-dB frequency of our buffer is connected to the model parameters through the approximate relationship

$$f_{-3\,\mathrm{dB}}^{\mathrm{buf}} \simeq \frac{g_{\mathrm{mI}}}{2\pi\,C} \tag{4.11}$$

4.1.3 Time Domain Analysis of the Circuit with the Buffer

The analysis performed in the previous section allows us now to write the time-domain equations describing the circuit behavior after inserting the non-linear buffer.

Thus by referring to Fig. 4.5 which shows the whole equivalent circuit including the non-linear buffer, we are able to write the new non-linear system governing the circuit.

Equations (4.1), (4.2), (4.3), (4.4), (4.5) still apply here. On the other hand equation (4.6) must be written now as

$$\frac{v_{\mathrm{c}}}{\tau_{\mathrm{HP}}} + \frac{\mathrm{d}v_{\mathrm{c}}}{\mathrm{d}t} - \frac{v_{\mathrm{out}}^{\mathrm{buf}}}{\tau_{\mathrm{HP}}} = 0 \tag{4.12}$$

and a supplementary non-linear differential equation representing the buffer behavior must be added.

This equation can be written as

$$C\,\frac{\mathrm{d}v_{\mathrm{out}}^{\mathrm{buf}}}{\mathrm{d}t} = I_{\mathrm{outI}}\left(V_{\mathrm{d}}\left(t\right)\right) \tag{4.13}$$

where

$$V_{\mathrm{d}}\left(t\right) = v_{\mathrm{out}} - v_{\mathrm{out}}^{\mathrm{buf}} \tag{4.14}$$

due to the unity-gain feedback configuration of our op-amp model, and $I_{\mathrm{outI}}\left(V_{\mathrm{d}}\right)$ represents the shape of the large-signal transfer characteristic of the input stage of the model.

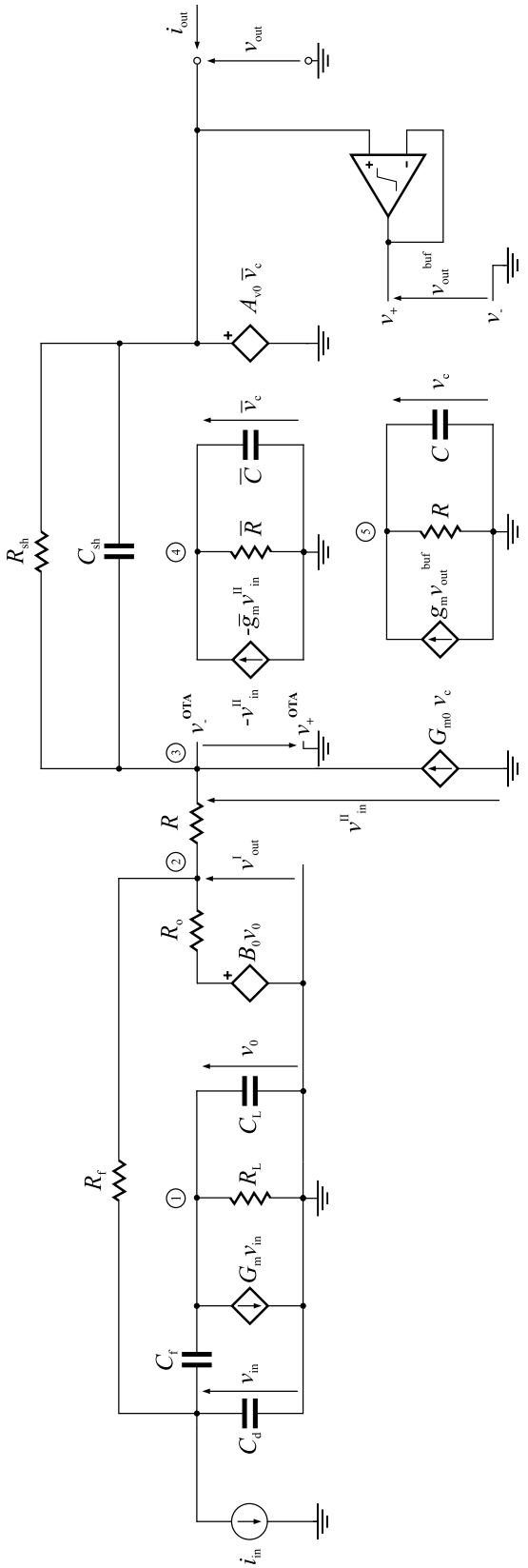


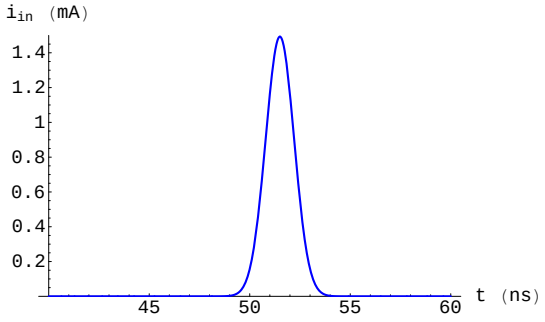
Figure 4.5: The full equivalent circuit for the time domain analysis including the non-linear buffer.

4.2 Computer Simulations of the Full Circuit

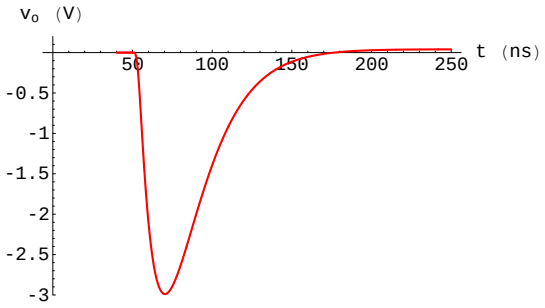
In this section we will present the graphical results obtained by numerically solving the non-linear system governing the circuit and given in the preceding section.

The purpose of these simulations is to find the best slew-rate values satisfying the strict design specifications such as the maximum tolerable fluctuation of the circuit output baseline, namely from 1 mV to 3 mV for 3-V output signals.

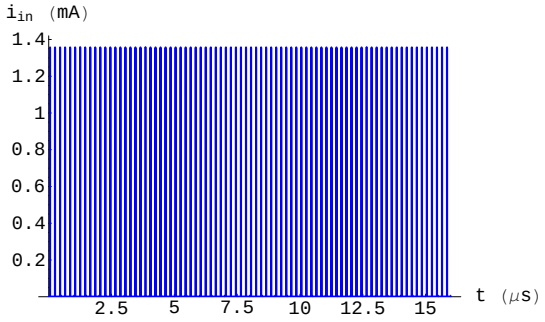
Moreover, in agreement with the considerations stated at the end of the previous chapter, the simulations have been performed even in the case of a narrower output signal (fast option) in order to take into account further circuit performance improvements.



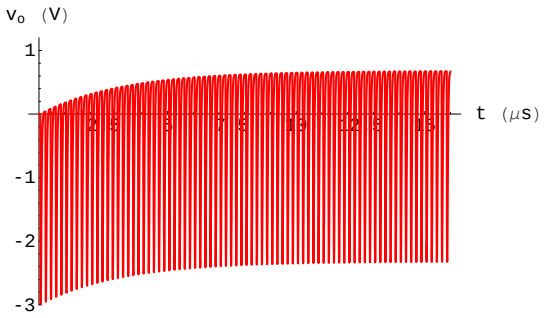
(a) Single input current pulse.



(b) Corresponding output voltage signal.



(c) Pulse train $i_{in}\,(t)$.



(d) Circuit response $v_{out}\,(t)$.

Figure 4.6: Slow-circuit response (no buffer) to a single large pulse and a train of large pulses (rate $r = 5\,\text{MHz}$).

Figure 4.6(a) shows the shape of the input current pulse (giving a 3-V output signal) which has been used for our computer simulations. From an analytical point of view this signal is given by

$$i_{in}(t) = h_{\max}\, e^{-k\,(t-t_{\max})^2} \tag{4.15}$$

where $h_{\max}$ and $t_{\max}$ represent the coordinates of the pulse peak.

The charge carried by this pulse is approximately equal to 2.7 pC.

The response of the slow circuit without the buffer to a sequence of such pulses is shown in Fig. 4.6(d). By inspecting the figure we can observe a baseline shift of about 0.7 V.

4.2.1 Slew-Rate Symmetrically Limited Buffer

In this subsection we consider the simulations performed by assuming that the large-signal transfer characteristic of the input stage of our op-amp model had the shape shown in Fig. 4.7.

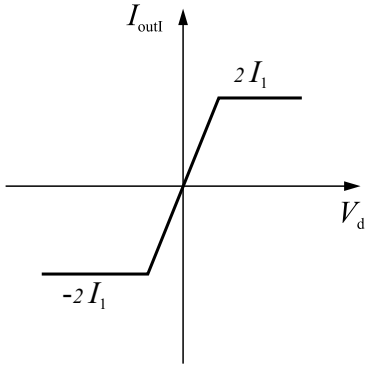


Figure 4.7: Large-signal transfer characteristic of the input stage.

By direct inspection of the figure we can predict that the constant rate of change of the buffer output voltage will be

$$\mathrm{SR}_1 = \frac{2\,I_1}{C} \tag{4.16}$$

when the buffer operates nonlinearly and $V_\mathrm{d} > 0$, and

$$|\,\mathrm{SR}_2\,| = \frac{2\,I_1}{C} \tag{4.17}$$

when the buffer operates nonlinearly and $V_\mathrm{d} < 0$.

Thus, due to the symmetry of the large-signal transfer characteristic, we have $\mathrm{SR}_1 = |\,\mathrm{SR}_2\,|$. This is what we mean with the expression slew-rate symmetrically limited buffer.

Moreover, by opportunely setting the values of I_1 and C, in theory we are able to set the slope of the output ramp. However in practice several design constraints mean that the desired SR value is not always so easy to obtain.

Let us now give the analytical form of the function $I_{\mathrm{outI}}(V_{\mathrm{d}})$ shown in Fig. 4.7. This function is to be substituted into (4.13) to solve the system in the case under examination.

We have

$$I_{\mathrm{outI}}(V_{\mathrm{d}}) = \begin{cases} -2\,I_1 & V_{\mathrm{d}} < -\dfrac{2\,I_1}{g_{\mathrm{mI}}} \\ g_{\mathrm{mI}}\,V_{\mathrm{d}} & -\dfrac{2\,I_1}{g_{\mathrm{mI}}} \le V_{\mathrm{d}} < \dfrac{2\,I_1}{g_{\mathrm{mI}}} \\ 2\,I_1 & V_{\mathrm{d}} \ge \dfrac{2\,I_1}{g_{\mathrm{mI}}} \end{cases} \tag{4.18}$$

However after several simulations performed by varying SR, we realised that the resulting symmetrical shape of the buffer output voltage (a signal in the shape of a isosceles triangle) is not able to provide a baseline stabilisation which meets the given specifications.

We also realised that the efficiency of this baseline stabilisation method is too dependent on the pulse shape and width. Thus we decided not to continue such simulations.

4.2.2 Slew-Rate Asymmetrically Limited Buffer

Let us now consider the simulations performed by assuming that the large-signal transfer characteristic of the input stage of our op-amp model had the shape shown in Fig. 4.8.

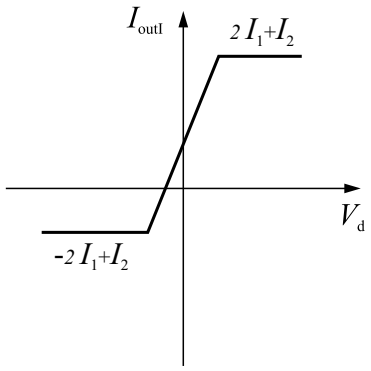


Figure 4.8: Large-signal transfer characteristic of the input stage.

By letting

$$I_{\mathrm{MAX1}} = 2\,I_1 + I_2$$

and

$$I_{\mathrm{MAX2}} = 2\,I_1 - I_2$$

and further assuming $I_2 < 2\,I_1$, we can predict that the constant rate of change of the buffer output voltage will now be

$$\mathrm{SR}_1 = \frac{I_{\mathrm{MAX1}}}{C} \tag{4.19}$$

when the buffer operates nonlinearly and $V_\mathrm{d} > 0$, and

$$|\,\mathrm{SR}_2\,| = \frac{I_\mathrm{MAX2}}{C} \tag{4.20}$$

when the buffer operates nonlinearly and $V_\mathrm{d} < 0$.

The analytical form of the function $\bar{I}_\mathrm{outI}\,(V_\mathrm{d})$ shown in Fig. 4.8 can be found by simply adding a constant term I_2 to $I_\mathrm{outI}\,(V_\mathrm{d})$ given in (4.18). This function is to be substituted into (4.13) to solve the system in the case under examination.

Unlike the symmetrical case the simulations performed in the asymmetrical case by varying SR have given interesting results and have allowed us to obtain two slew-rate values providing a baseline fluctuation which meets the specifications.

These values are $I_1 = 107.5\,\mathrm{nA}$, $I_2 = 185\,\mathrm{nA}$ (from which $I_\mathrm{MAX1} = 400\,\mathrm{nA}$, $I_\mathrm{MAX2} = 30\,\mathrm{nA}$) and $C = 1\,\mathrm{pF}$, from which

$$\mathrm{SR}_1 = \frac{I_\mathrm{MAX1}}{C} = 0.4\,\frac{\mathrm{V}}{\mu\mathrm{s}} \tag{4.21}$$

and

$$|\,\mathrm{SR}_2\,| = \frac{I_\mathrm{MAX2}}{C} = 0.03\,\frac{\mathrm{V}}{\mu\mathrm{s}} \tag{4.22}$$

The graphical outputs obtained by using the above values and setting $g_\mathrm{mI} = 1\,\mathrm{mS}$ (it will be shown later that this value plays an important role only in determining the proper buffer bandwidth) are shown in Fig. 4.9 in the case of the slow circuit and in Fig. 4.10 in the case of the fast circuit (in this case narrower output signals have been obtained by setting $R_\mathrm{f} = 4.408\,\mathrm{k\Omega}$ and $C_\mathrm{sh} = 186.964\,\mathrm{fF}$).

By examining Fig. 4.9(d) we can appreciate a maximum baseline shift approximately equal to 2.2 mV with the buffer to be compared to the approximate value of 0.7 V without the buffer, shown in Fig. 4.6(d).

The above value of maximum baseline shift has been obtained in the case of the slow circuit at a pulse rate $r = 5\,\mathrm{MHz}$ to avoid the *pile-up* effect.

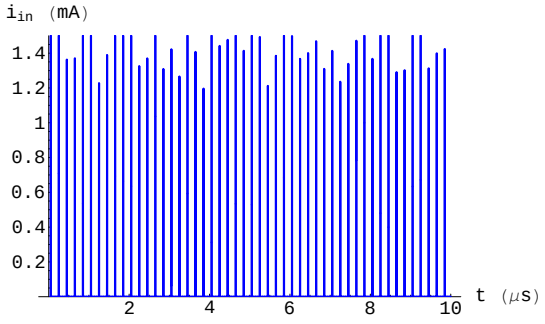
However further simulations have shown that baseline-shift values satisfying the given design specifications can be still found up to a rate $r = 6.2\,\mathrm{MHz}$ (shift predicted: 2.75 mV).

On the other hand, by examining Fig. 4.10(d) we can appreciate a maximum baseline shift approximately equal to 0.7 mV with the buffer to be compared to the approximate value of 0.4 V obtained without the buffer (not shown).

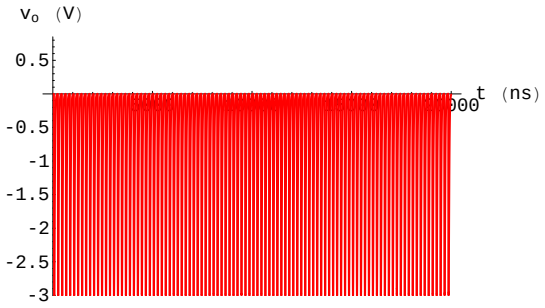
Moreover, unlike the preceding case, this maximum value of baseline shift has been obtained in the case of the fast circuit at a pulse rate $r = 10\,\text{MHz}$ without the *pile-up* effect occurring.

In fact, reducing the time length of the output pulses gives very good results even at a high counting rate and results in an important improvement of the circuit performance.

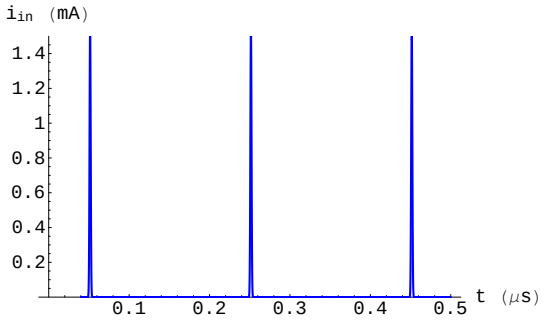
In particular the fast circuit is able to work properly up to a rate $r = 10\,\text{MHz}$ because the time length of its output pulses is nearly the half of the one of the slow-circuit output pulses.



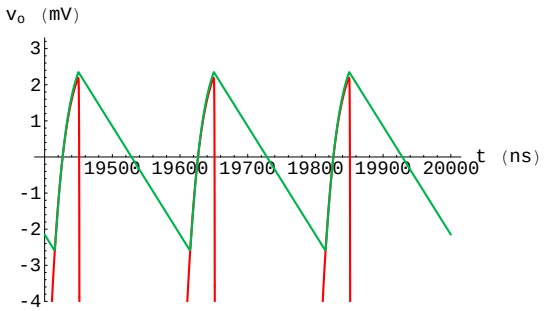
(a) Pulse train $i_{in}\,(t)$.



(b) Circuit response (with buffer) $v_{out}\,(t)$.

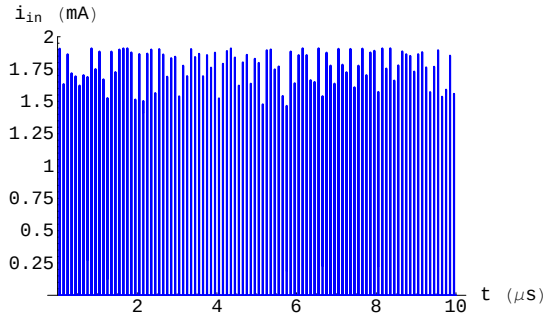


(c)

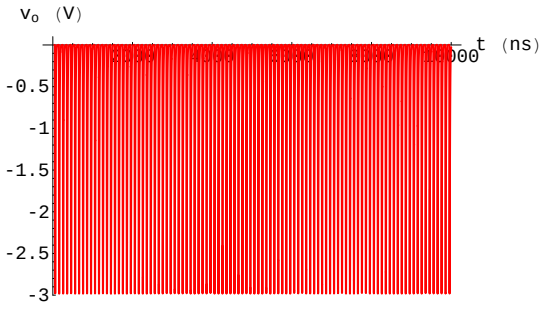


(d) The last three pulses (*Red* line: circuit output voltage. *Green* line: buffer output voltage).

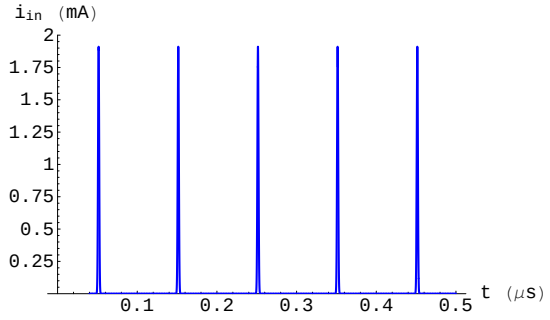
Figure 4.9: Slow-circuit response to a train of pulses (rate $r = 5\,\text{MHz}$).



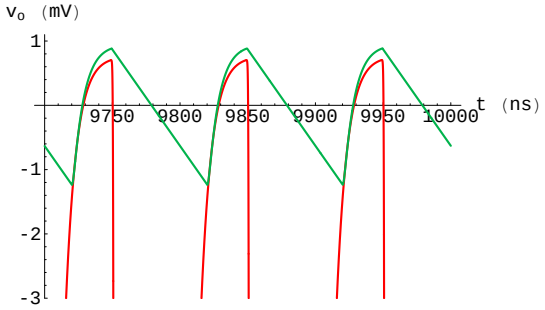
(a) Pulse train $i_{in}(t)$.



(b) Circuit response (with buffer) $v_{out}(t)$.



(c)



(d) The last three pulses (*Red* line: circuit output voltage. *Green* line: buffer output voltage).

Figure 4.10: Fast-circuit response to a train of pulses (rate $r = 10\,\text{MHz}$).

4.2.3 Circuit Response to Bipolar Incoming Pulses

So far we have considered the circuit response to a sequence of unipolar incoming pulses. In fact this is in exact agreement with the detector features.

However, even the circuit response to pulses of opposite sign to that of the main pulses must be taken into consideration, due to the fact that a sporadical presence of such pulses is likely to exist (due to noise, for example).

Obviously, because of the non-symmetrical behavior of the buffer we can imagine that the circuit response to pulses of opposite sign to that of the main pulses will not give the same good results shown in the previous section, due to the strong one-directional slew-rate limitation.

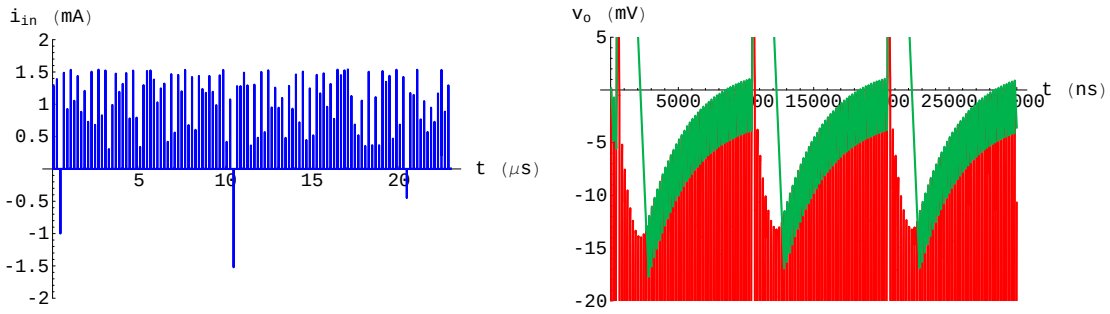
Thus, our aim is to check whether the slew-rate values optimised for the main pulses are able to provide at least a fairly fast restoration of the circuit's normal working conditions.

Figure 4.11(b) shows the slow-circuit response predicted by our analytical model by assuming that every fifty main pulses a pulse of opposite sign occurs.

On the other hand, Fig. 4.12(b) shows the fast-circuit response under the same above assumption.

By examining the graphical results we can observe that the slew-rate values we have chosen allow the circuit to manage fairly well even incoming pulses of opposite sign to that of the main pulses.

Finally we point out that the circuit response to higher noise pulse rates has not been taken into consideration because it does not seem realistic that the detector performance is worse than that we have previously supposed and analysed.



(a) Pulse train $i_{in}(t)$ with noise spikes (1 every 50).

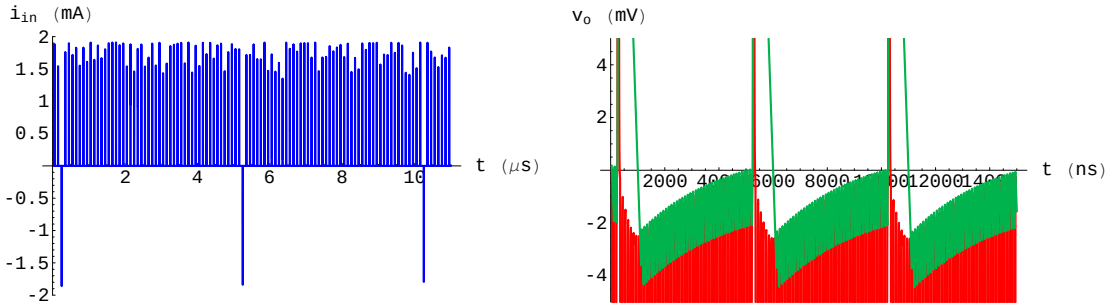
(b) Magnification of the circuit output voltage region near the t axis.

Figure 4.11: Slow-circuit response (with buffer) to a train of pulses with noise spikes (rate $r = 5\,\mathrm{MHz}$).

4.2.4 The Buffer Bandwidth

The simulation results so far examined have concerned only the buffer slew-rate best values. Moreover, as mentioned earlier, all these simulations have been performed by setting $g_{\mathrm{mI}} = 1\,\mathrm{mS}$.

This is correct since in practice and also in our model the buffer slew rate and



(a) Pulse train $i_{in}(t)$ with noise spikes (1 every 50).

(b) Magnification of the circuit output voltage region near the t axis.

Figure 4.12: Fast-circuit response (with buffer) to a train of pulses with noise spikes (rate $r = 10\,\text{MHz}$).

the buffer bandwidth can be considered independent of each other and thus taken into consideration separately.

However, in order to check the preceding assumption we have performed a test whose graphical result is shown in Fig. 4.13.

We have applied to the buffer an input signal consisting of a voltage step from 0 to -1 V followed by a second step from -1 V to 0 in order to test whether both the slew-rate values are really independent of the buffer bandwidth.

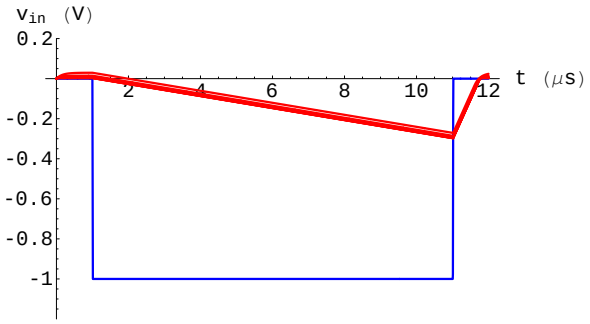
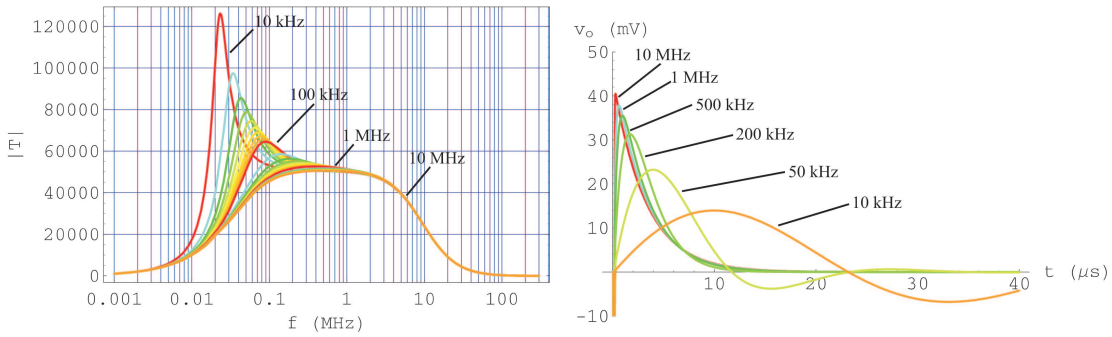


Figure 4.13: Buffer response to two consecutive large voltage steps (descending and ascending step).

Then we performed several simulations by varying the –3-dB frequency of the buffer from a value of 1 MHz to a value of 10 MHz in steps of 1 MHz. Even a –3-dB frequency value of 500 kHz has been tested (the first red line on high shown in Fig. 4.13).

By inspecting the figure we can note that the slope of both of the expected ramps (the descending ramp and the ascending ramp) turn out to be unaffected by the bandwidth changes.



(a) (b)

Figure 4.14: (a) Magnitude in Ω of the full-circuit small-signal transfer function (with buffer) and (b) slow-circuit single-pulse response (with buffer): magnification of the region (of a 3-V output signal) showing the baseline fluctuations occurring by varying the buffer pole position.

Let us now investigate the effect of the buffer bandwidth on the small-signal transfer function of the whole circuit, to find the bandwidth values which could involve the circuit instability.

The performed simulations have given the results shown in Fig. 4.14.

Figure 4.14(a) shows the magnitude of the small-signal transfer function of the full circuit including the buffer, by varying the position of the dominant pole characterising the unity-gain small-signal transfer function of the buffer.

By inspecting the figure we can see that a buffer bandwidth greater than 1 MHz is required in order to avoid the slow oscillations of the baseline shown in Fig. 4.14(b).

In fact, Fig. 4.14(b) allows us to appreciate the shape of such oscillations, in the case of the slow circuit, for a 3-V output signal as the buffer bandwidth changes.

Chapter 5

The Non-Linear Buffer: Transistor-Level Design and SPICE Simulations

In the previous chapter an analytical model suitable for representing the buffer large-signal behavior was presented.

The shape of the large-signal transfer characteristic giving the best results from a specification matching point of view has been investigated.

The best slew-rate values for the slew-rate asymmetrically limited buffer have been found and tested by means of *Mathematica* simulations.

Now, in this chapter the circuit designed to obtain the results predicted by the performed computer simulations will be presented and analysed.

We will also point out some circuit drawbacks arising especially when large and fast signals are processed.

Thus, we will show two alternative circuits able to improve circuit performance in order to overcome the encountered problems.

5.1 The Non-Linear Buffer Basic Circuit

In this section we will analyse the behavior of the circuit achieving the slew-rate limited non-linear buffer.

Figure 5.1 shows the schematic diagram of the circuit. By inspecting the figure we can note that a n-channel MOS source-coupled pair with a p-channel current-mirror

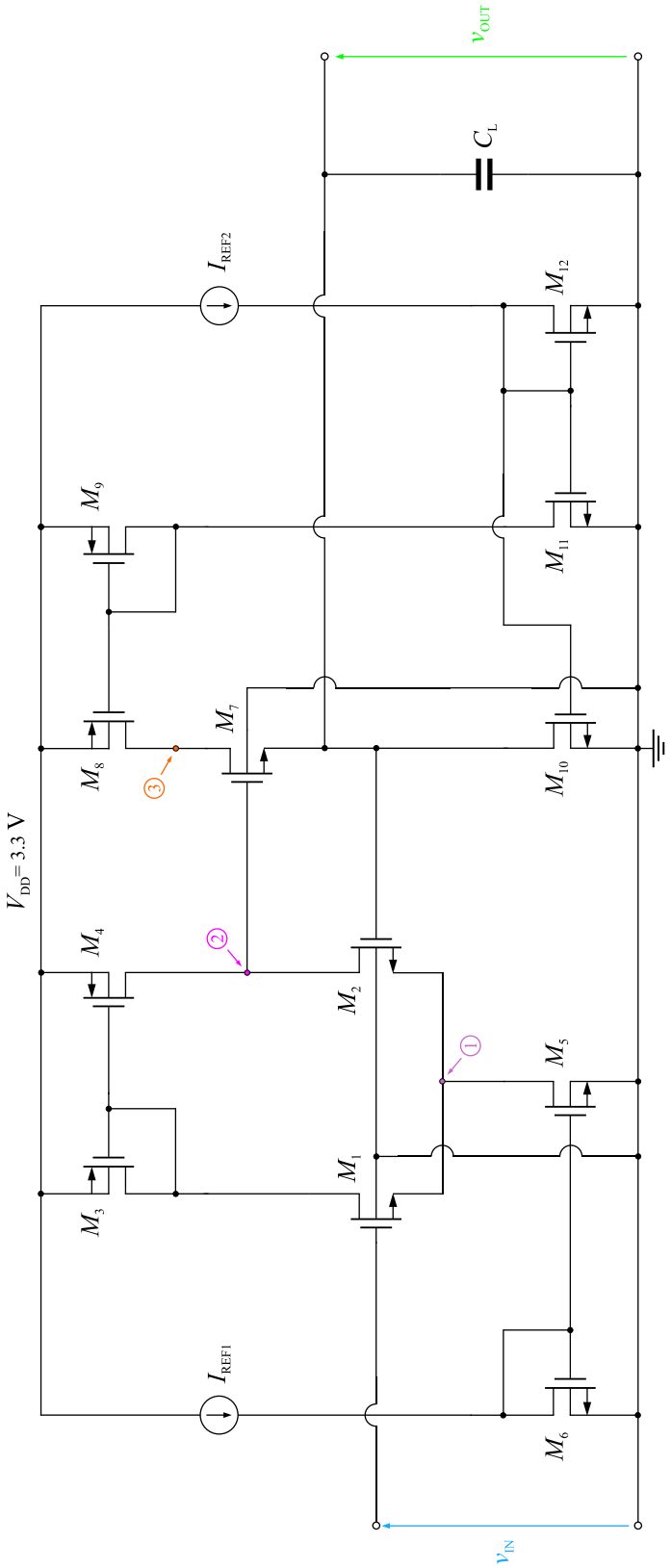


Figure 5.1: Circuit schematic diagram of the non-linear buffer.

load implements the differential input stage of the buffer whereas a common-drain configuration (source follower) consisting of an n-channel MOS with an n-channel MOS current-mirror load realises the single-ended output stage.

Furthermore a capacitive load C_{L} is connected between the source of M_7 (the circuit output) and ground.

We can add that a source follower has been used to drive this capacitive load due to its intrinsic feature of providing the asymmetrical slew-rate limitation whose advantages have been pointed out in the previous chapter.

On the other hand the p-channel MOS current mirror consisting of transistors M_8, M_9 only performs the function of limiting the current that M_7 would be able to pull down for charging the output capacitor.

However this topic will be discussed later when a detailed analysis of the large-signal circuit behavior will be carried out.

We only note here that the maximum value of this current can be set by choosing a proper value of the input current source of the mirror under consideration, namely the constant current pulled down by M_{11}.

Finally we can observe that a unity-gain negative feedback is provided by connecting the inverting terminal of the input differential pair to the output of the circuit.

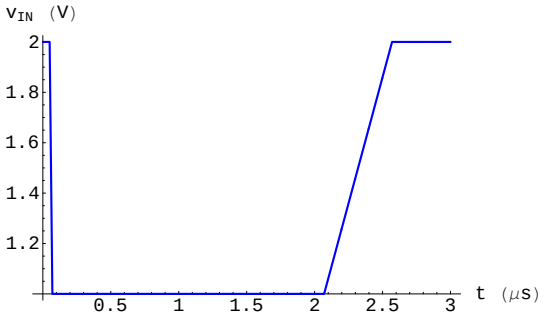
5.2 Large-Signal Behavior of the Buffer Circuit

In this section we will analyse the behavior of the actual circuit implementing the slew-rate limited buffer stage, from a large-signal standpoint.

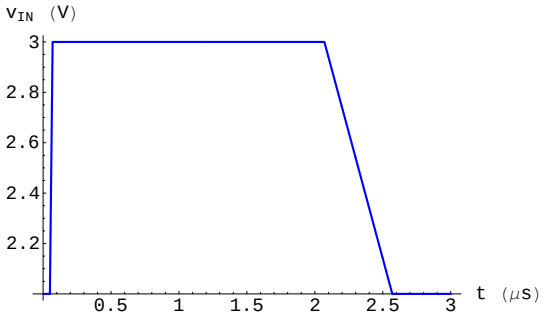
The graphic results of several transistor-level SPICE simulations will be shown and discussed in order to check whether the limiting function performed by the circuit corresponds to that required to satisfy the strict requirements on the maximum baseline shift.

SPICE simulations have been performed by applying to the circuit three different input voltage signals whose shape is shown in Fig. 5.2 together with the respective signals of opposite sign.

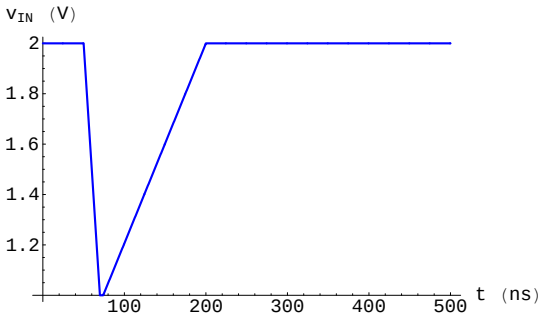
From the figure we can see that the applied input signals start from a dc voltage level of 2 V and reach a maximum voltage value of 3 V or a minimum voltage value of 1 V.



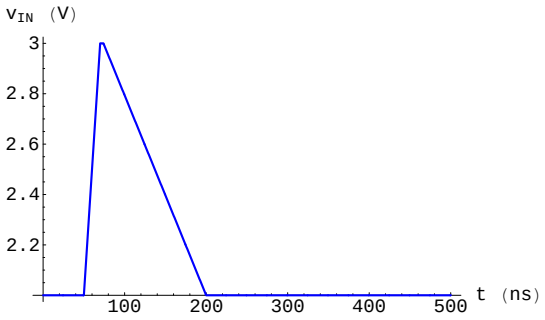
(a) Wide negative test signal



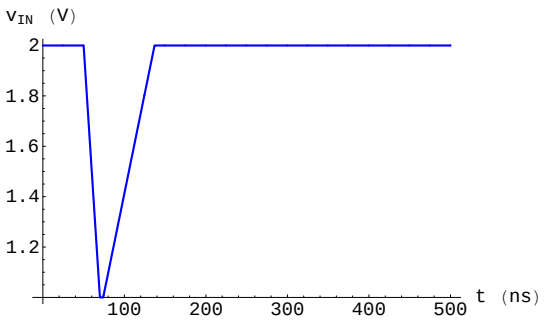
(b) Wide positive test signal



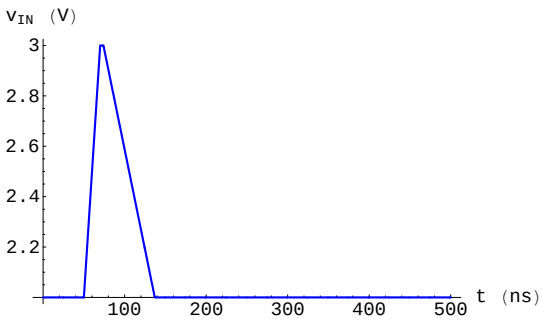
(c) Narrow negative test signal



(d) Narrow positive test signal



(e) Very narrow negative test signal



(f) Very narrow positive test signal

Figure 5.2: Input signals used to test the circuit large-signal performance.

The above value of 2 V has been set by taking into account that the circuit is used in a unity-gain feedback configuration causing the circuit dc output voltage to be very near to the input dc voltage level, namely 2 V in our case.

In fact, since the circuit output voltage also represents the source voltage of M_7 in our case and since the gate-source voltage of M_7 is approximately equal to 1 V, when the output voltage is set to 2 V the source-drain voltage of M_4 assumes a value of about 0.3 V which is almost the minimum value required to bias M_4 at the edge of the active region.

The preceding considerations highlight an important drawback of this circuit.

In fact it reduces to 2 V only the maximum output swing of the whole front-end circuit since we should recall that the dc output voltage of the whole circuit is really the dc input voltage of our buffer.

On the other hand a maximum output swing approximately equal to 3 V would be strongly recommendable to fully exploit the output dynamic range of the shaper.

To overcome this problem a change in the circuit schematic will be performed and shown in a following section.

5.2.1 Circuit Response to a Wide Test Signal

In this section we will analyse the circuit response to the first pair of test input signals shown in Fig. 5.2, namely the signals displayed in Fig. 5.2(a) and Fig. 5.2(b).

We will refer to these signals as wide test input signals, meaning that their time length (nearly 2.5 μs) is much greater than the one that the output signals of the whole front-end circuit (which will be the buffer input signals when it is inserted in the whole circuit) are assumed to have.

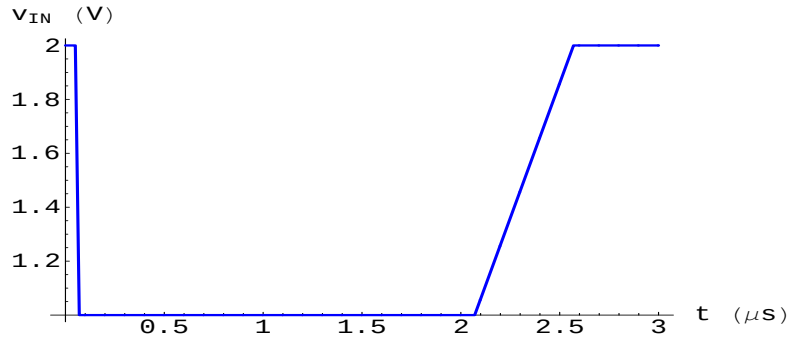
Moreover we will call the signal shown in Fig. 5.2(a) the negative test signal whereas the signal shown in Fig. 5.2(b) the positive test signal, where here the signals are considered to be negative and positive with respect to the dc value of 2 V.

Finally we will discuss in detail the buffer response to the wide test signals in order to obtain an insight into the large-signal behavior of the circuit under examination.

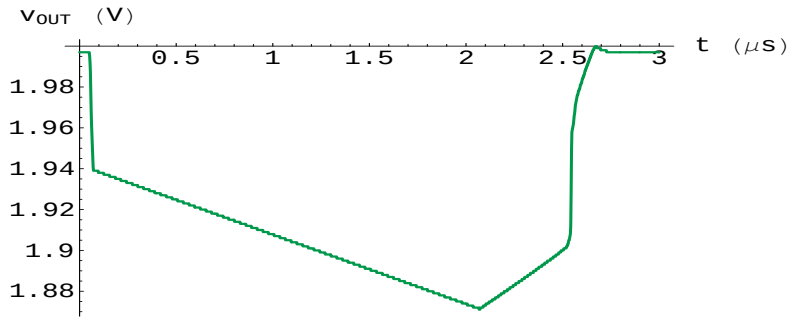
Negative Test Signal

Figure 5.3 and Fig. 5.4 show the time evolution of some significant circuit node voltages such as the input node, the output node and other interesting internal nodes, namely the nodes we labeled 1, 2 and 3 in the circuit diagram of Fig. 5.1.

On the other hand Fig. 5.5 shows the graphical superimposition of the above node voltages as well as the current flowing into the capacitor C_{L} in order to realise whether the two different slew-rate limitations occur (as far as the current flowing into the capacitor is concerned, let us recall that during the slewing period the capacitor is charged by a constant current whose value should be in agreement with the design value).

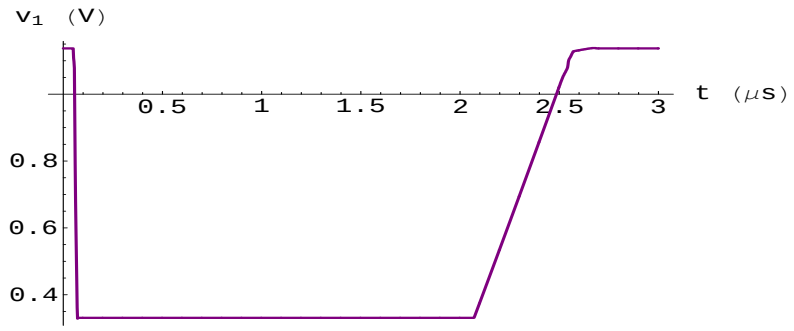


(a) Input voltage

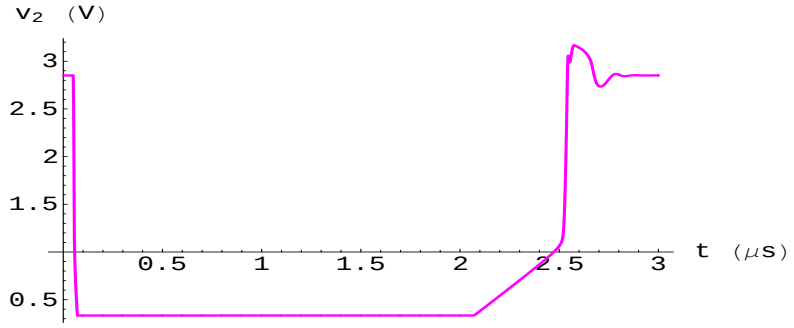


(b) Output voltage

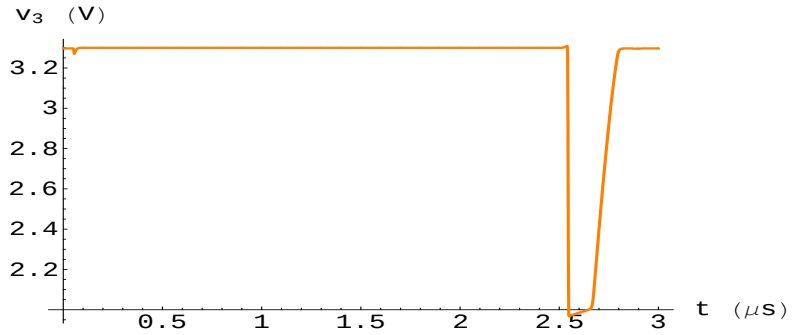
Figure 5.3: Time evolution of some significant circuit node voltages.



(a) Voltage at node 1

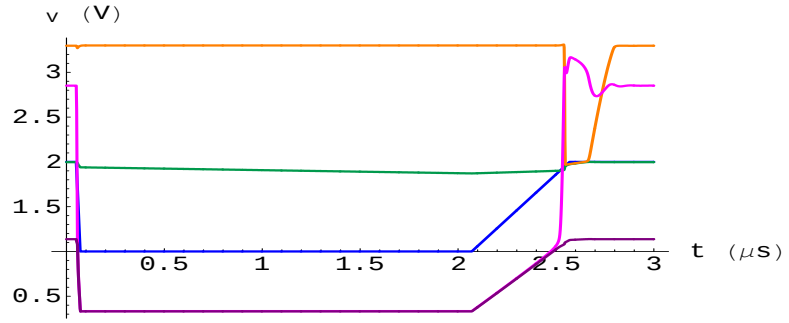


(b) Voltage at node 2

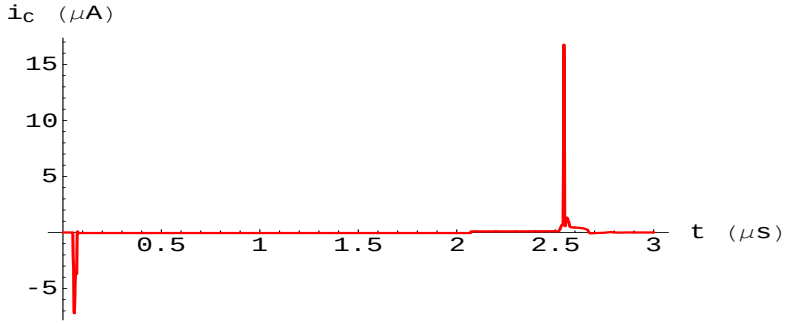


(c) Voltage at node 3

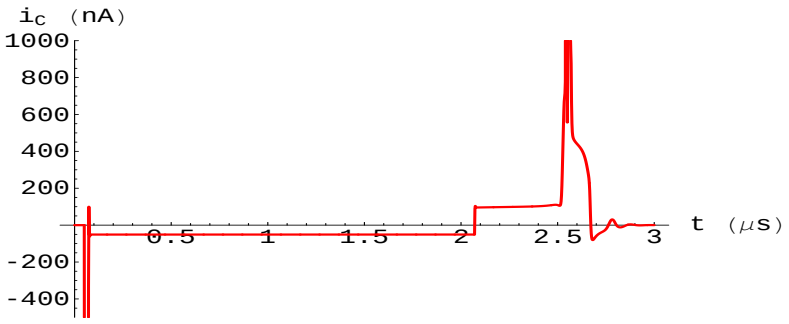
Figure 5.4: Time evolution of some significant circuit node voltages.



(a)



(b)



(c)

Figure 5.5: (a) Superimposition of some significant node voltages, (b) current flowing into the capacitor C_{L} and (c) magnification of the region near the t axis.

Thus, by interpreting the graphical results shown in Fig. 5.5(a) we are able to discuss the circuit behavior.

At the beginning the node voltages we are interested in have the quiescent values listed below

- $v_{\mathrm{IN}} = 2\,\mathrm{V}\,, v_{\mathrm{OUT}} = 1.997\,\mathrm{V}$
- $v_1 = 1.137\,\mathrm{V}\,, v_2 = 2.851\,\mathrm{V}\,, v_3 = 3.297\,\mathrm{V}$

The input signal v_{IN} is applied to the gate of M_1 and thus its gate voltage, following the signal, reaches the value of 1 V in only 20 ns (the signal fall time).

Since v_1 also represents the source voltage of M_1 and this transistor can be thought of as operating in a common-drain configuration (source follower), we can imagine that v_1 follows the gate voltage of M_1.

In fact, from a large-signal standpoint, v_1 is equal to the input voltage minus the gate-source voltage of M_1. As a result, if we assume that the gate-source voltage is approximately constant, v_1 will be simply offset from the input, as shown in Fig. 5.5(a).

On the other hand v_{OUT}, which is also the gate voltage of M_2, cannot respond instantaneously and is initially near to its quiescent value of about 2 V. In fact some charge must be removed from the capacitor C_{L} connected to the output node, in order to lower the output node voltage.

As a consequence the gate-source voltage of M_2 becomes much larger than the gate-source voltage of M_1 which is still approximately equal to its initial value, in agreement with the preceding considerations.

Thus the current pulled down by M_1 which is nearly the same current as the transistor M_4 pushes down due to the current mirror, is less than the current pulled down by M_2.

Then the voltage v_2 must diminish to reduce the current in M_2, forcing M_2 to operate in the triode region in order to satisfy KCL at node 2.

As a result the drain voltage of M_2 approaches the voltage v_1, as shown in Fig. 5.5(a), causing the gate-source voltage of M_7 to become largely negative so that M_7 is now forced to operate in the cutoff region.

Let us recall that at the beginning, before the signal arrived, M_7 operated in the active region whereas M_8 was forced to operate in the triode region.

In fact the value of the bias current of M_7 (50 nA) dictated by the current mirror M_{12}, M_{10} is less than the current value dictated by the current mirror M_{12}, M_{11} (500 nA) and pushed down by M_8 (due to the current mirror M_9, M_8) so that v_3 must rise to reduce the current in M_8 and satisfy KCL at node 3.

On the other hand, now, as mentioned before, M_7 operates in the cutoff region so that it pulls down zero current, causing v_3 to further rise to reach the maximum voltage value of 3.3 V (power supply), as shown in Fig. 5.5(a) or in Fig. 5.4(c).

Thus the output capacitor C_{L} is discharged at the expected constant rate $\mathrm{SR}_1 = I/C_{\mathrm{L}}$, where I is the constant bias current of M_7 (50 nA), as shown in Fig. 5.5(c).

The capacitor discharge continues till the output voltage becomes equal to the input voltage.

In fact, starting from this point the circuit behavior is reversed with respect to the one that we have so far described.

The input voltage is rising and its value becomes greater than the output voltage value so that now M_1 (and hence M_4) pulls down a current which is more than the current pulled down by M_2, causing v_2 to increase to reduce the current in M_4.

As v_2 increases also the gate-source voltage of M_7 increases, so that the current pulled down by M_7 causes the source-drain voltage of M_8 to rise until it enters the active region. Since the current pulled down by M_7 is more than the current pushed down by M_8 (500 nA), v_3 must diminish to reduce the current in M_7, forcing M_7 to operate in the triode region, as shown in Fig. 5.5(a).

During this period the output capacitor is charged for the output voltage to reach the value of 2 V.

However in this case it is quite difficult to appreciate the constant current of about 500 nA charging the capacitor since the voltage gap to be filled is so small (only a few tens of millivolts) that the above limitation of 500 nA only occurs for a very short time, as shown in Fig. 5.5(c).

It should also be pointed out that the shape of the output voltage shown in Fig. 5.3(b) has some drops (not predicted by the ideal model) at the points where the signal changes rapidly, due to the parasitic feedthrough of the input signal.

Because of this phenomenon some extra current (the peaks shown in Fig. 5.5(b) at the points where the signal changes rapidly) can charge or discharge the capacitor through alternative capacitive paths involving some circuit parasitic capacitances.

The capacitive feedthrough plays a crucial role in our case since it causes the

strong slew-rate limitation to occur only after the output voltage dropped a few tens of millivolts, as we can appreciate by inspecting Fig. 5.3(b).

This drop increases the total area of the output signal significantly so that we can imagine that this area will be too large to guarantee a baseline stabilisation in the order given by our design specifications.

One possible solution to this problem will be taken into consideration later.

Positive Test Signal

Let us consider the circuit response to the wide positive test signal shown in Fig. 5.2(b).

The circuit large-signal behavior is reversed now with respect to the one that we described in the preceding subsection so that a detailed analysis of the behavior in the case under consideration can be performed by following steps analogous to those previously discussed in detail for the opposite case (first of all we should take into consideration the situation that occurred at the end of the preceding analysis and vice versa).

The time evolution of the same node voltages as in the preceding case are shown separately in Fig. 5.6 and Fig. 5.7 as well as simultaneously in Fig. 5.8 to allow an immediate graphical check of the circuit behavior in this case.

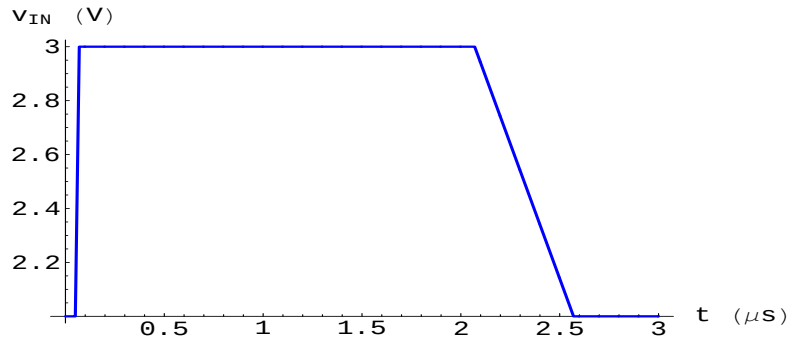
By examining Fig. 5.8(a) we can see that unlike in the preceding case, the capacitor current limitation to the value of about 500 nA is very evident now, due to the large voltage gap to be filled in this case for the output voltage to reach the input voltage.

Figure 5.8(c) shows very clearly what we stated above, even allowing us to appreciate the current limitation of about 50 nA occurring after the output voltage has crossed the descending input voltage ramp.

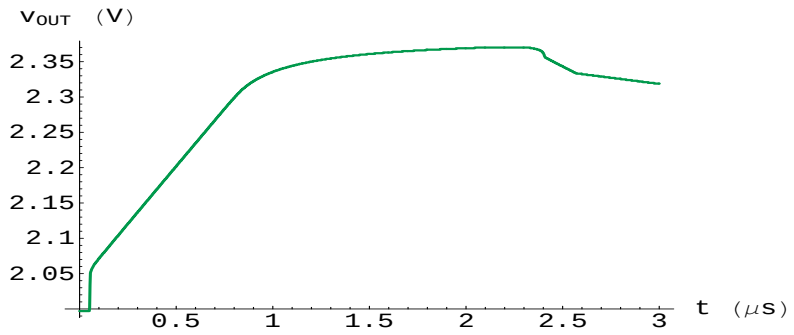
However, by further inspecting Fig. 5.8(a) we can note that the current limitation dictated by M_8 forcing M_7 to operate in the triode region halts when the output voltage reaches a value approximately equal to 2.35 V which is evidently sufficient to cause the gate-source voltage of M_7 to assume a value such that the current it pulls down is less than the current of 500 nA pushed down by M_8.

5.2.2 Circuit Response to a Narrow Test Signal

After investigating the circuit behavior by using a wide test input signal, in this section we are interested in testing the large-signal circuit response in the case when



(a) Input voltage



(b) Output voltage

Figure 5.6: Time evolution of some significant circuit node voltages.

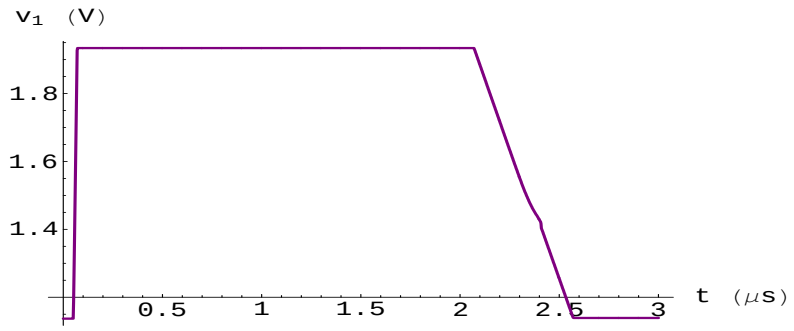
a narrow input signal is applied.

In fact the shape and time length of such a signal are fairly similar to the output signals that our actual circuit will present to the buffer input when the buffer is inserted in the whole circuit.

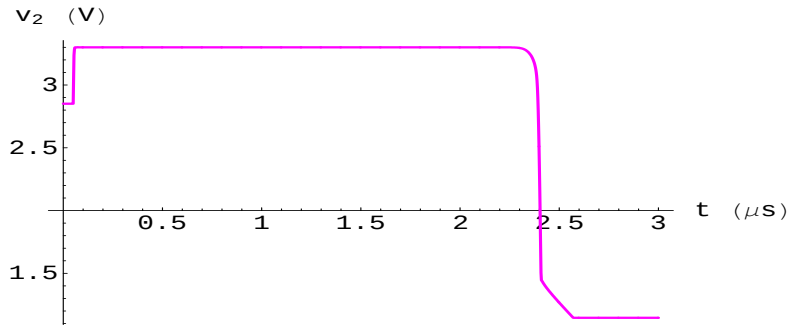
Negative Test Signal

The circuit response to the test signal shown in Fig. 5.2(c) is illustrated in Fig. 5.9 together with the current flowing into the capacitor C_{L}.

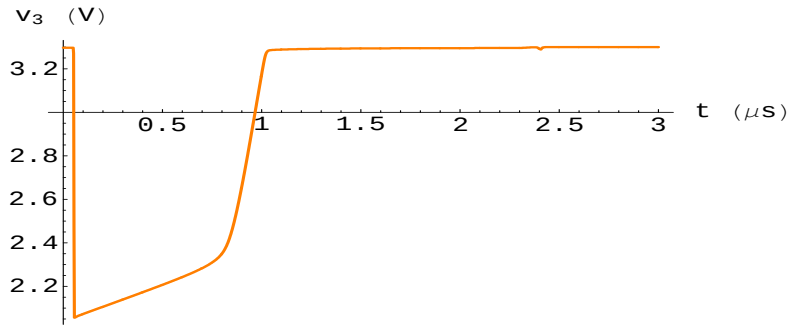
Let us note that the signal shows a fall time $t_{\mathrm{f}} = 20\,\mathrm{ns}$, a rise time $t_{\mathrm{r}} = 126\,\mathrm{ns}$ and a duration $t_{\mathrm{d}} = 4\,\mathrm{ns}$.



(a) Voltage at node 1

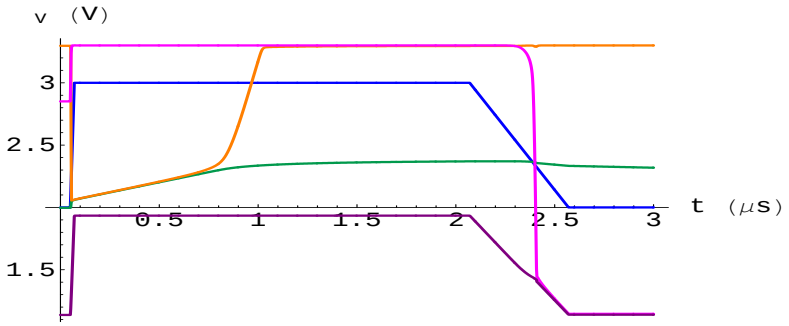


(b) Voltage at node 2

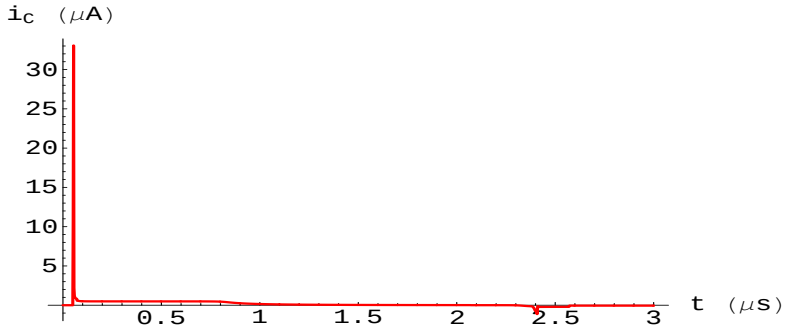


(c) Voltage at node 3

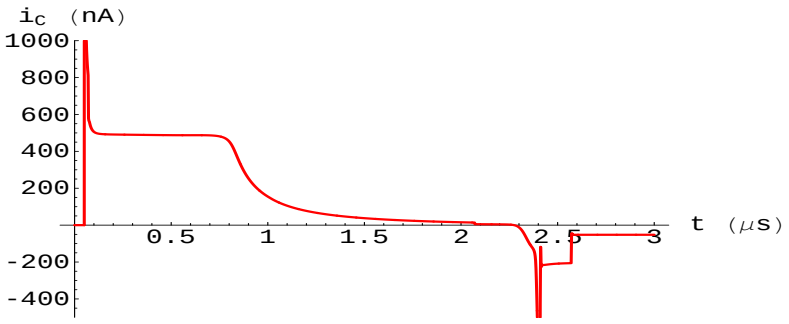
Figure 5.7: Time evolution of some significant circuit node voltages.



(a)

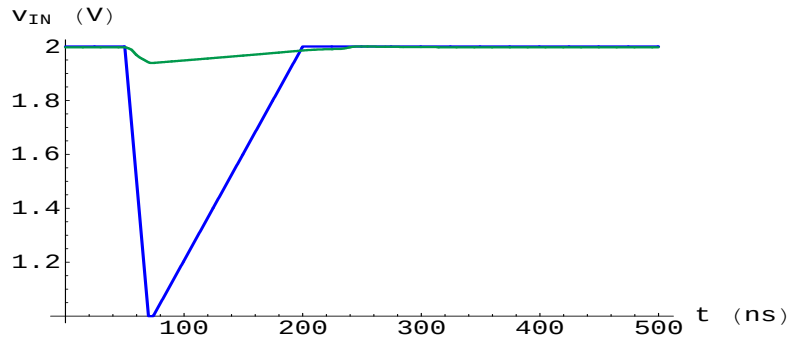


(b)

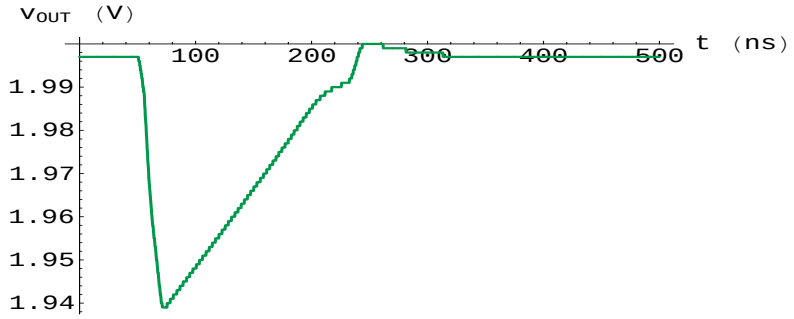


(c)

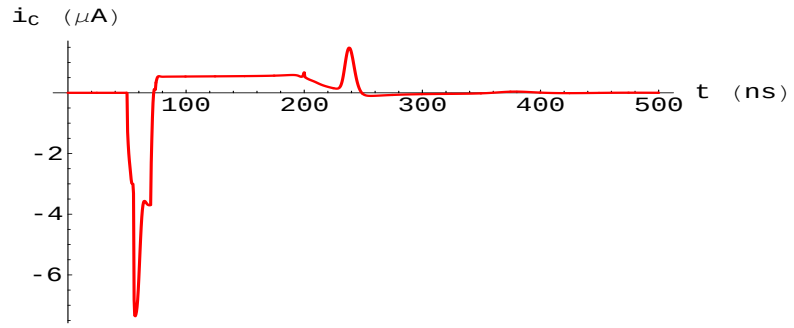
Figure 5.8: (a) Superimposition of some significant node voltages, (b) current flowing into the capacitor C_{L} and (c) magnification of the region near the t axis.



(a)



(b)



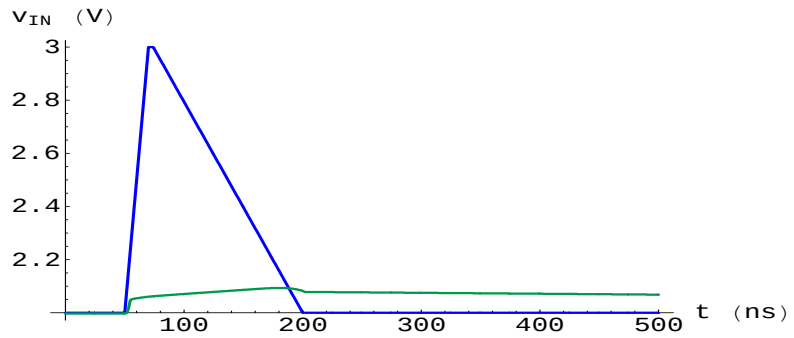
(c)

Figure 5.9: (a) Input (and output) voltage, (b) output voltage and (c) current flowing into the capacitor C_{L}.

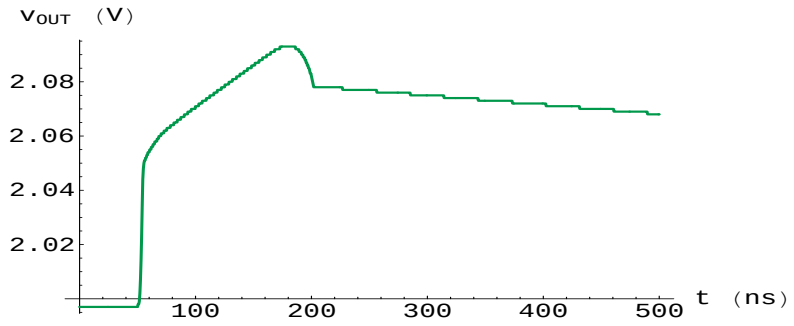
By inspecting Fig. 5.9(b) as well as Fig. 5.9(c), we can observe that in this case the circuit response is completely dominated by the parasitic feedthrough so that we cannot recognise any kind of current limitation, even by examining the capacitor current graph.

Positive Test Signal

The circuit response to the test signal shown in Fig. 5.2(d) is illustrated in Fig. 5.10 whereas Fig. 5.11 shows the current flowing into the capacitor C_{L}.



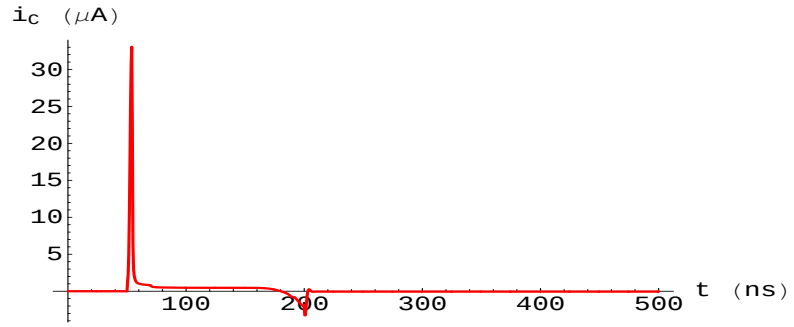
(a)



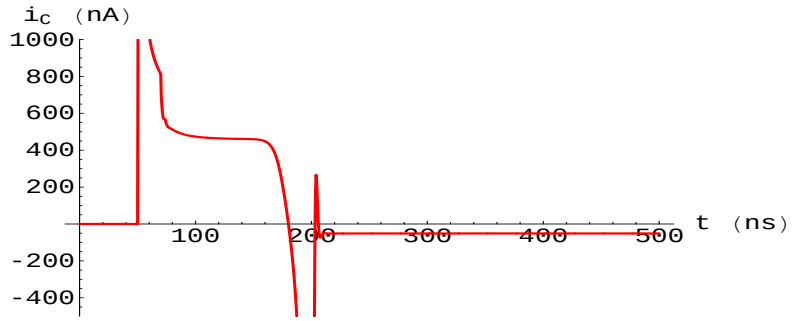
(b)

Figure 5.10: (a) Input (and output) voltage, (b) output voltage.

Unlike the preceding case, by direct inspection of Fig. 5.11(b) we are able to recognise the two constant currents (500 nA and 50 nA) charging and discharging the output capacitor.



(a)



(b)

Figure 5.11: (a) Current flowing into the capacitor C_{L} and (b) magnification of the region near the t axis (Positive narrow test signal).

5.2.3 Circuit Response to a Very Narrow Test Signal

After investigating the circuit response to a narrow test input signal, we will now test the large-signal circuit response in the case when a very narrow input signal is applied.

In fact we wish to know the circuit response to such signals since they are the signals we should obtain at the output of our whole circuit in order to improve its counting rate up to a rate in the order of 10 MHz still satisfying the specifications on the maximum baseline shift.

Negative Test Signal

The circuit response to the test signal shown in Fig. 5.2(e) is illustrated in Fig. 5.12 together with the current flowing into the capacitor C_{L}.

We note that the signal shows a fall time $t_{\mathrm{f}} = 20\,\mathrm{ns}$, a rise time $t_{\mathrm{r}} = 63\,\mathrm{ns}$ and a duration $t_{\mathrm{w}} = 4\,\mathrm{ns}$.

By inspecting Fig. 5.12(b) as well as Fig. 5.12(c), we can observe that also in this case the circuit response is completely dominated by the capacitive feedthrough.

Thus we cannot recognise any kind of current limitation even by examining the capacitor current graph, which was predictable given that the time length of the input signal has been further reduced.

Positive Test Signal

The circuit response to the test signal shown in Fig. 5.2(f) is illustrated in Fig. 5.13 whereas Fig. 5.14 shows the current flowing into the capacitor C_{L}.

By direct inspection of Fig. 5.14(b) we can note that we are still able to recognise the two constant currents (500 nA and 50 nA) limiting the current flowing into the capacitor.

5.2.4 Reducing the Capacitive Feedthrough

The detailed analysis performed in the previous section has pointed out that the main factor increasing the total area of the buffer output signal is the initial output-voltage drop due to the capacitive feedthrough phenomenon.

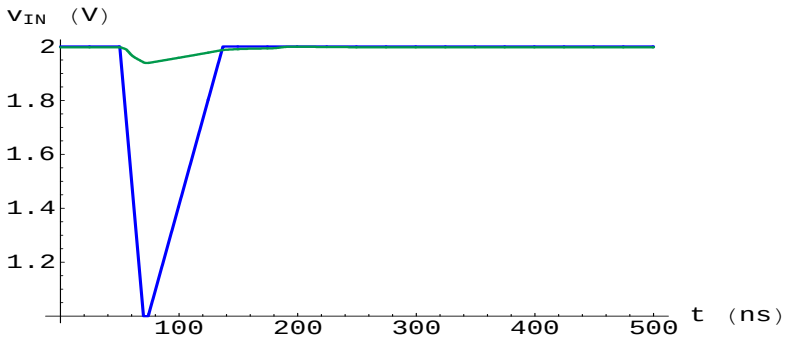
As a result, our principal goal becomes the capacitive-feedthrough reduction.

First, we should verify whether the voltage drop depends on the very angular shape of our test signals.

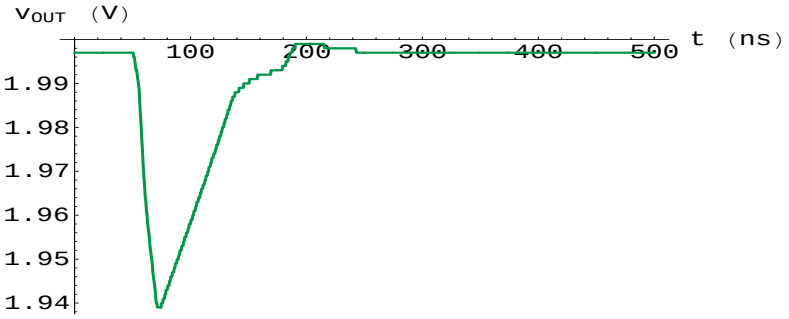
For this purpose we have decided to insert a low-pass filter (an RC-filter with $R = 5\,\mathrm{k}\Omega$ and $C = 1\,\mathrm{pF}$) downstream to the signal generator in order to give the input signal a shape more similar to the actual one.

The graphical results obtained in the case when the very narrow test signal is used are shown in Fig. 5.15.

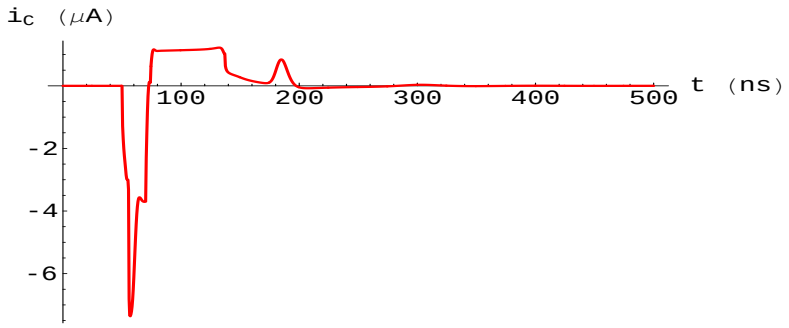
By inspecting the figure we can deduce that the shape of the test signal does not affect the circuit response.



(a)

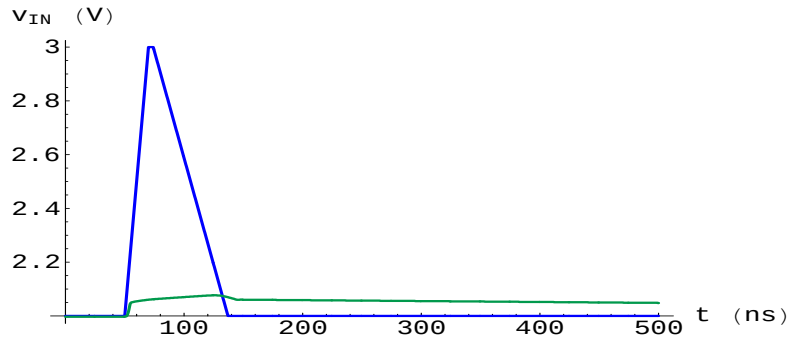


(b)

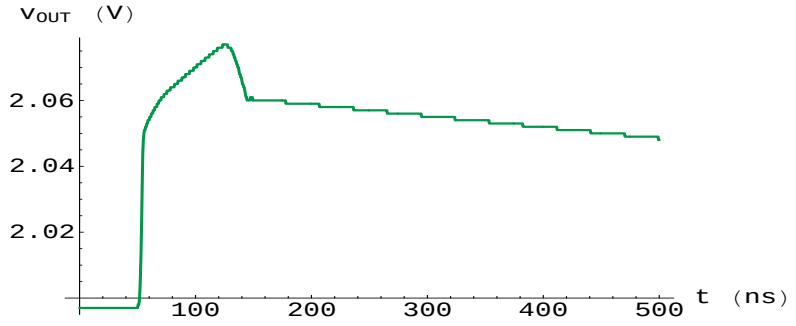


(c)

Figure 5.12: (a) Input (and output) voltage, (b) output voltage and (c) current flowing into the capacitor C_{L}.



(a)



(b)

Figure 5.13: (a) Input (and output) voltage, (b) output voltage.

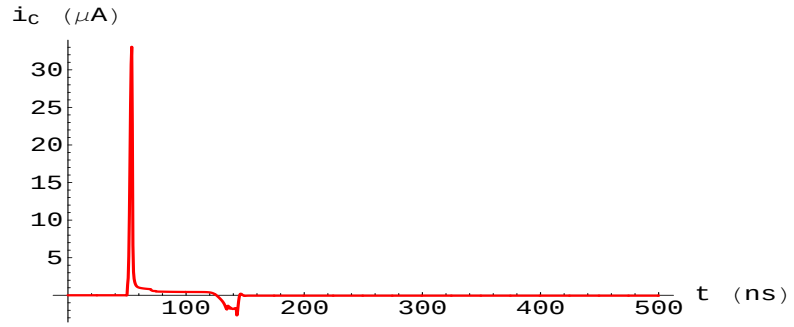
On the other hand, by examining the circuit schematic diagram shown in Fig. 5.1 we can imagine that the parasitic capacitances C_{gs} of the input differential pair play the most dominant role from the feedthrough point of view.

To quantitatively show their contribution we report in Fig. 5.16 the graphical results of a significant test we have performed.

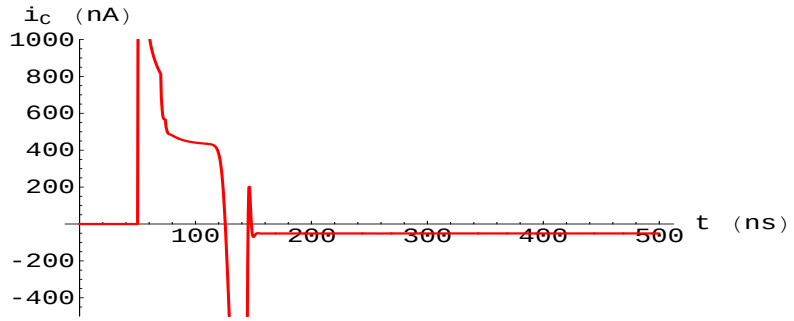
As shown in Fig. 5.17, we have connected two additional capacitors $C_{\text{test}} = 100\,\text{fF}$ in parallel with the respective intrinsic parasitic capacitances C_{gs} of the differential pair in order to check whether a feedthrough increase would occur.

The direct examination of Fig. 5.16 allows us to realise the important role played by the value of such parasitic capacitances.

As a consequence we need to reduce this value and a possible way of achieving



(a)



(b)

Figure 5.14: (a) Current flowing into the capacitor C_{L} and (b) magnification of the region near the t axis (Positive very narrow input signal).

this goal is to resize the transistors of the input pair.

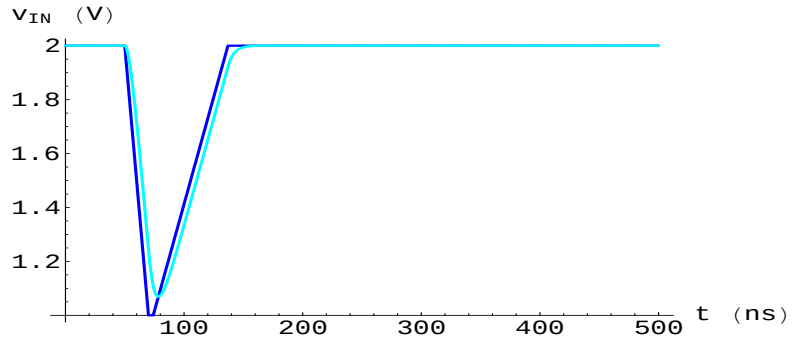
It can be shown that the intrinsic gate-source capacitance of a MOS transistor when it operates in the triode region is

$$C_{\mathrm{gs}} = \frac{C_{\mathrm{ox}} W L}{2}$$

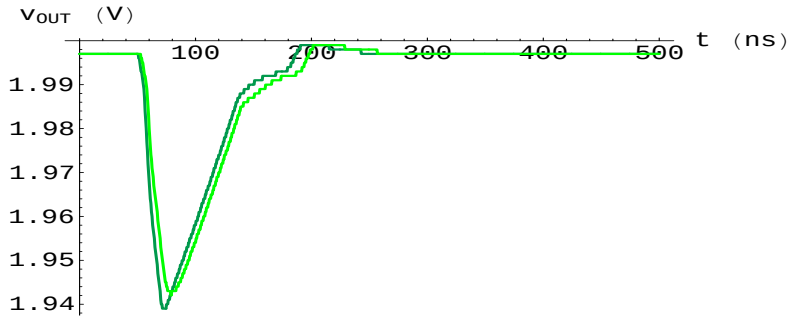
whereas when it operates in the active region is

$$C_{\mathrm{gs}} = \frac{2}{3} W L C_{\mathrm{ox}}$$

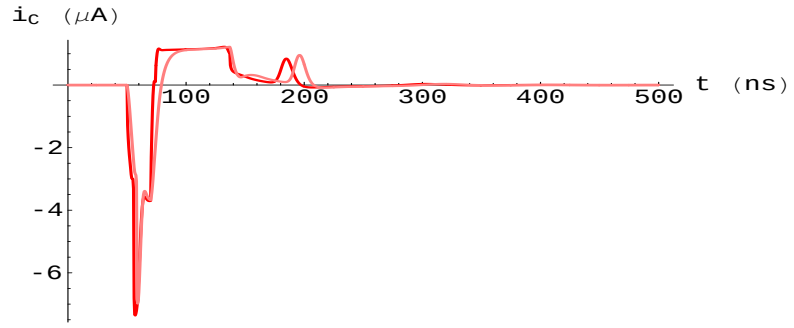
where C_{ox} is the oxide capacitance per unit area from gate to channel whereas W and L are the device width and the channel length respectively.



(a)



(b)

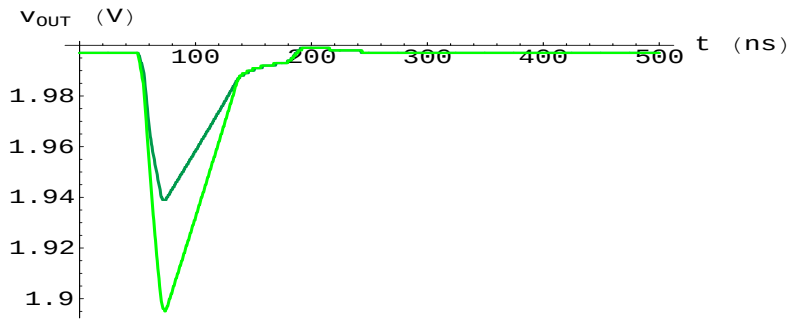


(c)

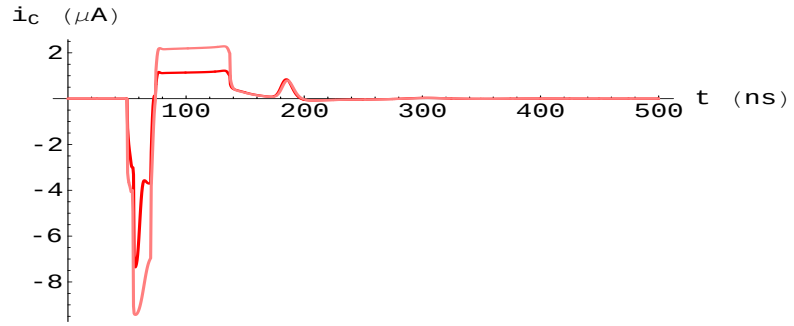
Figure 5.15: (a) Input voltage, (b) output voltage and (c) current flowing into C_{L} compared to their respective signals obtained by filtering the input test signal (light colours).

The above relationships show that the intrinsic gate-source capacitance of a MOS transistor can be reduced by shortening its physical dimensions.

Thus, setting $L = 0.35\,\mu$m (the minimum dimension) and decreasing the bias current of the pair in order to keep the gain quite high, gives fairly good results providing a significant feedthrough limitation.



(a)



(b)

Figure 5.16: (a) Output voltage and (b) current flowing into C_{L} compared to their respective signals obtained by increasing the parasitic capacitances C_{gs} of the differential pair (light colours).

However in practice such a solution would involve relevant drawbacks since it would increase the mismatch between the input pair, leading to a substantial offset.

As a consequence the only way to improve the buffer performance without resizing the input transistors is to modify the basic circuit.

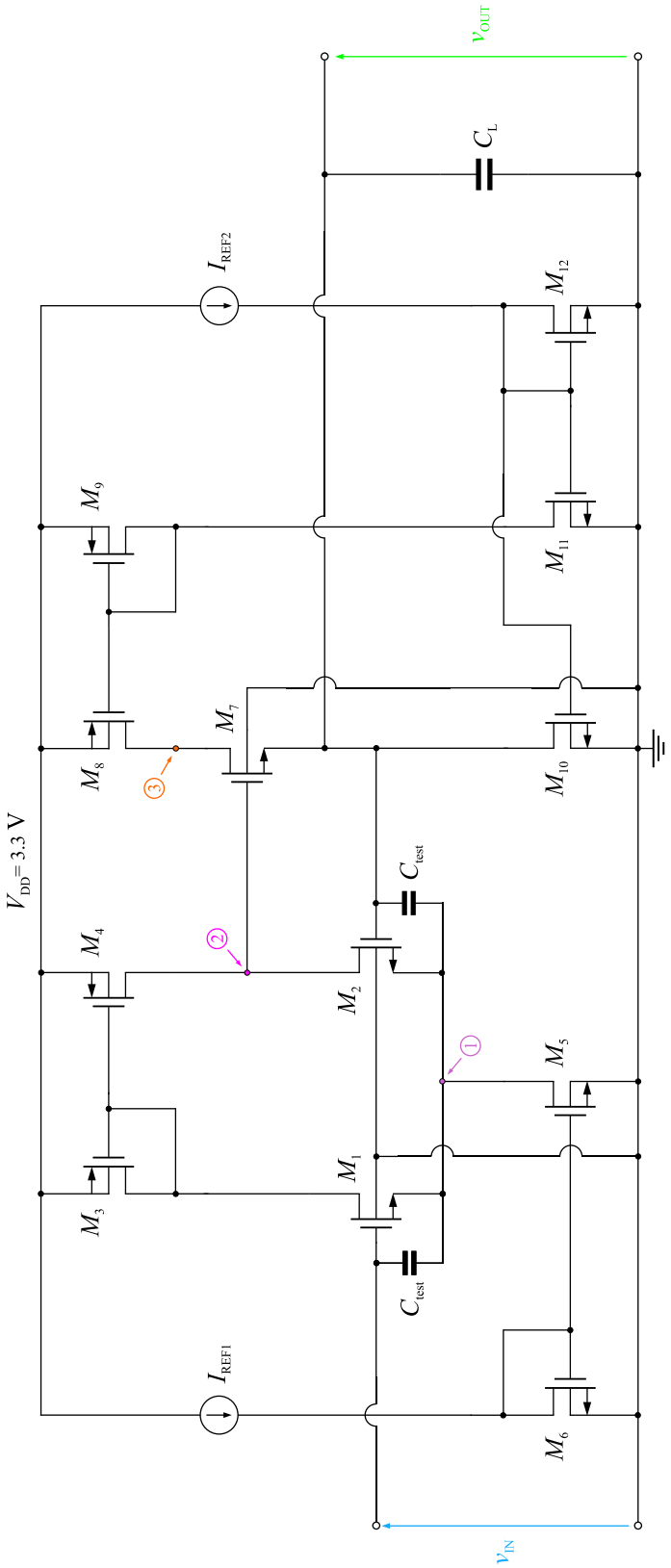


Figure 5.17: Circuit schematic diagram of the non-linear buffer showing the two test capacitors $C_{\text{test}} = 100\,\text{fF}$.

For purposes of illustration we present the alternative circuit shown in Fig. 5.18. By inspecting the figure we can see that to overcome the feedthrough problem the output stage has been moved and a source follower has been added in order to separate the output capacitor from the parasitic capacitance of the input differential pair.

However this new configuration has the disadvantage that the output stage is not included in the feedback loop, and thus this circuit will not be further taken into consideration.

5.3 The Non-Linear Buffer Final Circuit

In this section we will analyse the large-signal behavior of the final circuit implementing the slew-rate limited non-linear buffer.

The schematic diagram of the circuit is shown in Fig. 5.19. By examining the figure we can note that the new circuit is essentially the same as the basic circuit that we have so far described and analysed with the exception of a source follower consisting of a p-channel MOS with a p-channel MOS current-mirror load.

This source follower turns out to be particularly useful to overcome both the problem of the parasitic feedthrough and the problem of the maximum output swing which we mentioned in section 5.2.

In fact as far as the output swing is concerned, we can immediately observe that the dc output voltage of the new circuit can even be set at 3 V since the magnitude of the gate-source voltage of M_{13} is approximately equal to the gate-source voltage of M_7 whereas the sign is opposite so that the source voltage of M_4 is nearly equal to the output voltage.

As a result, in the new circuit the transistor M_4 can still be biased in the active region even if the dc output voltage is set at 3 V.

As mentioned before the source follower is able to reduce the capacitive feedthrough of the input signal avoiding the direct coupling between the output capacitor C_{L} and the intrinsic gate-source capacitances of the input pair.

Moreover the feedthrough of the input signal now passes through the source of M_{13} whose bias current can be freely set because it does not take part in the slew-rate limitation process.

Hence we can increase the bias current of M_{13} in order to reduce its output

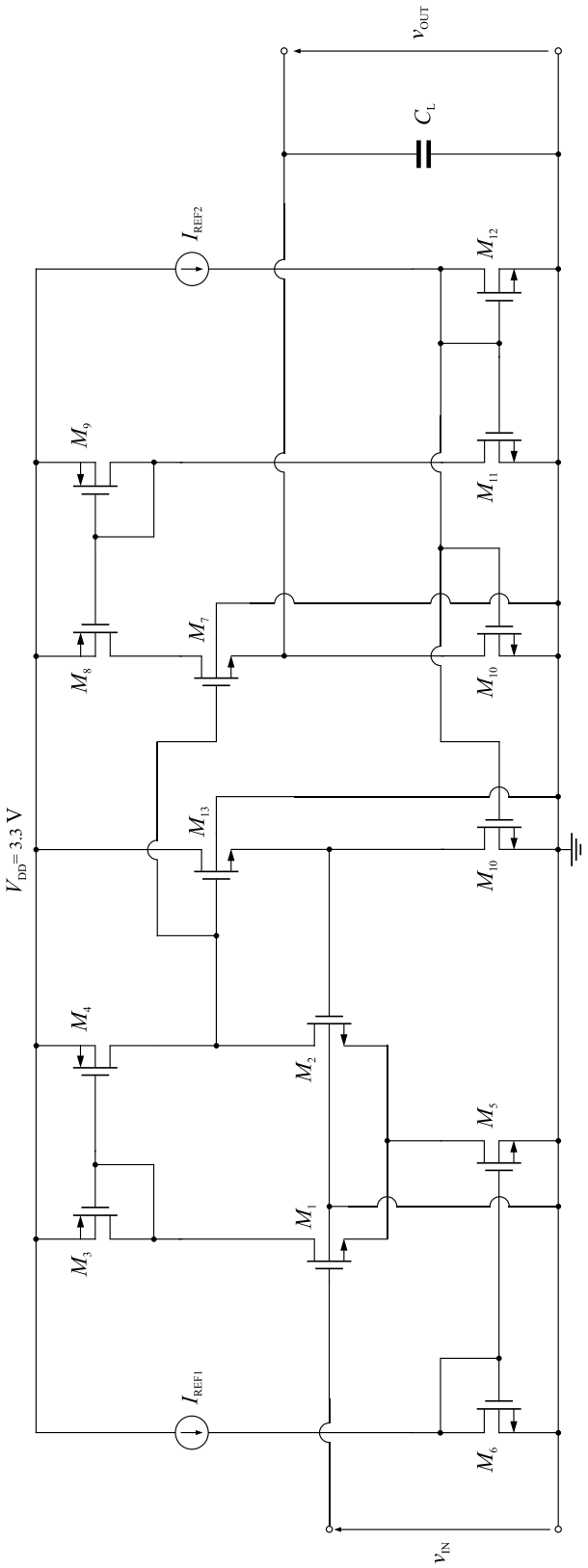


Figure 5.18: Schematic diagram of an alternative circuit implementing the non-linear buffer.

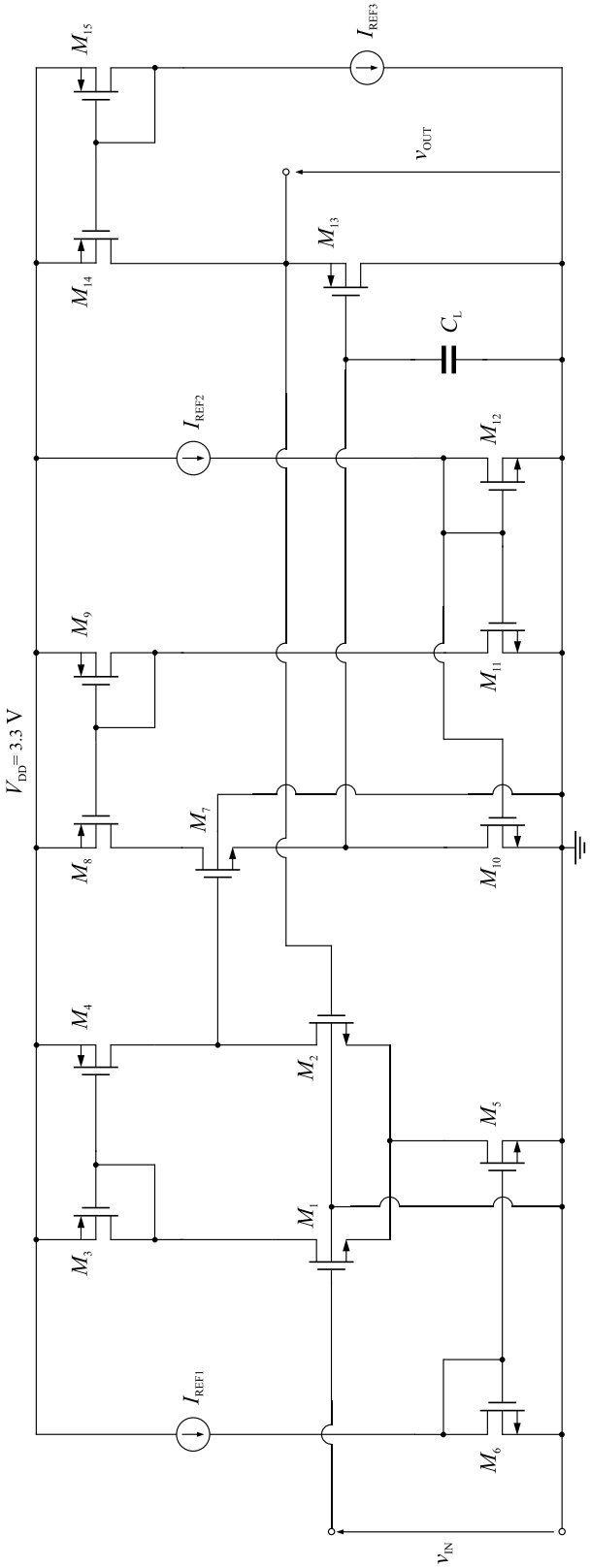


Figure 5.19: Final schematic diagram of the non-linear buffer.

resistance (let us recall that $r_o = 1/g_m$) to provide a low-resistance path connecting the output node and ground.

In order to verify what we have just stated, in the following section we will show the results of the SPICE simulations for the new circuit.

5.4 Large-Signal Behavior of the New Circuit

5.4.1 Circuit Response to a Wide Test Signal

In this section we will analyse the circuit response to the first two test input signals shown in Fig. 5.2, namely the signals displayed in Fig. 5.2(a) and Fig. 5.2(b), in order to compare the large-signal behavior of the new circuit to the one of the basic circuit.

Negative Test Signal

The circuit response to the test signal shown in Fig. 5.2(a) is illustrated in Fig. 5.20 whereas Fig. 5.21 shows the current flowing into the capacitor C_L.

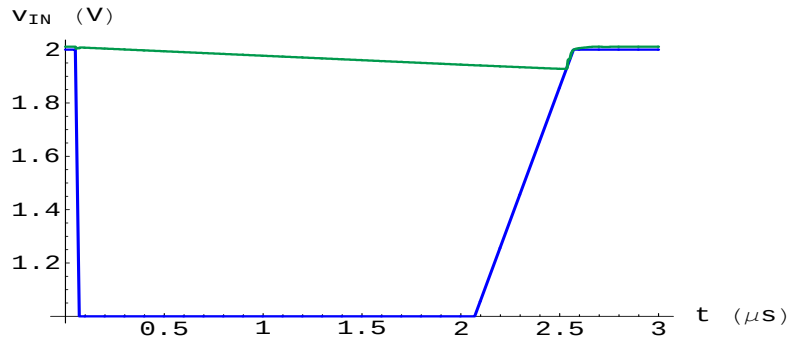
By inspecting the figure we can note that the behavior of the output voltage is now very similar to the ideal behavior predicted by Mathematica simulations and analysed in the previous chapters.

Moreover by comparing the graph of Fig. 5.21(a) showing the current flowing into the capacitor C_L with the analogous graph shown in Fig. 5.5(b) obtained by simulating the basic circuit, we can observe a significant reduction of the current changes due to the parasitic feedthrough.

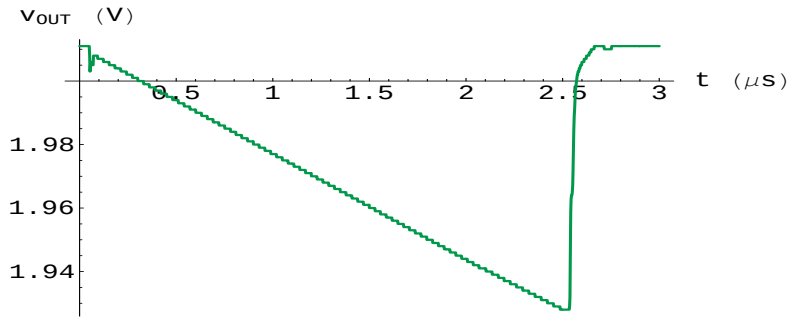
In fact, as mentioned earlier, the transistor M_{13} is mainly concerned now with the parasitic feedthrough.

To highlight the effect of the physical dimensions of M_{13} and its bias current on the feedthrough of the input signal, we have shown in Fig. 5.22(a) the graphical superimposition of the output voltage obtained by halving both the bias current and the transistor width, and the output voltage obtained without performing any change.

By inspecting both Fig. 5.22(a) and Fig. 5.22(b) we can deduce that the parasitic feedthrough has little influence on C_L (whose current is nearly the same in both



(a)



(b)

Figure 5.20: (a) Input (and output) voltage, (b) output voltage.

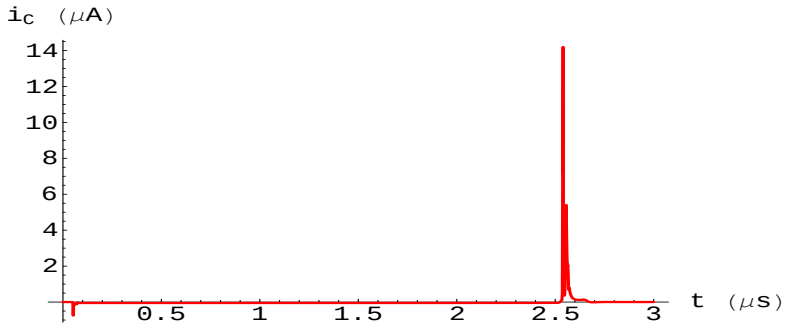
cases) and that the output resistance as well as the intrinsic capacitances of M_{13} really play the role we had supposed in the previous section.

Finally let us note that the strong slew-rate limitation as well as the constant current (50 nA) discharging the capacitor (shown in Fig. 5.20(b) and in Fig. 5.21(b) respectively) are now very evident.

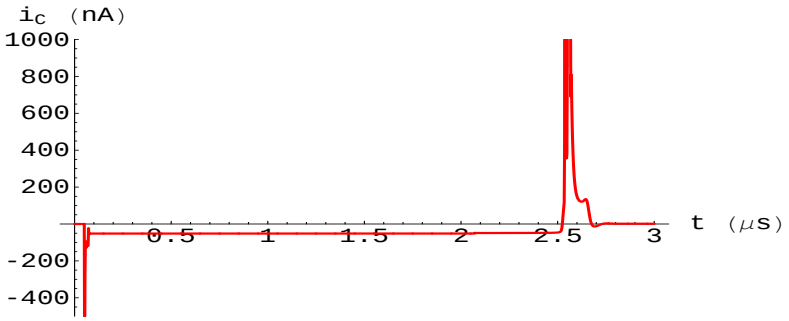
Positive Test Signal

The circuit response to the test signal shown in Fig. 5.2(b) is illustrated in Fig. 5.23 whereas Fig. 5.24 shows the current flowing into the capacitor C_{L}.

By direct inspection of Fig. 5.24(b) we are able to recognise the two constant



(a)



(b)

Figure 5.21: (a) Current flowing into the capacitor C_{L} and (b) magnification of the region near the t axis (Negative wide test signal).

currents (200 nA and 50 nA) charging and discharging the output capacitor.

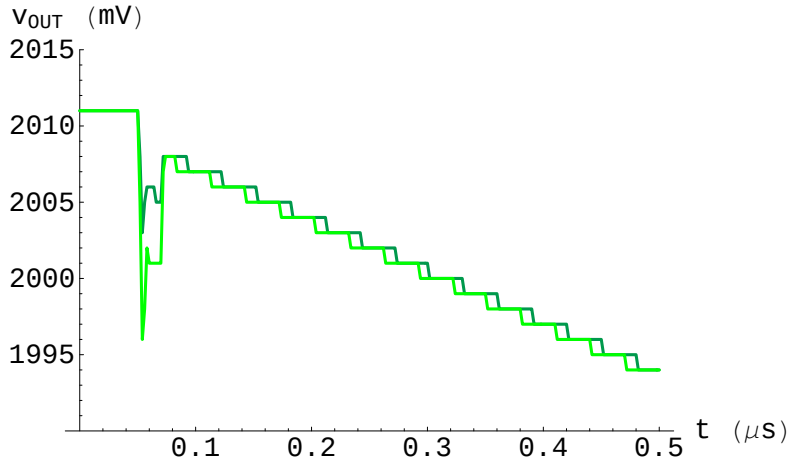
Let us now calculate the slew-rate design values to be compared with those we have measured directly on the curve shown in Fig. 5.23(b).

We have

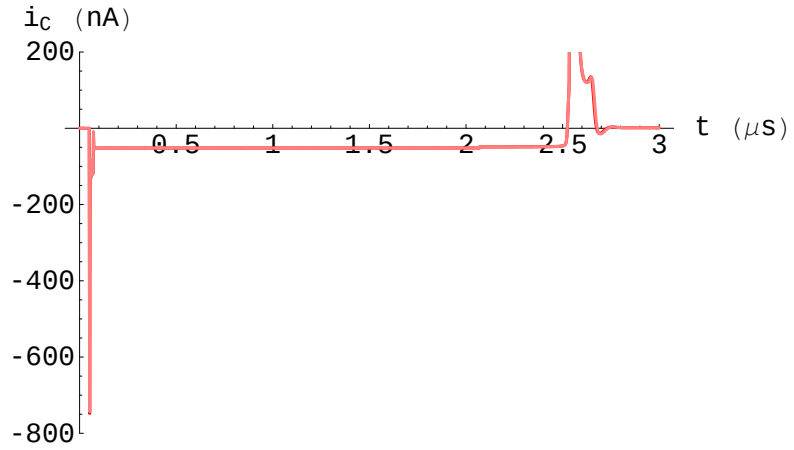
$$\mathrm{SR}_1 = \frac{|I_{\mathrm{disch}}|}{C_{\mathrm{L}}} = \frac{50\,\mathrm{nA}}{1.5\,\mathrm{pF}} \simeq 0.033\,\mathrm{V}/\mu\mathrm{s}$$

and

$$\mathrm{SR}_2 = \frac{I_{\mathrm{ch}}}{C_{\mathrm{L}}} = \frac{200\,\mathrm{nA}}{1.5\,\mathrm{pF}} \simeq 0.1333\,\mathrm{V}/\mu\mathrm{s}$$

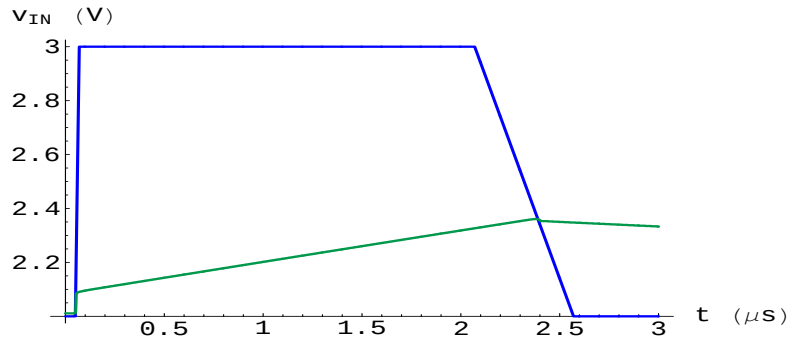


(a)

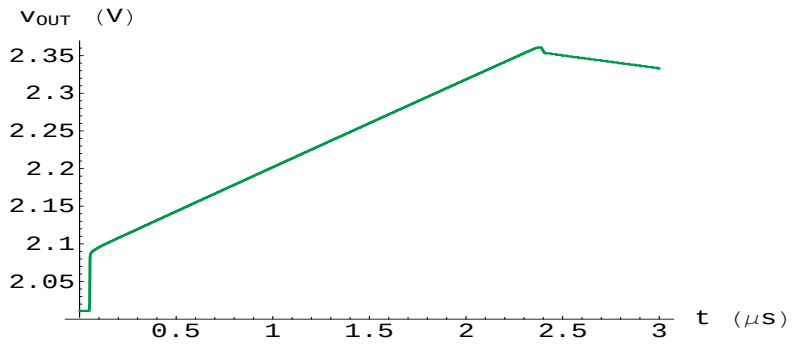


(b)

Figure 5.22: (a) Comparison between the output voltage obtained by changing the physical dimensions and the bias current of M_{13} (*light green*) and the output voltage without changes, (b) comparison between the currents flowing into the capacitor C_{L} in both cases (Let us observe that the graph (a) shows a descending ramp in the shape of steps due to the numerical approximation performed by SPICE on the given data points).



(a)



(b)

Figure 5.23: (a) Input (and output) voltage, (b) output voltage.

whereas the measured values are

$$\mathrm{SR}_1 \simeq 0.034\,\mathrm{V}/\mu\mathrm{s}$$

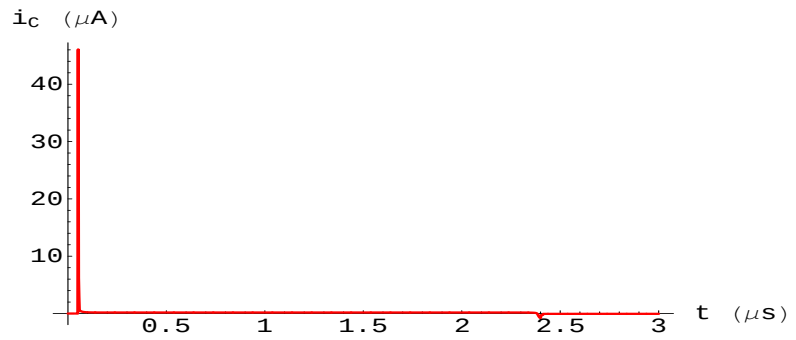
and

$$\mathrm{SR}_2 \simeq 0.121\,\mathrm{V}/\mu\mathrm{s}$$

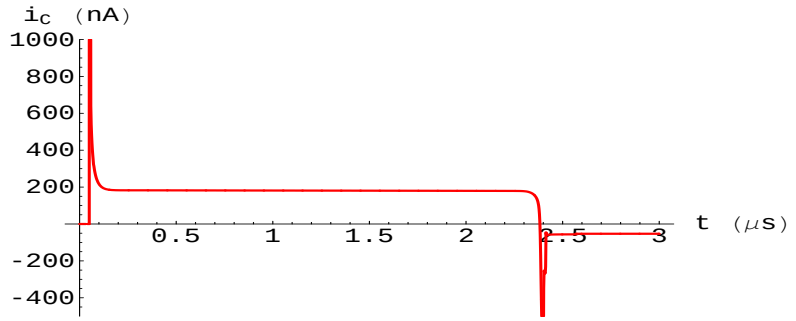
which turn out to be in good agreement with the design values.

5.4.2 Circuit Response to a Narrow Test Signal

In this subsection we are interested in testing the large-signal circuit response in the case when a narrow input signal is applied.



(a)



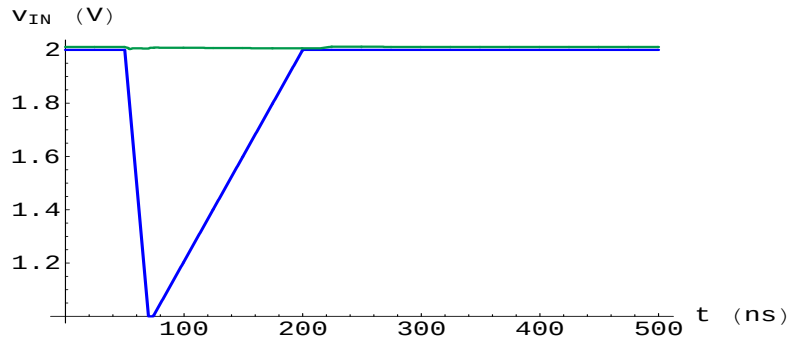
(b)

Figure 5.24: (a) Current flowing into the capacitor C_{L} and (b) magnification of the region near the t axis (Positive wide test signal).

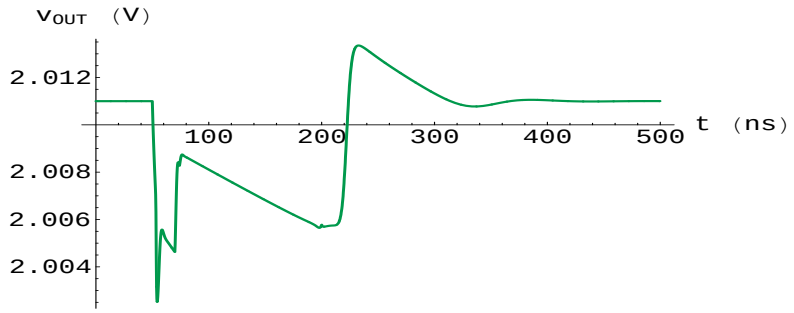
Negative Test Signal

The circuit response to the test signal shown in Fig. 5.2(c) is illustrated in Fig. 5.25 whereas Fig. 5.26 shows the current flowing into the capacitor C_{L}.

By inspecting Fig. 5.25(b) as well as Fig. 5.26(b), we can observe that unlike the analogous case shown in Fig. 5.9 where the circuit response is completely dominated by the parasitic feedthrough, in this case we are still able to recognise the current limitation (50 nA), even if it occurs only for a short time interval.



(a)



(b)

Figure 5.25: (a) Input (and output) voltage, (b) output voltage.

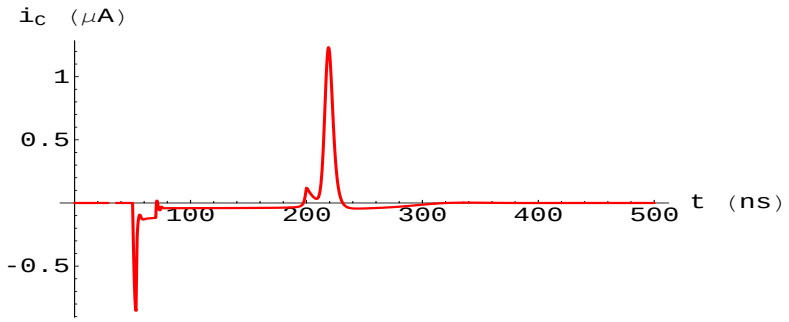
Positive Test Signal

The circuit response to the test signal shown in Fig. 5.2(d) is illustrated in Fig. 5.27 whereas Fig. 5.28 shows the current flowing into the capacitor C_{L}.

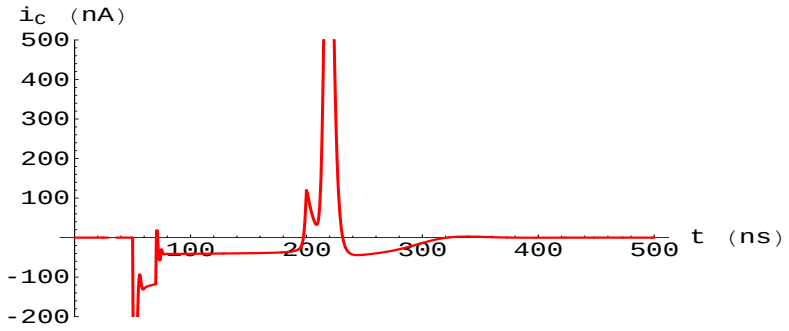
In this case, by direct inspection of Fig. 5.28(b) we are able to recognise both the constant currents (200 nA and 50 nA) charging and discharging the output capacitor.

5.4.3 Circuit Response to a Very Narrow Test Signal

In this subsection we will show the large-signal response of the new circuit to a very narrow input test signal.



(a)



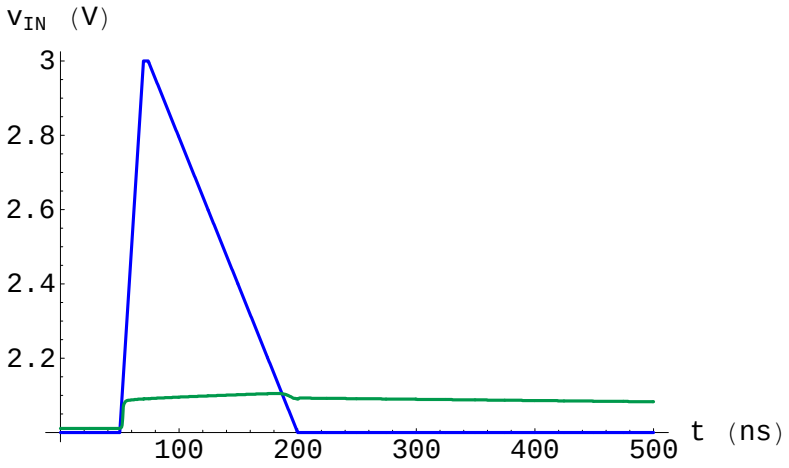
(b)

Figure 5.26: (a) Current flowing into the capacitor C_{L} and (b) magnification of the region near the t axis (Negative narrow test signal).

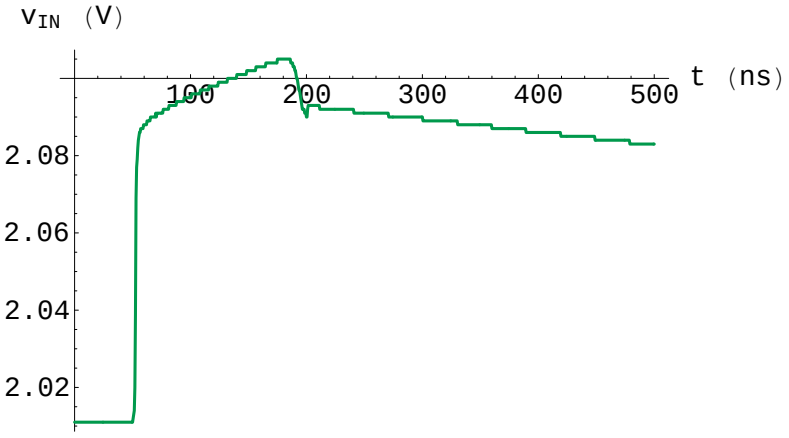
Negative Test Signal

The circuit response to the test signal shown in Fig. 5.2(e) is illustrated in Fig. 5.29 whereas Fig. 5.30 shows the current flowing into the capacitor C_{L}.

By inspecting Fig. 5.29(b) as well as Fig. 5.30(b), we can still appreciate a very short time interval where the current limitation occurs even if the constant-current value we are able to identify ($\sim 30\,\mathrm{nA}$) is not really the nominal one ($50\,\mathrm{nA}$).

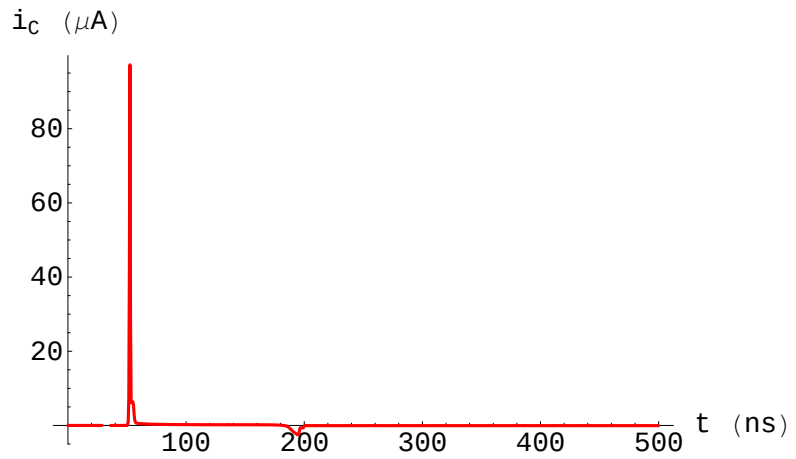


(a)

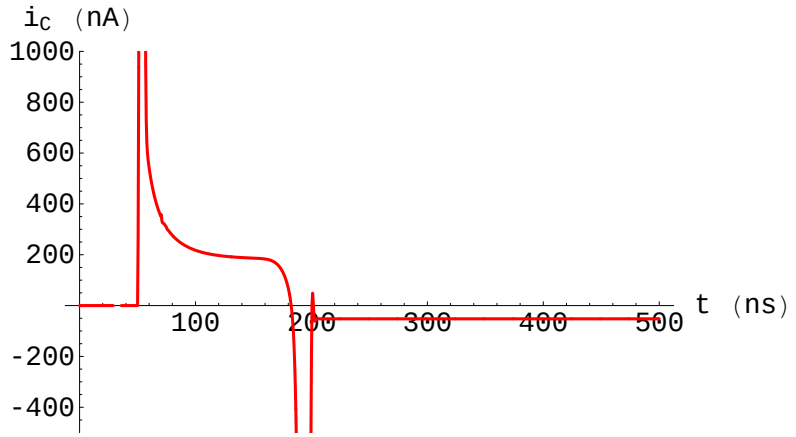


(b)

Figure 5.27: (a) Input (and output) voltage, (b) output voltage.

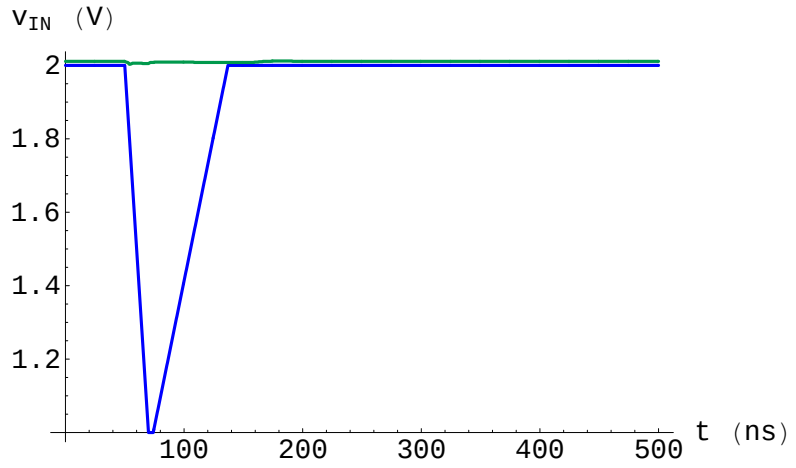


(a)

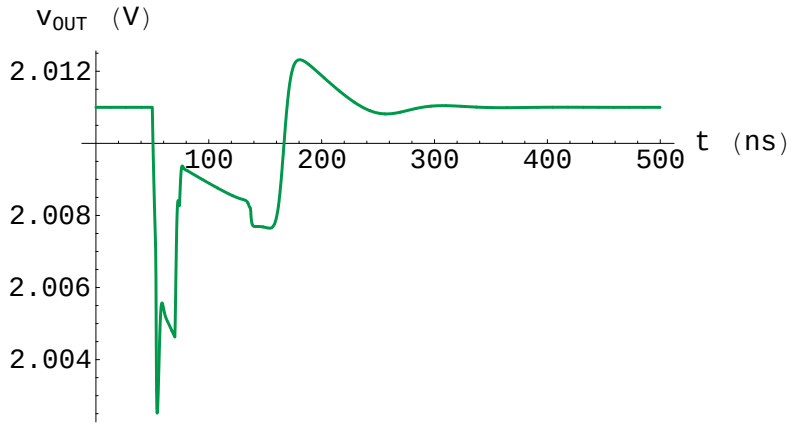


(b)

Figure 5.28: (a) Current flowing into the capacitor C_{L} and (b) magnification of the region near the t axis (Positive narrow test signal).

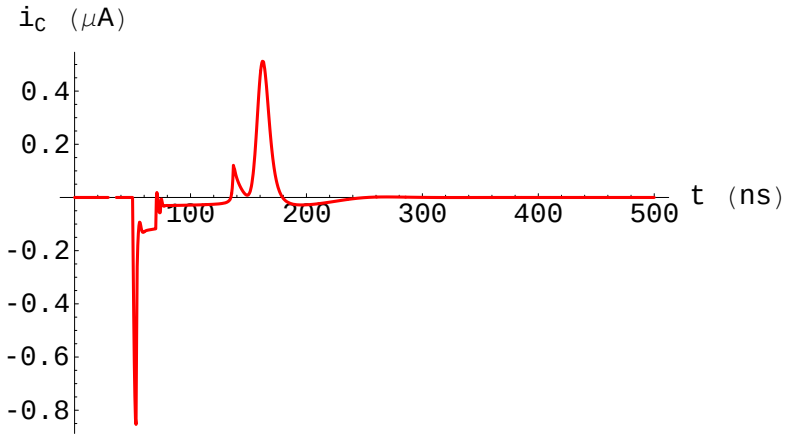


(a)

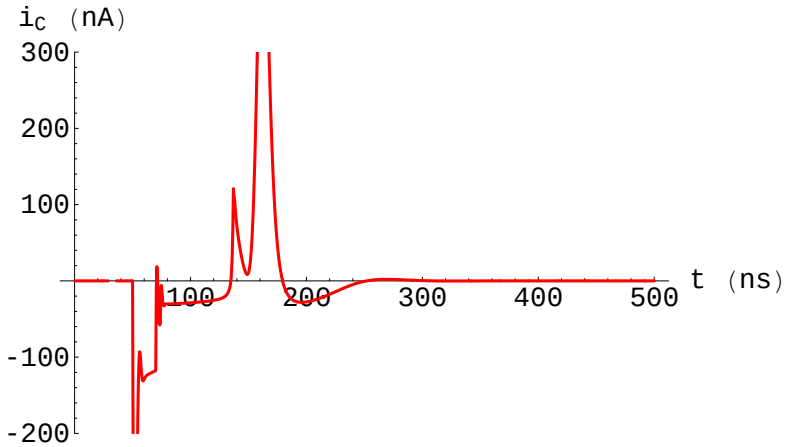


(b)

Figure 5.29: (a) Input (and output) voltage, (b) output voltage.



(a)



(b)

Figure 5.30: (a) Current flowing into the capacitor C_{L} and (b) magnification of the region near the t axis (Negative very narrow test signal).

Positive Test Signal

The circuit response to the test signal shown in Fig. 5.2(d) is illustrated in Fig. 5.31 whereas Fig. 5.32 shows the current flowing into the capacitor C_L.

By the examination of Fig. 5.32(b) we can see that even in the case of a very narrow input test signal both the constant currents (200 nA and 50 nA) charging and discharging the output capacitor are still appreciable.

5.4.4 Frequency Response of the New Circuit

As mentioned at the end of the previous chapter (subsection 4.2.4), the position of the buffer dominant pole (i.e. the buffer bandwidth) can have a significant effect on the shape of the small-signal transfer function of the whole circuit.

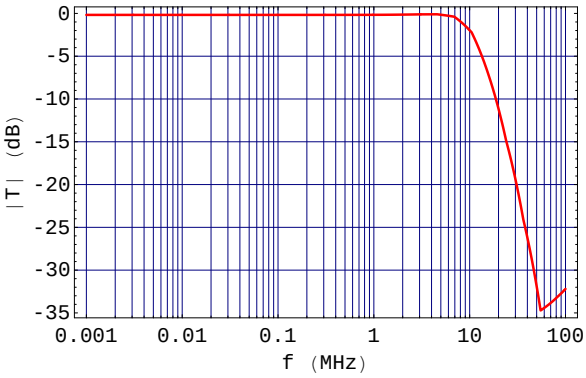
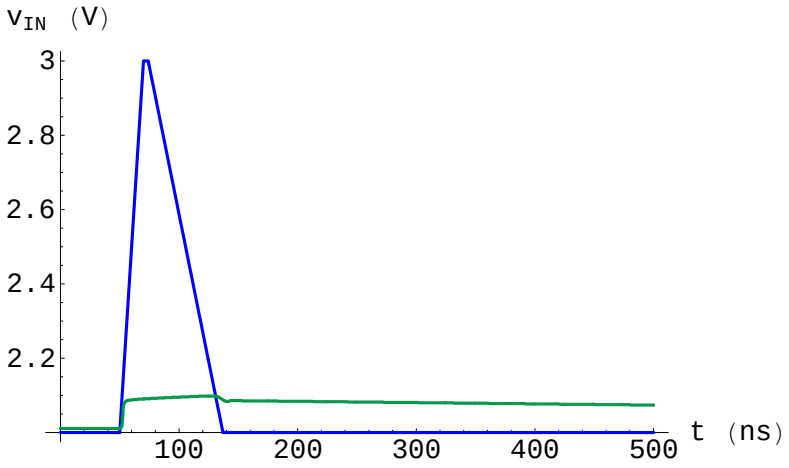


Figure 5.33: Magnitude in dB of the buffer small-signal transfer function.

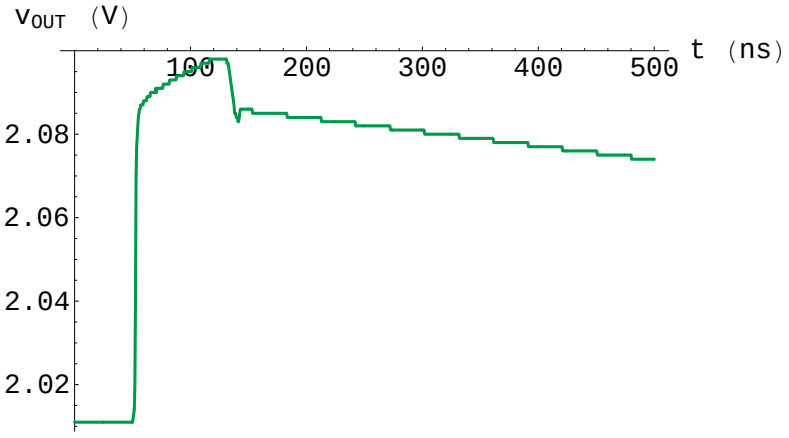
The results obtained there by means of *Mathematica* simulations founded on an analytical model of our circuit, point out that a buffer bandwidth greater than 1 MHz is required to avoid slow oscillations of the circuit baseline.

Thus we report in Fig. 5.33 the magnitude of the buffer small-signal transfer function, to show that the circuit under examination is able to provide a bandwidth unaffecting the small-signal behavior of the total circuit.

By referring to the figure we can observe that the buffer bandwidth is even greater than 10 MHz so that the desired small-signal behavior of the whole circuit is preserved.

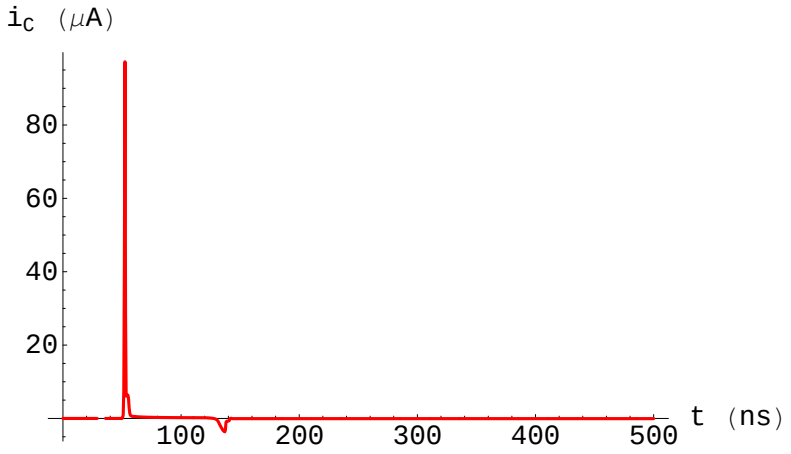


(a)

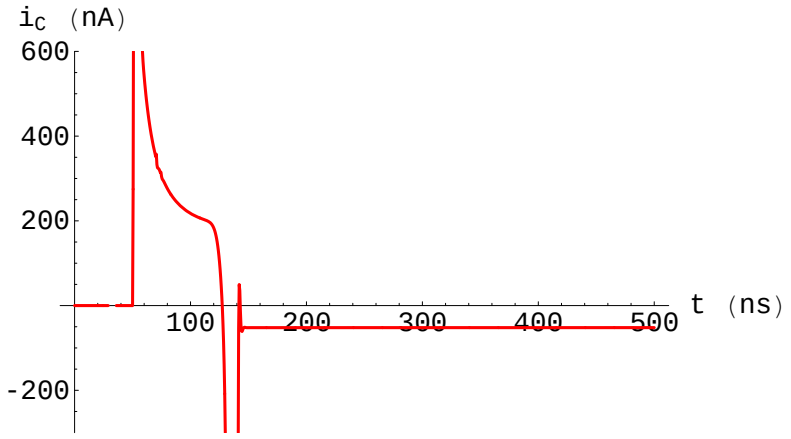


(b)

Figure 5.31: (a) Input (and output) voltage, (b) output voltage.



(a)



(b)

Figure 5.32: (a) Current flowing into the capacitor C_{L} and (b) magnification of the region near the t axis (Positive very narrow test signal).

Chapter 6

Design and Simulation of the Full Front-End Amplifier

This chapter will be mainly concerned with the single-pulse characterisation and the actual-circuit response to various sequences of pulses carrying an increasingly large charge.

In fact our interest is to know whether the circuit really operates linearly and whether the slew-rate limited buffer performs an output baseline stabilisation meeting the given specifications.

Thus, several SPICE-simulation graphical results will be shown and analysed in order to observe the actual-circuit behavior by varying the charge carried by each pulse making up the incoming pulse train.

In particular the presented graphs will allow us to appreciate from a quantitative point of view the baseline shift occurring in each of the considered cases.

Morover such simulations will concern both the total circuit designed to produce output signals in the order of 150 ns (the "slow" circuit) and the circuit conceived to give output signals in the order of 70 ns (the "fast" circuit) and able to provide a higher counting rate.

Let us note that the two circuits are different from one another mainly due to the different values of the components (resistors and capacitors) involved in the feedback network of the preamplifier and the pulse shaper.

On the other hand both circuits are provided with the same BLH including the slew-rate limited buffer described in the previous chapter.

6.1 Behavior of the Slow Circuit

Before performing the characterisation of the voltage output signal produced by the circuit under consideration, we will show the response of this circuit to a sequence of charges $Q_{\text{in}} = 2\,\text{pC}$ injected at rate $r = 5\,\text{MHz}$.

This response has been obtained after excluding the BLH from the circuit in order to point out the output baseline shift we would observe without a proper baseline stabilisation.

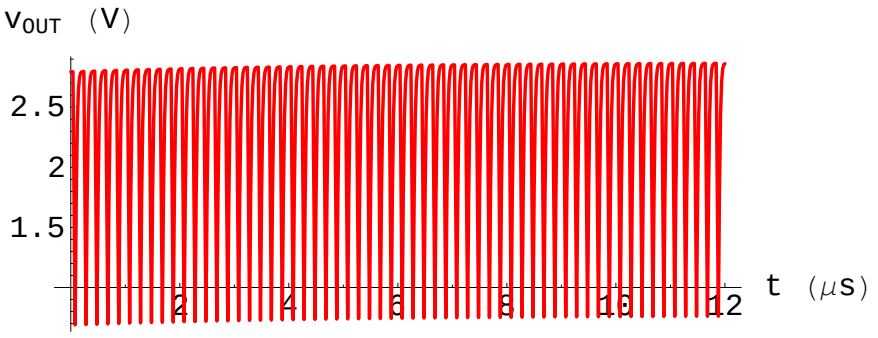


Figure 6.1: Slow-circuit response (no BLH) to a train of pulses carrying a charge $Q_{\text{in}} = 2\,\text{pC}$.

Figure 6.1 shows the circuit response to the first sixty incoming pulses.

By inspecting the figure a certain output-voltage drift can be observed even if this graph does not allow us to appreciate the size of the drift due to the fact that the output signals are very large ($\sim 2.3\,\text{V}$) compared to the expected baseline shift.

On the other hand Fig. 6.2 shows a magnification of the graph region near the circuit dc output voltage ($\sim 2.8\,\text{V}$) and also displays the circuit response over a larger time interval.

Thus we are now able to estimate the baseline shift, which is approximately equal to 80 mV, a value much larger than the one dictated by the specifications ($1\,\text{mV} \div 3\,\text{mV}$).

It should be pointed out that the 80-mV baseline shift occurring when the BLH is disabled turns out to be fairly different to the value of about 500 mV predictable on the basis of the *Mathematica* simulations reported at the end of Chap. 3 and showing a baseline shift to peaking voltage ratio in the order of 22.5%, for the slow circuit at rate $r = 5\,\text{MHz}$.

The reason of this disagreement is that the transconductor block itself is slew-rate limited for large and fast output signals and this problem was not taken into account in those *Mathematica* simulations.

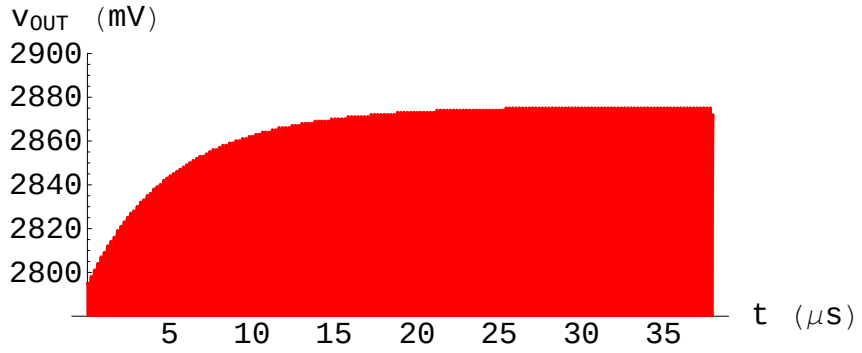


Figure 6.2: Magnification of the output-voltage region near the dc output voltage, showing the voltage drift.

6.1.1 Characterisation of the Single Output Pulse

As mentioned earlier we are interested in testing the circuit linearity, namely to verify whether the circuit operates in such a way that the output pulse peaking voltage V_{p} can be considered directly proportional to the charge Q_{in} carried by the single incoming pulse.

In addition, it could also be interesting to check whether the output pulse peaking time t_{p} remains approximately constant by varying the incoming charge.

Thus some SPICE simulations have been performed in order to answer the two preceding questions and the numerical results obtained in both cases by increasing the incoming charge are shown in Tab. 6.1 and in Tab. 6.2 respectively.

Moreover, to obtain a direct understanding of the correlation between V_{p} and Q_{in} as well as t_{p} and Q_{in}, the respective data acquired with the simulations have been represented in a graphical form and shown in Fig. 6.3(a) and in Fig. 6.3(b).

In both cases a fit to the data points has been obtained by using *Mathematica* and a plot of the performed fits is given in Fig. 6.4 which also displays each fit superimposed on the respective original data.

By referring to the fit shown in Fig. 6.4(a) we can directly appreciate the goodness of the linear fit in the case under examination.

$\mathbf{Q}_{\mathrm{in}}$ (fC)	$\mathbf{V}_{\mathrm{p}}$ (mV)
4	4.5715
100	118.59
200	237.62
500	592.56
1000	1185.4
1500	1770.1
2000	2292.3
2500	2702.7

Table 6.1: Peaking voltage data points.

$\mathbf{Q}_{\mathrm{in}}$ (fC)	$\mathbf{t}_{\mathrm{p}}$ (ns)
4	18.96
100	18.98
200	18.99
500	19.19
1000	19.60
1500	19.62
2000	21.49
2500	25.74

Table 6.2: Peaking time data points.

However Pearson's correlation coefficient can be calculated in order to obtain a quantitative measure of the linear correlation between V_{p} and Q_{in}.

A coefficient value close to zero indicates there is little linear correlation between the variables but it does not exclude a significant nonlinear correlation.

By considering two generic variables x and y, the above coefficient is given by

$$r = \frac{\sum_{i=1}^{n} (x_i - \bar{x})\ (y_i - \bar{y})}{\sqrt{\sum_{i=1}^{n} (x_i - \bar{x})^2} \sqrt{\sum_{i=1}^{n} (y_i - \bar{y})^2}}$$

where n is the sample size, $\bar{x}$ and $\bar{y}$ are the average values of the data related to the respective samples.

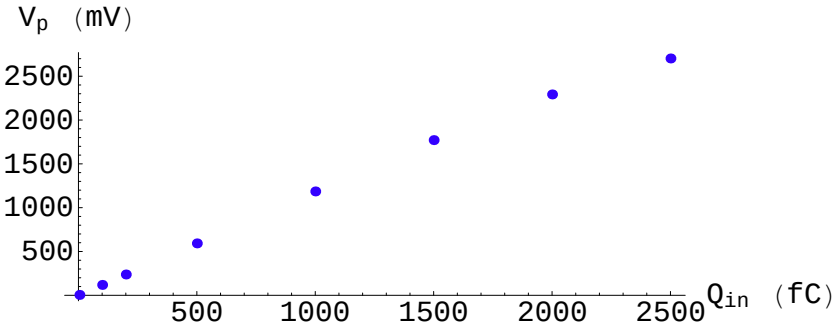
Carrying out the calculation for the data points of Tab. 6.1 gives

$$r_1 = 0.9986$$

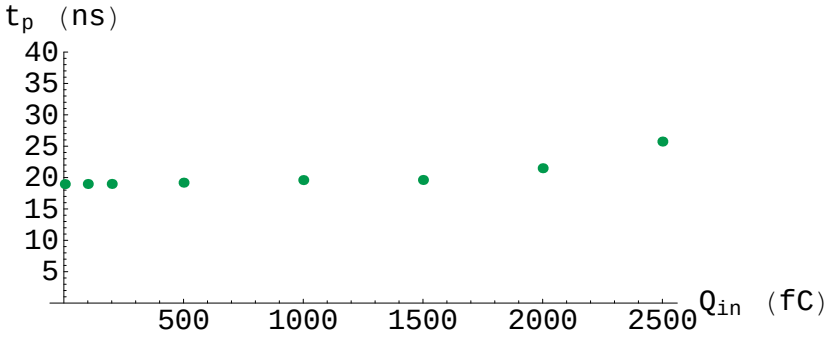
which is a value very close to unity and indicates an almost perfect linear correlation between the variables.

Although the correlation coefficient value obtained before approaches unity, a unilateral hypothesis test should be performed to check whether the hypothesis that the population from which the sample comes has a zero correlation coefficient ρ (i.e. $H_0 : \rho = 0$) must be rejected at a given significance level α, accepting thus the hypothesis that it has a positive linear correlation (i.e. $H_1 : \rho > 0$).

Since it can be shown that the correlation coefficient can be used to construct a



(a)



(b)

Figure 6.3: (a) Peaking voltage and (b) peaking time versus incoming charge.

t statistic with $n-2$ degrees of freedom (where n is the sample size) of the form

$$t^{(n-2)} = \sqrt{n-2}\,\frac{r}{\sqrt{1-r^2}},$$

we should thus verify wheter

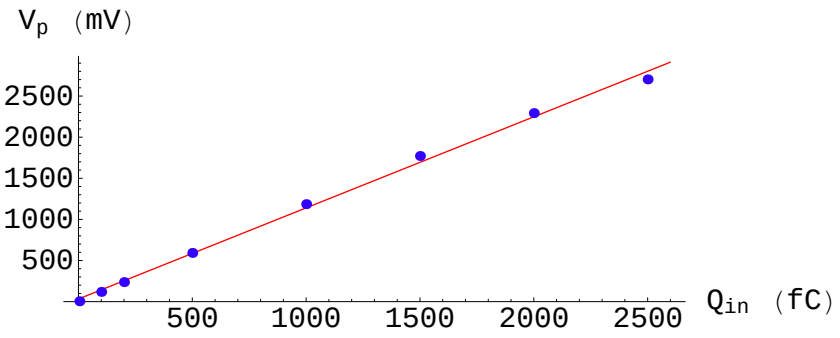
$$t^{(n-2)} > t_{\alpha}^{(n-2)}$$

at a given α level.

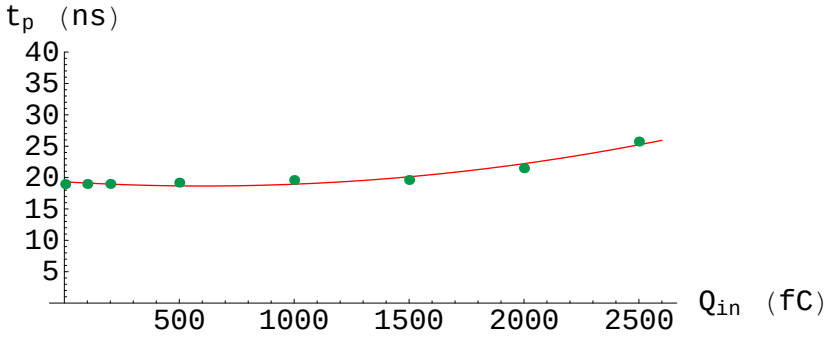
If a level $\alpha = 0.01$ is chosen, we must verify

$$t^{(6)} > t_{0.01}^{(6)} = 3.143$$

in the case under consideration.



(a)



(b)

Figure 6.4: (a) Linear fit to the data points of Tab. 6.1 and (b) quadratic fit to the data points of Tab. 6.2, superimposed on the respective original data.

Since $t^{(6)} = 45.800$ is obtained from the sample data, we can deduce that there is very significant positive linear correlation between V_p and Q_in, at a level even much greater than the given $\alpha = 1\%$.

Finally we report the linear fit equation obtained in the considered case, namely

$$V_\mathrm{p} = 32.719 + 1.1075\, Q_\mathrm{in}$$

by considering V_p and Q_in as expressed in millivolts and femtocoulombs respectively.

Let us note that the value 1.1075 mV/fC (the slope of the linear fit) can also represent a fairly good estimate of the linear gain of our circuit.

By referring now to the fit shown in Fig. 6.4(b), we can directly appreciate the goodness of the quadratic fit in the case under examination.

The quadratic fit equation obtained on the basis of the sample data is

$$t_{\mathrm{p}} = 19.324 - 0.0221\, Q_{\mathrm{in}} + 1.827 \times 10^{-6}\, Q_{\mathrm{in}}^2$$

by considering t_{p} and Q_{in} as expressed in nanoseconds and femtocoulombs respectively.

Finally let us note that the value $\bar{t_{\mathrm{p}}} = 20.32\,\mathrm{ns}$ we can calculate from the data points can represent a good estimate of the average peaking time.

6.1.2 The Shape of the Single Output Pulse

After investigating the circuit linearity, it can be interesting to analyse the shape of the full circuit output signal as well as the buffer output signal in the case when a small charge $Q_{\mathrm{in}} = 4\,\mathrm{fC}$ and a larger charge $Q_{\mathrm{in}} = 2\,\mathrm{pC}$ are injected into the circuit.

By inspecting Fig. 6.5(a) and Fig. 6.6(a) we can see that a circuit output signal of about 4.6 mV is obtained in the case $Q_{\mathrm{in}} = 4\,\mathrm{fC}$ whereas an output signal of about 2.3 V is obtained in the case $Q_{\mathrm{in}} = 2\,\mathrm{pC}$.

In addition we can observe that the shape of the two signals is conserved.

On the other hand, comparing Fig. 6.5(b) to Fig. 6.6(b) shows that the shape of the buffer output voltage is very different in the two cases since the dynamic clipping performed by the buffer only occurs for fast and large signals.

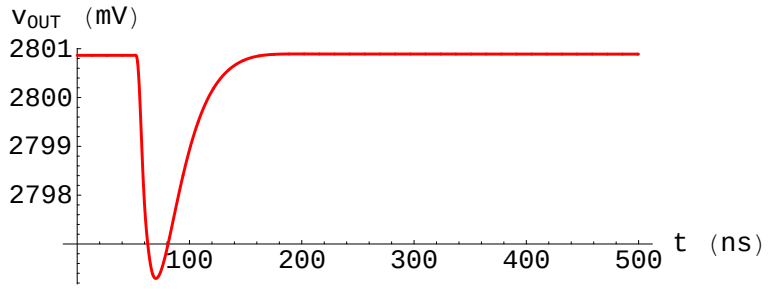
Finally let us note that the buffer dc output voltage level ($\sim 2.795\,\mathrm{V}$) is slightly less than the one of the whole circuit ($\sim 2.801\,\mathrm{V}$).

This slight difference stems from the fact that the transconductor block which kept the circuit dc output voltage about equal to its reference voltage (2.8 V in this case) is now connected to the buffer output and the low-frequency open-circuit voltage gain A_{v0} of the basic differential amplifier used in the unity-gain feedback configuration is finite.

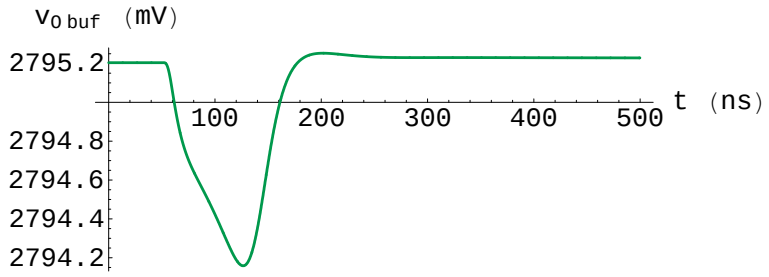
In fact the corresponding buffer voltage gain is less than unity, since

$$A_{\mathrm{v0}}^{\mathrm{buf}} = \frac{A_{\mathrm{v0}}}{1 + A_{\mathrm{v0}}}$$

Hence a circuit optimisation has been performed (by increasing the basic differential amplifier voltage gain) to obtain a value very near to the transconductor block reference voltage.



(a)



(b)

Figure 6.5: Pulse shape of (a) the full-circuit output voltage signal and (b) the buffer output voltage signal, for an incoming charge $Q_{\text{in}} = 4\,\text{fC}$.

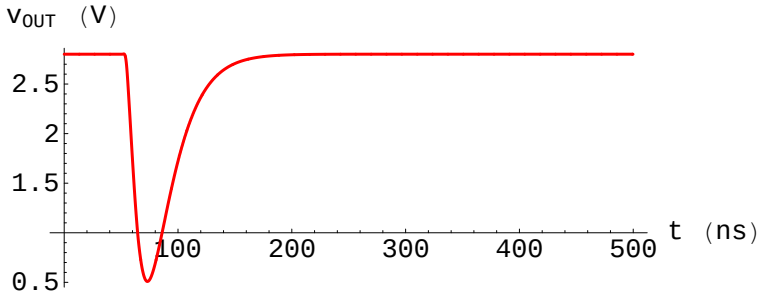
6.1.3 The Circuit Response to a Pulse Train

In order to quantitatively show the baseline stabilisation performed by the BLH block, we will present the actual-circuit response to three sequences of pulses injected at the same rate $r = 5\,\text{MHz}$ but carrying a different charge in each of the three simulations.

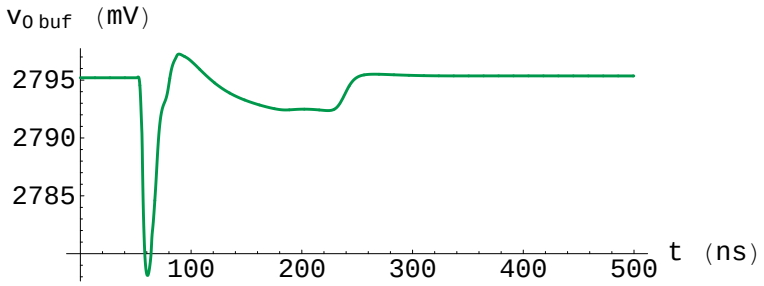
By inspecting Fig. 6.7(b) we can note that a baseline shift approximately equal to $375\,\mu\text{V}$ occurs in the case when the charge carried by each incoming pulse is $Q_{\text{in}} = 4\,\text{fC}$.

By examining Fig. 6.8(b) we can observe a baseline shift approximately equal to $1.8\,\text{mV}$ when the charge carried by each pulse is $Q_{\text{in}} = 1\,\text{pC}$.

Finally by direct inspection of Fig. 6.9(b) a baseline shift approximately equal to $2\,\text{mV}$ can be appreciated when each incoming pulse carries a charge $Q_{\text{in}} = 2\,\text{pC}$.



(a)



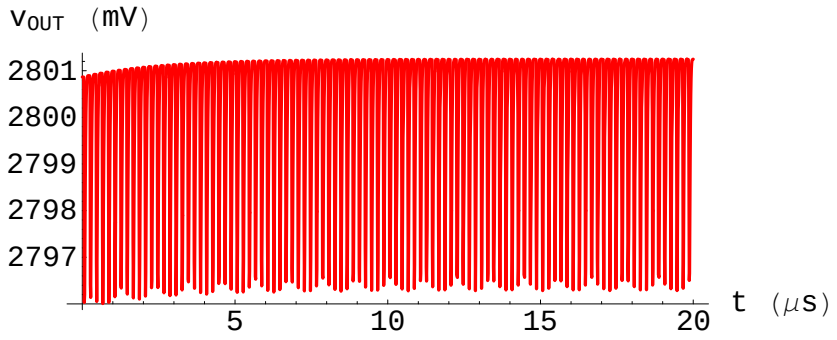
(b)

Figure 6.6: Pulse shape of (a) the full-circuit output voltage signal and (b) the buffer output voltage signal, for an incoming charge $Q_{\text{in}} = 2\,\text{pC}$.

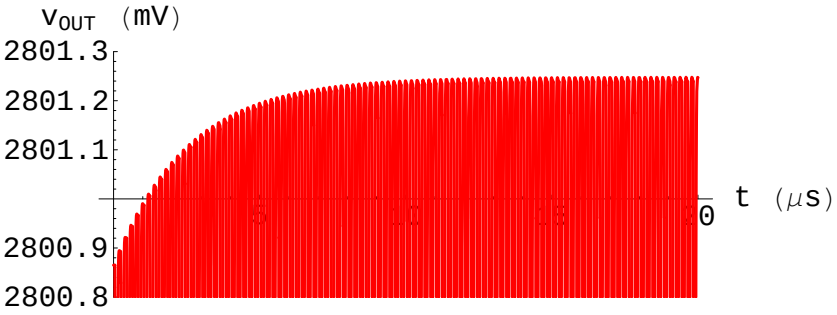
Carrying out the calculation of the maximum baseline shift to the peaking voltage ratio for the three preceding cases, gives the following values per cent

- ▷ 8.2% when $Q_{\text{in}} = 4\,\text{fC}$
- ▷ 0.15% when $Q_{\text{in}} = 1\,\text{pC}$
- ▷ 0.09% when $Q_{\text{in}} = 2\,\text{pC}$

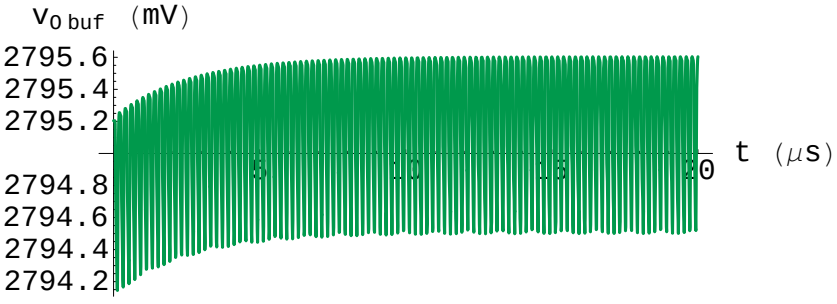
which indicate that the buffer performs a non-linear dynamic clipping which becomes increasingly evident as the charge of the incoming pulses is increased.



(a)

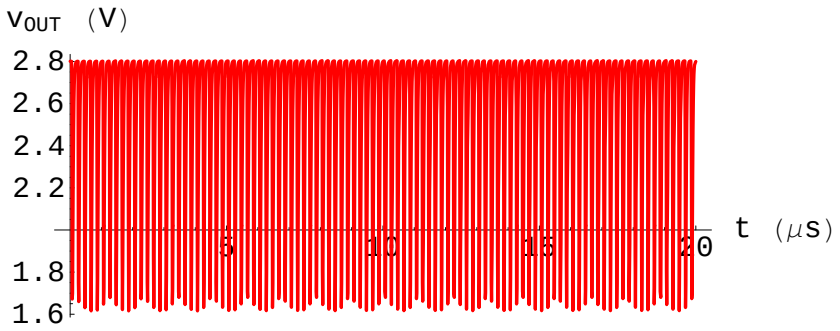


(b)

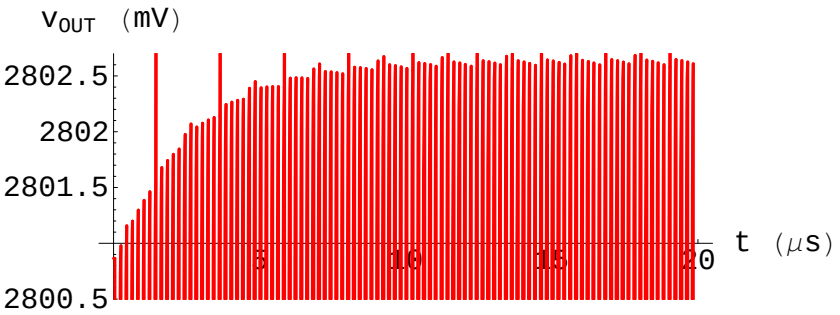


(c)

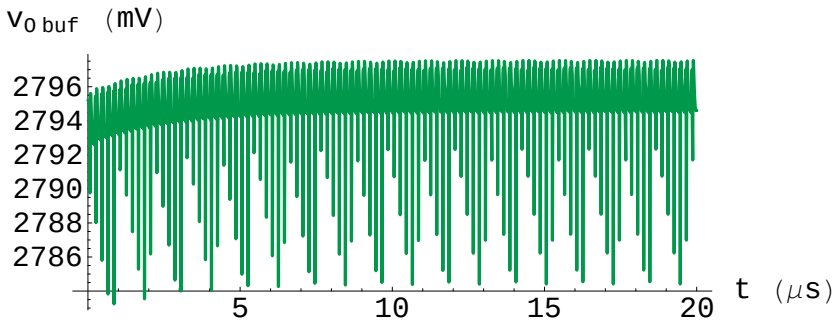
Figure 6.7: (a) Slow-circuit response to a sequence of charges $Q_{\text{in}} = 4\,\text{fC}$ injected at rate $r = 5\,\text{MHz}$, (b) magnification of the region where the baseline shift occurs and (c) buffer output voltage.



(a)

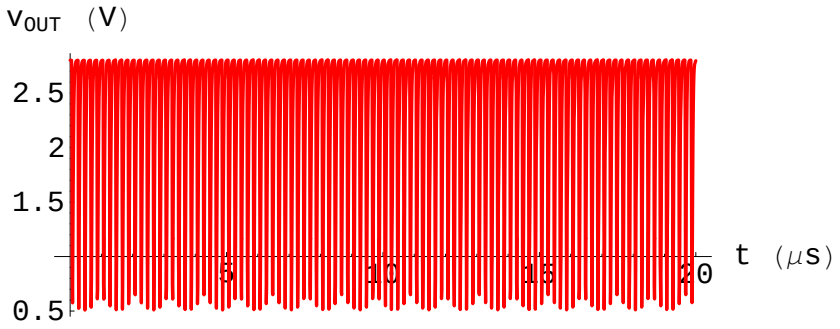


(b)

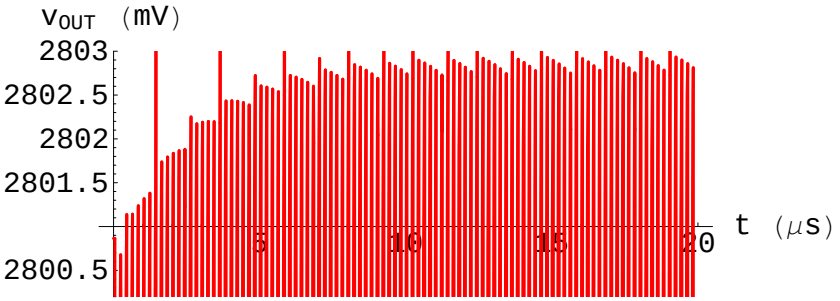


(c)

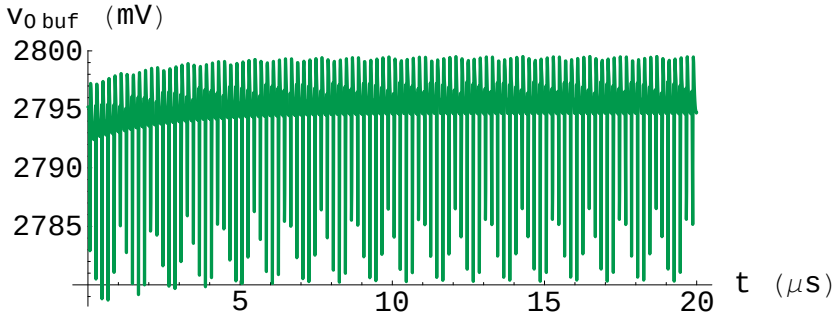
Figure 6.8: (a) Slow-circuit response to a sequence of charges $Q_{\text{in}} = 1\,\text{pC}$ injected at rate $r = 5\,\text{MHz}$, (b) magnification of the region where the baseline shift occurs and (c) buffer output voltage.



(a)



(b)



(c)

Figure 6.9: (a) Slow-circuit response to a sequence of charges $Q_{\text{in}} = 2\,\text{pC}$ injected at rate $r = 5\,\text{MHz}$, (b) magnification of the region where the baseline shift occurs and (c) buffer output voltage.

6.2 Behavior of the Fast Circuit

In this section the fast circuit will be taken into consideration and its response to a single incoming charge as well as a sequence of different charges injected at rate $r = 10\,\text{MHz}$ will be shown and briefly analysed.

The performed SPICE simulations will also allow the comparison between the results achieved in the case under examination and those obtained in the previous section when the slow circuit were considered.

Before showing the shape of the single output pulse, we wish displays the circuit response to a pulse train consisting of pulses carrying a charge $Q_{\text{in}} = 1.5\,\text{pC}$ and injected at rate $r = 10\,\text{MHz}$ in the case when the BLH was disabled.

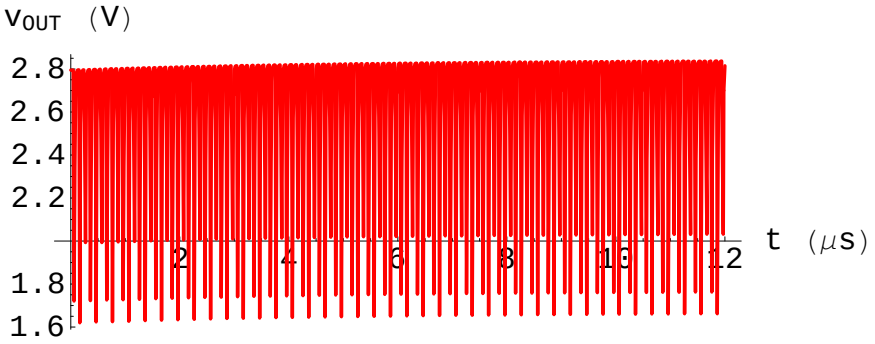


Figure 6.10: Fast-circuit response (no BLH) to a train of pulses carrying a charge $Q_{\text{in}} = 1.5\,\text{pC}$ at a rate $r = 10\,\text{MHz}$.

Figure 6.10 shows the circuit response to the first one hundred and twenty incoming pulses but does not allow us to appreciate the size of the expected voltage drift.

On the other hand from inspection of Fig. 6.11 (showing a magnification of the asymptotic output voltage drift) we can estimate a baseline shift nearly equal to 45 mV for an output signal whose peaking voltage is about 1.2 V.

6.2.1 The Shape of the Single Output Pulse

The shape of the full-circuit output signal will now be analysed in the case when a charge $Q_{\text{in}} = 4\,\text{fC}$ and a charge$Q_{\text{in}} = 1.5\,\text{pC}$ are injected into the circuit.

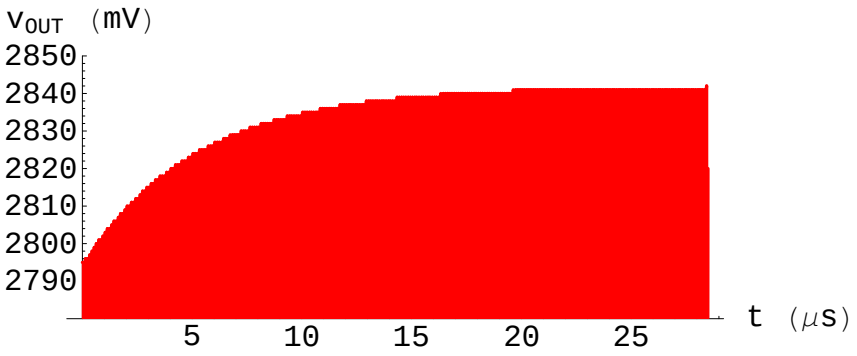


Figure 6.11: Magnification of the output-voltage region near the dc output voltage, showing the voltage drift ($Q_{\text{in}} = 1.5\,\text{pC}$, $r = 10\,\text{MHz}$).

By inspecting Fig. 6.12(a) and Fig. 6.13(a) we can see that a circuit output signal of about 4 mV is obtained in the case $Q_{\text{in}} = 4\,\text{fC}$ whereas an output signal of about 1.2 V is obtained in the case $Q_{\text{in}} = 1.5\,\text{pC}$.

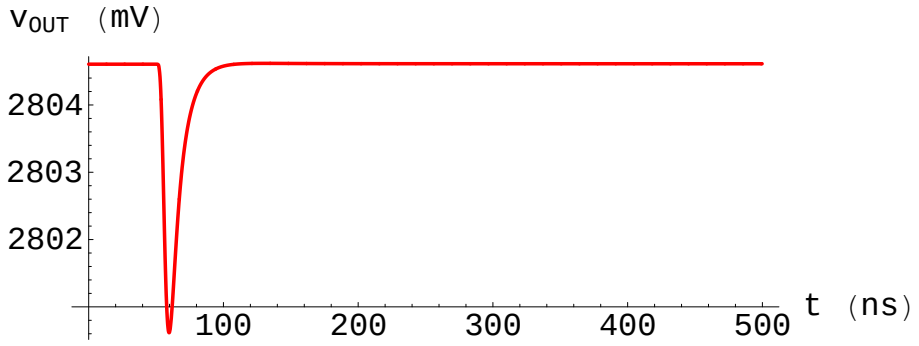
On the other hand, comparing Fig. 6.12(b) and Fig. 6.13(b) points out once again the different shape of the buffer output voltage, which is due to the dynamic clipping performed by the buffer only in the case of fast and large enough signals.

6.2.2 The Circuit Response to a Pulse Train

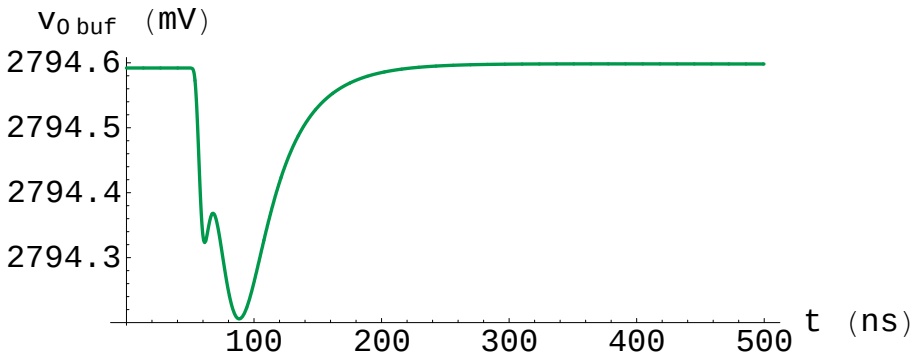
In order to quantitatively show the baseline stabilisation performed by the BLH block in the case of very narrow output signals, we will present the actual-circuit response to a two sequences of pulses injected at the same rate $r = 10\,\text{MHz}$ but carrying a different charge in each simulation.

By inspecting Fig. 6.14(b) we can note that a baseline shift approximately equal to $250\,\mu\text{V}$ occurs in the case when the charge carried by each incoming pulse is $Q_{\text{in}} = 4\,\text{fC}$.

On the other hand, by examining Fig. 6.15(b) we can observe a baseline shift approximately equal to 1.7 mV when the charge carried by each pulse is $Q_{\text{in}} = 1.5\,\text{pC}$.

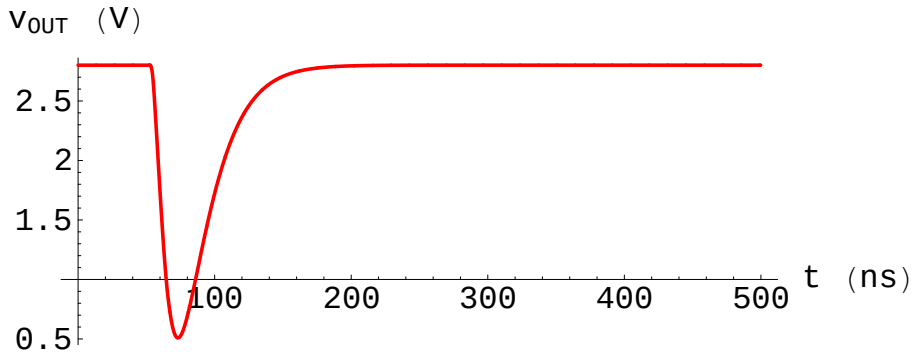


(a)

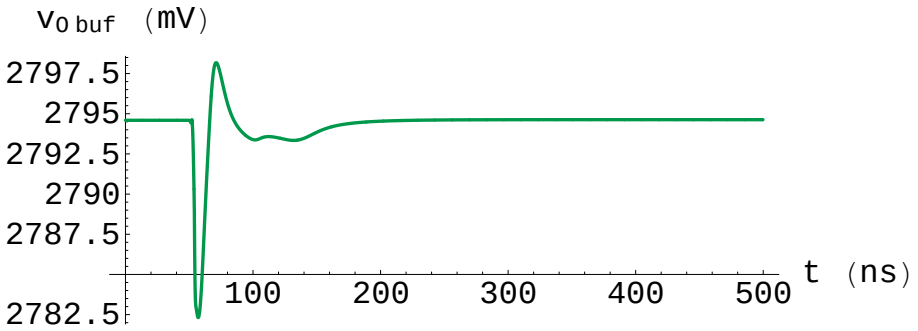


(b)

Figure 6.12: Pulse shape of (a) the full-circuit output voltage signal and (b) the buffer output voltage signal, for an incoming charge $Q_{\text{in}} = 4\,\text{fC}$ (*fast circuit*).

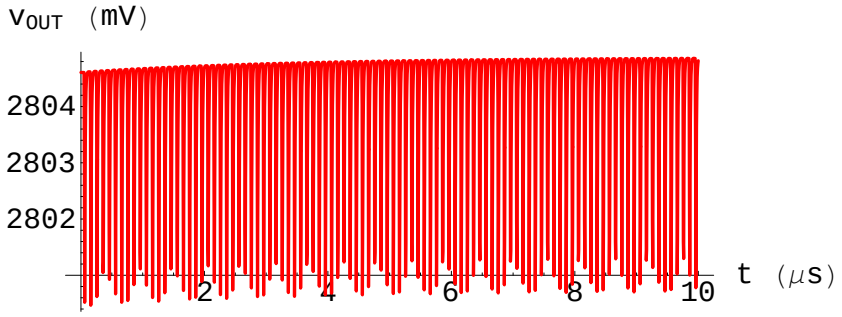


(a)

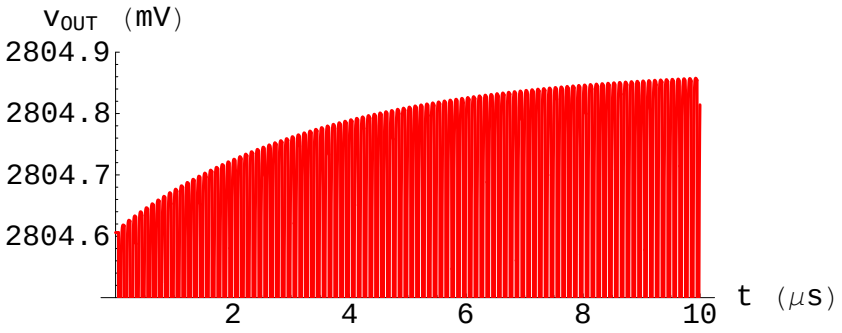


(b)

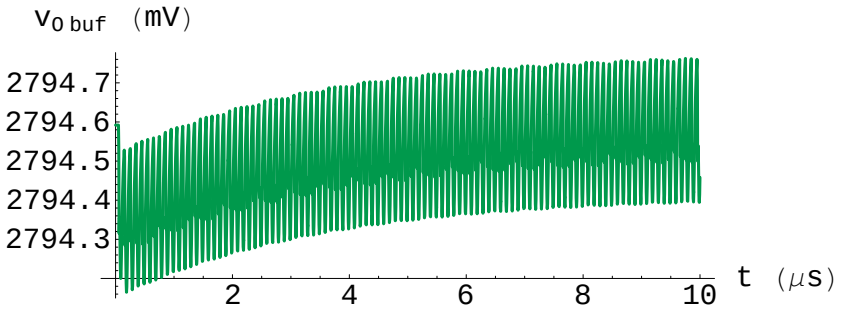
Figure 6.13: Pulse shape of (a) the full-circuit output voltage signal and (b) the buffer output voltage signal, for an incoming charge $Q_{\text{in}} = 1.5\,\text{pC}$ (*fast circuit*).



(a)

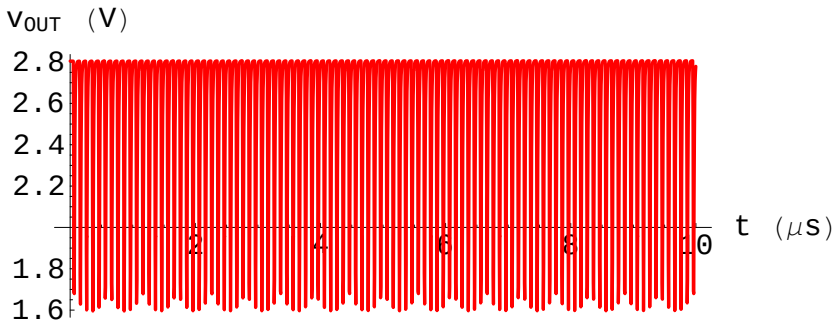


(b)

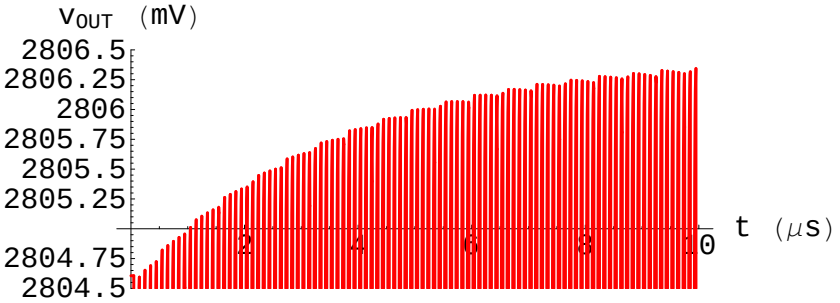


(c)

Figure 6.14: (a) Fast-circuit response to a sequence of charges $Q_{\text{in}} = 4\,\text{fC}$ injected at rate $r = 10\,\text{MHz}$, (b) magnification of the region where the baseline shift occurs and (c) buffer output voltage.



(a)



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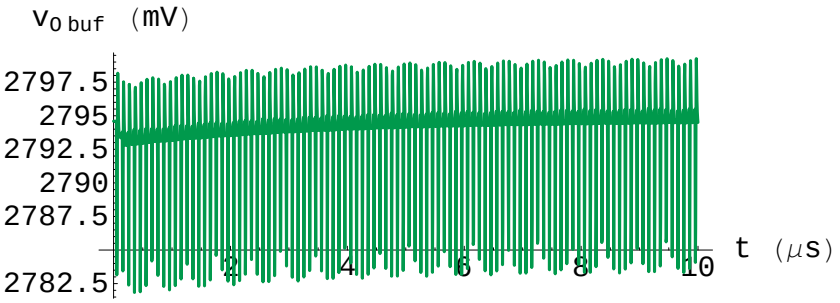


(c)

Figure 6.15: (a) Fast-circuit response to a sequence of charges $Q_{\text{in}} = 1.5\,\text{pC}$ injected at rate $r = 10\,\text{MHz}$, (b) magnification of the region where the baseline shift occurs and (c) buffer output voltage.

6.3 Baseline Fluctuations

In this section the full-circuit response to a train of random pulses will be taken into account.

In fact all the simulations so far presented have been carried out by using sequences of pulses incoming at a constant rate in order to highlight the corresponding asymptotic voltage shift.

However in practice output baseline fluctuations occur due to the random arrival of the pulses coming from the detector.

Thus, by means of *Mathematica* simulations concerning the slow-circuit response when the slew-rate limited buffer is disabled, we will show some typical circuit responses to random sequences of incoming pulses.

As mentioned in Chap. 3, it is known that the number of events (pulse arrivals) occurring in a time interval t follows the Poisson distribution so that the time elapsing between two consecutive events follows an exponential distribution.

In particular let us recall that a *counting process* $\{X(t) \,|\, t \in \mathrm{R}^+ \cup \{0\}\}$ is called a *Poisson process* with *intensity* $\lambda(>0)$ if:

1. $X(0) = 0$
2. $\{X(t)\}$ has *stationary*[1] *independent*[2] *increments*
3. $P[X(t+\Delta t) - X(t) = 1] = \lambda\,\Delta t + o(\Delta t)$
4. $P[X(t+\Delta t) - X(t) \geq 2] = o(\Delta t)$

where $o(\Delta t)$ is a function of Δt such that

$$\lim_{\Delta t \to 0} \frac{o(\Delta t)}{\Delta t} = 0$$

It can be shown that under the above assumptions $X(t)$ has a Poisson distribution with parameter $\lambda\, t$

$$p_n(t) = P[X(t) = n] = e^{-\lambda t}\frac{(\lambda\, t)^n}{n!} \qquad n = 0, 1, 2, \ldots$$

[1] A stochastic process $\{X(t) \,|\, t \in \mathrm{T}\}$ of real-valued random variables $X(t)$ is said have *stationary increments* if the pdf for $X(s+t) - X(s)$ is the same for all $s \in t$ such that $(s+t) \in t$.

[2] A stochastic process $\{X(t) \,|\, t \in \mathrm{T}\}$ of real-valued random variables $X(t)$ where T is linearly ordered is said have *independent increments* if for any t_1, t_2, t_3, $t_4 \in \mathrm{T}$ such that $t_1 < t_2 < t_3 < t_4$, $X(t_2) - X(t_1)$ and $X(t_4) - X(t_3)$ are independent random variables.

and

$$E[X(t)] = \lambda\, t$$

As a result the random variables Z_1, Z_2, ... each representing the time elapsing between two successive events in a Poisson process $X(t)$ with *intensity* λ, are independent exponential random variables with parameter λ.

For purposes of illustration, let us show what we have just stated, only for Z_1. Since

$$P\,[Z_1 > t\,] = P\,[X(t) = 0\,] = e^{-\lambda t}$$

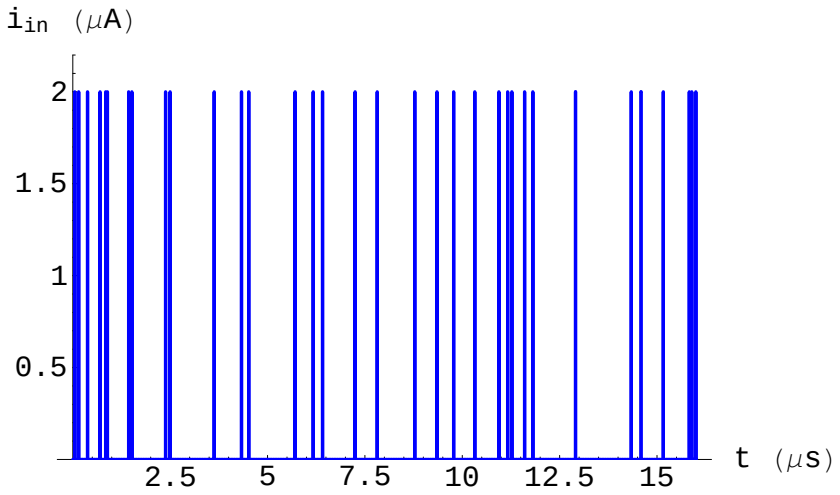
we have

$$F_{Z_1}(t) = P\,[Z_1 \leq t\,] = 1 - e^{-\lambda t}$$

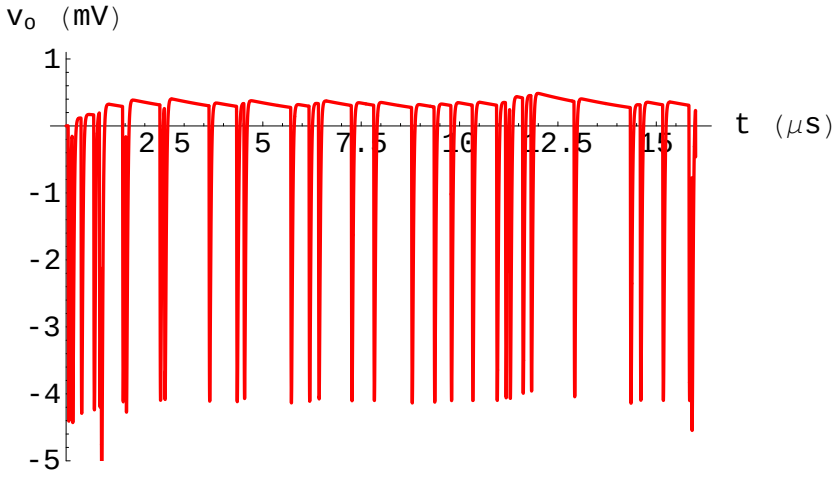
which implies that Z_1 is really an exponential random variable with parameter λ.

By examining now the simulation results shown in Fig. 6.16(b) and in Fig. 6.17(b) we can directly appreciate the expected baseline fluctuations.

We can note that in the case of an average counting rate of 5 MHz the *pile-up* effect becomes evident due to the fact that even pulses separated by a time interval shorter than 200 ns can occur.

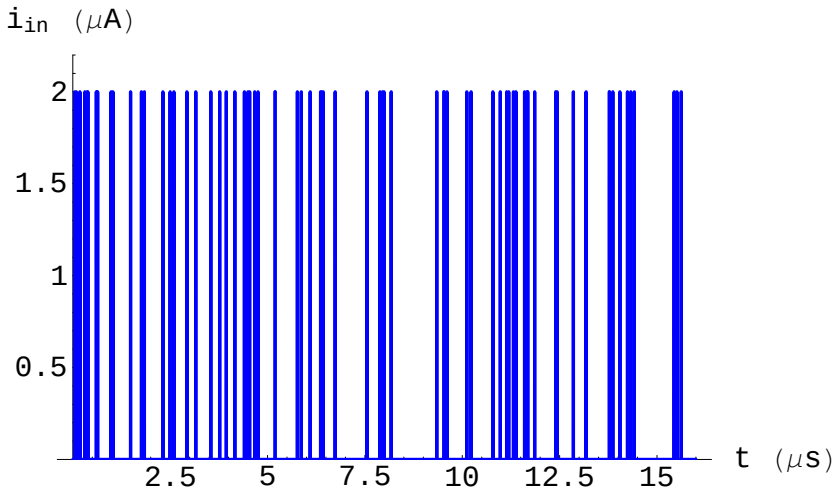


(a)

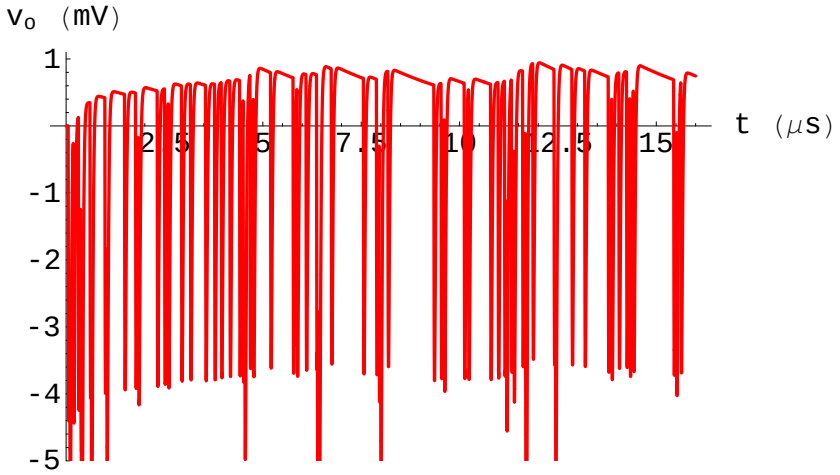


(b)

Figure 6.16: (a) Random sequence of incoming pulses (average pulse rate: 2 MHz) and (b) circuit response (*slow circuit*).



(a)



(b)

Figure 6.17: (a) Random sequence of incoming pulses (average pulse rate: 5 MHz) and (b) circuit response (*slow circuit*).

Conclusions

The thesis has presented the design of the final version of the CMAD chip for the COMPASS experiment.

First, a thorough study of all the analog part of the circuit has been carried out and an analytical model suitable for representing and predicting the circuit behavior has been conceived in order to identify the main architecture limitations and drawbacks.

It has been found that the most severe limitations to the circuit prototype came from a non-linear buffer employed in the baseline holder (BLH) circuit.

Therefore a modified version of this buffer has been developed.

The improvement in circuit performance can be observed both when the circuit deals with the main unipolar pulses coming from the detector and when it manages sporadical pulses of opposite sign, even if in this case the circuit shows an adequate behavior up to a maximum pulse rate of about 500 kHz.

In particular, in the case of the main unipolar pulses, with an output peaking voltage equal to 2.3 V (incoming charge: 2 pC), a peaking time of 21 ns and a pulse rate of 5 MHz an aymptotic baseline shift nearly equal to 2 mV has been predicted on the basis of the performed transistor-level SPICE simulations.

Also the BLH sensitivity to the parasitic feedthrough of the input signal has been considerably reduced by avoiding the direct coupling between the buffer load capacitance and the intrinsic gate-source capacitances of the differential input pair.

Moreover, another important goal achieved has been a significant increase in the full-circuit output swing.

The old circuit architecture allowed only a dc output voltage equal to 2 V whereas the new architecture is able to provide a maximum output swing nearly equal to 3 V, without any transistor entering the triode region.

As far as the BLH power consumption is concerned, we wish to point out that

the buffer consumes about 330 μW whereas the transconductor block only consumes 3 μW.

Furthermore the new buffer has an area which is only 40% with respect to the one taken by the old buffer.

An enhanced version of the whole amplifier has already been designed. The CSA and the pulse shaper have been modified in this version to obtain faster signals providing a higher counting rate.

In fact the new version can work properly up to a rate $r = 10$ MHz still providing a baseline stabilisation within the given specifications, namely a baseline shift approximately equal to 1.7 mV with an output peaking voltage of 1.2 V (incoming charge: 1.5 pC), a peaking time of 10 ns and a rate of 10 MHz.

It should also be pointed out that the maximum counting rate is related to the preamplifier and pulse shaper parameter optimisation.

Such an optimisation should be performed by taking into account both the time length of the pulse and the circuit noise performance.

In fact although an increasingly narrow output pulse provides an increasingly high maximum counting rate, we must recall that the faster the circuit the wider its bandwidth and thus the larger the noise contribution involved in the signal processing.

The circuit will be submitted to the foundry by the end of January 2006 (Austria Mikro Systeme, AMS – 0.35 μm) whereas the integration of the ASIC in the final application is foreseen for late 2006.

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