Analog Front-end Design in Deep Sub-micron CMOS Technology for Timing application in Pixel detectors

Lorenzo Piccolo

Università degli studi di Torino

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1 TIMESPOT

2 The Studied Front-end design

3 Simulations Results

4 Conclusions and Future Developments
1. TIMESPOT

2. The Studied Front-end design

3. Simulations Results

4. Conclusions and Future Developments
Measure rare events $\rightarrow$ peak luminosity increase $(\sim 7 \times 10^{34} \text{cm}^{-2}\text{s}^{-1})$
- Pile-up events per bunch crossing increases from 27 to 200 $\rightarrow$ loss in tracking efficiency
- Detectors radiation hardness must be up to $10^{17} \text{MeV/cm}^2 \text{n}_{eq}$
- HL-LHC will be operative by the end of 2025

100 pile-up events of a pp 13 TeV collision recorded by CMS on 14 Oct 2016
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TIMESPOT: R&D a 4D Tracking Detector Prototype

- Requirements:
  - Pixel pitch $(55 \times 55) \mu m$
  - Time resolution on single hit $< 100ps$
  - Radiation resistance: $10^{16}$ to $10^{17} n_{eq}/cm^2$
  - System level solution $\rightarrow$ sensor, front-end electronics and tracking logic
  - 10 INFN research unit involved
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Shorter inter-electrodes distance
- Fast current signals
- Intrinsic radiation hardness

Two variants explored: Silicon (Università di Trento) and Diamond (INFN Perugia) based

Geometry impacts timing and electrical characteristics → interplay with electronics design
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Pixel Architecture

- **Binary FE with Timing** $\rightarrow < 100\text{ps TDC}$
- High signal-rate $\rightarrow$ **per-Pixel timing** measurement
- Pixel FE requirements $\rightarrow$ low-noise, compact, low-power, rad-hard
- A novel **28 nm CMOS** process node is selected
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The 28 nm CMOS Process

- **Novel technology** in the radiation detectors field
- More compact and power efficient → new integration possibilities
- **New materials**
- New lithography technique based on *interference masks* → *regular fabrics*
- Interconnections doesn’t scale properly → more parasitic effects → careful layout design
- Reduced power supply voltage → less headroom for analog circuits
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Sensor modelled with parameters extracted from simulations

- Input amplifier: **Charge Sensitive Amplifier** with DC current compensation and DC voltage setting
- Discriminator: **Leading Edge Discriminator** with offset compensation
- **Two versions**: preliminary 65 nm one and 28 nm target one (currently CSA only)
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Input current pulse  Amplifier output  Discriminator output
**Charge Sensitive Amplifier (CSA)**

- **Output voltage amplitude** $\propto$ **input charge**
- **Constant peaking and falling times** $\rightarrow$ **good timing performance**
- **Low noise**

**Krummenacher Filter:**
- Active feedback path $\rightarrow$ pulse shape
- **DC current compensation** $\rightarrow$ **input leakage current**
- **DC voltage setting** $\rightarrow$ full range exploitation
- **50 nA** total current $\rightarrow$ small power consumption impact

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**Telescopic cascode amplifier** with split bias current branches

- Almost 60 dB gain
- Output buffer
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2 stage amplification

- Inverter → digital output buffer
- Offset Correction Circuit: store offset variability inside $C_{oc}$
  - correct intra-channels variability
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Offset Correction Circuit: store offset variability inside $C_{oc}$
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● **1st** stage: low gain, differential
● **2nd** stage: high gain, single ended
● $t_d \sim 5\,\text{ns}$ average delay time
● 3 $\mu\text{A}$ total current

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CSA successfully ported to the 28 nm node

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● Main effect on baseline $\rightarrow$ offset correction ($\times 5$ improvement)

● $\sigma_p = 163\,\text{ps} \rightarrow$ per-chip calibration
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  - Studied on discriminator differential cell $\rightarrow$ discriminator delay time $t_d$
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- In 28 nm, for low range signals: $SNR \sim 14.5$,

- Simulated $\sigma_{tn} \sim 100$ ps RMS

- Optimization needed
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\begin{align*}
\text{SNR} &= \frac{V_{peak}}{V_{noise}} \\
\text{Noise} &= \frac{1}{\sqrt{2}} \cdot \frac{V_{peak}}{\text{SNR}}
\end{align*}
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Time-walk

- **threshold crossing drift** related to signals **amplitude**
- Current pulses obtained assuming constant pulses **duration** → input charge: \((1 \div 10)fC\)
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- total variation 2.1 ns → time-walk correction needed (CFD or ToT)
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- Ideal ToT very linear → correction applicable in the monotonic range
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- Good results for the 65 nm design
- The CSA design was successfully ported in 28 nm
- Good timing reliability for signal, mismatch and process variations

Future Developments

- Optimize for noise reduction
- Investigate time-walk correction techniques
- 28 nm discriminator implementation
- Produce 28nm layout
- Simulation with parasitics and optimization
- A test chip for analog blocks will be produced later this year
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