Analog Front-end Design in Deep Sub-micron CMOS Technology for Timing application in Pixel detectors

Lorenzo Piccolo

Università degli studi di Torino

13.04.2018, Presentazione Tesi

Outline

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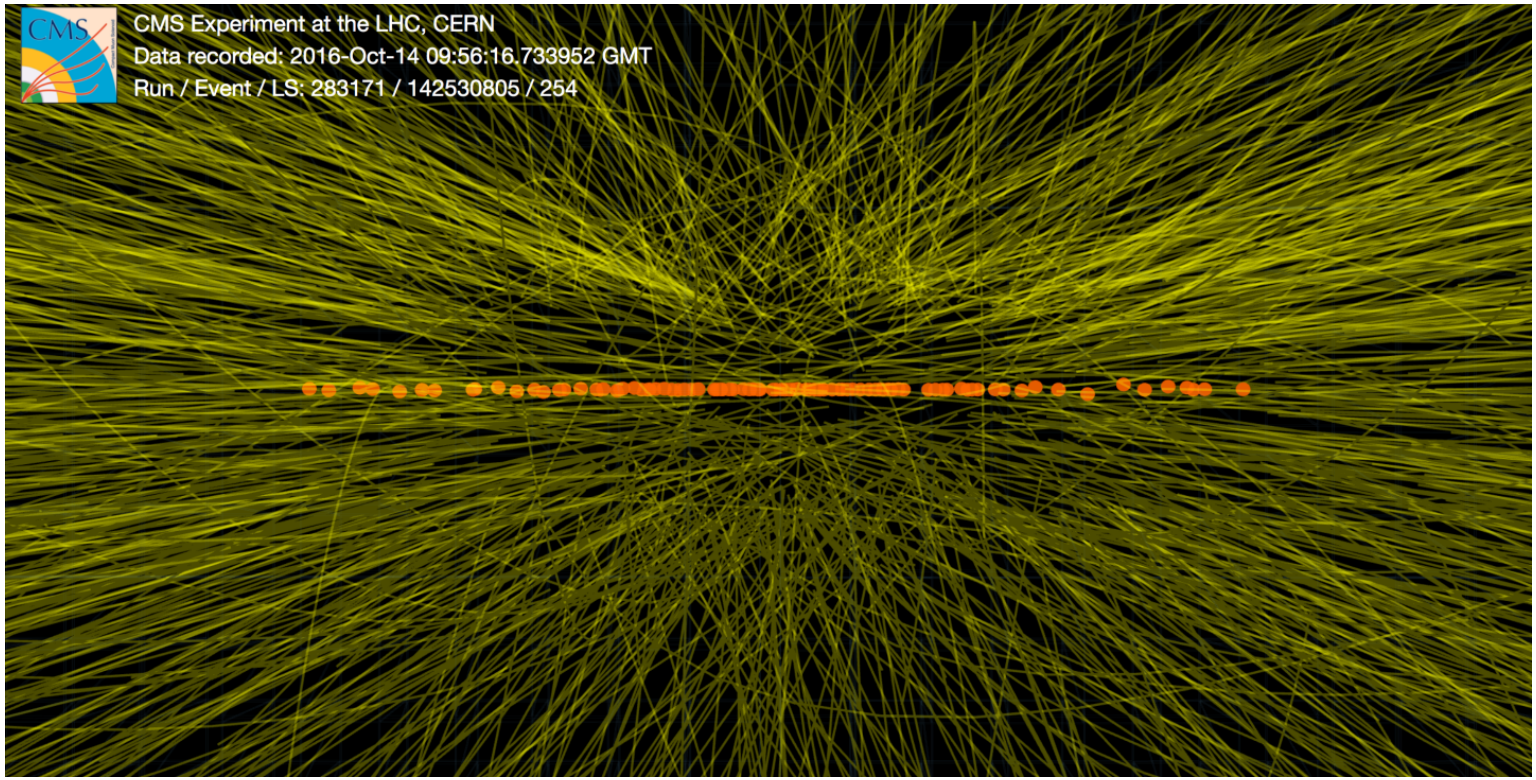
High Luminosity HEP Experiments Upgrade



100 pile-up events of a pp 13 TeV collision recorded by CMS on 14 Oct 2016

- Measure rare events $\rightarrow$ peak luminosity increase ($\sim 7 \times 10^{34} cm^{-2} s^{-1}$)
- Pile-up events per bunch crossing increases from 27 to 200 $\rightarrow$ **loss in tracking efficiency**
- Detectors **radiation hardness** must be up to $10^{17} MeV/cm^2$ n_{eq}
- HL-LHC will be operative by the end of 2025

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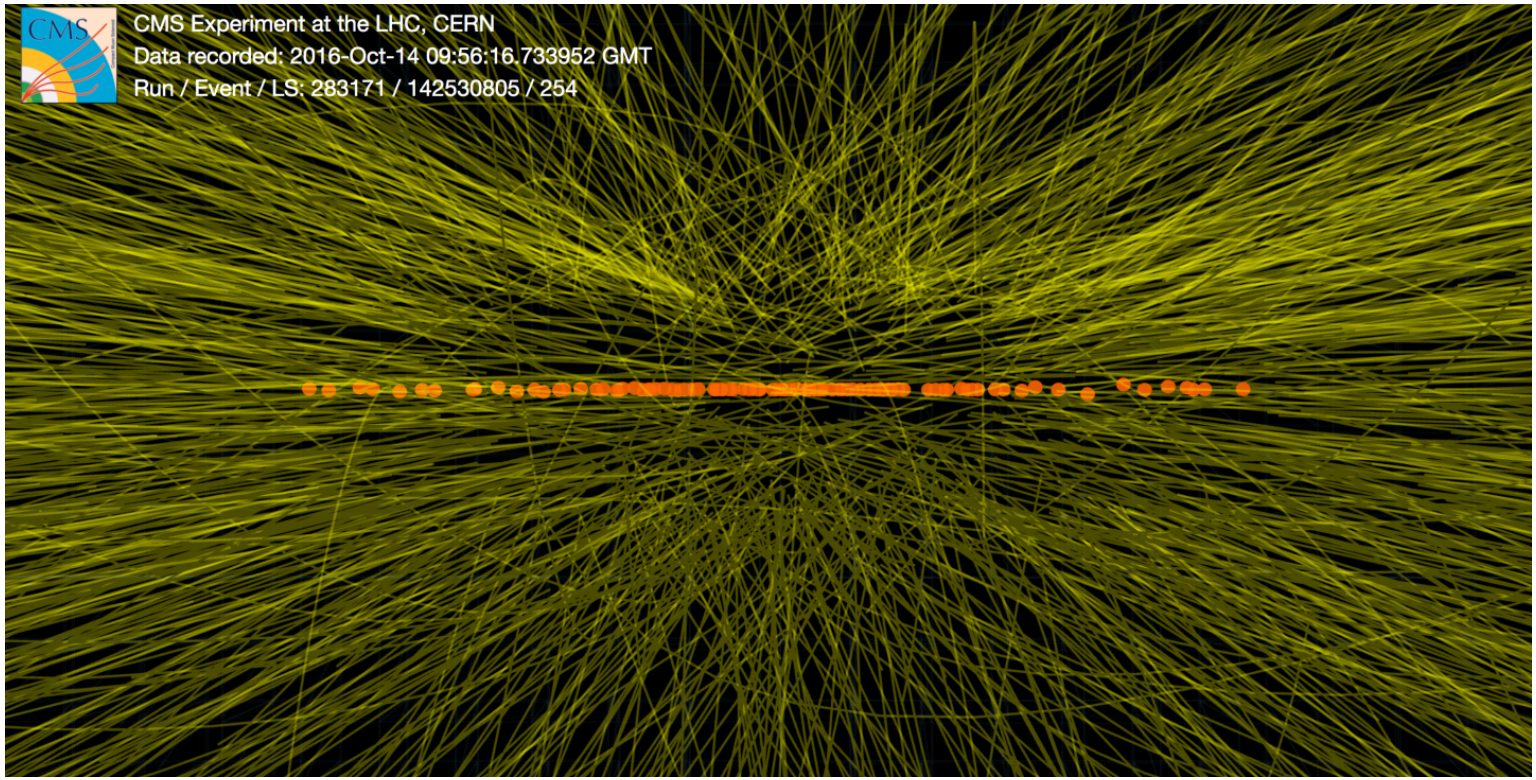

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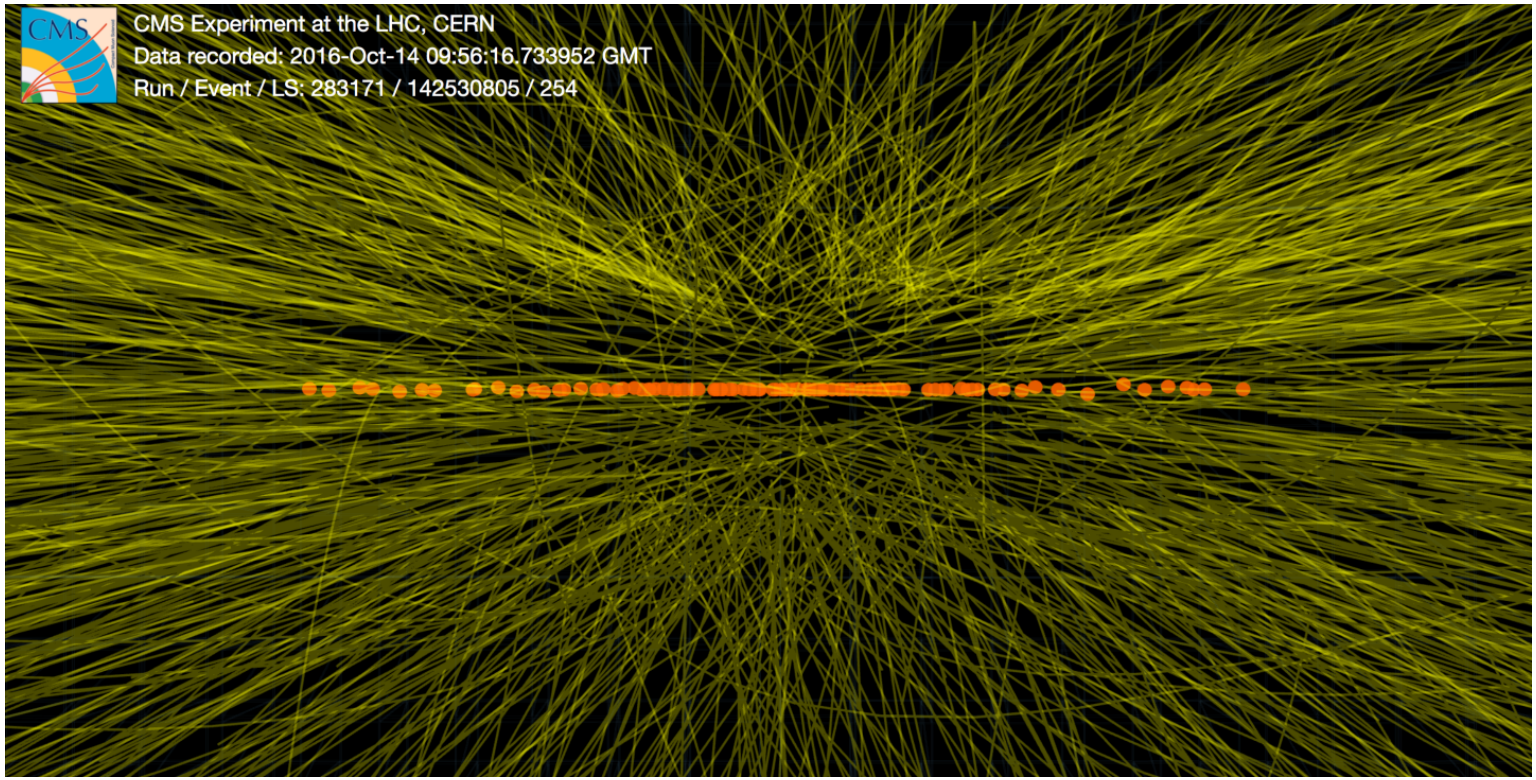

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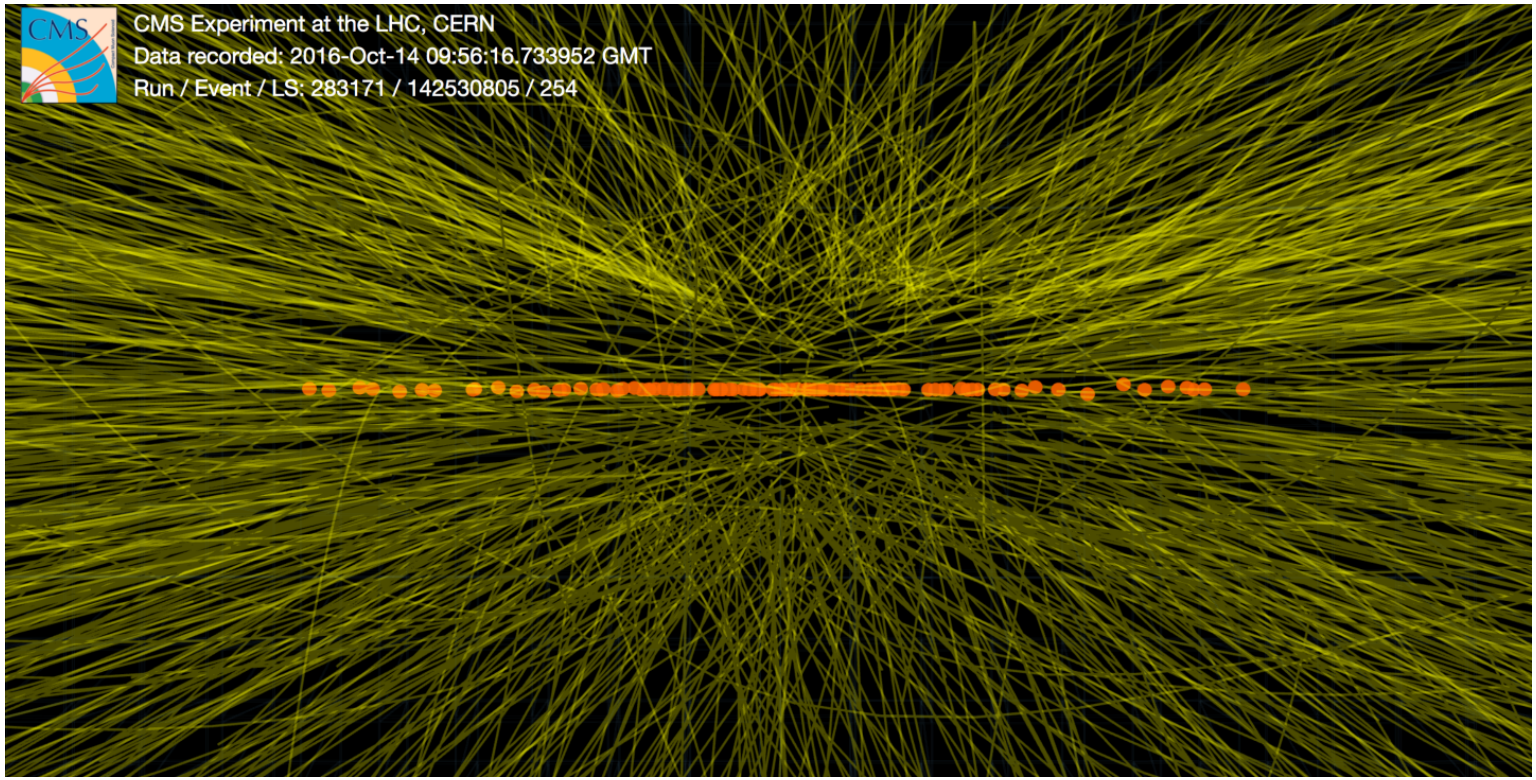

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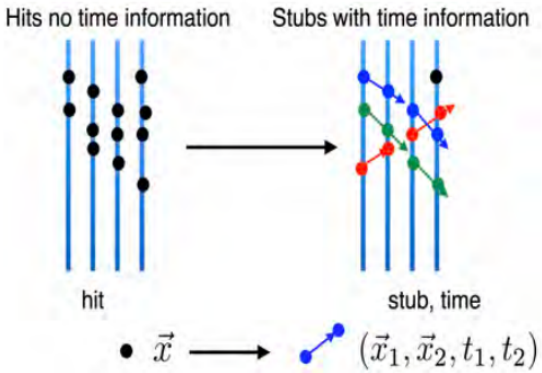

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- Requirements:
  - Pixel pitch $(55 \times 55)\mu m$
  - Time resolution on single hit $< 100ps$
  - Radiation resistance: 10^{16} to $10^{17} n_{eq}/cm^2$
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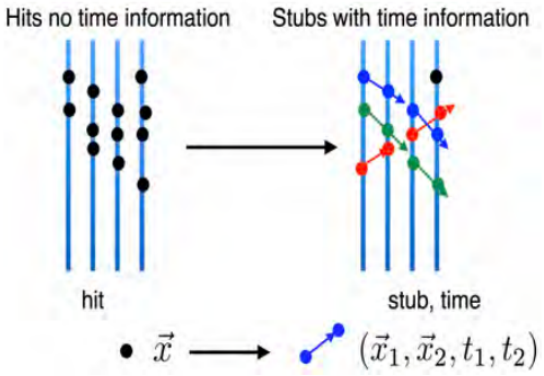

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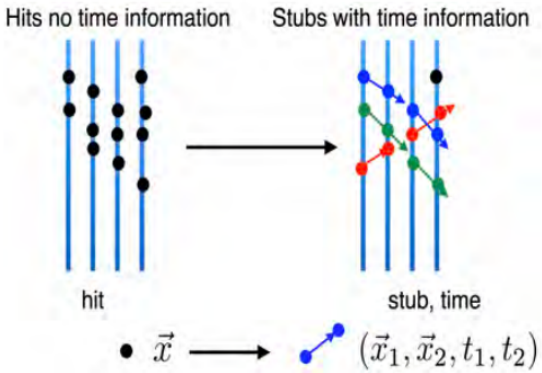

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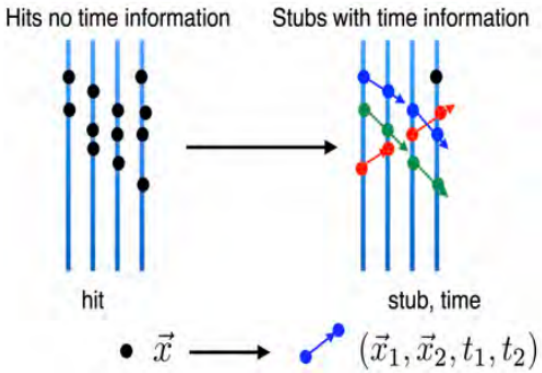

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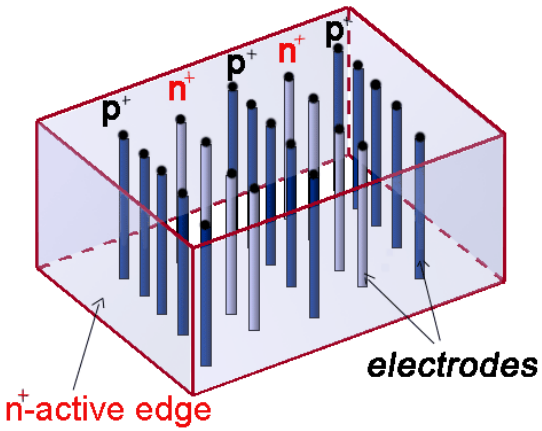
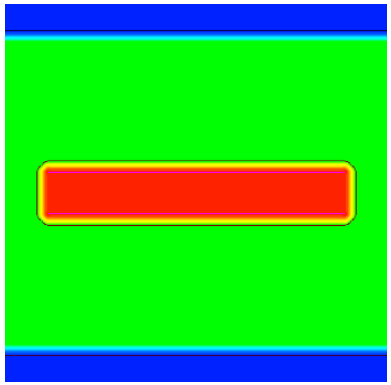
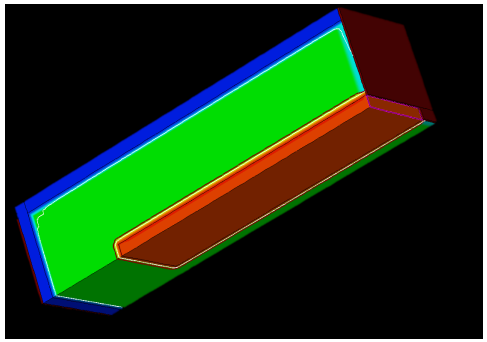




3D Si cross section



3D Si sensor

- Shorter inter-electrodes distance
  - **Fast** current signals
  - Intrinsic **radiation hardness**
- Two variants explored: Silicon (Università di Trento) and Diamond (INFN Perugia) based
- Geometry impacts timing and electrical characteristics → interplay with electronics design

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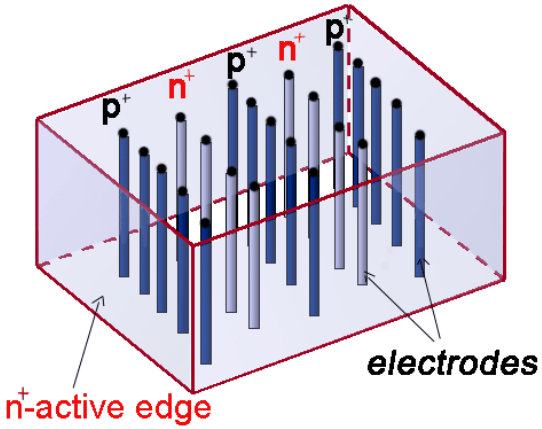

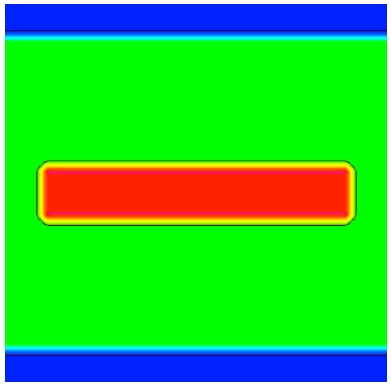

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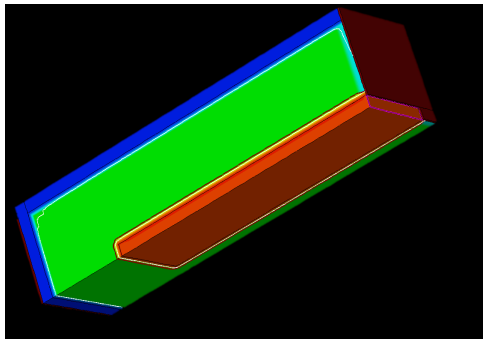

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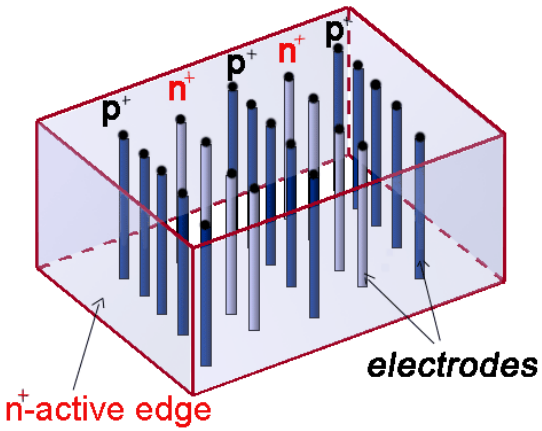

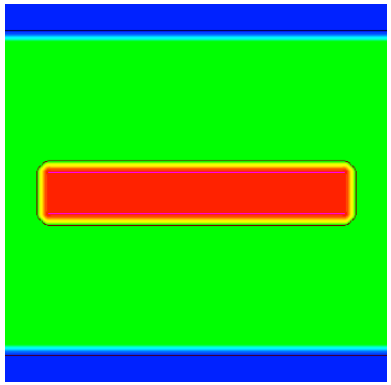

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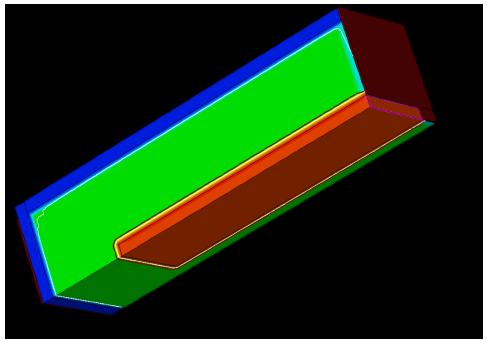

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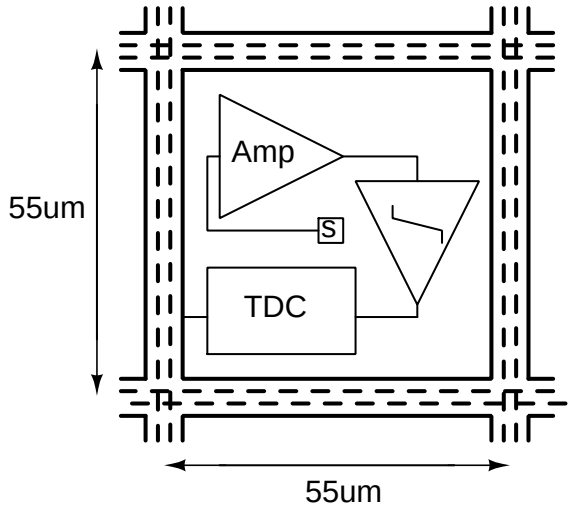

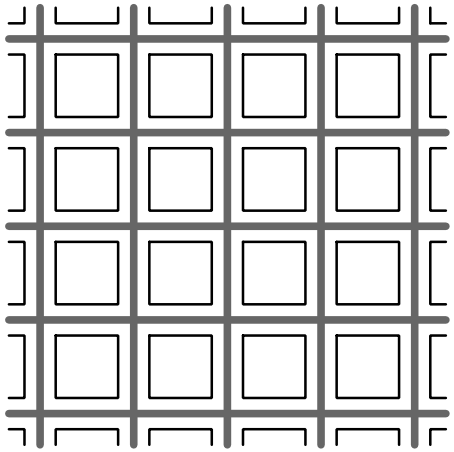

- Binary FE with Timing $\rightarrow$ $<$ **100*ps* TDC**
- High signal-rate $\rightarrow$ **per-Pixel timing** measurement
- Pixel FE requirements $\rightarrow$ low-noise, compact, low-power, rad-hard
- A novel **28 nm CMOS** process node is selected

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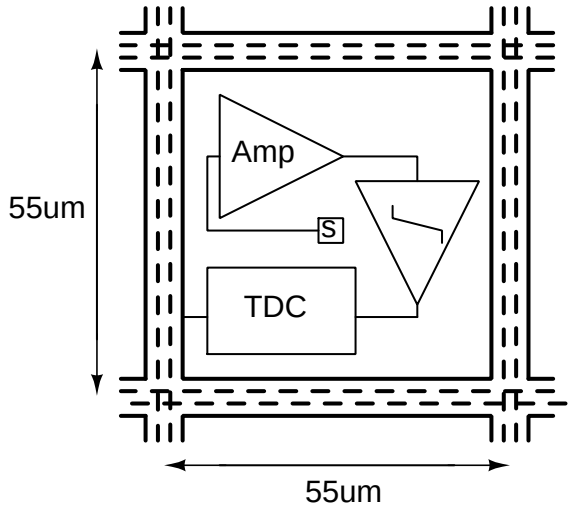

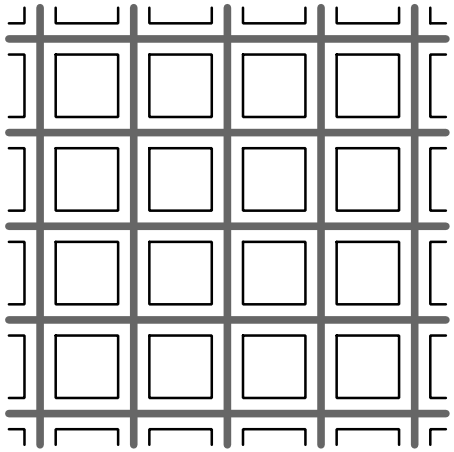

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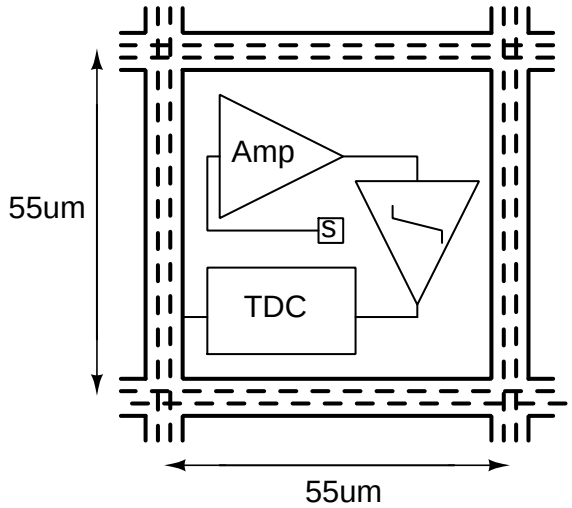

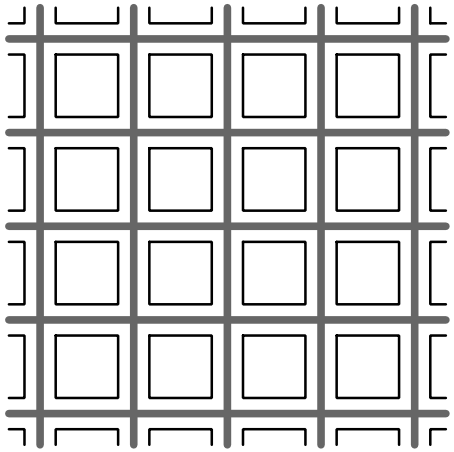

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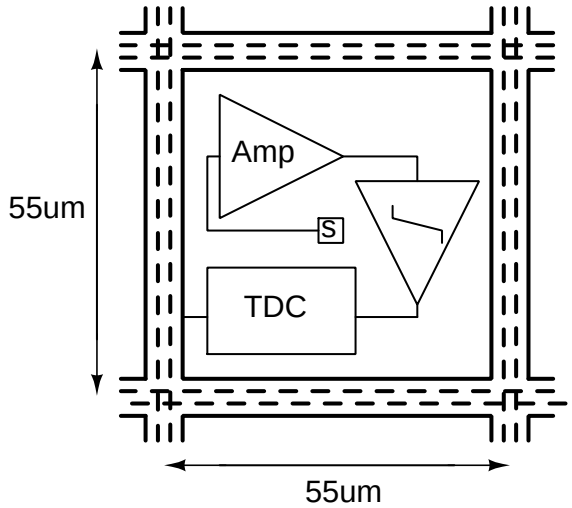

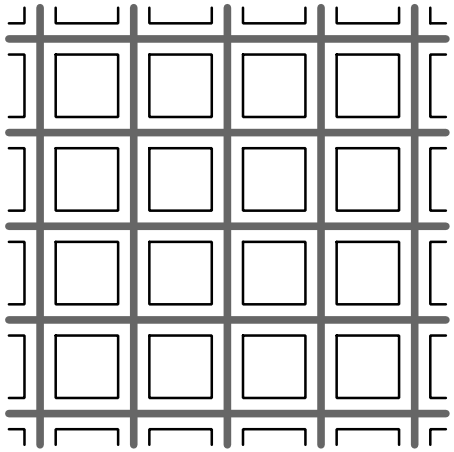

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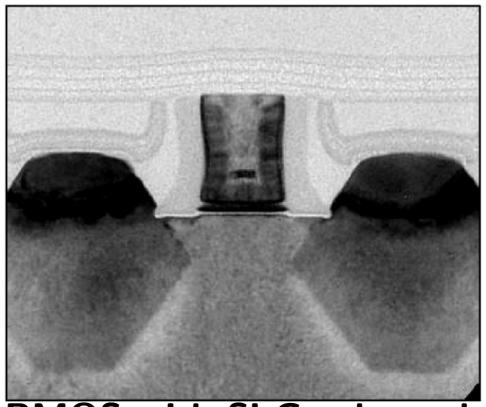

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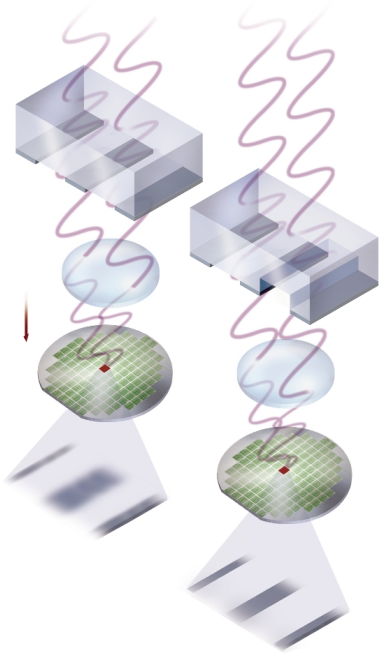
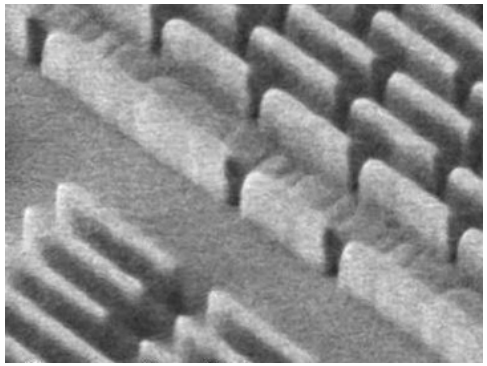


concept of PSM



regular fabrics

- **Novel technology** in the radiation detectors filed
- More compact and power efficient → new integration possibilities
- **New materials**
- New lithography technique based on **inteference masks** → **regular fabrics**
- interconnections doesn't scale properly → more parasitic effects
  → careful layout design
- reduced power supply voltage → **less headroom for analog circuits**

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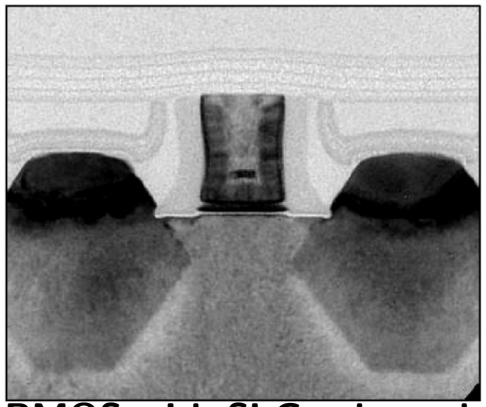

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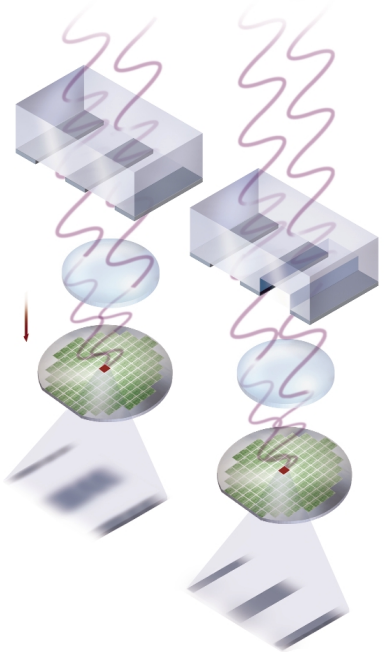

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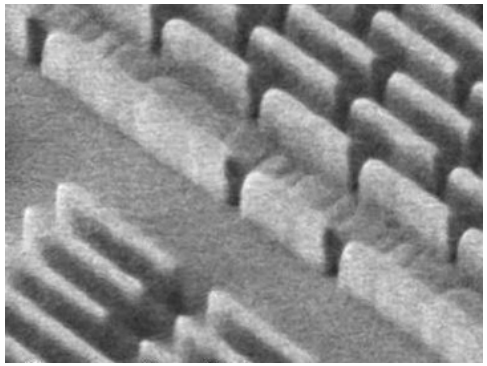

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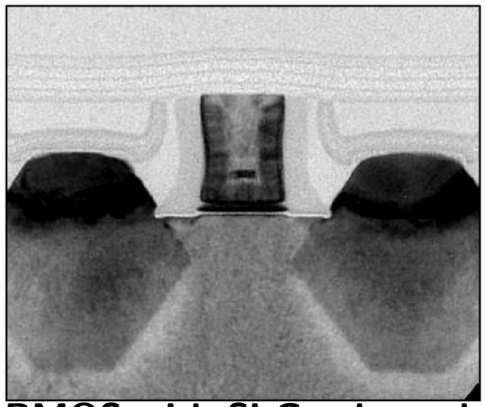

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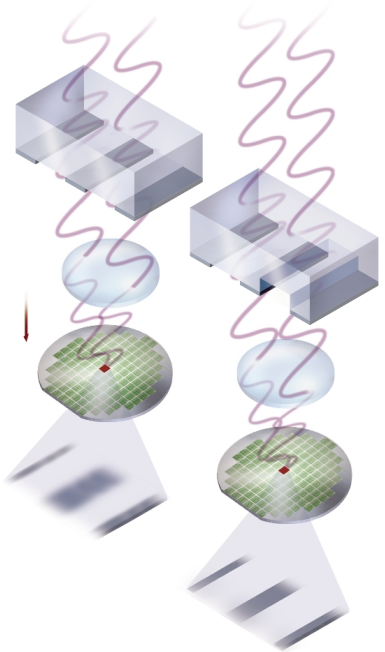

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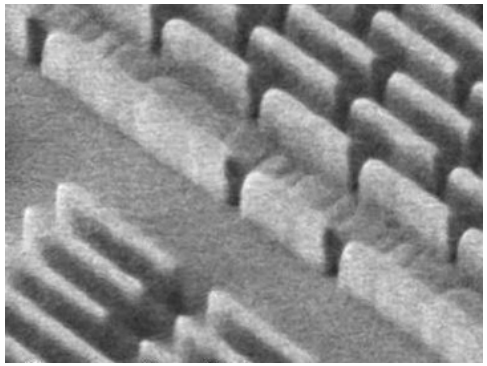

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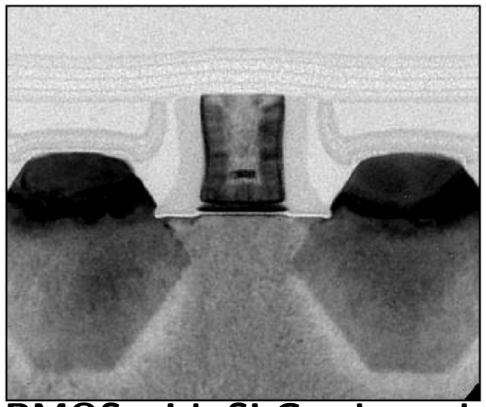

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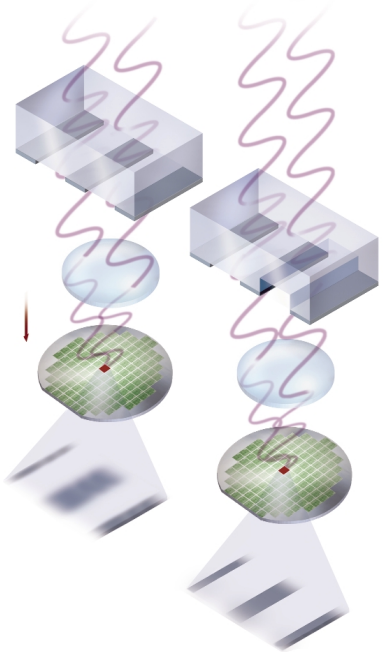

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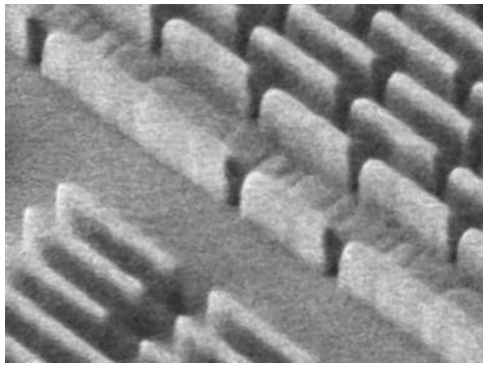

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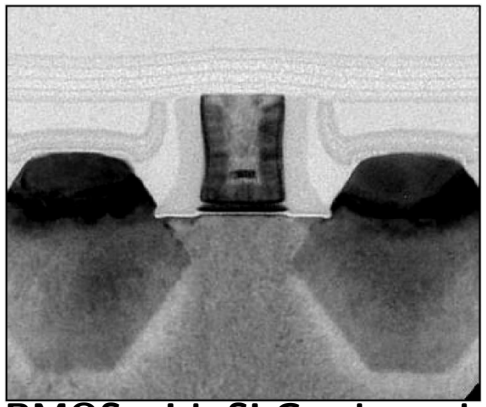

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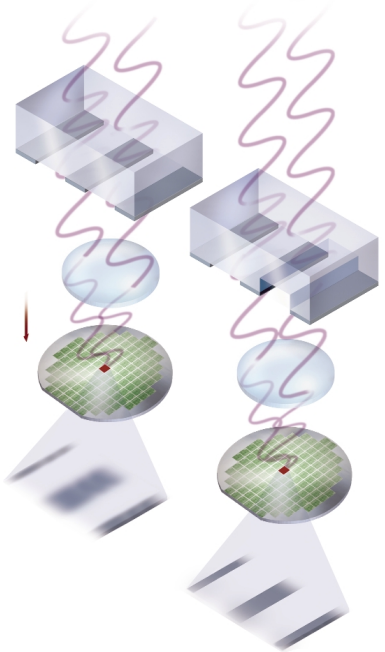

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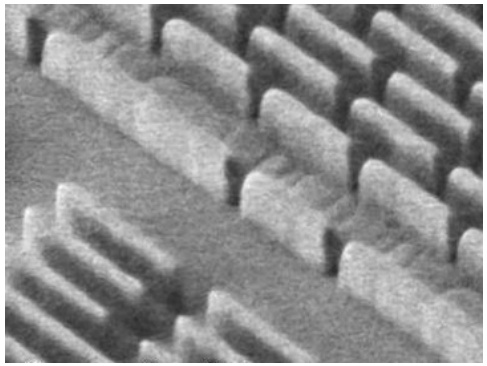

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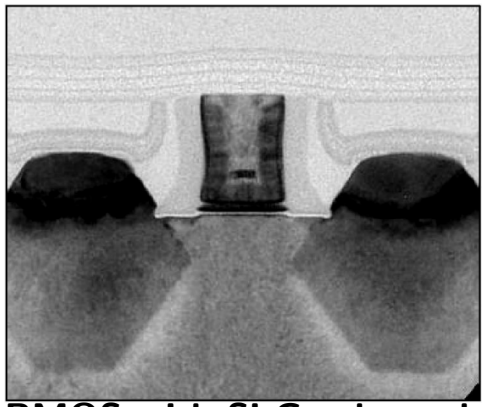

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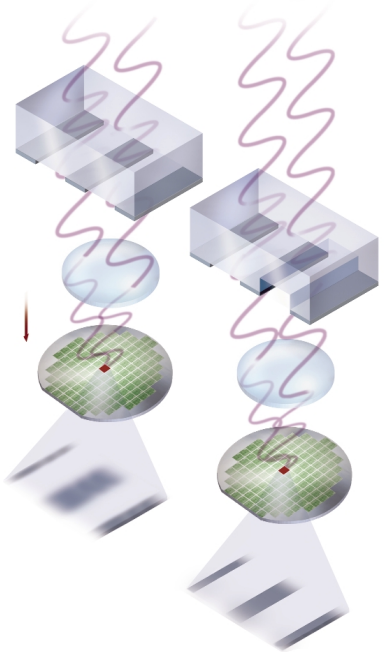

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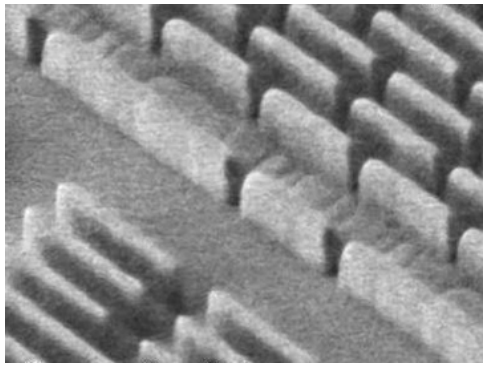

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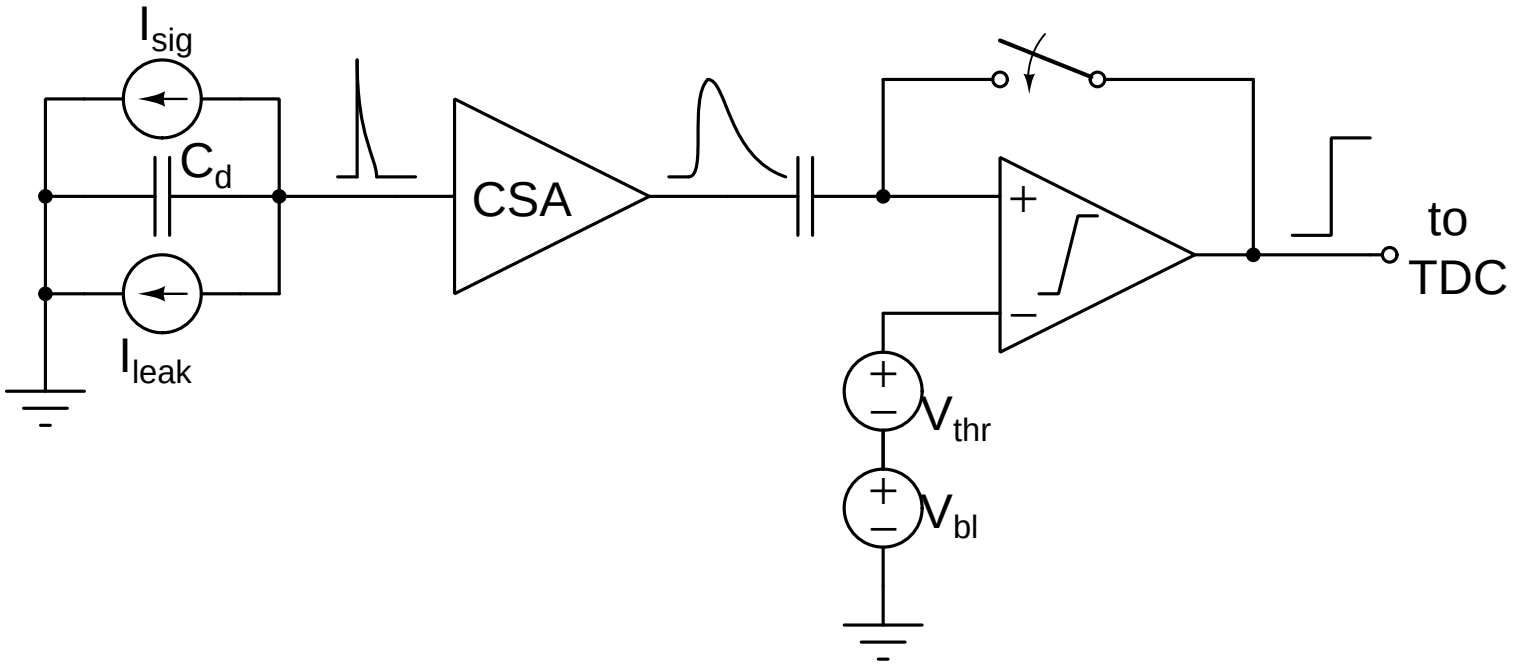
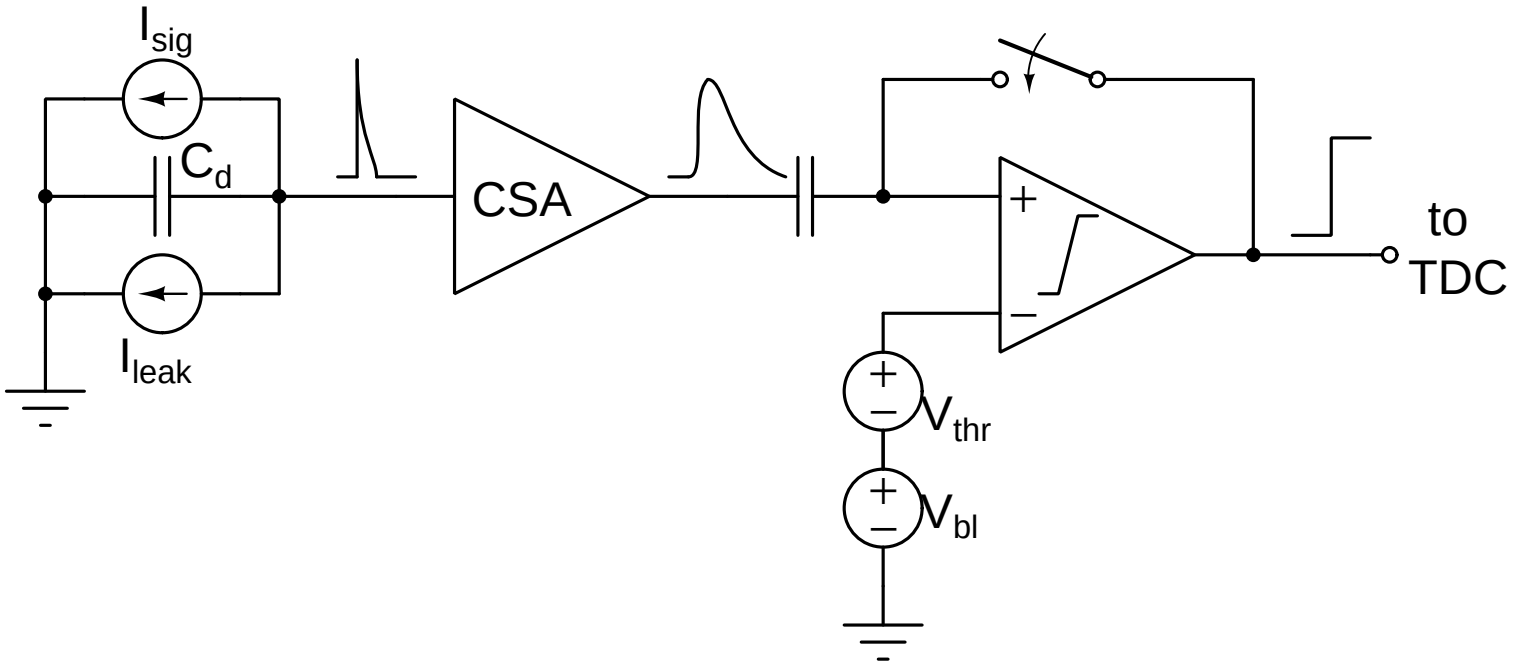


- Sensor modelled with parameters extracted from simulations
- Input amplifier: **Charge Sensitive Amplifier** with DC current compensation and DC voltage setting
- Discriminator: **Leading Edge Discriminator** with offset compensation
- **Two versions**: preliminary 65 nm one and 28 nm target one (currently CSA only)

Overview



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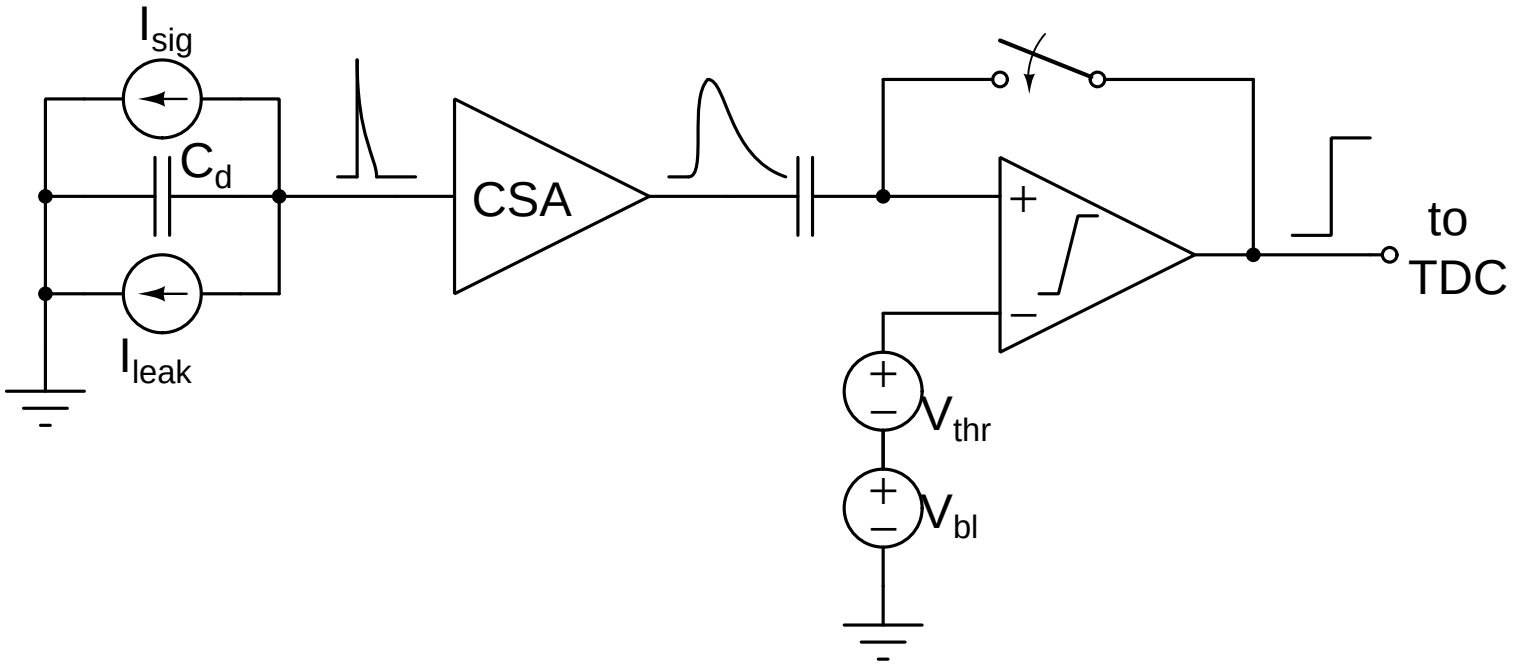

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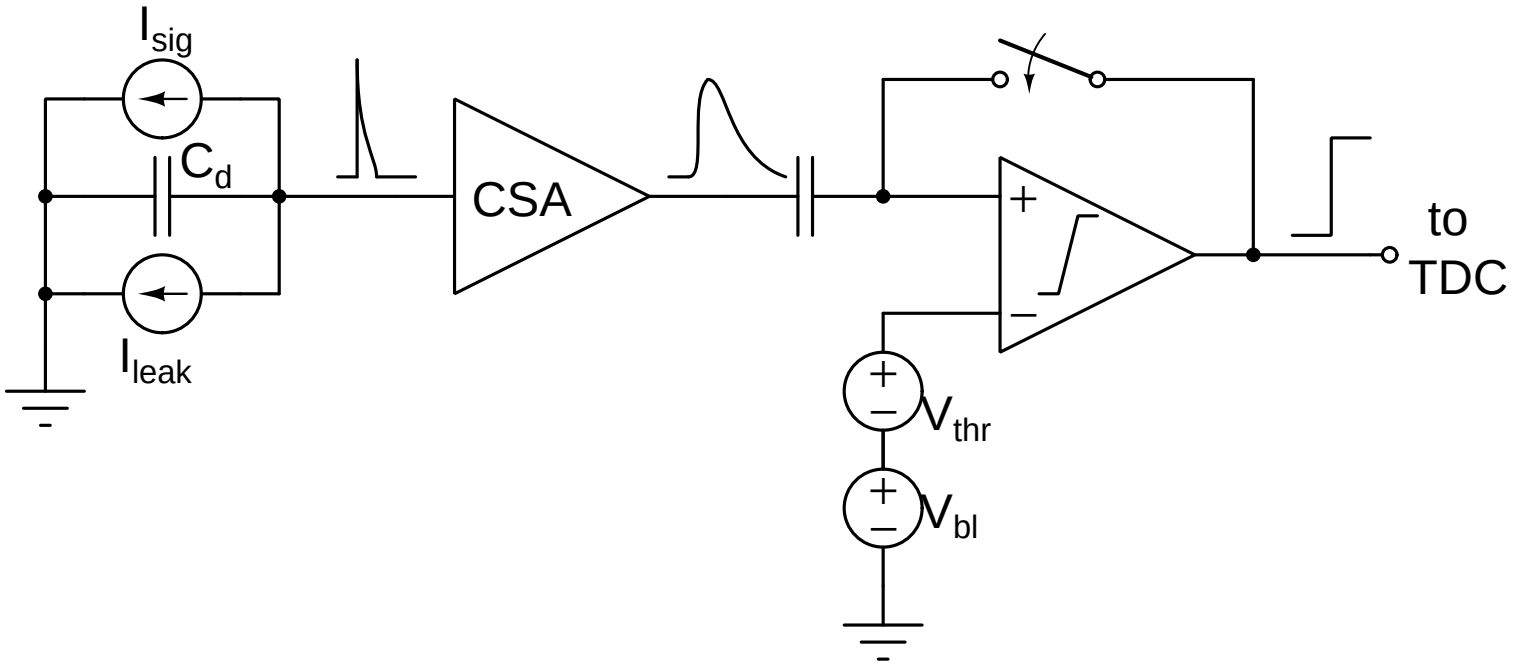

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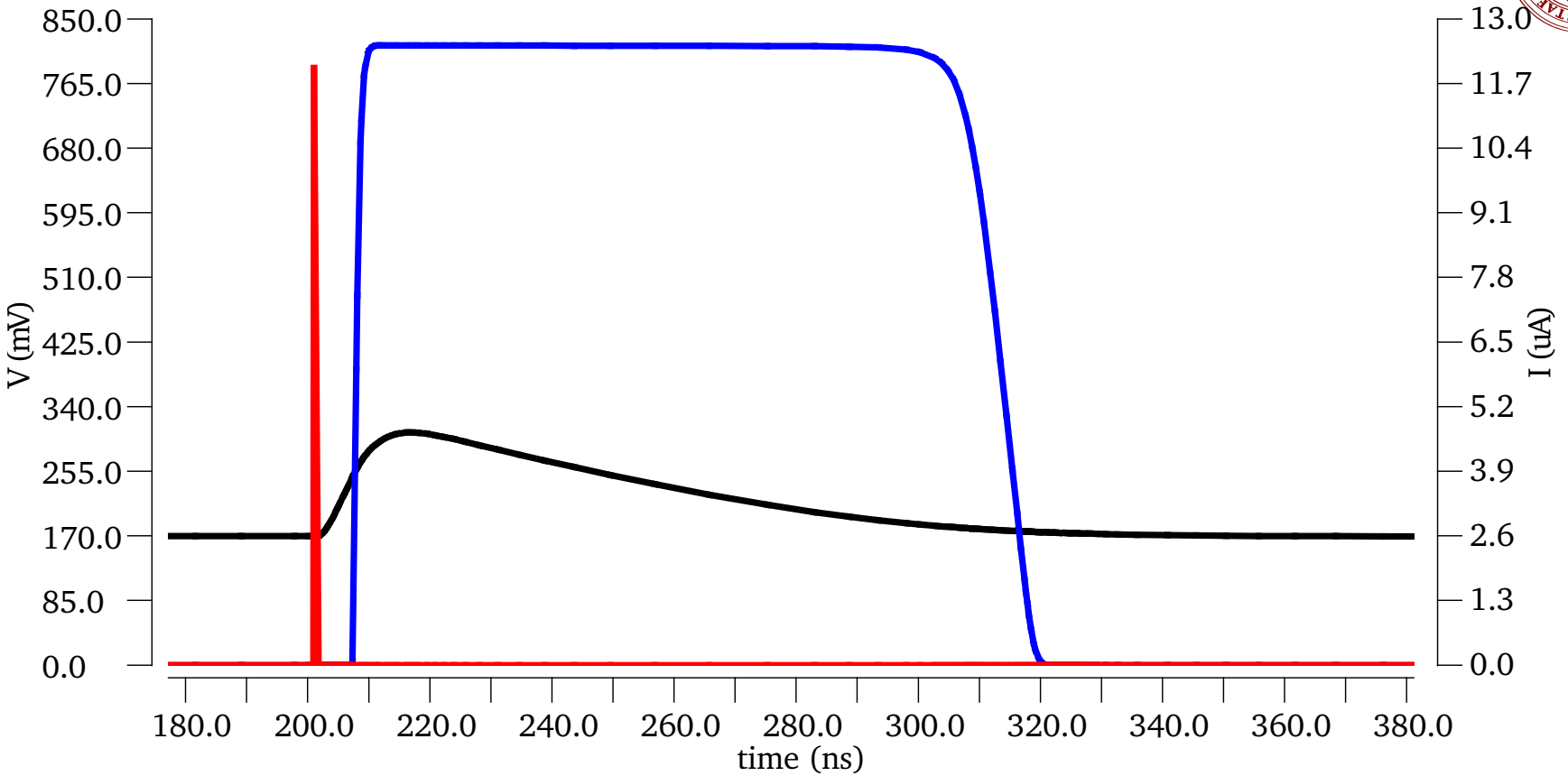
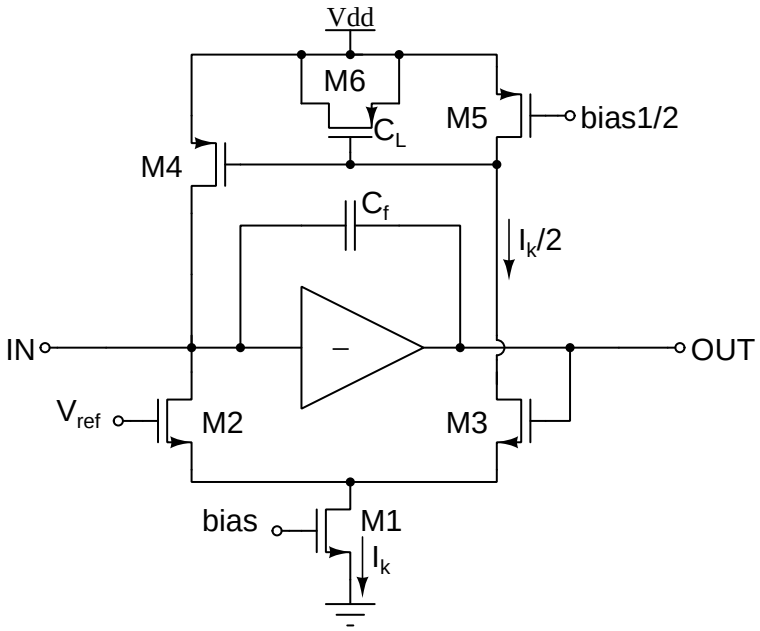


Input current pulse **Amplifier output** **Discriminator output**

Charge Sensitive Amplifier (CSA)



	G_c $[\frac{mV}{fC}]$	T_{pk} $[ns]$
65 nm	107	16.3
28 nm	121	9.5

- **CSA**:
  - Output **voltage amplitude** $\propto$ **input charge**
  - Constant peaking and falling times $\rightarrow$ **good timing performance**
  - **Low noise**
- **Krummenacher Filter**:
  - Active feedback path $\rightarrow$ pulse shape
  - **DC current compensation** $\rightarrow$ **input leakage current**
  - DC voltage setting $\rightarrow$ full range exploitation
  - **50 nA** total current $\rightarrow$ small power consumption impact

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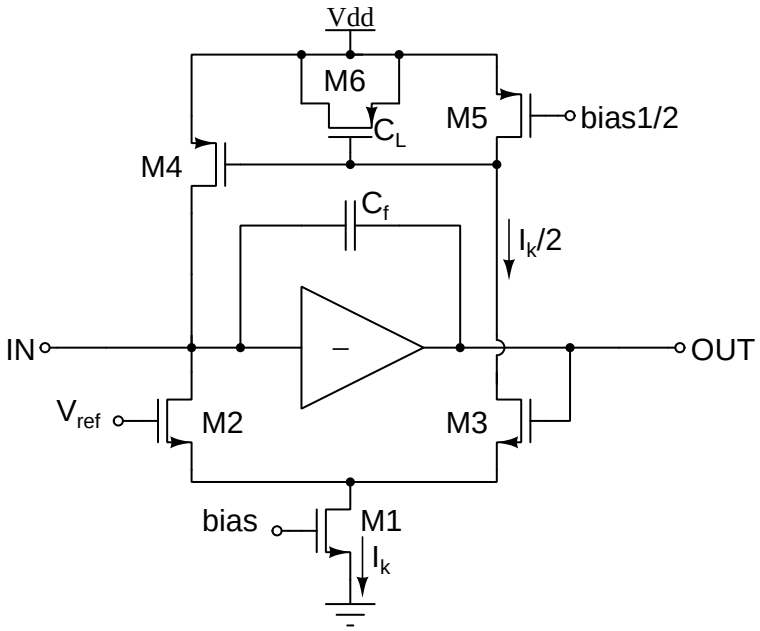

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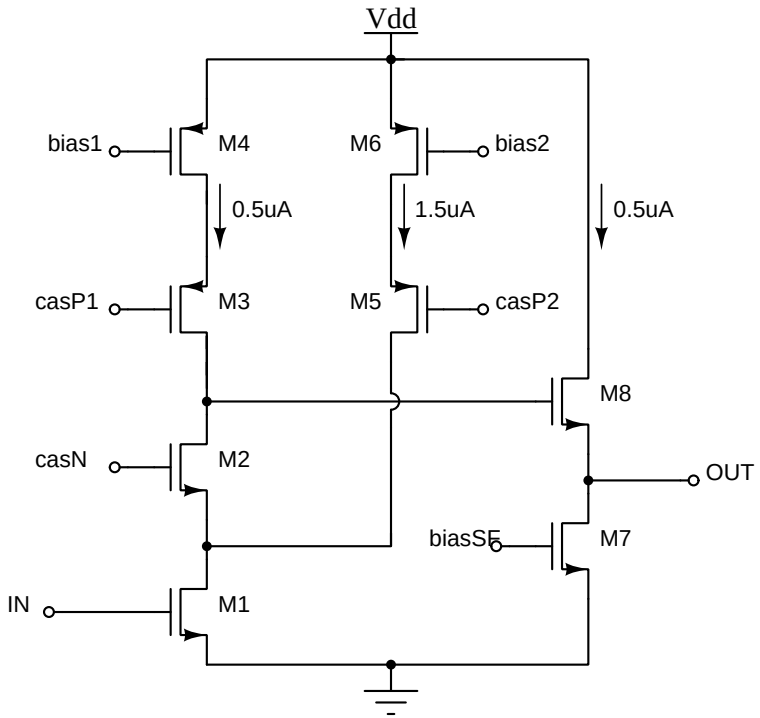

	A_0 $[dB]$	BW $[MHz]$
65 nm	54.4	5.9
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- **Telescopic cascode amplifier** with split bias current branches
- Almost 60 dB gain
- Output buffer
- **$2.5\mu A$** estimated total current $\rightarrow$ low power consumption

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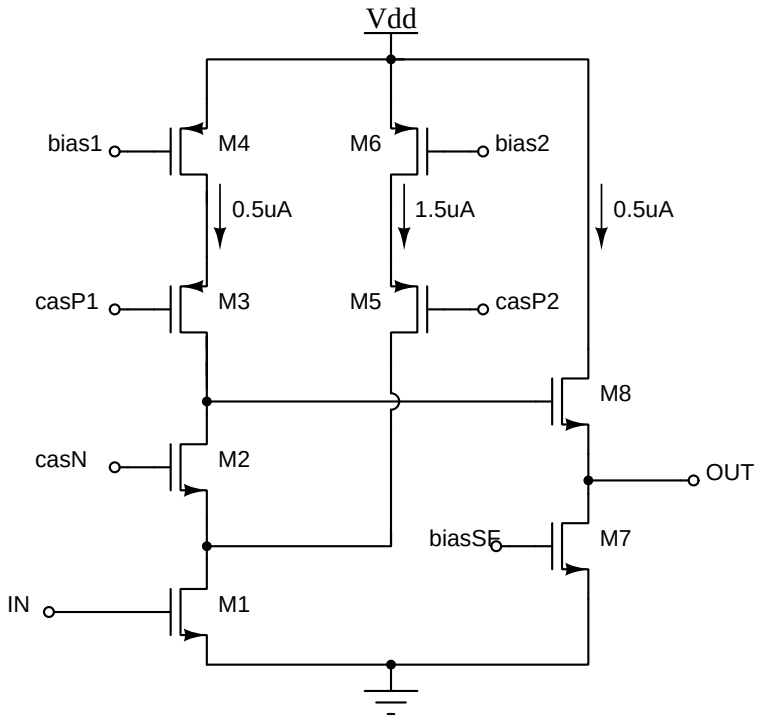

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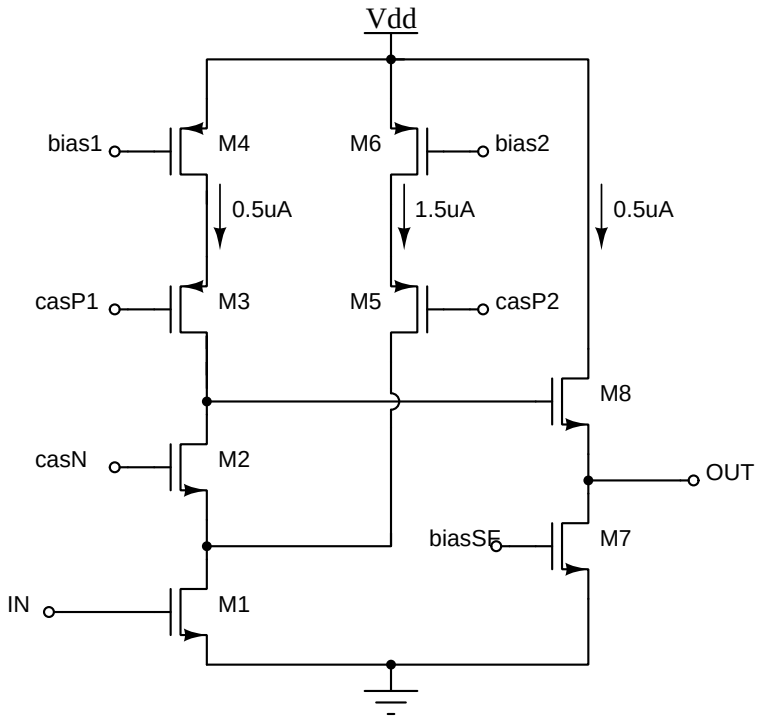

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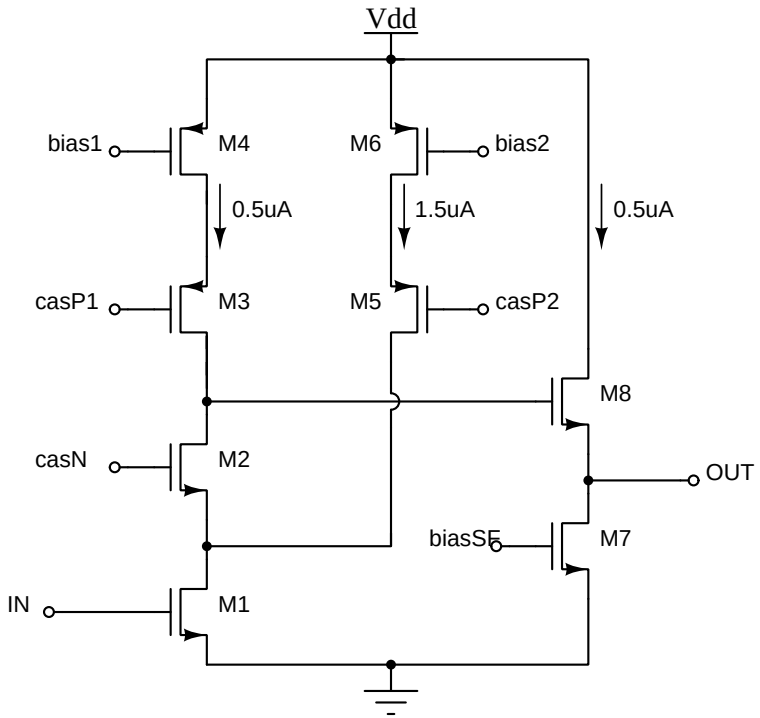

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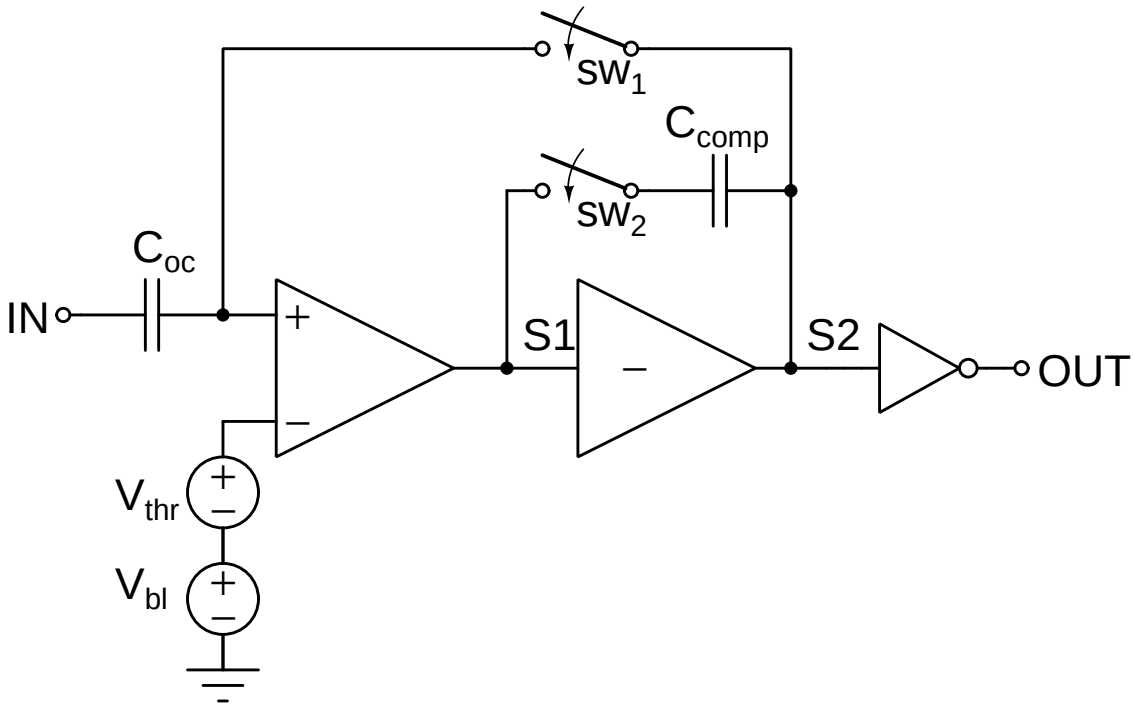

- **2 stage** amplification
- Inverter → **digital output buffer**
- **Offset Correction Circuit**: store offset variability inside C_{oc}
  - **correct intra-channels variability**
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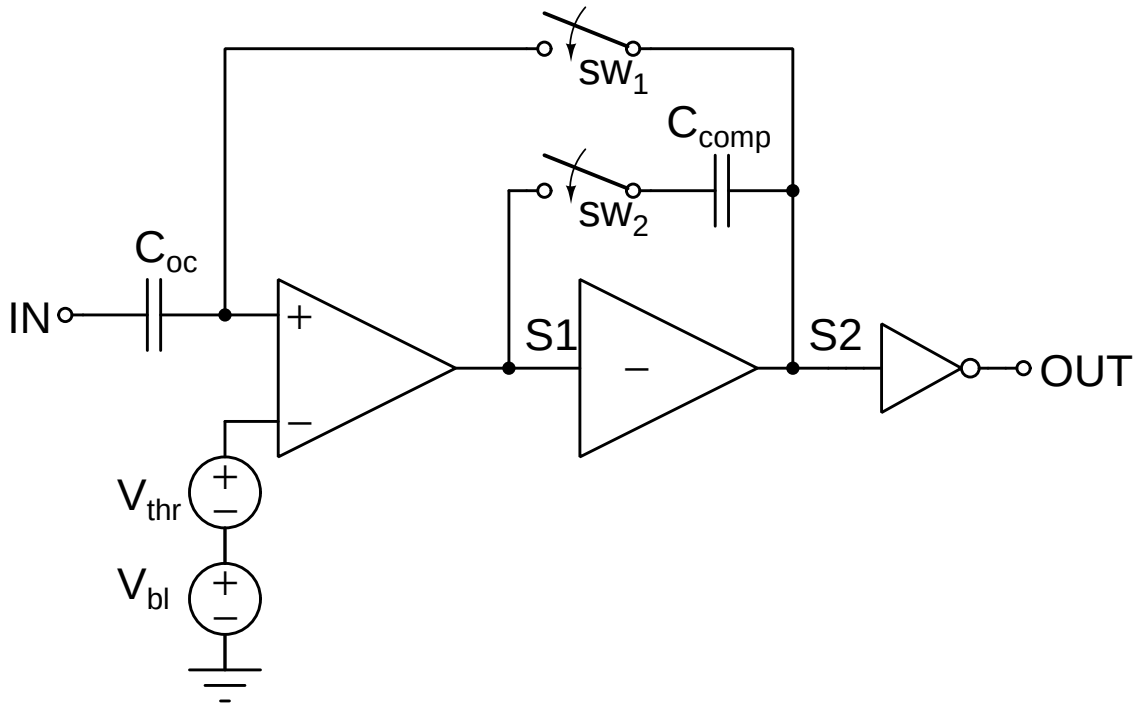

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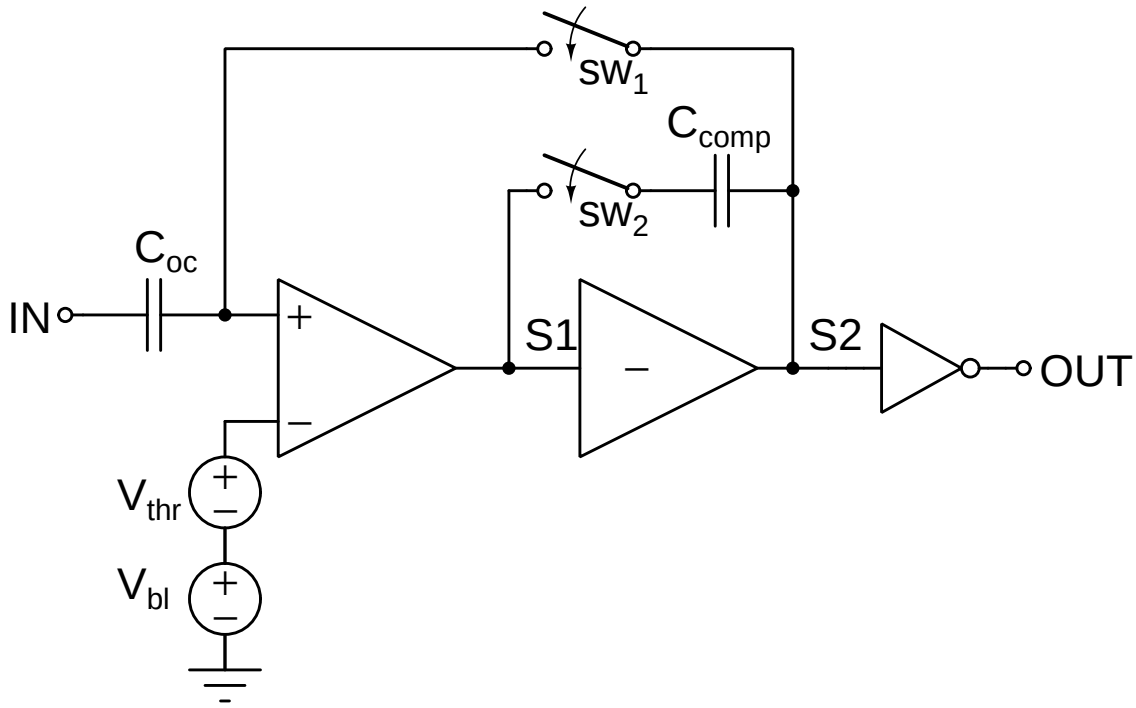

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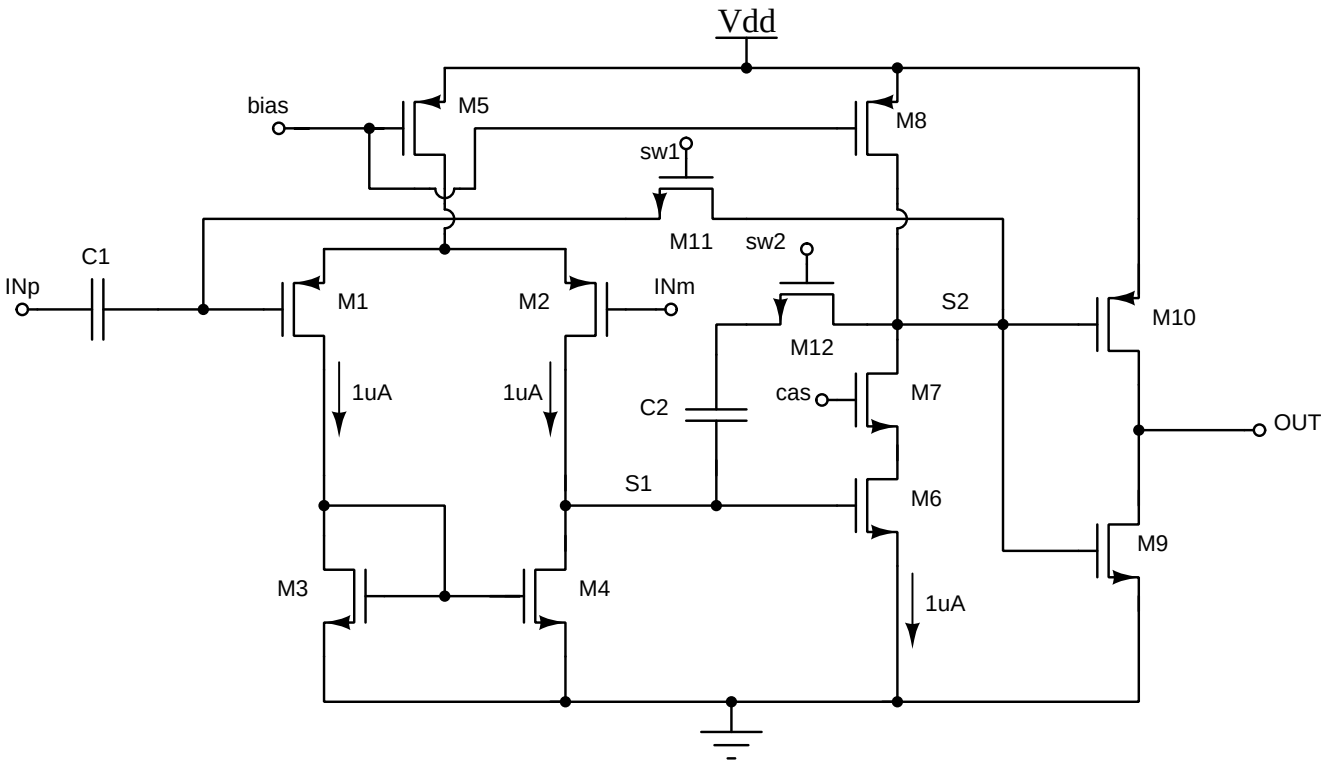

	A_0 [dB]	BW [MHz]
S_1	24.2	56.3
S_2	34.0	13.1
total	58.2	13.3

- 1^{st} stage: **low gain, differential**
- 2^{st} stage: **high gain**, single ended
- $t_d \sim 5ns$ average delay time
- **3** μA total current

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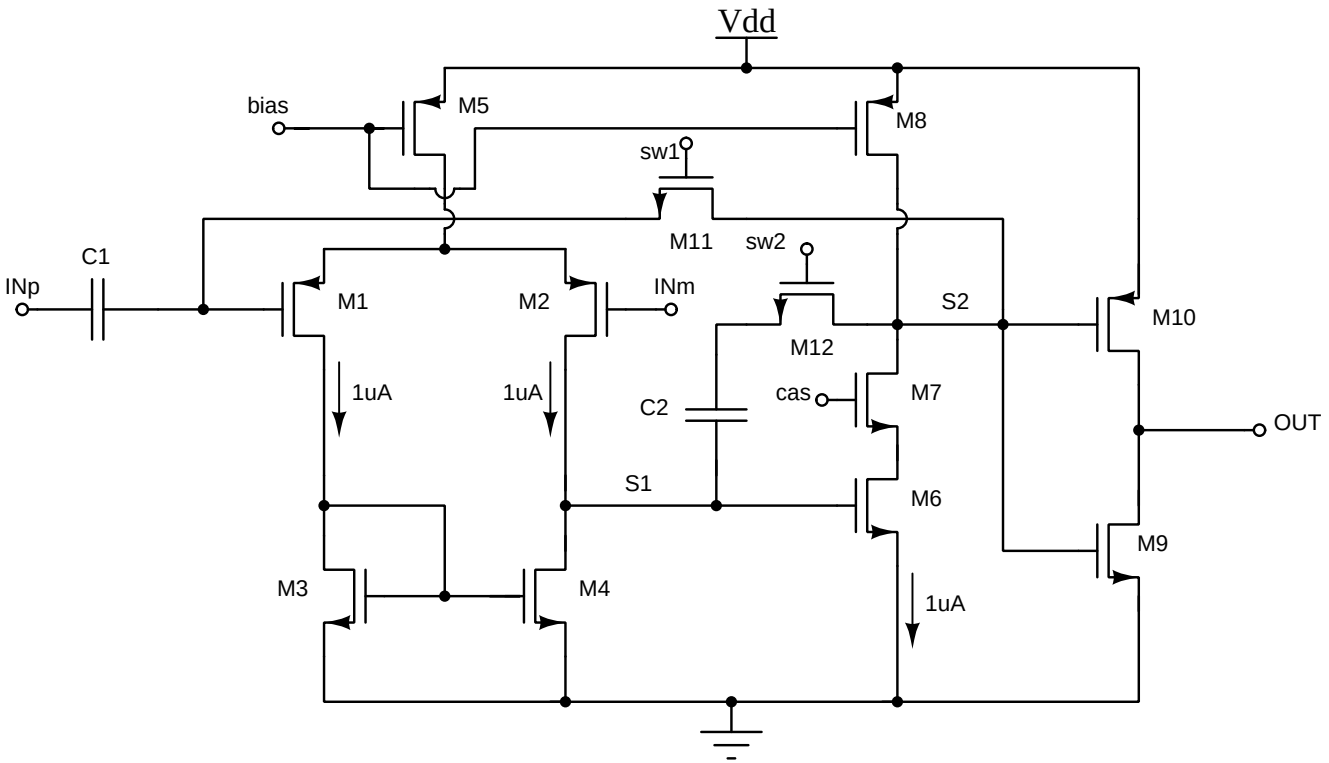

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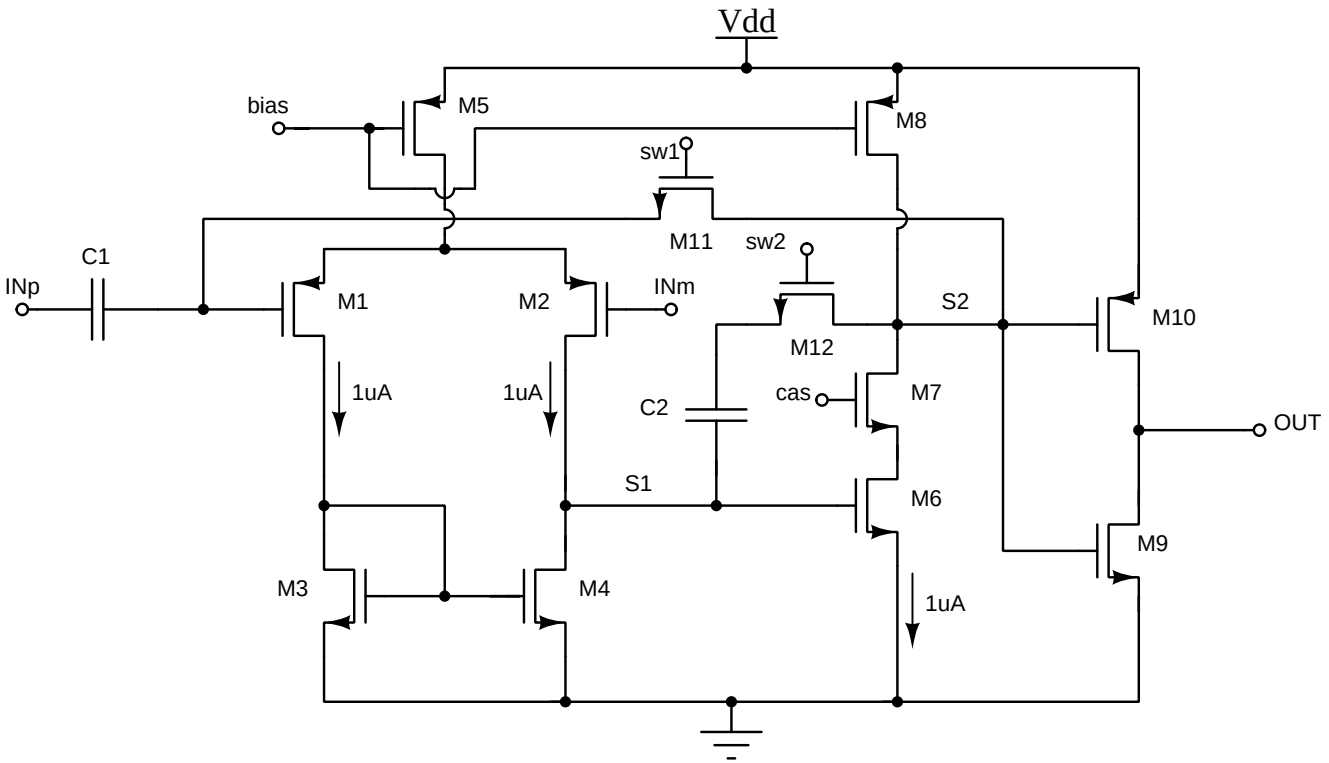

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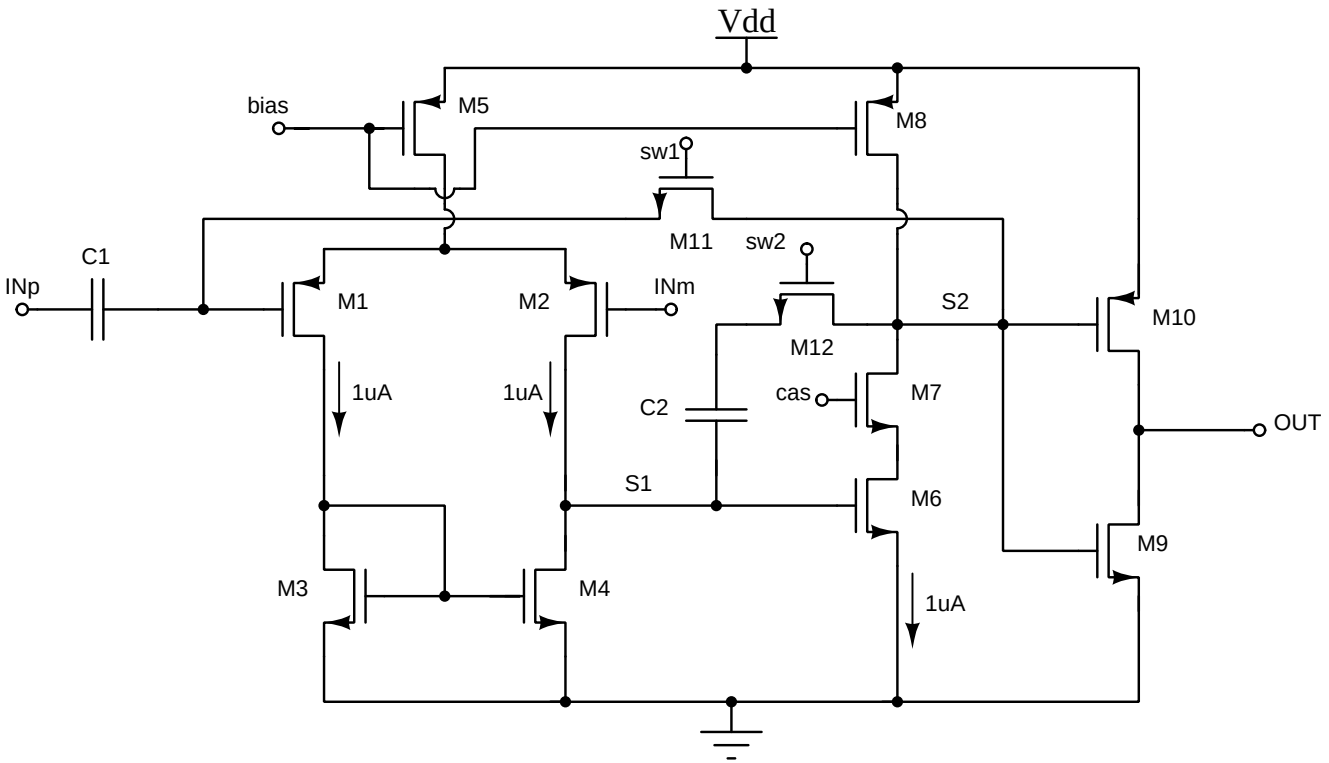

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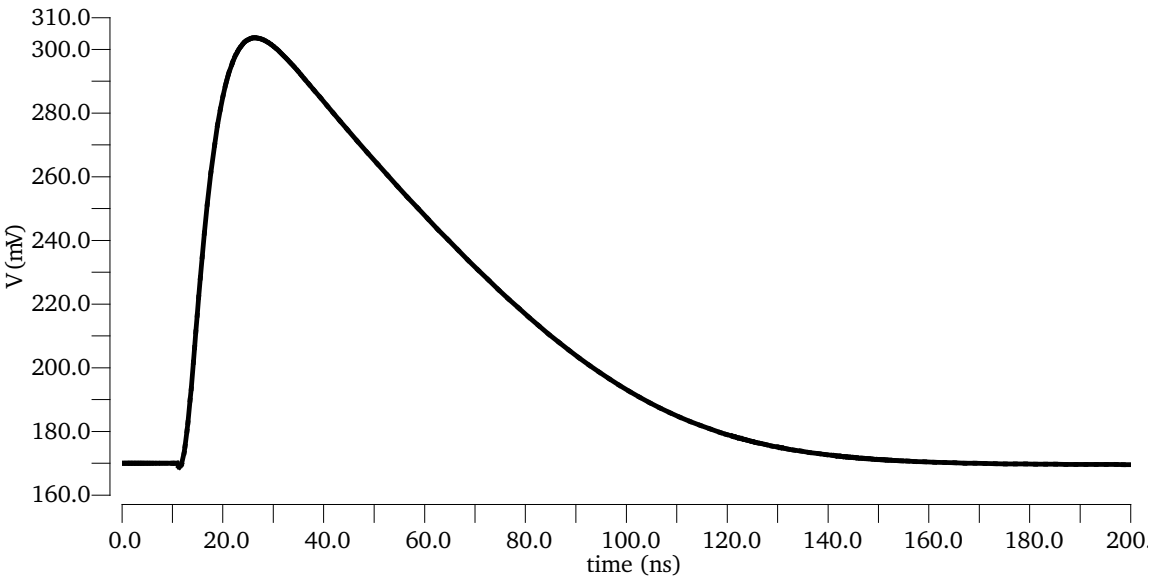
Outline

Passage to the 28nm Design



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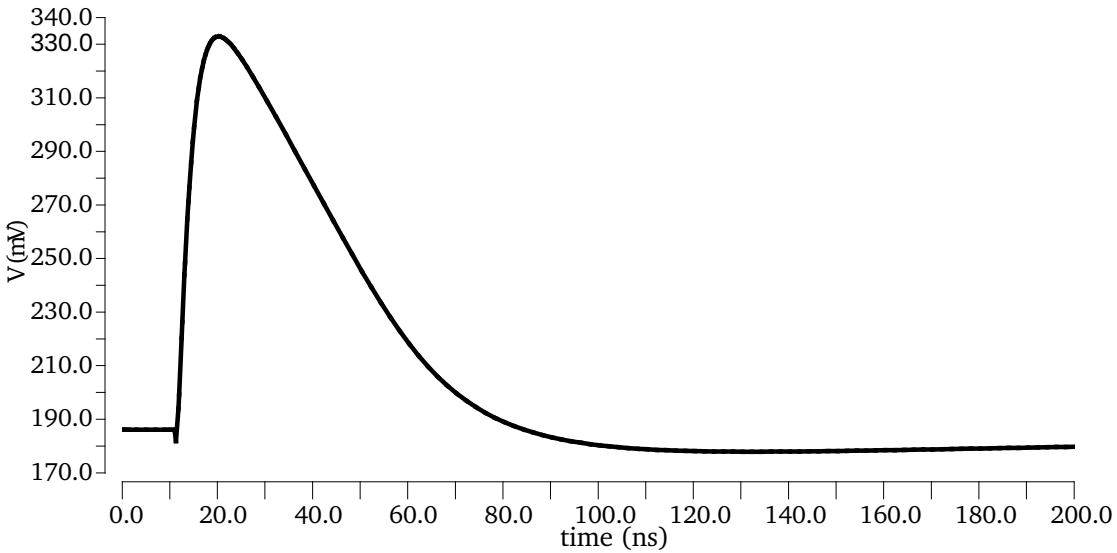

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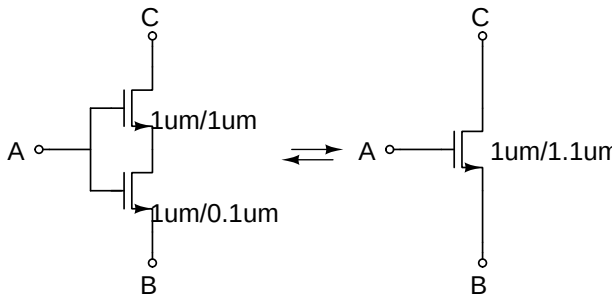

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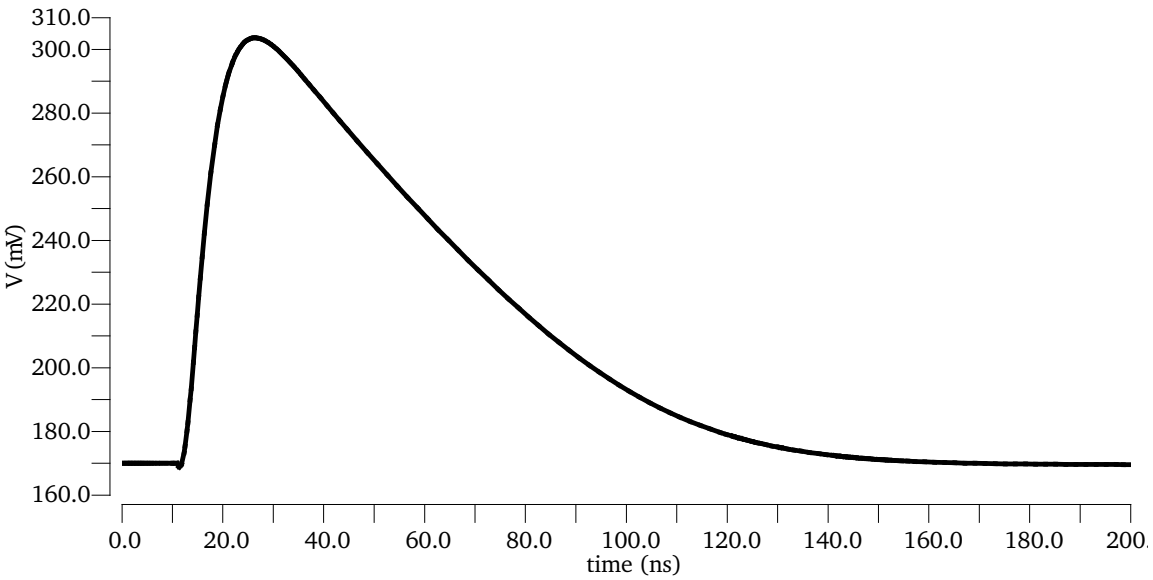

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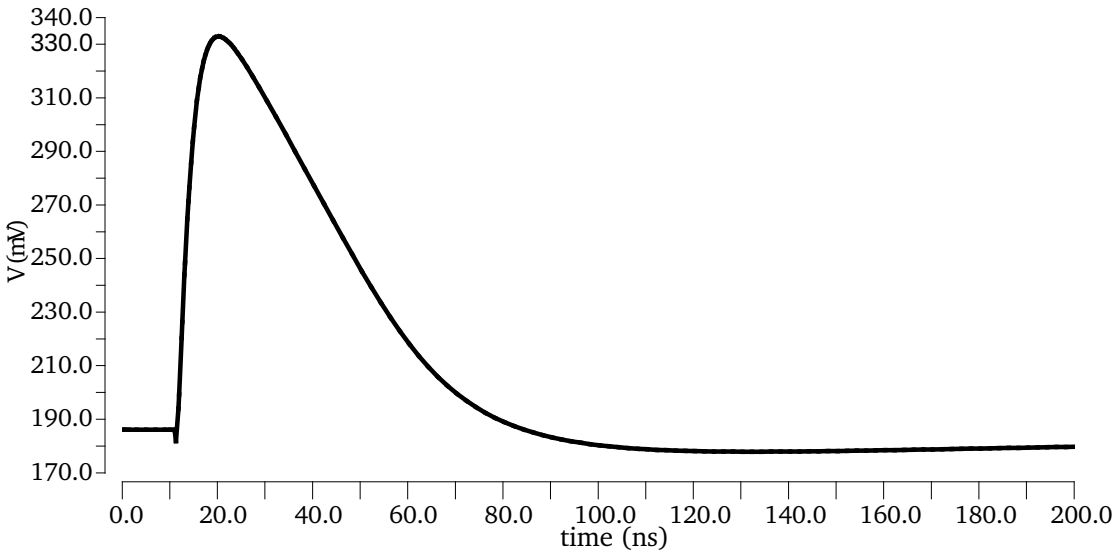

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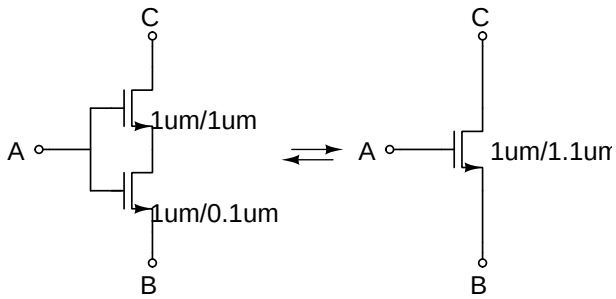

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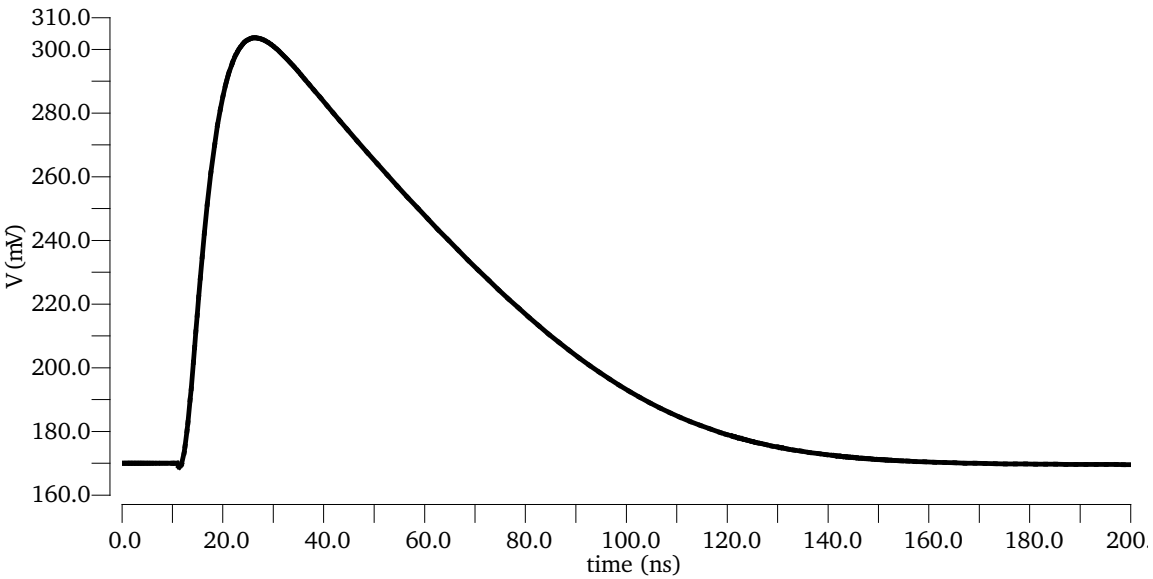

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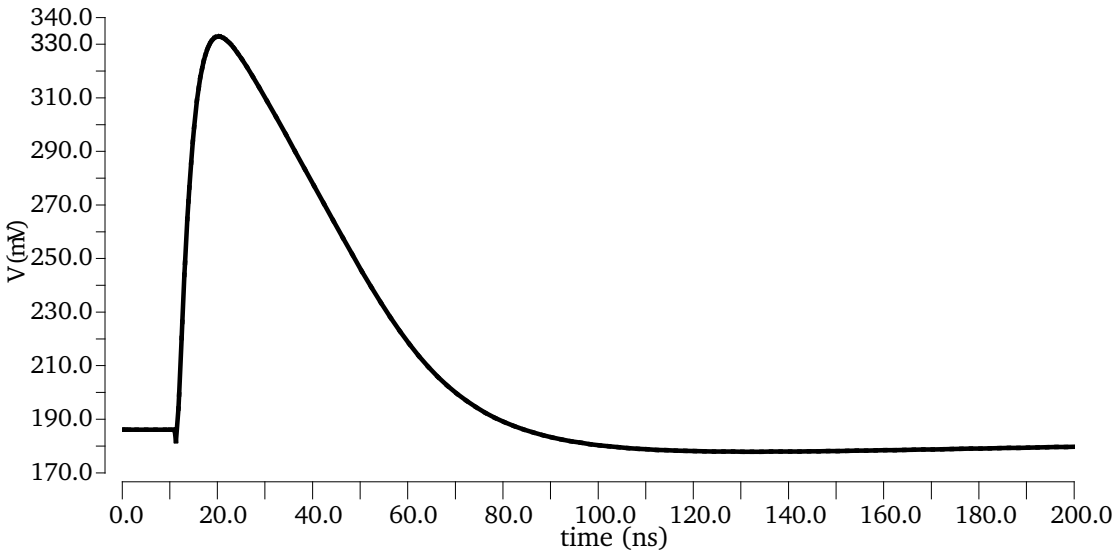

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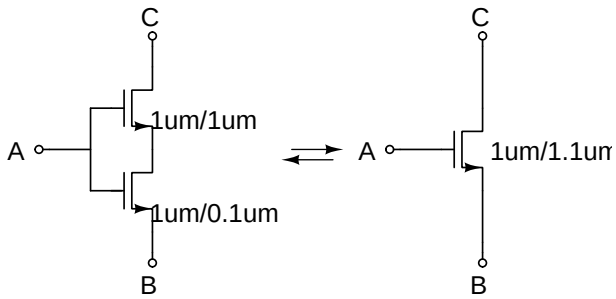

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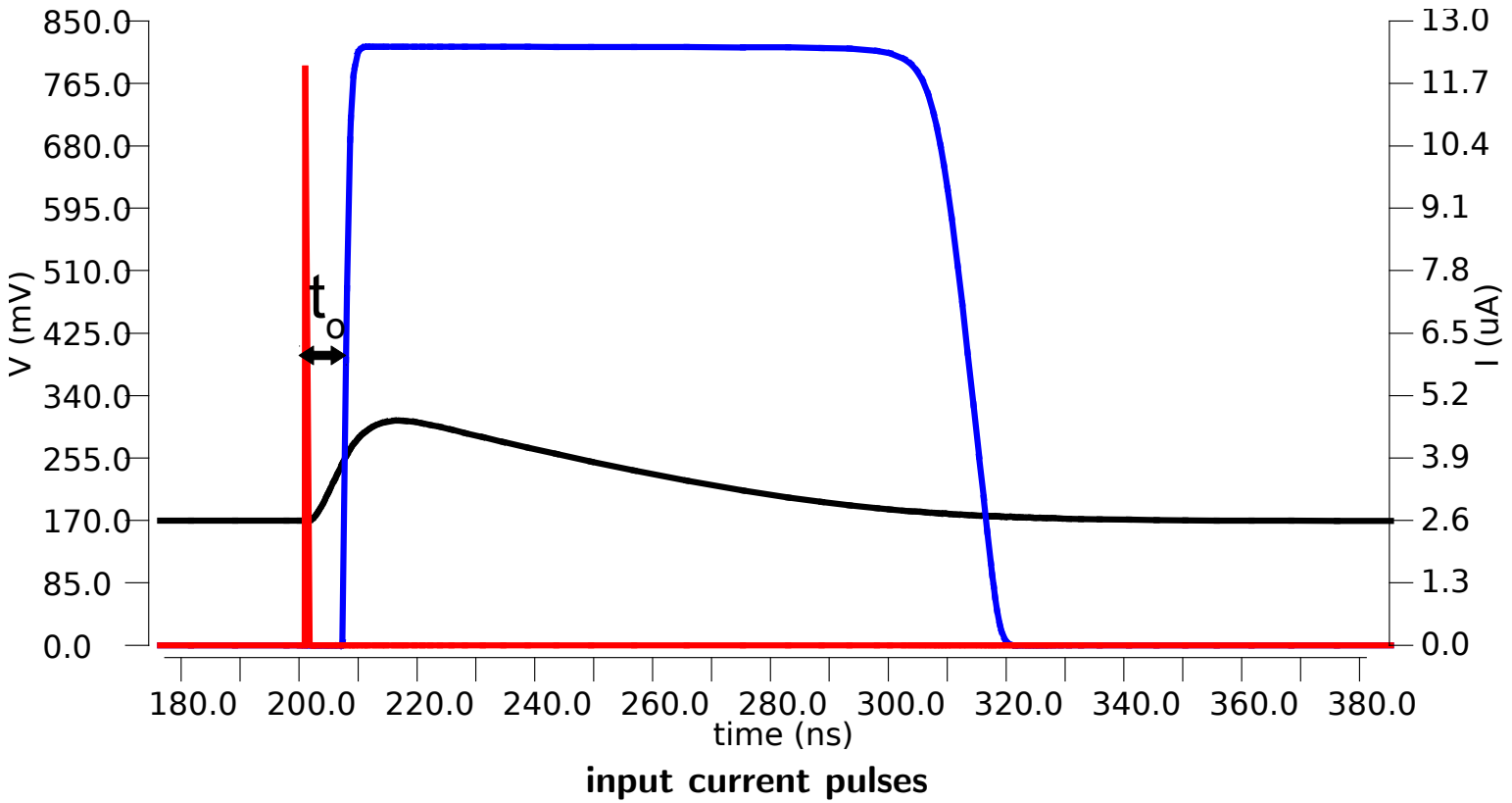

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- Setup: 1.2 fC input charge, $V_{thr} = 10$ mV, discriminator baseline 200 mV

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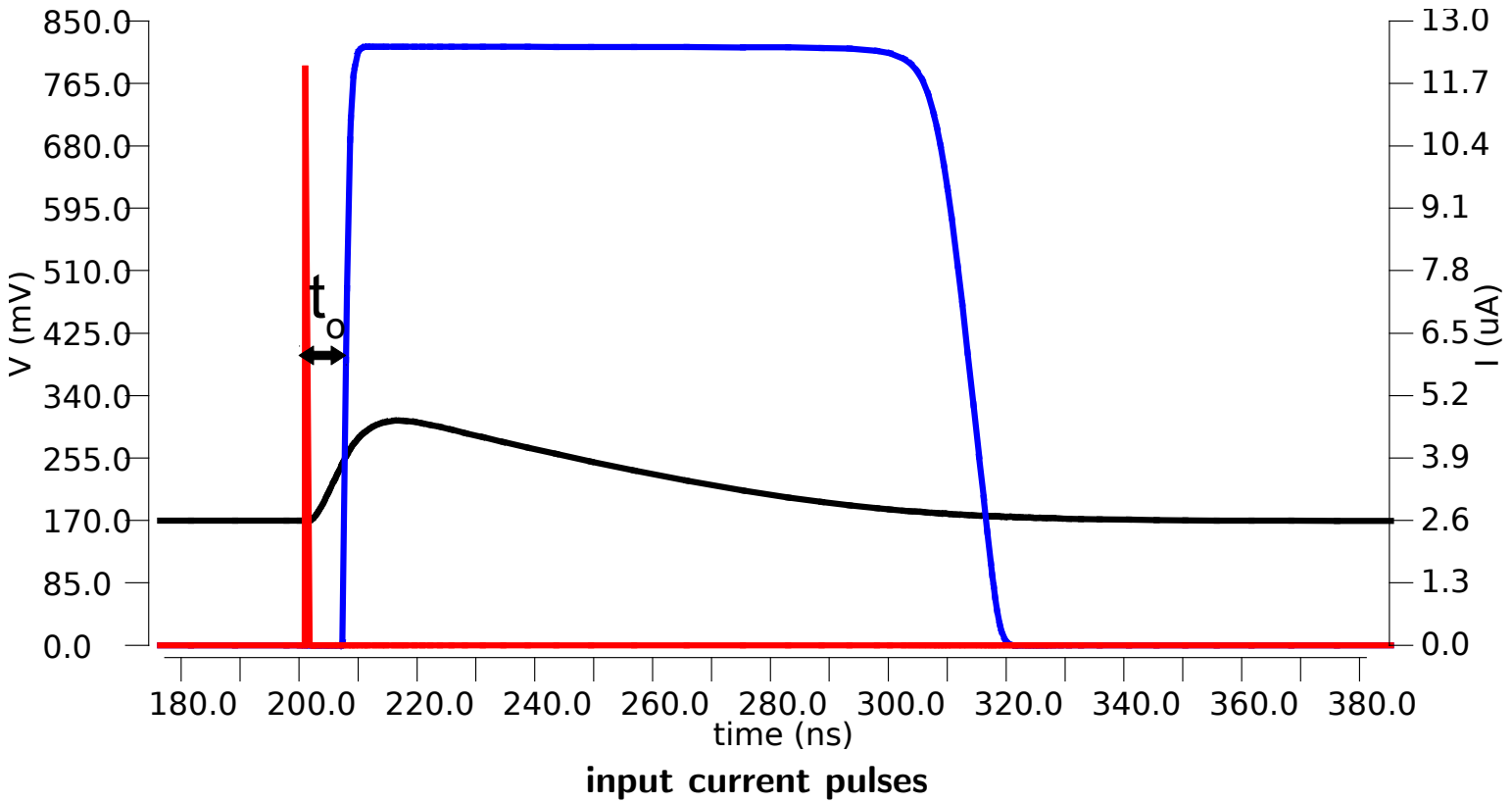

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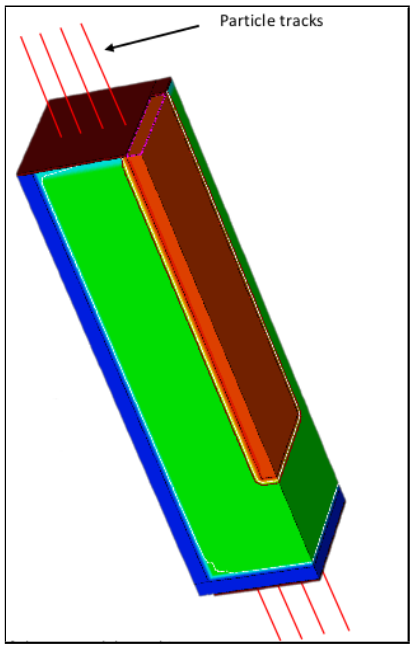

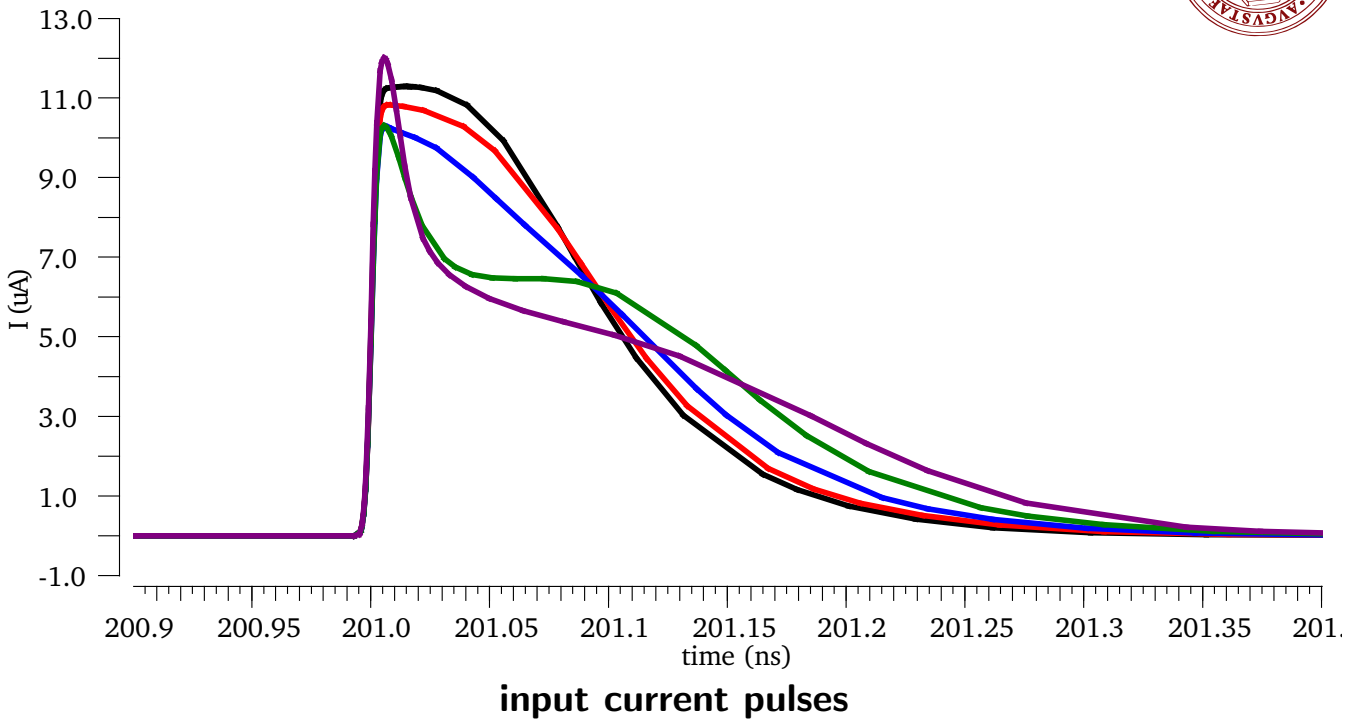

input current pulses

- Current pulses: **simulations** of 1.2 fC charge linear development in the **3D Si** model (by **INFN Cagliari** using Synoposis-TCAD tool)
- 5 **different positions** $\rightarrow \Delta_{sv} =\sim$ **34 ps**

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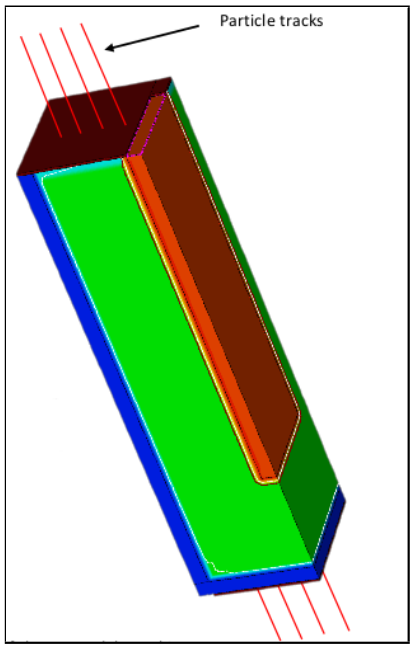

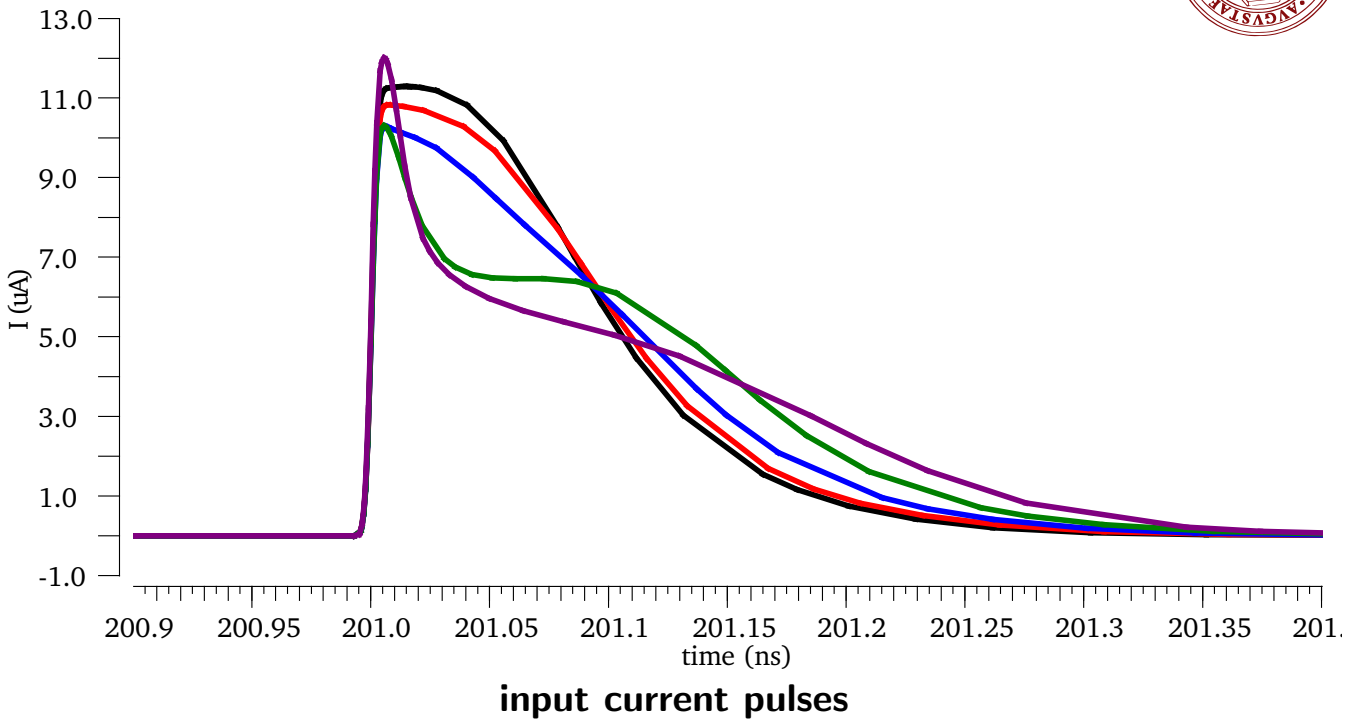

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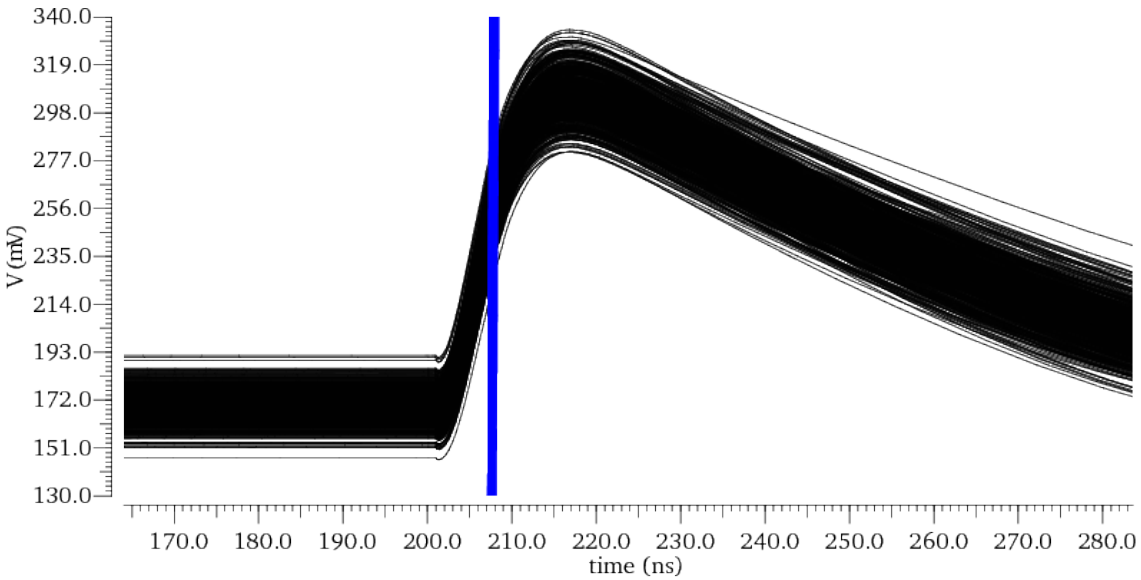
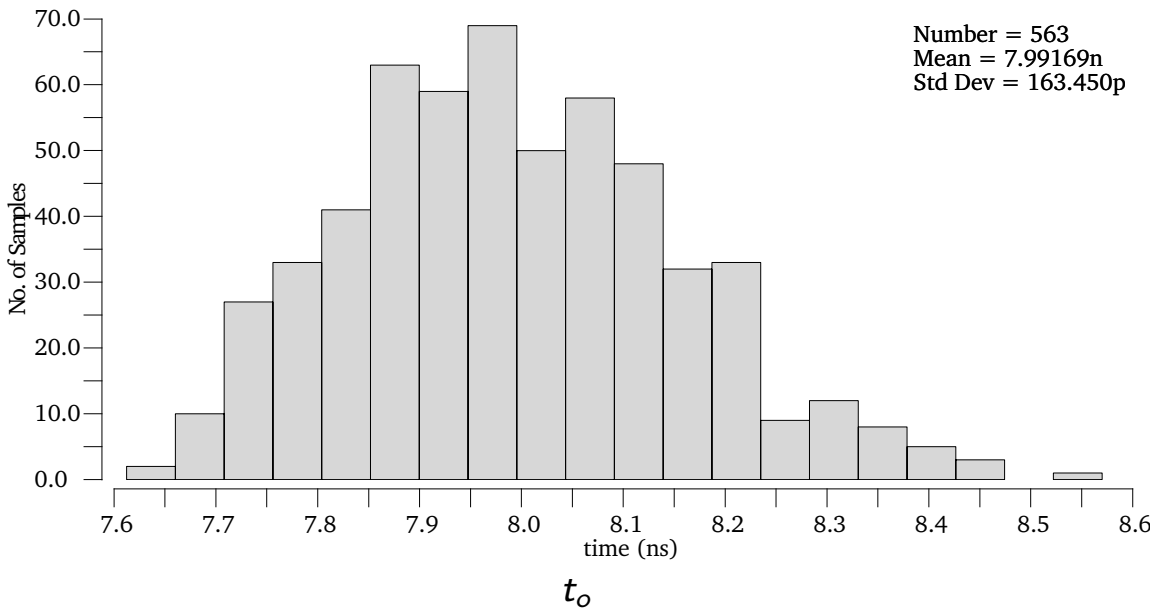


Amplifier output **Discriminator output**



t_o

- t_o variation due to systematic **large distance process variability**
- Main effect on baseline $\rightarrow$ offset correction ($\times 5$ improvement)
- $\sigma_p = 163ps \rightarrow$ **per-chip calibration**

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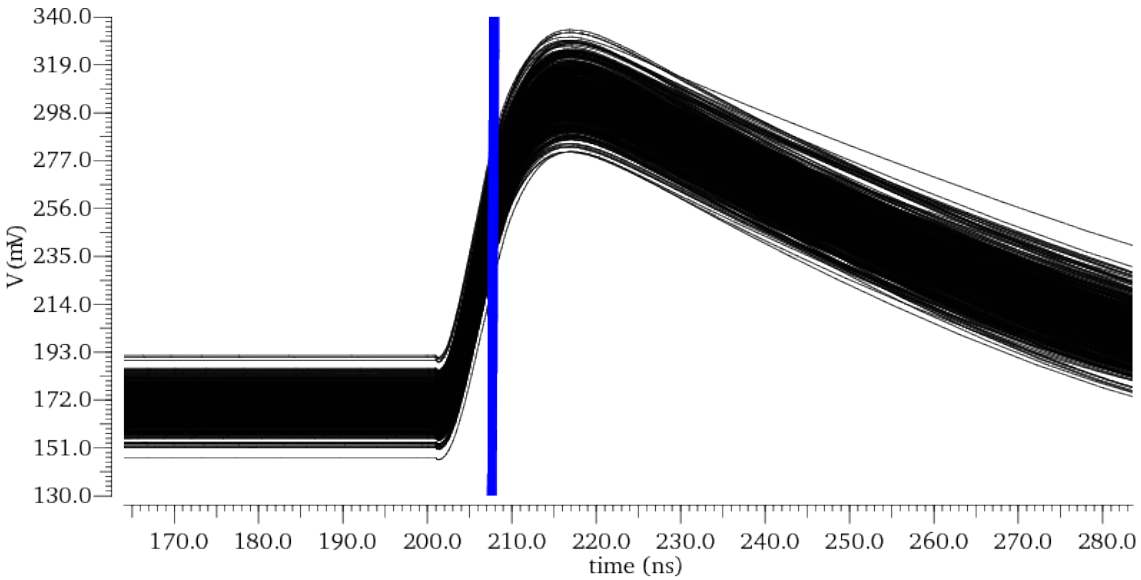

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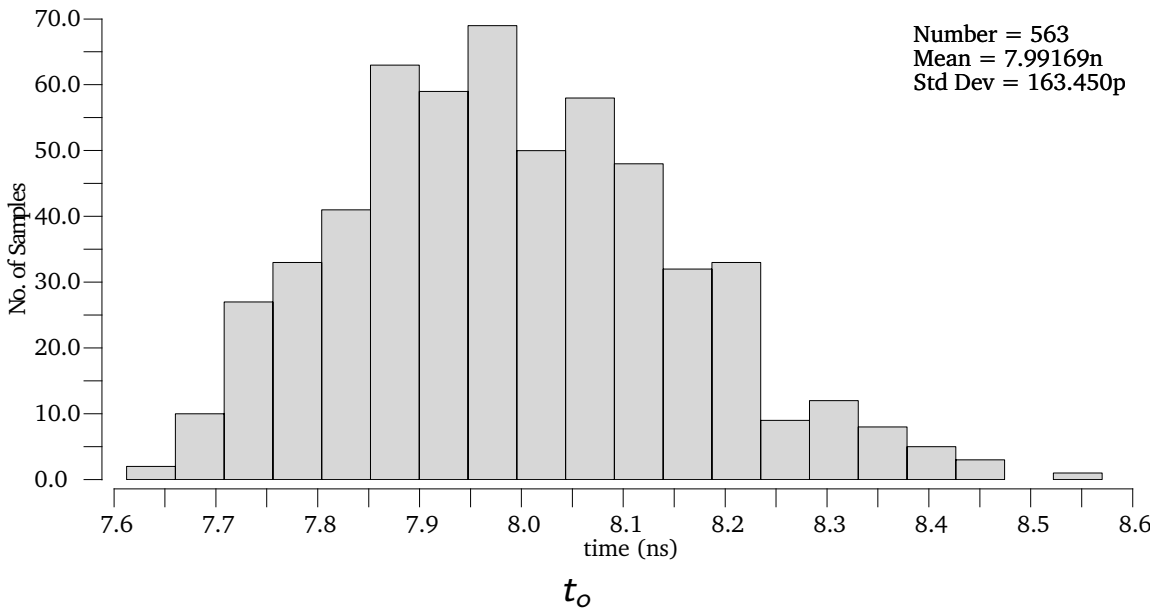

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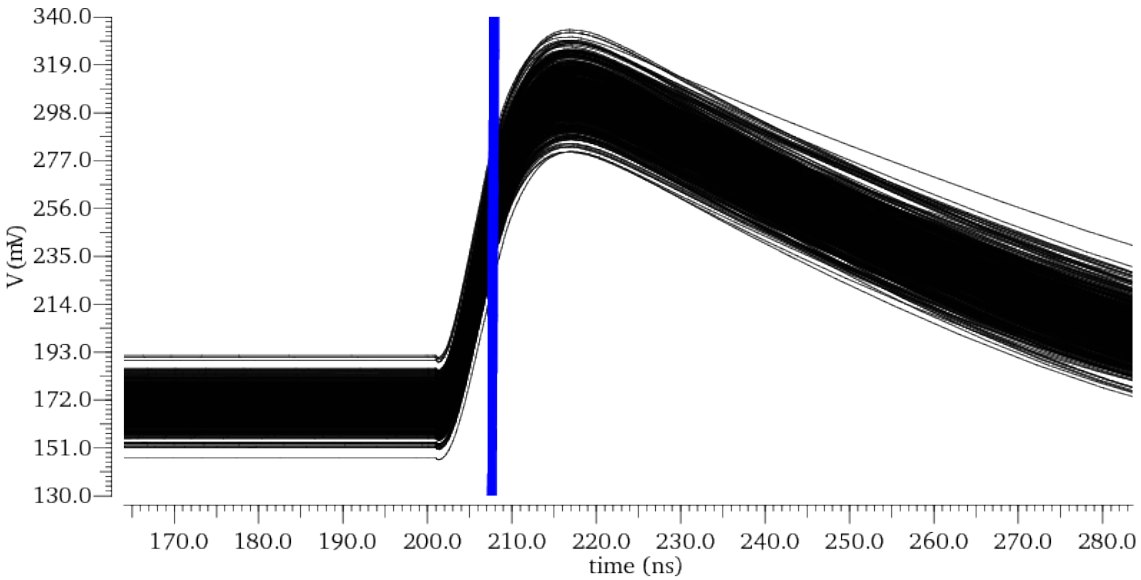

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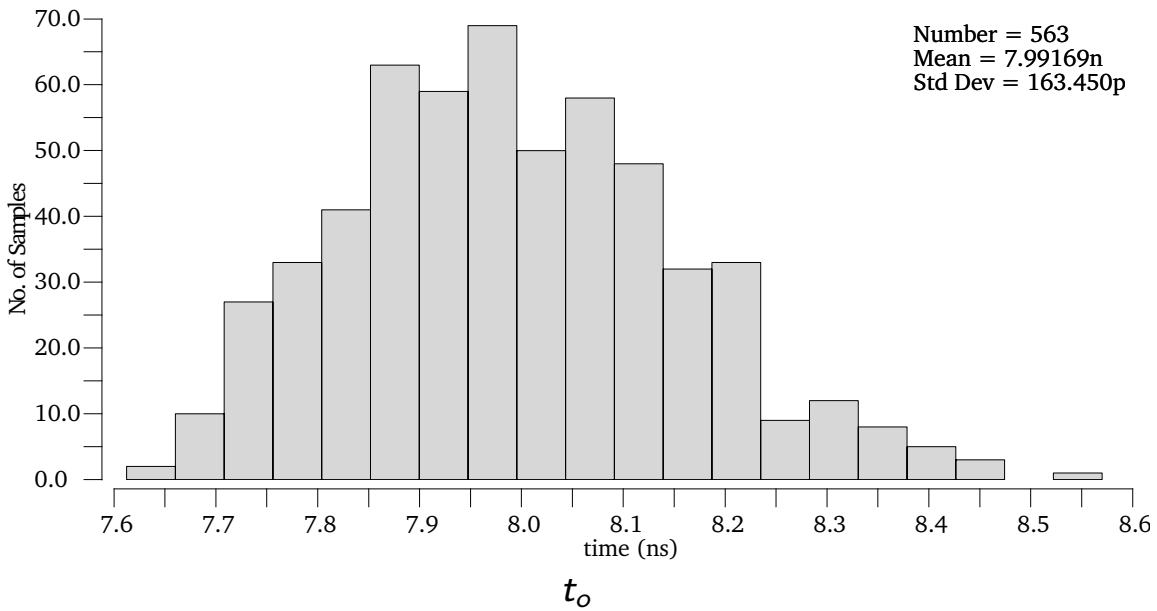

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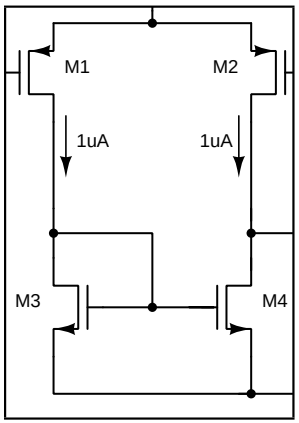

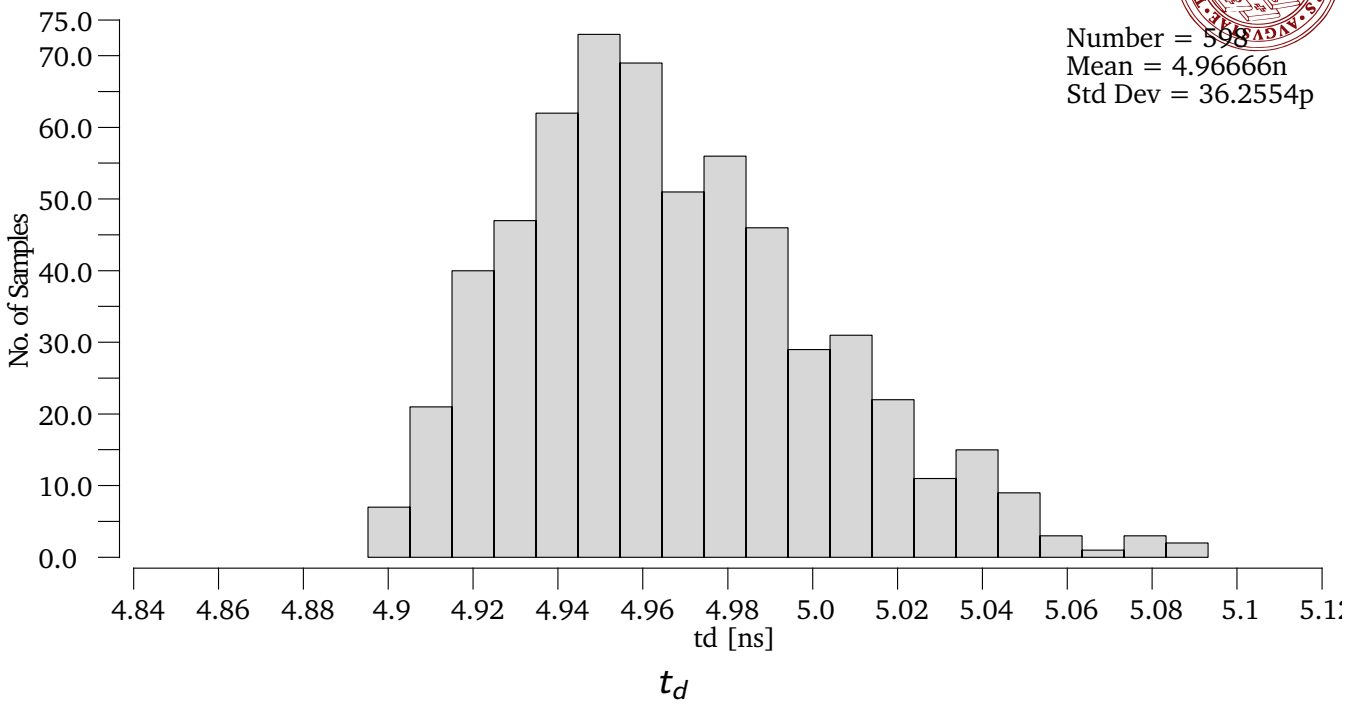

t_d

- Variation due to **nearby transistors variabilities**
- Studied on discriminator **differential cell** $\rightarrow$ **discriminator delay time** t_d
- $\sigma_{mm} = 36$ ps
- offset correction $\rightarrow$ $\times 20$ improvement

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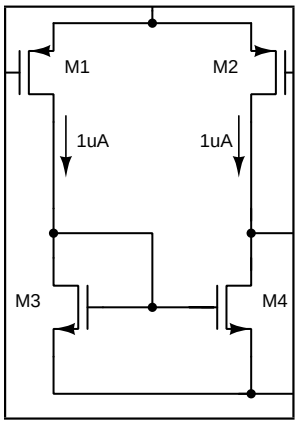

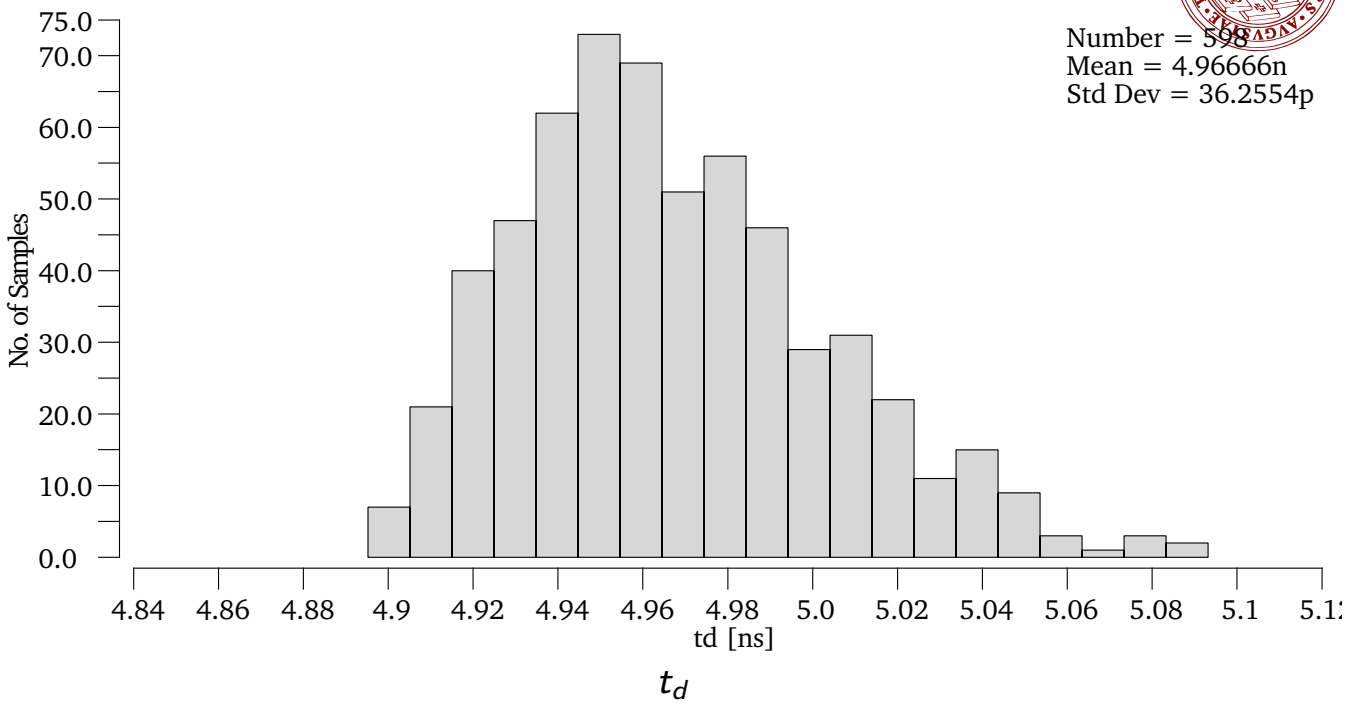

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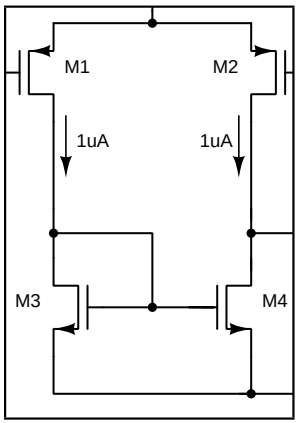

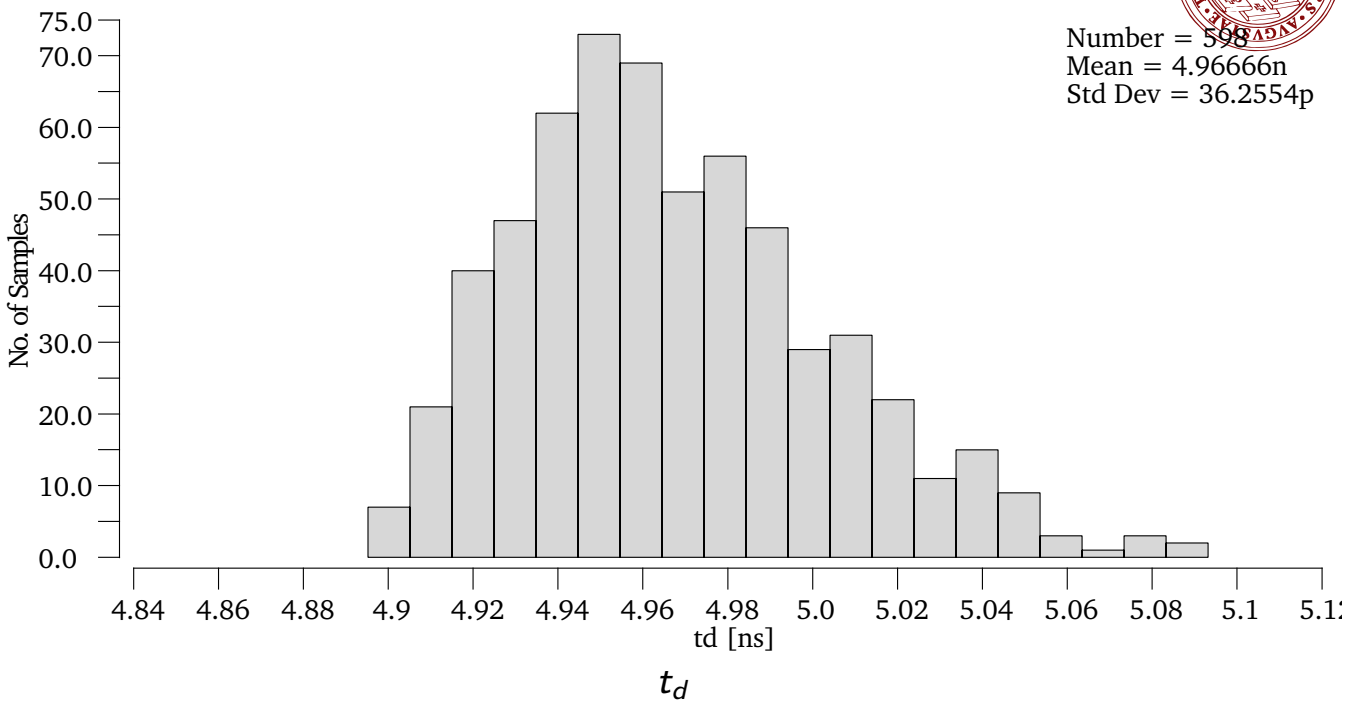

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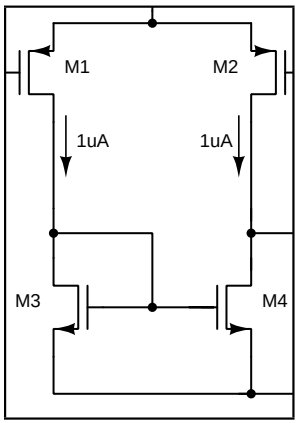
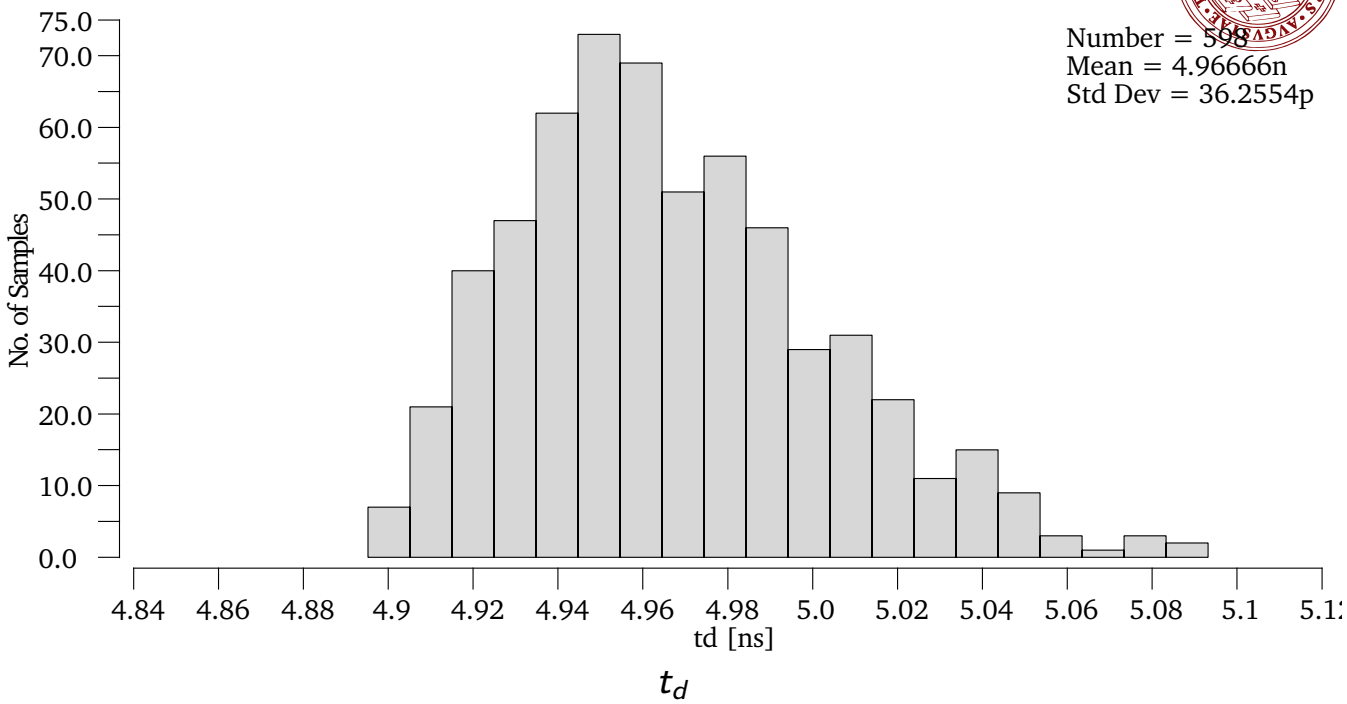
- $\sigma_{mm} = 36$ ps
- offset correction $\rightarrow$ $\times 20$ improvement

Mismatch Contribution





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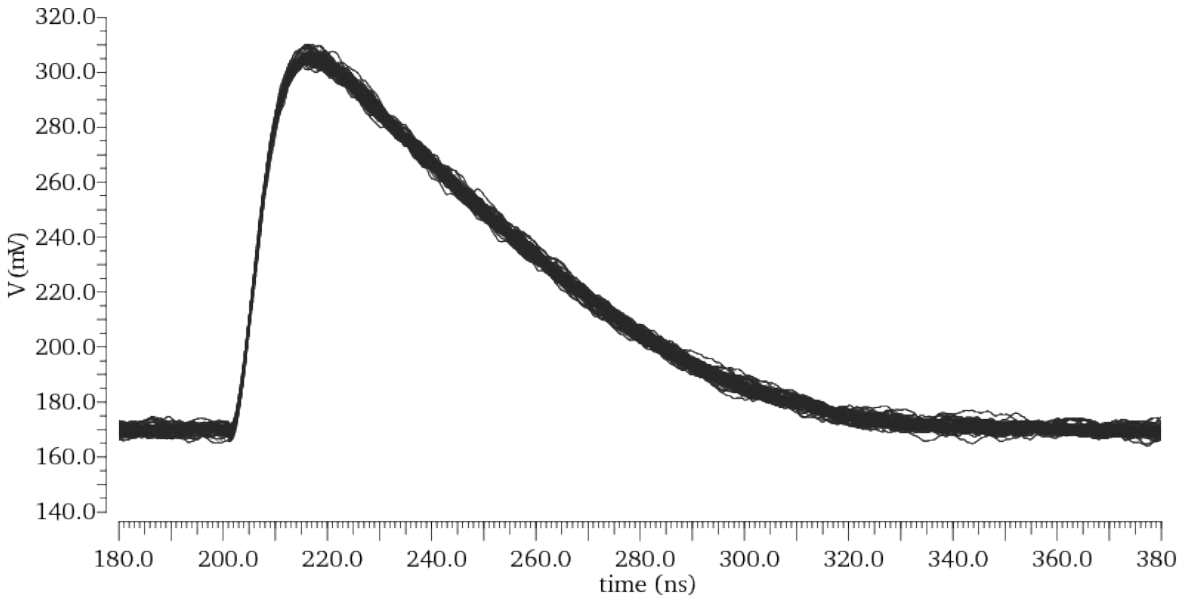
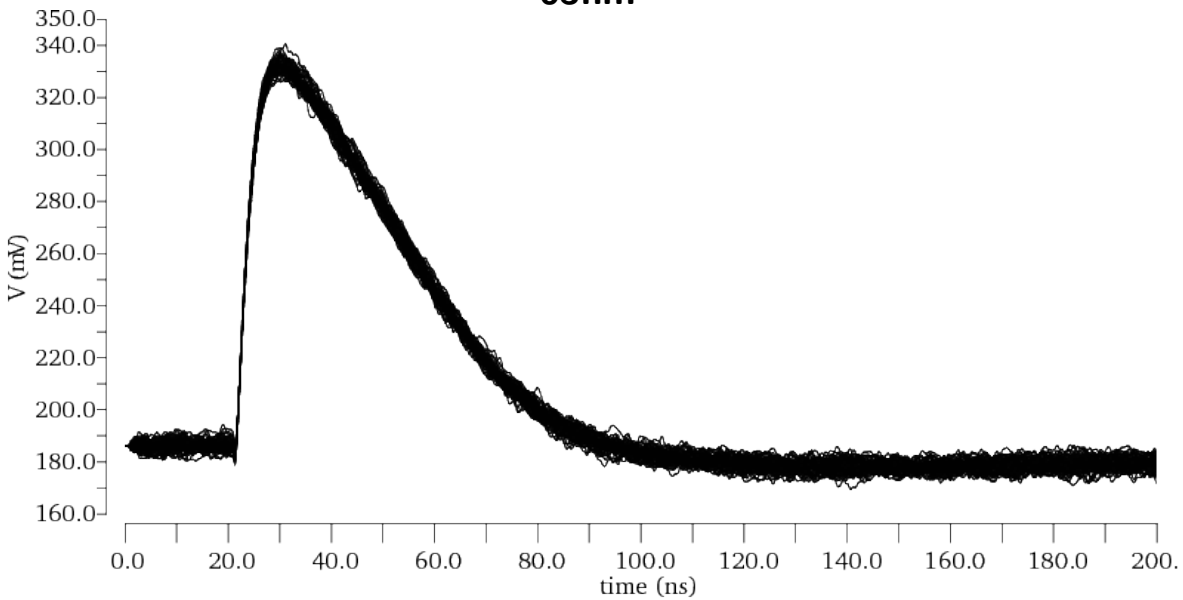


65nm



28nm

- **Noise induced jitter**: $\sigma_{tn} = \frac{SNR}{T_{pk}}$
- In 28 nm, for low range signals: SNR $\sim$ 14.5,
- Simulated $\sigma_{tn} \sim 100$ ps RMS
- **Optimization needed**

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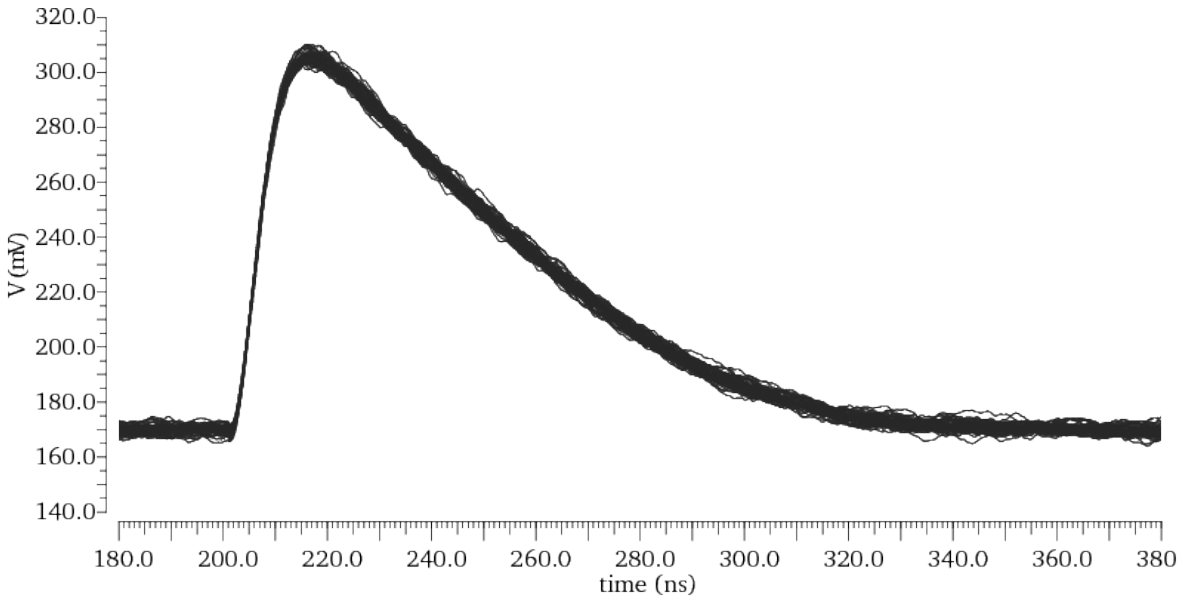

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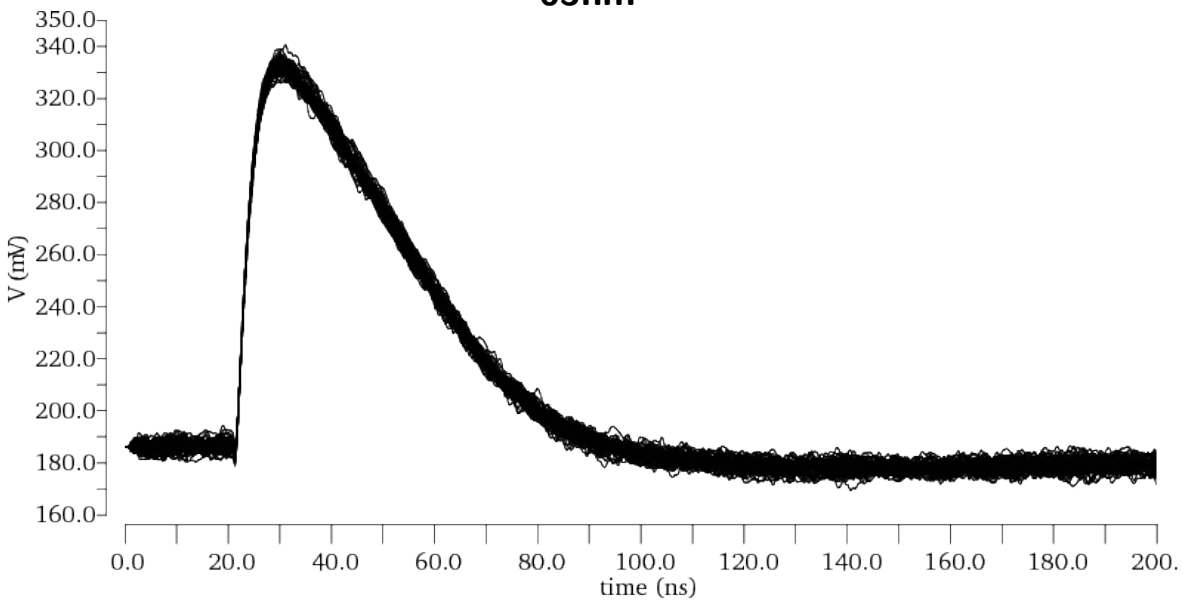

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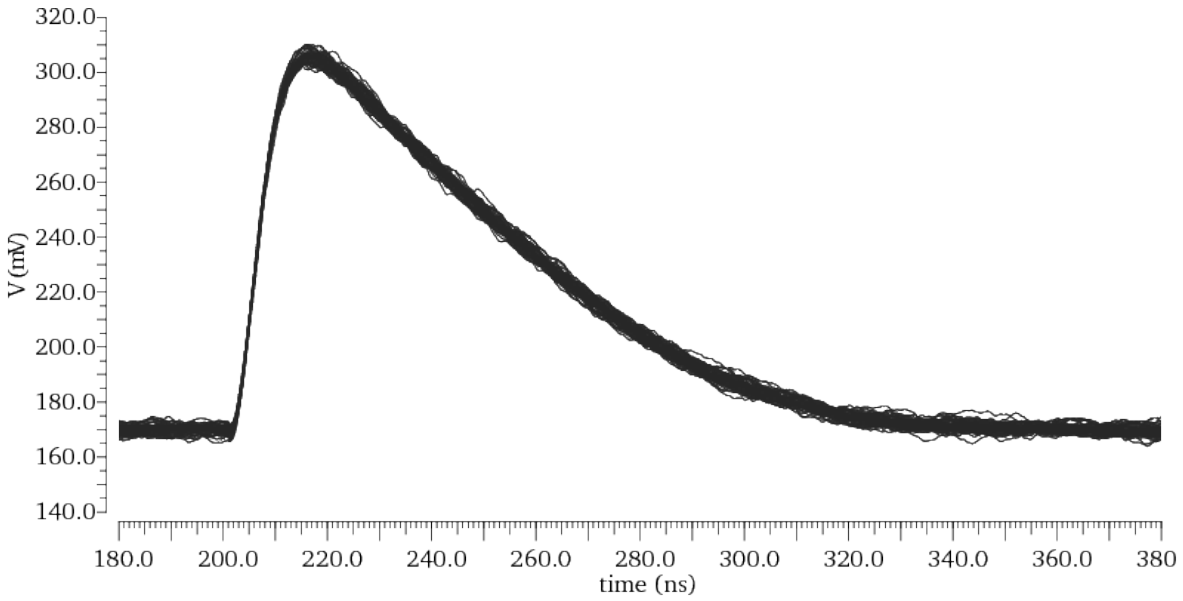

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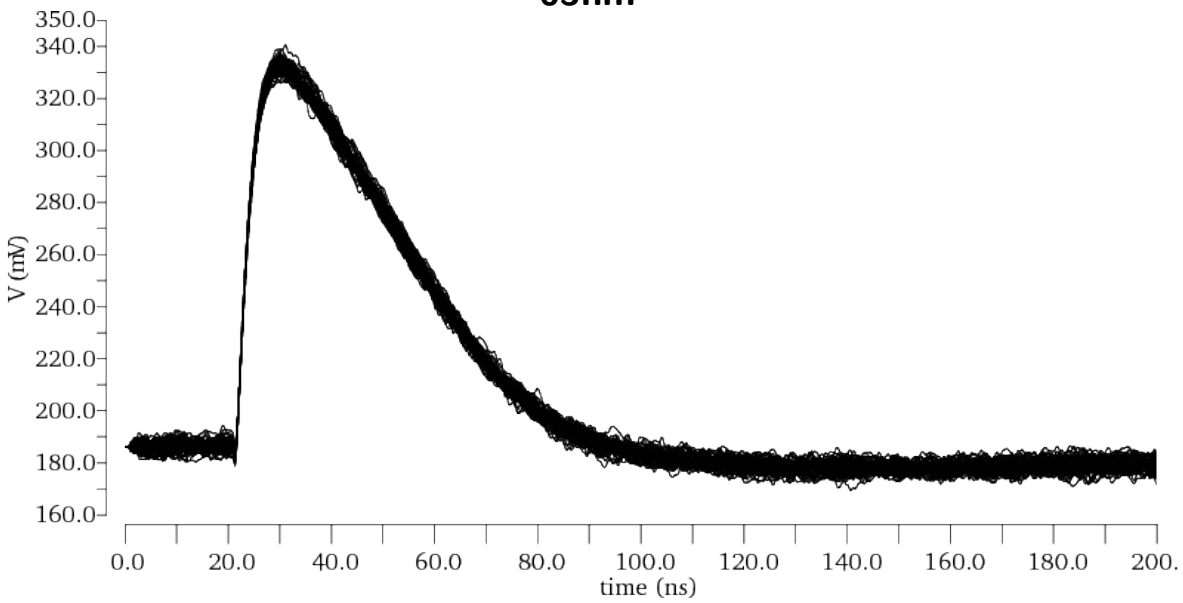

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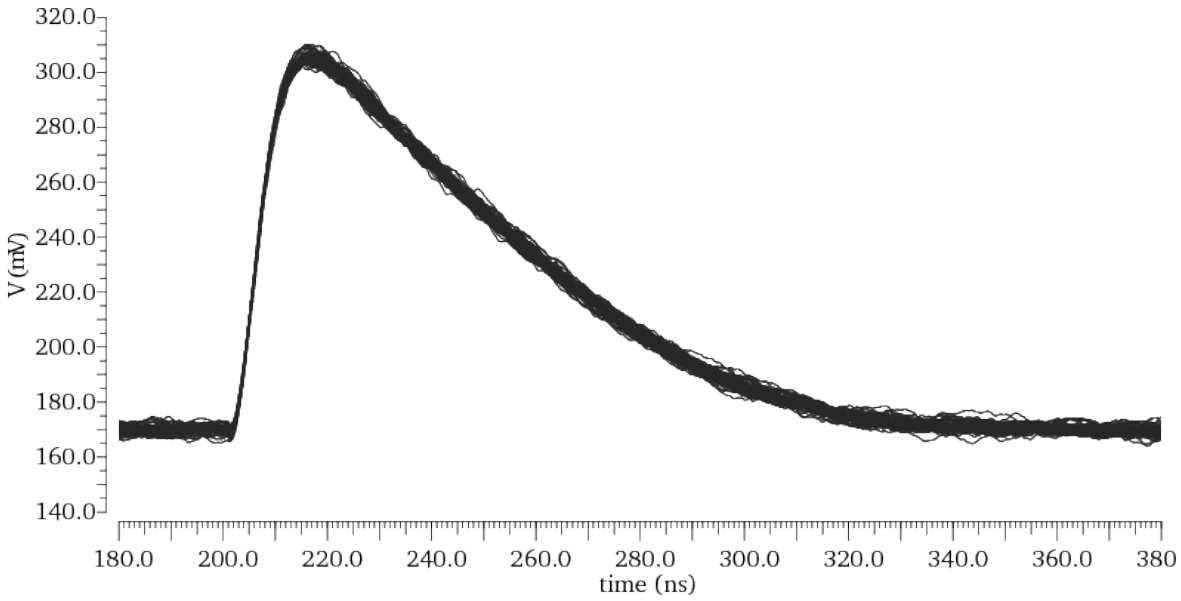

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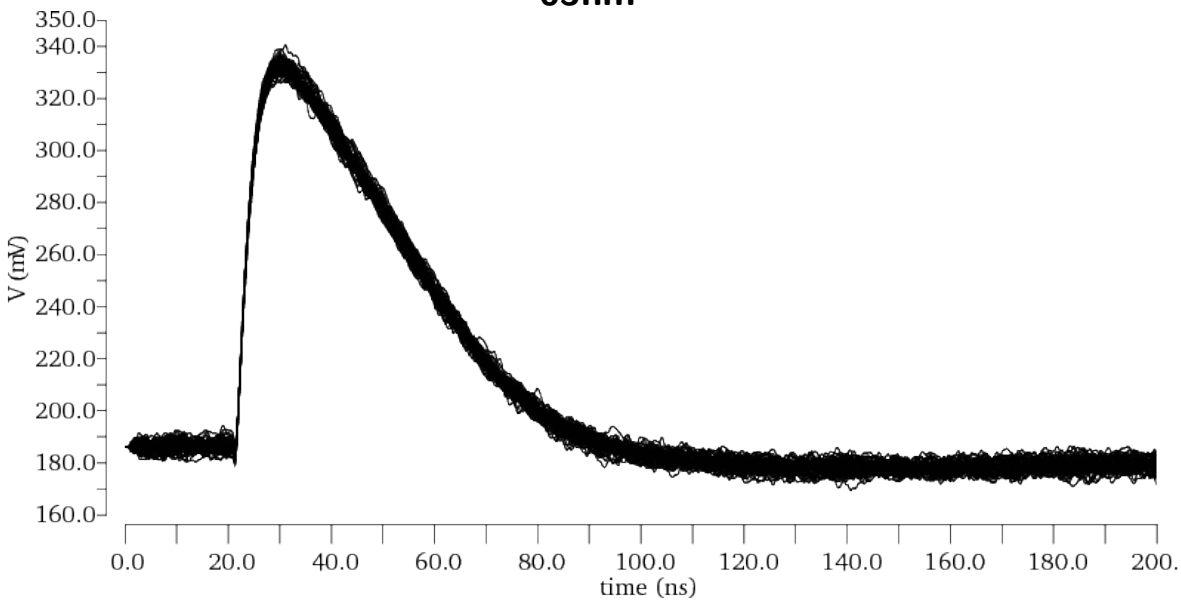

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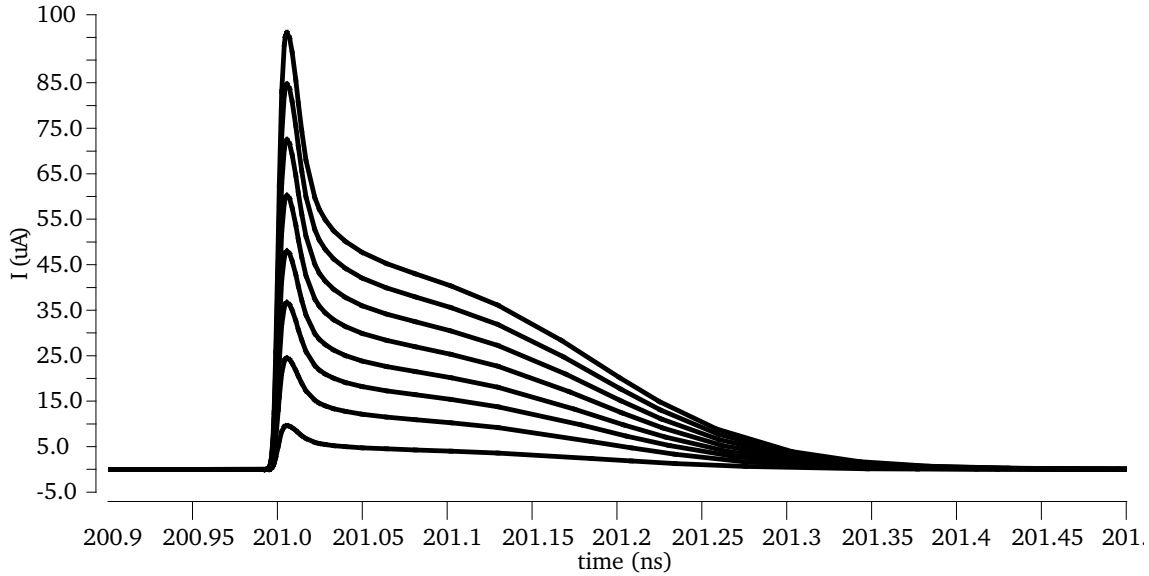
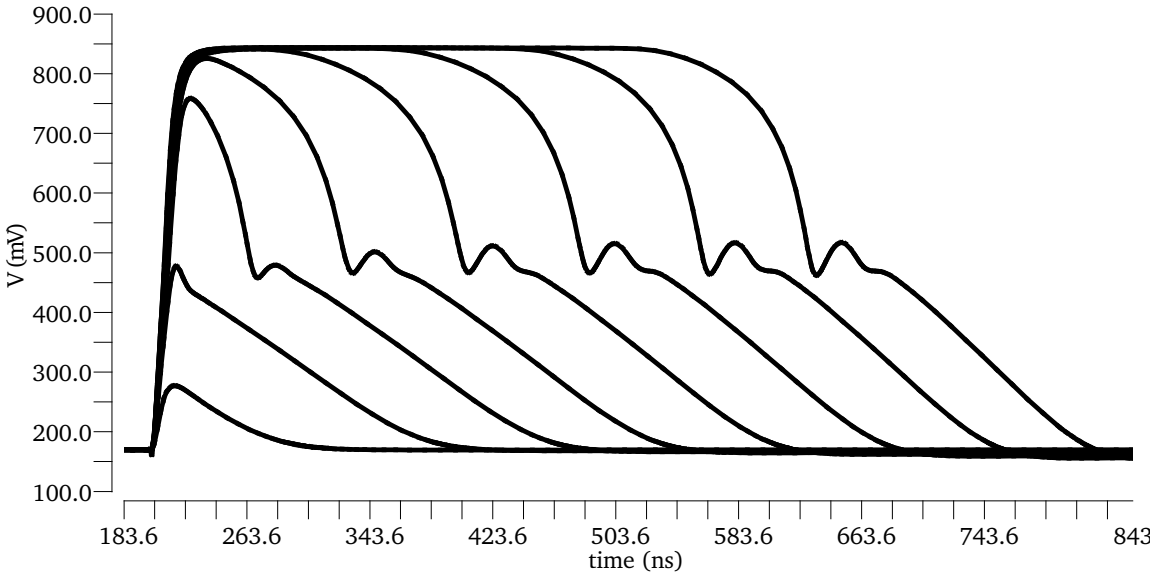


input current pulses



output voltage pulses

- **threshold crossing drift** related to signals **amplitude**
- Current pulses obtained **assuming** constant **pulses duration** $\rightarrow$ input charge: $(1 \div 10) fC$
- Range saturation observed at 4 fC

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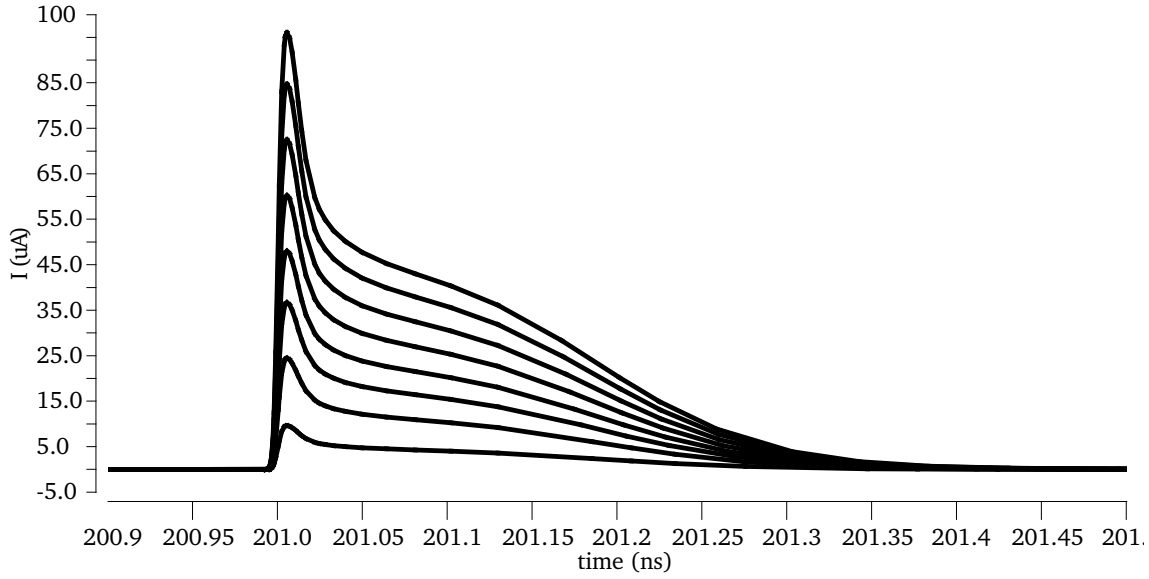

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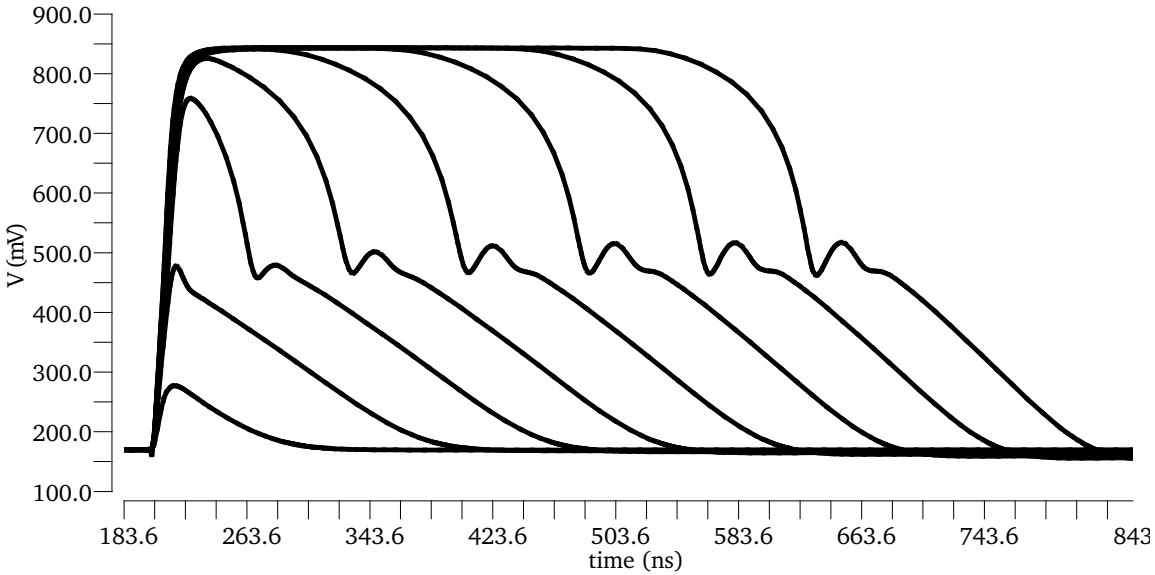

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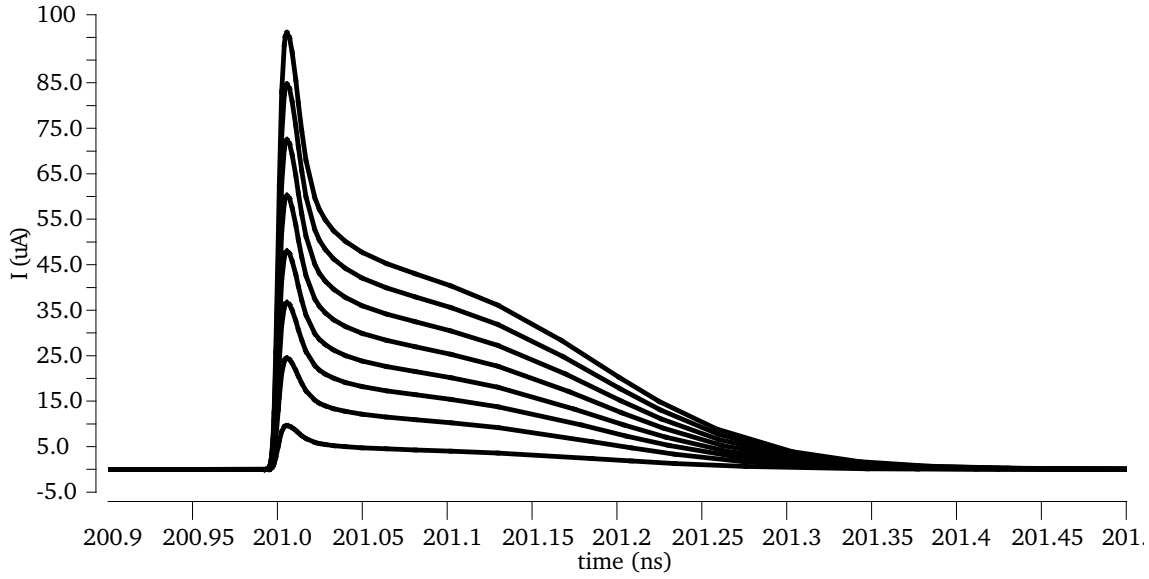

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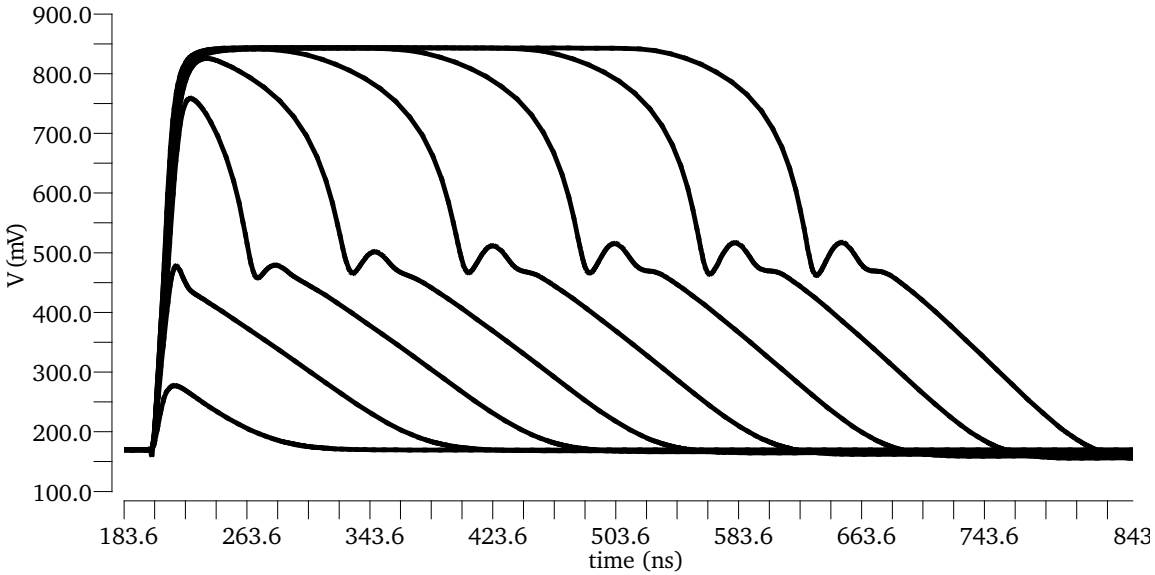

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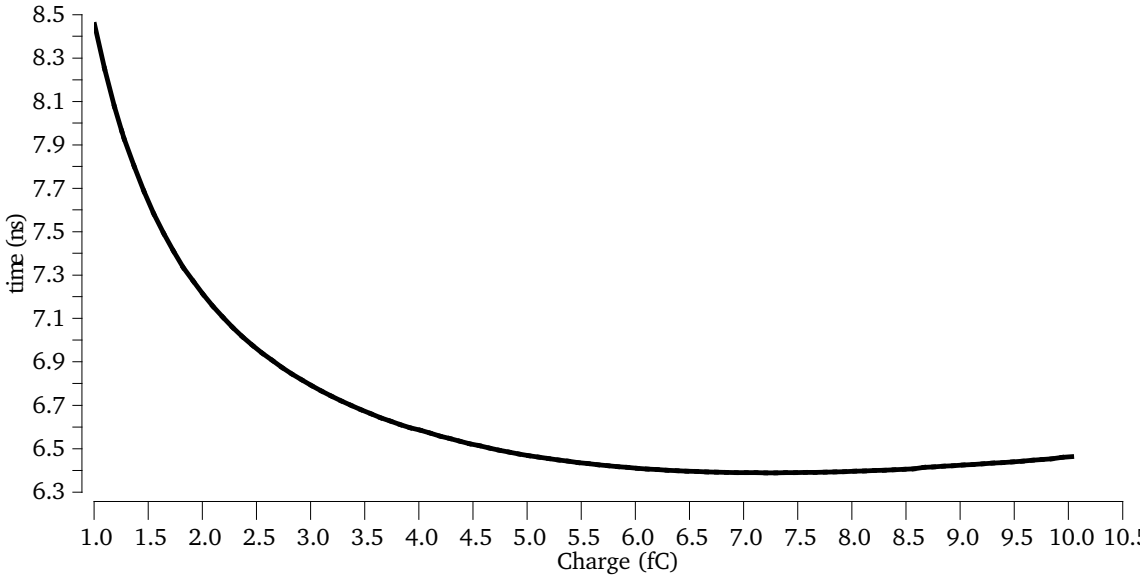
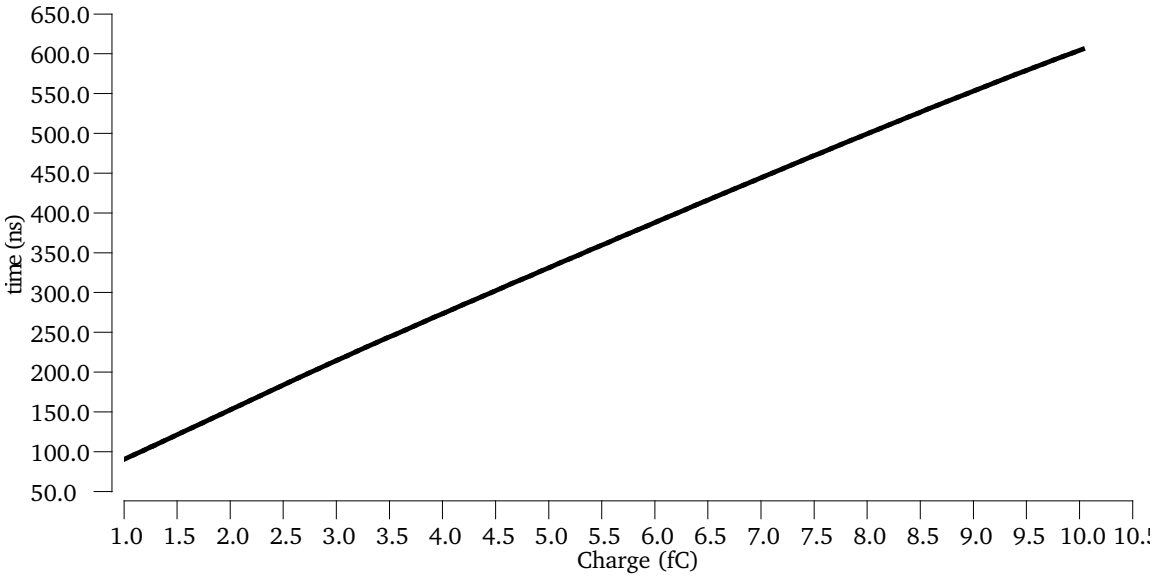


time-walk versus charge



Ideal ToT versus charge

- total variation 2.1 ns $\rightarrow$ **time-walk correction needed** (CFD or ToT)
- non monotonic response to be investigated
- Ideal ToT very linear $\rightarrow$ correction applicable in the monotonic range

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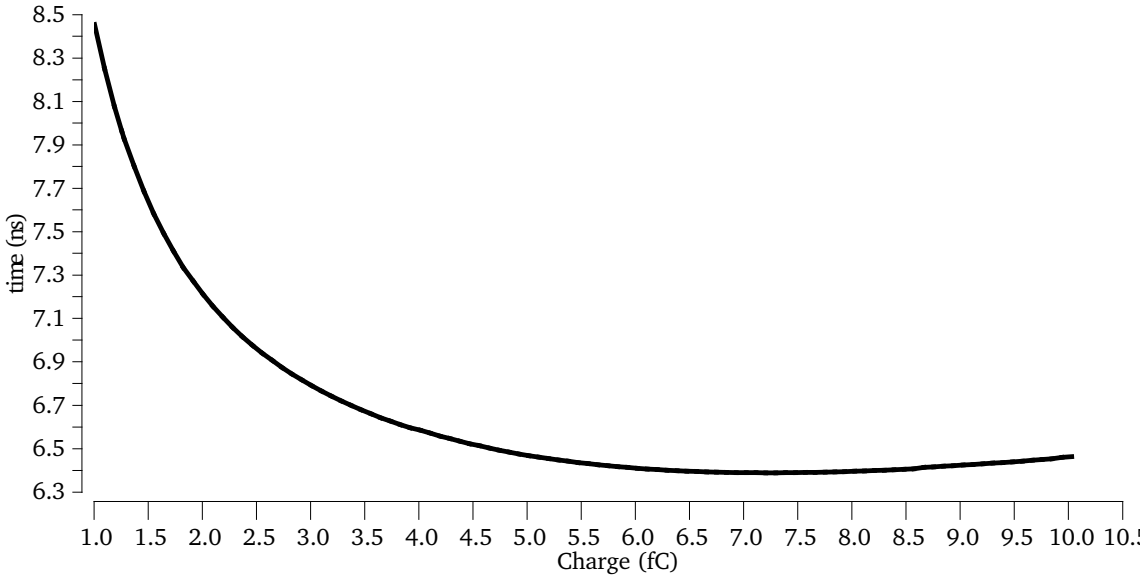

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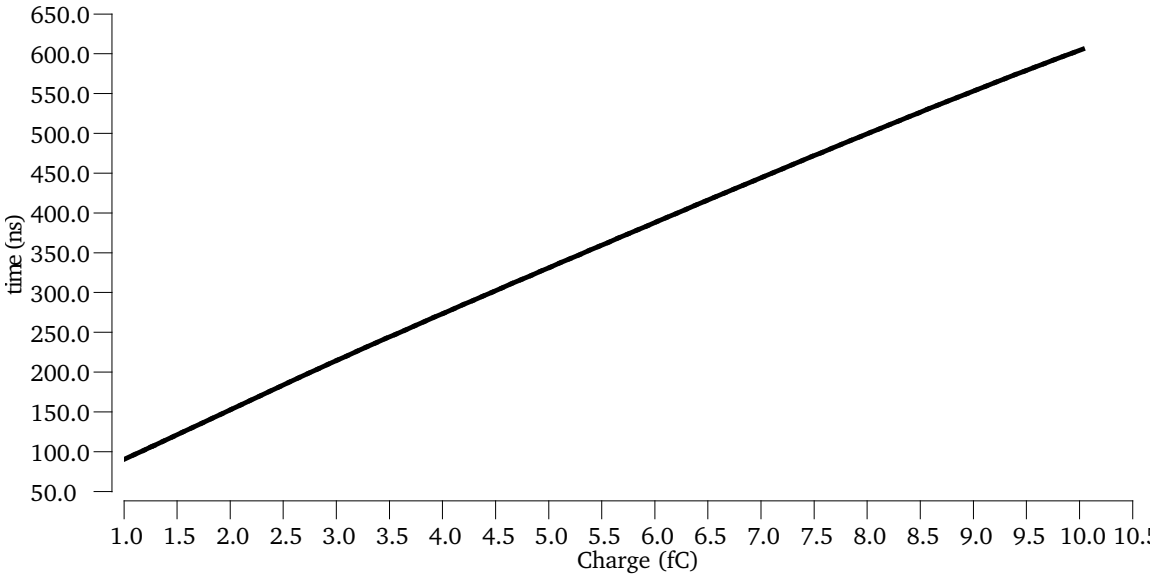

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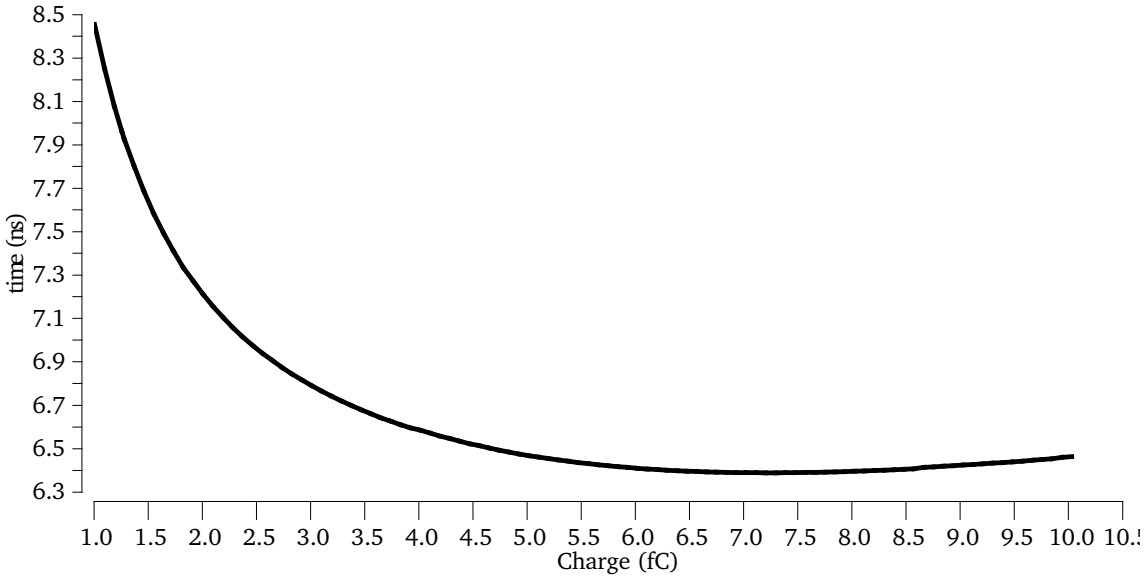

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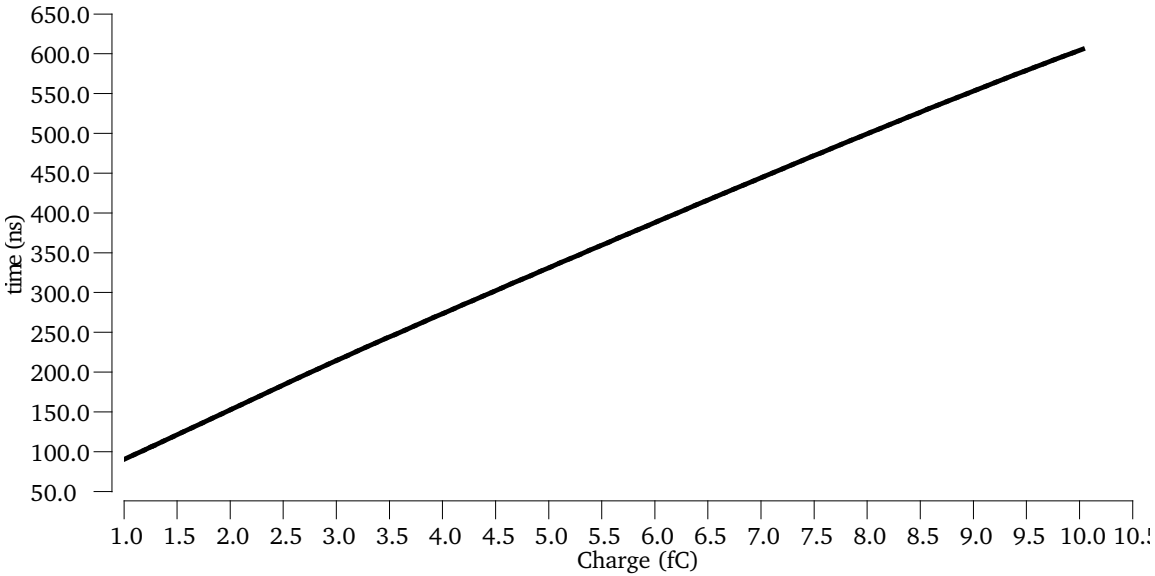

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Outline

Conclusions

- Good results for the 65 nm design
- The CSA design was successfully ported in 28 nm
- Good timing reliability for signal, mismatch and process variations

Future Developments

- Optimize for noise reduction
- Investigate time-walk correction techniques
- 28 nm discriminator implementation
- Produce 28nm layout
- Simulation with parasitics and optimization
- A test chip for analog blocks will be produced later this year

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