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~ MASTER THESIS ~

LOW POWER FRONT-END ELECTRONICS FOR HYBRID PIXEL DETECTORS

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Low Power Front-End Electronics for Hybrid Pixel Detectors [1]

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1 *Thesis written with LaTeX[1]*

A thought is a seed with promise.
A dream is a wish with wings.

Dedicated to my family.

ABSTRACT

$\overline{\text{P}}$ANDA is a planned particle physics experiment at the future international Facility for Antiprotron and Ion Research (FAIR) which is currently being built in Darmstadt. In order to cope with the physics goals of the experiment, the $\overline{\text{P}}$ANDA detector is based on an asymmetric double spectrometer. In these work the main parts of the detector are described with a particular attention to the MVD, the silicon based high precision vertex detector placed close to the interaction point. The inner layers of the MVD are equipped with hybrid pixels detectors which are based on a modular structure where detector, transmission bus and readout ASIC are connected using bonding techniques. The ASIC developed for the hybrid pixel sensors, called ToPix, uses a commercial deep-submicron CMOS 0.13 μm technology with a power supply of 1.2 V and, based on the Time over Threshold Technique (ToT), allows to obtain from the analog signal generated by a particle hit, the time stamp and the energy loss measurement. In this thesis, the three prototypes until now developed are described together with the experimental results, underlining the problems observed. The test results of the third prototype, ToPix v3, show a good performance but with some features to improve, like the tuning system which, due to a non-linear response between the DAC code and the voltage variation obtained, would require a lot of time to tune the threshold of the millions of pixels of the MVD. This work aims to find a solution for this problem analyzing the parts of the front-end involved, as the DAC and the discriminator. The solution should be implemented in the very small silicon area of 13 μm $\times$ 28 μm and will be part of a new version of the DAC which would allow to obtain the linear relation required to solve the problem. Three possible solutions are described with the help of the most significant simulation results. The solution selected is described in more detail and the most important simulations performed to check the circuit reliability for different working conditions are illustrated.

A part of this work is also dedicated to study the use of a new CMOS technology with similar feature size which should allow to develop an ASIC with the same performance but at a lower production cost. The study is based on the comparison between the different performances of the discriminator, which has been studied exploring different devices flavours. The most significant simulation results obtained selecting from the large set of simulations performed, are discussed.

SOMMARIO

$\overline{\text{P}}$ANDA è un esperimento di fisica nucleare che avrà luogo presso la Facility for Antiprotron and Ion Research (FAIR) attualmente in costruzione a Darmstadt. Per raggiungere gli obiettivi dell'esperimento, il detector di $\overline{\text{P}}$ANDA utilizza una struttura a doppio spettrometro asimmetrico. In questa tesi vengono descritte le parti più importanti del detector, focalizzandosi con maggior attenzione sul MVD, il vertex detector ad alta precisione collocato vicino al punto di interazione. Gli strati più interni del MVD utilizzano pixel ibridi basati su una struttura modulare in cui detector, bus di trasmissione e ASIC di readout vengono connessi utilizzando la tecnica del bonding. L'ASIC sviluppato per i pixel ibridi, chiamato ToPix, utilizza la tecnologia commerciale CMOS 0.13 μm alimentata a 1.2 V e, grazie alla tecnica del Time over Threshold (ToT), permette di ottenere dal segnale creato da una particella, l'energia depositata ed il tempo relativo all'urto con il sensore. In questa tesi i tre prototipi di ToPix finora sviluppati sono descritti insieme ai risultati sperimentali, sottolineando gli eventuali problemi riscontrati. Si parte dai risultati del terzo prototipo, ToPix v3, che mostrano un ottimo funzionamento ma con alcune caratteristiche che potrebbero essere migliorate, come il sistema di regolazione della soglia dei pixel che, a causa di un comportamento non lineare tra regolazione del DAC e la variazione di tensione ottenuta, richiede molto tempo per regolare i milioni di canali presenti nel MVD. Questo lavoro punta allo studio delle cause che sono alla base di questo problema, analizzando le parti del front-end coinvolte, come il DAC e il discriminatore, in modo da trovare una soluzione da realizzare in un'area di silicio di 13 μm $\times$ 28 μm. Sono descritte tre possibili soluzioni del problema insieme all'aiuto dei risultati più significativi. Infine la soluzione finale scelta è descritta con più attenzione, riportando anche la descrizione delle simulazioni più importanti svolte al fine di controllare l'affidabilità del circuito in diverse condizioni di lavoro.

Una parte di questa tesi è poi dedicata allo studio dell'utilizzo di una nuova tecnologia CMOS con una dimensione simile a quella attualmete utilizzata che potrebbe permettere lo sviluppo di un ASIC con le medesime caratteristiche ma ad una costo di produzione inferiore. Lo studio è basato sul confronto tra le caratteristiche del discriminatore ottenute implementandolo con i dipositivi forniti dalle due diverse tecnologie. I risultati più significativi, scelti da una lunga serie di simulazioni svolte, sono riportati al fine di poter fare un confronto sulle due tecnologie analizzate.

CONTENTS

1

THE $\overline{\text{P}}$ANDA EXPERIMENT

1.1 INTRODUCTION

$\overline{\text{P}}$ANDA (antiProton ANnihilation at DAmstadt) will be one of the most important planned experiments at FAIR, the future international Facility for Antiprotron and Ion Research which is currently being built on the area of the GSI, in Darmstadt. For this new facility the present GSI accelerators, once upgraded and together with a new proton linear accelerator, will serve as pre-accelerator and injector for the new complex. An overview of the FAIR facility is given in Figure 1.1.

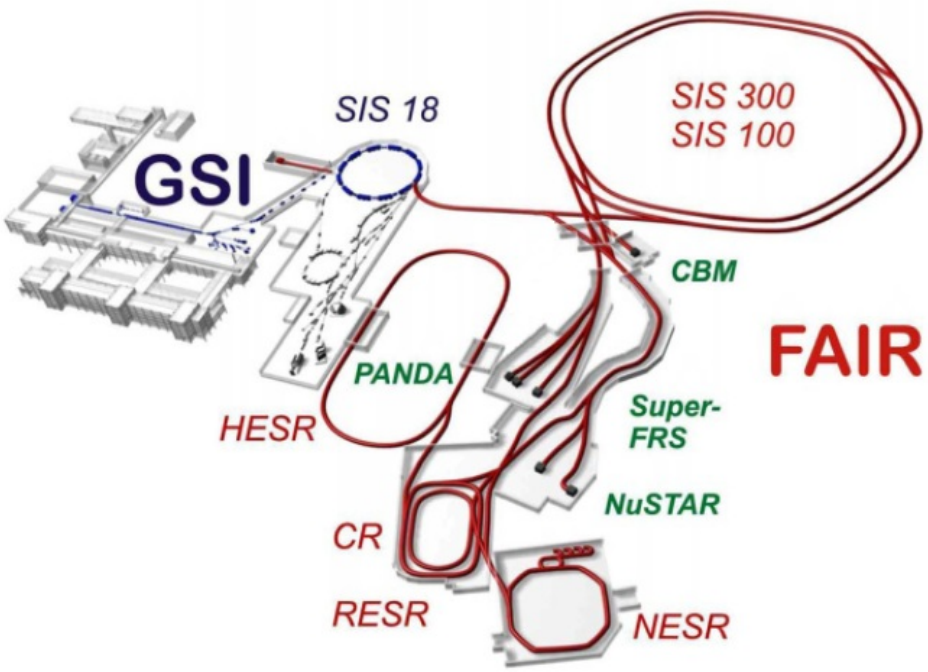


Figure 1.1: FAIR Facilities Layout. New accelerators and storage rings are highlighted in red while the experimental sites are indicated with green letters [2].

The core of FAIR, a double-ring accelerator (SIS100 heavy ion synchrotron), will be associated with a complex system of cooler and storage rings and experimental setups. This complex system allows to drastically improve the quality of the secondary beams, providing antiprotons and exotic nuclei for several experiments.
One of the most important elements of FAIR is the High Storage Ring (HESR), designed to run with antiproton in two operating modes: high resolution mode and high intensity mode. In the high resolution mode, the particle momentum can be varied from 1.5 to 8.9 GeV/c and the resolution $\delta p/p$ is 10^{-5}, while in the high intensity mode the momentum increases up to 15 GeV/c but at the price of a resolution reduction $\delta p/p$ to the value of 10^{-4}. During the experiments the antiprotons produced by a primary proton beam will be filled into the HESR and then collide with the fixed target inside the $\overline{\text{P}}$ANDA Detector [2].

The $\overline{\text{P}}$ANDA experiment is being designed to fully exploit the physics potential arising from the availability of beams of antiprotons or radioactive ions of unprecedented intensities, energies and qualities. In order to cope with this challenge the whole project is characterized by many technological innovations.

1.2 THE SCIENTIFIC PROGRAM

FAIR will be constructed to explore the nature of matter and the evolution of the universe. The scientific program ranges in different fields of physics from charmonium spectroscopy to the search for exotic hadrons and the study of nucleon structure, from the study of in-medium modifications of hadron masses to the physics of hypernuclei. Therefore, to make these experiments possible, antiproton beams in the momentum range from 1.5 GeV/c to 15 GeV/c will be provided by the high energy storage ring (HESR) to the $\overline{\text{P}}$ANDA experiment giving the access to a center of mass energy range from 2.2 GeV/c^2 to 5.5 GeV/c^2 [2] [3].

Nowadays all these studies are carried out mainly at electron machines. These facilities offer the advantage of kinematically clean reactions but at the price of a reduced set of final states and reduced cross-sections that limit the precision data over the full charm spectrum for the future planned experiments. For this reason, the $\overline{\text{P}}$ANDA experiment will be in the future a unique tool to improve both statistics and precision of existing data and to further explore the physics in the charm quark sector.

The main fields of the hadron physics program are briefly summarized below:

- **The Hypernuclear Physics**:

  Single and double Λ-hypernuclei were discovered more than 30 years ago but, in spite of a considerable effort during the last 10 years, only 6 double Λ-hypernuclei are presently known.

  A hypernucleus is a nucleus obtained replacing an up or a down quark with a strange quark. In this way a new quantum number is introduced into the

nucleus: the strangeness. Thanks to the use of $\overline{p}$ beams an efficient production of hypernuclei with more than one strange hadron will be possible. In this way with these studies a new chapter of strange physics will be opened for nuclear structure spectroscopy.

- **Open Charm Spectroscopy**:

  In highly energetic collisions the momentum transfer can be large enough to create hadrons which contain heavier quarks. D mesons are examples of hadrons which contain a light quark $D^0 = (c\overline{u})$ and they are referred to as open charm.

  A large production number of $D\overline{D}$ meson pairs is expected running the HESR at full luminosity mode and at $\overline{p}$ momenta larger than 6.4 GeV/c. Thanks to the well-defined production kinematics of D meson pairs and to the high yield would be possible to accomplish with the charmed meson spectroscopy program.

- **Charmonium Spectroscopy**:

  $\overline{p}p$ annihilations will be used to create charmonium states. In this way the whole energy region below and above the open charm threshold will be probed. This will be very important for a better understanding of QCD. The charmonium spectroscopy will be performed using a $\overline{p}$ beam with the resonance energy required for the experiment and then performing an energy scan with a fine tuning of the beam momentum. The several thousand of $\overline{C}C$ states expected per day, obtained by using the detector at full luminosity, will allow fine scans to measure masses with accuracies of the order of 100 keV and widths to 10% or better. In general the precision of these measurements depends only on the accuracy of the determination of the initial $\overline{p}p$ state energy, thus only on the momentum spread.

- **Gluonic Excitations**:

  The $\overline{P}$ANDA physics program contains also one of the challenges of hadron physics: the search for gluonic excitations. The gluonic hadrons can be divided in two main categories: glueballs and hybrids. Glueballs are for example states where only gluons contribute to the overall quantum numbers while hybrids consist of a valence-quark plus one or more excited gluons which contribute to the overall quantum numbers.

  The additional degrees of freedom carried by gluons allow these hybrids and glueballs to have J^{PC} exotic quantum numbers. In this case, where is possible to exclude mixing effects with nearby $q\overline{q}$ states, the experimental identification of these particles is easier. The study of the glueballs and hybrids properties, which are determined by the long-distance, is important for understanding the dynamics of low energy QCD and of the structure of the QCD vacuum.

The gluonic hadrons mass range will be studied in the first step using the high luminosity modality to observe the candidate states and then using the precision modality to analyze the interesting mass region. The final step consists in a spin-orbit analysis for the determination of the quantum numbers of the observed states.

- **Hadrons in Nuclear Matter**:

  Nowadays in other facilities experiments are focused only on the light quark sector, but thanks to the high intensity $\overline{p}$ beam, up to 15 GeV/c, in $\overline{P}$ANDA it will be possible to obtain an extension of the existing experiments to the charm sector, both for hadrons with hidden and open charm.

  The study of in-medium modifications of hadrons embedded in hadronic matter is aimed at understanding its partial restoration in a hadronic environment and the nature of hadron masses in the context of spontaneous chiral symmetry breaking in QCD.

  Another study which can be made is the measurement of J/ψ and D meson production cross sections in $\overline{p}$ annihilation on a series of nuclear targets.

- **The Nucleon Structure**:

  The recent theoretical framework of GPDs (Generalized Parton Distributions) caused excitement in the field of understanding the nucleon structure. In fact, it has been shown that exclusive $\overline{p}p$ annihilation into two photons at large s and t can be described in terms of GPDs. In this context, thanks to the electromagnetic processes, $\overline{P}$ANDA will also be able to investigate the structure of the nucleon.

  The main electromagnetic processes used in the experiment will be the Deeply Virtual Compton Scattering (DVCS) and the process $\overline{p} + p \rightarrow e^+ e^-$. The last one will allow the determination of the electromagnetic form factors of the proton in the time-like region over an extended q^2 region [2][3].

1.3 THE PANDA DETECTOR

A complex detector arrangement based on a setup of modular subsystems is necessary in order to achieve the proposed physics goals. Therefore, PANDA is designed as a multi-purpose apparatus following the below requirements:

- High resolution for tracking
- Good particle identification
- Full coverage of the solid angle
- High rate capabilities
- Versatile Readout
- Good event selection
- A triggerless system for the data acquisition

To obtain a good momentum resolution the proposed detector will be arranged as an asymmetric double spectrometer composed by the following two parts:

- **The Target Spectrometer (TS)**: This part of the detector surrounds the interaction point where the charge tracks will be measured using a highly homogeneous solenoidal field. The detectors contained in TS will have an onion shell like configuration in the same manner of a collider detector. The pipes for the injection of target material will have to cross the spectrometer perpendicular to the beam pipe. An overview of the TS layout is given in Figure 1.2.

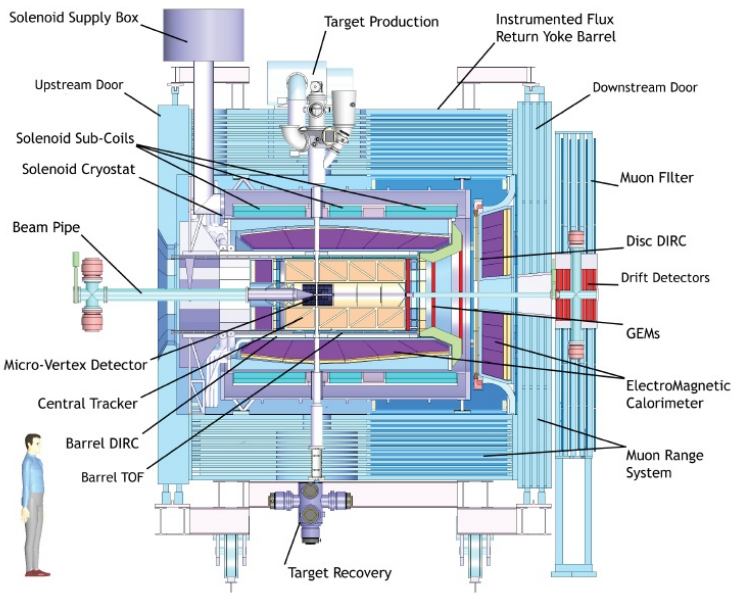


Figure 1.2: Artistic side view of the Target Spectrometer (TS) of PANDA [2].

- **The Forward Spectrometer (FS)**: Based on a dipole magnet, the FS will allow the reconstruction of all particles emitted with horizontal and vertical polar angle smaller than 10° and 5°, respectively. Many devices, like the dipole magnet, the Forward RICH, the drift chambers and the Muon/hadron identification systems will compose this part of the detector. The setup of the FS is depicted in Figure 1.3.

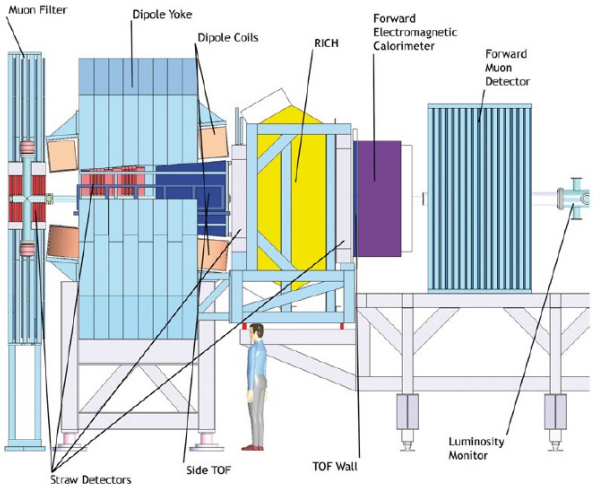


Figure 1.3: Artistic side view of the Forward Spectrometer (FS) of PANDA [2].

With the installed setup, a good particle identification with an almost complete solid angle will be combined with excellent mass, momentum and spatial resolution. Moreover, the foreseen triggerless readout will improve the system flexibility. The final PANDA detector layout contains both Target Spectrometer and Forward Spectrometer, as shown in Figure 1.4.

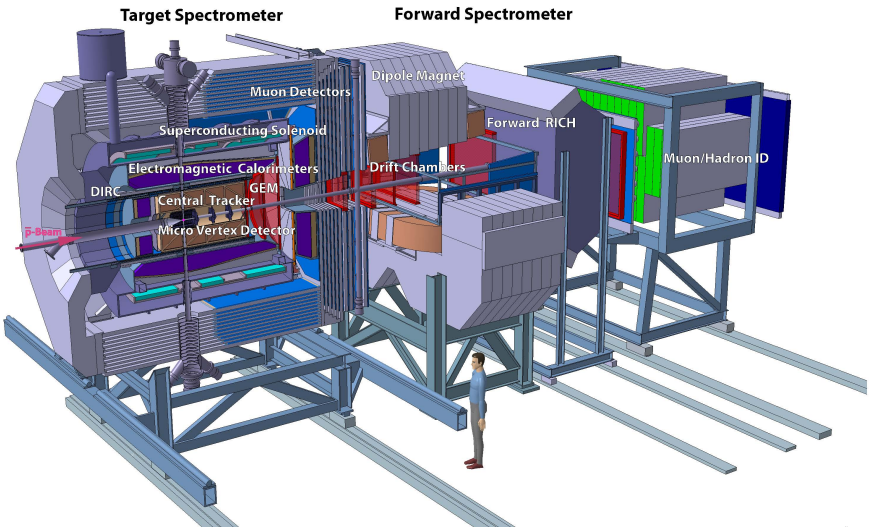


Figure 1.4: Layout of the PANDA detector consisting of a Target Spectrometer, surrounding the interaction region, and a Forward Spectrometer to detect particles emitted in the forward region [2].

The whole detector contains the fundamental systems, like the charged particle identification system, the tracking system, the target systems and the calorimetry which are compulsory to achieve the experimental purposes of PANDA. A short description of these systems is given in the following paragraphs.

1.3.1 *Charged Particle ID system*

One of the most important goals to achieve the physics program envisaged, is the identification of charged particles with extreme precision. Therefore, the PANDA Detector will be equipped with some dedicated particle identification systems inside the target spectrometer and in the forward region around the dipole magnet. The planned configuration will allow to classify the particle species over the whole kinematic range in addition to *dE/dx* measurements from tracking and information from the electromagnetic calorimetry.

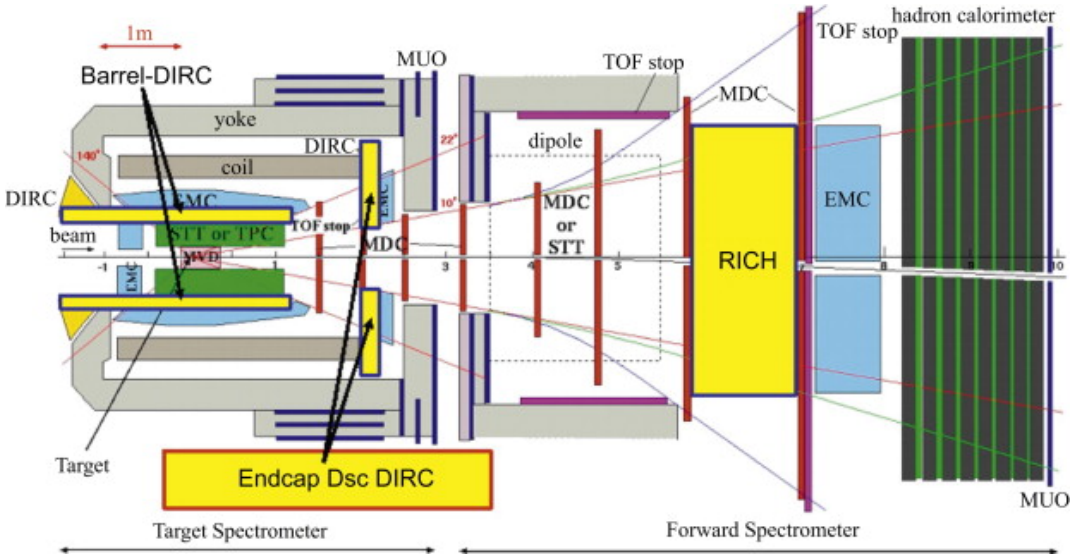


Figure 1.5: Layout of the Identification particles of the PANDA detector. The Čherenkov detectors are indicated in yellow while the Muon Detection System in blue color. The ToF system is indicated in purple color.

The systems, which allow the particle identification, are called PID devices. They are shown in the Figure 1.5 and briefly described below.

- *ČHERENKOV DETECTORS*

  These detectors are based on the Čherenkov radiation phenomenon which consists of photons that are emitted along a characteristic cone when a charged particle passes through a dielectric.

  It is well known that the speed of light in vacuum (c = 300,000 km/s) is the maximum reachable velocity. However, if n is the index of refraction the

speed of light in the medium is less than c ($v = c/n$). It can happen that very fast particles traverse medium with a velocity that is slower than the speed of light in vacuum but faster than the speed of light in that medium. This particle will emit a cone of light called *Čherenkov radiation*. If $\beta > 1/n$ is the velocity, the radiation will be emitted at an angle $\theta_c = \arccos(1/\beta\, n)$ [4]. Thus, combining the velocity information determined from θ_c with the momentum information from the tracking detectors, it is possible to determine the particle mass.
Since the momentum particle of this detectors has a strong variation with the polar angle, two different Čerenkov detectors will be employed for particle identification.

The DIRC detectors, which are based on the principle of Detection of Internally Reflected Čherenkov radiation, will be located in the target spectrometer where relatively slow particles are expected. The DIRC is also used in the BaBar detector but at $\overline{\text{P}}$ANDA, it is intended to focus the images by lenses onto Micro Channel Plate PhotoMultiplier Tubes (MCP PMTs) which are insensitive to magnet fields [5].

The first DIRC detector is the barrel DIRC which will cover the angular region between 22° and 140°. It will consist of 1.7 cm thick quartz slabs surrounding the beam line at a radial distance of 45 cm to 54 cm.

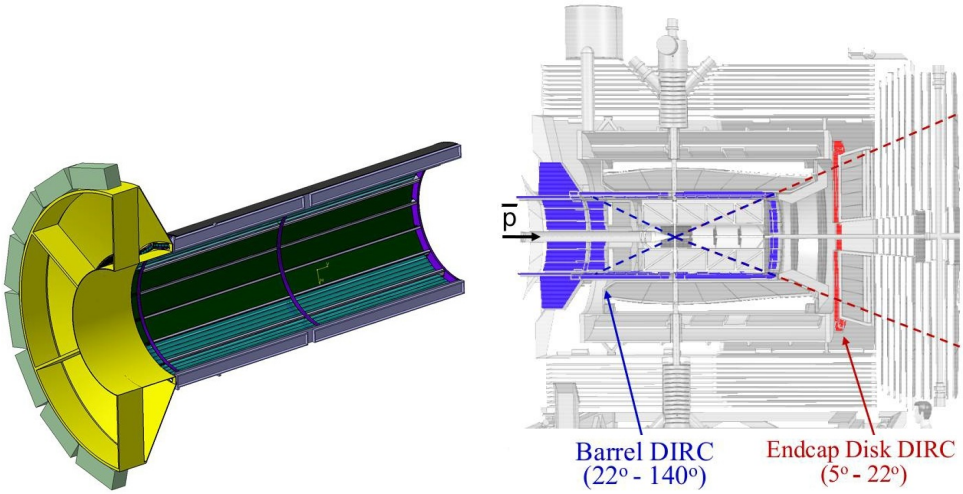


Figure 1.6: Layout of the DIRC detector. The blue and the red region represent the barrel DIRC and the end cap disk DIRC, respectively.

The End-Cap DIRC, the second DIRC detector, will be placed as shown in Figure 1.6, directly upstream of the forward end cap calorimeter and it will cover the remaining angular region down to 5°. It consists in the same radiator fused silica, but in a shape of a disk of 2 cm thick and 110 cm of radii.

In this configuration the DIRC will provide the π/K separation up to about 4 Gev/c and the distinction between γ's and relativistic charged particles.

The Ring Imaging Čerenkov detector, or simply RICH, is the third Čherenkov detector and will be used for hadron identification. Like shown in Figure 1.7, it will be placed in the forward direction. The RICH estimates the particles velocity with a high accuracy (0.1%). To reduce the RICH material effect on the electromagnetic calorimeter (ECAL) energy measurement, the sensitive area presents a hole [6].

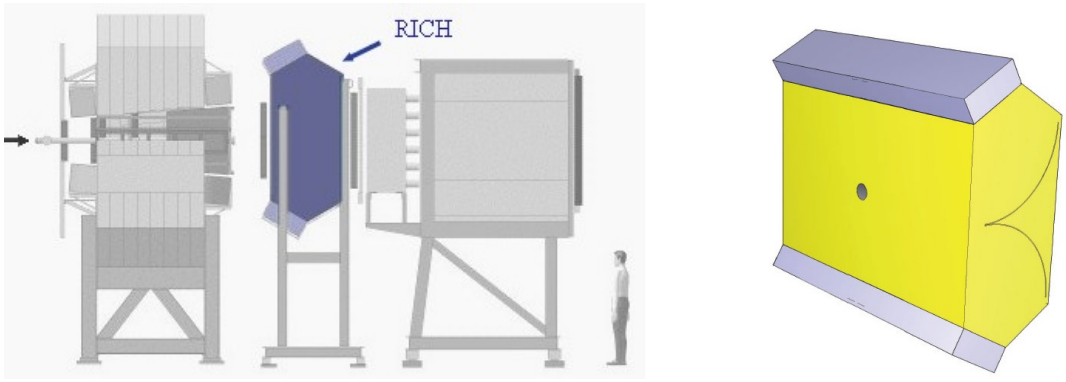


Figure 1.7: Layout of the RICH detector.

- *MUON DETECTION SYSTEM*

  This system (MUO) is composed of the instrumentation of the magnet yokes to identify muons. Generally the processes of interest having muons in final states could have small cross sections as compared with the backgrounds. Therefore, a very good muon identification will be necessary to maximize signal to background ratio.

  The muon detection will be implemented through the Range tracking System (RS) which is composed of 13 sensitive layers, each with 3 cm thick like shown in Figure 1.5. They alternate with 3 cm thick iron absorber layers, introducing enough material for the absorption of pions in the PANDA momentum range and angles. Thanks to this configuration it will be possible to distinguish the energy loss processes of muons and pions and therefore obtain a good separation between the background and the primary muons.

  The setup is different in the forward and cap because more material is needed due to the higher momenta of the occurring particles. The foreseen setup in this region consists of six detection layers placed around five iron layers of 6 cm each within the downstream door of the return yoke, and a removable muon filter with additional five layers of 6 cm iron. Moreover, rectangular aluminum Mini Drift Tubes (MDT) are foreseen as sensors between the absorber layers.

  This system is a good way to detect the muons stopped by the absorber and those which pass through the iron.

- *TIME OF FLIGHT SYSTEM (TOF)*

  The TOF system will provide the particle identification for slow particles at large polar angles. Since the released energies per particle both at low beam energies and at high beam energies are low, a Time of Flight barrel in the Target Spectrometer is desirable for the particle identification of slow charged particles and for the DIRC detector.

  The reaction $\overline{p} + p \rightarrow \Xi^- + \Xi^+$ is an example of the production of Ξ which has low momentum energy. Since the value of this cross section is likely four orders of magnitude lower than the one corresponding to the $\overline{p} + p$ annihilation process, the background suppression plays an important role in the unique identification of hypernuclei. Moreover, the mayor part of Ξ^+ annihilates releasing in most cases two positive kaons. The identification of this kaon via a TOF provides a possibility to tag the production of hyperons.

  The Time Of Flight system consists of a scintillating fibers array and a cylindrical scintillator detector, which provides the start and stop time measurement, respectively.

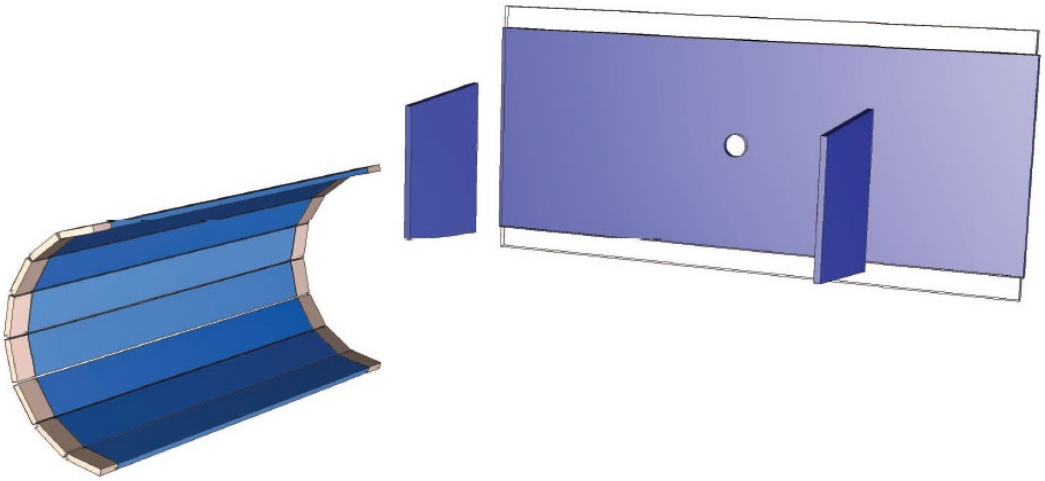


Figure 1.8: Complete layout of the TOF scintillator barrel.

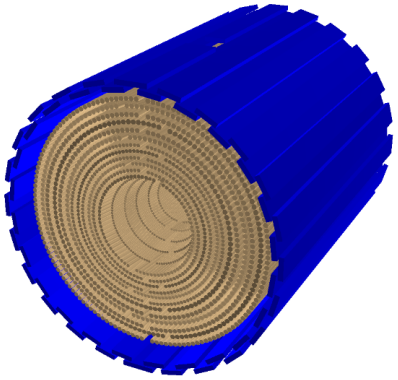


Figure 1.9: Schematic view of the Mini Drift Chamber (brown) enclosed by the Scintillator Barrel (blue).

The TOF scintillator barrel at $\overline{\text{P}}$ANDA, shown in Figure 1.8, is composed of 2.85×2.85 cm^2 tiles of fast scintillator with thickness 0.5 cm mechanically mounted together with the DIRC detector in order to achieve low energy threshold. In total the 5000 tiles foreseen will allow to obtain a time resolution of 100 fs [2][7].

The ToF system foresees also a scintillator wall of 5.6 m wide and 1.4 m tall which will be placed in the forward region at a distance of ~ 7 m downstream the target. The wall will be composed of 60 vertical scintillator strips. In this part of the ToF system a time resolution of 50 ps is expected.

The timing barrel for the trigger of the hypernuclei program will allow to increase the detection probability for $\overline{\Xi}$ particles by a factor of up to 1000 by detecting the slow kaon decay products. For the DIRC subsystem, the TS-ToF barrel could serve as a time reference to use in addition to the information obtained from the Čherenkov images. Thanks to these information it will be possible to reduce the background and to correct dispersion effects.

The full system is optimized in order to reduce the material budget to a value less than 2% of one radiation length.

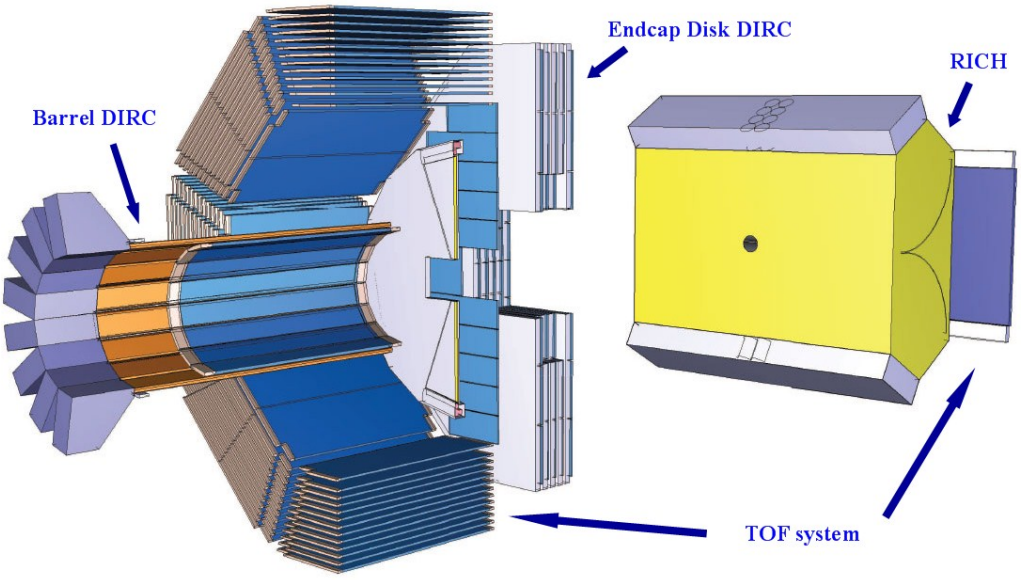


Figure 1.10: Layout of the complete identification system.

1.3.2 *Tracking System*

The tracking system will provide a measurement of charged particle trajectories with high spatial resolution over the complete solid angle. To achieve the proposed goals of the experiment four different tracking systems are foreseen inside the Target Spectrometer and in the forward region around the dipole magnet.
In Figure 1.11 is shown the complete tracking system of PANDA.

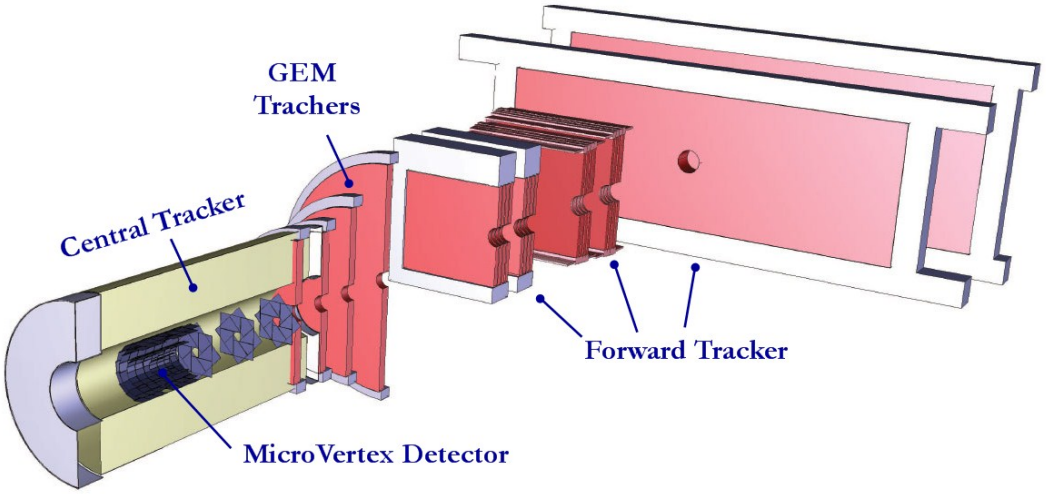


Figure 1.11: Layout of the Tracking System.

The different subdetectors illustrated in the figure are optimized in order to get an accurate determination of the particle momenta, a high spatial resolution of the primary interaction vertex and the detection of displaced secondary vertices.

A brief description of these subdetectors is given in the following:

- *THE MICRO VERTEX DETECTOR (MVD)*

  The Micro Vertex Detector, or simply MVD, is the silicon based high precision vertex detector for the Target Spectrometer. The MVD is placed in the inner part of the detector close to the interaction point, therefore its design is properly optimized for a maximum acceptance. The detector will detect the secondary decay vertices from charmed and strange hadrons and will also improve the transverse momentum resolution. A complete description of the Micro Vertex Detector will be given in Charter 2.

- *THE SRAW TUBE TRACKER (STT)*

  The Straw Tube Tracker (STT), together with the Time Projection Chamber, is a subdetector used for the principal track reconstruction. The STT consists of aluminized mylar tubes called straws. Each straw tube is constructed with a single anode wire in the center that is made of 20 μm thick gold plated tungsten and it is filled with a gas mixture. In PANDA the straws will be stiffened by operating them at an overpressure of 1 bar which makes them self-supporting.

The detection of the particle which transverses the straw tube will be possible thanks to the ionization effect and to the high voltage of some kV applied between the wire and the tube. With this configuration setup, once the charges are near enough to the wire (~ 50 μm), an avalanche multiplication takes place with an amplification of 10^4 - 10^5 of the primary charge allowing the readout of the electric signal. Measuring the arrival time of the signal and the charge collected it is possible to evaluate the coordinates and the particle energy lost by ionization, respectively.

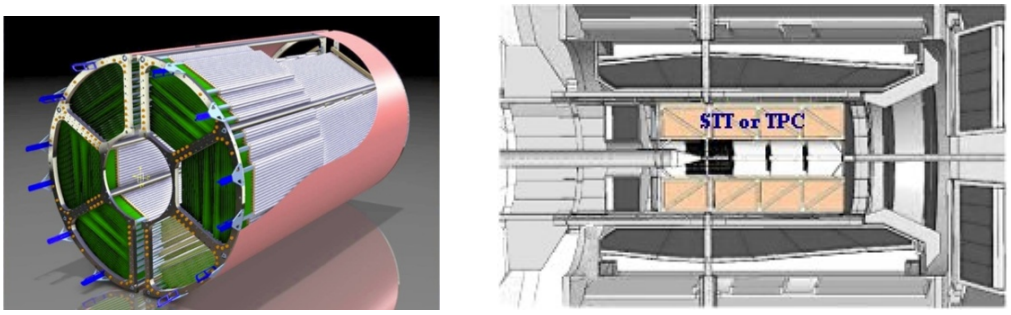


Figure 1.12: Schematic view of the Straw Tube Tracker with the position in the Target Spectrometer.

The PANDA Straw Tube Tracker is composed of an ensemble of 150 cm long drift tubes, arranged in planar layers in a hexagonal shape around the MVD like shown in Figure 1.12. In total the layers are 27 of which the 8 central ones are skewed to achieve a good spatial resolution also in z. The basic module used is a planar double-layer of tubes in order to resolve the left-right ambiguity of the track position with respect to the wire. Moreover, the gap to the surrounding detectors will be filled with further individuals straws so that in total there will be 4210 straws around the beam pipe [8].

Concerning the gas choice, an Ar/CO2 gas mixture (90/10) has been chosen for the PANDA straw tubes. This mixture is a compromise between a good spatial resolution and the material budget, which must be small to minimize the multiple scattering [3].

- *GAS ELECTRON MULTIPLIER STATIONS (GEM)*

  The Gas Electron Multiplier (GEM) is a type of gaseous ionization detector used for radiation detection. These detectors are able to collect the electrons released by ionizing radiation guiding them to a region with a large electric field and thereby initiating an electron avalanche. The avalanche is able to produce enough electrons to create a current large enough to be detected by electronics.

  The GEM-Trackers are composed of a set of large area planar GEM detectors and will be used as a first forward tracking detector after the central tracker (see Figure 1.13) in other to track the particles emitted at angles below 22° which are not covered fully by the STT.

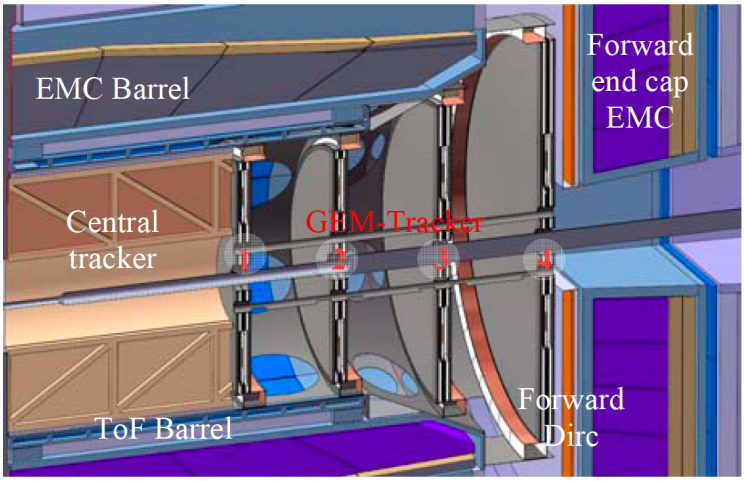


Figure 1.13: Gas Electron Multiplier Trackers in the Target Spectrometer [3].

In Figure 1.13 the planar GEM detectors used in the target spectrometer are shown. The current implementation includes 3 or 4 GEMS discs depending on the length of the central tracker. Anyway the exact number of planes and also their positions, are yet to be determined based on the simulations studies. Each GEM disc will be equipped with Gaseous micro-pattern detectors based on GEM foils as amplification stages. Moreover, each disc will contain in the middle a double sided read-out pad plane which allows particle track position measurement in four projections.
Thanks to the high number of projections per GEM discs it will be possible to obtain an optimal determination of the particle trajectory position with a resolution better than 100 µm.

- *FORWARD TRACKER (FT)*

  The Forward Tracker (FT) consists of three pairs of planar tracking stations designed for momentum analysis of charged particles which are deflected in the magnetic field. The detector will be placed in front, within and behind the dipole magnet. Each pair will contain two autonomous detectors so that the independent detectors mounted will be 6. The FT covers angular acceptance equal to $\pm$ 10° horizontally and $\pm$ 5° vertically with respect the beam direction.

  The same straws used for the central tracker will be employed for the modules which form the detection planes. Every module consists of 32 straws arranged in two layers and has its own preamplifier-discriminator card in order to be autonomous mechanically and electrically. The modules are mounted side by side on a support frame which is employed for two double layers. Moreover, each tracking station consists of four double-layers mounted with a configuration which allows to reconstruct tracks in each pair of tracking stations separately, also in case of multitrack events. Concerning the read-out electronics for the straw detector, it should meet high requirements caused by the high counting rates [3].

1.3.3 *Calorimetry system*

The calorimetry system is composed, as shown in Figure 1.14, of two electromagnetic calorimeters placed in the target spectrometer and a hadron calorimeter in the forward spectrometer used respectively for the detection of photons and for the detection of neutral hadrons.

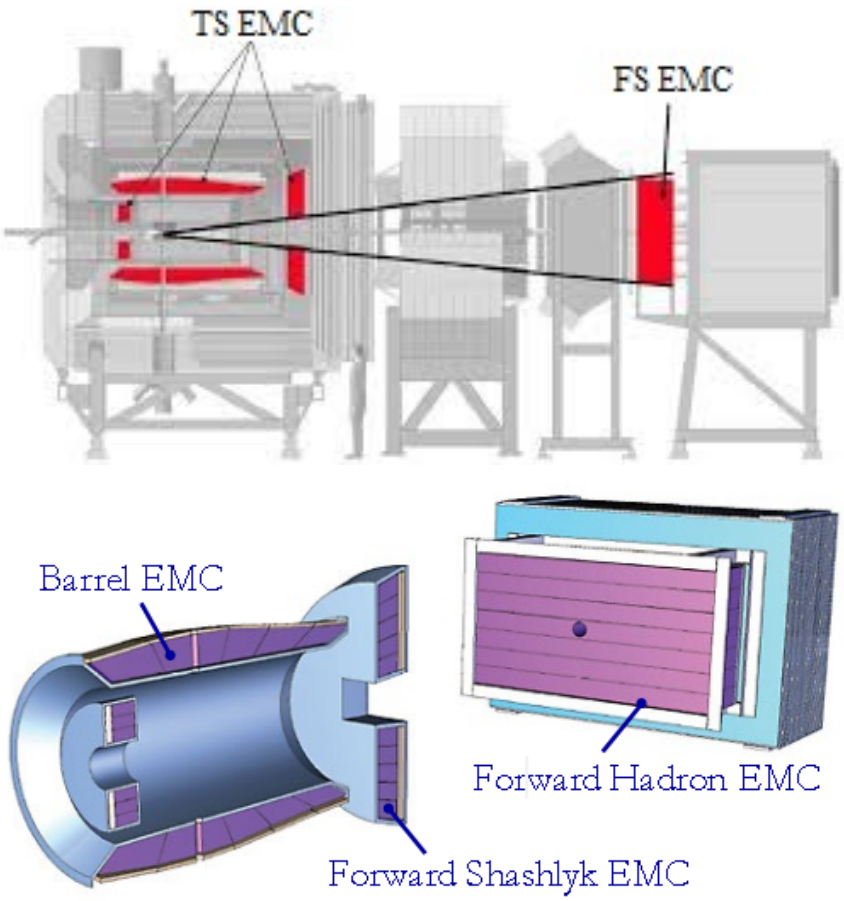


Figure 1.14: PANDA Detector schematic view. Target spectrometer calorimeter (TS EMC) and forward spectrometer calorimeter (FS EMC) are shown in red.

- *THE BARREL EMC & THE FORWARD EMC*

  The electromagnetic calorimeter (EMC), due to the high count rates expected, requires a fast scintillator material with a short radiation length and Molière radius. The EMC will provide measurements of photons with accurate energy, position and time with high resolution. Therefore, in order to achieve this sufficient resolution for photon, electron and hadron detection even at intermediates energies, the high density inorganic scintillator chosen was the lead-tungsten ($PbWO_4$). This material, the same used at CERN and thus efficiently optimized, will allow a compact setup due to its good energy resolution and fast response.

  The barrel EMC, shown in Figure 1.15, will be positioned behind the DIRC barrel inside the solenoid magnet. It has an inner radius of 57 cm and will

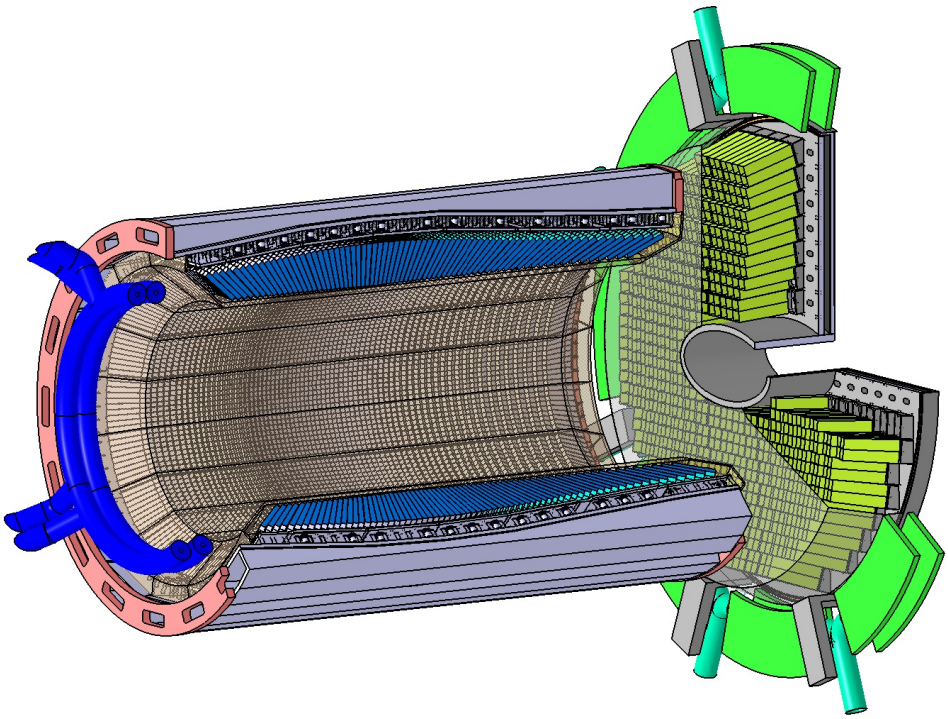


Figure 1.15: The Barrel EMC and the Forward EMC [9].

consist in 11,360 tapered crystals with a front size of 2.1 × 2.1 cm^2. Each crystal will be 20 cm long in order to achieve an energy resolution below 2%.

The forward end cap EMC and the backward end cap consist in a planar arrangement of 3,600 tapered crystals and 592 crystals, respectively.

The light yield of the whole system can be increased of about 4 compared to room temperature by cooling the crystals down to - 25 °C. With this configuration the EMC will provide a coverage of 96 % of the full solid angle and will allow a π/e^- discrimination of 10^3 for the momenta above 0.5 GeV/c [9].

- *THE SHASHLYK ELECTROMAGNETIC CALORIMETER*

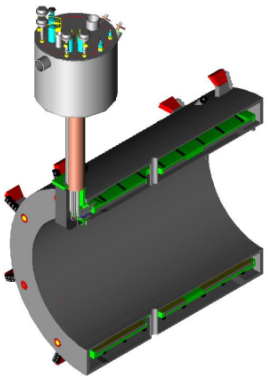
  The Shashlyk EMC will be located outside the target region, seven meters from the interaction point beside the dipole magnet. This subdetector will be employed for the detection of photons and electrons with high resolution and efficiency. The system is based on a lead-scintillator sandwiches read out with wavelength shifting fibers (WLS) passing through the block. The geometrical size constraints in the region where this EMC is located are not so strict as well as position resolution requirements thus it is possible to obtain a granularity of 10 cm × 10 cm employing 351 modules arranged in 13 rows and 27 columns. Each module will be 70 cm length, which correspond with a radiation depth of $20X_0$, and it will be divided into four channels of 55 mm × 55 mm size in order to achieve a higher spatial resolution.
  Using this technique an energy resolution of 4 % is expected [10] [9] .

1.3.4 *Magnet system*

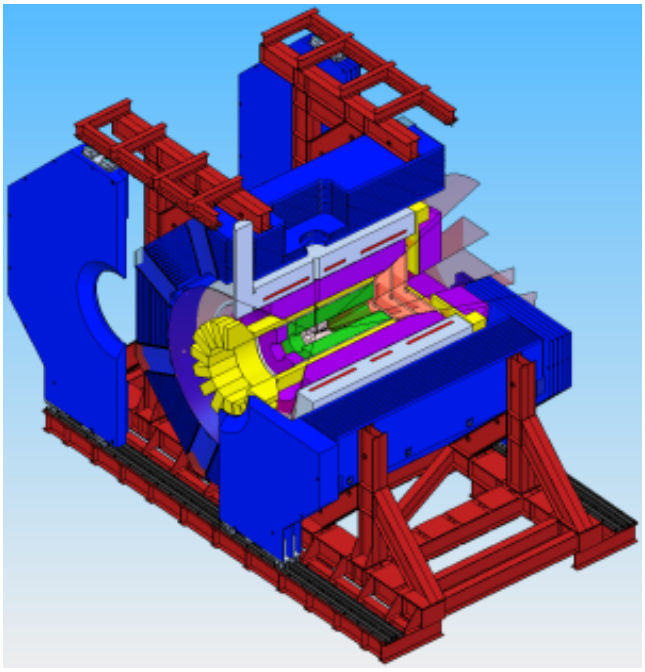
The Magnet System of PANDA is designed to provide an ideal combination of fields. This system, compulsory for the momentum reconstruction and for the particle identification, will be composed of two magnets. A brief description of these devices is given below.

- *SOLENOID MAGNET*

  Positioned in the Target Spectrometer, the solenoid magnet will deliver a homogeneous solenoid field of about 2Tm. The inner diameter of 1.9 m will be left free for the detector placement [6]. In Figure 1.16 is shown the magnet position in the TS.



(a) Solenoid magnet.



(b) Solenoid magnet in the target spectrometer.

Figure 1.16: View of the solenoid magnet (a) and its position in the target spectrometer (b).

In order to satisfy all the requirements for the field, this magnet is designed using a superconducting split coil which has a length of 2.8 m and a laminated yoke for the flux return. This design allows the allocation of the vertical target pipe, like shown in Figure 1.16, without sacrificing the homogenous field. The cryostat will surround all detectors and will serve as their mounting structure. The whole system weights about 300 t and it will be placed in a moveable platform for an easier maintenance.

- *DIPOLE MAGNET*

  The dipole magnet, the central part of the forward spectrometer, is used for reconstruction of charged particle tracks with a good momentum resolution. The dipole covers the entire angular acceptance of the target spectrometer of $\pm$ 10° and $\pm$ 5° in the horizontal and in the vertical direction, respectively. The device will provide a bending power of 2 Tm.
  In addition to these devices, also two correcting dipole magnets are foreseen around the $\overline{\text{P}}$ANDA detector system in order to compensate the beam deflection. The whole system weight is about 220 t and it has an aperture of 1 m $\times$ 3 m. The dipole is designed properly in order to operate fully synchronous with the High Energy Storage Ring (HESR). In Figure 1.17 is shown a view of the dipole magnet of $\overline{\text{P}}$ANDA [11].

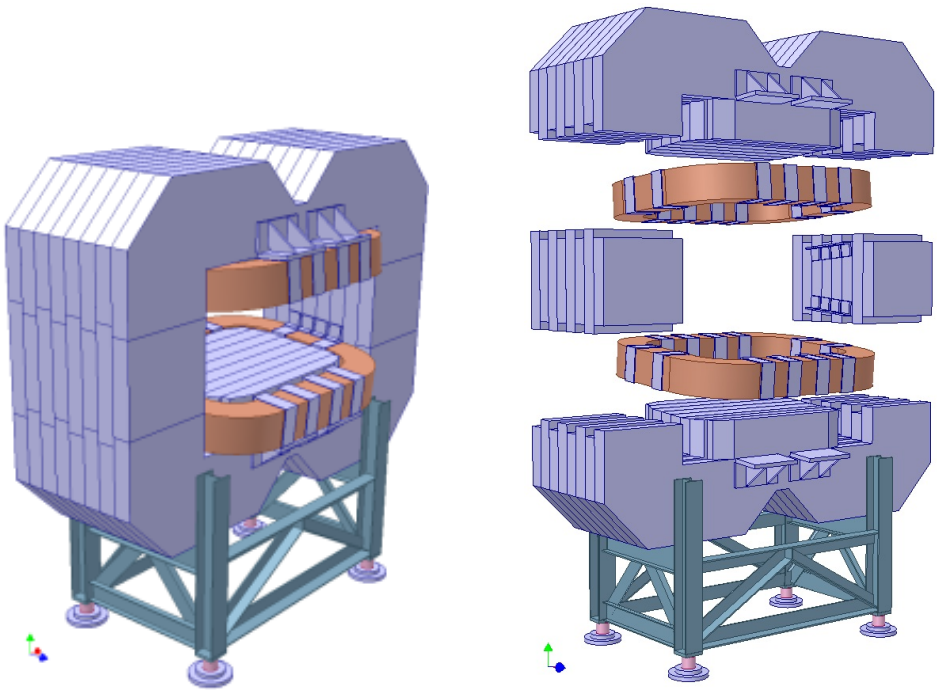


Figure 1.17: View of the dipole Magnet.

1.3.5 *Beam-Target system*

The Beam-Target system is composed of the devices used for the target production and for the vacuum generation necessary for the region close to the interaction point (IP). Like shown in Figure 1.18, the target and beam pipe cross sections are decreased until an inner diameter of 20 mm close to the IP. The planned materials to use for the innermost parts are mainly beryllium, titanium and suitable alloys.

Figure 1.18: View of the Target system in PANDA.

The constraints on the material budget and the limited space in the proximity of the IP impose to place the vacuum pumps outside the target spectrometer.

Moreover, depending on the experimental requirements, the target material can be of three different types: the cluster beam target, the pellet beam target and the fiber target. Therefore, the vacuum system will be feasible so that the operation with the different target types will be possible. To prevent the backscattering into the interaction region a dumping system of the target residuals after beam crossing is mandatory.

2

THE PANDA MICRO VERTEX DETECTOR

The Micro Vertex Detector (MVD) is the innermost subsystem of the $\overline{\text{P}}$ANDA apparatus. Located inside the solenoid magnet of the target spectrometer at 2.5 cm from the interaction point, this silicon tracking device will be used for the identification of the primary and secondary vertices which are important for the study of the weak decay of hadrons with charm or strange content.

Figure 2.1 shows the location of the MVD inside the target spectrometer.

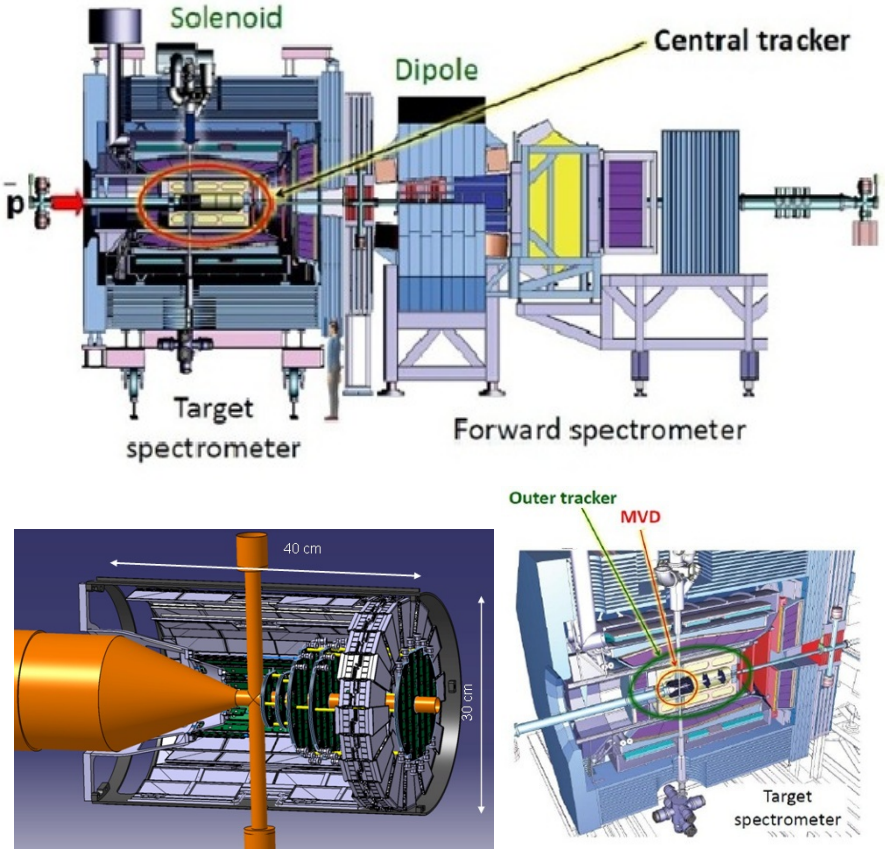


Figure 2.1: The Micro Vertex Detector in the Target Spectrometer [2].

A particular attention will be given to D mesons which are important for the investigation of the charmonium states. The tagging of these particles is achieved through the detection of their charged decay products and, due to their short decay length, it requires a spatial resolution less than 100 μm.

The detector will also allow to improve the momentum resolution on all tracks and will provide information for the identification of low momentum particles through dE/dx measurements.

2.1 THE REQUIREMENTS

The MVD is of central importance to cope with all the physics program of the $\overline{\text{P}}$ANDA experiment, thus a particular attention must be given to its design which must respect some requirements listed below:

- **Good space resolution:**

  The decay length ($c\tau$) of $D_s^{\pm}$ mesons is about 150 μm thus a spatial resolution of 100 μm, or possibly better, is compulsory in the bending plane. Also the spatial resolution in the perpendicular plane to the beam axis is important to obtain a good transverse momentum resolution.

- **Good time resolution:**

  The time resolution required for the reliability of the detector depends on the expected rate. The detector is designed to work with a maximum interaction rate of 2×10^7 events per second and thus a very good time resolution is mandatory to associate unambiguously each track with its parent interaction. The time resolution of the current design is down to 2 ns rms.

- **Adequate radiation hardness:**

  Due to the position close to the interaction point and to the high rate expected, the radiation hardness is an important parameter to analyze. All the sensors and the electronics components must have an adequate radiation tolerance to guarantee an enough life-time of the detector.

- **Triggerless read-out scheme:**

  This is one of the main properties which improve the apparatus flexibility. The triggerless concept implies an event selection based on the physics properties of detected particles, such as reconstructed invariant mass or a detected secondary vertex. To be compliant with the triggerless scheme, the chips should employ a free running architecture, in which all the events above a preset threshold are time-stamped and transmitted off-chip.

- **Compact geometry:**

  The detector is located inside the solenoid magnet so that the space available for the detector is restricted and a very compact geometry will be necessary for all the system. The current geometry foresees a diameter of 30 cm and a length of 46 cm in the beam direction.

- **Material budget:**

  The use of one additional track point improves a lot the performances of the tracking system, but it means that the particle is crossing another layer of material, loosing energy and making multiple scattering. Thus, in this detector it is really important to reach a correct trade-off between resolution and material budget. Therefore study the amount of material budget present inside the MVD and its influence on particles is mandatory for a correct design of the detector. .

2.2 THE TRIGGERLESS DATA ACQUISITION SYSTEM

The $\overline{\text{P}}$ANDA experiment will employ a novel data acquisition concept based on triggerless readout. This approach is necessary to manage the average number of 2×10^7 antiproton-proton annihilations/s expected during the experiment. In fact, the particular $\overline{\text{P}}$ANDA requirements lead to a new design of the readout chain from the front-end to the data acquisition: the readout will use a DAQ system operating without a hardware trigger signal while the front-end electronics will operate with a continuous data transmission.

The front-end will send the information to the Data Concentrators (DCs) during a given period of time. Then, when the SODA (Synchronization Of Data Acquisition) system sends a common reference time signal to all the DCs, they will combine all the collected data into time stamped messages which will be sent to the DAQ system. The DAQ architecture, depicted in Figure 2.2, has to be able to analyze the data collected and build messages, each with the same time tag to a simple output. At the output, the fragments from all the DCs will be pushed forward into two stage burst merging switching network based on Compute Nodes located in ATCA crates [12].

Using this architecture the concatenated fragments with the same time-stamp tag will be available for physics selection processing.

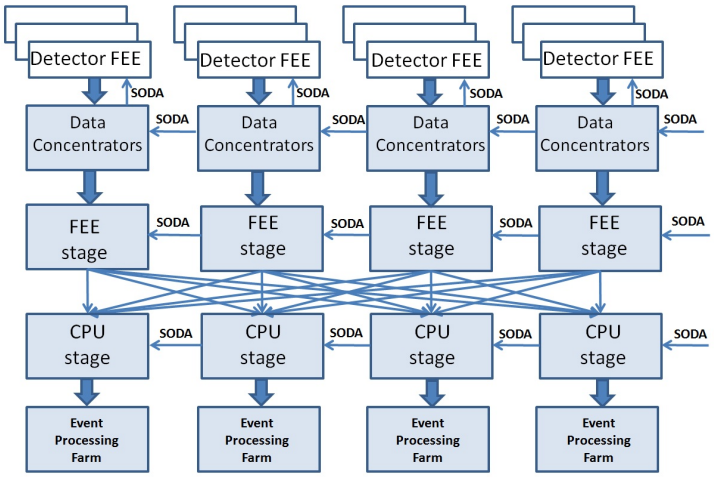


Figure 2.2: Triggerless system: the DAQ architecture.

2.3 SILICON SENSORS

A little general introduction about the silicon detectors is given before the description of the MVD in order to understand the design choices.

The silicon properties make of this material an optimal stuff for charged particle tracking detectors in high radiation environment under strong magnetic field. The silicon sensor consists in a reversed p-n junction, fully depleted by a high voltage ($\sim 10^2$ V). As shown in Figure 2.3, when a charged particle crosses this region it loses the part of its energy in the matter which starts the electron hole pairs generation. Thanks to the high mobility of both these charge carriers in silicon, a very fast collection time is possible ($\sim$ 10 ns).

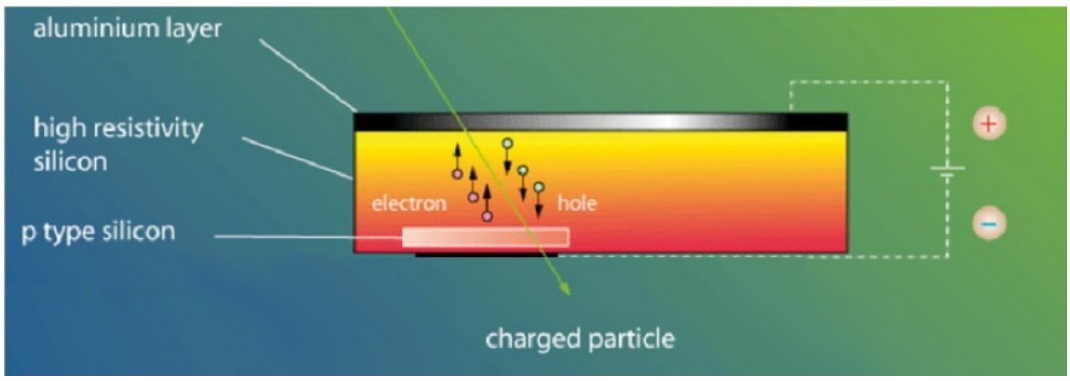


Figure 2.3: P-N junction and the hole pairs generation.

Silicon is successfully employed for tracking detectors because it allows a very high degree of miniaturization with a segmentation density larger of three orders of magnitude than the gaseous detectors. Moreover, not less important, is the very good reproducibility in big quantities limiting the costs. Due to these properties they perfectly meet the requirements imposed on the MVD.

The two different sensors foreseen for the MVD are hybrid pixel detectors and Double Sided Silicon Detectors which are based on different technologies and thus these sensors will be discussed separately in the following paragraphs.

2.3.1 *Hybrid Pixel Detectors*

Hybrid pixel detectors, thanks to their good radiation tolerance and their intrinsic good spatial resolution, are an optimal solution for the regions near to the interaction point where the expected rate of particles is very high. The use of this kind of detector in fact, allows to identify particles unambiguously also with high rates but at the price of using a very high number of channels to cover the surface.

The design of systems based on hybrid pixel detectors has been consolidated in LHC experiments like ALICE, ATLAS and CMS, however the $\overline{\text{P}}$ANDA constraints required the use of a dedicated solution.

In $\overline{\text{P}}$ANDA in fact, it is necessary a triggerless system and so a hardware able to perform a continuous readout. For this reason a front-end ASIC (Application

Specific Integrated Circuits), which was developed in a CMOS 0.13 µm technology, is used for the readout of the pixel sensors. This custom front-end, called Topix, will be discussed in Chapter 3.

In addition to the triggerless constraint, since the material budget must be reduced, the electronics and sensors must be thinned as much as possible.

The following figure shows a schematic view of the hybrid pixels used for the Micro Vertex Detector.

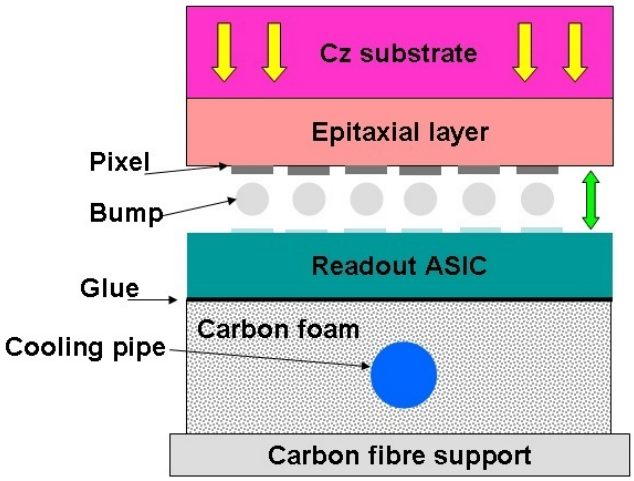


Figure 2.4: Hybrid pixels assembly for the $\overline{\text{P}}$ANDA experiment [2].

The sensor consists of a matrix of reverse biased silicon diodes flip-chip bonded to several readout chips. The diodes are obtained growing an epitaxial silicon layer on a silicon Czochraski substrate which is then almost completely removed. Each cell on the sensor matrix is then, like shown in Figure 2.4, connected by bump bonding technique to the corresponding readout cell of a custom ASIC properly developed in CMOS 0.13 µm technology. To make this connection possible the readout cell must fit into the same area as the pixel sensitive element. Then the whole assembly is glued to a carbon foam layer to improve the heat dissipation towards the cooling pipe. The mechanical support is made of a structure of carbon with a suitable shape [2].

After a dedicated R&D effort an elementary cell size of 100 µm x 100 µm x 100 µm with a resistivity of 2 kΩ·cm has been chosen as the optimal compromise, combining a good space resolution with acceptable performance towards the end of the experiment [13]. After ten years, which is considered the experiment lifetime, for pixels with this geometry is expected a leakage current of 60 nA, that can be tolerated because the charge collection efficiency should still allow the detection of minimum ionizing particles.
Moreover, the power consumption will be reduced thanks to the use of the CMOS 0.13 µm technology and thus it will be possible a simplification of the cooling system.

The pixel part of the MVD will contain in total about 10 million independent channels which will give, in addition to the two-dimensional spatial information, also the time and energy loss of every hit.

2.3.2 *The Double-Sided Silicon Microstrip Detectors*

The Double-Sided Silicon Detectors (DSSDs), based on the double sided technology, are produced on FZ wafers. The layout of DSSD foreseen in $\overline{\text{P}}$ANDA is shown in Figure 2.5. The strips, realized in p^+type silicon on the front side and in n^+type silicon on the other side, are arranged in rows and columns in order to obtain a two dimensional information. In the foreseen configuration for this detectors the resolution in one dimension is defined by the strip pitch.

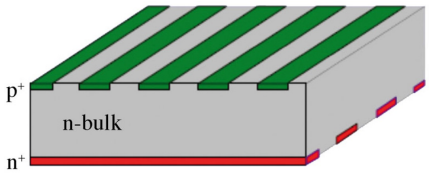


Figure 2.5: Layout of the DSSDs.

Silicon strip detectors have a good spatial resolution and a low material budget, but unfortunately they cannot handle unambiguously very high rates of particle and so they cannot be used where a high rate is expected like the region close the interaction point. This limit is caused by the method employed in the hit identification. In fact, like shown in Figure 2.6, when a single particle hits the sensor the first layer gives the coordinates x_1 and the second layer gives the coordinate y_1 identifying correctly the hit number 1. While when two particles hit the sensor the first layer gives the coordinate x_1 and x_2 and the second layer gives the coordinates y_1 and y_2. In this case, where the particles arrive simultaneously, is not possible to identify correctly the two hits because also the coordinates (x_1, y_2) and (x_2, y_1) could be possible. These two additional hits are called ghost hits.

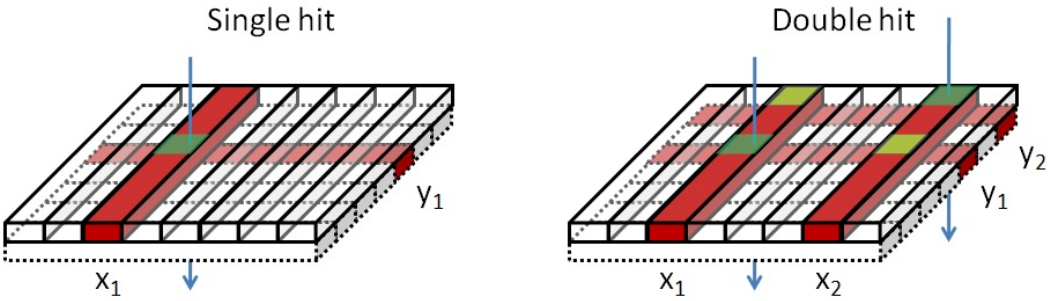


Figure 2.6: Ghost hit effect with a double hit in DSSDs.

Nevertheless, strips could be efficiently employed in regions with a low hit rate and moreover, make possible the reduction of the number of readout channels reducing also the material budget. In fact, if $N_{pixel} = \frac{A}{w^2}$ pixels readout channels are required to cover an area A with a spatial resolution w, using $N_{strip} = 2\sqrt{N_{pixels}}$ strip readout channels, it is possible to cover the same area and with the same resolution [14]. More specific details about the strips used in the MVD will be given in the next paragraph.

2.4 THE MVD DESIGN

The MVD, located inside the solenoid magnet of the $\overline{\text{P}}$ANDA target spectrometer, is divided into a barrel and a forward part. A schematic picture of the MVD layers is shown in Figure 2.7.
The detector is composed of four barrel layers and six forward disks arranged perpendicularly to the beam in order to achieve the best acceptance for the forward part. The layer structure is equipped with silicon hybrid pixels detectors or double sided silicon micro strips according to their position and covers a polar angle between 9° and 145°.

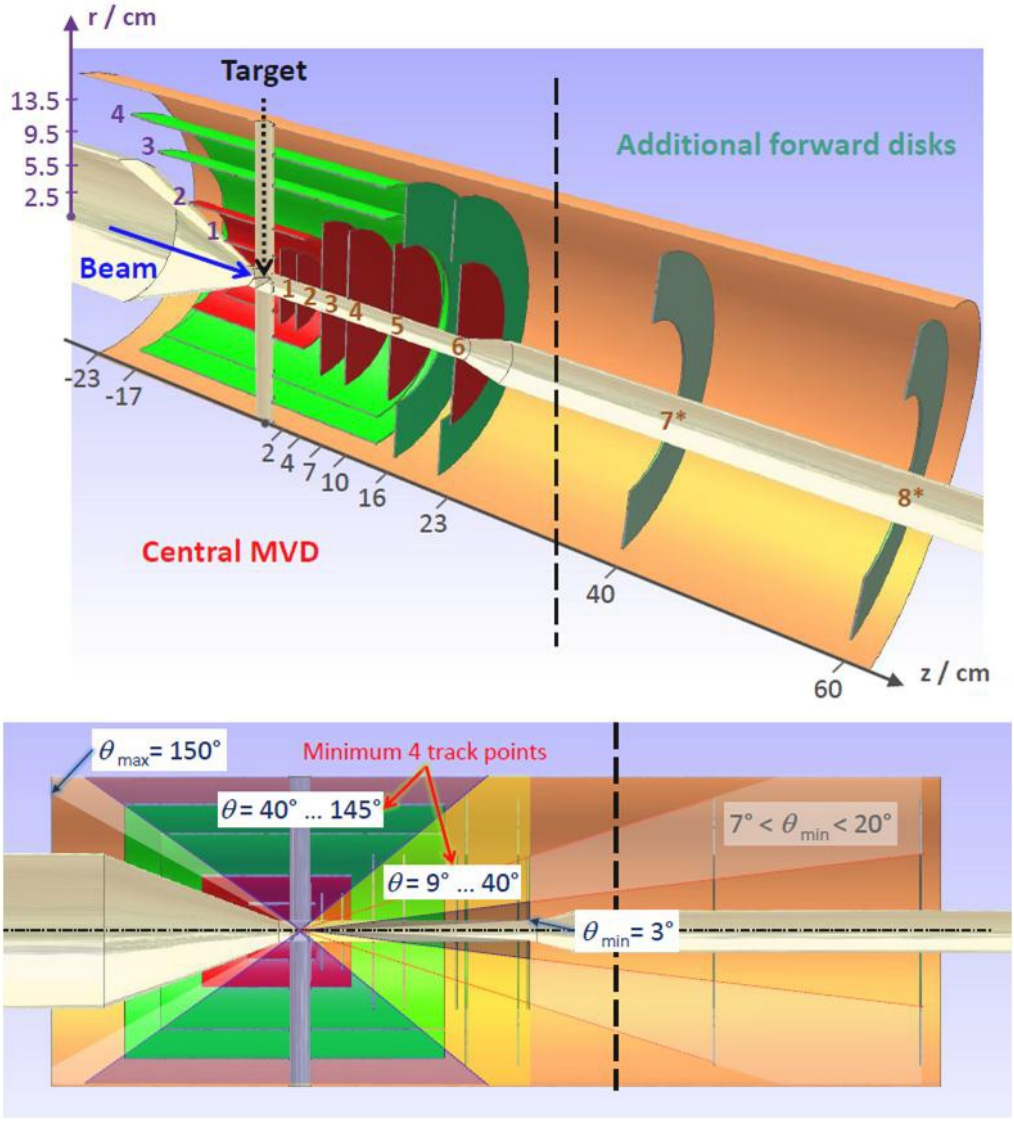


Figure 2.7: Layout of the MVD. The red inner parts use hybrid pixel sensors while the green parts use DSSDs micro-strip. Bottom: Side view along the beam axis illustrating the polar angle coverage. The barrel and the forward part meet at a polar angle of θ=40° [2].

The radii of the innermost and the outmost barrel layer are set to 2.5 cm and 13.5 cm respectively while the two intermediate barrel layers are arranged in increasing order. The barrel part covers polar angles between 40° and 150° while the disks in forward direction allow the measurements at small polar angles between 3° and 40°. The innermost disk is located at 2 cm from the interaction point and it has an interspacing of 2 cm to the second disk. These two first disks have the same radii and are located inside the second barrel layer. Located further downstream there are the other four disks which have a bigger radii. The first two of them are positioned inside the third barrel layer while the last two are outside the barrel layers. In addition to the disks, in order to achieve a better acceptance of hyperon cascades, two additional silicon disk layers are considered further downstream at around 40 cm and 60 cm.

Based on the detectors type used in the layers is possible to divide the MVD in two parts: the silicon pixel part and the silicon strip part.

The silicon pixel part of the Micro Vertex Detector is the region highlighted in red in Figure 2.7, and it is composed of the two innermost barrel layers and of the six forward disks. These layers are the most important ones for determining primary and secondary vertices of charm mesons.
In the region where these layers are located a high hit rate is expected thus the detectors must be able to transmit very high data rates due to the untriggered readout. For this part is also required a very high precision and granularity. In addition, since these layers are exposed to relatively high radiation also an adequate radition hardness is mandatory. To cope with all these requirements a hybrid silicon pixel detector appears to be the best solution for this part of the MVD.

Concerning the silicon strip part of the MVD, it is composed of the barrels and the forward disks highlighted in green in Figure 2.7. In these layers is possible to employ the Double-Sided silicon detectors because the hit rate expected is not so high and thus the probability to have ghost hits is low. The use of DSSDs simplifies the readout of a much larger area with significantly fewer channels. In the current MVD design are foreseen 254 strip modules which will be better described in the next paragraph.

2.4.1 *The sensor Geometry*

The structure of the MVD is based on a module concept where the silicon sensors represents the lowest level. The detector module is defined as the smallest functional unit which is electronically independent. The schematic layers shown in Figure 2.8 must be approximated by an arrangement of these individual detector modules. The sensor dimensions and the sensor positions chosen for the different parts of the MVD result from an explicit design optimization which takes into account some technical aspects.

The pixel design is based on a quadratic pixel cell size of 100 µm × 100 µm which is used like elementary unit to make the main module. It contains 116 columns and 110 rows of pixels covering an area of approximately 1.3 cm^2. This module allows to build the four different pixel sensors shown in Figure 2.8 on the left. All of them have a rectangular shape and the same height but their length is different.
An optimal coverage of both the barrel and the forward regions can be reached by using these modules which are readout respectively by two, four, five and six chips.

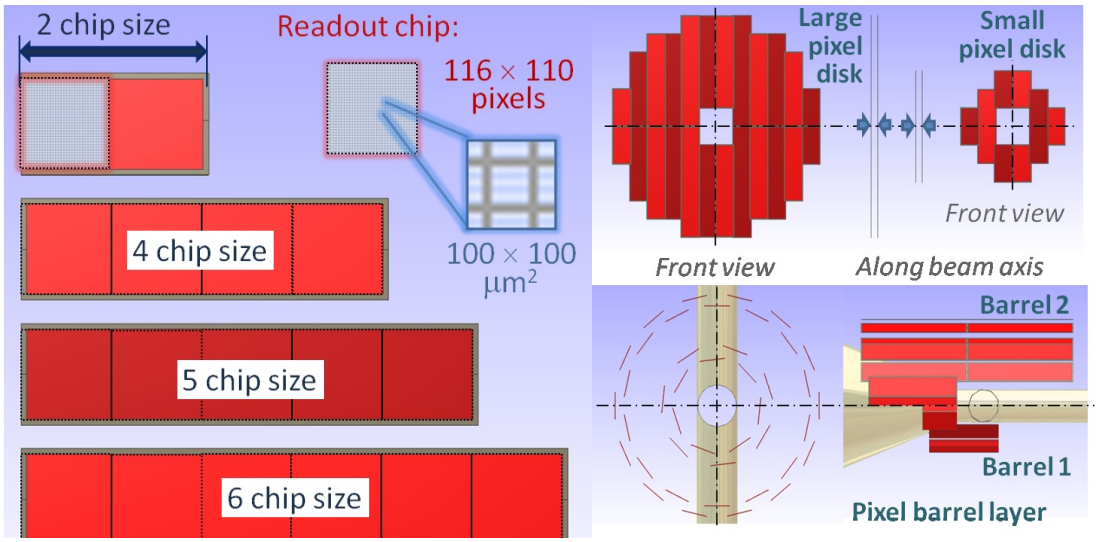


Figure 2.8: Left: The pixel sensors employed in the MVD layers. Right: The pixel sensor arrangement in different detector layers.

In the same Figure (on the right) is shown the basic geometry for the pixel sensor arrangement. The forward disks layers consist of an adequate configuration of the four modules described previously. The modules appear aligned in rows with a small interspace along the beam axis. The Figure 2.8 shows also the barrel layers which are composed of a double-ring arrangement of the four modules in order to achieve sufficient radial overlap.

For the silicon strips detectors unlike the pixel detectors, there isn't the constraint due to the readout chip size on the dimension of the sensor segmentation thus the

strip design is more feasible. The basic design of the MVD foresees DSSDs of three different geometries shown in Figure 2.9 and described below:

- Rectangular or squared sensors: Used for the barrel part, these sensors feature a stereo angle of 90°. The pitch for these sensors is set to 130 µm.
- Trapezoidal sensors: They are used for the peripherical region of the forward disks and feature a stereo angle of 15° in order to place the strips parallel to the sensor edge. The pitch chosen for this geometry is 70 µm.

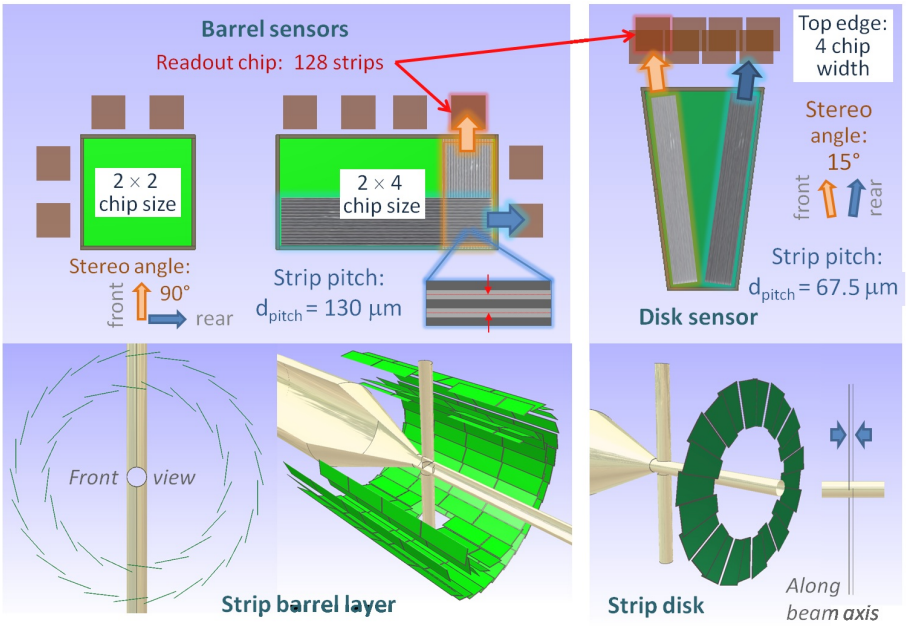


Figure 2.9: Sensor geometry for the MVS strip part. Top: The sensor types employed for the MVD. Bottom: The sensor arrangement in the layers. [2]

The complete detector will contain about 10 million pixel channels and 200000 strips. Figure 2.10 and Figure 2.11 list the compilation design parameters for the MVD and the position of the sensors in the different layers.

Basic parameter	Pixel part	Strip part
Number of super-modules	66	70
Number of detector modules	176	140
Number of sensors	34 (2 chips size) 28 (4 chips size) 54 (5 chips size) 60 (6 chips size)	172 (rectangular) 34 (squared) 48 (trapezoidal)
Total:	176	254
Active silicon area / [m^2]	0.106	0.494
Number of front-end chips	338 (barrels) 472 (disks)	940 (barrels) 384 (disks)
Total:	810	1324
Number of readout channels	$\approx 10.3 \cdot 10^6$	$\approx 1.7 \cdot 10^5$

Figure 2.10: Modules employed for the pixel and strip parts [2].

Main layer	Sub-layer	$\langle r_{def} \rangle$ [mm]	$\langle r_{opt} \rangle$ [mm]	r_{min} [mm]	r_{max} [mm]	$\langle z_{def} \rangle$ [mm]	$\langle z_{opt} \rangle$ [mm]	z_{min} [mm]	z_{max} [mm]
Barrel layer 1	Inner ring Outer ring	25	22 28	21.80 27.80	22.75 28.58	-	-	−39.8	9.8
Barrel layer 2	Inner ring Outer ring	50	47.5 52.5	47.30 52.30	47.85 52.82	-	-	−79.8	57.8
Barrel layer 3		95	92	89.72	96.86	-	-	−133.8	139.0
Barrel layer 4		135	125	123.20	129.24	-	-	−169.2	139.0
Disk layer 1	Sdk 1, front Sdk 1, rear	< 50	-	11.70	36.56	20	22	19.7 24.1	19.9 24.3
Disk layer 2	Sdk 1, front Sdk 2, rear	< 50	-	11.70	36.56	40	42	39.7 44.1	39.9 44.3
Disk layer 3	Ldk 1, front Ldk 1, rear	< 95	-	11.70	73.96	70	72	69.7 74.1	69.9 74.3
Disk layer 4	Ldk 2, front Ldk 2, rear	< 95	-	11.70	73.96	100	102	99.7 104.1	99.9 104.3

Disk layer 5	Ldk 3, front
	Ldk 3, rear
	StripDk 1, L
	StripDk 1, S
		-
		
		-
		
			-
			
			-
			
				11.70
				
				74.33
				
					73.96
					
					131.15
					
						160
						
							150
							
							162.5
							
								147.7
								152.1
								160.0
								165.0
									147.9
									152.3
									160.3
									165.3

Disk layer 6	Ldk 4, front
	Ldk 4, rear
	StripDk 2, S
	StripDk 2, L
		-
		
		-
		
			-
			
			-
			
				11.70
				
				74.33
				
					73.96
					
					131.15
					
						230
						
							220
							
							207.5
							
								217.7
								222.1
								204.7
								209.7
									217.9
									222.3
									205.0
									210.0

Figure 2.11: Positions and design parameters of the active sensor volumes within the different detector layers [2].

2.4.2 *The Mechanics and the cooling system*

Since the MVD will operate at room temperature of about +25° , both for pixels and strips, an active cooling system is required for a long term stability of the detector. Therefore the cooling pipes, together with other service structures must be brought from outside close to the detector in order to allow the sensor supply and the data transmissions. The limitations given by the stringent boundary conditions are shown in Figure 2.12.

Due to the fixed target setup, the access to the MVD is possible only from the upstream direction. In fact, the downstream region is occupied by the forward spectrometer. Moreover, also the downstream access is limited caused by the conic expansion of the pipe and this leads to inhomogeneities in the material budget distribution. For these reasons the service layout chosen concentrates most of the material where it is less harmful for the physics performance. Moreover, the use of Aluminium-Kapton cables for power supply distribution and signal transmission in addition to a light-mass cooling system allows to keep the average material budget of the full MVD below 8%.

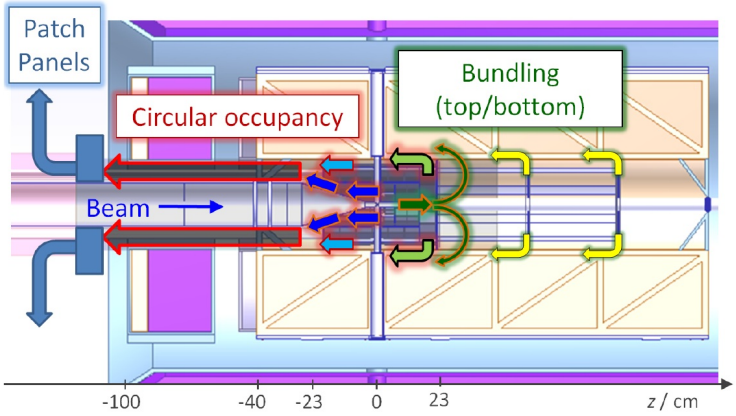


Figure 2.12: Schematic routing for the MVD. The blue and green arrows illustrate the concept used for the barrel and forward region, respectively. With yellow arrows are indicated the probable routing of the additional forward disks which could interfere with the MVD volume.

In Figure 2.13 is shown the global support structure which is composed of two half frames mechanically independent. They allow the mounting of all detector half layers and the attachment of the central frame. All the sensors are supported by a light weight carbon fiber structure and the interconnections are realized using low mass flex cables [2][3][15].

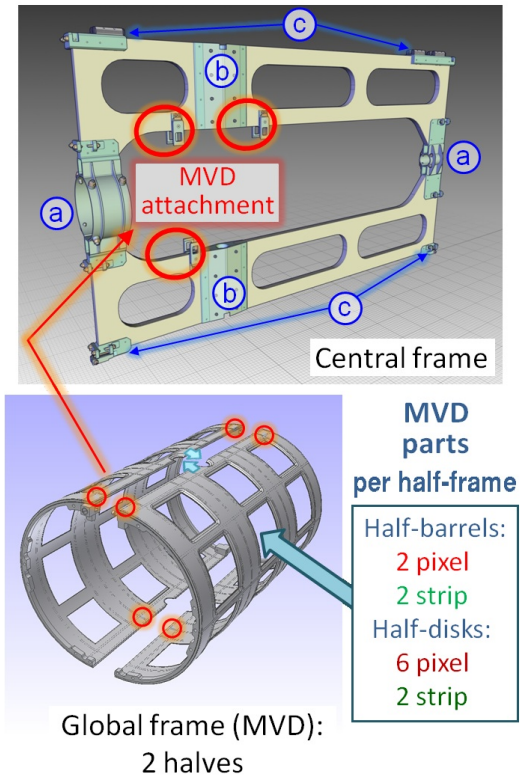


Figure 2.13: Detector integration of the MVD. Left: Three-point fixation to the central frame which also provides fixation points for the beam pipe (a), the target pipe (b) and the connection to a rail system (c).

3

THE FRONT-END ELECTRONICS ASIC

An Application Specific Integrated Circuit, or simply ASIC, is an Integrated Circuit (IC) customized for a particular application. In recent years several radiation tolerant customized ICs were realized for High Energy Physics (HEP) experiments such as ALICE, ATLAS and CMS at the Large Hadron Collider (LHC) at CERN. However, due to its unique requirements, mainly related to the absence of a trigger signal, for the $\overline{\text{P}}$ANDA experiment it is necessary the development of a specific custom readout ASIC for the hybrid pixel sensors.

The technology employed to develop the ASIC is a commercial deep sub-micron CMOS 0.13 µm which, like all the deep sub-micron technologies with a very thin gate oxide and Shallow Trench Insulation (STI), has the potential to withstand high levels of Total Ionizing Dose (TID) using standard layout techniques [16]. In addition to the good radiation hardness, this technology offers also a much higher integration density respect to other technologies. In order to obtain a robust system, the ASIC is designed in the way that the information is sent out from the device digitally. Therefore the ASIC design is based on a mixed signal approach which foresees analogue signals and digital signals in the same monolithic system.

In this chapter the more important requirements of ToPix and the readout architecture are described. The blocks that form the front-end are presented using a high level description. More specific information about the transistor implementation is given in Chapter 4 and Chapter 5. The ASIC operation, with particular regard to the Time over Threshold (ToT) technique which is used for the digitization, is explained. Moreover at the end of the chapter is foreseen a description of the three prototypes developed until now with a discussion about the results obtained from tests.

More details can be found in the Technical Design Report for the $\overline{\text{P}}$ANDA Micro Vertex Detector [2].

3.1 REQUIREMENTS OF THE READOUT

The proximity of the MVD to the interaction point and the $\overline{\text{P}}$ANDA radiation environment are two fundamental parameters which are very influential for the pixel readout requirements.

The custom ASIC, especially developed for the $\overline{\text{P}}$ANDA experiment, has to provide position, time stamp and energy loss measurements for every hit. In order to achieve a correct track reconstruction a high granularity, is requested. This requirement leads to minimize the pixel size but with this reduction the perimeter to area ratio increases and consequently also the input capacitance. For this reason many simulations were made to find the optimal trade-off and the results indicate a pixel size of 100 µm × 100 µm as the best solution.

The pixel detector is based on a modular concept as explained in the previous chapter. Figure 3.1 shows the whole wafer employed for the full size prototype sensors. As shown in the figure, the wafer contains an arrangement of 1, 2, 4, 5 and 6 readout chips together with some diagnostic structures. The vertical bars on the modules correspond to two columns with a pixel size of 100 µm × 300 µm and they represent the border between two different readout chips.

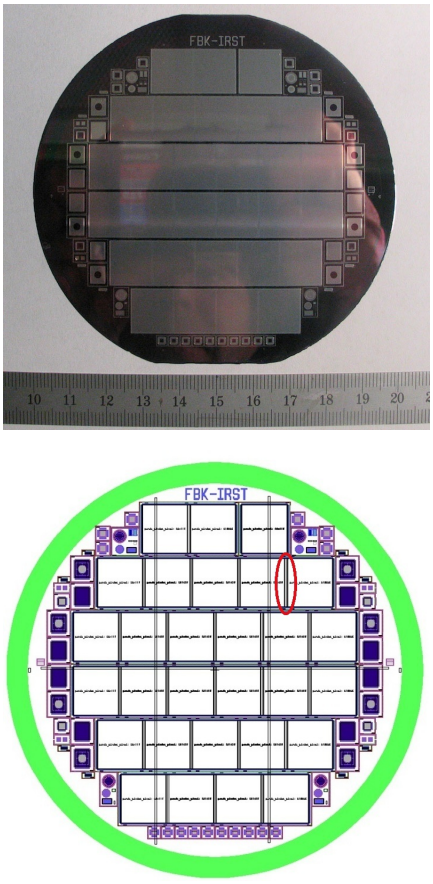


Figure 3.1: The wafer used for the sensors prototype. In red is indicated the boundary region with larger pixels [17].

Figure 3.2 is a zoom of the last image where it is possible to observe the pixel sensor arrangement in each module. It is also possible to see at one corner of every pixel the pad used for bump bonding which follows a mirror configuration with respect to the bus serving two pixel columns.

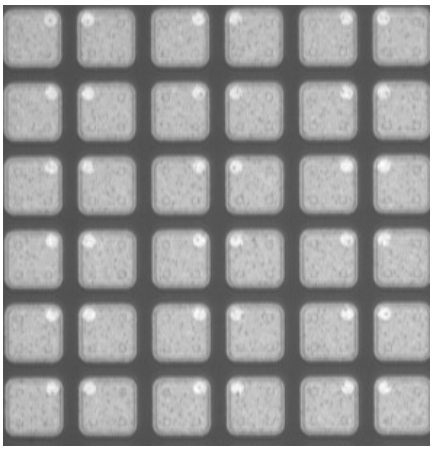


Figure 3.2: Picture of the pixel matrix.

To cover the whole region of the barrel and the disk layers a minimum of 34 wafers, all with the design of Figure 3.1, has to be produced. The number of needed sensors for the different layers of the MVD is briefly summarized in Table 3.1.

SENSOR NUMBERS					
	S2	**S4**	**S5**	**S6**	**Total**
Barrel 1	6	8	0	0	14
Barrel 2	0	0	6	44	50
Disk 1	6	2	0	0	8
Disk 2	6	2	0	0	8
Disk 3	4	4	12	4	24
Disk 4	4	4	12	4	24
Disk 5	4	4	12	4	24
Disk 6	4	4	12	4	24
Total	34	28	54	60	176

Table 3.1: The sensors employed to build the sensitive area of the MVD. The S number corresponds to the number of readout chips contained in the modules employed [2].

Since each hybrid pixel sensor is obtained connecting the pixel sensor to the readout cell via bump bonding technique, the readout cell matrix has to respect the same geometry as the pixel sensor matrix. The pixel matrix is realized using pixels with a size of 100 μm × 100 μm which are arranged in a configuration of 110 columns each composed of 116 pixel cells covering a total area of 11.4 mm × 11.6 mm. Every pixel has to transmit only digital information and therefore time and charge digitization has to be preformed at the pixel level. This impose the use of a mixed signal electronics for the readout system of each pixel.

In the experiment it is foreseen to employ p-in-n epitaxial silicon sensors which have optimal features but in order to have a backup solution, such as the well known n-in-n sensor employed in LHC, the front-end has to be designed to be compatible also with this second polarity.

The sensor chosen has a thickness of 100 μm in order to cope with the limited material budget. The average ionization expected in a sensor with this geometry goes from a Minimum Ionizing Particle (MIP) of 1.3 fC up to 50 fC.

The front-end is designed to tolerate a power density of up to W/cm^2 so that, due to high pixel density of about 10^4 cm^{-2}, a limit of 15 μW has been put on the power consumption of the analogue pixel cell. Concerning the noise, it is a function of the bias current because, as will be explained later, it is mainly limited by the input transistor thermal noise. An Equivalent Noise Charge (ENC) of ~ 200 e$^-$ has been chosen as a good trade-off between minimum detectable charge and power consumption of the ASIC.

The choice of the master clock aims at reusing buildings blocks derived by the present trigger system of the COMPASS experiment; therefore the particular value of 155.52 MHz is foreseen [14].

Concerning the time resolution requirement, it is linked to the average hit rate expected which has a magnitude of 2×10^7 events/s. Simulations estimate that to tag correctly the events from the collision rate expected the time resolution has to be below 10 ns. Hence the time resolution LSB chosen for the ASIC is 6.45 ns [18].

Since the readout electronics has to work in the $\overline{\text{P}}$ANDA radiation environment the energy deposited in the medium by ionizing radiation is an important parameter to consider. Simulations estimate a TID, that is the measure of this energy per unit mass, of 100 kGy in 10 years which should be the life-time of the experiment. Therefore an important requirement for the ASIC is a tolerance to this value of radiation dose [15].

Moreover in order to allow a correct particle identification with an average value of 10^3 events per second on a single pixel, the system must be self-triggered and all the particles above a given threshold have to be readout, leading to a high data rate.

All the requirements described until now are summarized in Table 3.2 .

SPECIFICATION FOR THE ASIC	
Measurements	Hit position Energy Loss Hit time stamp
Pixel Size	100 μm × 100 μm
Chip active area	11.4 mm × 11.6 mm 116 rows and 110 columns
Chip size	11.6 mm and 14.8 mm
Time/charge digitization	At pixel level
Trigger	Self triggering
Input Polarity	Selectable
dE/dx measurement Energy loss measurement	ToT 12 bits resolution 7 bits linearity
Input range Noise floor Noise Level	up to 50 fC 0.032 fC 200 e- rms
Clock frequency	155.52 MHz
Time resolution LSB	6.45 ns (1.9 ns r.m.s.)
Power consumption	< 20 μW
Max event rate/cm^2 Max data rate/chip	6.1×10^6 Hits/s ~ 250 Mbit/s
Total ionizing dose	⩽ 100 kGy

Table 3.2: Specifications for the front end ASIC.

3.1.1 *The Readout ASIC*

The readout ASIC architecture of the pixel cell can be divided in the two sections analogue and digital. The block structure of these two parts are depicted in Figure 3.3 and 3.4.

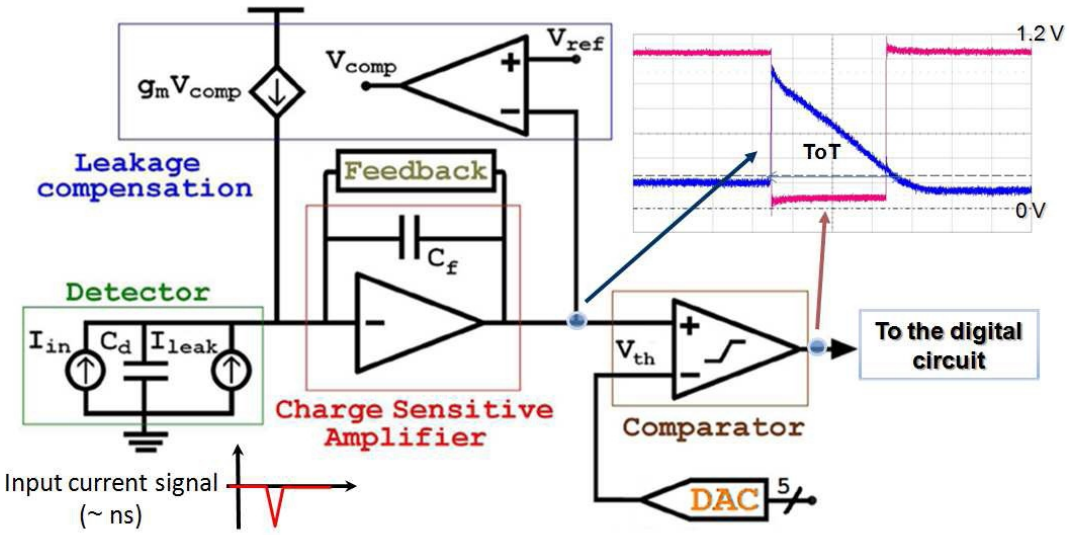


Figure 3.3: Analogue part of the ASIC architecture. The signal in blue color is the preamplifier output while the signal in red color is the comparator output which is sent directly to the digital part of the architecture [14].

The analogue part, contained in every pixel cell, consists in a block structure which allows to manage the input signal received from the detector in order to create the digital signal that is then processed in the digital part of the architecture. These blocks form the front-end and have the function of extracting the important informations contained in each particle hit.

The main blocks of the front-end are the following:

- **The detector**
  This is the sensitive block of the ASIC which detects the particle hits and creates the analogue signal that must be processed. The detector is connected directly to the input amplifier that can be configured to accept signals of both polarities via control bits. The signal that comes out from this block appears like a delta shape signal as depicted in red color in Figure 3.3.

- **The Charge Sensitive Amplifier (CSA)**
  The CSA consists in a direct cascode amplifier which is connected to a feedback capacitance and to a constant current discharge circuit. The feedback capacitance fixes the charge gain which is $1/C_{FB}$. This means that increasing the C_{FB} the gain decreases while decreasing C_{FB} decreases the loop stability. Therefore the chosen value has to be an adequate trade-off between these conditions.

- **The Discriminator**
  The discriminator design employs a folded cascode architecture following a low-voltage approach. It allows to get a signal which contains the information about the comparison of the two input values. The inputs of this block are the preamplifier output voltage and the threshold voltage which is first set through a global DAC and then fine adjusted using a local five bits DAC. The DAC can sink or source current to a low impedance node of the comparator. This operation allows to modify the voltage threshold in a magnitude set by an external component on the PCB as explained in Chapter 4.

  The output of the discriminator is digital and therefore it is sent directly to the digital part of the ASIC.

- **The baseline holder and the costant current feedback**
  This block implements the baseline restorer and it consists of a low pass filter stage in feedback with the input stage. This specific feedback network analyses the difference between the baseline reference voltage V_{REF} and the CSA output V_{CSA}. The operation is based on a differential pair biased by a current source. When the condition $V_{REF} = V_{CSA}$ is satisfied the current in the two branches has the same value. If a negative current signal is present at the CSA input, V_{CSA} increases thus switching off one of the two branches changing the output of the block.

  The output of the filter controls the gate of a PMOS transistor which generates the current compensation by forcing the stage DC output value to a reference voltage. A good constant discharge is achieved only when V_{CSA} is sufficiently large to fully steer the current from one branch to the other of the differential pair.

The digital part architecture, partially depicted in Figure 3.4, contains the blocks used to manage the informations obtained by the analogue part. The part depicted in Figure 3.4, with the exception of the buses, is contained in each pixel and allows to store in the adequate registers the pieces of information obtained. These pieces of information are then put on the buses which allow to transfer data to other blocks of the architecture. Figure 3.5 shows the remaining part of the digital logic which allow to collect the data obtained from columns and store them in a FIFO. The complete readout architecture and the role of every block will be explained in the next paragraph.

Following is given a brief description of the main digital blocks.

- **Configuration register**
  This 12 bit register contains the data used to mask the comparator output, to set the value of the DAC used to tune the voltage threshold and to program other relevant features on the chip.

- **Leading edge register**
  The Leading edge register consists of a 12 bit register used to save the time stamp relative to the instant in which the comparator switches from 0 to 1. This value gives the time information.

- **Trailing edge register**
  This 12 bit register contains the time stamp relative to the instant in which the comparator switches back to 0. Using this value together to the value contained in the leading register is possible to obtain the ToT and thus the energy information.

- **Time stamp buses:**
  They are 12 bit buses which are shared by two adjacent columns in every pixel cell. These buses are used to send the time information to the digital storage cells. In order to reduce the power consumption each time stamp bus uses a reduced swing pseudo differential logic with pre-emphasis which generates an intentional alteration of the amplitude of the signal. In order to reduce the switching noise and to avoid synchronization problems with the asynchronous pixel logic, the data are sent on this bus with a Gray encoding scheme.

- **Data buses:**
  They consist of 12 pseudo differential lines used for carrying the data obtained from each pixel. As the time stamp bus, also this kind of bus uses a logic with pre-emphasis and a Gray encoding.

- **Address buses:**
  Also these buses are pseudo differential lines and they are used to send the pixel address information. In order to keep the cell output drivers to a manageable power consumption and size, these buses together to the data buses, are read out at the end of the column via sense amplifiers.

- **The Columns Readout Control Unit (CRCU):**
  The CRCU is the control system of each double columns. Each CRCU is composed of a bank of sense amplifiers used for the data readout, a bank of differential drivers used for the time stamp, the control logic and a 32 cells output FIFO. In total 55 CRCUs are necessary to control the 110 columns of the ASIC.

- **The Chip Controller Unit (CCU):**
  The CCU is the controller of the ASIC readout. It reads the data from CRCUs and multiplexed them to up to 3 double data rate serial links.

- **The FIFO:**
  In this 32 bit $\times$ 32 bit memory, based on the method "First In, Firs Out", are stored the data read-out from the pixel column.

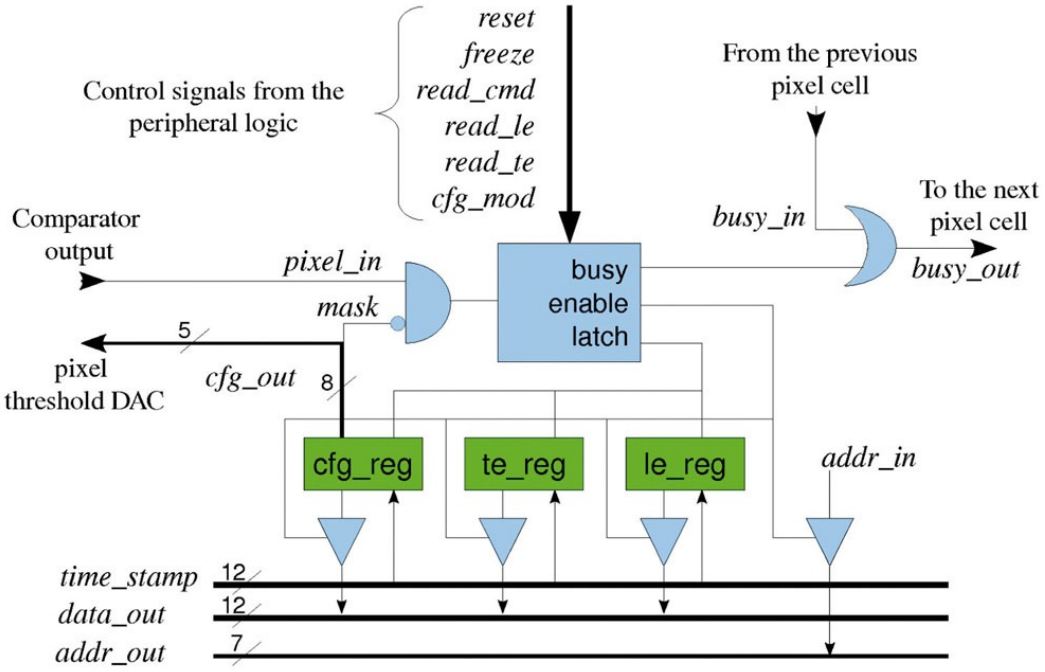


Figure 3.4: Digital part of the ASIC architecture contained in each pixel.

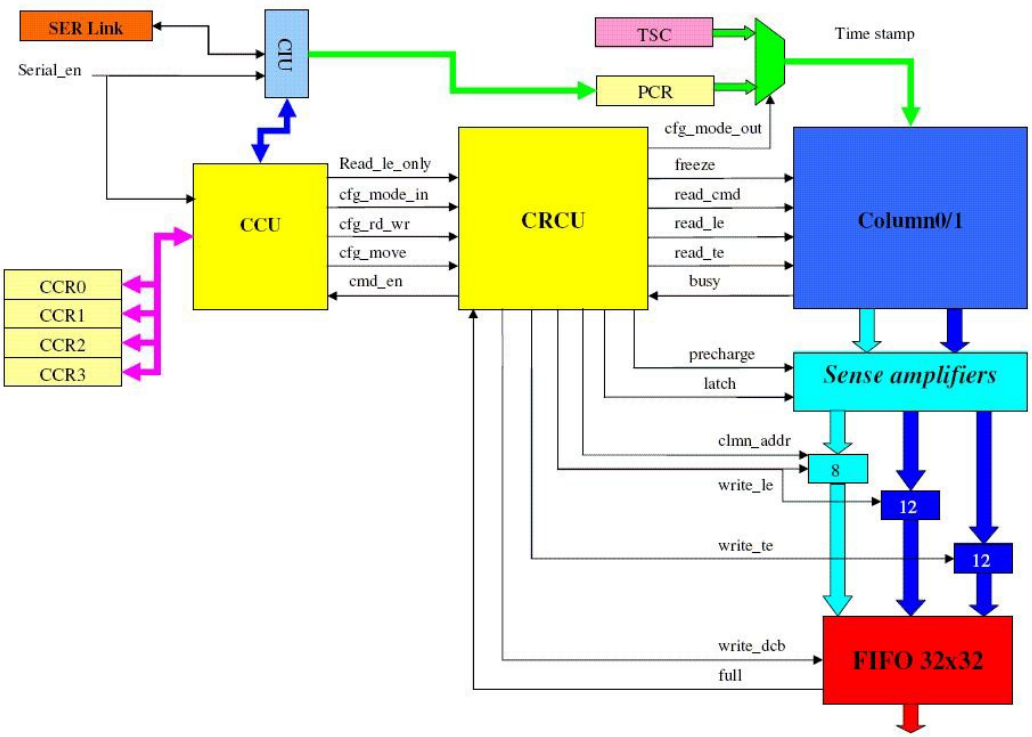


Figure 3.5: Schematic of the end of column circuitry.

3.1.2 *The ASIC operation*

The pixel readout architecture is based on the Time over Threshold (ToT) technique which allows the signal digitalization using low power circuits. The technique allows to measure with a good resolution the value of the injected charge through the time needed to discharge the feedback capacitor of the front-end with the use of a constant current.

The ToT technique

Considering a front-end circuit with a feedback capacitance C_f and a discharge current $I_{dis}(t)$, it is possible to demonstrate that when a charge $Q_{in}(t)$ is collected at the input node a current $I_{in}(t)$ is injected and the output voltage v_{out} of the CSA is given by [19] [20]:

$$v_{out}(t) = \frac{Q_{in}(t)}{C_f} = \frac{1}{C_f}\int_0^t [I_{in}(t') - I_{dis}(t')]dt' \tag{3.1}$$

It is also possible to assume the charge injection as:

$$Q_{inj} = \int_0^{\epsilon} I_{in}(t')dt' \tag{3.2}$$

Since the discharging current I_{dis} is constant follows that:

$$\int_0^t I_{dis}(t')dt' = I_{dis}t \tag{3.3}$$

Using (3.1), (3.2) and (3.3) the output voltage of the CSA can be easily written as:

$$v_{out}(t) = \frac{Q_{inj} - I_{dist}t}{C_f} \tag{3.4}$$

Since when t = ToT the output voltage is zero, it is possible to obtain the linear relationship between the injected charge and the ToT as follows:

$$v_{out}(ToT) = \frac{Q_{inj} - I_{dist}t}{C_f} = 0 \tag{3.5}$$

$$ToT = \frac{Q_{inj}}{I_{dis}} \tag{3.6}$$

The last relation shows how using a constant current to discharge the capacitance of the front-end and measuring the ToT it is possible to obtain the charge released in the sensor.

This measurement, called Time over Threshold technique, allows to achieve a good linearity even when the preamplifier is saturated.

Figure 3.6 shows in blue color the preamplifier output voltage obtained with a high charge value. The plot shows how thanks to the ToT technique, although the preamplifier is saturated by an high input signal, it is possible to extract the information from the signal by discharging the feedback capacitor at the input

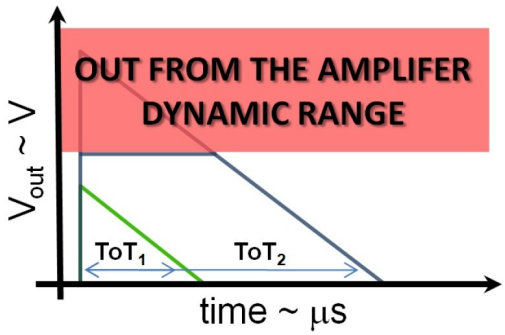


Figure 3.6: ToT Outputs: The ToT1 is obtained from the green signal which don't saturate the preamplifier while the ToT2 is obtained from the blue signal which saturates the preamplifier.

node, preserving the linearity of the ToT measurement. In this way the dynamic range of the front-end is extended up to 50 fC.

The ToT and the time information are obtained by taking advantage of the time stamp. In order to have a common time reference a 12-bit time stamp signal is transmitted to all pixels. If a particle impinges on the sensor, the released charge is detected by the preamplifier-comparator chain, the time stamp value is stored into the pixel and an analogue signal is sent to the preamplifier input. The signal is integrated on the feedback capacitor C_f located in parallel to the CSA and the preamplifier gives the output depicted in blue color in Figure 3.3. This signal is sent to the comparator together to the voltage threshold value. Whenever a hit is observed the preamplifier output voltage increases very fast. If the output crosses the threshold voltage, which is set previously by the 5 bit DAC, the comparator switches from 0 to the digital level 1 and the time stamp value is loaded into the leading edge register. After this operation the integrated capacitor is slowly discharged using a constant current and the amplifier output decreases. When it goes below the threshold, the comparator switches from 1 to 0 and the time stamp value is loaded into the trailing edge register. The constant current discharge provides a constant slope trailing edge of the preamplifier output which in turn, as demonstrated previously, provides a linear ToT measurement of the energy.

In this way the timing information will be given by the leading information while the ToT, and thus also the injected charge information, will be obtained by the difference between leading and trailing edge time stamps.

The technique used for the particle detection depends strongly on the threshold voltage value and therefore it has to be set properly considering also the presence of noise: if the chosen value is too close to the baseline the noise could cause spurious hits while if it is too far the smallest signals are cut. It is important to have the same voltage threshold for all channels with the best precision, therefore the tune system of the threshold has to work properly.

In order to simplify the tests operation the ASIC contains a calibration system which can be enabled indipendently for each pixel. This system is applied to the input of the amplifier via an integrated capacitor.

3.2 THE READOUT ARCHITECTURE

The final ASIC will contain a total of 12760 cells organised in a matrix of 116 × 110. The architecture foresees a double columns structure where two adjacent columns share the same time stamp and readout buses. Each readout cell has a unique address in its column and a size of 100 µm × 100 µm as explained in the previous section.

The scheme employed for the readout foresees a system which allows to create a signal whenever at least one pixel of a column contains data. The system consists in a logic implementation that uses a busy signal generated when a particle is detected by the pixel cell. This busy signal and the busy signal of the previous cell of the column are sent in a logical OR which creates a new signal for the next cell as show in Figure 3.4. If at the end of the column the busy signal is high means that at least one pixel contains data and therefore it is possible to start the read operation.

In order to read data from a column, read commands are sent to all pixels but only the one with its busy input signal at zero sends its data and address to the output buses. The system guarantees that all the pixels are addressed during a readout cycle using the freeze signal which blocks the generation of new busy signals during the readout operation.

Concerning the scheme used to upload the configuration data, it is very similar to the one just described. First the config mode signal is sent to all pixels and puts them in the busy state. In the address cycle, it is possible to load the data stored in the configuration register on the data bus or write the data contained on the time stamp bus in the configuration register.

The readout commands used in these operations are created by the CRCU on the base of the state of the busy signal and of the output FIFO. The data contained in all the CRCUs are stored in the FIFO. The CCU reads the output of the FIFOs and then sends it to the output serializer for data transmission. The serializer is basically a shift register switching on both edges of the clock signal. Both the FIFO registers and the CRCU and CCU state machines are protected against Single Event Upset (SEU) via Hamming encoding. Since a SEU in the state bits is detected and corrected in the successive clock cycle the protection employed is ineffective only when two or more errors occur in the same clock cycle. [2]

The data transmission uses frames which contain all the data received by the chip during a single time stamp counter cycle. A header and a trailer are used to divide the frame from the next and the previous one. The header consists in a word of 40 bits which contains the chip address, the frame counter and error detection and correction bits. For the trailer word it is foreseen the same number of bits and it contains the number of words present in the frame, the Cyclic Redundant Check (CRC) of the entire frame and the error detection and correction bits. Concerning the data frame, it is composed of 2 bits for the header and the trailer word and 38 bits for the data word with a total of 40 bits. The 38 bits of the data word are dedicated to the leading and trailing information (24 bits) and to the pixel address (14 bits).

The module architecture has a structure composed of three interconnected layers: the front-end, the detector and the transmission bus. Concerning the interconnections between these layers, in the case of the sensor and the readout chip they are realized using the bump bonding technique, while in the case of the readout chip and the transmission bus they are realized using the wire bonding technique. In addition to these connections, it is also foreseen a bidirectional link to an external service board which is used to send the clock and to perform the data multiplexing. Moreover this link allows the electrical to optical conversion decreasing in this way the amount of cabling.

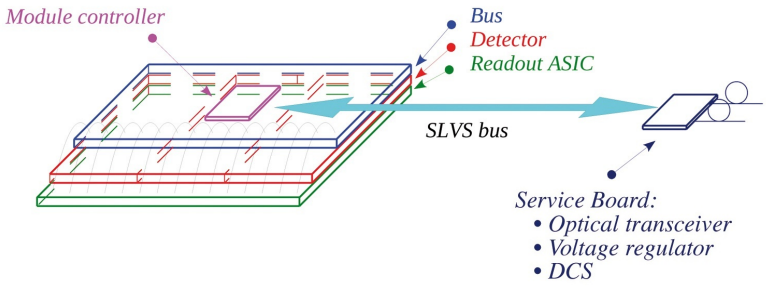


Figure 3.7: Architecture for the readout system.

Two possible architectures are studied for the readout system: the first one, depicted in Figure 3.7, foresees an additional module controller chip located on top the transmission layer which is used to manage the receipt and transmission of data.

Since the use of a module controller gives a greater degree of flexibility, it has been a common choice in the electronic readout of the LHC pixel detectors. This solution allows a reduction of the number of wires coming out the module by using a Phase Locked Loop (PLL) and therefore the possibility to transmit data at a bit rate faster than the clock frequency but at the price of having to use an extra ASIC and thus of a greater power consumption which requires an increment of the cooling pipes number.

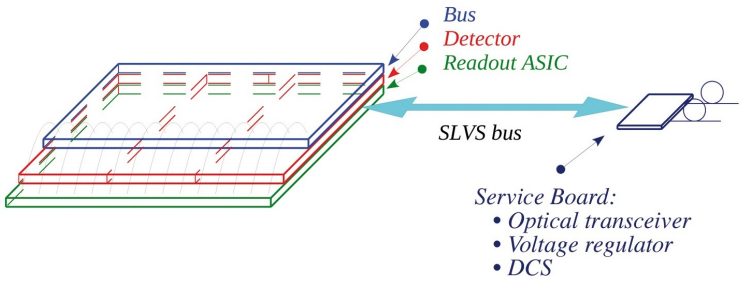


Figure 3.8: Second architecture for the readout system.

The Figure 3.8 illustrates the second possible architecture where the module is connected directly to the service board. Since this solution doesn't use the additional module controller the power consumption is lower and thus it is more attractive than the first architecture.

3.3 ASIC PROTOTYPES

The development of ToPix has been divided in many steps in order to test and verify easily every single part of the complete ASIC architecture. Until now three different prototypes have been carried out. Each prototype contains the improvements of the parts tested in its previous version and a further part of the complete architecture. In this way it is possible to identify any operating problems step by step. In this section are described the three versions of ToPix, the architecture choices made for each version and the comparison between the results obtained from the simulations and from the laboratory tests.

3.3.1 *ToPix Version 1*

The first prototype of ToPix, developed using the commercial CMOS 0.13 µm technology, has been designed to evaluate the analogue performance of the ASIC. Hence it was developed using only the basic analogue blocks described previously.

This first version has been developed without enclosing layout techniques in order to verify if this technology with a simple layout is suitable for the $\overline{\text{P}}$ANDA needs.

The prototype contains 32 readout cells each one with their own preamplifier and discriminator. They are arranged in 8 groups of 4 cells as shown in Figure 3.9. For each group there are 4 calibration input lines, 4 multiplexed analogue outputs and 4 multiplexed digital outputs. Moreover this version contains also 6 additional input lines in order to connect the sensors .

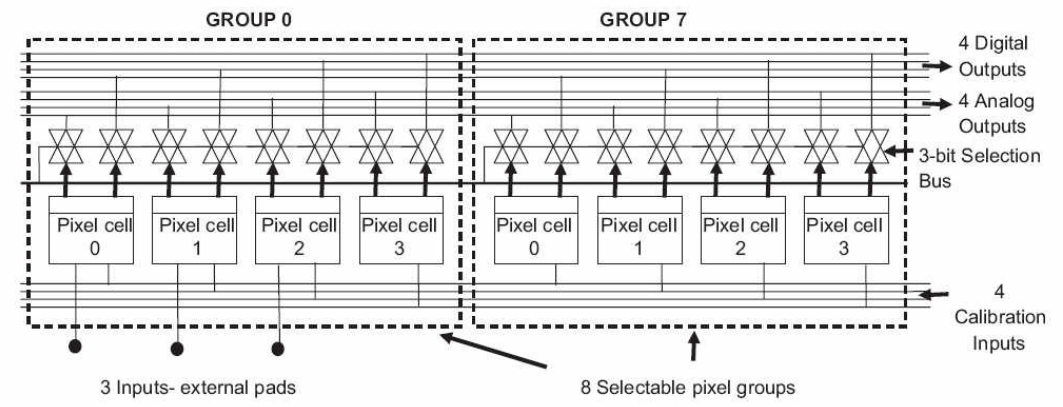


Figure 3.9: Schematic representation of the first prototype of ToPix.

The structure of the preamplifier consists of a CSA and a costant current feedback as depicted in Figure 3.10. The feedback capacitance employed has a value of 10 fF which is considered a good trade-off between the loop stability and the charge gain.

The input IN_{CAL} shown in Figure 3.10, is the calibration line which is common for one of the cells in each of the 8 groups. The calibration capacitor C_{CAL} used

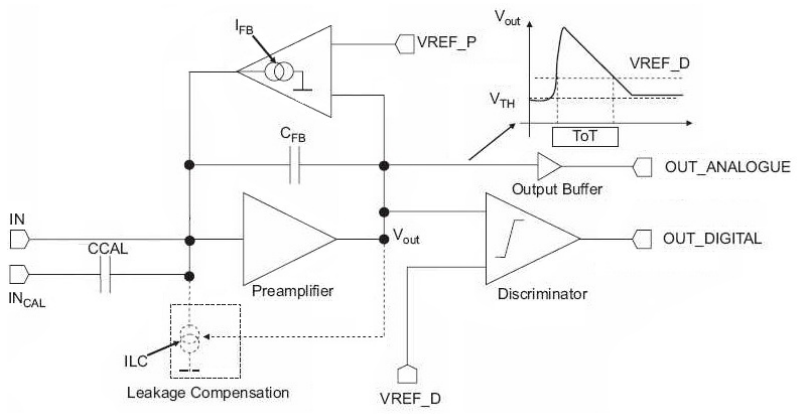


Figure 3.10: Analogue blocks of the first prototype of ToPix.

in this line allows to obtain a delta shaped current pulse injected at the input node of the preamplifier when a voltage step is sent on the calibration line. The value chosen for this capacitance in this version of ToPix is 30 fF.

Moreover since the capacitive load of output pads and measurement probes can be up to 10 pF, the analogue signals are driven by a source follower and the digital signals are driven by a buffer.

Concerning the layout, the absence of enclosed structures allows to reduce its size. As illustrated in Figure 3.11, it consists of a preamplifier and a discriminator with a size of 37 µm × 51 µm and 12.8 µm × 48 µm, respectively. The ASIC size features an area of 2 mm × 1 mm [2][21].

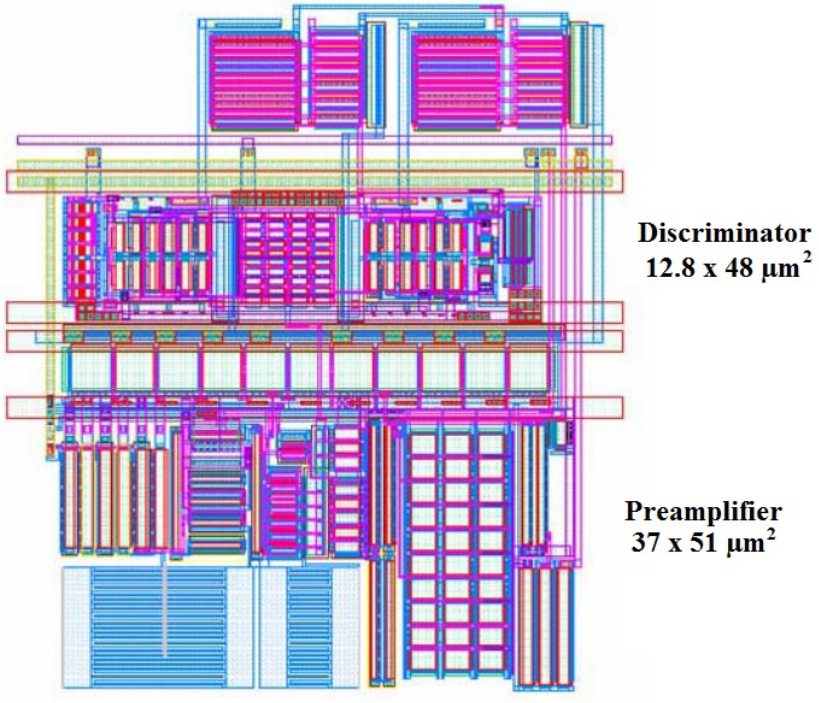


Figure 3.11: Layout of the preamplifier and discriminator in ToPix 1.

3.3.1.1 *Test and results*

As explained previously a capacitance C_{CAL} is employed on the calibration line. During the test, in order to inject a charge into the pixel cells, an external step signal of amplitude V_{CAL} is applied at the calibration input node of the line. In these conditions the injected charge during the tests is given by $V_{CAL} \cdot C_{CAL}$.

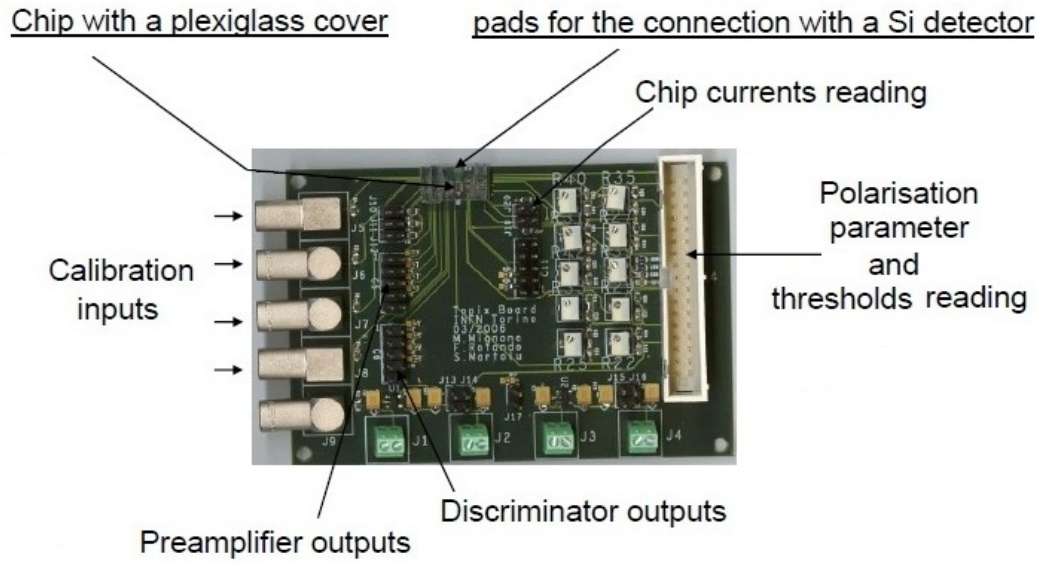


Figure 3.12: The PCB board and the chip used for the tests [21].

The PCB illustrated in Figure 3.12 was employed to make many tests on the prototype starting from electrical functionality tests where the ToT linearity, the preamplifier response were analysed, to radiation damage tests employing X-rays and neutrons.

The preamplifier output obtained with a pulse input and a charge of 0.5 fC is depicted in Figure 3.13. The output was measured with a differential probe in order to get the best common mode noise rejection.

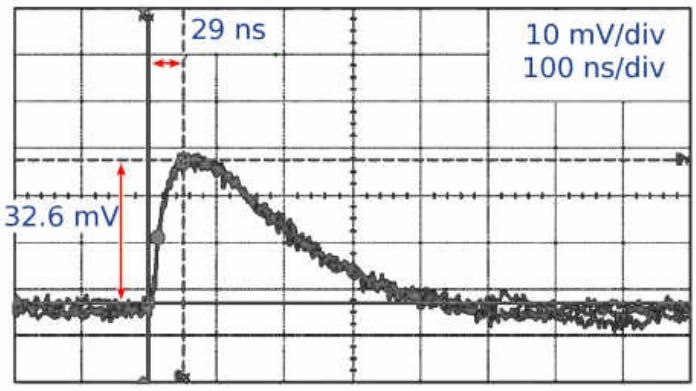
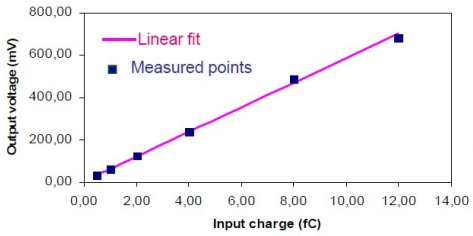


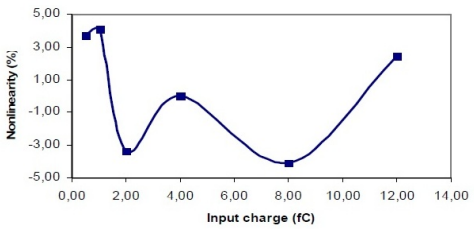
Figure 3.13: Preamplifier output for an input charge of 0.5 fC.

Other tests were made injecting charge values of 1, 3, 4, 8 and 12 fC and fitting the nominal values of the output in the linear region in order to obtain the preamplifier gain. From this measurement the gain results to be 60 mV/fC. Concerning the noise, measurements give a value of 1 mV r.m.s. which, using the measured gain, corresponds to a ENC (Equivalent Noise Charge) value of 104 e^- r.m.s.

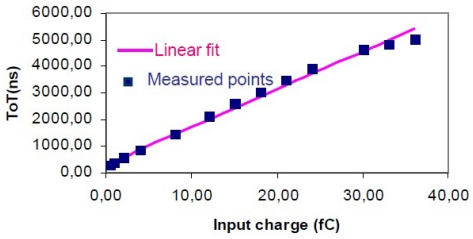
The power consumption of each pixel with a voltage supply of 1.2 V is about 12 µW and thus respects the low consumption requirement of the MVD.
In Figure 3.14, where plots of the preamplifier output and of the ToT obtained from tests are depicted, it is possible to observe that both of them preserve a good linearity at least up to 12 fC and 30 fC, respectively.



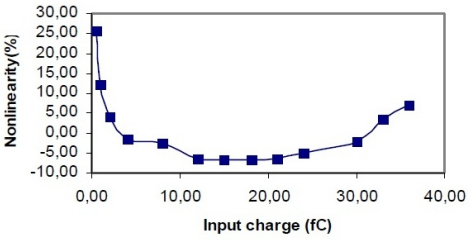
(a) Preamplifier output V_{OUT} linearity.



(b) V_{OUT}: Deviation from the linear fit.



(c) Time over Threshold linearity.



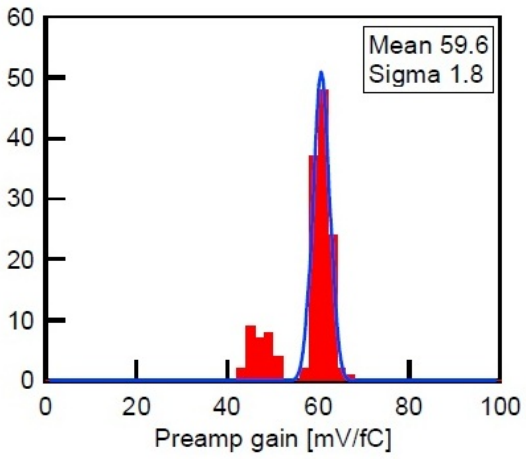
(d) ToT: Deviation from the linear fit.

Figure 3.14: Linearity plots.

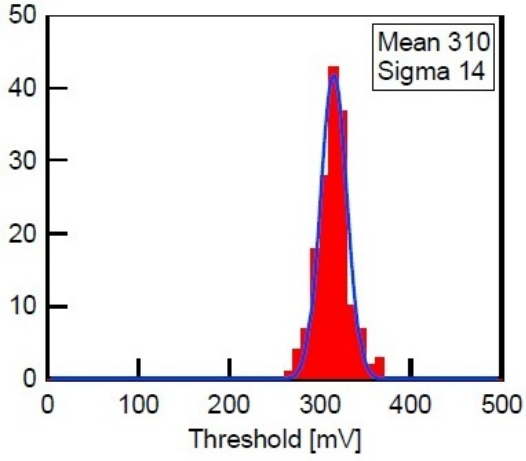
Parameters like the voltage threshold, the preamplifier gain and the ToT gain are very important and therefore they were measured in 144 different pixel cells. The distributions of these measurements are illustrated in Figure 3.15.

Also a TID (Total Ionizing Dose) test has been performed on four different ToPix chips using X-rays up to a final value of ~ 20 Mrad. After the radiation damage tests the chips were subjected to annealing. The plots obtained by these measurements are represented in Figure 3.16 where it is possible to observe the leakage current, the threshold V_{TH}, the baseline V_b, the preamplifier gain and ToT gain variations due to the radiation and the annealing. Although the preamplifier gain variation is negligible (below 2%), for the ToT is noticed a dispersion of 20% rms and for the baseline a value of about 13 mV rms. In this prototype the annealing allows a partial recovery in particular for the threshold voltage V_{TH} and for the baseline V_b.

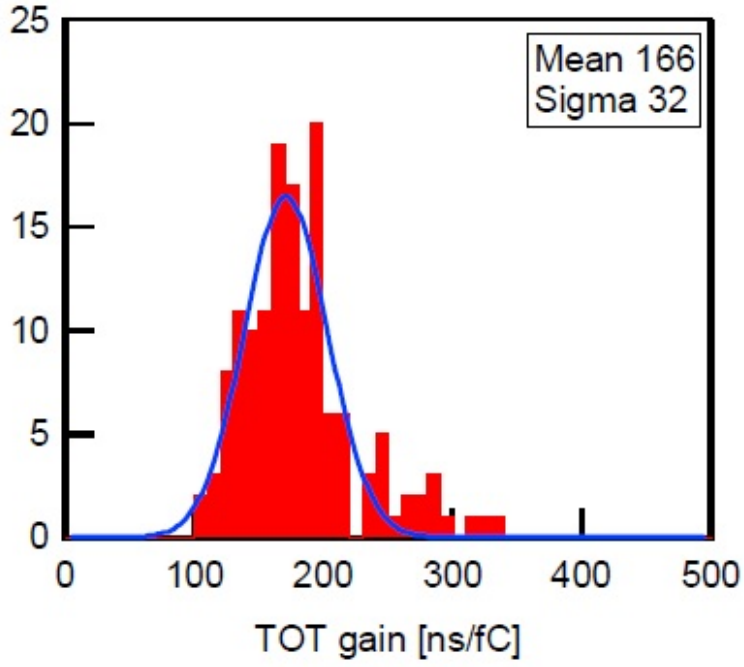
In addition to this measurements also the neutron test has been performed and no significant variations have been observed in the more important parameters of the prototype. The results are explained in detail in [21].



(a) Preamplifier gain distribution.

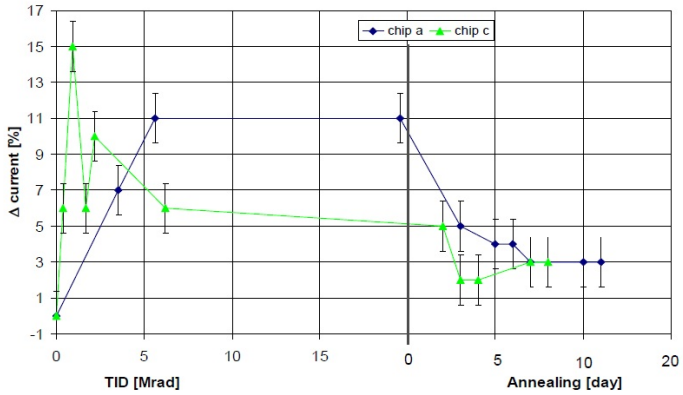


(b) Threshold distribution.

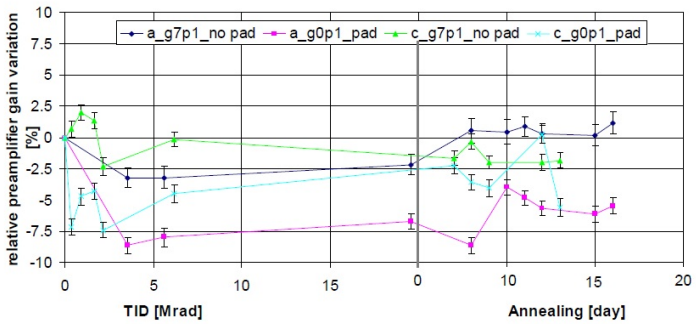


(c) Time over Threshold distribution.

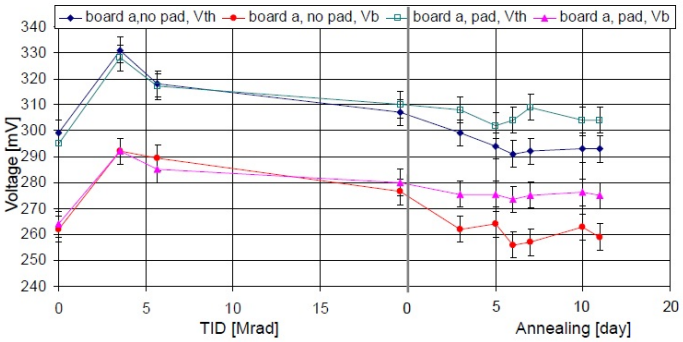
Figure 3.15: Distributions of the more important parameters for 144 pixel cells.



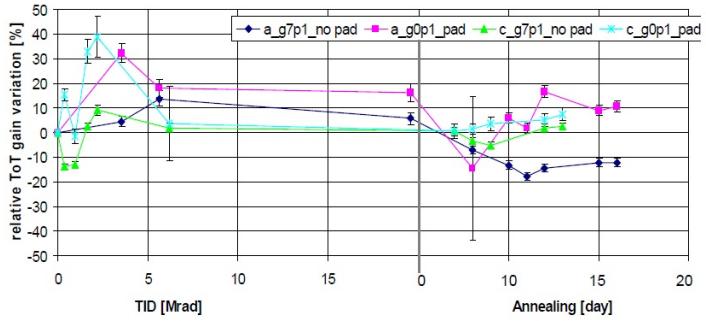
(a) Leakage current as a function of TID and Annealing.



(b) Preamplifier gain variation for pixel cells with and without pad.



(c) Threshold voltage (Vth) and baseline voltage (Vb) for both pixel cells with pad and without pad as a function of TID and Annealing.



(d) Relative TOT gain variation for pixel cells with and without pad.

Figure 3.16: Results from the TID at high dose rate and annealing tests.

3.3.2 *ToPix Version 2*

The second version of ToPix, designed in the commercial sub-micron CMOS 0.13 µm technology as the first prototype, was developed to prove the pixel cells and column functionality. Therefore the cells contain also the digital part and all the blocks required for the final ASIC architecture with the exception of the bonding pad opening.

The prototype contains two 128 cell and two 32 cell columns. The two 128 cell columns are folded in four 32-cell slices in order to get a good form factor. A simplified schematic of the architecture of the prototype is depicted in Figure 3.17.

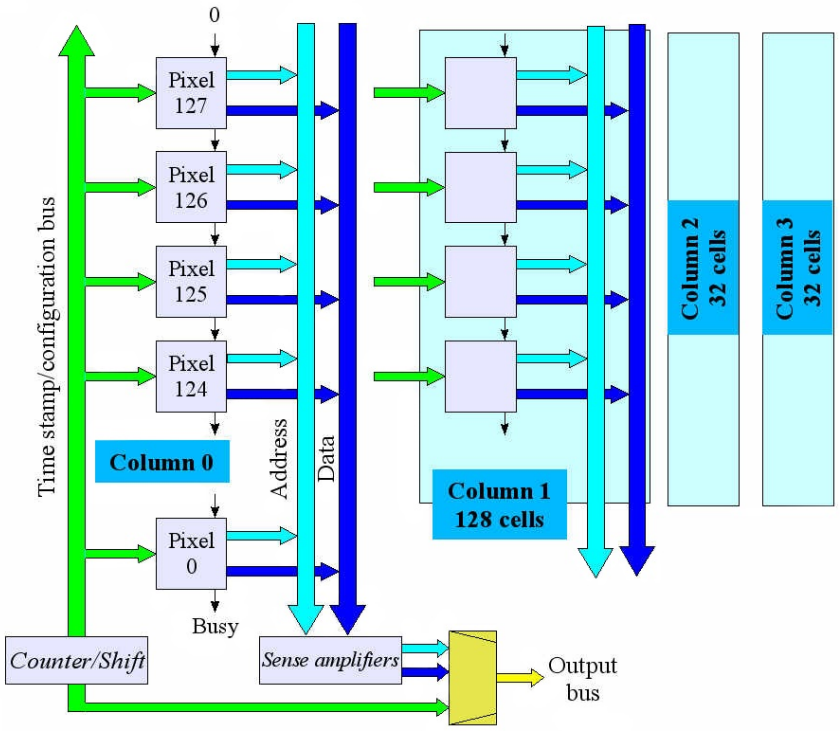


Figure 3.17: Simplified schematic of ToPix version 2.

In this version of ToPix the architecture of the end of the column logic contains only the counter and the bus readout sense amplifier in order to simplify it for test purposes. The ASIC contains also new features to improve the testability like the easily connection between the chip and the detector via external pads connected to the input of 16 cells of the first column. However, this arrangement has the price of a significant increase of the input capacitance and therefore of noise.

Since the DICE (Dual Interlocked storage Cell) design should provide better protection against SEU for sub-micron technologies as is the case of the CMOS 0.13 µm technology, latches and flip flops in the pixel cell are based on this architecture allowing also to save area compared with a triple redundancy architecture.

3.3.2.1 *Test and results*

A DAC chain based on a NI-PCI system and LabVIEW software were employed for tests following the diagram of Figure 3.18 . The FPGA board illustrated in the diagram uses a bidirectional FIFO in order to test the ASIC with the design clock of 50 MHz.

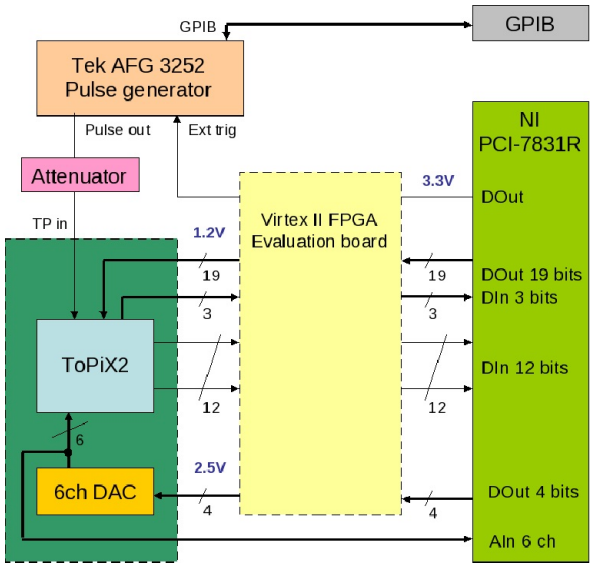


Figure 3.18: Diagram for the data acquisition system.

The prototype has been tested in all its electrical functionality with ToT, gain preamplifier and TID measurements. In order to examine if there is any influence of pads, during tests the charge was injected both through the calibration circuit and through the inputs connected to the pads.

The ToT measurements aim to verify the linear relation between the ToT and the charge injected. The results obtained over the whole dynamic range are similar in all pixels therefore in order to simplify this exposition only the results for the pixels 16 and 21 are reported in Figure 3.19. The results show a linear response with a maximum deviation from the linear fit of 3% just as obtained with the first version of ToPix.

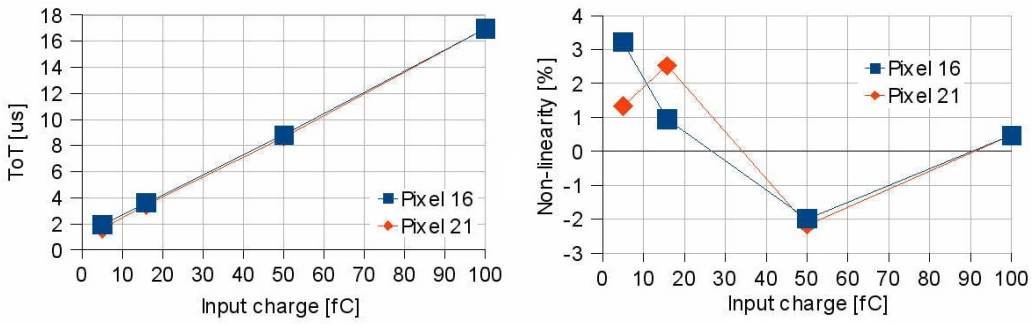
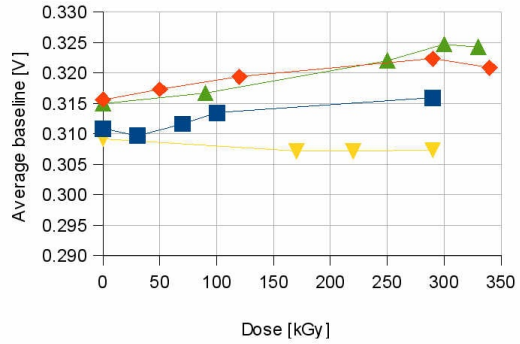
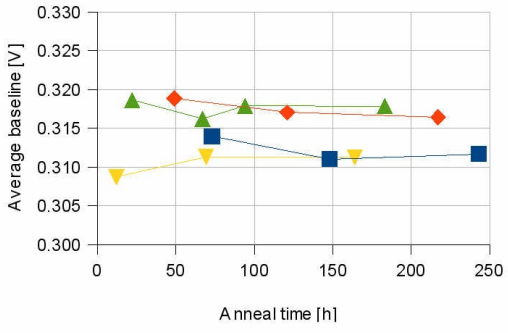


Figure 3.19: ToT linearity measurement.

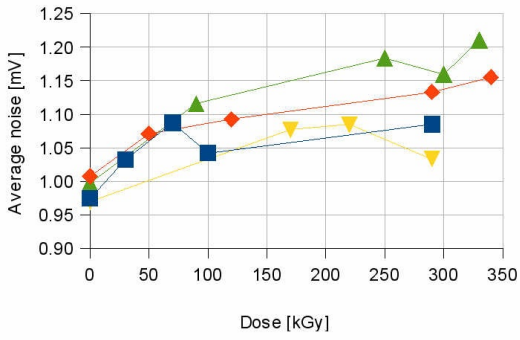
The total dose irradiation (TID) tests have been performed with a rate of 4.07 Gy/s. Both the average baseline and noise voltage were studied during the irradiation and then during the annealing at 100° C. The results obtained for four different chips, are depicted in Figure 3.20 and they show a baseline variation bellow 3 % that is comparable with the dispersion due to the process variation. This variation has the same magnitude for all the chips tested. Concerning the noise an increment of about 20% was observed after irradiation which is a worse result compared with the first version of ToPix but simulations show that it is justified by the capacitance added by the metal plate connected to the pixel input to emulate the bonding bad capacitance. From the annealing tests a partial recovery was observed in the baseline value and an almost complete recovery of the noise level.



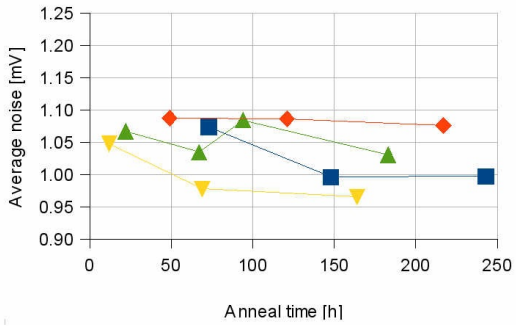
(a) During irradiation.



(b) During annealing.



(c) During irradiation.

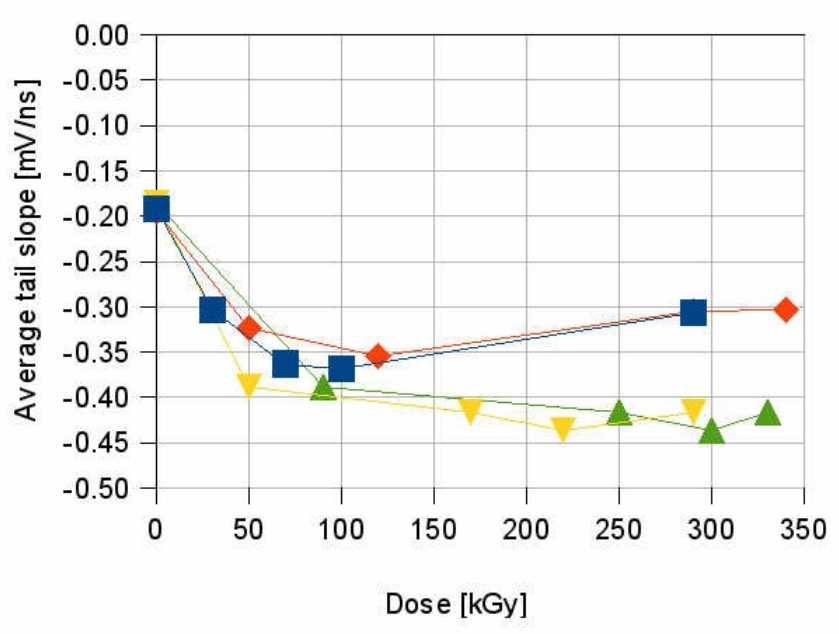


(d) During annealing.

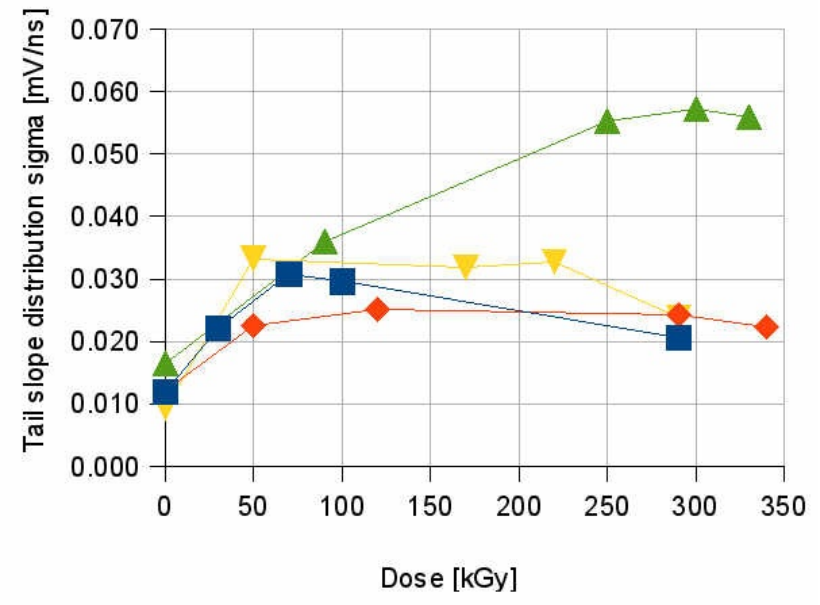
Figure 3.20: Average baseline and noise plots.

From Figure 3.21, where the average tail slope during the irradiation is depicted, follows that the variations of average and sigma are much more relevant. This effect could be caused by the current used to discharge the integrating capacitor which is very small (around 6 nA) and therefore it results comparable with the leakage currents induced by radiation. A solution for this could to be use an enclosed gate layout for the critical transistors of the discharge circuit.

In addition to the tests described so far, also a dedicated study of the SEU has been performed in order to verify if the DICE architecture was sufficient for the MVD requirements. The study shows possible variations of one bit in the digital circuitry due to SEU. The effect can be problematic not for the corruption of the



(a) Average slope.



(b) Average slope sigma.

Figure 3.21: Slope trend during irradiation.

data since it can be easily identified and discharged but for the loss of the detector control function. In fact the system can be restored only with a reset at the price of discharge all the data collected from the upset event to the reset operation.

Therefore although the configuration register has a radiation tolerant architecture some devices of the digital part, like the shift register and the counter, are not radiation tolerant in this prototype [2].

3.3.3 *ToPix Version 3*

As done in the previous versions of ToPix also the third prototype was developed in CMOS 0.13 µm DM technology. This version is designed to work with the frequency foreseen for the final version of ToPix which is 155.52 MHz.

The ASIC contains two 256-cells double columns and two 64-cells double columns. In order to fit the ASIC area and obtain a square geometry, the 256-cell columns have been folded in four 32-cells. In this way the die obtained covers an area of 4.5 mm $\times$ 4 mm with the layout depicted in Figure 3.22.

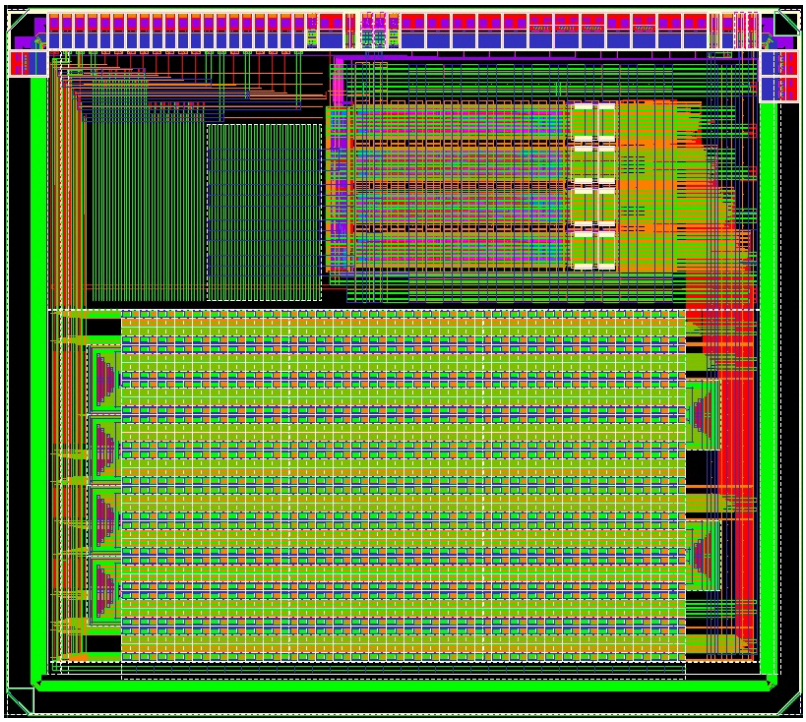


Figure 3.22: ToPix v3 layout. The die size is 4.5 mm $\times$ 4 mm [22].

The chip developed contains complete cells with the full analogue and the digital circuitry, the buffers and the end of the column logic as foreseen for the final version while other parts, like the output multiplexer and serializer, are still in a simplified revision. New direct connections to the detector have been added by the use of bump bonding pads.

In order to improve the SEU tolerance of the ASIC some parts are designed using particular techniques: a design based on Triple Modular Redundant (TMR) technique and the Hamming encoding were employed for the pixel registers and for the end of the column logic, respectively. This configuration allows an asynchronous error detection and a self-correction for the configuration register at the price of reducing its bits number from 12 to 8 in order to fit the pixel area. Due to the same area constraint, the correction of the trailing and edge registers is implemented only for the majority voter.

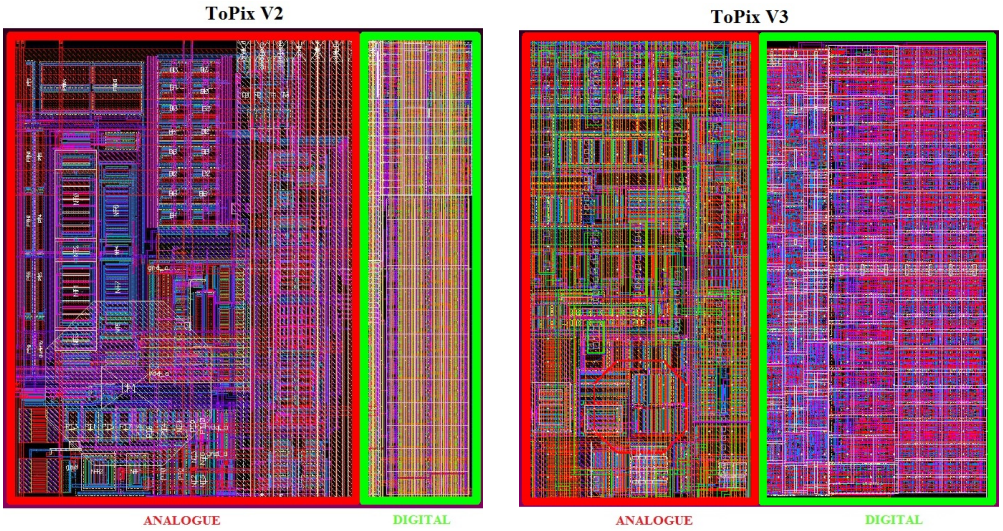


Figure 3.23: The analogue and digital layout pixel cell in Topix V2 and ToPix V3.

The prototype contains also a clipping circuit designed to avoid the long dead times which has been observed for large input charges in ToPix v2. This new circuit has been designed in order to force a ToT saturation at about 16.5 µs.

The power supply foreseen of 1.2 V allows to obtain a low power consumption and moreover the use of the differential SLVS standard allows also to reduce the digital noise contribution.
The layout, shown in Figure 3.23, has been optimized in order to place the comparator between the most sensible analogue blocks. Figure also shows that area management is different from the version two because the analogue and the digital part has been implemented in the equal area of 50 µm × 100 µm.

The single event upset tests of the chip have been made at the SIRAD Facility of the Laboratory Nazionali di Legnaro (LNL) of INFN with a set of several ions ranging from Oxygen to Bromine with energies in the range of 100 and 200 MeV. The tests foreseen measurements at angles of 0 and 30 degrees [23].
The tests aim to get an analysis of the SEU tolerance of the various protection schemes and to obtain comparative results with a second chip designed in the same technology but with a full logic triplication.

From simulations results are expected a ToT gain of 200.022 ± 0.046 ns/fC at V_{TH} = 30 mV and a channel to channel ToT spread of 7%. The simulated noise level obtained is 155 e^- at I_{LEAK} = 0 nA and 209$^-$ at I_{LEAK}= 10nA [2].

3.3.3.1 *Test results*

The experimental setup consists in a Xilinx evaluation board equipped with the Virtex 6 FPGA and an acquisition system based on the Labview software. The integrated circuitry employed for the test allows to inject a programmable charge to the preamplifier input of one or more pixels.

An input circuit generates a voltage step with amplitude equal to the calibration level to a capacitor of 36 fF connected to the input of the preamplifier. Thanks to the test enable bit located in the pixel configuration register it is possible to select any combination of pixels for the test pulse injection

Although the ASIC was developed for a frequency of 155.52 MHz, due to a problem probably caused by the folded structure, in the column buses not all the 32 cells work at this frequency and therefore the tests have been performed at 50 MHz.

In order to verify the shape signal a test was made using different input charge values with a threshold scan and the internal test signal generator. In Figure 3.24, where the preamplifier output obtained from these measurements is depicted, is possible to observe that the rising edge is faster than the falling edge even in the saturation condition.

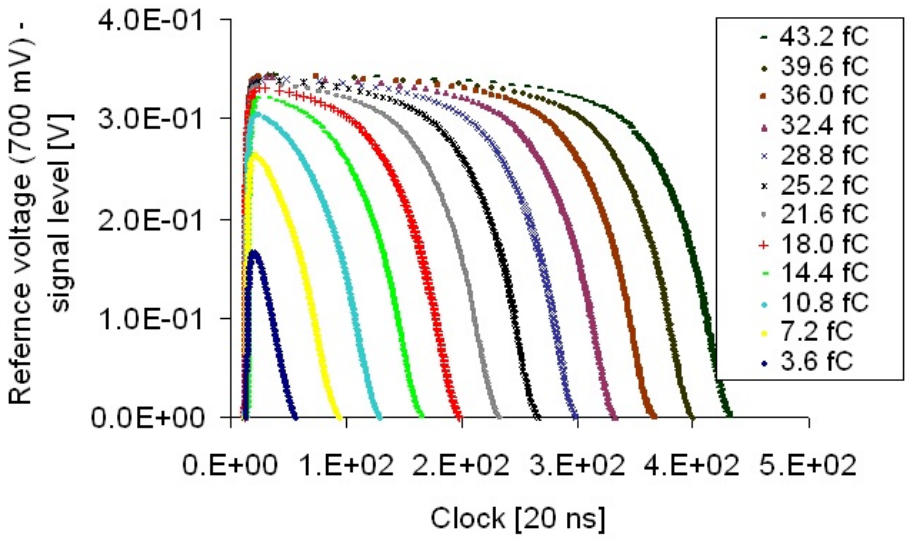
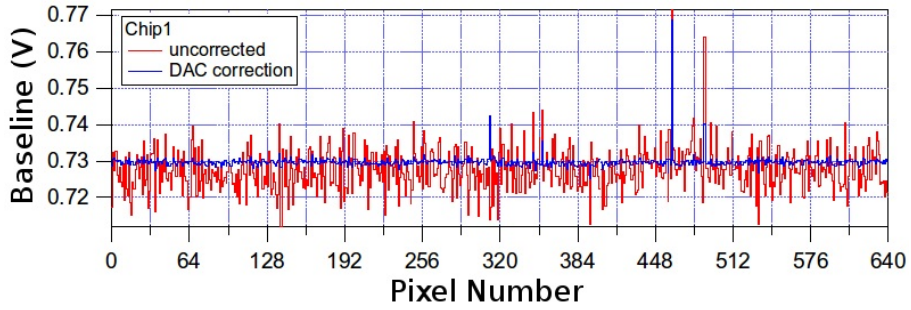


Figure 3.24: Signal shapes obtained with different charge values.

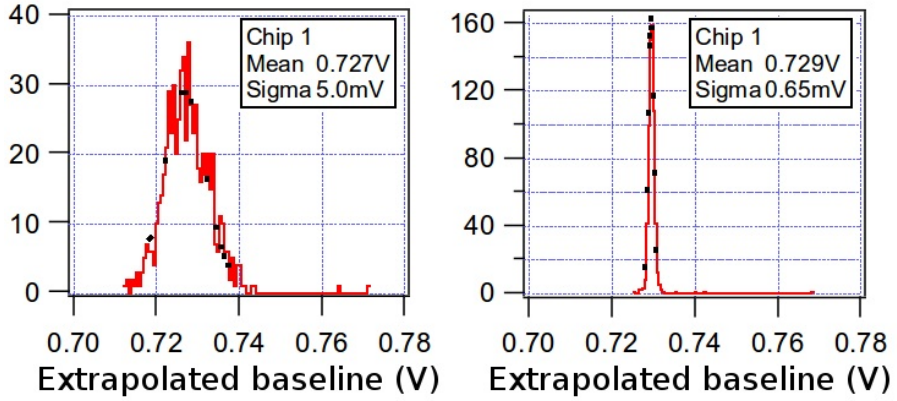
Tests were also performed to study the baseline equalisation using the 5-DAC correction. The test was made in four chips obtaining similar performances. In Figure 3.25 is depicted as an example the result obtained for the chip 1. Before the calibration an average baseline value is 0.73 V with a sigma of 5 mV while after the calibration procedure the sigma is reduced to 0.65 mV.

Although the results show the good effect of the correction, the tuning for all the pixels appears a complex operation due to the non linearity response between

the DAC correction and the baseline. Therefore in order to simplify this operation it should be useful to have a similar correction system, but with a linear response.



(a) Extrapolated baseline.



(b) Baseline distribution before (left) and after (right) the correction.

Figure 3.25: Equalitation effect in the baseline distribution for 640 pixels [2].

During test of the 640 pixels the gain measured is an average value of 66 mV/fC which differs from the expected value from simulations (75 mV/fC). However, this difference is compatible with the process variations. Figure 3.26 shows the noise measurement of the 640 pixels. The average value obtained is 104 e^-. Since this measurement have been made without the detector connected to the preamplifier input, an increase of the noise value in the final system is expected.

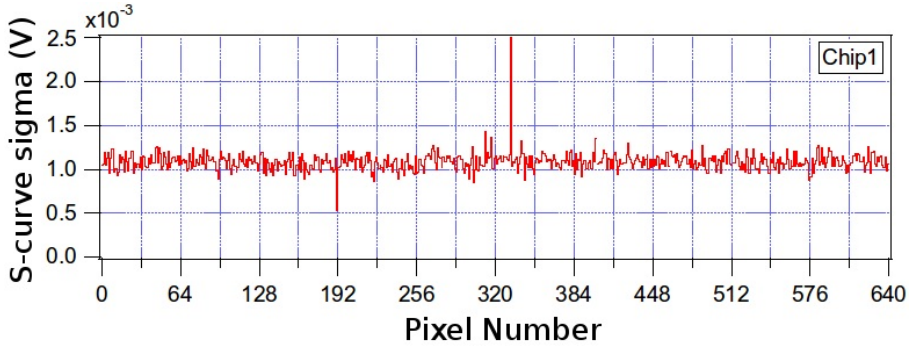


Figure 3.26: Noise measurement

The Time over Threshold transfer function obtained with different charge injected values and the deviation from the linear fit is shown in Figure 3.27. The ToT gain measured is 232 ns/fC in good agreement with the expected value of 202 ns/fC obtained from simulations. The circuit maintains a good linearity even when the input preamplifier is saturated.

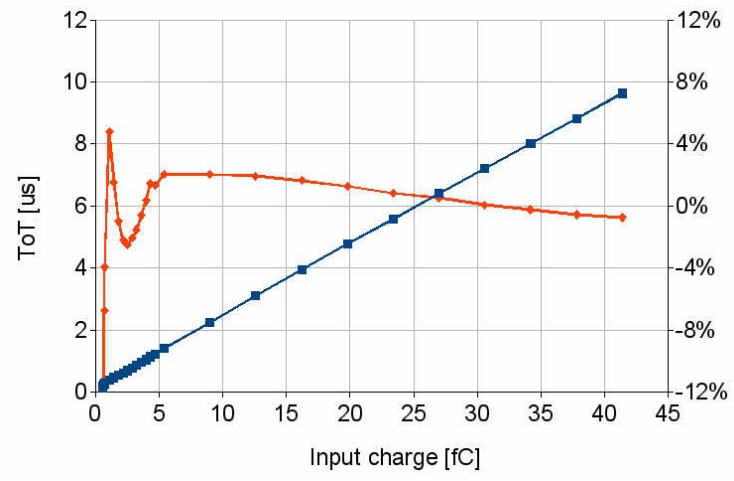


Figure 3.27: ToT measurement.

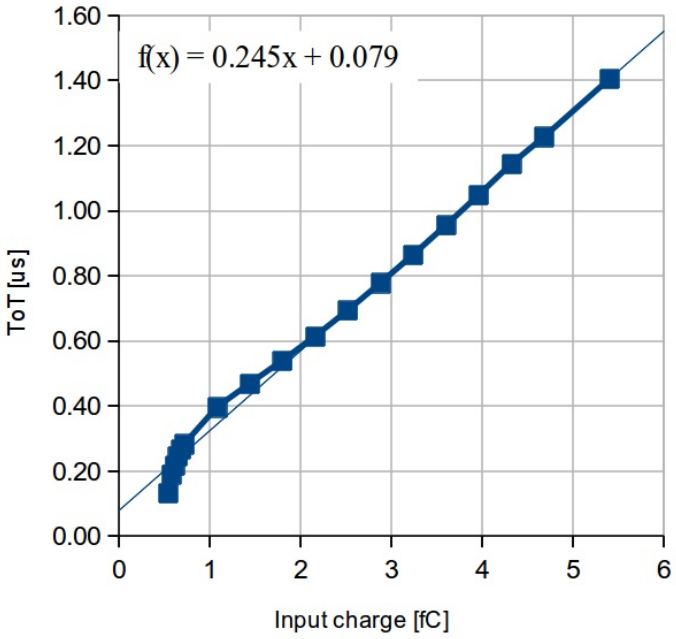


Figure 3.28: ToT measurement until 6 fC.

In Figure 3.28, where the same plot for charges up to 6 fC is depicted, it is possible to observe that most relevant non-linearity occurs for charges under 3 fC. In order to get a good linearity response also in this region, the gain preamplifier will be increased in the new version of ToPix [22]

Electrical test results show a good agreement with the simulations proving the good functionality of the chip.

4

LINEAR IN-PIXEL DAC

The test results of ToPix v3, illustrated in Chapter 3, show a good behaviour of the tuning system in mitigating the threshold voltage dispersion. In fact, the results obtained testing the prototype show how with the fine tuning it is possible to make a good correction reducing the peak to peak value of the dispersion from ~ 30 mV to ~ 2 mV. However, the tuning operation which is made using an automatic system, appears a quite difficult one because of the non-linear relationship between the DAC code and the threshold voltage.

In this Chapter, in order to study the origin of this non-linear response, the DAC and its function in ToPix v3 as well as the tuning system, are described in detail. The study is made with the use of theoretical concepts and simulation results. Moreover it is illustrated a possible solution which allows to obtain the linear response which might facilitate the tuning operation for the million of channels of the MVD. The route towards the realisation of the solution is described step by step.

The chapter begins with a section where the simulations done are explained. The analysis of the non-linearity starts with a section dedicated to the DAC of ToPix v3, where the device is analyzed in detail at transistor level and its function is explained with the help of some simulation results. The descriptions of the devices use a top-down approach which employs first blocks to explain the principal functions and then the transistor implementation to describe how each block is realized.

The tuning is explained and simulated using also the comparator block in order to observe the non-linear response and to study a possible solution.

The design criteria to develop the circuit, the optimisation process as well as the technical solutions chosen are discussed with the help of some simulation results. The challenge of this work is to develop a circuit, whose implementation is common and so well known, but with a new strong constraint which is the reduced area available in the pixel. The possible ideas to solve the problem are proposed together with their realistic implementations. Their strengths and weaknesses are discussed and a trade-off solution is proposed. At the end of the chapter, the final circuit operation in the whole analogue cell is simulated. An example of correction is proposed in order to demonstrate the way to predict the DAC code necessary to tune the voltage threshold of each pixel.

4.1 DESIGN AND SIMULATIONS

The design and the study of the circuits made in this chapter use a top-down approach which starts with set of design specifications. The specifications describe the expected functionality of the designed block as well as the silicon area and other properties such as power dissipation. In particular, as it will be observed for the linearization circuit, in order to cope with the ASIC requirements described in Chapter 3, size and power dissipation represent design constraints which must be kept in consideration during the design.

After the transistor-level description of circuits, their electrical performance and functionality are verified using a Simulation tool. Detailed transistor-level simulations as temperature analysis, stability tests and noise estimations are made in order to test the performance of the devices.

The simulator includes also advanced statistical analysis like Monte Carlo to help to improve the design and the analysis of the circuits. The Monte Carlo simulation refers to statistics blocks which contain statistical distributions and correlations of some device parameters. For each iteration of the Monte Carlo analysis a pseudo-random value is generated for the specific parameter. The Monte Carlo analysis therefore becomes a tool that allows to examine and predict circuit performance variations, which affect yield. The simulator tool allows to choose between specify batch-to-batch (Process) and per-instance (mismatch) variations for parameters. These simulations may represent IC manufacturing process variation or component variations for board-level designs [24]. This kind of simulations are often used in this chapter to analyse the voltage dispersion in particular nodes and to chose the adequate transistor size to use in order to reduce the mismatch effects [16][25].

Since some of the blocks discussed in this chapter, as the DAC and the comparator, have already their mask layout design, for these devices the tool employed allows the ”extraction” of a mask layout which allows to accurately assess the the electrical performance of the completed design. The extractor is able to identify the transistors employed and the points electrically connected together as well as the parasitic resistances and capacitances which are inevitably present between the layers. All these informations are collected in the extracted net-list which is used in the post-layout simulations to evaluate the parasitic effects and thus get an idea of how the circuit would work.

Where possible the comparison between schematic and post-layout simulations is done to underline some critical effects which can affect the performance of the design.

It is important to note that a satisfactory result in post-layout simulation is still no guarantee for a completely successful product because the more realistic performance of the chip can only be verified by testing the fabricated prototype. In fact, even though the parasitic extraction is used to identify the realistic circuit conditions to a large degree from the actual mask layout, most of the extraction routines and the simulation models used in modern design tools have inevitable numerical limitations.

4.2 THE DAC OF TOPIX VERSION 3

Some characteristic parameters of the analogue pixel cell, as the threshold voltage of the comparator, are very important to correctly collect the information from the particle hits.

A comparator is a device that compares two voltages (or currents) and outputs a digital signal indicating which is larger. In the analogue pixel cell of ToPix the device compares the CSA output with a voltage reference which is set properly based on the polarity of the sensor employed. The threshold voltage of the comparator is defined as the voltage value which the CSA output has to reach, when the voltage reference is set to a fixed value, to cause the commutation of the comparator. Ideally, this parameter should be equal to the voltage reference; however, due to the inevitable mismatch between the real devices, these two values are different in each pixel.

Controling this parameter with high accuracy is very important, therefore it is required a system which allows to mitigate the threshold dispersion.

To solve the problem created by the mismatch effects, in the third version of ToPix each pixel cell contains a DAC (Digital to Analog Converter) which converts a 5 bit digital code in an analogue signal (a current). The signal generated is sent to the comparator allowing to change the threshold voltage. The converter works locally and therefore, in order to obtain for all the channels the same value, the DAC code must be chosen pixel by pixel.

The principle of operation of the converter is illustrated in Figure 4.1.

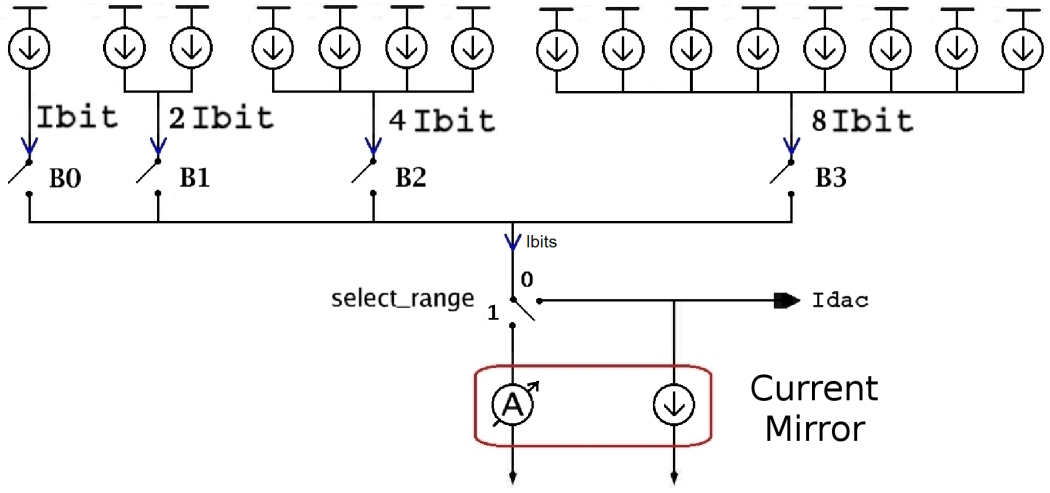


Figure 4.1: Simplified block model of the 5 BIT DAC of ToPix version 3 [14].

In the block diagram the bits weight is represented using a different number of ideal current generators. For the bit B0, B1, B2 and B3 a number of 1, 2, 4 and 8 current generators, are respectively foreseen. Therefore the DAC contains in total 15 current sources.

Each bit, after being activated by the corresponding switch, feeds a principal line where the current Ibits flows. This current changes its value according to the DAC code chosen for the pixel. In this way using 4 bits it is possible to set 16 (2^4)

different values for Ibits. The additional switch "select range", shown at the bottom of Figure 4.1, implements the fifth bit. The switch controls the current polarity allowing to increase the selectable values from 16 to 32. The current generated with the 5 bits (Idac) is then sent to the comparator.

It is important to consider that it is also possible to obtain the last bit using additional 16 current sources, as done for the other bits. However, the solution adopted allows to obtain the same result using less transistors and thus using a smaller silicon area. In general, solutions which need less area appears more attractive due to the design constraint to fit the complete analogue pixel cell in a size of 100 µm × 50 µm.

With the described scheme, the DAC can sink or source current to a low impedance node in the comparator, that is the drain of M9 and M11 as depicted in Figure 4.2.

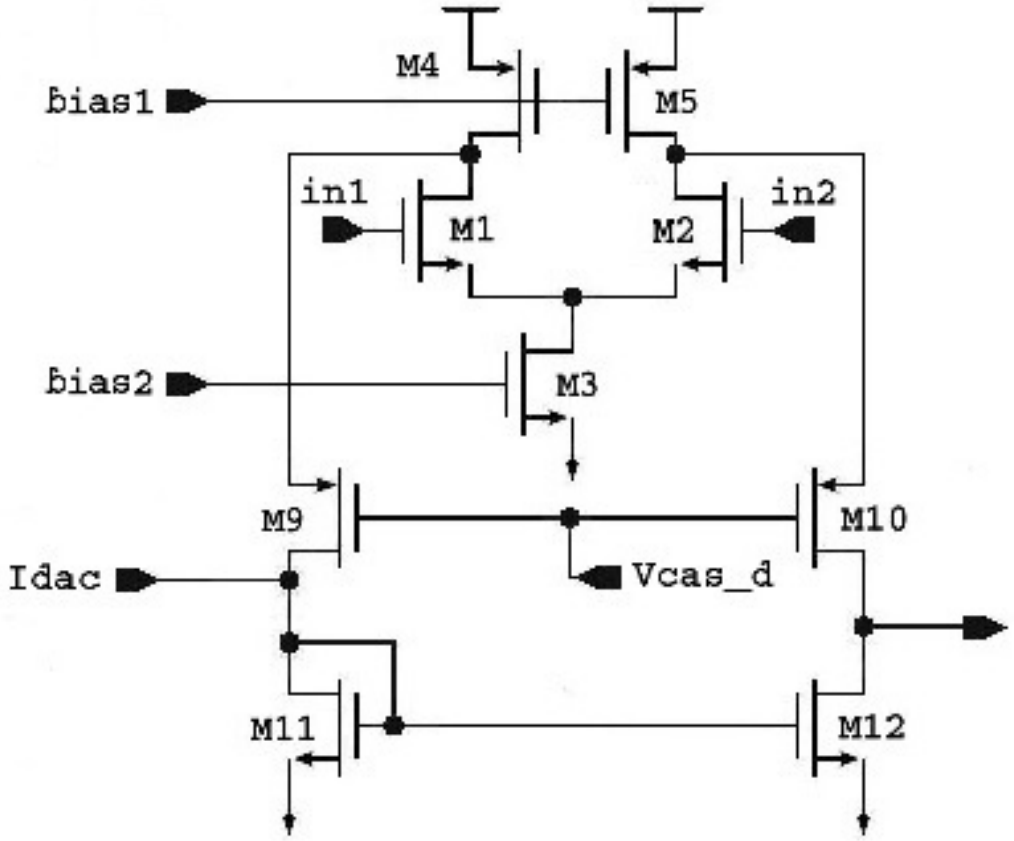


Figure 4.2: Partial implementation of the comparator of ToPix v3: the single stage differential amplifier.

The comparator with all its features will be described in a detailed way in Chapter 5 while the effect of the Idac current in the comparator circuit is discussed in the following sections.

4.2.1 *The transistor level implementation*

The basic element which forms the DAC is the single bit block. Each block consists in a current source obtained using 3 PMOS transistors connected in series as depicted in Figure 4.3. The source of M1 is connected directly to the voltage supply Vdd, which is set to 1.2 V, while the drain of M3 is connected to the line where the current Ibits flows. Transistors M1 and M2 are used to implement a cascoded current source. The signals *dac_bias* and *dac_bias_2* come from a dedicated biasing cell which allows, changing the value of a resistance located outside the pixel, to tune the value of the current generated by each single bit. A unique bias cell is used to control the current of all the 15 current generators foreseen in the DAC. The signal *bit_set* is used to drive transistor M3 as follows: if the signal *bit_set* has a low value, the transistor works in the linear region and lets the current flow feeding in this way the current Ibits. If the control signal has a high value (1.2 V) the transistor is switched off and there is not current in the branch.

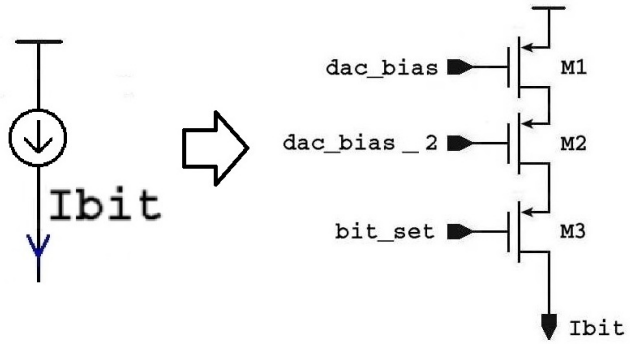


Figure 4.3: Transistor implementation of a single bit.

The scheme used for the DAC associates the low value of *bit_set* to an increment of the current generated and, therefore, it uses a negative logic. Since it could be useful to use the positive logic to increment the Idac current, the DAC contains a block of inverters. This block, depicted in Figure 4.4, is located between the four *bit_set* signals and the gates used as switches.

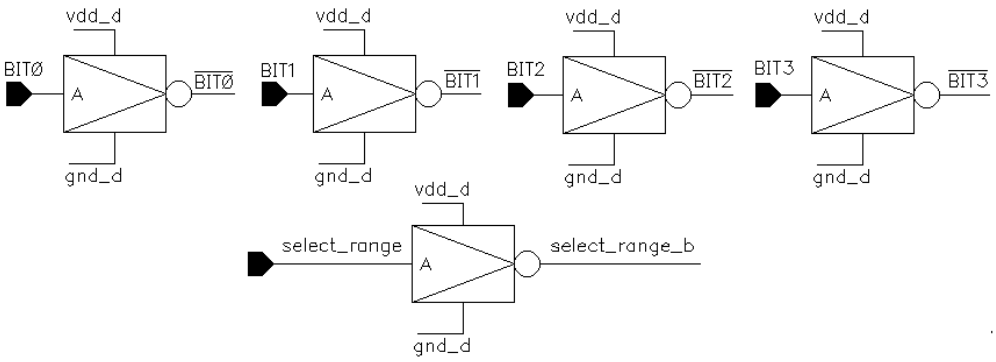


Figure 4.4: Inverters used to obtain the positive logic in the DAC.

The transistor block which realizes the fifth bit is depicted in Figure 4.5. The block is composed of a multiplexer with two select lines: *select_range* and *select_range_b*. Since, as shown in Figure 4.4, the signal *select_range* allows to obtain the signal *select_range_b* using an inverter, this signal allows to achieve a complete control of the multiplexer states. According to the value of *select_range*, the current Ibits is sent to one of the two outputs.

If *select_range*= 0, the transistors M1 and M2 works in linear region while M3 and M4 are inactive, therefore the current Ibits is sent to the output 1. In this case the DAC sources the current I_{DAC} to the node where the output line is connected.

Instead if *select_range*= 1, the transistors in linear region are M3 and M4 while M1 and M2 are inactive. In this case the current Idac is sent to the output 2 which is connected to the second block of Figure 4.5. This block is composed of 4 NMOS transistors connected in order to realize a current mirror which is switched on when the output 2 leads the Ibits current. In fact, in this condition due to the diode connections of M5 and M6, M7 and M8 are activated and the current I_{DAC} flows to ground. As a result the DAC sinks current from the node where it is connected.

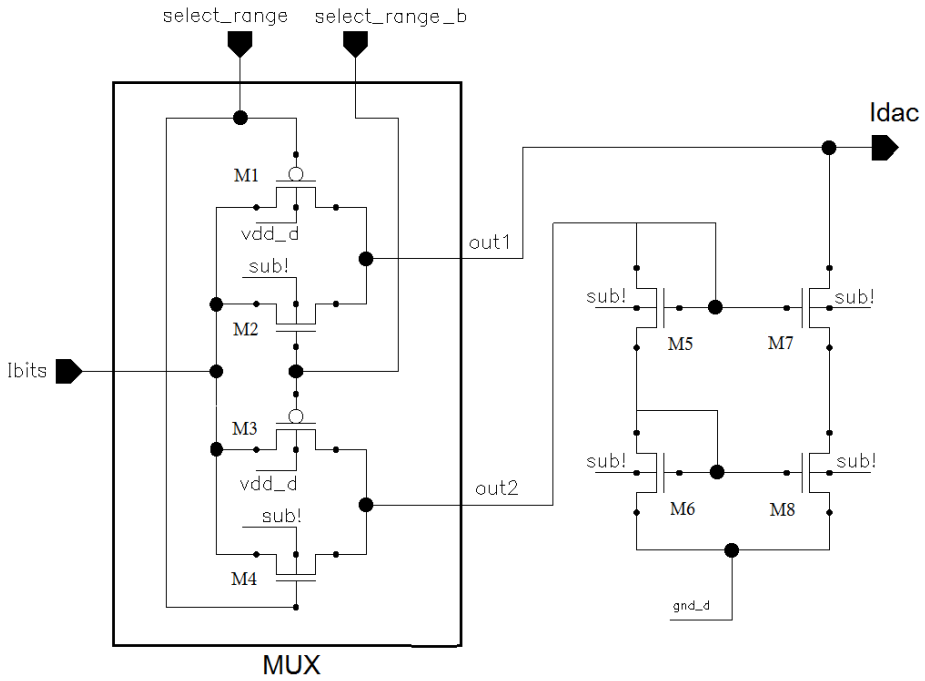
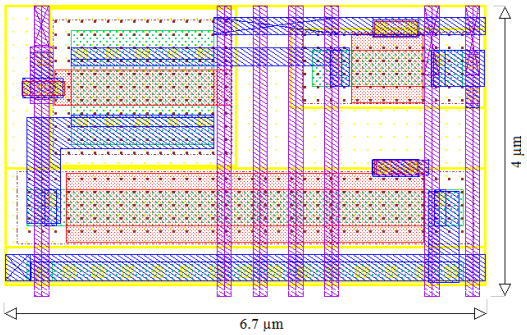
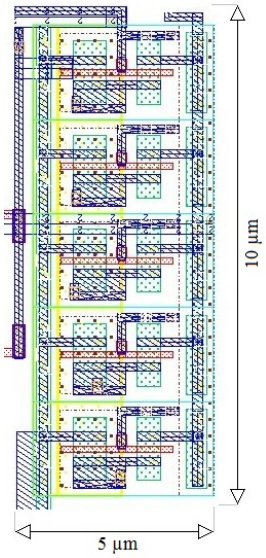


Figure 4.5: Transistor level implementation of the fifth bit

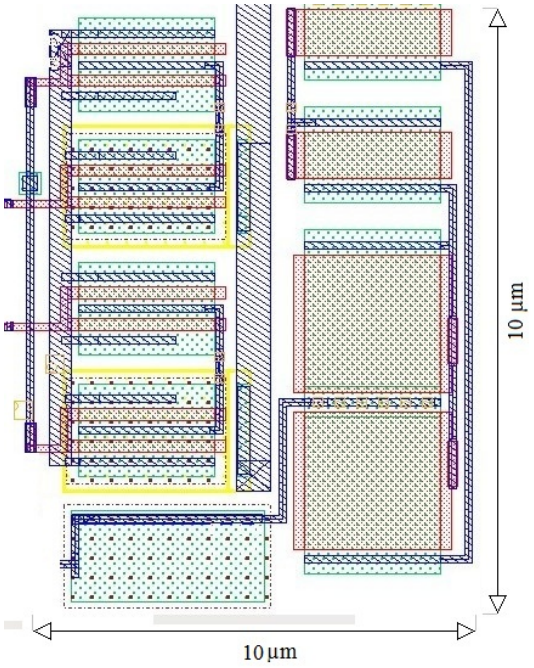
The layout of all the blocks described until now is very compact and it fits in a total area of 50 µm × 15 µm. A size of 6.7 µm × 4 µm is dedicated to the three transistors employed for implementation of a bit cell. This structure is repeated 15 times forming a compact design. Concerning the block used to change the logic, it fits in an area of 10 µm × 5 µm. The complete layout of the DAC is depicted in Figure 4.6



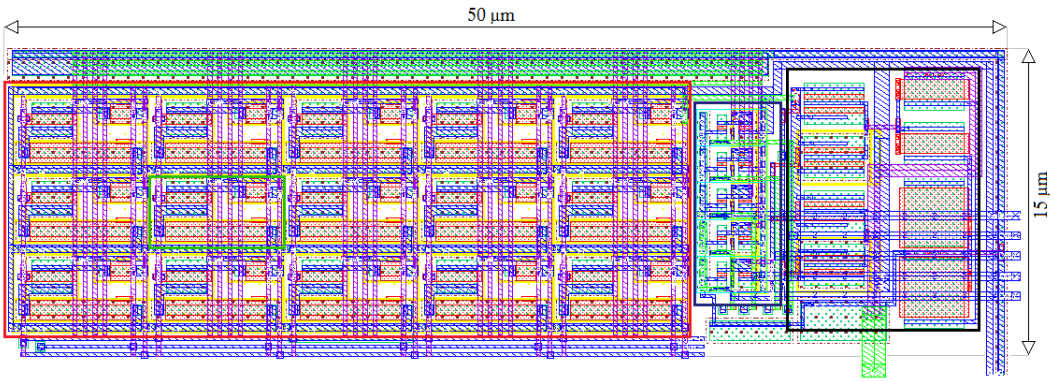
(a) Layout implementation of a bit.



(b) Block used to change the logic.



(c) Layout implementation to realize the fifth bit.



(d) Complete layout of the DAC in ToPix v3.

Figure 4.6: Layout and sizes of the blocks used to develop the DAC for ToPix v3. Figures (a), (b) and (c) show the size of the main blocks. In Figure (d) the green box shows a single bit in the group of 15 bits surrounded by the red box. The black and blue boxes show the position of the implementation of the fifth bit and the block to change logic, respectively.

4.2.2 *Simulation results*

The work done to study the DAC operation consists in some simulations made using the extracted layout of the DAC. The study aims to verify the linear relation between the bit code and the current I_{DAC} generated.

Figure 4.7 shows the current generated by the DAC for the 32 different codes. The simulation is made using a resistance of 1.3 MΩ for the biasing cell of the DAC, in order to set the LSB current to ~ 50 nA.

The results obtained with the signal *select_range*=1 are depicted on the top of Figure 4.7, while the ones obtained with the signal *select_range*=0 are illustrated at the bottom of the same Figure. During the simulation each binary code is sent to the DAC for a time sufficiently large (~ 2 µs) in order to observe the settling of the output signal. The Figure shows that spikes are present whenever the code changes. However, the duration of these transients is around 200 ns and thus it is acceptable because the DAC does not need to be fast.

The result obtained shows that the parasitic elements extracted from the layout do not affect the performance of the DAC, but for a more realistic simulation it is necessary consider also the effect of the neighbouring circuits. For this reason, the main circuits re tested using the extracted of the whole analogue pixel cell (see pag. 100).

Table 4.1 and the Figure 4.8 summarize the data obtained from this simulation. Observing the plot it is possible to note that there is a good linearity between the binary code and the current generated and therefore say that the non-linear effects do not come from the DAC.

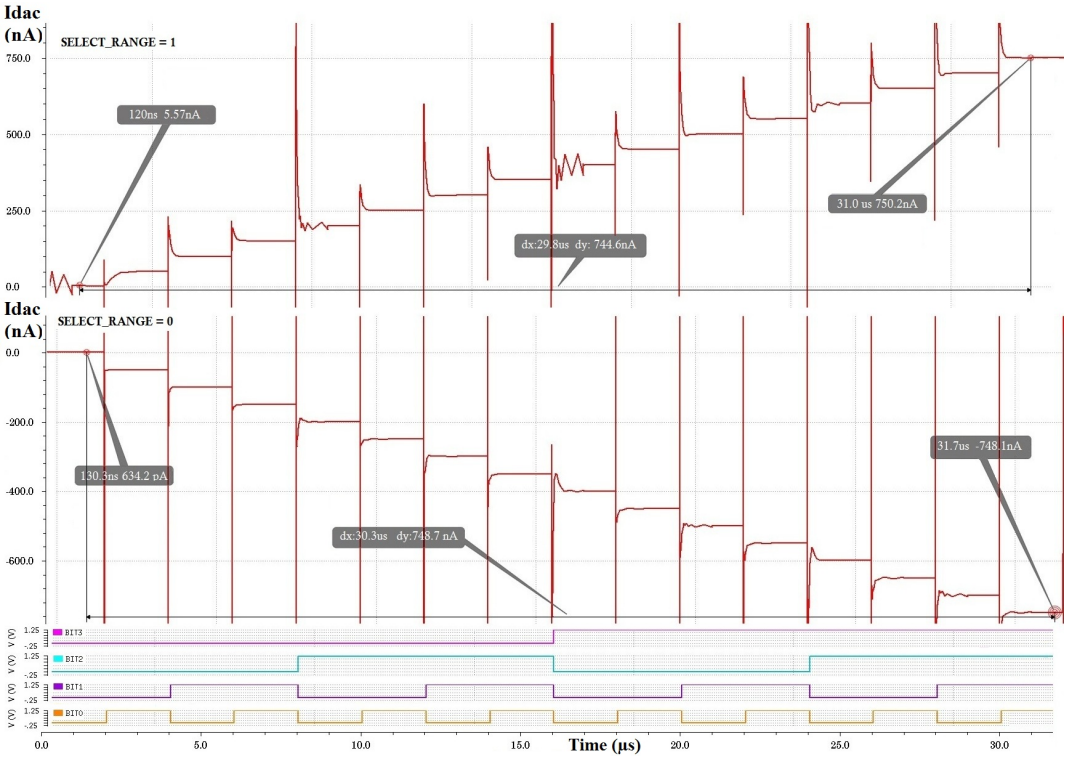


Figure 4.7: Idac current generated changing the binary code.

Idac CURRENT			
Binary code	**Idac [nA]**	**Binary code**	**Idac [nA]**
00000	1	1000	5
00001	-49	1001	54
00010	-100	1010	103
00011	- 149	1011	155
00100	- 201	1100	201
00101	- 250	1101	255
00110	-302	1110	302
00111	-352	1110	355
01000	-399	1110	405
01001	-450	1110	450
01010	-502	1110	505
01011	- 552	1110	557
01100	-598	1110	603
01101	- 650	1110	654
01110	- 701	1110	702
01111	-748	1111	750

Table 4.1: Simulation results of the current generated by the DAC.

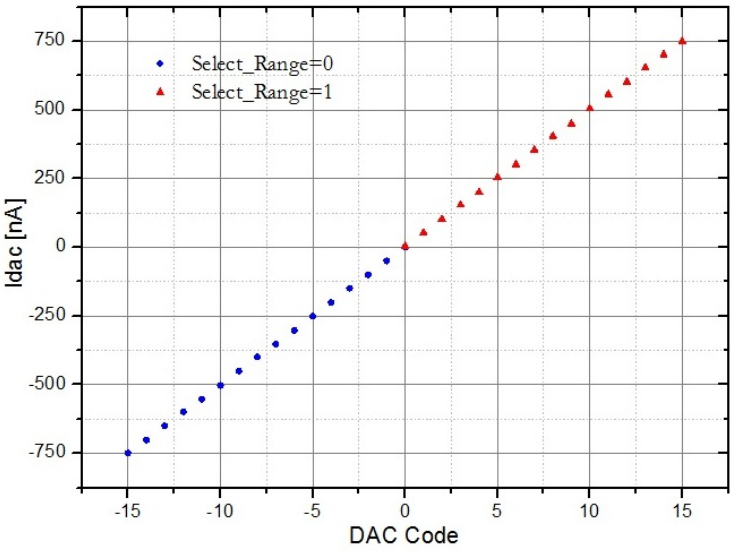


Figure 4.8: Idac current generated for binary codes from 0 to 15.

4.3 THE THRESHOLD VOLTAGE TUNING

The tuning system employed in ToPix v3 uses the DAC to unbalance the branches of the single stage differential amplifier of the comparator depicted in Figure 4.9. The DAC can sink or source current to the drain of the transistors M9 and M11.

If the DAC sources current, the drain voltage of M11 and, due to the diode connection, also the gate voltage of M11 and M12 increase. Due to this effect, when a current I_{DAC} is injected, the voltage to apply at one of the input transistors to obtain the same current in the two branches, changes of a quantity:

$$\Delta V = \frac{I_{DAC}}{g_{m1,2}} \tag{4.1}$$

The comparator commutes when the currents of the two branches have the same value. When the DAC sources current the voltage to apply at one of input nodes must be higher and thus the voltage threshold of the comparator (or trip point) is also higher if compared with the case that does not use the DAC. When the DAC sinks current, the opposite situation occurs and therefore the trip point decreases.

Formula (4.1) allows to obtain a linear relation between I_{DAC} and the ΔV but only for small values of I_{DAC}, where $g_{m_{1,2}}$ is constant, while for high values of I_{DAC}, $g_{m_{1,2}}$ changes and the result is a non-linear effect.

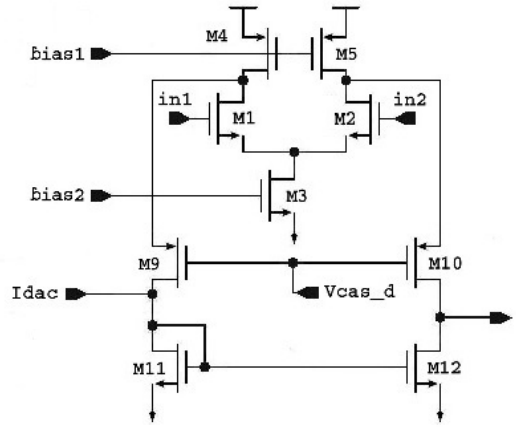


Figure 4.9: Partial implementation of the comparator of ToPix v3: the single stage differential amplifier.

Therefore, the basic idea of the tuning system consists in creating a difference between the current of the two branches. The mechanism used to create this difference is based on the variation of the current I_D due to the variation of the V_{DS} of the input transistors which is linear only when the transistors work in the saturation region.

Since the characteristic I-V of the transistors is non-linear, as shown in Figure 4.10, it is reasonable to expect non-linear effects for high values of the current generated by the DAC because it could generate large variations of the comparator bias current.

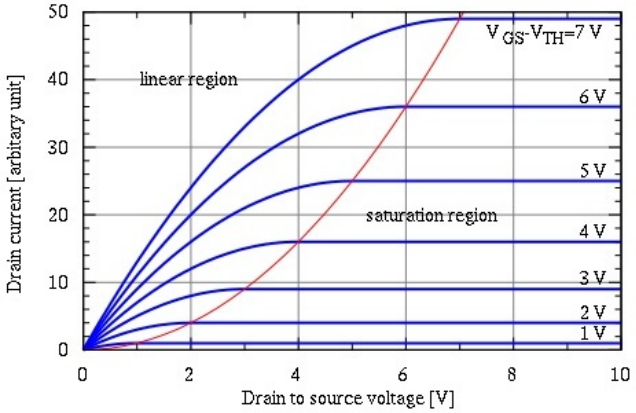


Figure 4.10: MOSFET drain current vs. drain-to-source voltage for several values of the overdrive voltage.

The non-linear effect has been observed testing the prototype. However, it is possible to simulate this effect to find a possible solution to linearize the response.

A simulation has been done to observe the output voltage of the comparator and the output of the single stage differential amplifier when the binary code of the DAC changes.

In figure 4.11 the blocks used for the simulation are shown.

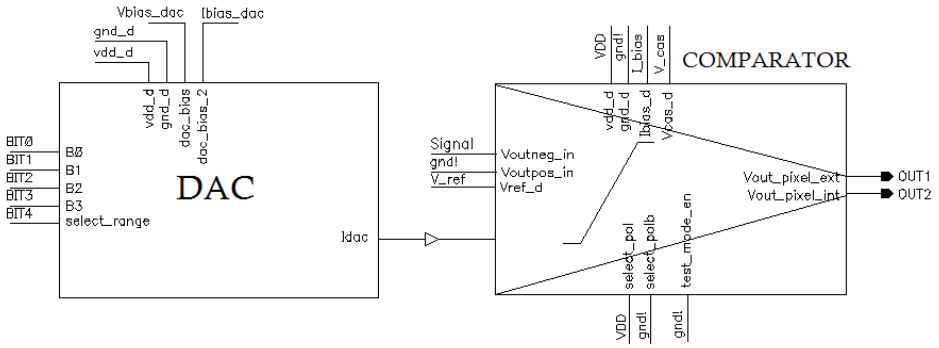


Figure 4.11: Block structure used in the simulations.

The whole system is simulated for both p-type and n-type polarities for comparison purposes. Table 4.2 resumes the comparator inputs for this two cases. A more detailed discussion about these inputs is given in Chapter 5.

COMPARATOR INPUTS			
Select_pol	**Polarity**	**IN1**	**IN2**
0	n-type	V_{CSA}	V_{REF}
1	p-type	V_{REF}	V_{CSA}

Table 4.2: Input polarities of the comparator.

The voltage reference is set to 700 mV and the signal V_{OUT} varies from 600 mV to 800 mV in order to observe a commutation.

Since in 1 is the non-inverting input of the comparator, for the p-type polarity it is expected a comparator output of 1.2 V when $V_{CSA} \leqslant V_{REF}$ and of 0 V when $V_{CSA} \geqslant V_{REF}$, as sketched in Figure 4.12.

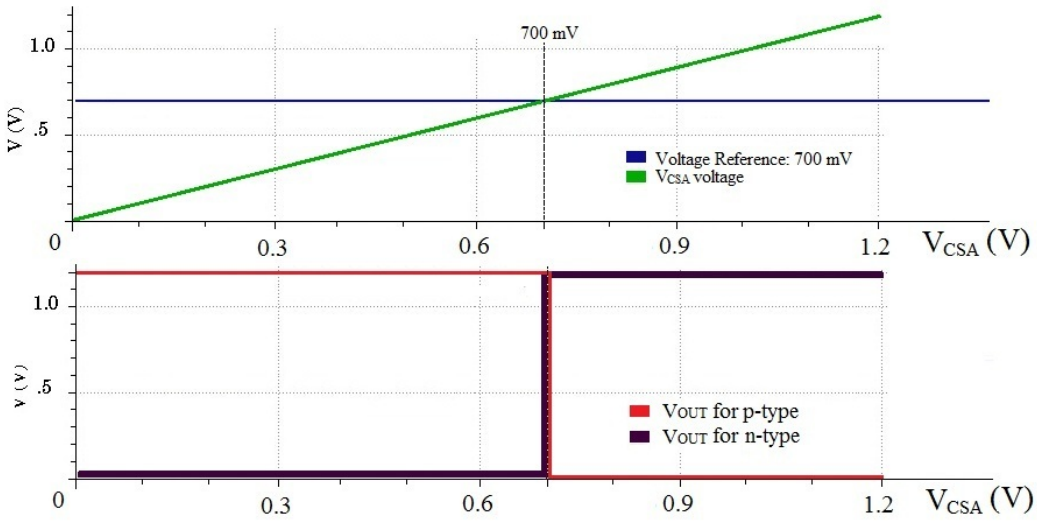


Figure 4.12: Comparator output expected for the polarities n-type and p-type with a voltage reference of 700 mV.

Figures 4.13 and 4.14 show the results obtained with p-type and n-type polarity, respectively.

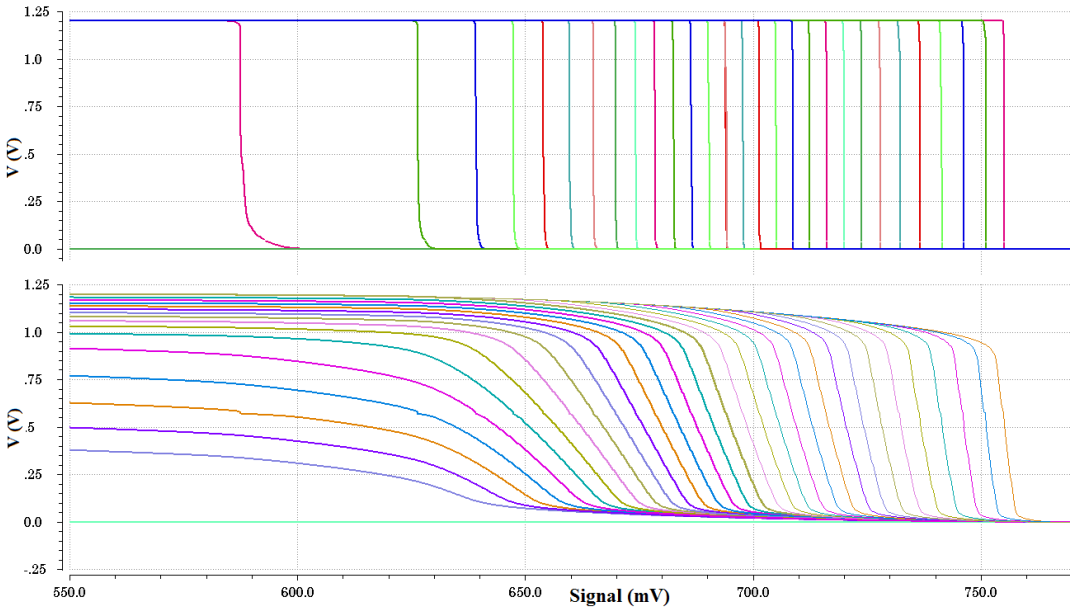


Figure 4.13: Output voltage of the comparator (top) and output of the single stage differential amplifier (bottom) for p-type polarity.

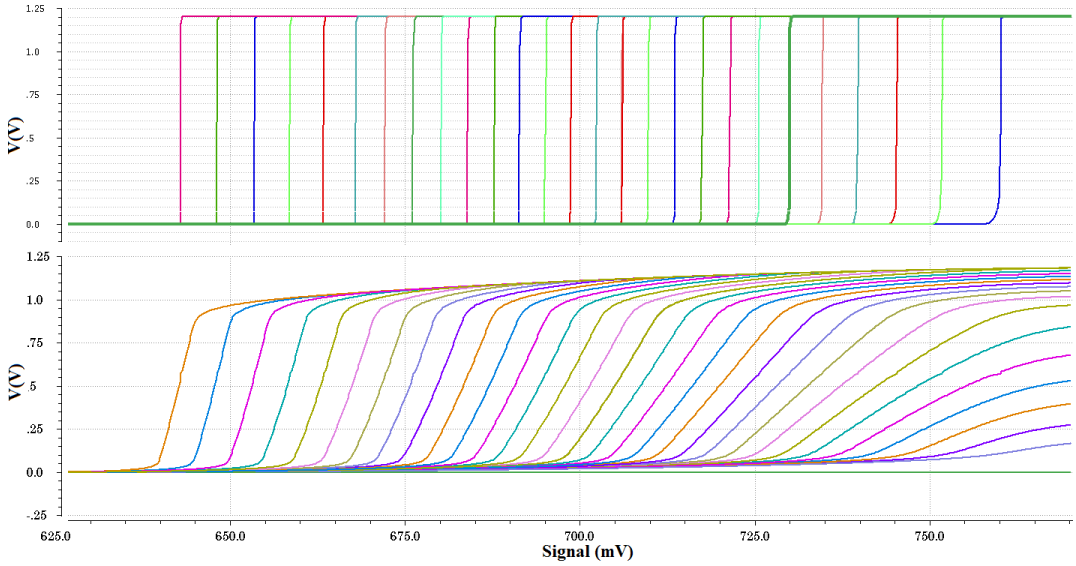


Figure 4.14: Output voltage of the comparator (top) and output of the single stage differential amplifier (bottom) for n-type polarity.

The trip point is defined as the voltage of V_{CSA} when the comparator output is 600 mV and it could be used as reference for comparison. The results obtained are summarized in Table 4.6 and 4.7 and depicted in Figure 4.15. The plots show the non linear effect which seems be more significant for high values of I_{DAC} current as expected.

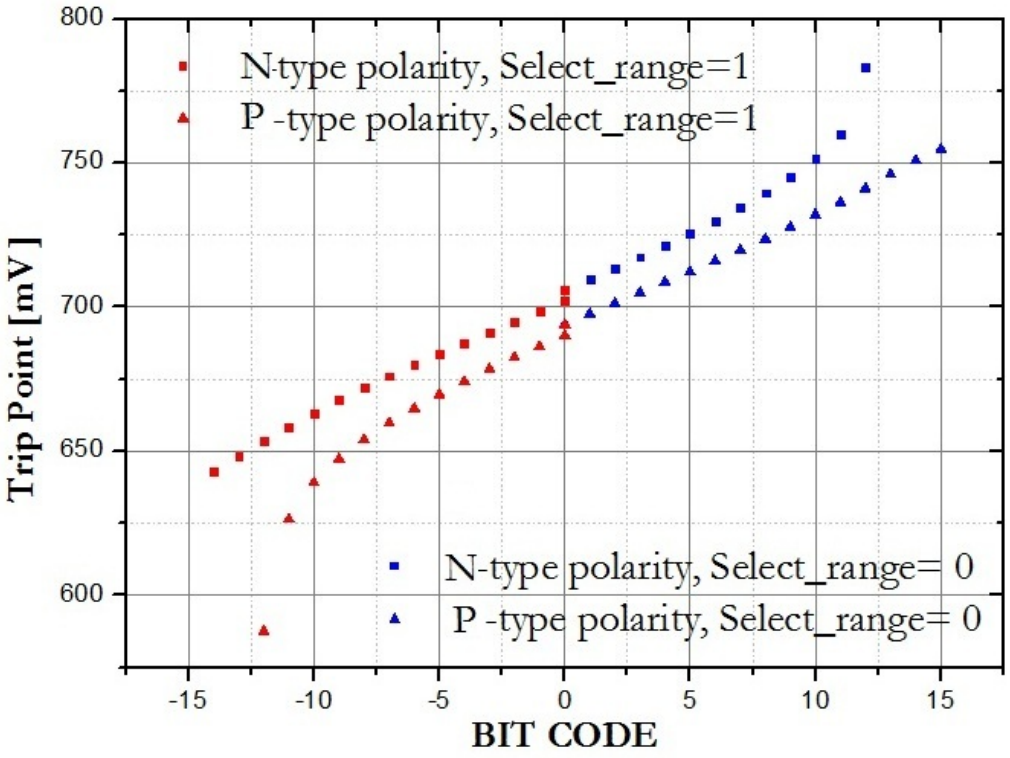


Figure 4.15: Trip points obtained with the DAC code variations for both polarities.

In Figure 4.15 it is possible to compare the behaviours of the two polarities. For the p-type polarity, which will employ voltage references around 700 mV, the trip point, when the DAC is inactive, presents an offset (~ 8 mV) to lower values, while for the n-type polarity the offset is lower (~ 4 mV) and to higher voltage values[1]. The Figure shows also how the non-linear effect is more relevant for the p-type polarity when *select_range* = 1 than for the n-type polarity when *select_range* = 0, but it is however always present.

A non linear response of the comparator threshold to the change in the DAC code makes the tuning procedure cumbersome. This can be a concern expecially for the final system, where each of the 10.5 million channels of the pixel detector must be calibrated. Therefore, the linearization of the threshold DAC is a highly desirable feature.

Trip Point with n-type polarity -			
Binary code	**Trip Point [mV]**	**Binary code**	**Trip Point [mV]**
00000	706.1	1000	702,3
00001	709.7	1001	698,7
00010	713,5	1010	695
00011	717,43	1011	691,3
00100	721,39	1100	687,7
00101	725,5	1101	683,9
00110	729,9	1110	680,1
00111	734,54	1110	676,1
01000	739,66	1110	672,1
01001	745,24	1110	667,9
01010	751,68	1110	663,3
01011	760	1110	658,5
01100	783,36	1110	653,5
01101	-	1110	648,1
01110	-	1110	642,9
01111	-	1111	-

Table 4.3: Simulation results of the trip point for the n-type polarity.

1 It is important to consider that for the simulation results it is not possible to estimate an error.

Trip Point with p-type polarity -			
Binary code	**Trip Point [mV]**	**Binary code**	**Trip Point [mV]**
00000	694,03	1000	690,19
00001	697,69	1001	686,34
00010	701,3	1010	682,49
00011	705	1011	678,46
00100	708,68	1100	674,17
00101	712,29	1101	669,7
00110	716,08	1110	664,92
00111	719,88	1110	659,74
01000	723,69	1110	653,97
01001	727,87	1110	647,33
01010	732,08	1110	639,15
01011	736,49	1110	626,36
01100	741,26	1110	587,6
01101	746,09	1110	-
01110	750,89	1110	-
01111	754,89	1111	-

Table 4.4: Simulation results of the trip point for the p-type polarity.

4.4 IDEA FOR THE LINEARIZATION CIRCUIT

The design specifications usually allow some freedom to the circuit designer on issues concerning the choice of a specific circuit topology, individual placement of the devices and the overall aspect ratio of the final design.

In this case instead the final aspect ratio of the final design is a very strong constraint. In fact, compared to ToPix v3, the analogue part of ToPix v4 presents some modifications in the layout which allow to insert a new device but with a maximum size of about 13 µm × 13 µm. However, since this free area is located close to the DAC it is possible to modify the DAC in order to combine the two circuits if necessary, increasing in this way the area available to built the circuit. The design of the circuit therefore is characterized by a strong size constraint which obliges to use a limited number of transistors to realize the circuit. For this reason the solution must be as simple as possible but has to respect also the other requirements of the ASIC, as the low power consumption.

The main design specifications of the circuit are summarized in Table 4.5.

DESIGN SPECIFICATIONS	
Technology	CMOS 0.13 µm
Circuit area	$<$ 13 µm × 13 µm
Power dissipation	$\sim$ 5 µW
Voltage supply	1.2 V
Polarity	n-type & p-type

Table 4.5: Design specifications of the linearization circuit.

Previously the linear relation between the I_{DAC} current and the DAC code has been verified and hence, the circuit to develop has to create a linear link between the I_{DAC} and the threshold voltage of the comparator. The basic idea to realize this linear link could be to use a linear device as a simple resistor.

The model to use to obtain the linear response might consists in sending the I_{DAC} current to the input of the linearization circuit, which should answer with a linear response in voltage on a line directly connected to one of the inputs of the comparator.

In this way one avoids sending the current into the comparator circuit which, as previously seen due to the transistor characteristic, generates non-linear effects.

A model which respects this conditions is depicted in Figure 4.16.

Here the current I_{DAC} is sent to a resistance which is connected by one end to a low impedance node (A). The node, which is kept at a fixed potential by a DC generator, must have a low impedance so that the associated voltage does not change when the DAC sources more current. Using this configuration, thanks to the linear characteristic of the resistance, it could be possible to reach the target of linearization.

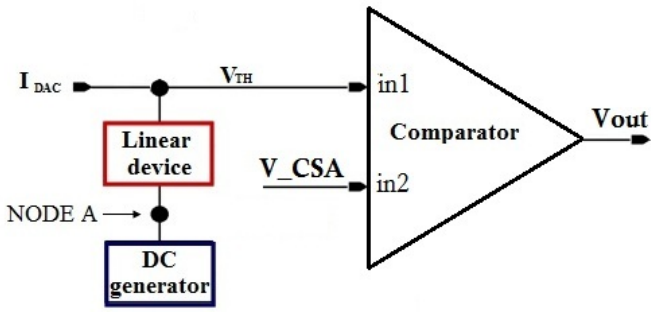


Figure 4.16: First model used to develop the linearization circuit.

The road followed to develop the final circuit starting from this simple model uses a top-down approach. The design starts implementing the model using ideal devices in order to verify the accuracy of the model. If the results obtained are correct, it means that the model works and it will be possible to replace the ideal devices with real devices in more steps until the desired result is achieved.

The model depicted in Figure 4.16 could be realized using a resistance as linear device and a DC generator which fixes the voltage at the node A.

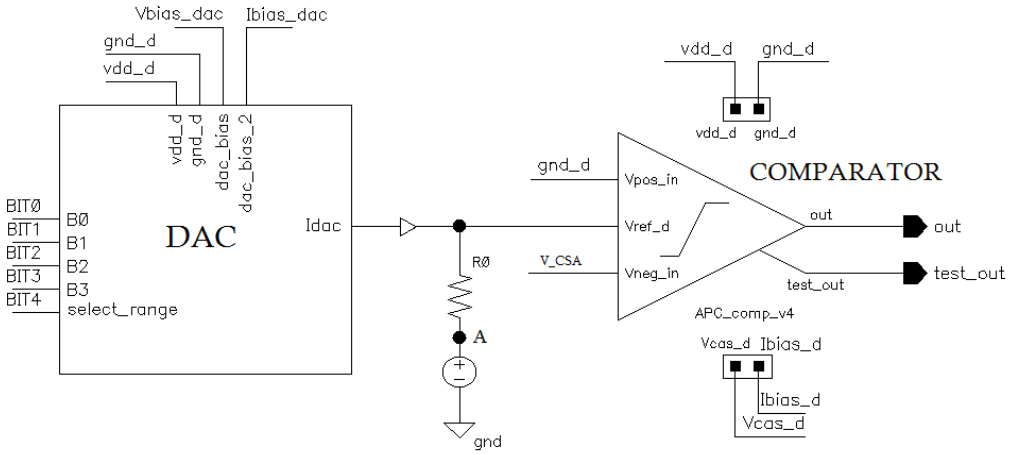


Figure 4.17: Block representation used to test the model.

The Figure 4.17 shows a block representation of the system employed to simulate the model. The DAC and the comparator used are the same of ToPix v3 and therefore the only two ideal devices in the model are the resistance, which could be then implemented easily with an integrated resistance, and the DC generator that is set to 700 mV.

Concerning the value of the resistance R, it should be the lowest possible in order to obtain a device with a reduced size, but on the other hand, it should be high enough to allow to get a reasonable swing for the voltage threshold also for the minimum current (LSB). Therefore, the choice of the R value requires a certain trade-off. The value of 50 kΩ is used for the simulations.

The simulations aim to verify the relation between the trip point and the DAC code and thus, as done in the previous section, the output voltage of the compara-

tor and the output of the single stage differential amplifier are analysed both for n-type and p-type polarity. With this setup when the DAC is inactive, the voltage reference is given by the value of the DC generator.

The outputs obtained changing the DAC code are depicted in Figure 4.18 and Figure 4.19, respectively.

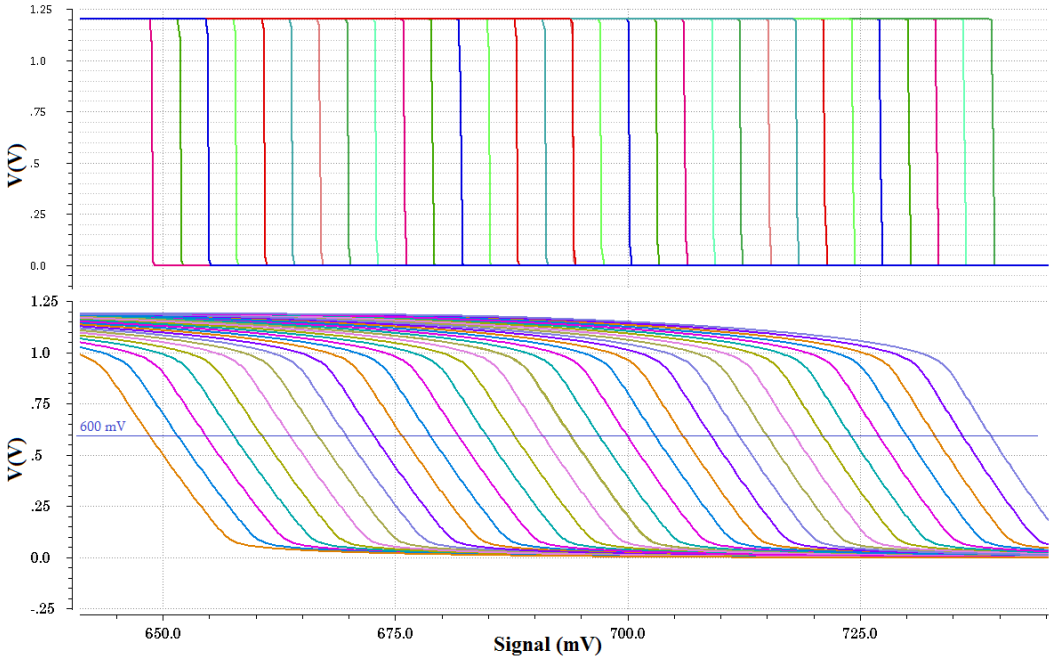


Figure 4.18: Model 1: Output voltage of the comparator (top) and output of the single stage differential amplifier (Bottom) for a p-type polarity.

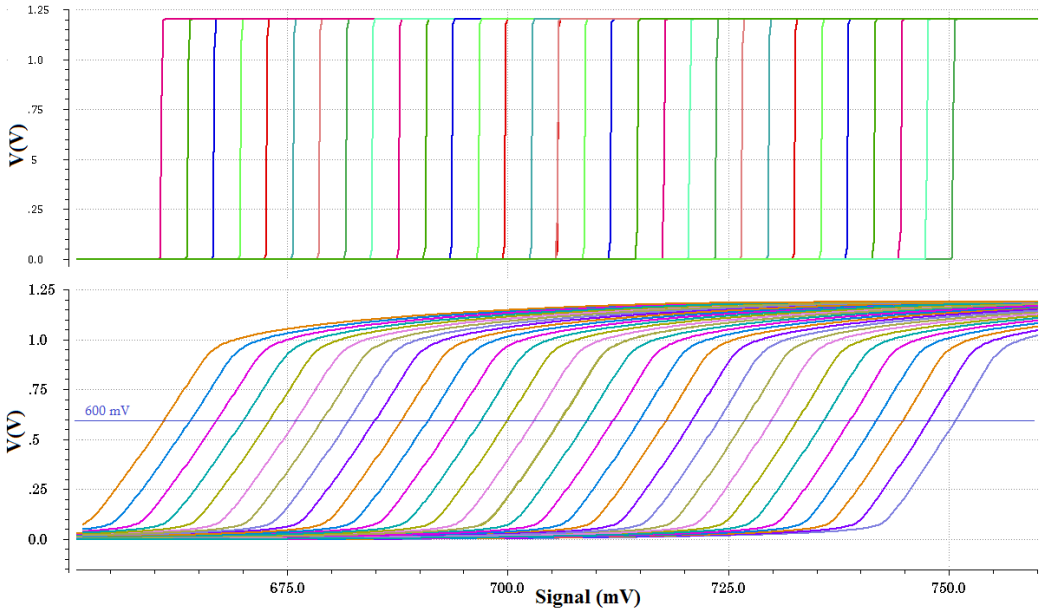


Figure 4.19: Model 1: Output voltage of the comparator (top) and output of the single stage differential amplifier (Bottom) for a n-type polarity.

The external resistance of the bias cell used to define the bit current, is set in order to observe the variation of the trip point for a large range to stress the non-linear effects, if they are present. The plots show that, contrary to the simulation of the configuration of ToPix v3, the comparator switches for all the DAC codes and that the distance between the signals seems to be constant. In order to verify the linearity, as done in the previous section, the trip point is used as a reference. Table 4.7 and Figure 4.20 illustrate the results obtained for the trip point.

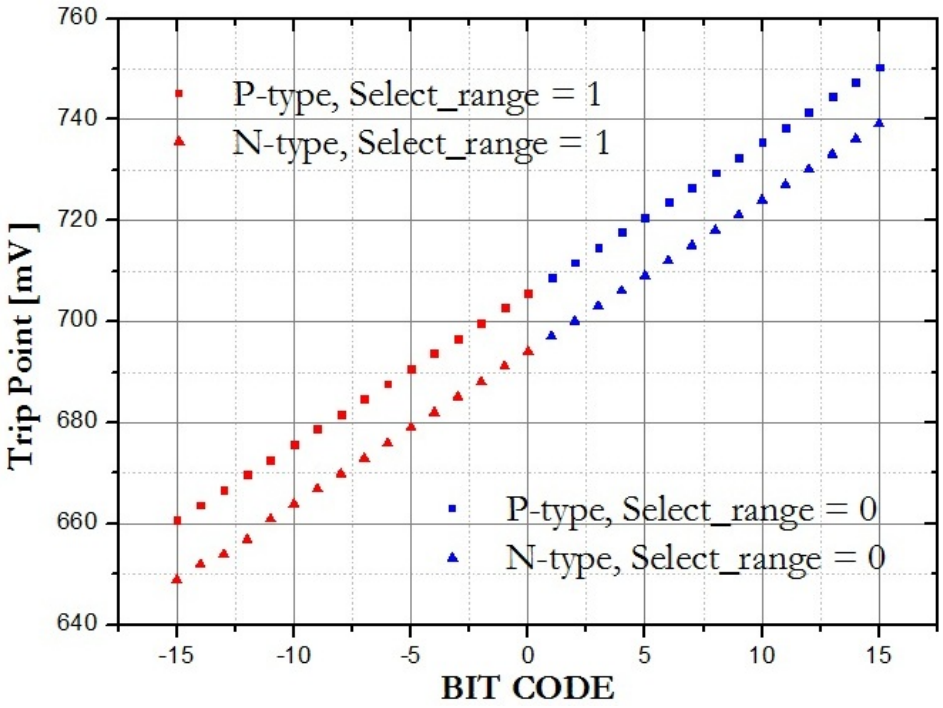


Figure 4.20: Results obtained with the ideal devices for the p-type and n-type polarity.

For a deeper analysis, using the data obtained from the Tables 4.6 and 4.7 and considering the DAC code as xdata and the trip point as ydata, it is possible to calculate the linear correlation coefficient ρ as follows [26]:

$$\sigma_X = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_i^2 - \mu_x^2)} \qquad \sigma_Y = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(y_i^2 - \mu_y^2)} \tag{4.2}$$

$$Cov_{Y,X} = \frac{1}{N}\sum_{i=1}^{N}(y_i - \mu_Y)(x_i - \mu_X) \qquad \rho = \frac{Cov_{Y,X}}{\sigma_Y \sigma_X} \tag{4.3}$$

The value calculated with (4.3) for both cases is 0.99 and therefore it is possible to assert that the relation between the two variables is linear.

The offset between the n-type and p-type polarity shown in the Figure underlines the not complete symmetry in the comparator. For both cases the offset is about 6 mV if compared with the voltage threshold, but for the p-type polarity it is lower while for the n-type it is higher.

Since the result obtained is satisfactory, it is possible to continue the design looking for a real device which can replace the ideal DC generator.

Trip Point with p-type polarity -			
Binary code	**Trip Point [mV]**	**Binary code**	**Trip Point [mV]**
00000	705.7	1000	705,7
00001	708.7	1001	702,7
00010	711,7	1010	699,7
00011	714,7	1011	696,7
00100	717,7	1100	693,7
00101	720,6	1101	690,7
00110	723,6	1110	687,7
00111	726,5	1110	684,7
01000	729,5	1110	681,7
01001	732,5	1110	678,7
01010	735,5	1110	675,7
01011	738.5	1110	672,7
01100	741,5	1110	669,7
01101	744.5	1110	666,7
01110	747.5	1110	663,7
01111	750.4	1111	660.8

Table 4.6: Simulation results of the trip point for the p-type polarity.

Trip Point with n-type polarity -			
Binary code	**Trip Point [mV]**	**Binary code**	**Trip Point [mV]**
00000	694,1	1000	694,1
00001	697,1	1001	691,1
00010	700,1	1010	688,1
00011	703,1	1011	685,1
00100	706,1	1100	682,0
00101	709,1	1101	679,0
00110	712,1	1110	675,9
00111	715,1	1110	672,9
01000	718,1	1110	669,9
01001	721,1	1110	666,9
01010	724,1	1110	663,9
01011	727,1	1110	660,9
01100	730,2	1110	656,9
01101	733,2	1110	653,9
01110	736,2	1110	651,9
01111	739,2	1111	648,9

Table 4.7: Simulation results of the trip point for the n-type polarity.

4.4.1 *Voltage amplifier model*

To develop the circuit it is now necessary to implement the ideal DC generator using only real devices. The limited number of transistors to employ is an important constraint to remember when the architecture is chosen.

Concerning the design specifications, the circuit must fix the voltage at the output node which must have a low impedance. Since the circuit is not used to send signals, the delay time is not so important but the stability must be verified.

An architecture proposed which respects these requirements is depicted in Figure 4.21. It implements a voltage reference based on a differential amplifier, a PMOS transistor and an ideal current source.

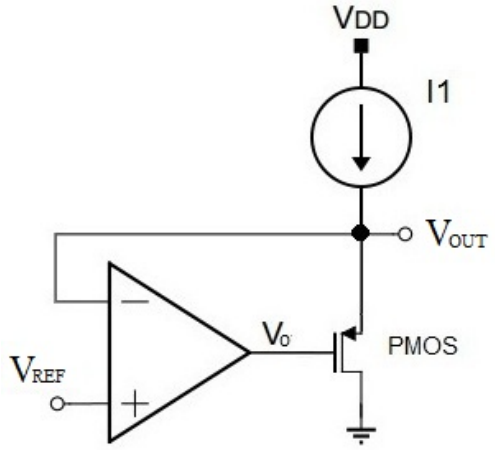


Figure 4.21: Voltage reference based on PMOS.

Using this model and considering a gain A for the differential amplifier it follows that [27][28]:

$$V_O = (V_{REF} - V_{OUT}) \cdot A \tag{4.4}$$

If the transistor works in the saturation region:

$$(V_{SG})_{PMOS} \simeq \sqrt{\frac{2 \cdot I_{SD}}{\mu_P \cdot C_{OX}} \left(\frac{L}{W}\right)} + |V_{TH_P}| = constant = K \tag{4.5}$$

$$(V_{GS})_{PMOS} = V_O - V_{OUT} \tag{4.6}$$

Using (4.4), (4.6) and (4.5) is possible to obtain the expression for V_{OUT}:

$$V_{OUT} \simeq \frac{V_{REF} \cdot A - K}{A + 1} \tag{4.7}$$

If the gain amplifier is high the relation becomes:

$$V_{OUT} \simeq V_{REF} \tag{4.8}$$

4.4.1.1 *The first solution*

The first solution studied aims to overcome the area constraint of the pixel using a DC generator in a bias cell located outside the pixel. In this way it is possible to use bigger transistors to reduce the mismatch effects as well as to use more devices. This solution foresees only the resistance in the pixel as depicted in Figure 4.22.

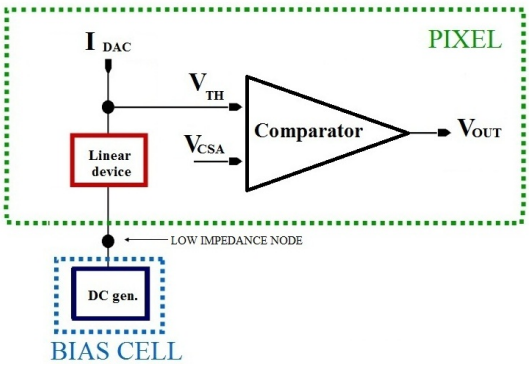


Figure 4.22: First model used to develop the voltage reference.

Figure 4.23 shows a schematic which implements the real DC generator for this model. The single stage differential amplifier uses large transistors (T0, T1, T2 and T3) in order to reduce the mismatch effects. The ideal current source of the model in Figure 4.21 is realized using a current mirror with the transistor T6, while the PMOS of the model is the transistor T9.

Since the gate of T2 is the inverting input of the differential amplifier, the feedback is realized connecting this node to the source of T9.

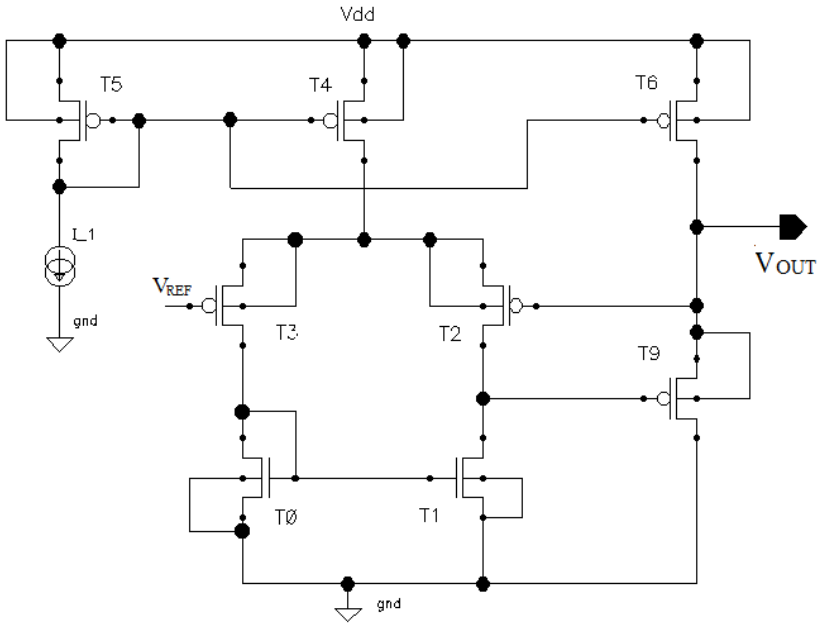


Figure 4.23: Transistor level implementation of the first analyzed solution.

4.4.1.2 *The second solution*

The second solution uses the same main model but it aims to develop all the circuit in the area available in the pixel cell following the scheme of Figure 4.24.

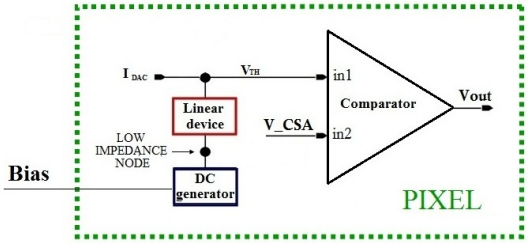


Figure 4.24: Second model used to develop the linearization circuit.

Since the whole circuit must fit in a limited area, the transistor implementation has to use a reduced number of devices as well as small sizes. In order to cope with these requirements the model foresees the use of a voltage bias which comes from the bias cell located outside the pixel.

The circuit proposed in Figure 4.25 implements the DC generator. The circuit uses an internal feedback realized by the transistors T1, T2 and T3 which allows to obtain a low impedance node. The transistors size is chosen using the results of Monte Carlo simulations in order to optimize its performance.

In spite this solution uses less transistors than the previous one, it has the disadvantage to depend by an external biasing connected to the gate of T3 which changes the value of the Vout. Since in general the bias voltage and the v_{OUT} are different, this solution appears less flexible than the first one described.

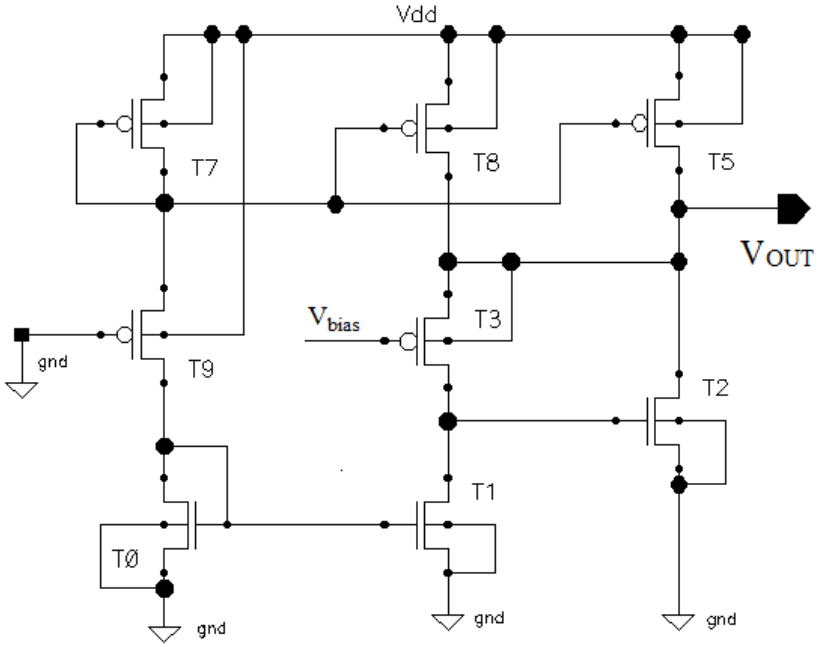


Figure 4.25: Transistor implementation of the second analyzed solution.

4.4.1.3 *Simulation results*

The results of Monte Carlo simulations are considered a good way to compare the two solutions analyzed. Therefore, for both Monte Carlo simulations are performed to study the dispersion of the voltage at the low impedance node with 250 runs. For each of them, the simulation considers process and mismatch, only process and only mismatch effects.

For both circuits the voltage of the output node is set to 700 mV. For the first solution this is done sending 700 mV at the gate of the transistor T3 while for the second solution is done using a bias voltage for T3 of about 510 mV.

The results obtained from these simulations are summarized in Table 4.8 and are depicted in Figures 4.26 and 4.27

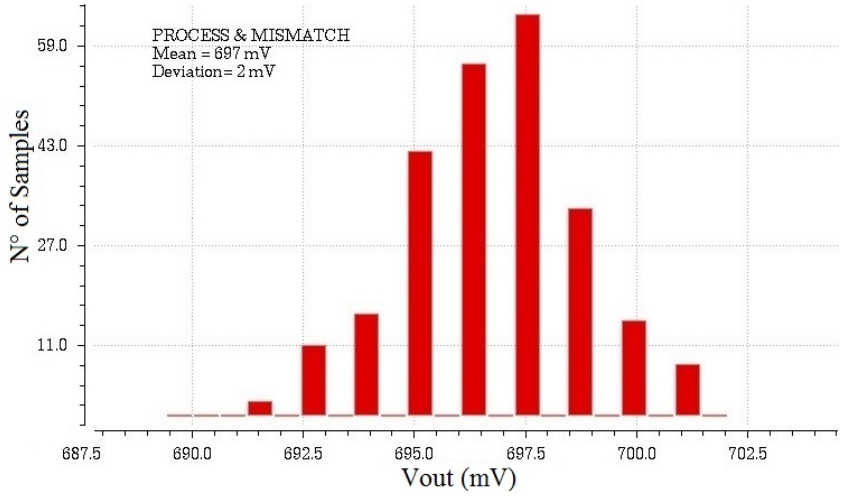
SIMULATION RESULTS - FIRST CIRCUIT -		
	Mean [mV]	**Standard Deviation [mV]**
Process & Mismatch	697	2
Mismatch	697.2	1.9
Process	697.2	0.1
SIMULATION RESULTS - SECOND CIRCUIT -		
	Mean [mV]	**Standard Deviation [mV]**
Process & Mismatch	702	11
Mismatch	700	2
Process	700	11

Table 4.8: Monte Carlo simulation results obtained with the first two circuits.

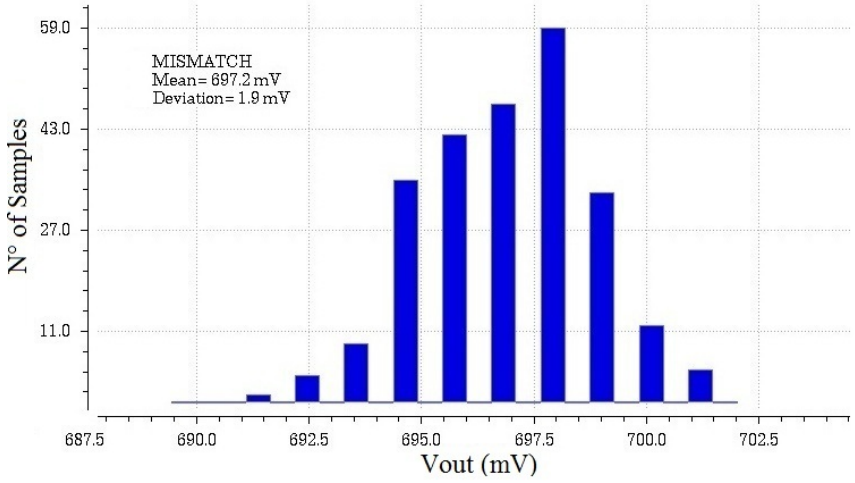
Simulations show that for the first solution the process effects are negligible and the mismatch is limited to 2 mV. However, the mean value is lower than the one expected (700 mV). This is justified because the gain of the amplifier is not so high. This first solution might appear attractive because the offset performed is good but unfortunately, this solution requires to have common line to distribute the reference voltage to all the pixels in a column. The current of all the DACs would flow in this line, and an unacceptable voltage drop will be generated. In fact, the resistance of a metal line 1 cm long can be high as high as 1 kΩ. For this reason this solution is rejected.

Concerning the second solution, the mean voltage corresponds to the expected value and the mismatch effects are limited to 2 mV as the first solution but the process effects are very high. However, since all the pixels belong to the same process, this parameter is less important than the mismatch. This second solution could appears acceptable but since the voltage output depends on the biasing, which must be given from the external bias cell, also this solution is rejected.

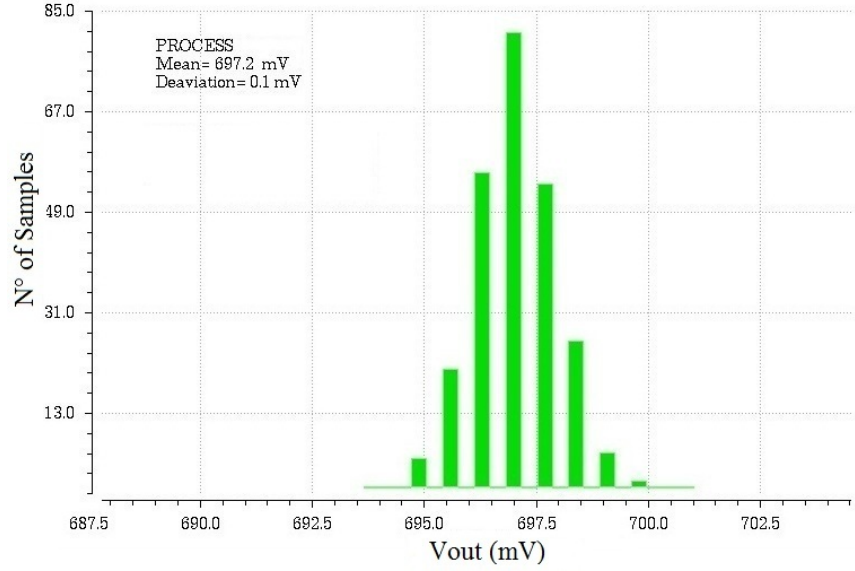
However, since both circuits contains good features, they could be use to develop a hybrid solution as will be explained in the next section.



(a) Monte Carlo simulation: Process & Mismatch

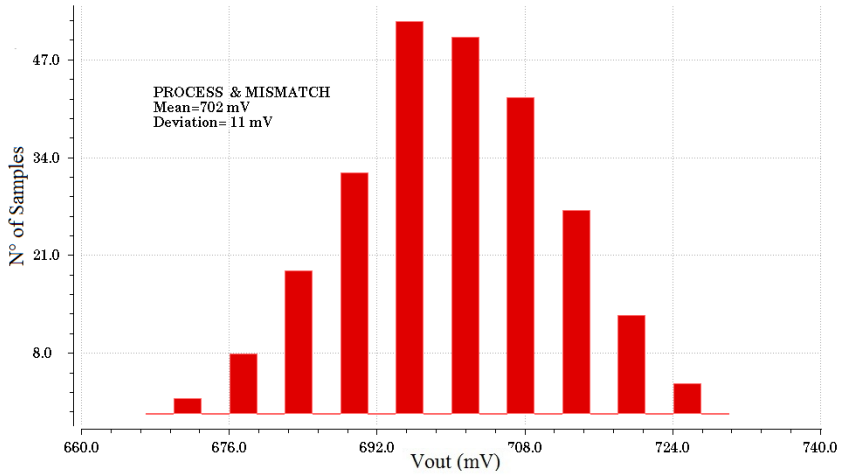


(b) Monte Carlo simulation: Mismatch

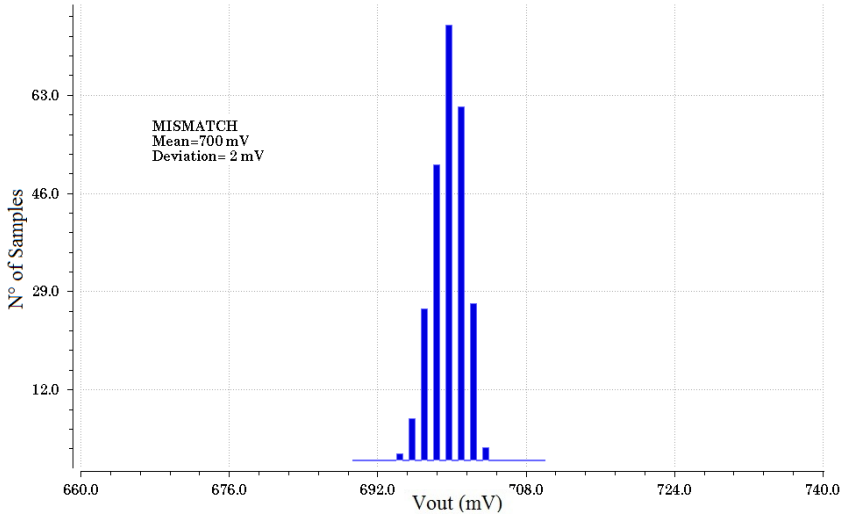


(c) Monte Carlo simulation: Process

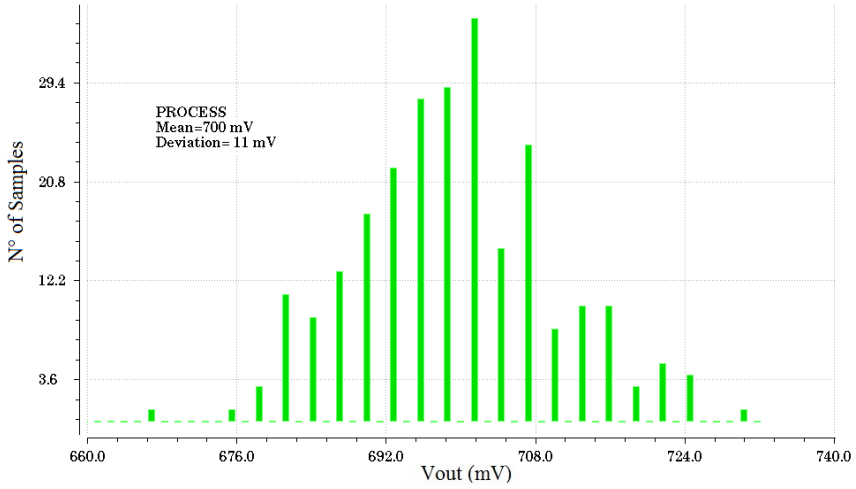
Figure 4.26: Monte Carlo Simulations for Vout of the first solution proposed.



(a) Monte Carlo simulation: Process & Mismatch



(b) Monte Carlo simulation: Mismatch



(c) Monte Carlo simulation: Process

Figure 4.27: Monte Carlo Simulations for Vout of the second solution proposed.

4.4.2 *Transconductance amplifier model*

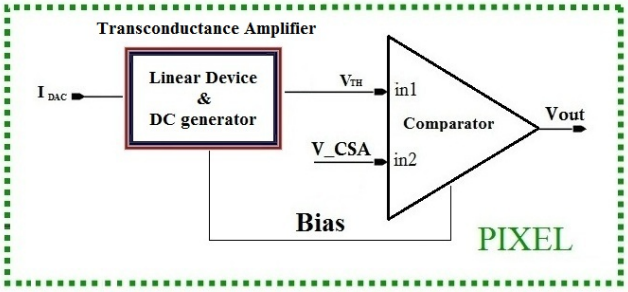


Figure 4.28: Final model used to develop the linearization circuit.

Figure 4.28 shows a model which contains features of the two models analyzed previously. It consists in a transconductance amplifier which contains both the DC generator and the resistance to realize the linearization. The amplifier receives in input I_{DAC} and generates the voltage threshold V_{TH} to send to the comparator. In this model, as in one of the two solutions previously analysed, is also foreseen a bias which allows to use less transistors and develop the whole circuit in the pixel.

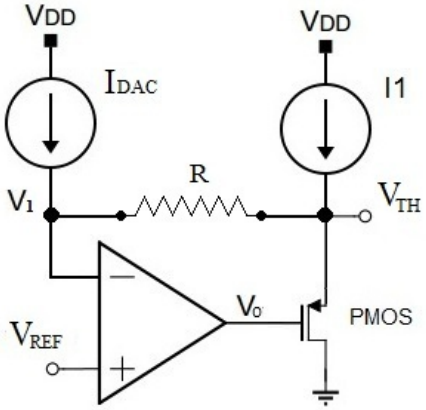


Figure 4.29: Transconductance amplifier model.

The transconductance amplifier can be realized using the schematic representation depicted in Figure 4.29. It reuses the idea based on the single stage differential amplifier connected to the gate of a PMOS transistor but it contains also the linear device which is connected in feedback between the output node and the input node. A good feature of this configuration consists in using a low impedance node to connect the DAC. Due to this feature, the voltage at this node is constant even if the current sourced by the DAC changes. In this way, changing the DAC code, the voltage at the drain node of all the transistors, used as switches for the DAC bits (see Figure 4.3), does not change and therefore it is reasonable to consider the DAC and the amplifier circuit as independent devices. Moreover, as required according to the specifications, since all the current sourced by the DAC flows although in the resistance, the voltage V_{TH} changes linearly. In fact, considering a gain A for the differential amplifier, follows that [27][26]:

$$V_O = (V_{REF} - V_1) \cdot A \tag{4.9}$$

Since all the current I_{DAC} flows through the resistance R, it is possible to obtain the voltage V_1:

$$V_1 - V_{TH} = R \cdot I_{DAC} \tag{4.10}$$

$$V_1 = V_{TH} + R \cdot I_{DAC} \tag{4.11}$$

If the PMOS transistor works in the saturation region, the current I_{SD} is given by:

$$I_{SD} = I_1 + I_{DAC} \simeq \frac{1}{2}\mu_P \cdot C_{ox} \cdot \left(\frac{W}{L}\right)(V_{SG} - |V_{TH_P}|)^2 \tag{4.12}$$

which, calling k all the constant terms, can be written as:

$$I_{SD} \simeq k \cdot (V_{SG} - |V_{TH_P}|)^2 \tag{4.13}$$

Equation (4.13) allows to obtain the expression of V_0:

$$V_{SG} = V_S - V_G = V_{TH} - V_0 \simeq \sqrt{\frac{(I_{SD} + I_{DAC})}{k}} + |V_{TH_P}| \tag{4.14}$$

$$V_O \simeq V_{TH} - \sqrt{\frac{(I_{SD} + I_{DAC})}{k}} - |V_{TH_P}| \tag{4.15}$$

Using (4.9), (4.11) and (4.15) it is possible to obtain the expression of V_{TH} as follows:

$$V_{TH} - \sqrt{\frac{(I_{SD} + I_{DAC})}{k}} - |V_{TH_P}| = (V_{REF} - V_{TH} + R \cdot I_{DAC}) \cdot A \tag{4.16}$$

$$V_{TH} \cdot (1 + A) = (V_{REF} + R \cdot I_{DAC}) \cdot A + \sqrt{\frac{(I_{SD} + I_{DAC})}{k}} + |V_{TH_P}| \tag{4.17}$$

$$V_{TH} = (V_{REF} + R \cdot I_{DAC}) \cdot \frac{A}{1 + A} + \frac{1}{1 + A}\left[\sqrt{\frac{(I_{SD} + I_{DAC})}{k}} + |V_{TH_P}|\right] \tag{4.18}$$

Equation (4.18) gives the analytic expression for the output of the transconductance amplifier when the PMOS transistor works in saturation.

Considering a limit condition where the gain A is high, the two elements of the Formula (4.18) become:

$$\lim_{A \mapsto \infty} (V_{REF} + R \cdot I_{DAC}) \cdot \frac{A}{1 + A} \to (V_{REF} + R \cdot I_{DAC}) \tag{4.19}$$

$$\lim_{A \mapsto \infty} \frac{1}{1 + A}\left[\sqrt{\frac{(I_{SD} + I_{DAC})}{k}} + |V_{TH_P}|\right] \to 0 \tag{4.20}$$

Therefore, when the differential amplifier has a high gain, the ouput V_{TH} can be written as:

$$V_{TH} \simeq (V_{REF} + R \cdot I_{DAC}) \tag{4.21}$$

The Formula (4.21) shows how the proposed model allows to obtain a linear relation between I_{DAC} and V_{TH} and underlines the importance of the value of the resistance R used as feedback.

However, the linearization is obtained at the cost of giving up the fifth bit of the DAC. In fact, in the scheme described, the current can flow through the resistance only from the input node V_1 to the output node V_{TH} and therefore works only if the DAC sources current. This limit imposes to reduce the number of levels from 32 to 16. However, this reduction is consider less important than the linearization of the threshold voltage of the comparator and moreover it allows to obtain more silicon area available to develop the circuit.

The transistor implementation used to realize the circuit is illustrated in Figure 4.30. The circuit uses a cascode differential amplifier, which is similar to the one used for the first circuit described, with the exception of the cascode transistors which is employed to increase the gain of the amplifier. The gain with this configuration is given by:

$$A = g_{1m}(r_{02}//(r_{03} + r_{04})) \tag{4.22}$$

The circuit contains also a capacitance which allows to guarantee the stability of the amplifier. The value chosen for the capacitance is $\sim$ 400 fF.

Concerning the bias voltage, it is given from a transistor located in the comparator and it is connected to the gate of T10 implementing a current mirror. The bias chosen makes a current of about 500 nA flow through transistor T10. Transistors T11, T9 and T8 realize current mirrors which supply the circuit. As show in the schematic, the resistance is located between the inverting input of the differential amplifier and the source of the PMOS T17.

Simulations indicate the transistors T1, T2, T4 and T5 as the ones which influence more the mismatch so that they have been designed with a larger size.

Table 4.9 summarizes the devices sizes used for the circuit.

An important consideration must be done concerning the range of V_{REF} where the performance of the circuit is optimal: for voltages over 500 mV the V_{SD} is large enough to guarantee to T7 to work in the saturation region, hence the circuit works properly. Instead, for values below 500 mV transistor T7 starts to enter in the linear region and in this case (4.21) is not more valid. Therefore a worse performance of the device is expected with values of V_{REF} below 500 mV. However, the size of T7 is chosen in order to limit this dependence allowing an acceptable performance of the device also for low reference voltages, as needed to work with n-type polarities.

As done for the previous circuits, in order to analyze the performance of the device, three kinds of Monte Carlo simulations are performed. These simulations aim to study the dispersion of V_{TH} when V_{REF} is set to 700 mV.

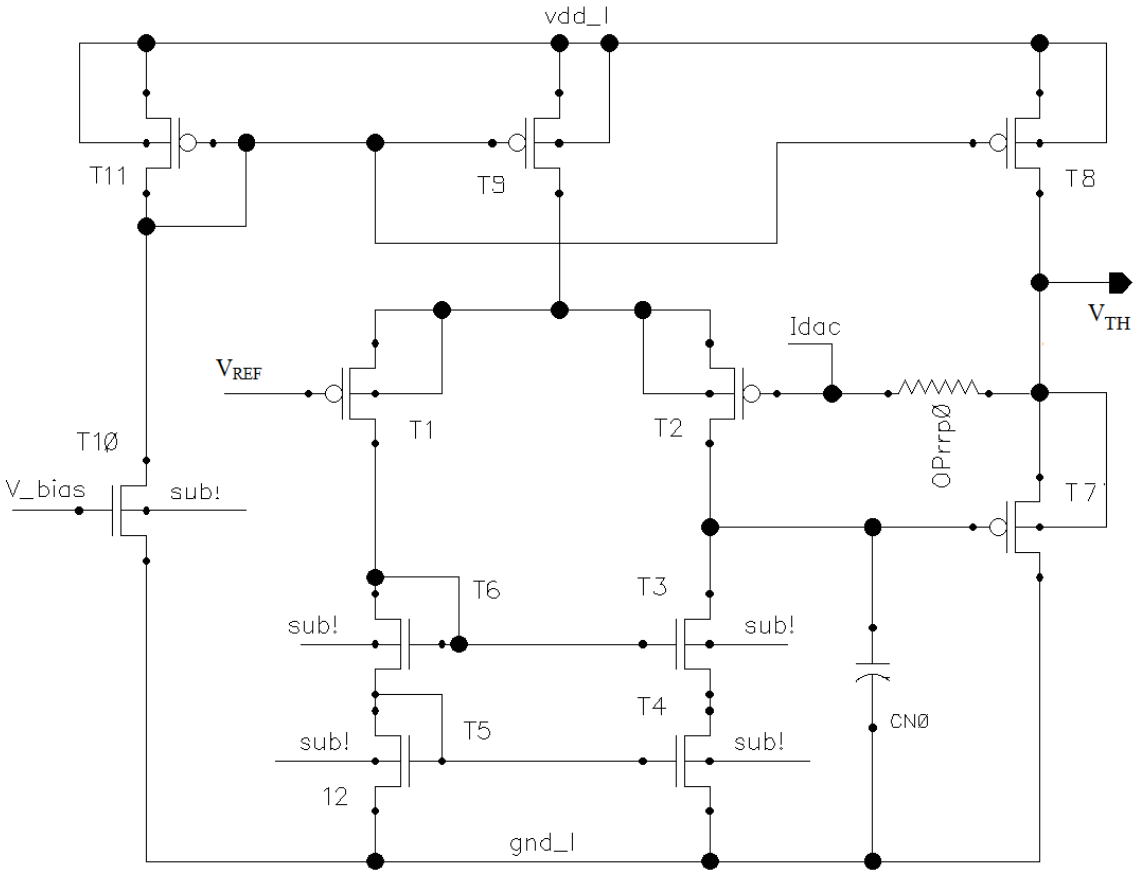


Figure 4.30: Final model used to develop the linearization circuit.

Device	Type	W [μm]	L [μm]	Device	Type	W [μm]	L [μm]
T1	PMOS	10	1	T7	PMOS	2	0.5
T2	PMOS	10	1	T8	PMOS	2	0.5
T3	NMOS	2	0.3	T9	PMOS	2	0.5
T4	NMOS	10	2	T10	NMOS	1	1
T5	NMOS	10	2	T11	PMOS	2	0.5
T6	NMOS	2	0.3				

Device	Type	W [μm]	L [μm]	Value
R	Resistance 1	0.740	10	24 kΩ
R	Resistance 2	0.740	10	24 kΩ
C	Capacitor	12	3	396 fF

Table 4.9: Transistor, resistance and capacitance parameters used for the circuit.

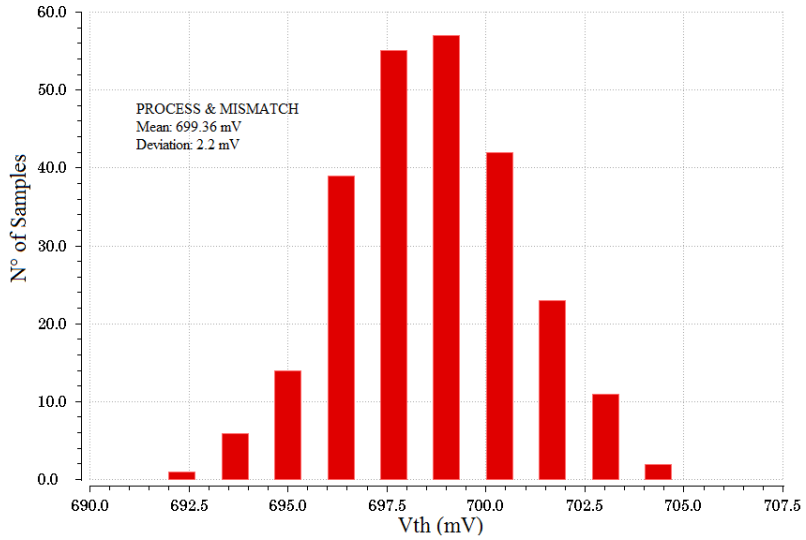
The results obtained for 250 runs are resumed in Table 4.10 and in Figure 4.31.

SIMULATION RESULTS		
	Mean [mV]	**Standard Deviation [mV]**
Process & Mismatch	699.4	2.2
Mismatch	699.4	0.6
Process	700	2

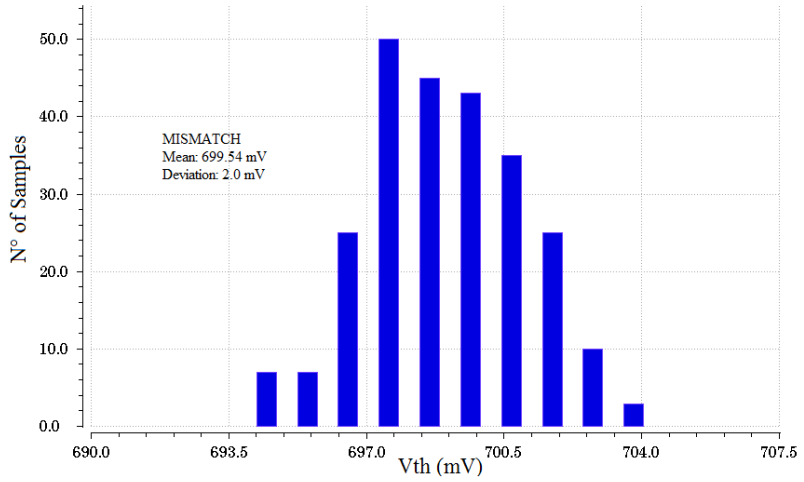
Table 4.10: Monte Carlo simulation results of V_{TH}.

Simulation results show a dispersion due to mismatch and process limited to values of 0.6 mV and 2.2 mV, respectively, and an optimal control of the output voltage which is very close to the expected value.

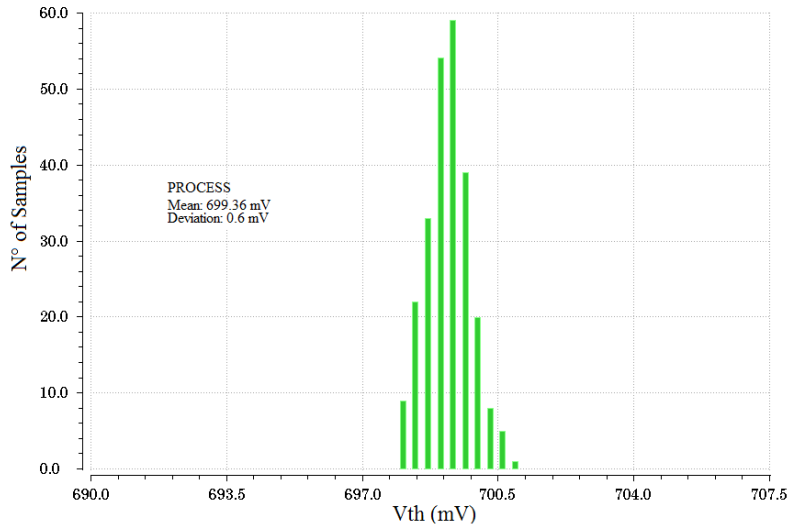
Since this circuit represents a good solution to realize the linearization, it is possible to go to the next step of the design which consists in the layout implementation.



(a) Monte Carlo simulation: Process & Mismatch



(b) Monte Carlo simulation: Mismatch



(c) Monte Carlo simulation: Process

Figure 4.31: Monte Carlo Simulations for Vth of the final solution.

The layout of the circuit must conform to a complex set of design rules, in order to ensure a lower probability of fabrication defects. A dedicated tool, called Design Rule Checker (DRC), has been used to detect any design rule violations during and after the mask layout design. The layout has been obtained following the rules contained in [29] and it is depicted in Figure 4.32.

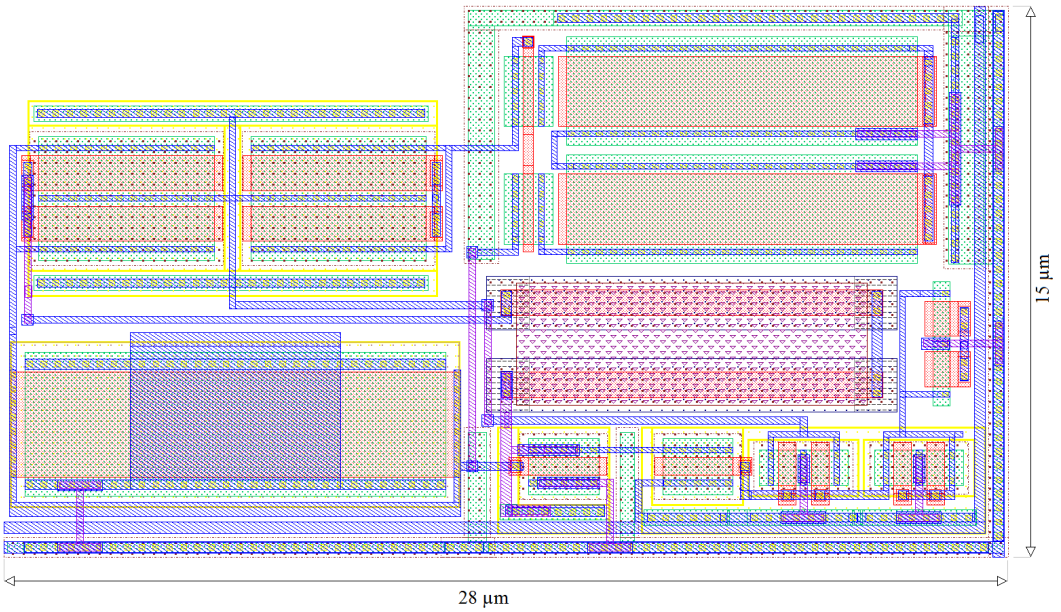


Figure 4.32: Layout implementation of the linearization circuit.

The Figure shows that the size of the final circuit is bigger than the 13 µm × 13 µm originally given. The more area available to realize the circuit comes from modifications in the DAC as will be explained in the next sections.

Using the layout it is possible to create an extracted view, which contains the parasitic resistances and capacitances to use for new simulations. In this way it is possible to observe a more realistic performance of the whole circuit and to verify if it operates as expected. These simulations are reported in the next section.

4.5 POST LAYOUT SIMULATIONS

In order to study more accurately the realized circuit, more simulations which consider some important parameters like the stability, the temperature and the effect of parasitic elements, were made. Since it is a reasonable value for the p-type polarity, the polarity foreseen for the $\overline{P}$ANDA, all these simulations use the value V_{REF} = 700 mV. The post-layout simulations are described below:

- **Comparison between the extract layout an schematic:**

  A Monte Carlo simulation which considers only the mismatch effect is performed both for the schematic and the extracted for comparison. The simulation is done observing the voltage at the output node V_{TH} The dispersion obtained with 250 runs is depicted in Figure 4.33 and 4.34.

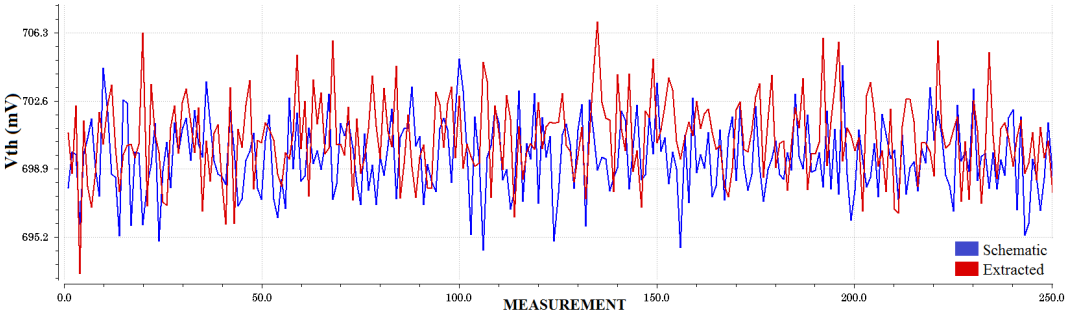


Figure 4.33: Dispersion of V_{TH} obtained using both schematic and extracted.

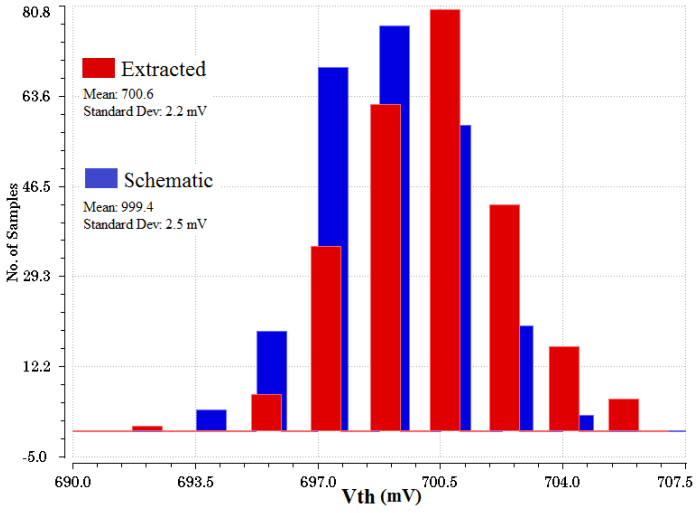


Figure 4.34: Dispersion of the voltage V_{TH} obtained with Monte Carlo simulations (only mismatch) using the schematic and the extracted.

The plots do not show relevant differences between the two cases. Therefore, it is possible to say that the parasitic capacitance does not influence the value at the output node. However, this simulation consider the parasitic resistances and capacitances that belong only to the linearization circuit and it does not consider the parasitic elements due to the neighbouring devices.

- **Temperature analysis:**

  Due to power dissipation, the circuit during its operation will work at temperatures different from 25° C. A simulation has been made in order to study the behaviour of V_{TH} for a range of temperature from 20° C to 100°C with steps of 5° C. The plot of Figure 4.35, which resumes the simulation result, shows variations of some mV in the worst case. Therefore, a little dependence from the temperature is noticed that must be considered based on the final temperature of operation of the pixel.

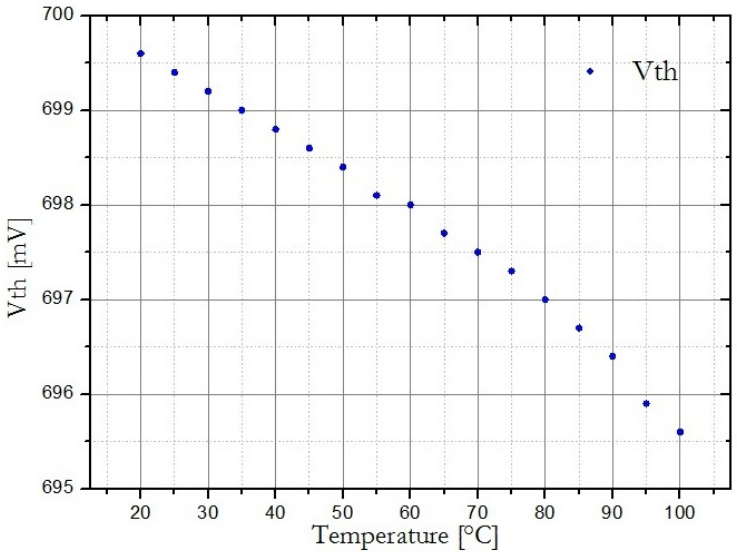


Figure 4.35: Simulation of Vth with temperatures from 20° C to 100° C.

- **Analysis of the voltage at the input node V_{REF}:**

  One of the reasons to chose the model of Figure 4.29 to implement the circuit was the fixed voltage present at the node where is connected to the DAC even changing the bit code. A simulation to verify this feature was made using the 16 levels of the DAC and it is resumed in Figure 4.36

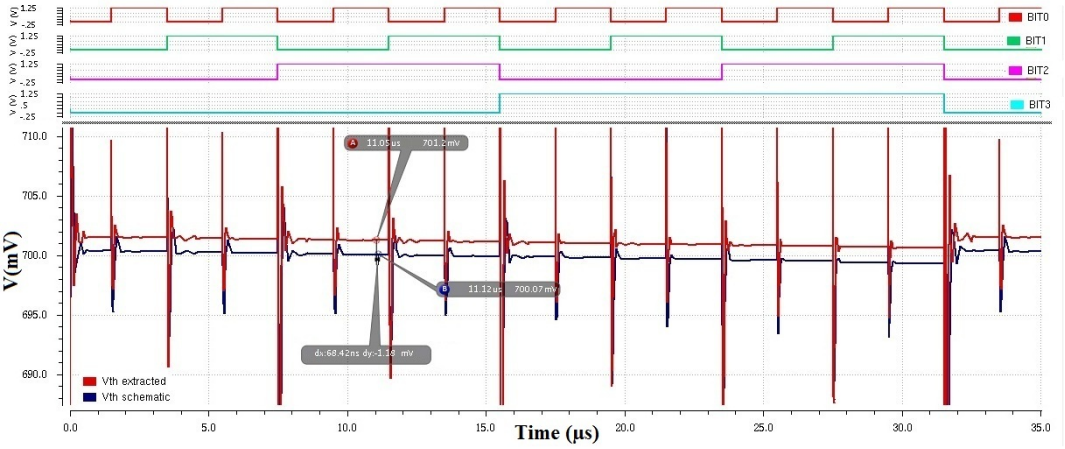


Figure 4.36: Voltage at the input node V_{REF} of the circuit.

The voltage in this node is measured sending a different code each 2 µs in order to verify the presence of any transient oscillation on the signal.

The plot shows that the signal obtained with the extracted presents an offset of ~ 1.2 mV to higher voltages respect the one obtained with the schematic. Moreover, it is observed a reduction of V_{REF}, both for schematic and extracted, of ~ 1 mV from the bit code 0 to 15. Since this variations are very small, it is reasonable to assume that they do not affect the operation of the DAC.

- **Analysis of the voltage at the output node V_{TH}:**

  This simulation aims to verify the voltage at the node V_{TH} changing the binary code of the DAC. It must be considered that the expected variation depends on the resistance R employed in the circuit (R=48 kΩ) and on the current generated by each bit of the DAC. This current is set by the external resistance connected to the bias cell of the DAC. For the simulation the value chosen for this external resistance is 1.3 MΩ and allows to obtain a current of 50 nA for each bit. Therefore, for the maximum current generated by the DAC is 750 nA and thus the maximum expected variation of V_{TH} is 36 mV.

  These values can be compared with the simulation results, which are depicted in Figure 4.37.

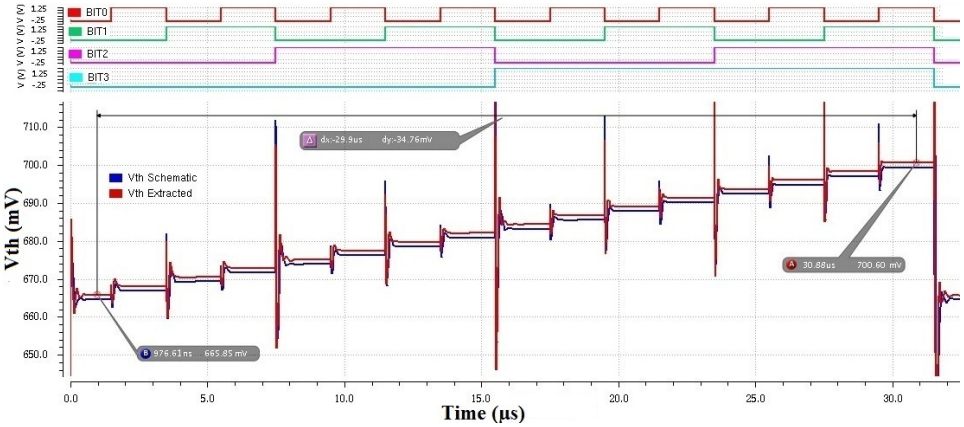


Figure 4.37: Voltage tuning with the DAC code.

The plot obtained shows oscillations for the signal for a duration of ~ 200 ns which shouldn't affect the performance of the device. The maximum variation observed for V_{TH} is of ~ 35 mV which is similar to the expected value of 36 mV. Also in this case the comparison between the simulation obtained with the extracted and with the schematic underlines a difference of ~ 1 mV.

The plot shows also the linear relation between the DAC code and V_{TH} as required from the specifications.

Moreover, it is observed that the voltage of 700 mV is not obtained with the code 0 (0000) as expected but with the code 15 (1111). This difference is caused by the modifications made in the DAC of ToPix v3 to implement this circuit. These modifications are described in the next section.

- **Dependence on the biasing:**

  The biasing of the circuit is obtained employing the line of the analogue pixel cell called "*Ibias_d*". This line, which is used to supply the comparator, leads a current of 500 nA. However, it is possible that in order to obtain a reduction of the power consumption of the comparator, this value changes.

  For this reason a dedicated simulation has made to verify the behaviour of the circuit to this possible variation using values of 250 nA, 500 nA, 750 nA and 1 µA. The simulation consists in measuring for each current the voltage V_{TH} using values of V_{REF} in a range from 300 mV to 800 mV.

  The results of this simulation are depicted in Figure 4.38 and 4.39.

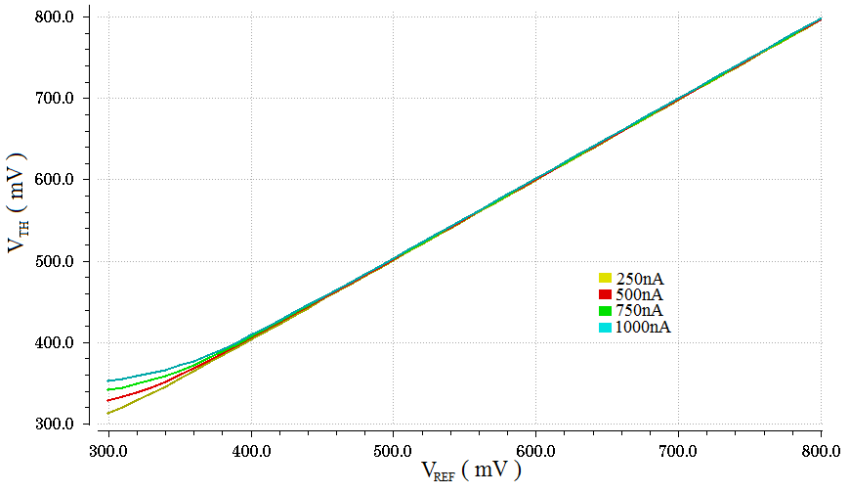


Figure 4.38: Influence of the polarization line in the V_{TH}.

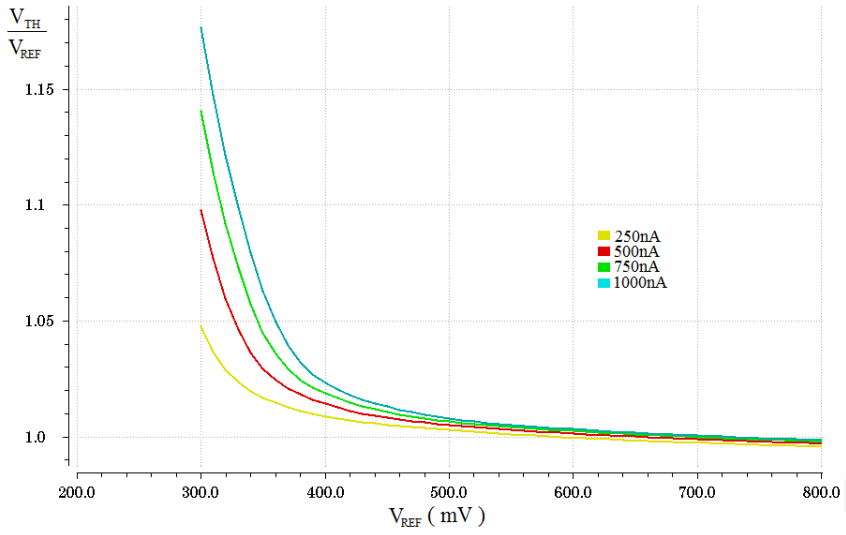


Figure 4.39: Influence of the polarization line in the gain.

The Figures show a very weak dependence by the current for values of V_{REF} higher that 400 mV, while the dependence becomes stronger for small values.

This result underlines the trade-off made during the design of the circuit in order to obtain a a good performance both with the p-type polarity, which uses V_{TH} values around 700 mV, and the n-type polarity which uses V_{TH} values arround 350 mV.

This simulation shows that, since the performance obtained with V_{REF} values arround 350 mV is acceptable, the use of a smaller current as bias might improve the performance of the circuit for the n-type polarity as well as reduce the power consumption of the circuit.

- **Stability analysis:**

  In order to verify the stability of the output voltage two other simulations with the extracted were performed.

  The first one consists in the study of the voltage at the output node when a small square signal is sent into the input node V_{REF}. The AC signal used has an amplitude of 50 mV, a period of 5 µs and is applied for 2.5 µs. Both rise time and fall time are set to 1 ns. The result, depicted in Figure 4.40, shows that the signal reaches the final value with a delay of about 200 ns. A small overshoot at the beginning of an amplitude of ~ 2.7 mV is observed. When the signal is switched off the output voltage turn back to 700 mV with a behaviour similar to that of the rising edge.

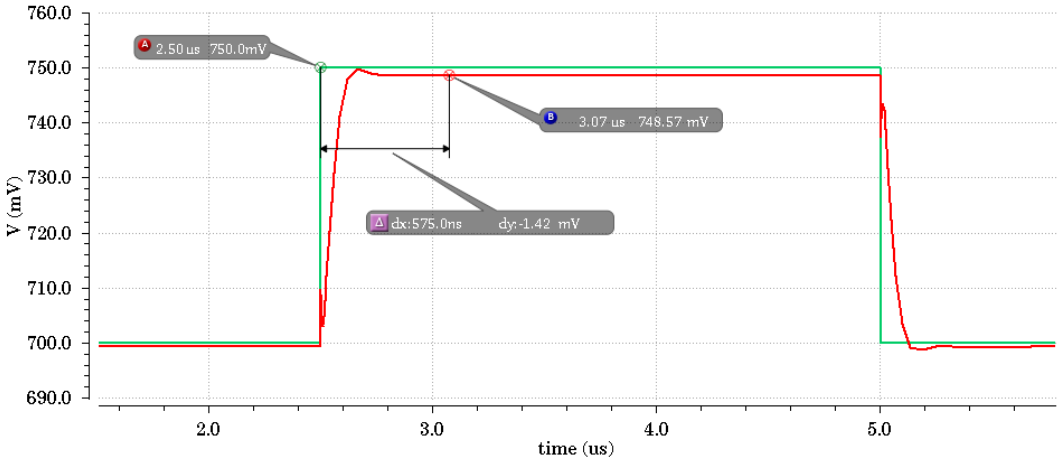


Figure 4.40: V_{TH} stability analysis.

The second simulation aims to verify the stability when the bit code of the DAC changes its value. The result obtained changing the bit code from 1 (0001) to 2 (0010) is depicted in Figure 4.41. In the Figure it is possible to observe that the overshoot has an amplitude of ~ 2.7 mV and that the signal needs ~ 200 ns to reach its the final value.

Since the delay times obtained from these simulations are limited and considering that the circuit is not used to send signals but only to define DC levels, these result are considered acceptable .

The results of these two simulations proves the stability of the signal for small variations of V_{REF} and for the variations of I_{DAC}.

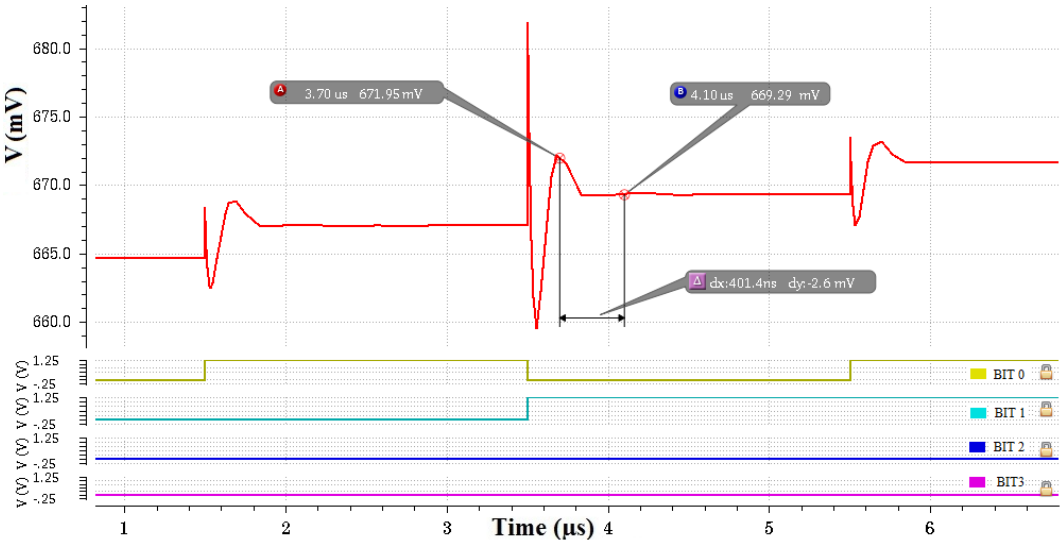


Figure 4.41: V_{TH} stability analisys.

4.6 NEW DAC FOR TOPIX VERSION 4

The DAC of ToPix v3, as explained in the previous sections, uses 4 NMOS transistors and a multiplexer to reverse the direction of the current I_{DAC}. Since the model used to realize the linearization circuit works only when the DAC sources current, these elements are not any more useful. For this reason the new version of the DAC does not contain these devices.

Moreover, in order to obtain more area to develop the circuit, it was decided not to use the four inverters employed to change the logic of the DAC. Therefore, the DAC in this configuration, generates the maximum current with the code 0 (0000).

Thanks to these modifications it is possible to obtain 15 µm × 15 µm in addition to the area initially available to develop the circuit.

In Figure 4.42 is illustrated the new layout used for the DAC in ToPix v4.

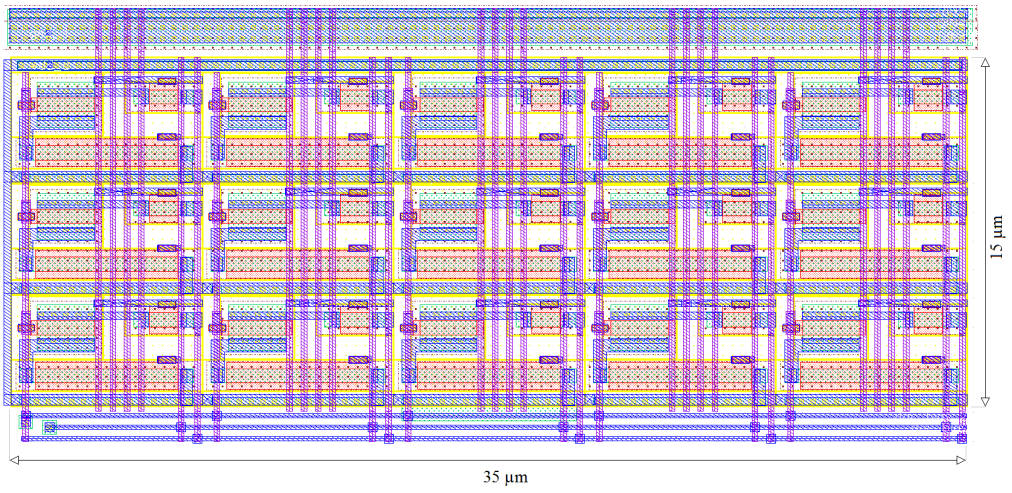


Figure 4.42: Layout of the DAC in ToPix v4.

4.7 THE VOLTAGE THRESHOLD LINEARITY IN TOPIX V4

In the previous sections the model to linearize the voltage threshold of the comparator has been explained. The final circuit has been realized in many steps, starting from an ideal device, which is the ideal DC generator, in order to verify the accuracy of the model. The next step was to find a real circuit to use as DC generator with features suitable to the requirements set by the model. Different circuits have been analyzed to find an optimal solution. The first two circuits proposed had good qualities but they didn't appear attractive as a final solution. However, since the two circuits contained good features, an hybrid solution has been analyzed and was chosen as the final solution.

Now the final step is to verify the linearization of the threshold voltage of the comparator using the real devices until now developed. In order to obtain a more realistic result, the circuit is analyzed using the extracted layout of the whole analogue pixel cell.

The Figures 4.43 and 4.44 show a block representation and the layout of the whole analogue pixel cell used for the simulation.

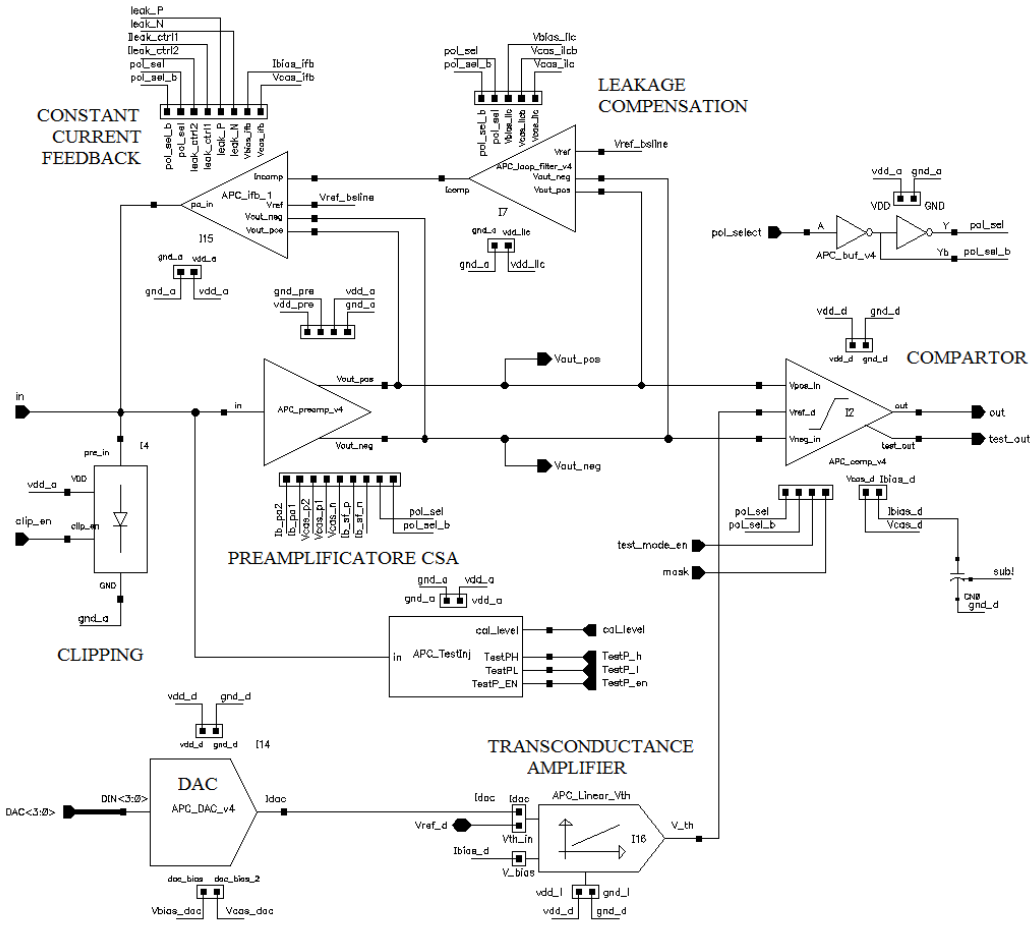


Figure 4.43: Block representation of ToPix v4.

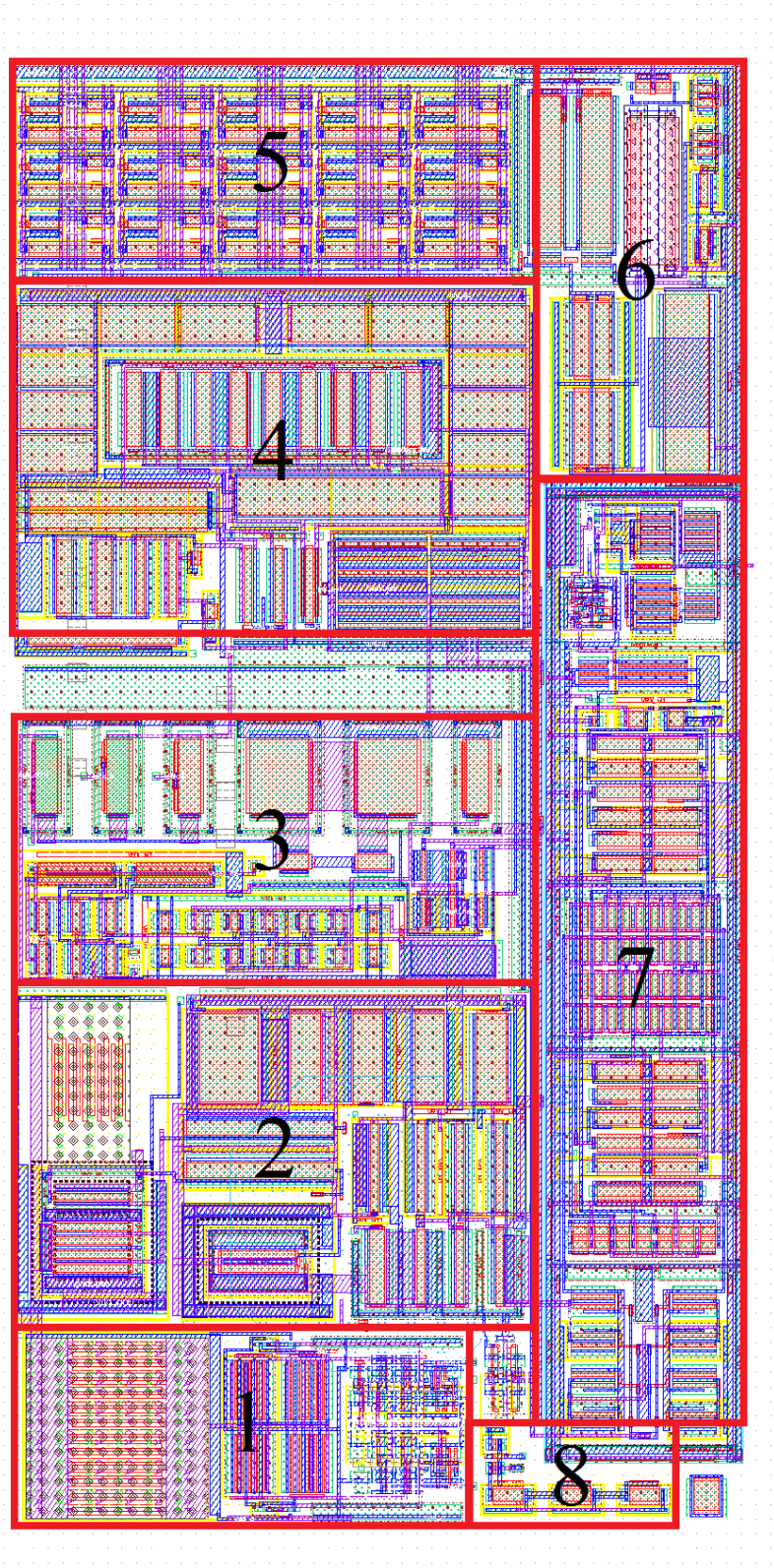


Figure 4.44: Analog pixel cell of ToPix v4: 1- Calibration circuit, 2- Charge Sensitive Amplifier, 3- Constant current feedback, 4- Leakage compensation, 5- DAC, 6- Linearization circuit, 7- Comparator, 8- Clipping.

The output voltage of the linearization circuit is analyzed injecting at the input node of the charge sensitive amplifier a delta shaped current pulse of amplitude 500 nA. This signal simulates a particle which impinges on the sensor.

The Figure 4.45 shows the signals V_{TH}, V_{REF} and the output of the CSA.

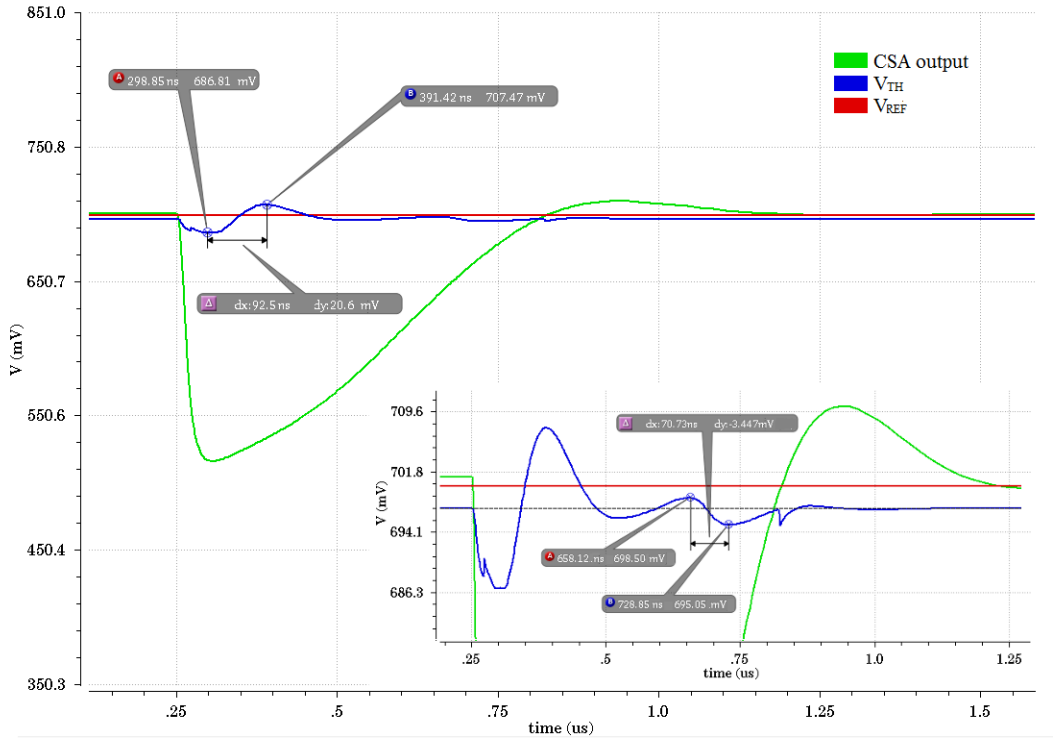


Figure 4.45: Hit particle simulation.

The Figure shows that at 0.25 µs, when V_{TH} and the output of the CSA have the same value, V_{TH} starts to oscillate. The oscillations are motivated by the use of the same line used by the comparator. In fact, the instant when the oscillations begins, corresponds to a commutation of the comparator. Is reasonable to assume that in this moment the signal of the bias changes, creating the oscillation illustrated in Figure.

The maximum oscillation observed has an amplitude of ~ 20 mV and has a duration of ~ 250 ns while the second oscillation has a much smaller amplitude of about 0.5 mV.

Since this oscillation starts after the commutation of the comparator and finishes before the second commutation, it should't influence the performance of the analogue pixel cell. Moreover, in order to reduce the amplitude of these oscillations an additional capacitance has been connected between *Ibias_d* and ground.

The final step of this work consists in verifying the relation between the trip voltage and the DAC code. The simulation has been performed using a voltage V_{TH}=700 mV and with a variation of the voltage reference V_{TH} from 0 to 1.2 V for the 16 levels of the DAC. Both polarities have been studied and the results obtained are illustrated in Figures 4.46 and 4.47.

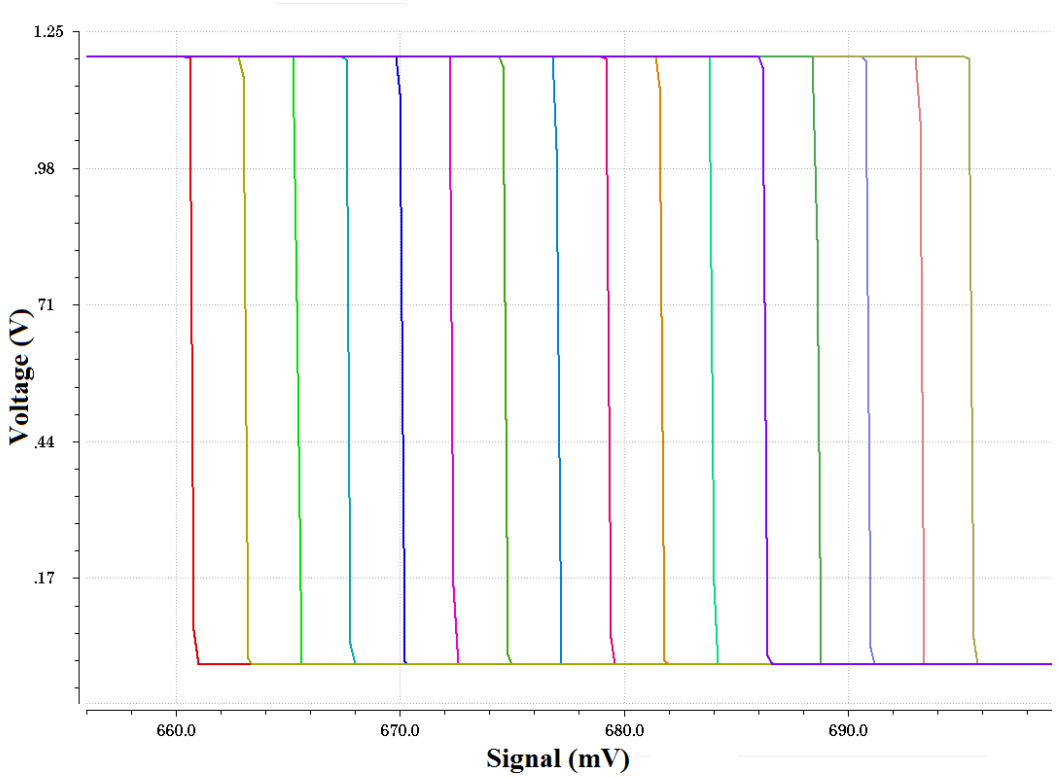


Figure 4.46: Comparator output for the 16 levels of the DAC for p-type polarity.

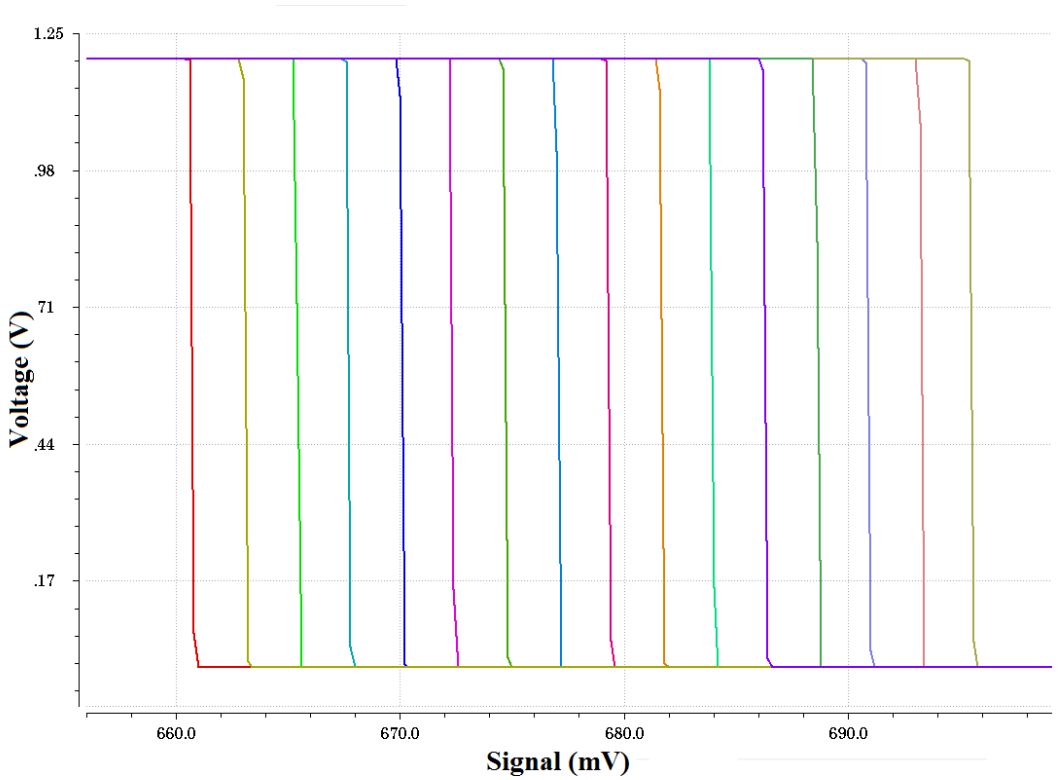


Figure 4.47: Comparator output for the 16 levels of the DAC for n-type polarity.

The plots are similar to the ones previously obtained using the ideal DC generator. For all the bits of the DAC the comparator works correctly. In order to verify the linear relation between the voltage threshold of the comparator and the DAC code, as done previously, it is possible to calculate the trip point for each V_{TH}.

The trip points obtained for both polarities are summarized in Table 4.11 and show that the LSB of 50 nA in current corresponds to 2.3 mV in voltage for both polarities. This value, which should allow a fine tuning, is fixed only by the external bias cell and therefore, it is possible to modify the LSB of the correction system.

The plot of Figure 4.48 shows that the relation between the two variables is linear. In order to estimate the linearity, the linear correlation coefficient ρ is calculated using the Formula (4.3) and the value obtained is 0.99 for both polarities. Therefore, it is reasonable say that the circuit realized allow to obtain the linear relation between the voltage threshold and the DAC code.

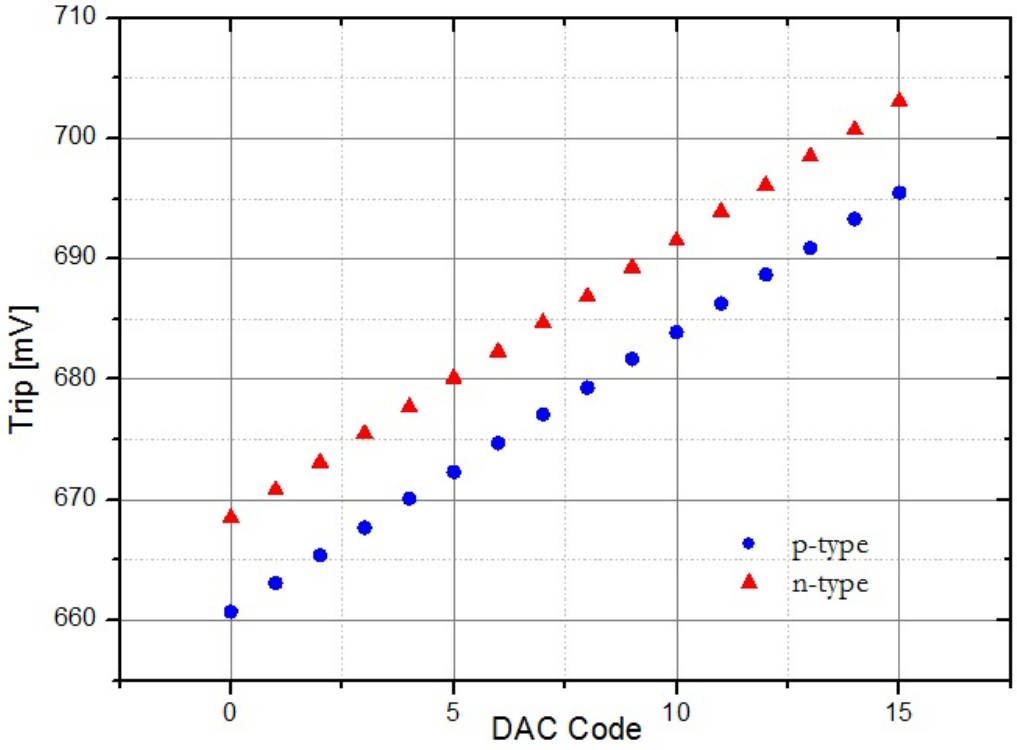


Figure 4.48: Trip points obtained with the DAC code variations with both polarities.

Trip Point		
Bijnary code	**Trip Point with p-type [mV]**	**Trip Point with n-type [mV]**
0000	660,7	668,5
0001	663,1	670,8
0010	665,4	673,1
0011	667,7	675,5
0100	670,1	677,7
0101	672,3	680,1
0110	674,7	682,3
0111	677,1	684,7
1000	679,3	686,9
1001	681,7	689,3
1010	683,9	691,5
1011	686,3	693,9
1100	688,7	696,1
1101	690,9	698,5
1110	693,3	700,7
1111	695,5	703,1

Table 4.11: Simulation results of the trip point for the two polarities.

4.7.1 *Simulation of the tuning system in ToPiX v4*

The tuning system of ToPix v4 uses the linearization circuit developed in the previous sections to simplify the operation of tuning.

Using Monte Carlo simulations it is possible to simulate the correction of the voltage threshold in order to verify the simple way to make the correction.

For example if for all the channels it is required a voltage threshold for the comparator of 680 mV, the voltage reference V_{REF} must be set to a higher value in order to correct all the pixels. Considering 150 pixels, for each of them the DAC code must be set to 1111 while the V_{REF} could the set to 700 mV. The dispersion due to mismatch effects is obtained from Monte Carlo simulations and it is the one depicted in Figure 4.49.

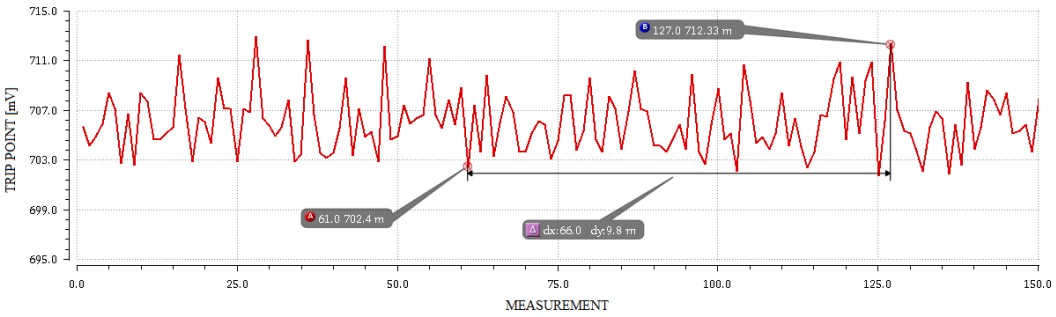


Figure 4.49: Dispersion of the trip point obtained with a Monte Carlo simulation using V_{REF}= 700 mV.

The dispersion helps to find the two extreme cases which are the pixel 61 and 127. In this cases the trip points have values of 702.4 mV and 712 mV and therefore to reach the desired trip point are necessary variations of 22.4 mV and 32 mV for the pixel 61 and 127, respectively. The Table 4.12, which contains the binary codes to use for the corrections, shows that the values to use for the corrections are 0110 and 0001 for the pixel 61 and 127, respectively.

Binary code	**ΔV [mV]**	**Binary code**	**ΔV [mV]**
0000	34.5	1000	15.1
0001	32.2	1001	13.8
0010	30.	1010	11.5
0011	28.6	1011	9.2
0100	25.3	1100	6.9
0101	23.0	1101	4.6
0110	20.7	1110	2.3
0111	18.4	1111	0

Table 4.12: BIT codes to use to tune of ΔV for an external polarization of 1.3 MΩ.

5

A POSSIBLE NEW TECHNOLOGY FOR THE HYBRID PIXEL FRONT-END CHIP

The discriminator is one of the main blocks which composes the front-end of each hybrid pixel sensor. This device, located at the end of the analogue part, converts the analog information generated by a particle hit in a digital signal, which is then sent to the digital circuit of the pixel. This digital signal contains the energy loss by the particle in the sensor cell and allows, after being analized by the digital pixel cell, to obtain the hit position and the hit time stamp.

In this Chapter, a general introduction about discriminators in the field of radiation detectors is given in order to understand the requirements which the comparator of ToPix must achieve to work properly. The description of the main parts, as well as the operation of the device is described in order to understand how the useful information is extracted from the analog output of the CSA. During the discussion, the main characteristic parameters as the gain and the delay time, are introduced in order to calculate them during the simulation.

The comparator of ToPix v3 is then described at transistor level and tested with the simulator tool. The simulations aim to evaluate some important parameters of the comparator developed with the CMOS 0.13 μm technology, which is the current technology of the ASIC. These parameters are then analized at the end of the chapter. For each test it is described the operation in which the simulation is done and the results are reported with the use of tables to underline the more important results.

The second part of the Chapter contains the same tests done with the comparator of ToPix v3, but they are done using a new sub-micron technology in CMOS 0.11 μm. This new technology has similar features to the CMOS 0.13 μm technology but allows also to obtain a substantially reduction of the production cost. The second comparator is analyzed in three different configurations. At the end of the Chapter all the parameters obtained from both technologies are summarized and discussed.

5.1 LOW POWER COMPARATORS

Comparators, in the field of radiation detectors, are often called discriminators due to their function of separating the useful information from the unwanted background. The discriminator plays a fundamental role in the front-end because it allows to extract the information contained in the analogue signal which comes from the CSA, whenever a particle impinges on the sensor.

These devices have been developed for many analogue systems and therefore, an optimal performance with high accuracy and fast response are feasible features, easy to implement in particular with the use of positive feedback circuits driven by a clock. However, the use of a clock would require a sampling of the analogue signal generated by the CSA at high speed, increasing in this way the power consumption. Moreover, this requires high speed digital control lines in close proximity of the sensitive area of the analogue part. For all these reasons the asynchronous topology is preferred.

A comparator basically consists of a high gain differential amplifier, followed by a block of CMOS inverters, as depicted in Figure 5.1.

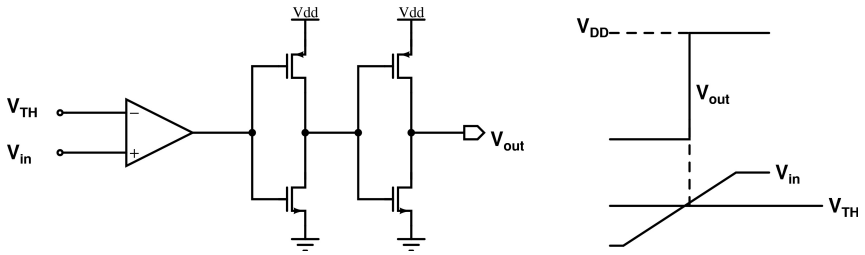


Figure 5.1: Basic structure of a comparator.

The differential amplifier is used in an open-loop configuration and receives the signals to be compared. Usually one of these two signals is fixed and used as a reference, while the other one is the signal which contains the information to analyze.

Concerning the two inverters employed, they plays a double role: they ensure a well defined logic signal at the output of the comparator and they are also used as buffer to drive the output load. The structure illustrated in Figure 5.1 contains only a couple of inverters, each realized with two CMOS transistors, but in general, the number of inverters depends on the load to drive. Anyway, the use of more stages of inverters increases the power consumption of the device, therefore, when it is possible, their number is reduced.

Ideally, the discriminator has two possible outputs which correspond to the voltage supply (1 logic) and to the ground (0 logic) and switches instantaneously. These conditions require to have an infinite gain and bandwidth, which is not possible in real circuits. Therefore, each real comparator is characterized by real features such as the gain of the differential amplifier, the minimum value to make the comparator flip and the propagation delay [27].

In the next section the comparator used in ToPix v3 is studied in order to obtain the value of these characteristic parameters. The same will be done with a comparator developed with the new technology for comparison.

5.2 THE COMPARATOR OF TOPIX VERSION 3

The comparator used in ToPix v3 is described and analyzed in this section. The goal is to find the main parameters of the device in order to quantify its performance. The section starts with a detailed description at transistor level of the comparator, where all its parts are analyzed. Several simulations were done and for each of them, the description of the simulation and the results are given.

The same analysis will be then proposed at the end of the chapter in the new technology for comparison purposes.

5.2.1 *The transistor level implementation*

The comparator used in the front-end of ToPix v3 consists in a folded cascode input stage with two CMOS inverters in series. The folded cascode is used in order to alleviate the limited output swing due to the low supply voltage set to 1.2 V for the technology employed. In fact, the folded structure does not stack the cascode transistor on the top of the input device allowing in this way to increment the output swing.

Figure 5.2 shows the transistor implementation of the comparator already discussed in Chapter 4.

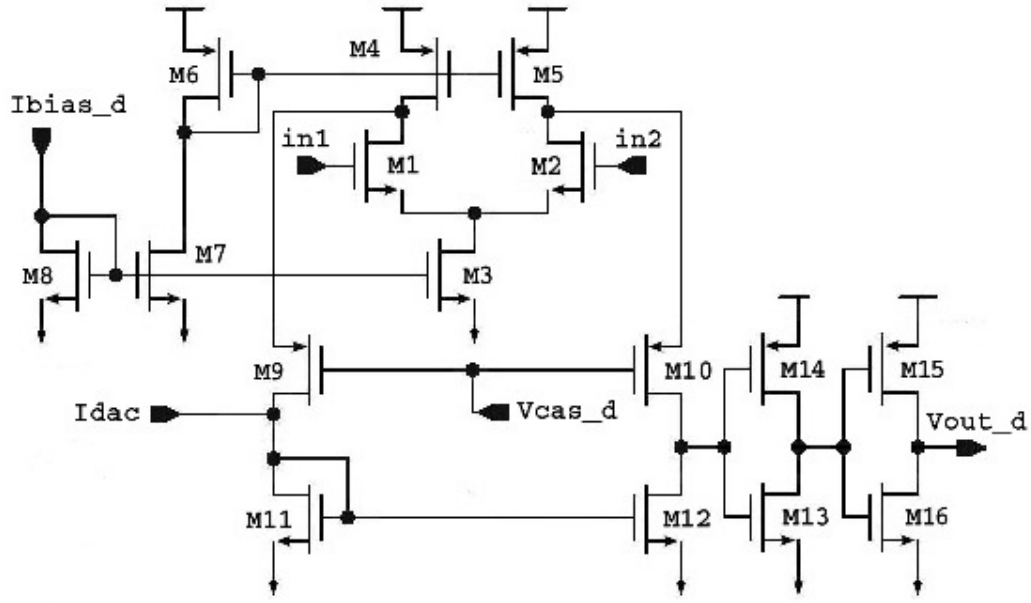


Figure 5.2: Transistor level implementation of the comparator of ToPix v3

The two input transistors are M1 and M2 and they are designed with a large size (W/L= 25 µm / 0.5 µm) in order to reduce the mismatch effect. Transistors M6 and M8 use a diode connection to create current mirrors together to transistors M3, M4, M5 and M7. The folded cascode is implemented by transistors M9 and M10, while transistors M11 and M12 provide the current to the cascode devices.

The inverters are implemented with the couples of complementary CMOS transistors M13, M14 and M15, M16 which are designed to obtain an output transition when the input voltage cross the value of 0.6 V. These logic gates are used as driver allowing fast transitions between the two logic states. The output of the last inverter is the digital output of the comparator (V_{out_d}) which is directly connected to the digital circuitry of the pixel.

Using the transistor implementation illustrated in Figure 5.2, the non-inverting input of the comparator is in1, while in2 corresponds to the inverting one. Therefore, the comparator gives the high level output when the condition Vin1 > Vin2 is satisfied.

In addition to the transistor level implementation just described, since the comparator has to be able to work with two polarities to cope with the ASIC requirements discussed in Chapter 3, a block which exchanges the two inputs is necessary. The block and the transistor implementation used to change the logic are depicted in Figure 5.3.

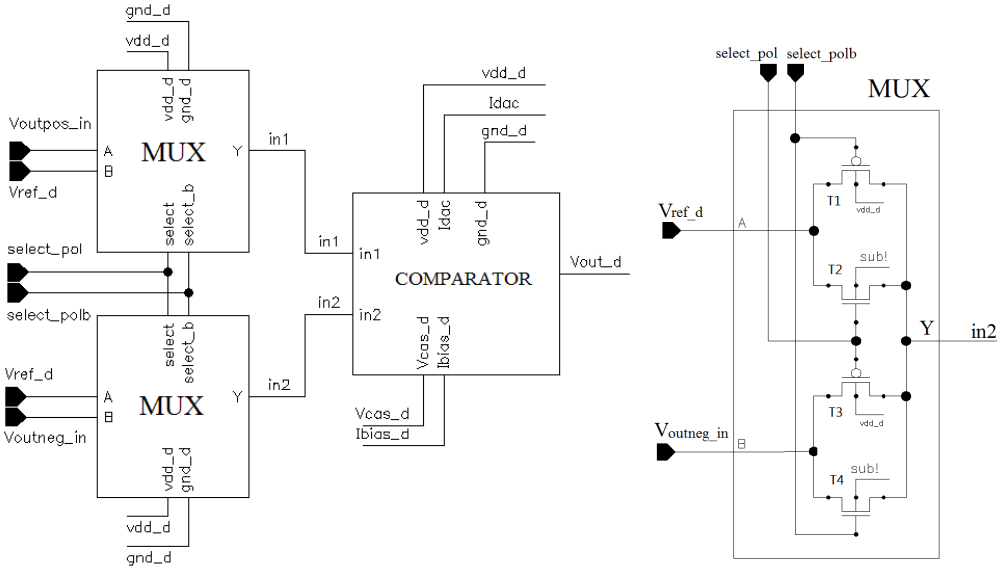


Figure 5.3: Left: Block implementation of the input selection system. Right: Transistor implementation of a multiplexer.

The Figure shows that for each comparator input it is foreseen a multiplexer which select the signal to be sent to the output.

In each multiplexer the inputs are controlled by the signal *select_pol*, which assumes the value 1.2 V and 0 V for the p-type and the n-type polarity, respectively.

Figure 5.3 shows also the transistor implementation of a multiplexer used for the polarity exchange. Since *select_polb* is obtained from the signal *select_pol*, the multiplexer is driven by one external signal as follows: when *select_pol* assumes the value of 1.2 V the transistors T1 and T2 are switched off, while T3 and T4 are switched on sending the input line B to the output. In the same way if *select_pol* assumes the value 0 V, the output of the device will be the signal A.

Table 5.1 resumes the inputs used with the two polarities.

COMPARATOR INPUTS			
Select_pol	**Polarity**	**IN1**	**IN2**
0	n-type	V_{OUT}	V_{REF}
1	p-type	V_{REF}	V_{OUT}

Table 5.1: Possible inputs of the comparator

In order to simplify the test operation, the comparator contains also a block which allows to send its output to a dedicated test pad. This block, depicted in Figure 5.4, is composed by a multiplexer and by a second stage which is driven by the signal *test_mode_en*. More details about this circuit test are given in the Technical Design Report of $\overline{\text{P}}$ANDA [2].

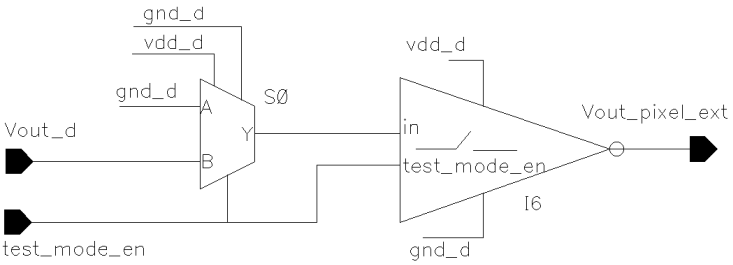


Figure 5.4: Block implementation of the test circuit.

Although the transistor level implementation of the whole comparator is the same employed in the third version of ToPix, the layout of this component has been modified in order to fit in a smaller area. Thanks to this modification has been possible obtain the free area necessary to develop the linearization circuit discussed in the previous Chapter.

The layout of the comparator, depicted in Figure 5.5, appears fairly compact and fits in an area of 14 µm × 67 µm.

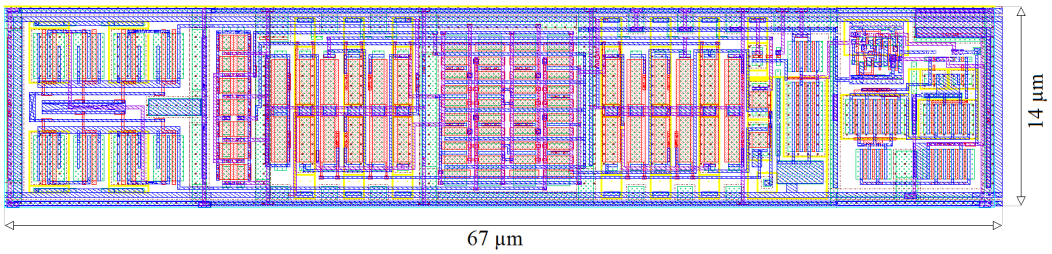


Figure 5.5: Comparator layout.

5.2.2 *Simulation results*

The comparator behaviour is tested using the simulator which allows to study the performance of the device with different analysis, as measurements of delay time, gain and trip point. Some of them are also proposed in the next section where the comparator realized with the new technology is studied.

For all simulations the comparator uses the p-type polarity and therefore the signal *select_pol* is set to 1.2 V, so that the voltage reference V_{REF} is sent to the non-inverting node of the comparator. All the inputs of the device and their values for these simulations are shown in Figure 5.6.

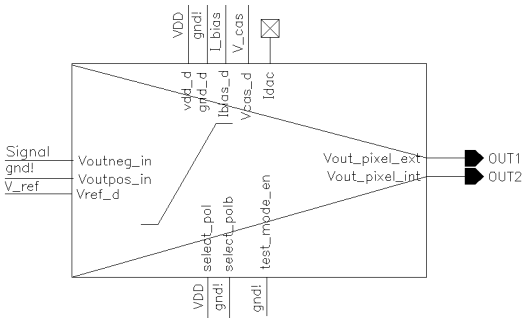


Figure 5.6: The comparator block with the inputs used during simulations.

The studies made on the comparator are described below.

- **Trip voltage analysis**

  The first tests aims to study the comparator output when the signal applied to the inverting input overcome the voltage reference V_{TH}.

  In order to study the behaviour of the comparator in this situation, a DC sweep of the signal input is done in the range from 650 mV to 750 mV. The voltage reference V_{REF} is set to the value 700 mV and the voltage trends at the input node of the inverter block and at the output of the comparator are analyzed. The output obtained from this simulation is depicted in Figure 5.7.

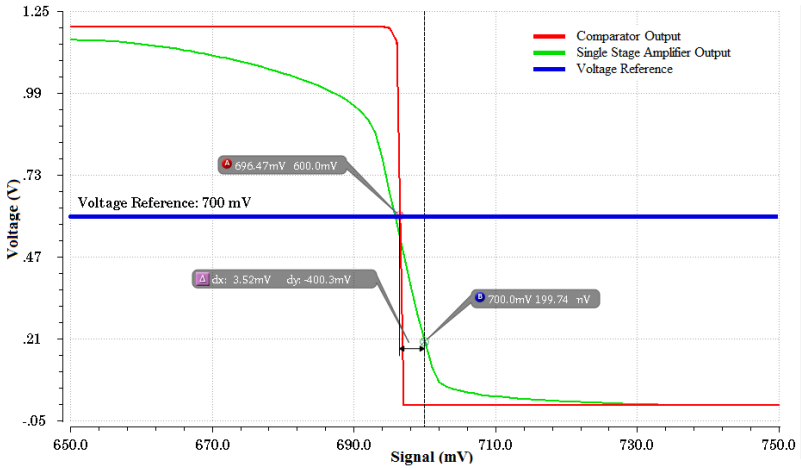


Figure 5.7: Trip point analysis in CMOS 0.13 µm technology.

The Figure shows that the comparator output flips when the input of the block of inverters reaches the value of 600 mV, as expected. Therefore, it is possible to say that the block of inverters does not create any offset in the signal.

The image shows also that the comparator switches before the signal reaches the value of the voltage reference. This offset, which is estimated to be ~3.5 mV, might be caused by the non perfect symmetry of the circuit used to implement the comparator.

In order to obtain a more realistic result, the same test is done using the extracted layout. As shown in Figure 5.8, also in this case is observed an offset but its value is ~ 6 mV, which is higher than the previous case.

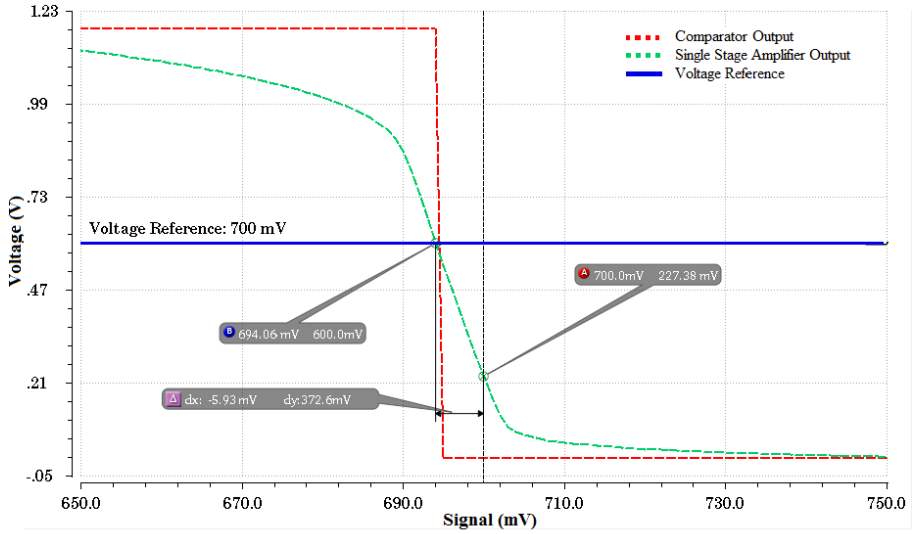


Figure 5.8: Trip point analysis in CMOS 0.13 µm technology with the extracted layout.

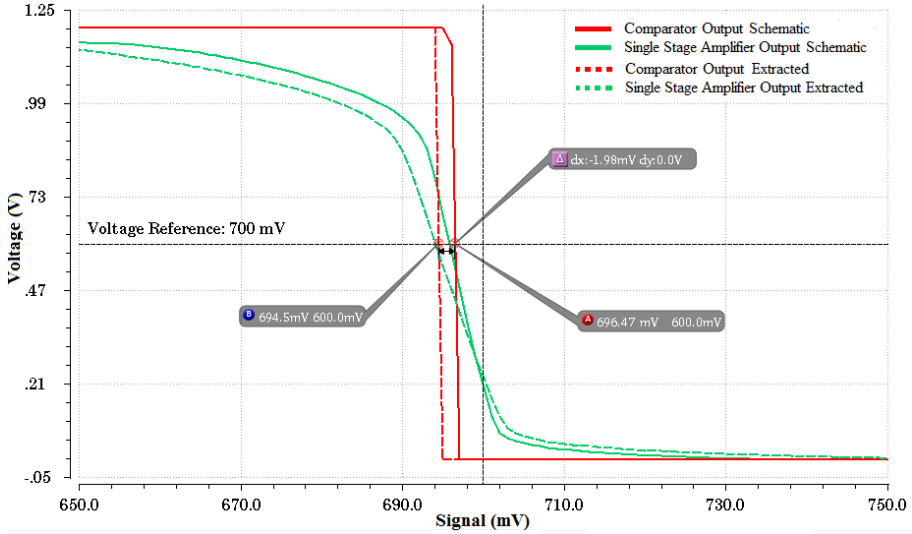
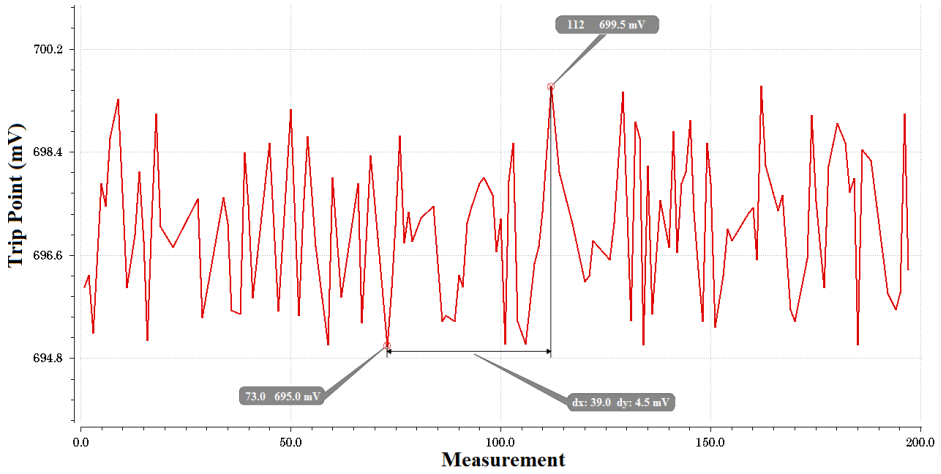


Figure 5.9: Comparison between the schematic and the extracted simulations.

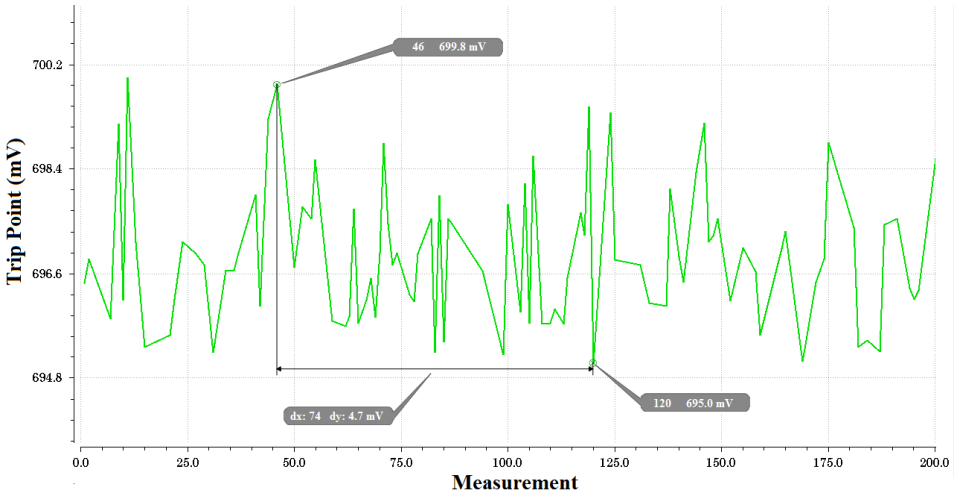
The Figure 5.9, which allows to compare the two results, shows that the parasitic capacitances and resistances increase of ~ 2 mV the offset observed in simulations using only the schematic.

To study also the dispersion of the trip point due to the mismatch effects, a Monte Carlo analysis with 150 runs is done, both for schematic and extracted.

All the results obtained are depicted in Figures 5.11 and 5.10.



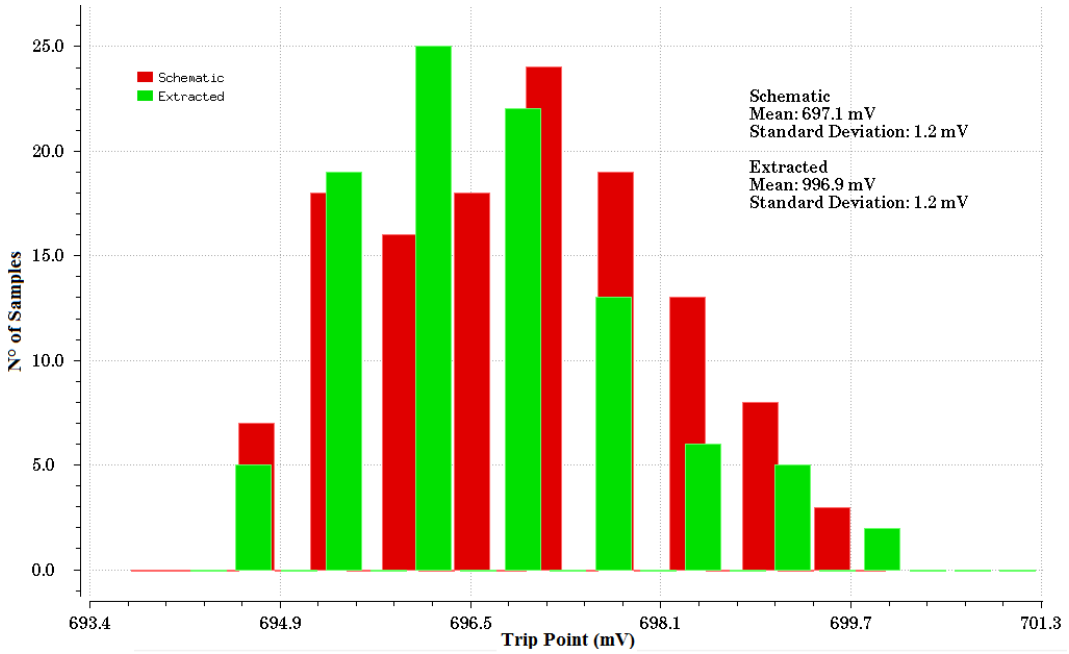
(a) Trip point distribution with schematic.



(b) Trip point distribution with extracted.

Figure 5.10: Trip point measurement in Monte Carlo simulation with schematic (red) and with the extracted layout (green)

For the simulation which uses the schematic, the trip values measured are included between 695 mV and 699.5 mV and thus, the peak to peak dispersion is of ~ 4.5 mV. Using the extracted the dispersion appears to be the same but it is shifted to lower voltage values. The mean voltages obtained from the simulation in fact, are 697.1 mV and 996.9 mV for the schematic and extracted, respectively.



(a) Histogram of the trip distribution.

Figure 5.11: Trip point measurement in Monte Carlo simulation with schematic (red) and with the extracted layout (green)

- **Gain analysis**

  The other important parameter which characterizes the comparator is the gain. This parameter, due to the implementation of the comparator, depends on the voltage applied at the gate of the cascode transistors M9 and M10. The value used to maximize the gain during the simulations is 465 mV and the gain estimated is 70, as illustrated in the Bode diagram of Figure 5.12. The Figure shows also that the gain is constant until 1Mhz where the drop frequency roll-off begins.

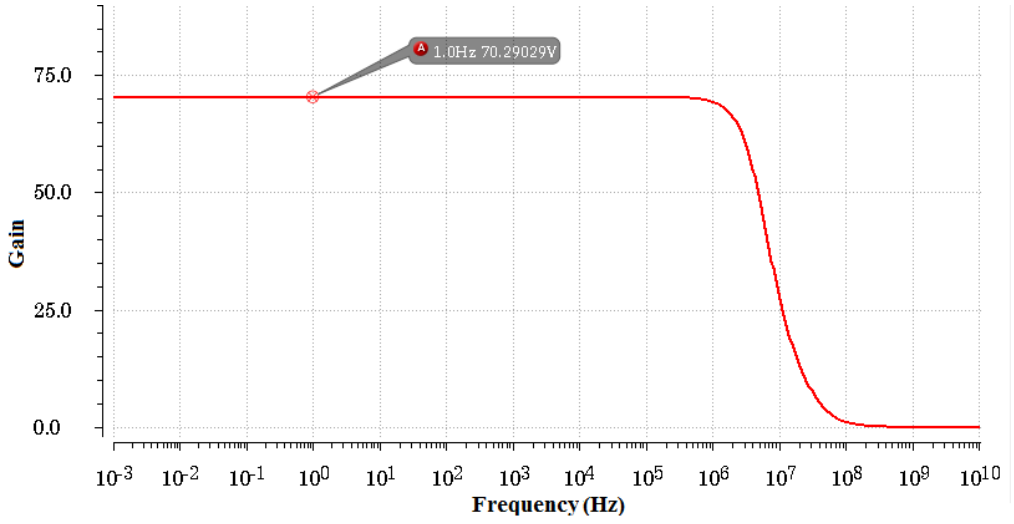


Figure 5.12: Bode diagram

- **Delay time analysis**

  To analyze the performance of the comparator the delay time of the signals is an important parameter to consider. The delay time can be defined as the time need by the comparator to generate the output from the instant when the variable inputs reach the value of the voltage reference. This time depends on the way used by the variable signal to overcome the voltage reference: if the signal overcomes the threshold reference slightly, the comparator switches with a delay time bigger than in the case where the signal overcomes the threshold reference abundantly. Moreover, it is reasonable to think that, since each transistor has its own characteristic delay, the delay time of the comparator depends also on the topology of devices employed to realize the circuit and hence, also on the technology used.

  A dedicated simulation is done to estimate the delay time of the comparator used in ToPix v3. The simulation consists in observing the behaviour of the comparator output applying at the inputs a voltage reference of 700 mV and a DC voltage of 690 mV in order to not to generate the switching of the comparator. During the simulations, the switching is simulated with the use of a step voltage of variable amplitude for each measure, to apply in addition to the DC voltage.

  In Figure 5.13 it is shown an example of simulation where it is possible to observe the propagation delay. Observing the transient of the signals it is possible to notice that, in spite of the signal overcome the voltage reference at the time 20.5 ns, the comparator switches with a delay of ~ 12 ns.

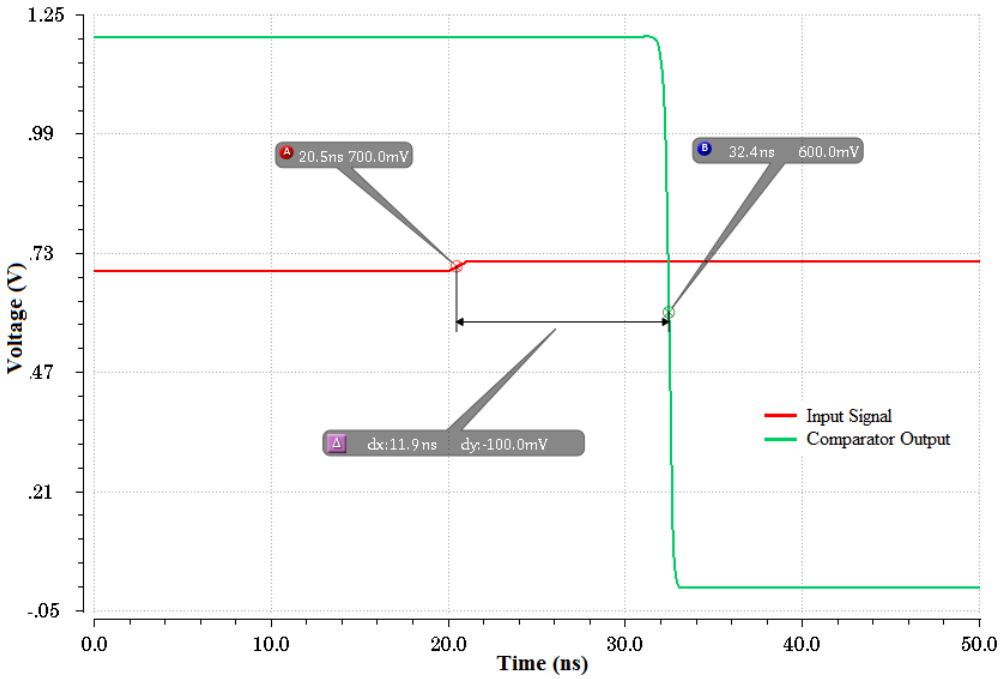


Figure 5.13: Example of delay time simulation with a step voltage of 20 mV.

During the simulation for each configuration the step amplitude varies from 20 mV to 120 mV with a step of 5 mV and the outputs observed are depicted

in Figure 5.14. The Figure shows that, in spite of the step used to change the amplitude of the signal is always the same, the delay time follows a non-linear trend.

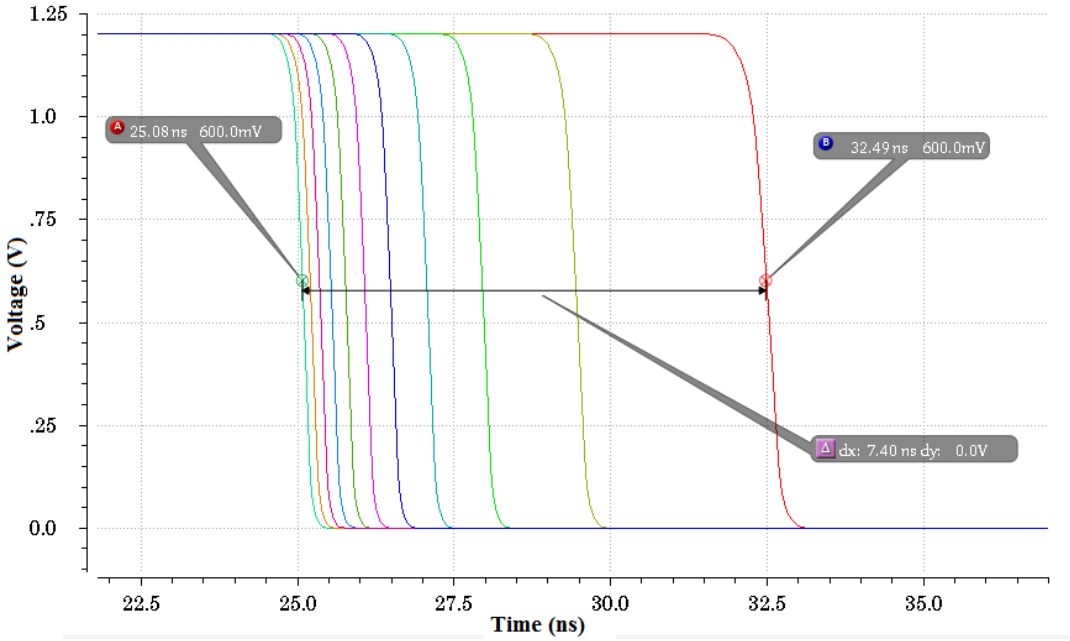


Figure 5.14: Example of delay time simulation with a step shape voltage from 20 mV to 120 mV with steps of 5 mV.

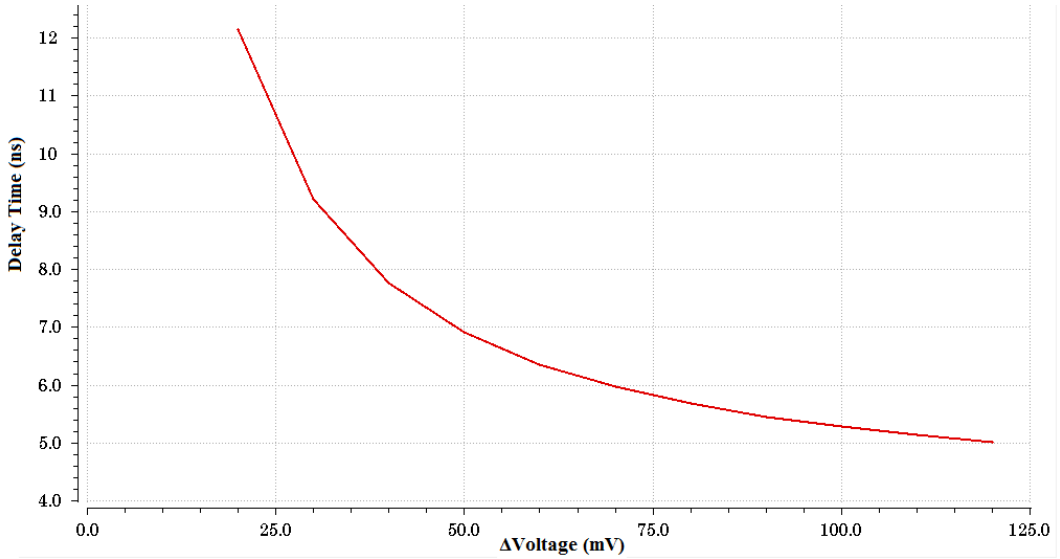


Figure 5.15: Propagation delay.

The relation between the delay time and the amplitude of the step used to overcome the voltage reference is depicted in Figure 5.15. The plot obtained shows clearly that the trend is non-linear and that for amplitudes higher than 100 mV the delay time flattens at about 5 ns.

- **Temperature analysis**

  Since the device during its function dissipate power, the temperature changes. Therefore, is useful to know the behaviour of the output voltage with temperature variations.

  The temperature test is done measuring the output voltage of the comparator and the relative trip point with temperatures from 20 °C to 100 °C. The test results are depicted in Figures 5.16 and 5.17

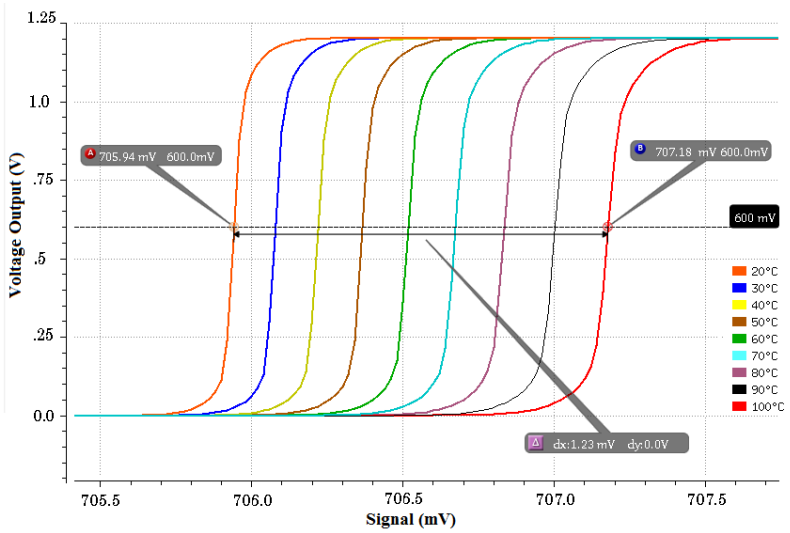


Figure 5.16: Output voltage with variations of temperature from 20 °C to 100 °C.

The results show that the trip point increase of ~1mV when the temperature is 100 ° C.

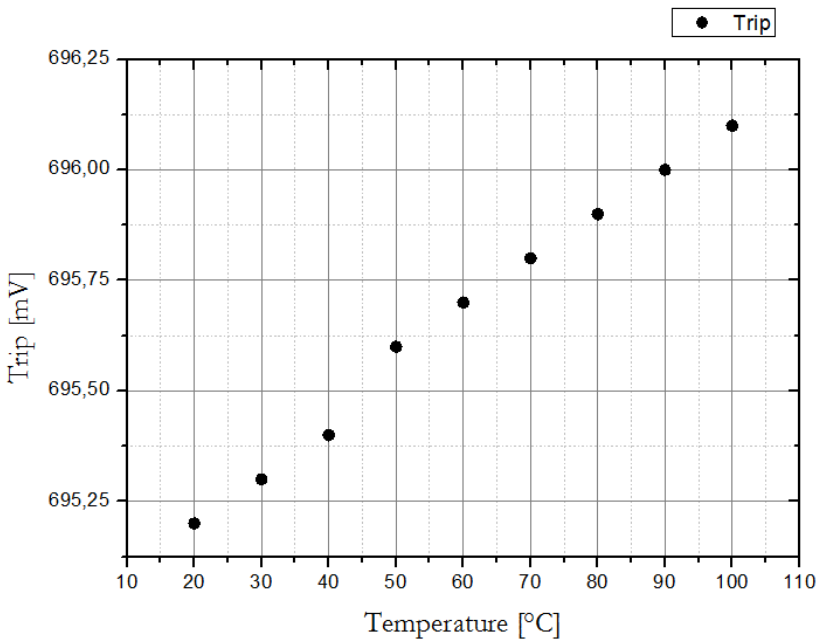


Figure 5.17: Trip voltage with variations of temperature from 20 °C to 100 °C.

TRIP VARIATION WITH TEMPERATURE	
Temperature [°C]	**Trip Point [mV]**
20	695.2
30	695.3
40	695.4
50	695.6
60	695.7
70	695.8
80	695.9
90	696.0
100	696.1

Table 5.2: Trip voltage with variations of temperature from 20 °C to 100 °C.

5.3 THE COMPARATOR WITH A NEW SUB-MICRON TECHNOLOGY

This section is dedicated to test the comparator using the CMOS 0.11 μm technology. The technology porting foresees the use of the same schematic used in ToPix v3 but with the possibility, where it is necessary, to modify the circuit design to improve the performance of the device. Some modifications in the circuit are expected since the transistors of the new technology could have a different threshold voltage.

This new technology, as well as for all the sub-micron technologies, provides the required integration density, allows a very low power consumption and should have a good radiation hardness. This feature comes from the thickness reduction of both gate and isolation dielectric layers [16].

The CMOS 0.11 μm technology, therefore, should have similar features to the CMOS 0.13 μm used to develop the ASIC of ToPix. However, the cost with the solution proposed is much lower and thus it is more attractive.

Hence, specific tests are necessary to evaluate the performance of the blocks which form the front-end using the available devices which the technology offers.

In this section the comparator develop in CMOS 0.11 μm technology, called technology B in this thesis, is analyzed using the following three different configurations:

- Standard transistors: This configuration uses for all the transistors of the circuit the standard transistors proposed by the technology B.
- Standard and High Speed transistors: This mixed configuration is based on use the high speed transistors available in the technology B. Since it is expected a critical influence by the input and output transistors on the delay, the high speed devices are used for the transistors M1, M2, M11, M12, M13, M14, M15 and M16 of Fig 5.2.
- High Speed transistors: This solution uses for all the comparator, high speed transistors.

For each configuration simulations are done to estimate the trip point, the gain and the delay time. The simulations and the results obtained are described below.

5.3.1 *Trip voltage Analysis*

A specific analysis is done in this section to compare the value of the trip voltage with the different configurations described previously. As done for the first technology studied, the simulations consist in measuring the voltage at the comparator output and extract the voltage value applied at the input node, when the comparator output reach 600 mV.

The simulations are done using the signal *select_range=1* in order to select the p-type polarity and the voltage reference V_{TH} is set to 700 mV. The plots reported contain both the output of the comparator and of the single stage amplifier to make possible analyzing any offset between the inverters stage.

The simulations done with three configurations of the technology B are described below:

- **Configuration with standard transistors**

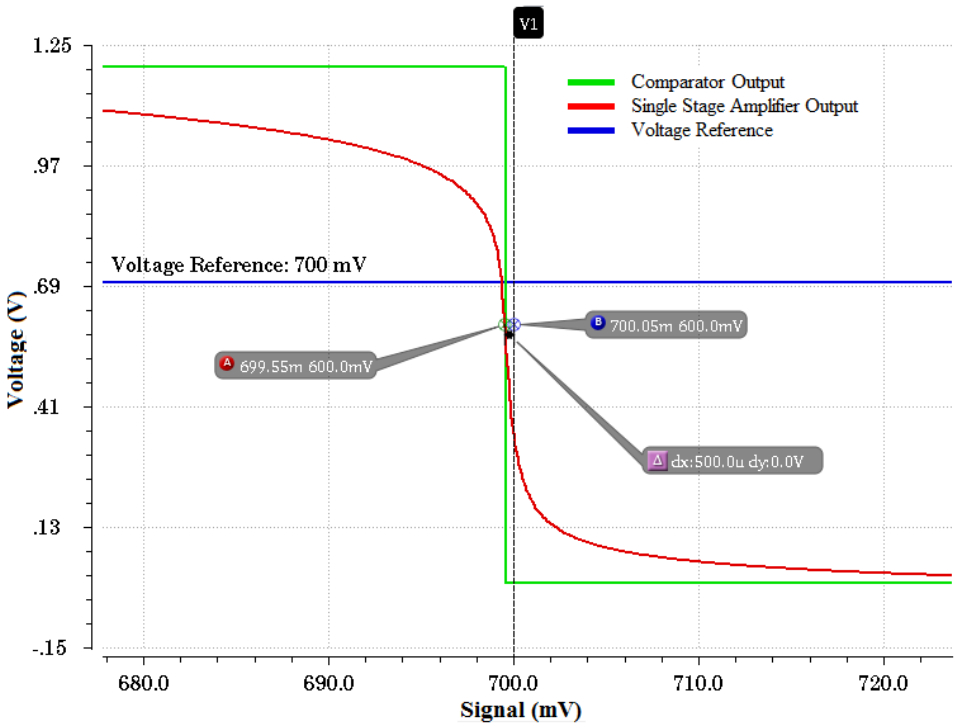
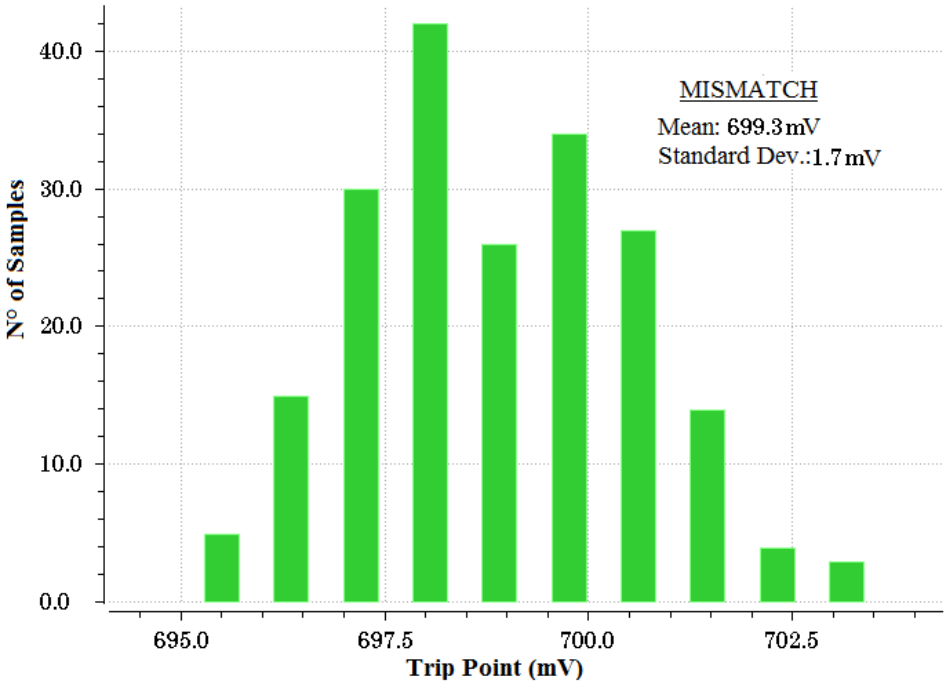
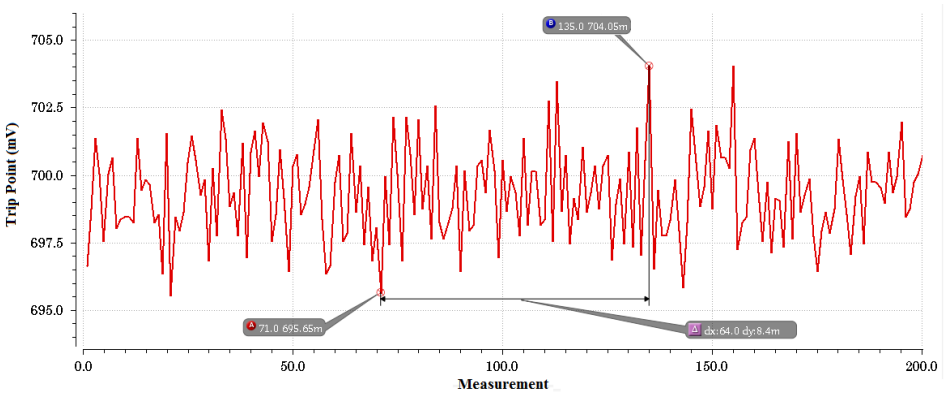


Figure 5.18: Trip point analysis using standard transistors.

Figure 5.18 shows that the comparator switches before that the voltage applied at the input reach the voltage reference value (700 mV). The advance is estimated to be ~ 0.5 mV. The simulation underlines the important role of the block of inverters which allows also with this technology to obtain a very fast transition between the two logic values, as shown in Figure. Moreover, the plot illustrates also that the comparator changes its output exactly when the input of the inverters stage reach the value 600 mV and, therefore, it is reasonable to say that this stage does not cause any offset in the propagation signal.



(a) Histogram of the dispersion.



(b) Distribution of the 200 runs.

Figure 5.19: Dispersion of the trip point obtained with Monte Carlo simulations using standard transistors.

In addition a Monte Carlo simulation with 200 runs is done to estimate the trip point dispersion due to mismatch effects. The results obtained are reported in the histogram of Figure 5.19

The histogram shows that the mean of the dispersion is less than the voltage reference as noticed in the previous analysis and that the standard deviation is limited to the value 1.7 mV. The peak to peak dispersion observed is ~ 8 mV. These results give an important information about the good choice of the transistors dimension used to develop the circuit. In fact, transistors M1 and M2 are designed with a large size so that reduce the mismatch effect [16]. Also with this new technology this choice seems to be enough to obtain a good performance.

- **Configuration with high speed and standard transistors**

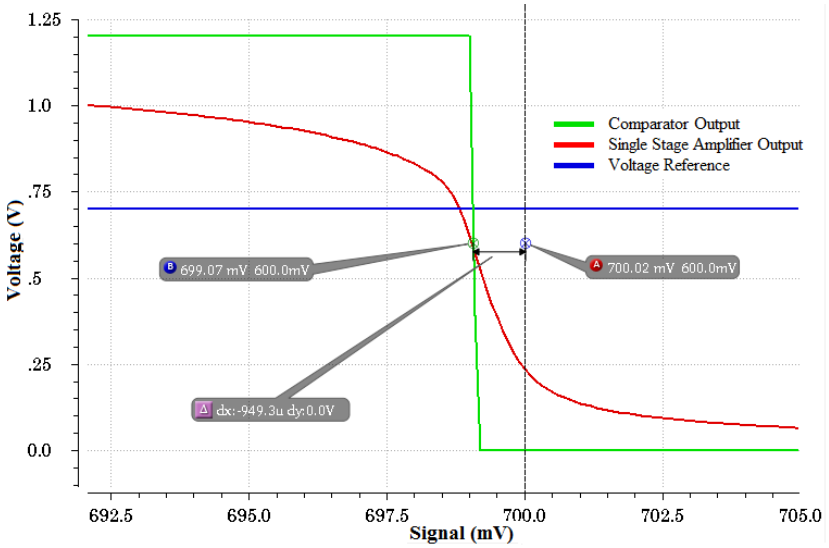


Figure 5.20: Trip point analysis using standard and high speed transistors.

As done with the previous configuration, the Figure 5.20 illustrates the signal voltages at the output of the comparator and at the output of the single stage amplifier. Also in this case it is noticed that the comparator switch before the expected value with an offset of ~ 1mV, which is higher than the previous case.

- **Configuration only high speed transistors**

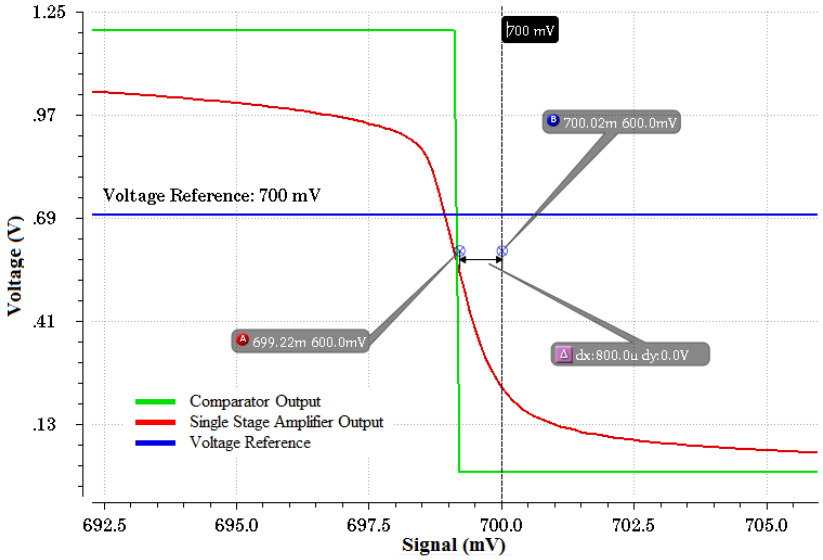


Figure 5.21: Trip point analysis using only high speed transistors.

The results obtained with this last configuration, as depicted in Figure 5.21 show that the inverters block does not create any offset in the propagation signal. Concerning the value of the trip point, also in this case it is lower than the expected value of 700 mV and the offset measured is 0.8 mV.

5.3.2 *Gain analysis*

The second parameter to characterize the comparator with technology B is the gain. To make a fair comparison, the same transistor size of the comparator implemented in technology A is used. Only the cascode voltage is adapted to keep the circuit properly biased at the equilibrium point.

In fact, it is reasonable to expect that, since the new technology uses a different topology of transistor, the voltage threshold is different from the one of the CMOS 0.13 µm. This changes the conditions to have all transistors in saturation region and therefore, changes also the voltage to apply to bias the cascode.

For each configuration the gain is measured using the voltage bias which maximises the performance of the comparator.

The results obtained are reported in Figure 5.22 and resumes in Table 5.3. The bias voltages used for the cascode transistors are 300 mV, 300 mV and 500mV for the configurations with only standard, standard and high speed and only high speed transistors, respectively.

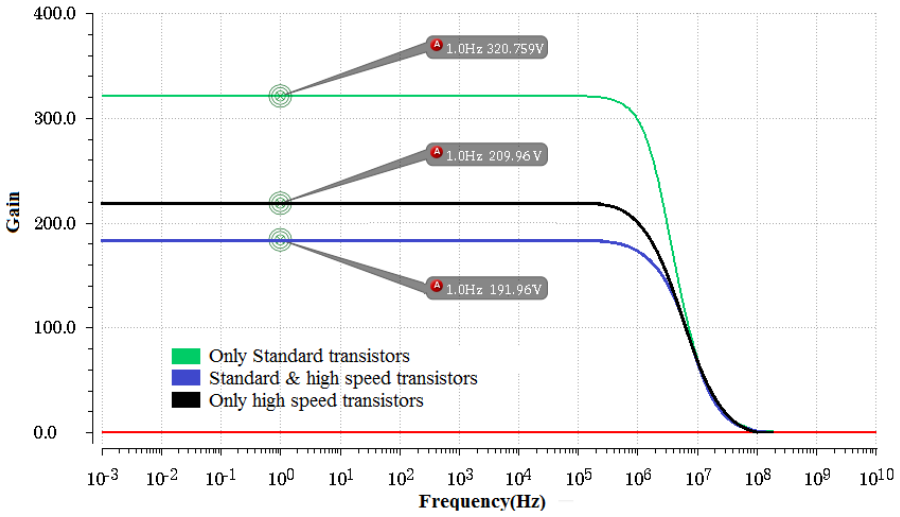


Figure 5.22: Amplifier gains obtained with the different configurations.

GAIN IN THE NEW TECHNOLOGY				
	Standard	**Standard & High speed**	**High Speed**	**Technology A**
Gain	320	191	209	70

Table 5.3: Amplifiers gains obtained with the simulations.

The simulation results show that the gain is constant until ~ 1 MHz for each configuration and that the maximum gain obtained with the use of this new technology corresponds to the configuration which uses only standard transistors. The worse performance is obtained using the configuration which uses both transistors. However, each configuration with the new technology has a gain much bigger than the gain obtained with the current technology which is estimated to be ~ 70.

5.3.3 *Delay time analysis*

To compare the speed performance of the discriminator in the two technologies, the delay time of the signals is the last parameter to estimate. For this reason, as done with the technology A, dedicated simulations are done to estimate the delay obtained with each of the three configuration proposed for the technology B.

The simulation is the same done with the technology A, and consists in a transient analyze of the comparator output starting from a situation where the voltage reference of 700 mV and a voltage of 690 mV are connected to the inputs of the device. Then, a step voltage of variable amplitude is sent together to the DC voltage. In this way, choosing for each measurement a different amplitude, it is possible to simulate the propagation delay of the comparator.

During the simulation for each configuration the step amplitude varies from 20 mV to 120 mV.

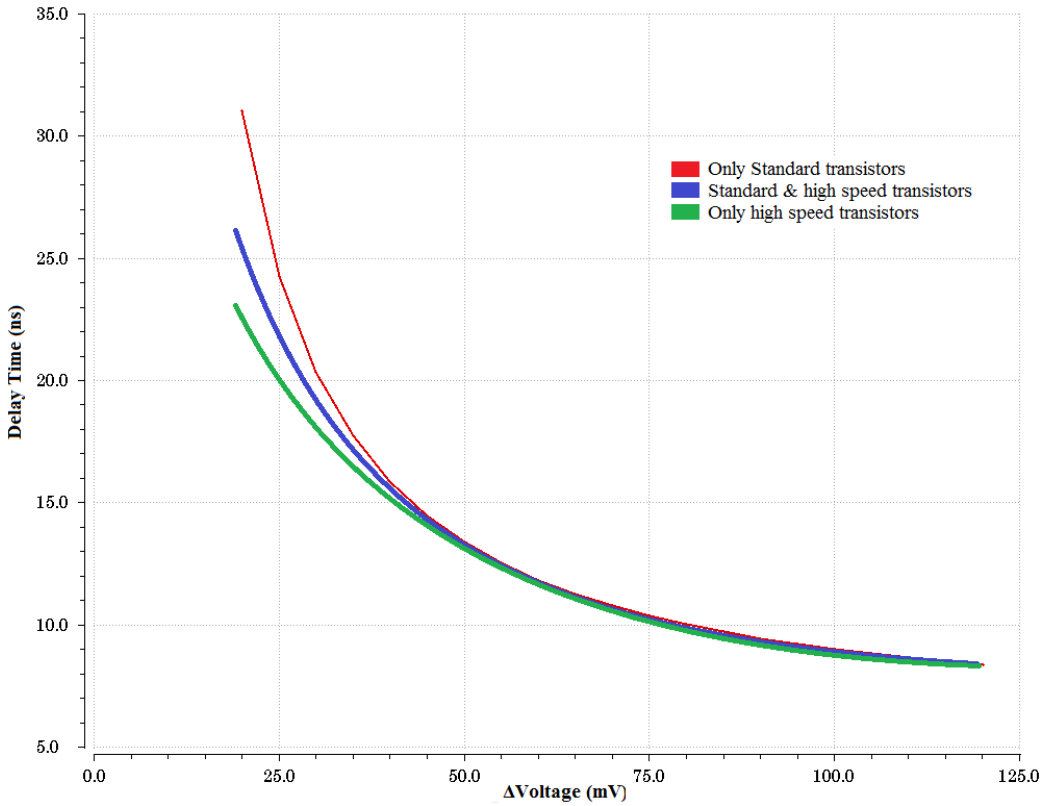


Figure 5.23: Propagation delay obtained with the three configurations.

The results obtained for all the configurations are summarized in Figure 5.23. Also in these case, as observed for the Technology A, in spite of the amplitude of the steps is incremented by the same quantity, the delay observed responses with a non- linear relation. Moreover, the Figure shows that as expected, the best performance is obtained using all high speed transistors. However, for steps bigger than 50 mV, the delay observed is ~ 8 ns for all the configurations.

5.4 COMPARISON BETWEEN THE TECHNOLOGIES

The new technology to use must respect the same requirements of the current technology employed. In order to verify if the proposed technology is adapt to the ASIC requirements, all the blocks of the front-end must be studied and where necessary modified to obtain an adequate performance.

Moreover, although the technology proposed is sub-micron, the radiation hardness must be verified with a dedicated radiation test.

In the previous section the performance of the comparator, has been simulated with both technologies. Calling A technology the CMOS 0.13 μm and B technology the CMOS 0.11 μm, the main results can be summarized in Table 5.4.

COMPARISON OF TECHNOLOGIES

	Technology A	**Technology B**		
Param.	**Standard**	**Standard**	**Stand. & High Speed**	**High Speed**
Trip[mV]	667	700	699	699
Gain	70	320	191	209
Delay[ns]	11	24	22	20
Delay'[ns]	5	8	8	8

Table 5.4: Comparison between the two technologies: To evaluate the delay time it is considered an amplitude for the step to overcome the voltage reference of 25 mV. Delay' instead, is relative to steps bigger than 100 mV.

The simulation results show for the technology A a delay time much lower than the ones obtained for the technology B, also employing high speed transistors. However, these values are valid only for amplitudes of the step to overcome the voltage reference of 25 mV. For amplitudes bigger than 100 mV the delay time observed with the two technologies are similar. Concerning the trip point, the results show that the offset present with the technology A is greatly reduced using the technology B.

Also for the gain, the technology B allows to obtain higher values with all the configurations analyzed.

These results illustrate the good performance of the comparator with the new sub-micron technology even using standard transistors. The only defect might be the delay time observed for small amplitudes, but this is not so significant if, as done for ToPix v4, the gain of the CSA is optimized to obtain a higher value.

6

CONCLUSIONS

The test results of ToPix v3 showed that the prototype needed to be improved in some of its features, as the threshold tuning system. In fact, the non linear response of the comparator threshold to the change in the DAC code observed during the tests, makes the tuning procedure cumbersome. This can be a concern expecially for the final system, where each of the 10.5 million channels of the pixel detector must be calibrated.

In this work the tuning system has been improved with a new circuit which allows to obtain the linearization of the threshold DAC. The solution applied consists in a transconductance amplifier based on a source follower and a differential amplifier which, thanks to a negative feedback, allows to tune linearly the voltage output changing the DAC code. In order to obtain the linearization, the output of this circuit is used as reference voltage and it is sent to the input of the discriminator. The circuit uses a reduced number of transistors due to the area constraint and fits in an area of 13 μm $\times$ 28 μm. The device developed limits the power consumption to $\sim$ 2 μW and takes part of the new configuration of the DAC in ToPix v4. The several post-layout simulations made on the circuit to control the performance of the tuning system show a satisfactory result but is still no guarantee for a completely successful product because the more realistic performance of the chip can only be verified by testing the fabricated prototype. In November 2013 the ToPix v4 prototype, incorporating the circuit designed and the new version of the DAC together with other improvements, was submitted to the foundry for fabrication.

In the second part of this work a CMOS 0.11 μm technology has been investigated as a possible alternative for the ASIC implementation. During this analysis, the discriminator is been studied with the CMOS 0.13 μm technology and the CMOS 0.11 μm technology. The aim of the study is to understand how much effort could be involved in porting the design to the new process. The results show that the discriminator developed with the new technology do not need to be significantly modified to obtain a satisfactory performance. The comparison shows a very good features, as gain and threshold voltage, for the discriminator imple-

mented with the new technology. However, the delay time results to be higher but, since it is possible to overcome this limit with other modifications in the front-end, it is not so significant. This first analysis is very encouraging because it shows that a migration of the design could be straight forward. However, this first indication needs to be consolidated with the implementation of other critical blocks.

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Guarda i girasoli: loro si inchinano al sole,
ma se uno è troppo inchinato vuol dire che è morto.
Tu sei un servitore, non un servo.
Servire è l'arte suprema.
Dio è il primo servitore;
Lui è il servitore di tutti gli uomini,
ma non è il servo di nessuno.

— "La vita è bella"

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