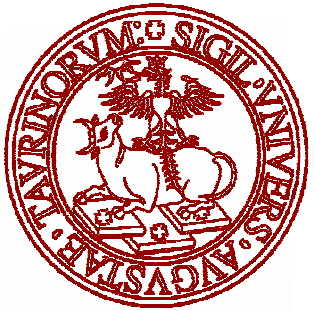


LOW POWER FRONT-END ELECTRONICS FOR HYBRID PIXEL DETECTORS

~ Master Degree in Physics of Advanced Technologies ~

SUPERVISOR

Prof. Angelo Rivetti

CANDIDATE

Olave Elias Jonhatan

CONTEXT

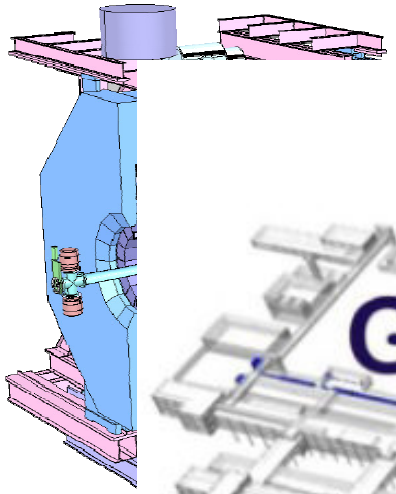
Developement for the panda Detector

WORK TOPIC

Design of a new Digital to Analog Converter for the ASIC

Study of a new technology for the ASIC

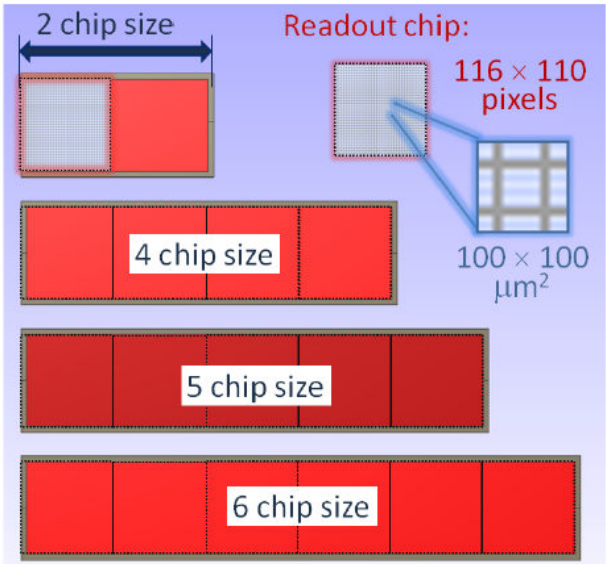
THE DETECTOR



Micro Vertex Detector

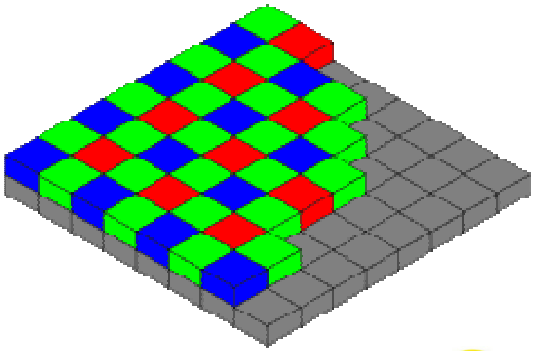
Requirements for the MVD
Good spatial resolution (< 100 μm)
Good time resolution (< 10 ns)
Low material budget

HYBRID PIXEL DETECTORS



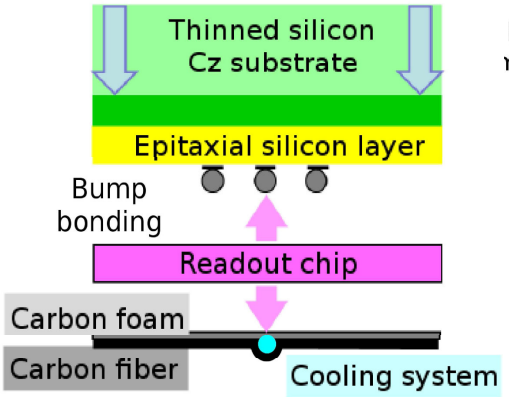
ASIC Requirements

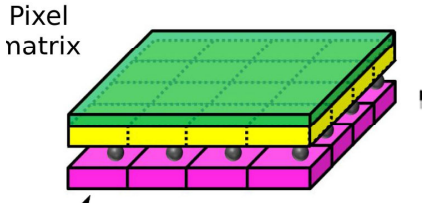
Measurements	Hit position Energy loss Time
Pixel Size	100 μm x 100 μm
Time/charge digitization	At pixel level
ASIC Size	Fixed by the pixel size
Input Polarity	Selectable
Trigger	Self triggering
Power Consumption	< 20 μw



116 rows
110 cols

- More channels are required
- The compact design allow to optain a very good resolution also with high rates

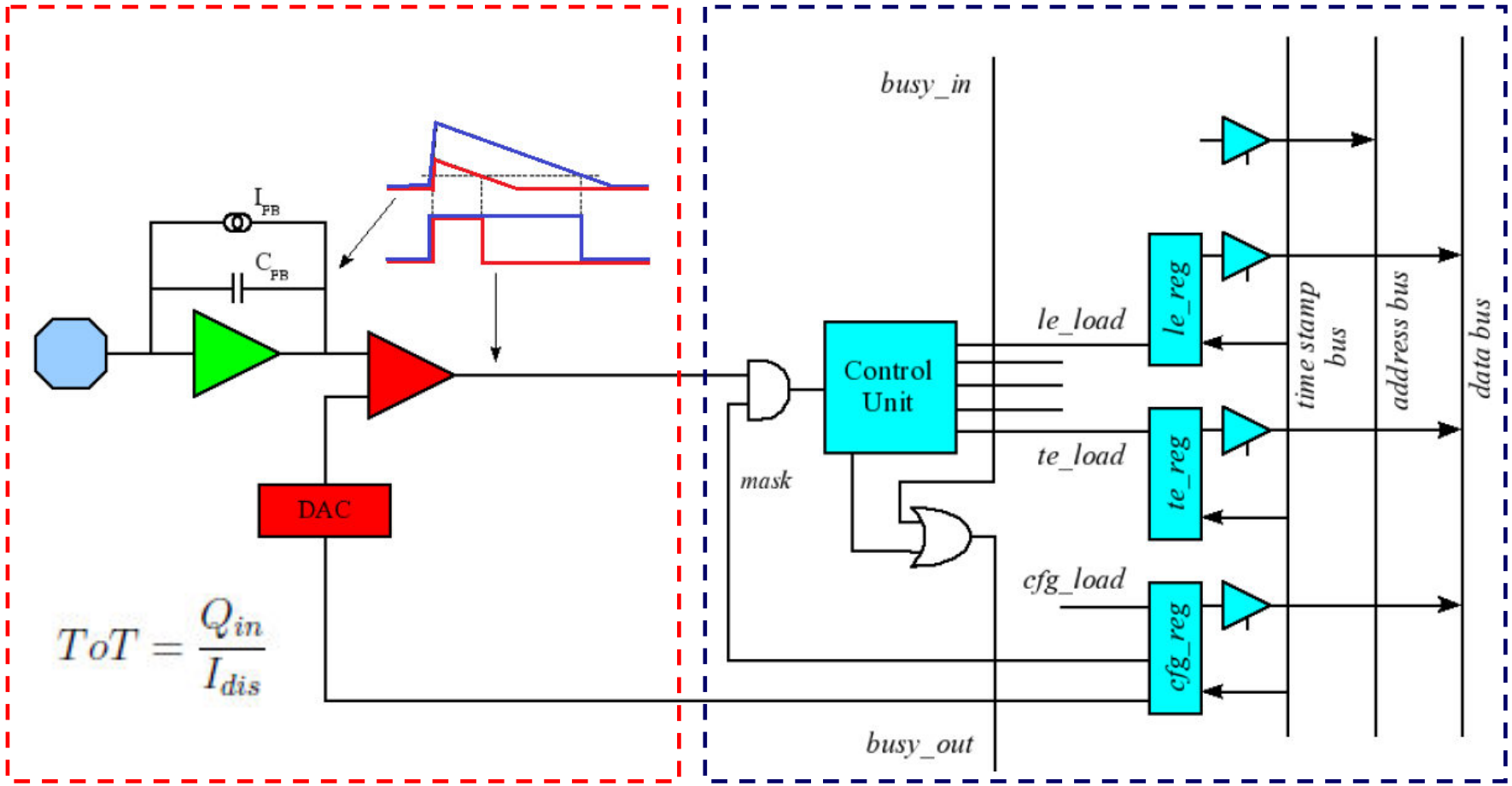




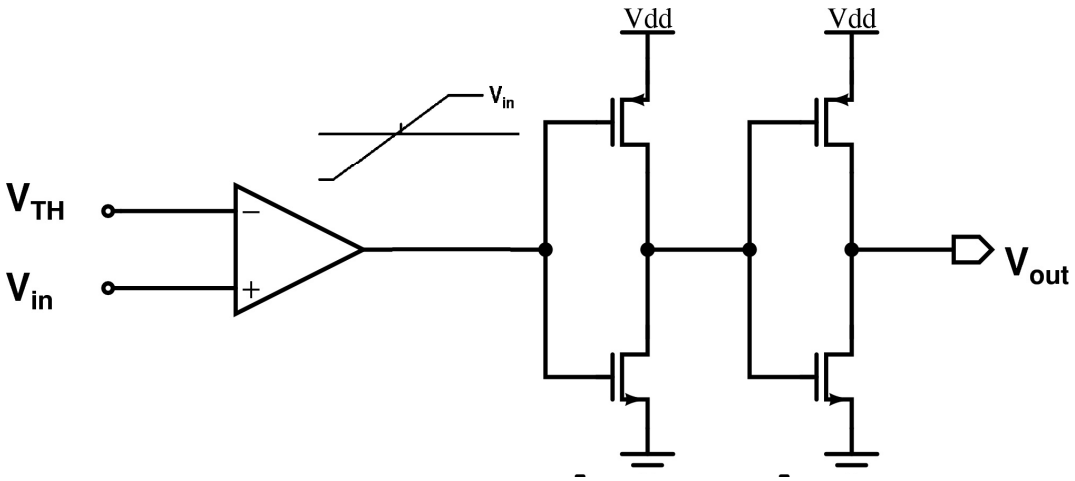
THE PIXEL ARCHITECTURE

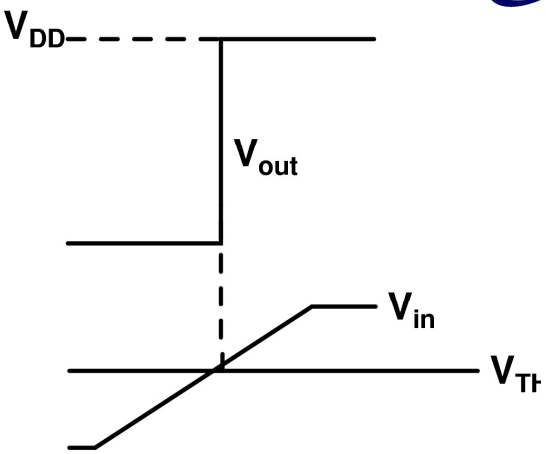
Analog Readout

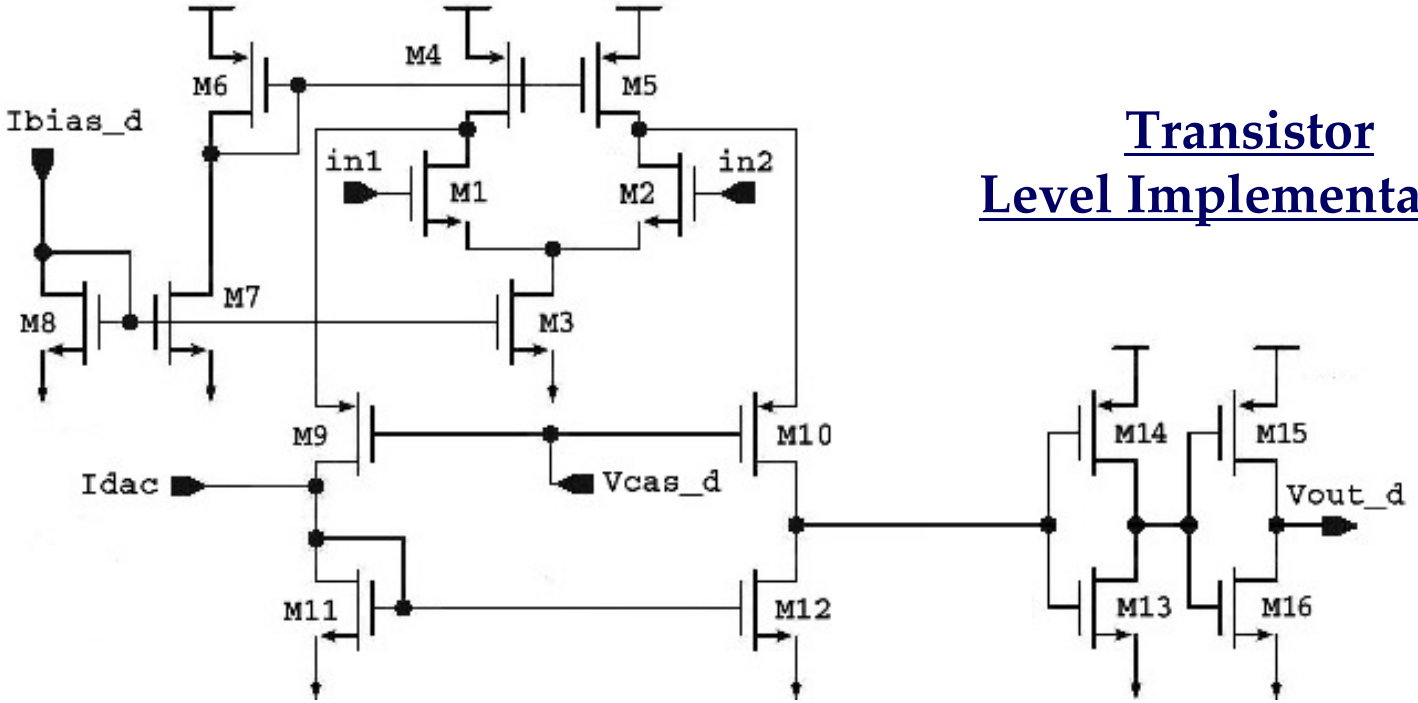
Digital Readout



THE DISCRIMINATOR

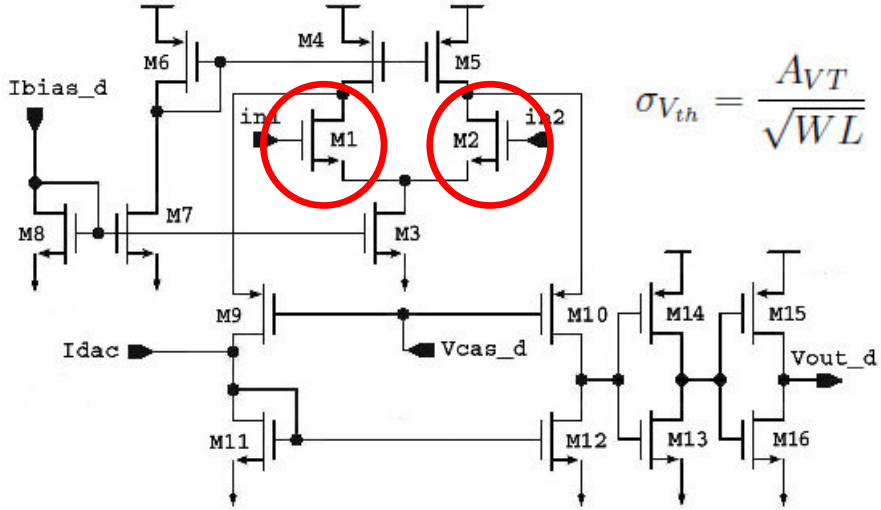






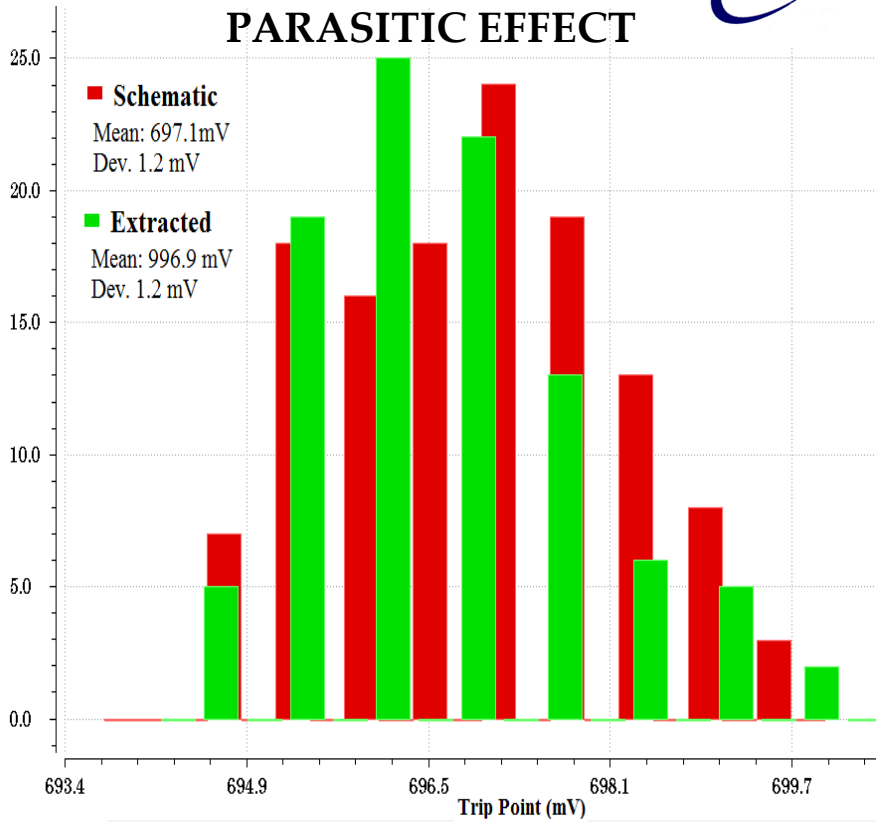
Transistor Level Implementation

THE DISCRIMINATOR

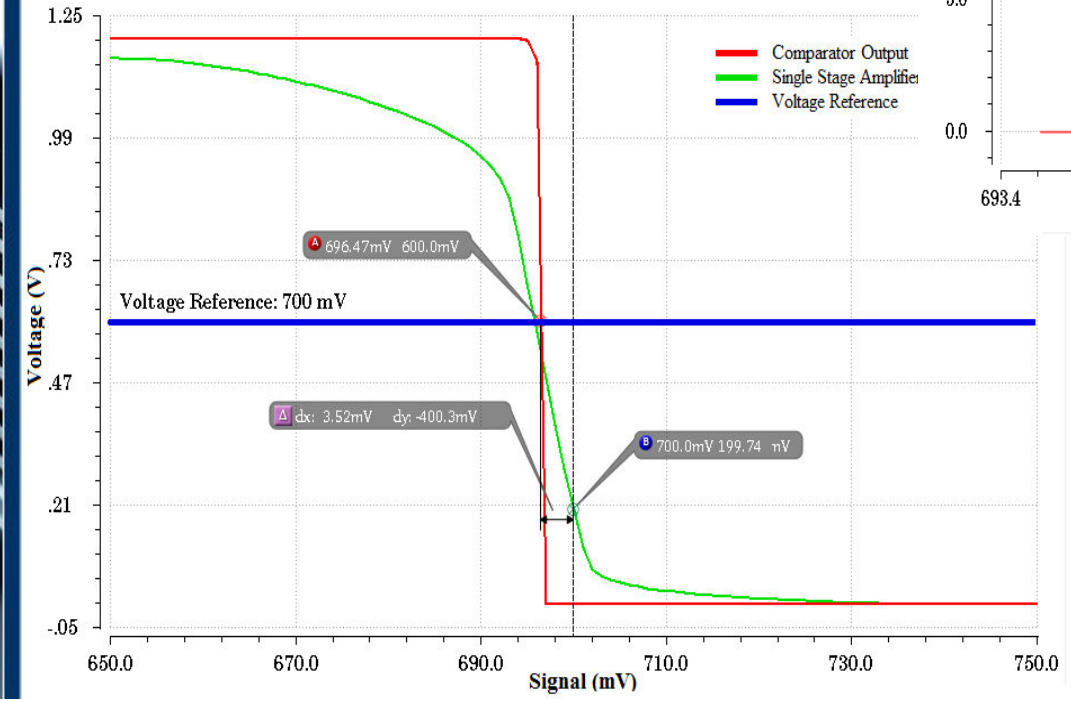


$$\sigma_{V_{th}} = \frac{A_{VT}}{\sqrt{WL}}$$

PARASITIC EFFECT

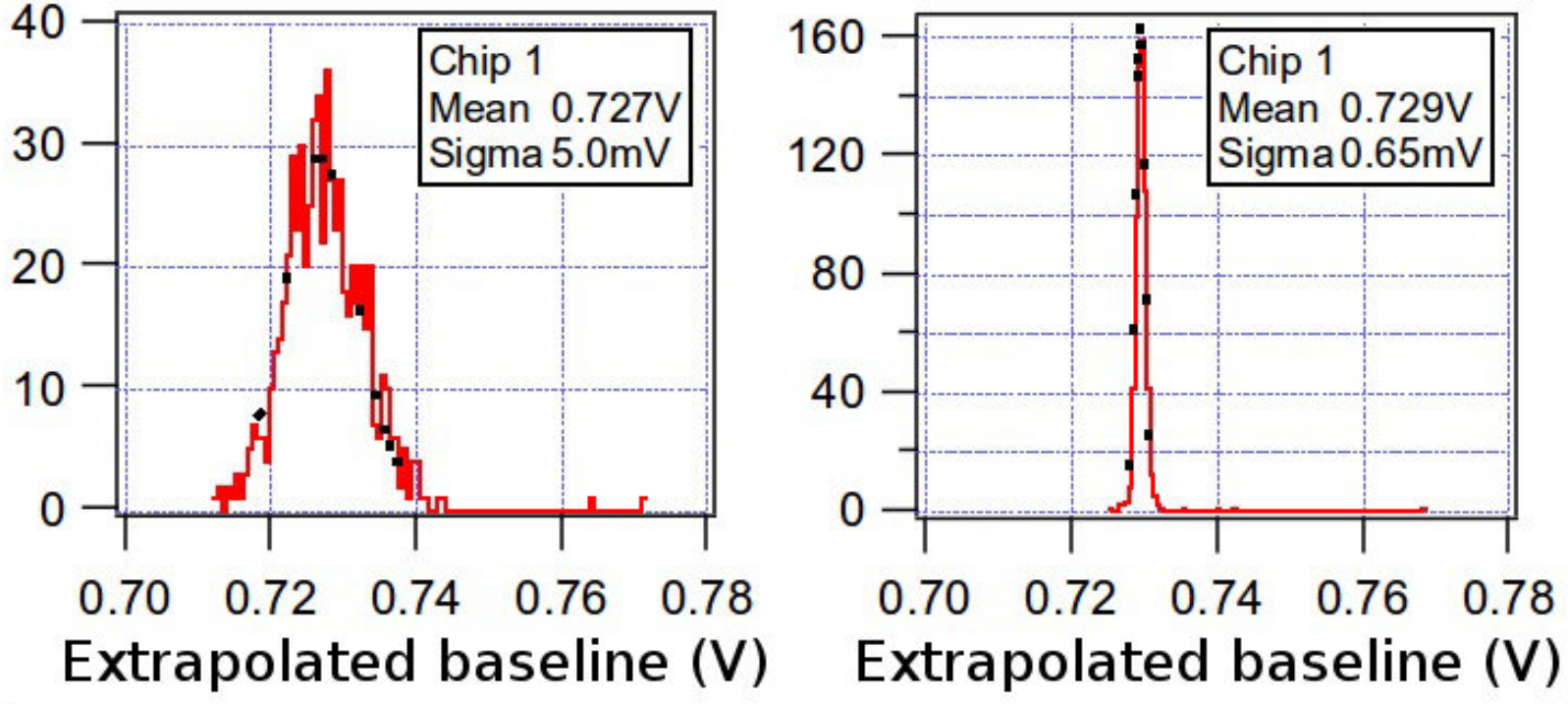


OFFSET



- Defined digital output
- Offset of ~ 2.6 mV
- Influence of parasitic effects

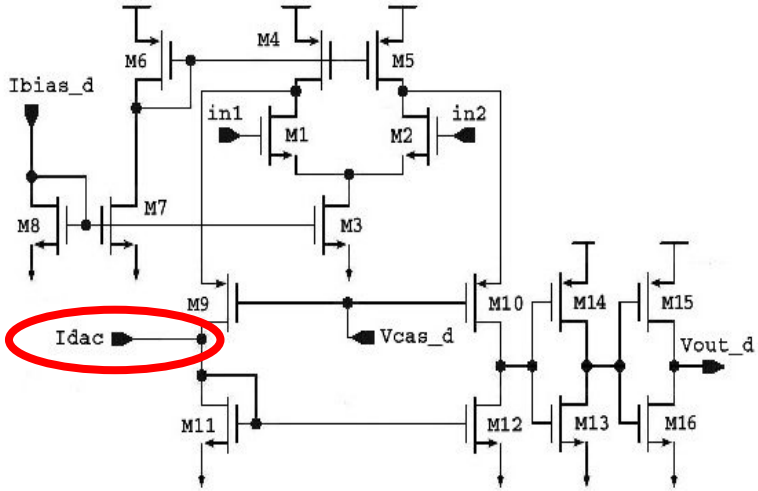
The tuning threshold system in ToPix 3



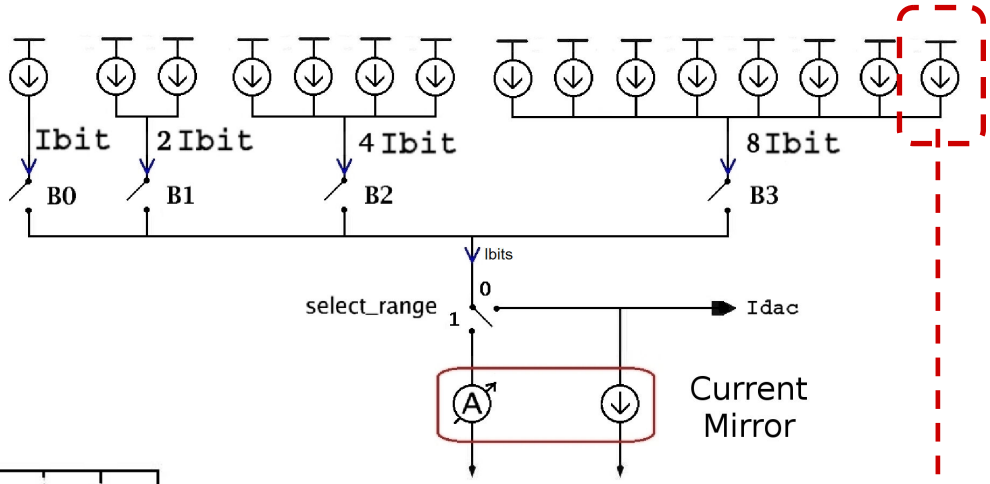
- The system allows a good correction
- Due to a non-linear response the tuning procedure appears cumbersome

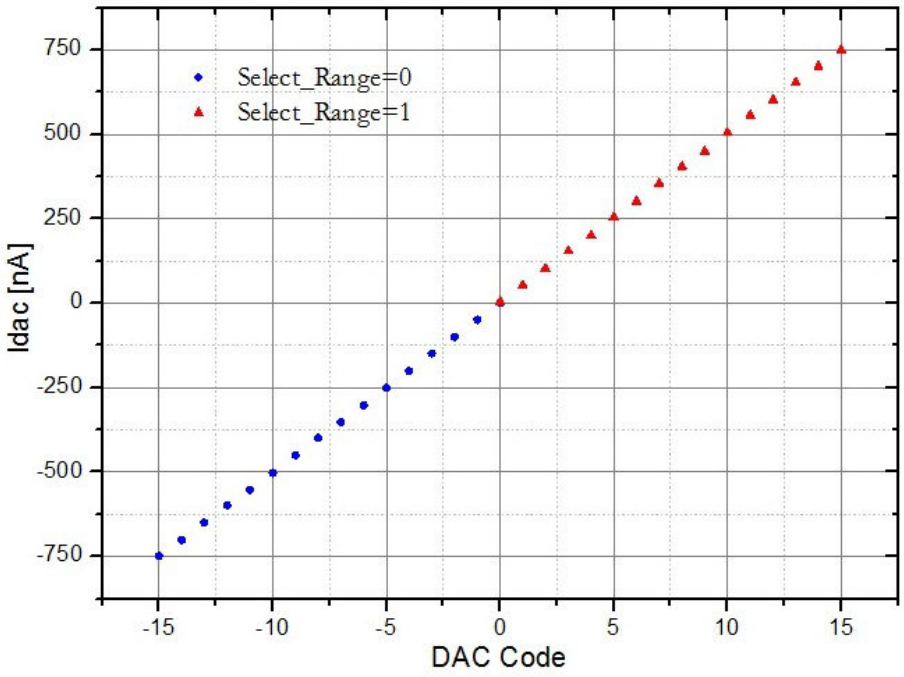
The devices involved are: COMPARATOR & DAC

The DAC

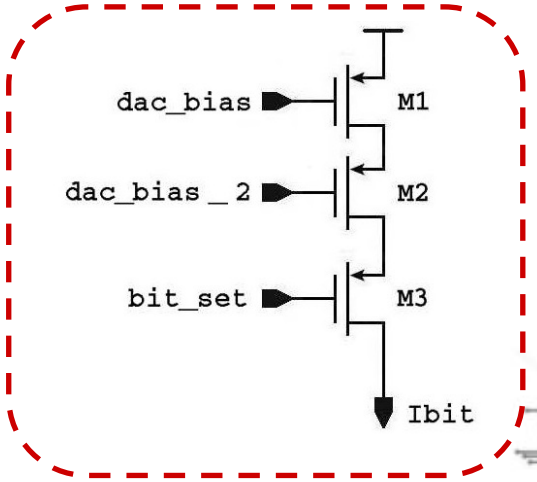


❑ Simple model for the I DAC

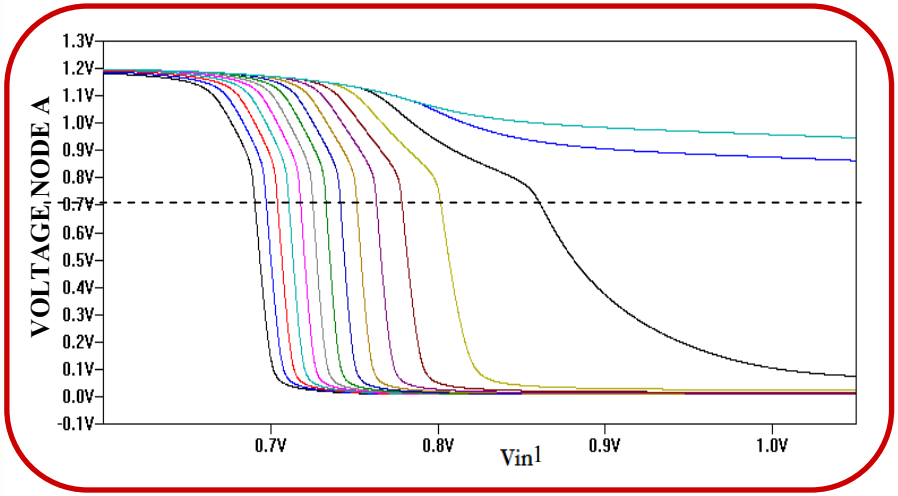


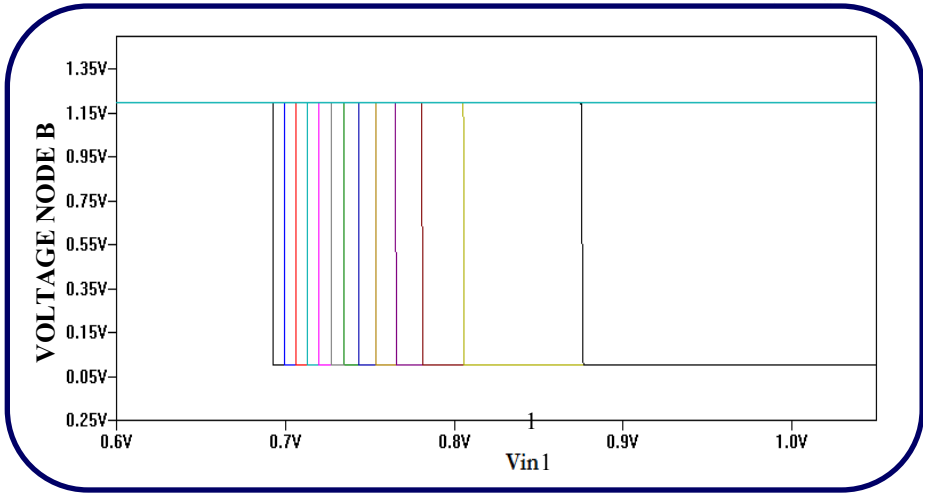


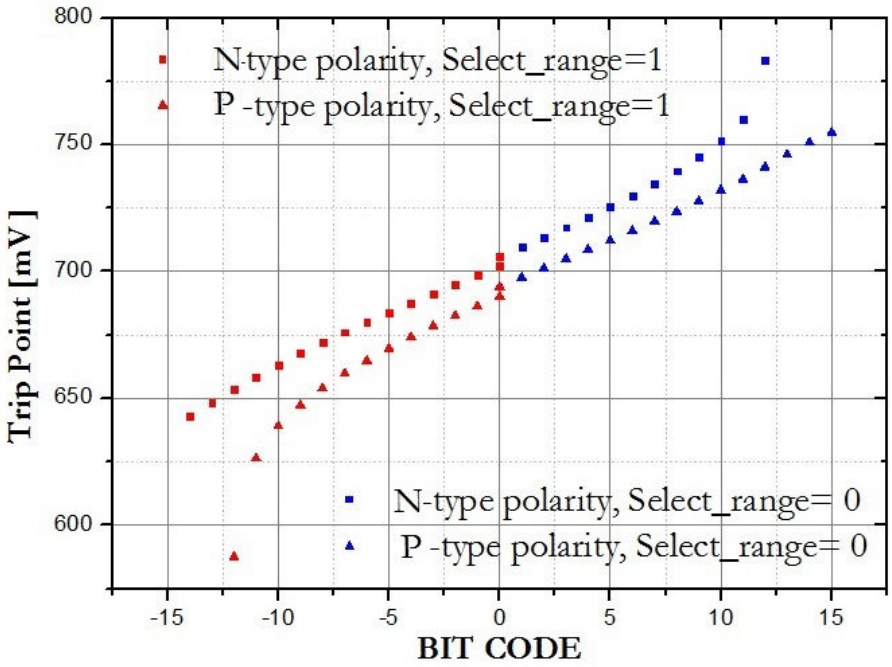
❑ Single bit implementation

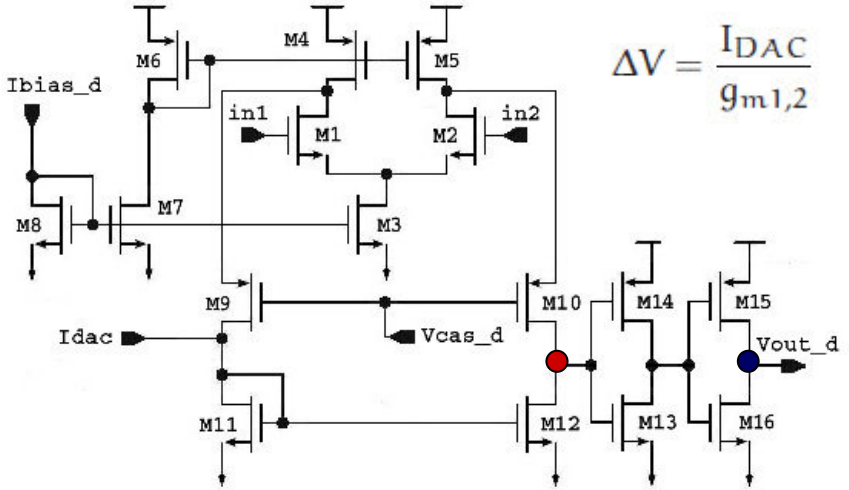


THE NON-LINAR EFFECT







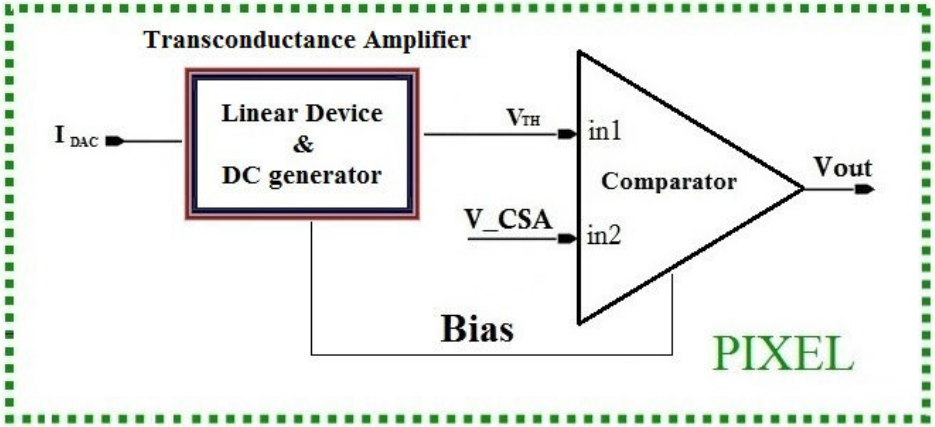


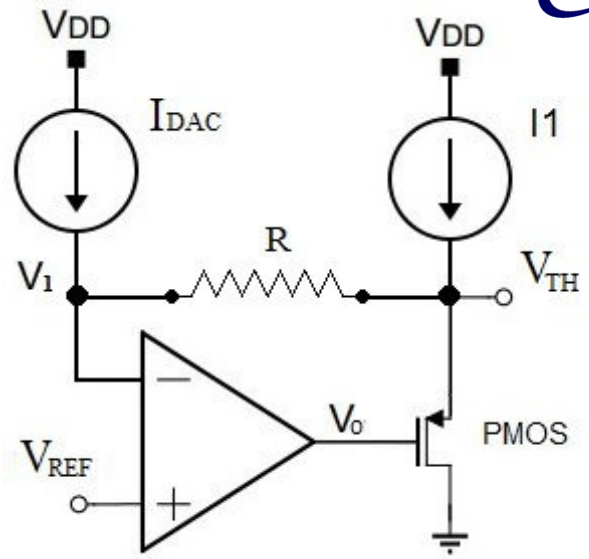
$$\Delta V = \frac{I_{DAC}}{g_{m1,2}}$$

● NODE A

● NODE B

The solution for the linearization





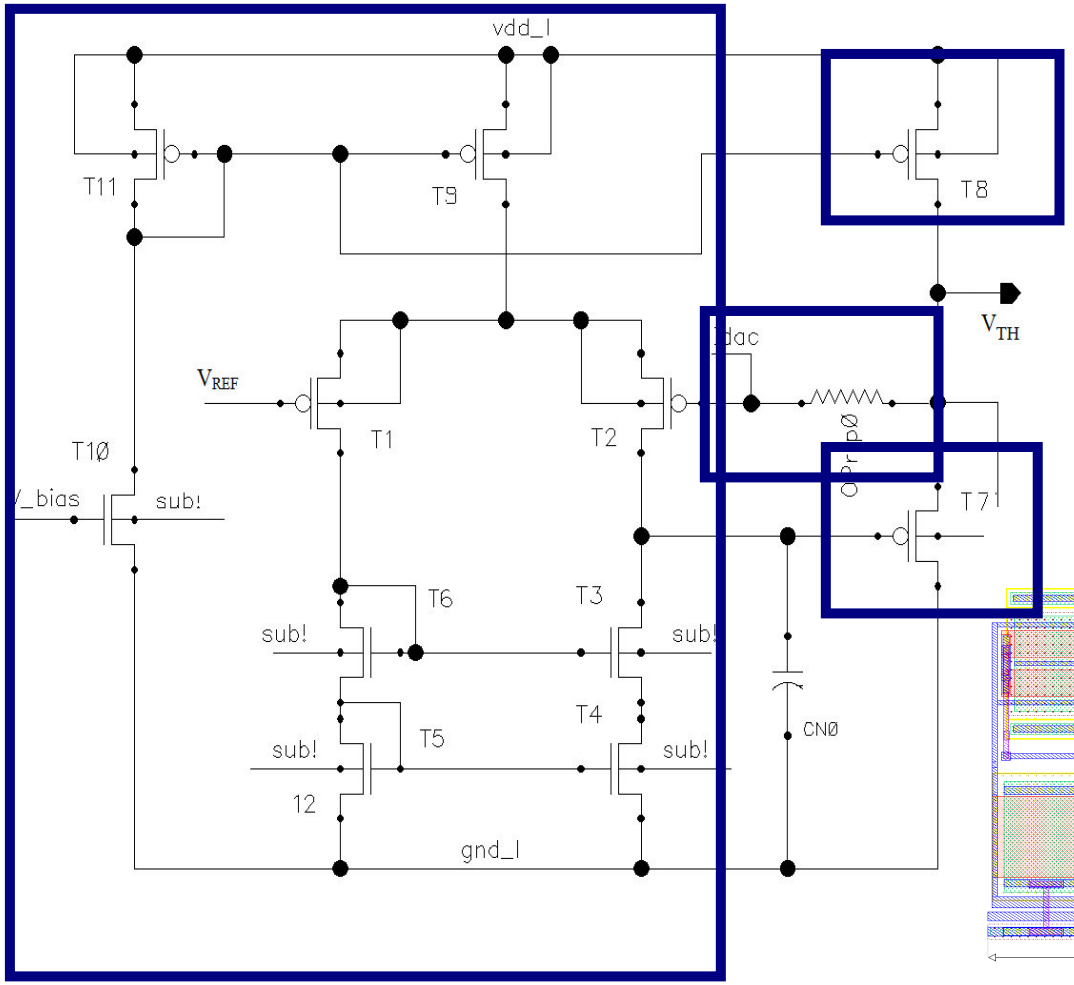
$$V_{TH} = (V_{REF} + R \cdot I_{DAC}) \cdot \frac{A}{1+A} + \frac{1}{1+A}\left[\sqrt{\frac{(I_{SD} + I_{DAC})}{k}} + |V_{THp}|\right]$$

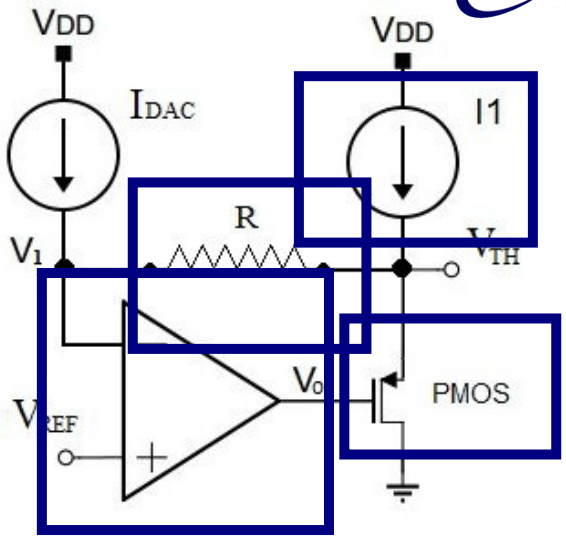
$$\lim_{A \mapsto \infty} (V_{REF} + R \cdot I_{DAC}) \cdot \frac{A}{1+A} \rightarrow (V_{REF} + R \cdot I_{DAC})$$

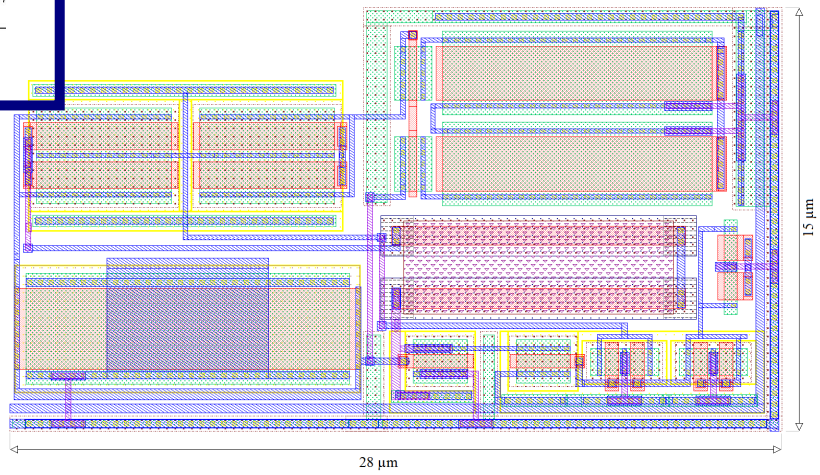
$$\lim_{A \mapsto \infty} \frac{1}{1+A}\left[\sqrt{\frac{(I_{SD} + I_{DAC})}{k}} + |V_{THp}|\right] \rightarrow 0$$

$$V_{TH} \simeq (V_{REF} + R \cdot I_{DAC})$$

The solution for the linearization



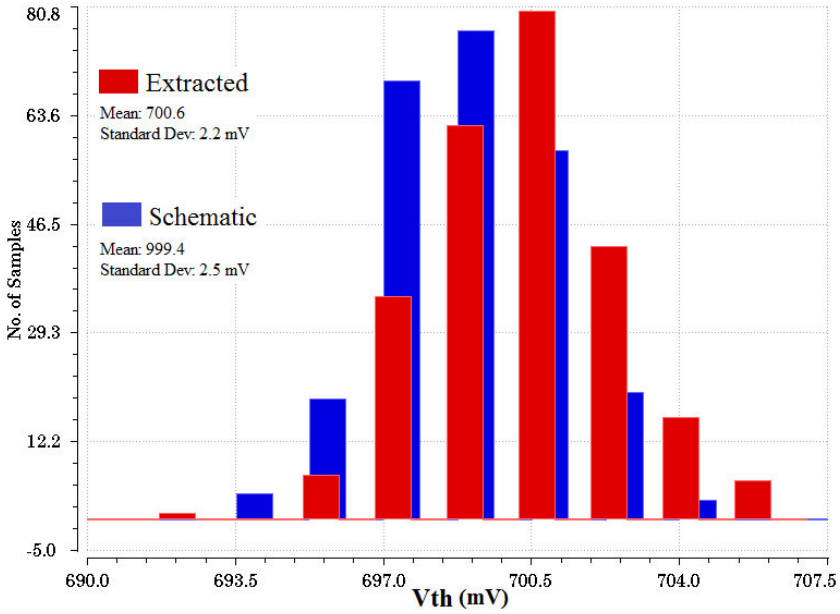




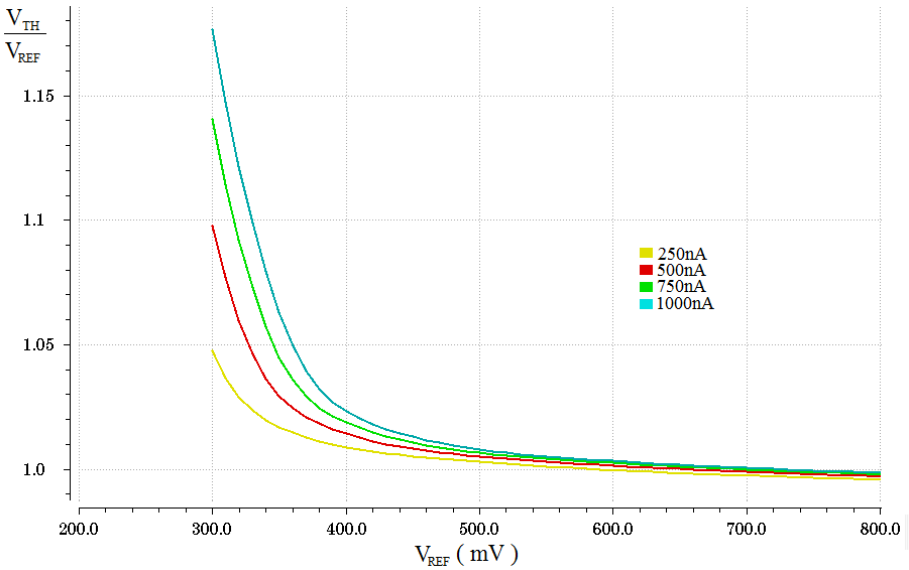
Some trade-offs are necessary to fit the circuit in the available area.

Post-Layout Simulations

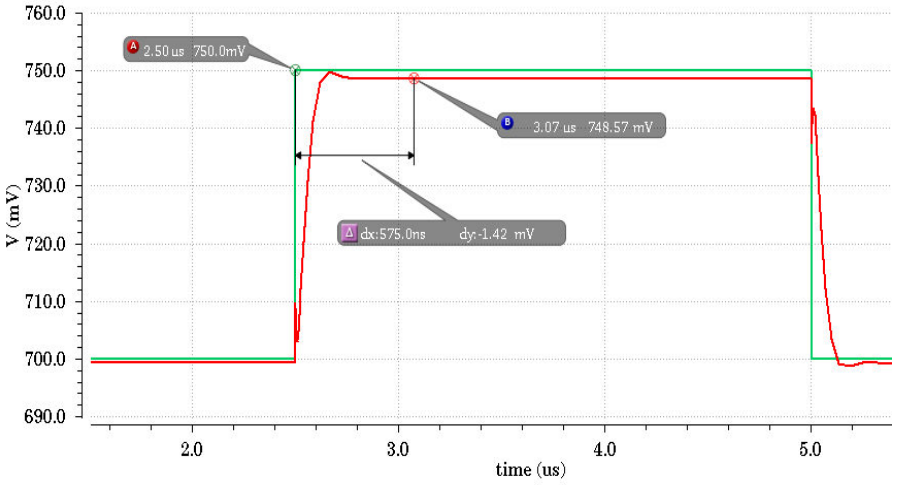
Mismatch

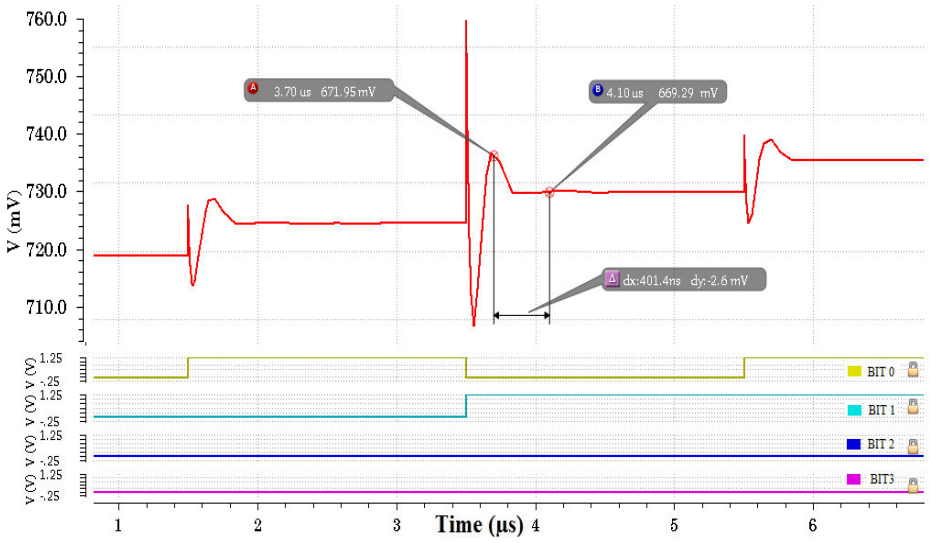


Dependence on the biasing



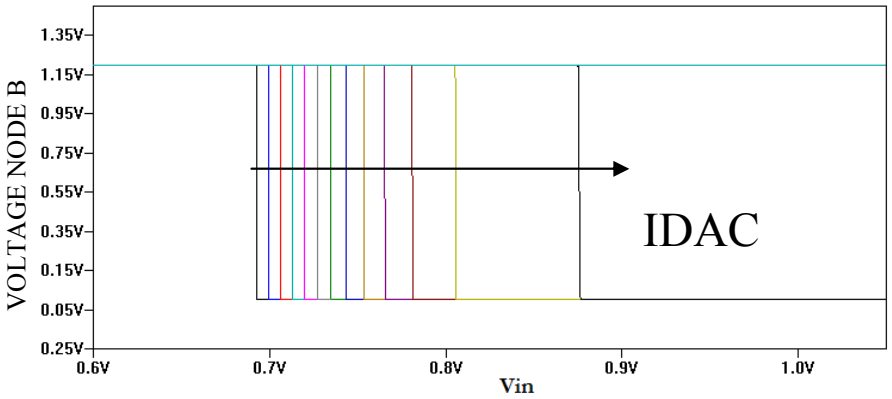
Stability analysis

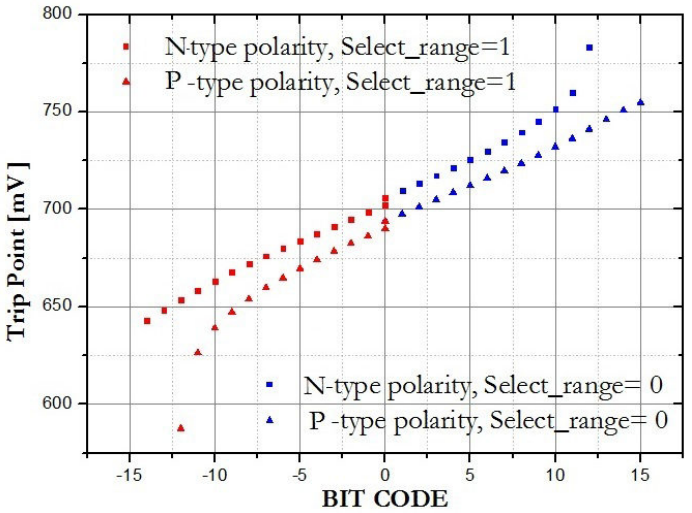




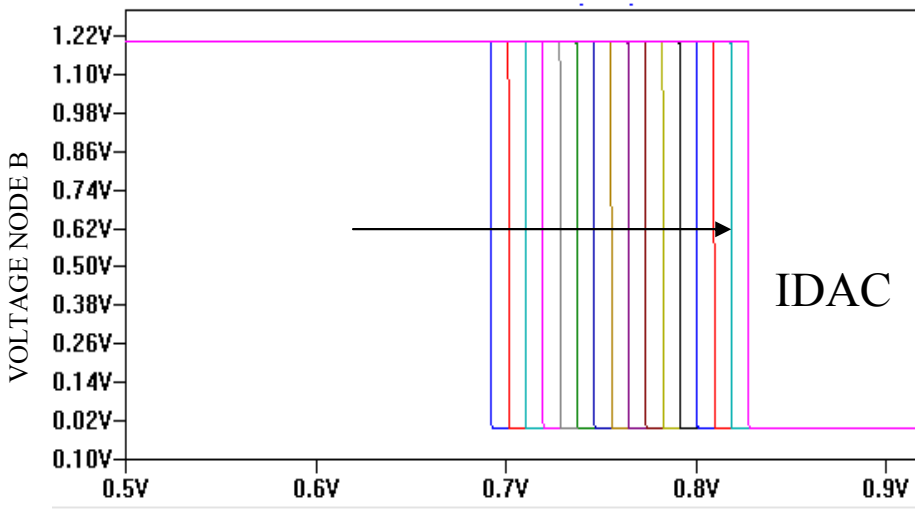
The linearization

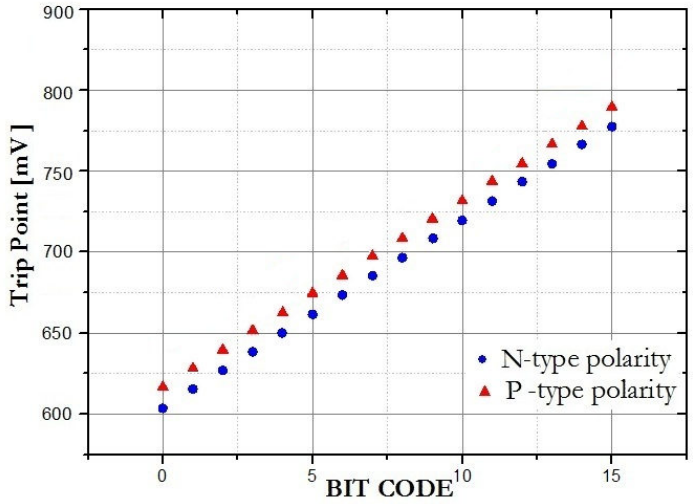
ToPix 3





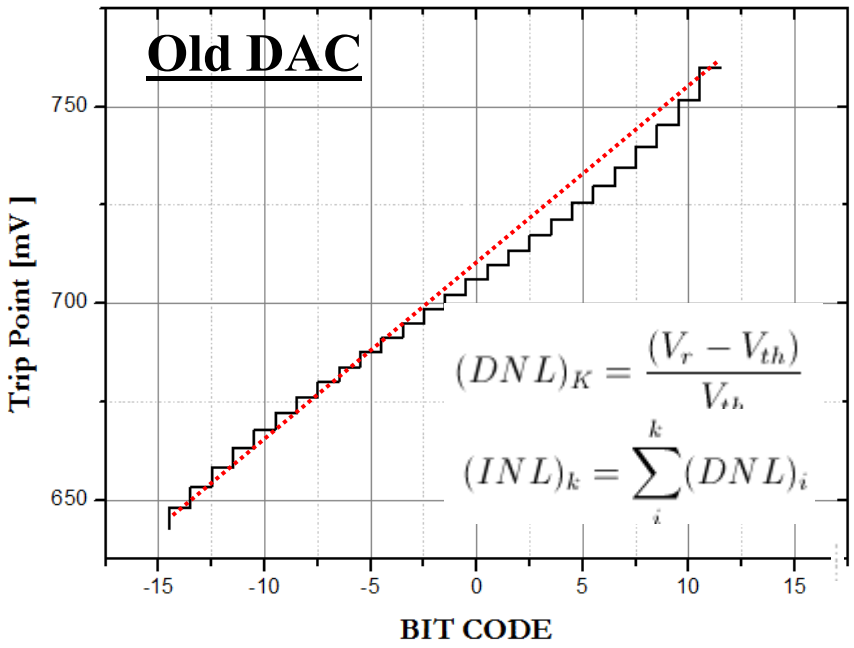
ToPix 4

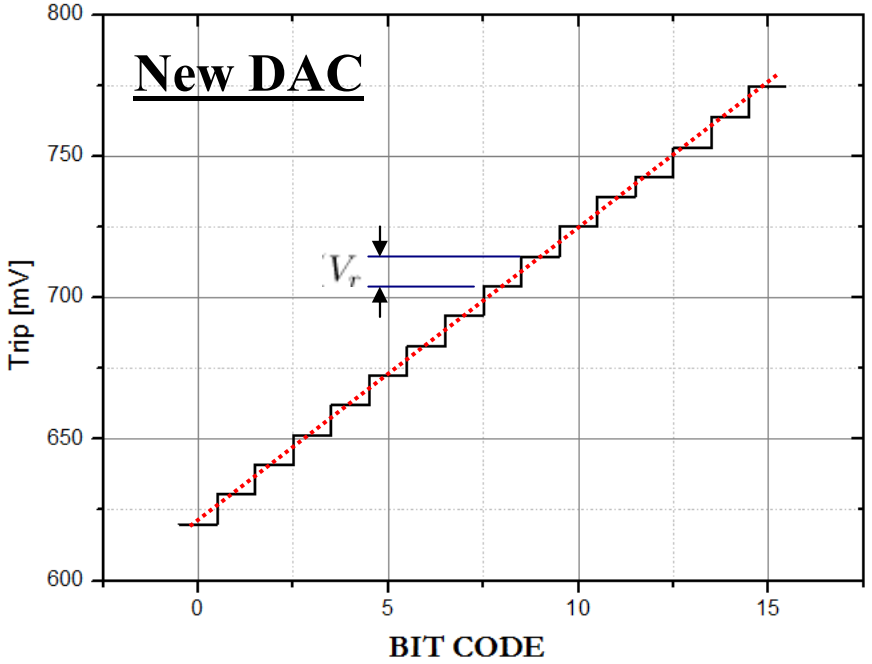


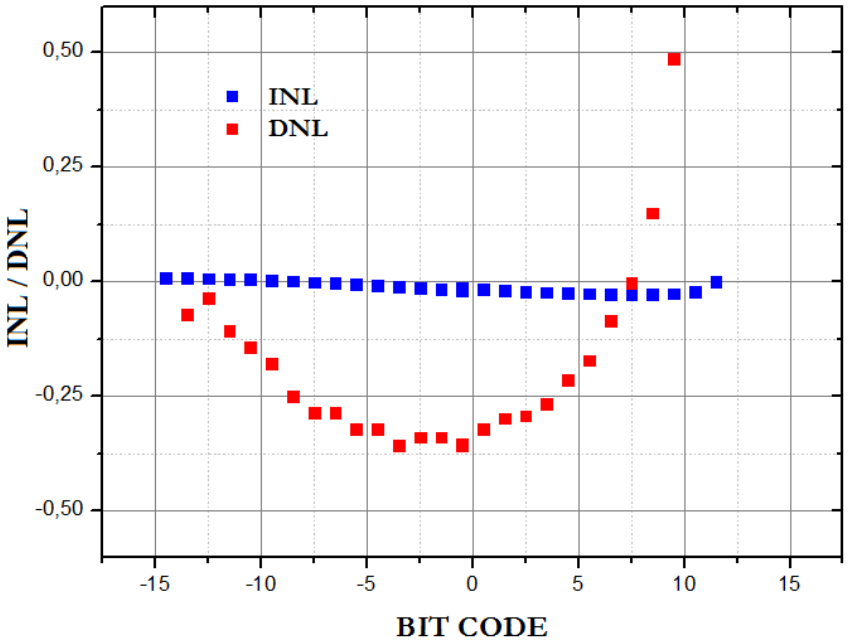


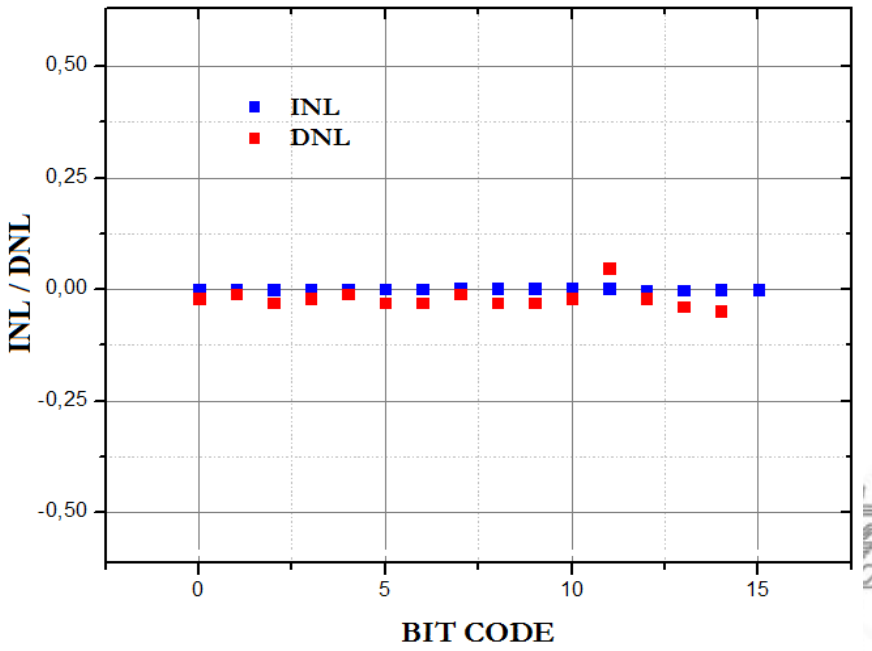
- The linear response in a large range
- It is possible modify the range

Comparison between DACs



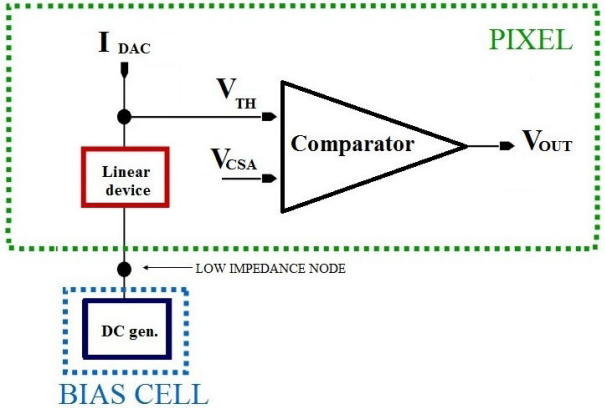




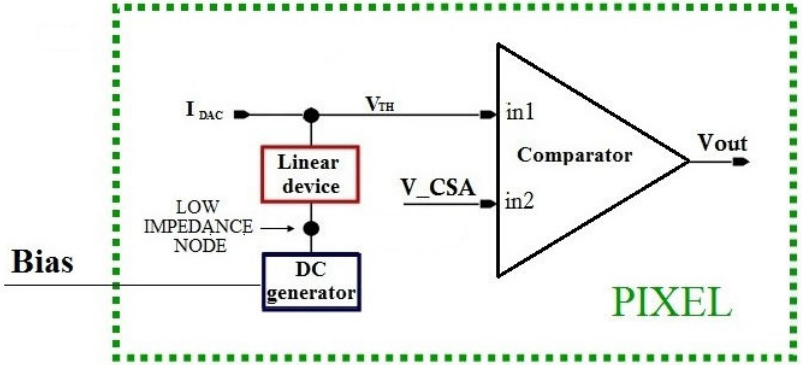


Other solutions studied

Solution A



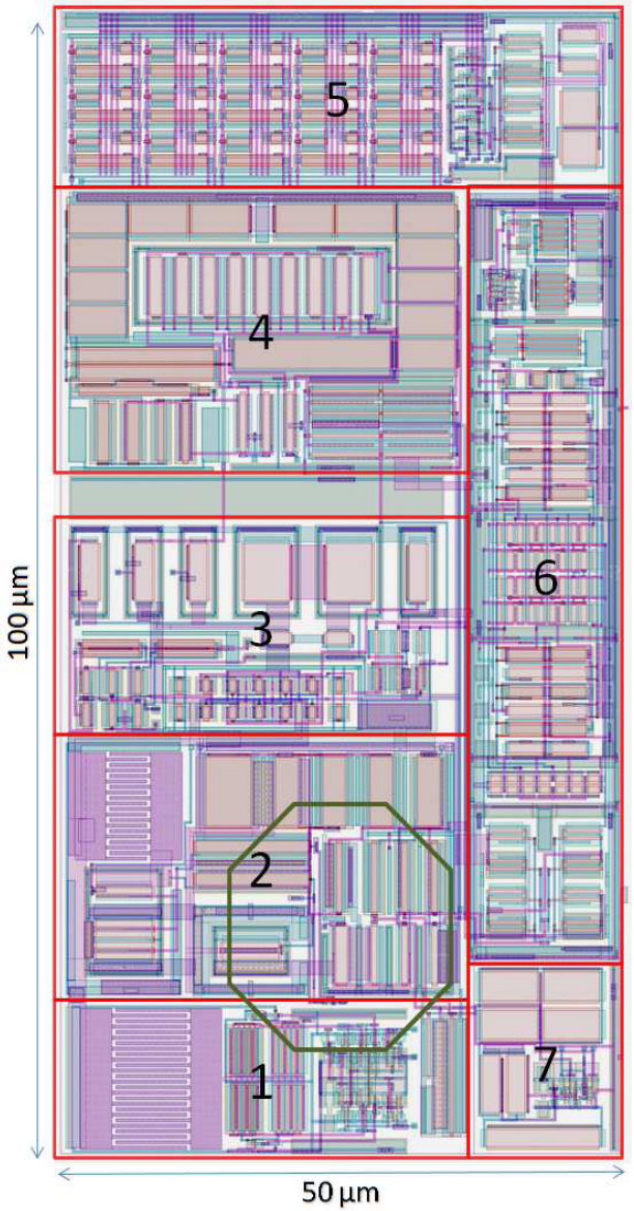
Solution B



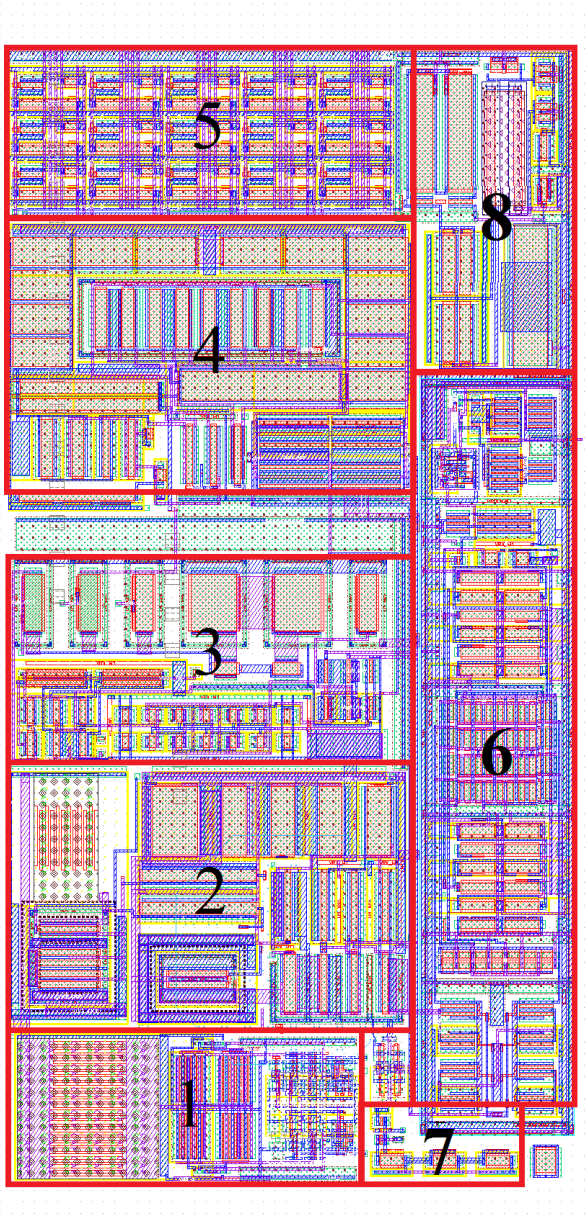
Results

	Mean value MISMATCH	Dev. Stand	Low impedance node	Homogeneity in different pixels	External bias	DAC protection
Solution A	700 mV ✓	1 mV ✓	✓	✗	✗	✗
Solution B	700 mV ✓	1.8 mV ✓	✓	✓	✗	✗
Final solution	697 mV ✓	1.9 mV ✓	✓	✓	✓	✓

Layout of the analog pixel cell



ToPix 3

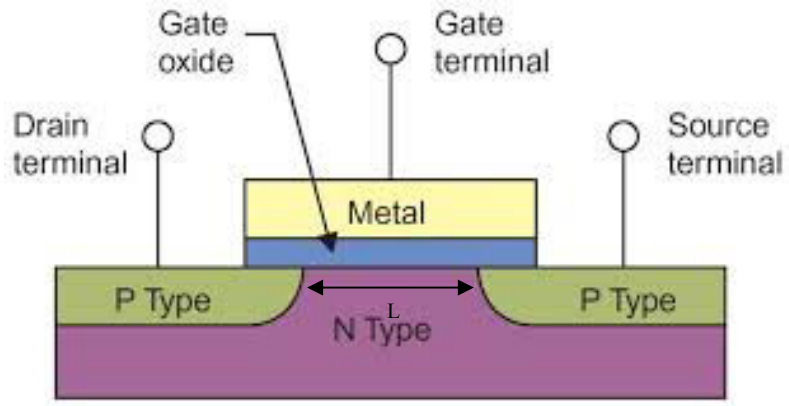


ToPix 4

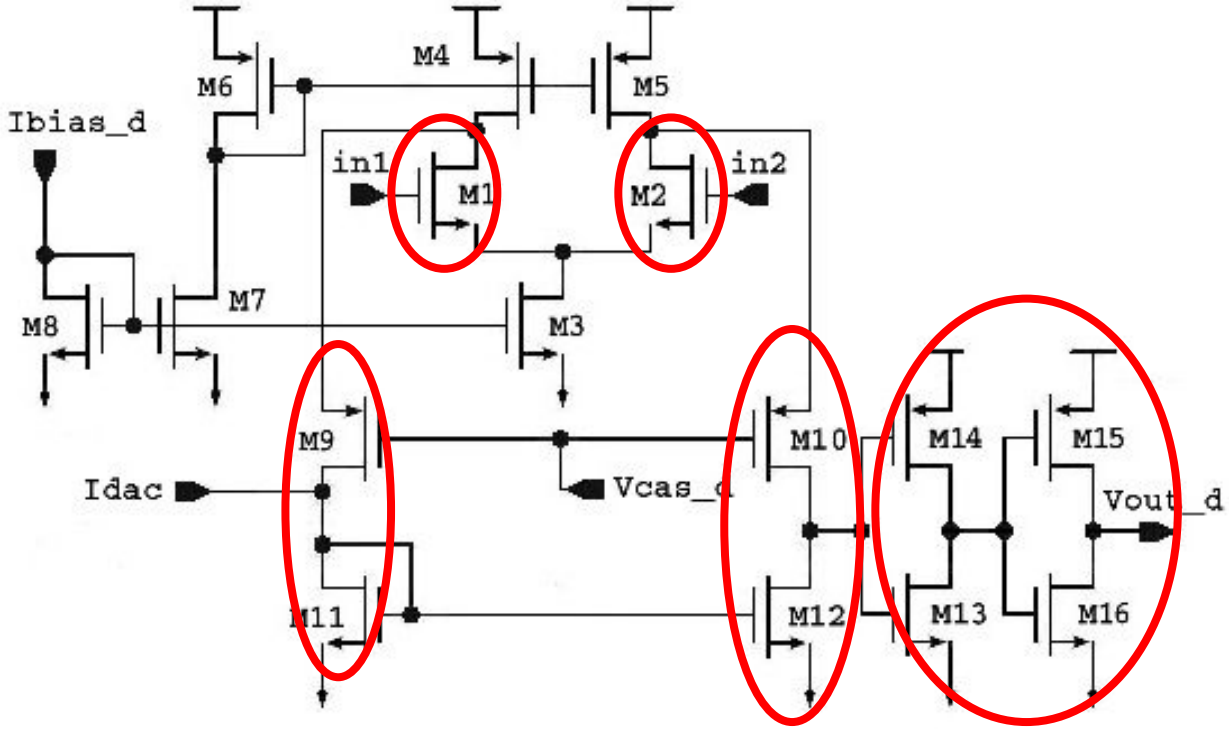
1 – Calibration circuit
2 – CSA
3 – Const. current feed-back
4 – Leakage compensation
5 – DAC
6 – Comparator
7 – Clipping circuit
8 – Lineariz. Circuit

A POS S I B L E NEW T ECHNOLOGY FOR THE FRONT- END

- **Current Technology A 0.13 µm**
  - More flavors of devices
  - High cost
- **Proposed Technology B 0.11 µm**
  - Less flavor of devices
  - Reduced cost

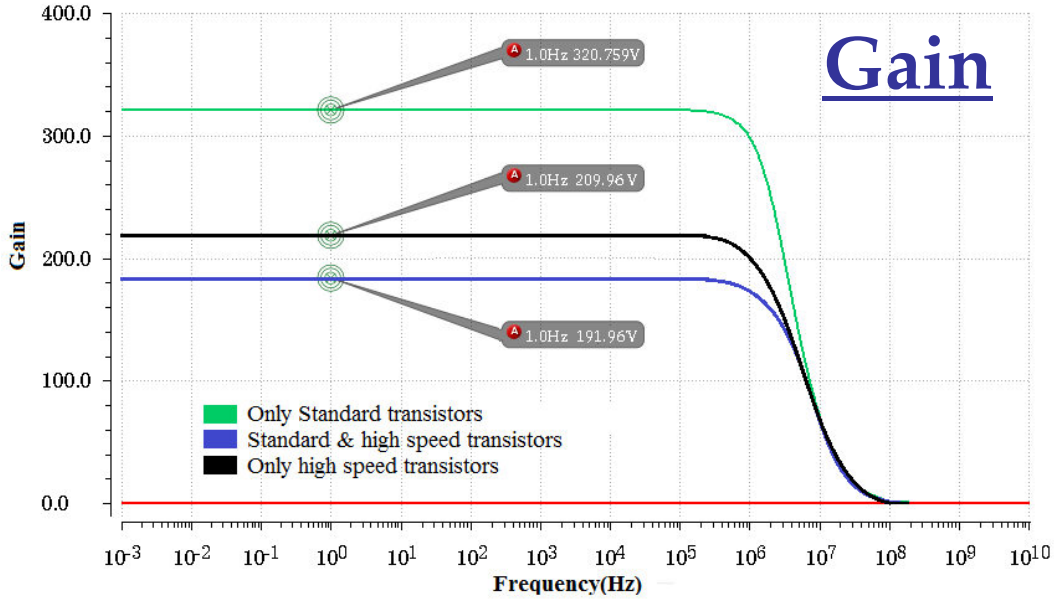


Study of the new technology

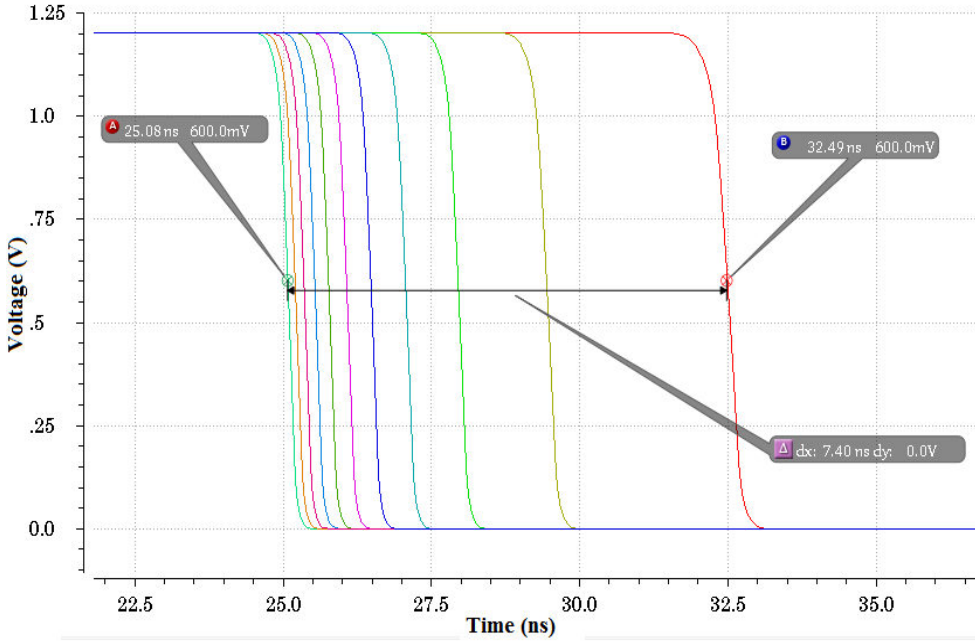


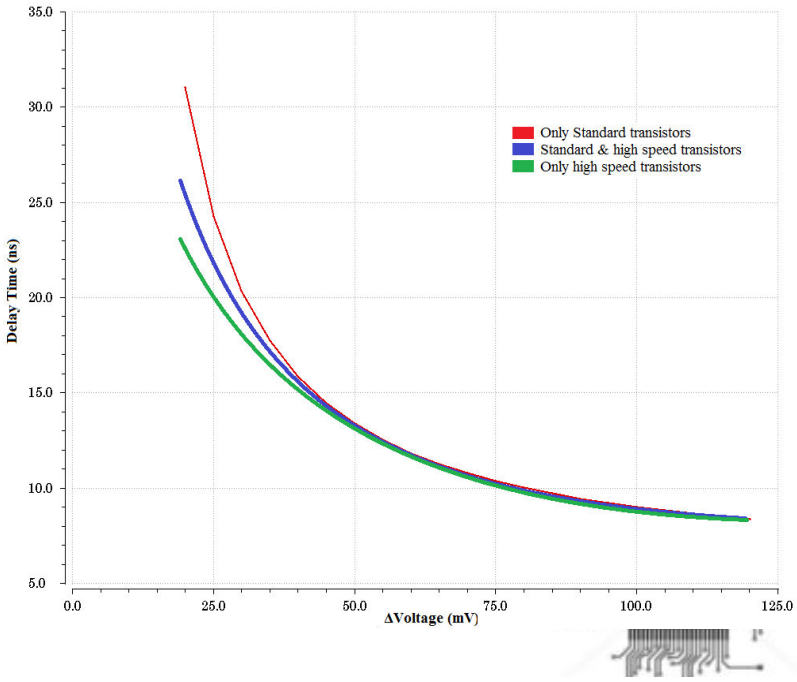
- **Three configurations**
  - Standard transistors
  - High speed transistors and Stantard Transistors
  - All High speed transistors
- **The analysis**
  - Gain
  - Offset
  - Delay time

Gain



Delay Time





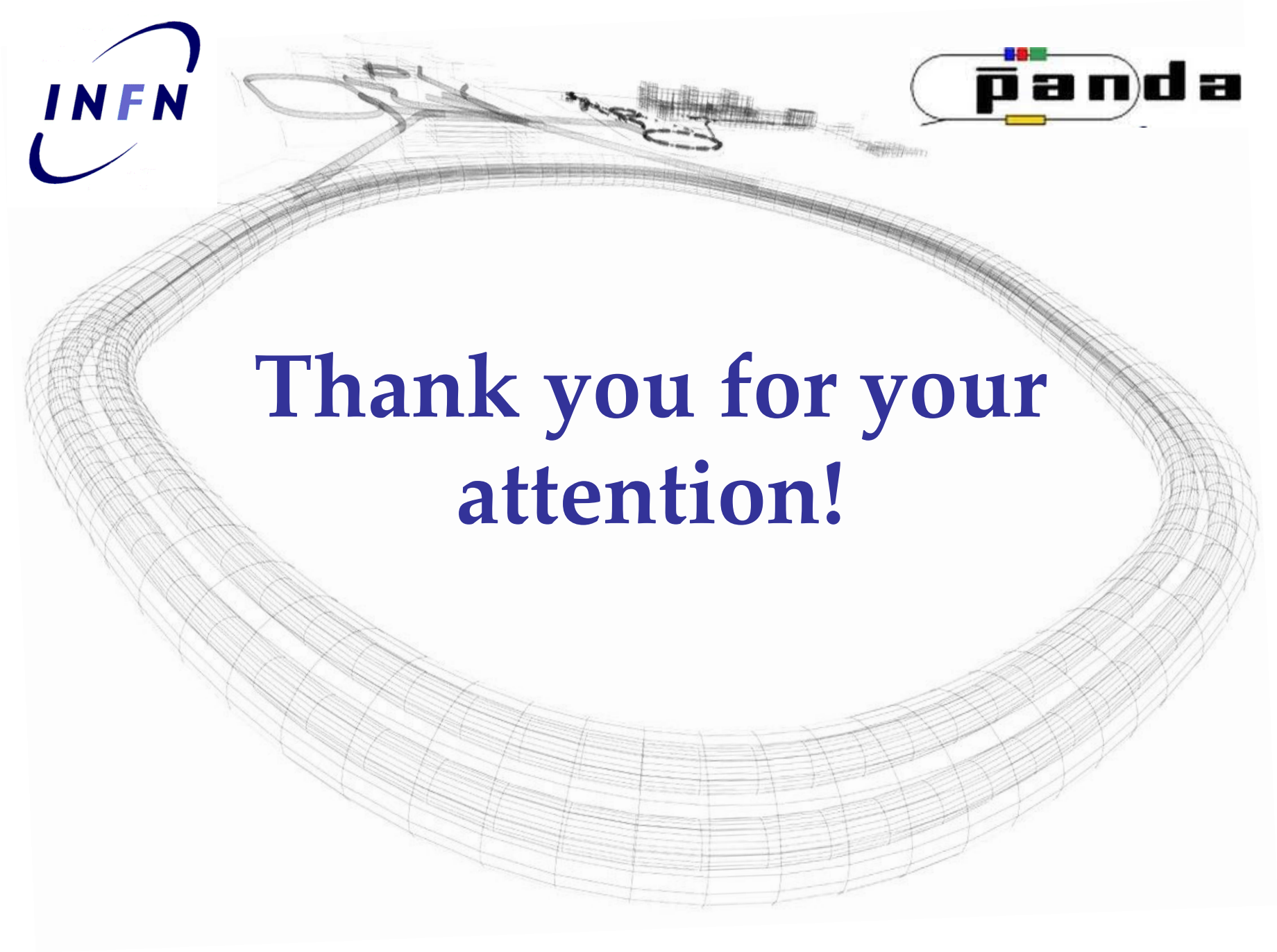
Results

COMPARISON OF TECHNOLOGIES				
	Technology A	Technology B		
Param.	Standard	Standard	Stand. & High Speed	High Speed
Trip[mV]	697	700	699	699
Gain	70	320	191	209
Delay[ns]	11	24	22	20
Delay'[ns]	5	8	8	8

- THE NEW TECHNOLOGY ALLOWS TO OBTAIN;
  - Higher gain
  - Better control voltage
  - Higher delay time

CONCLUSIONS

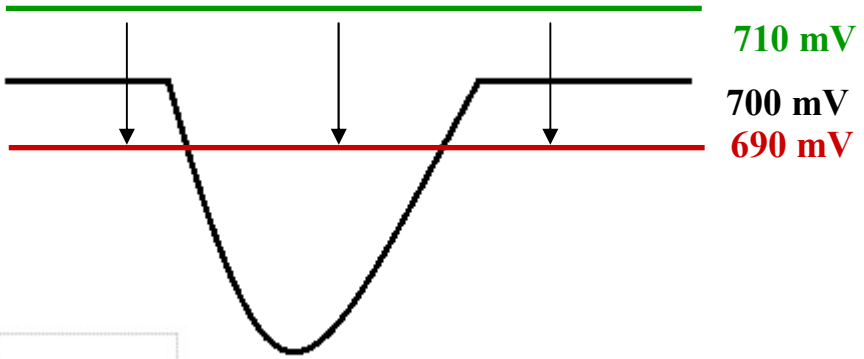
- The solution for the tuning system has been found
- In Novembre 2013 ToPix 4 with the improvement realized was submitted to the foundry for fabrication.
- The analysis of the new technology shows good results for the comparator.
- The study of the new technology for the whole ASIC needs more studies.

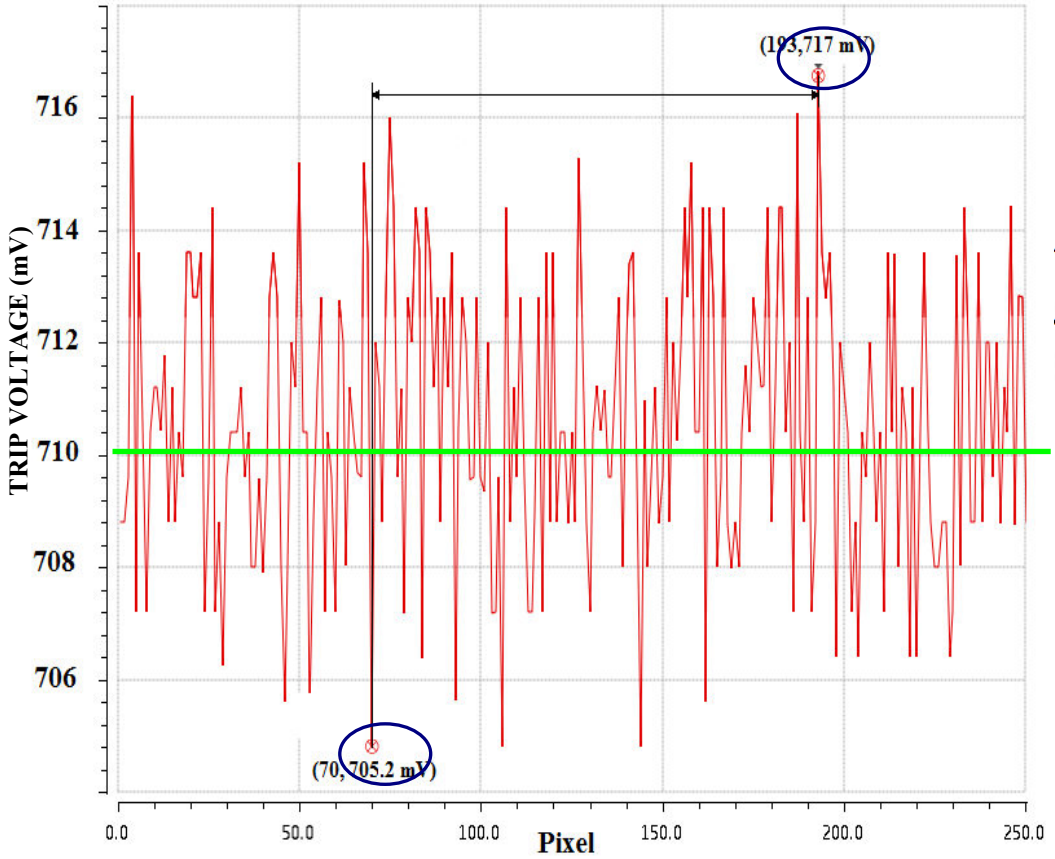


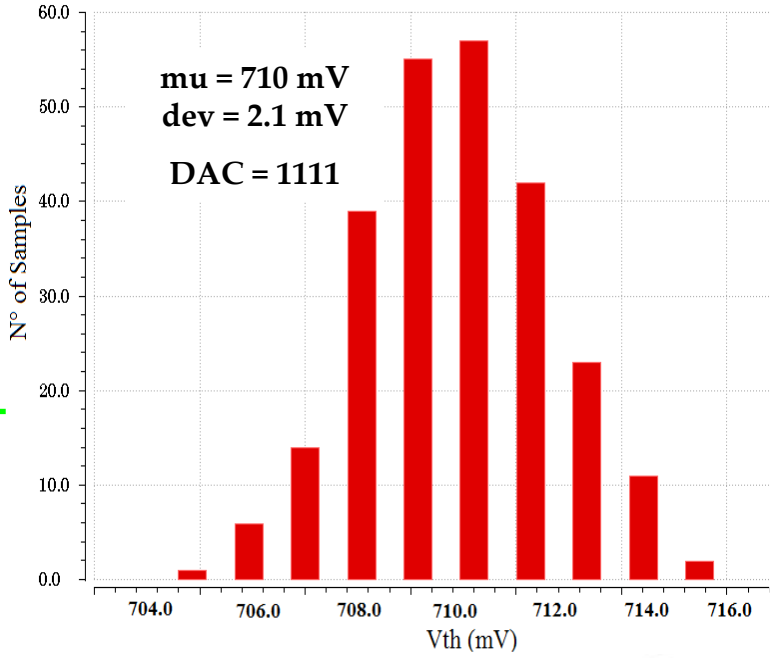
Thank you for your attention!

Tuning simulation

- The voltage reference must be HIGHER than the Vth
- The dinamic voltage (40 mV) allows to correct the worst value

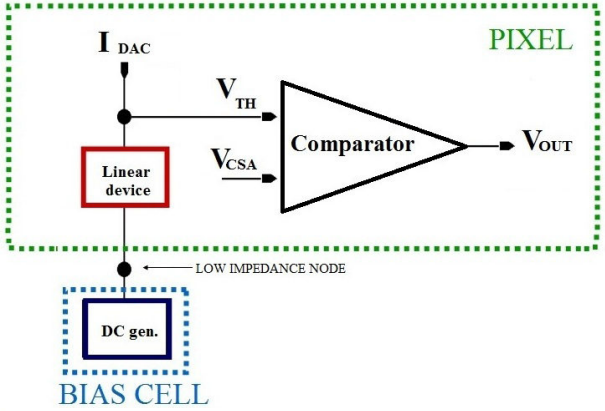


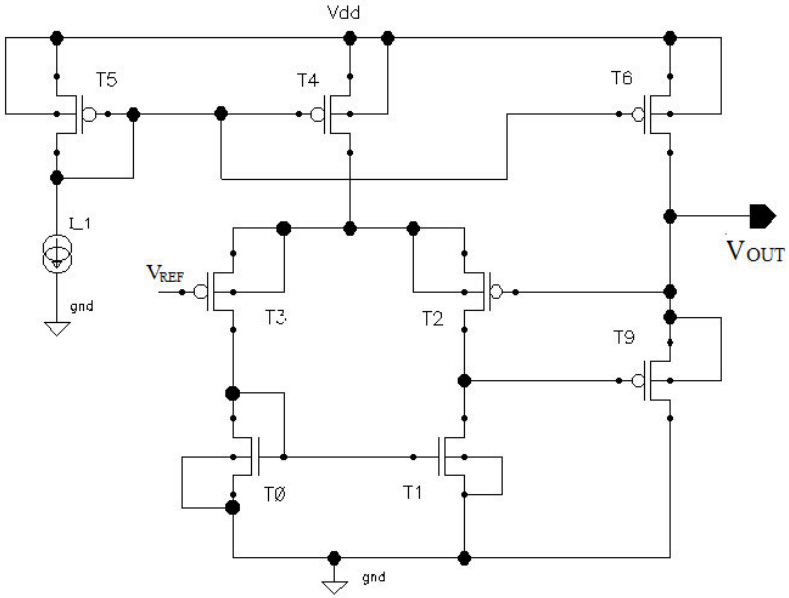




Other solutions studied

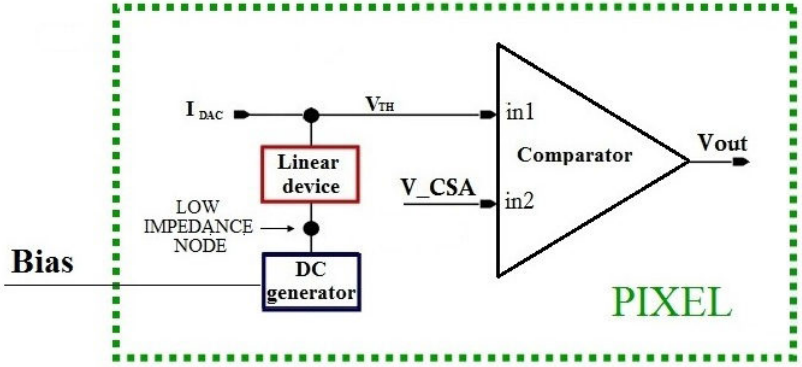
Solution A

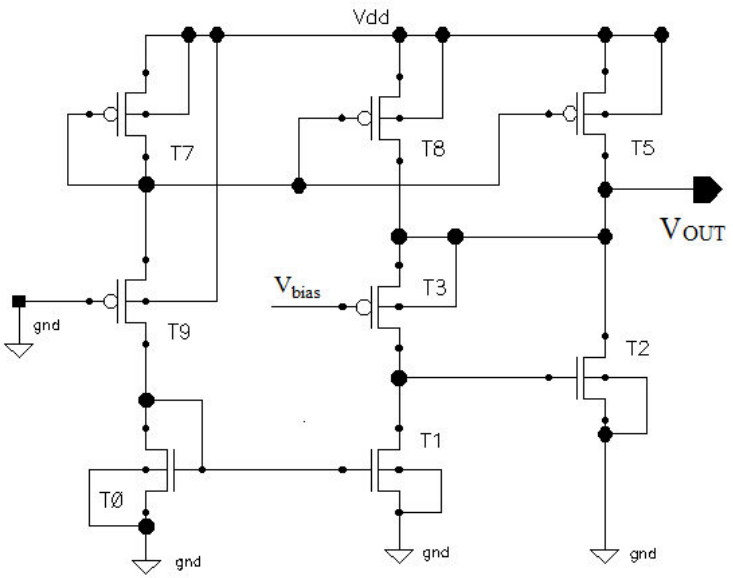




DC: generator 1

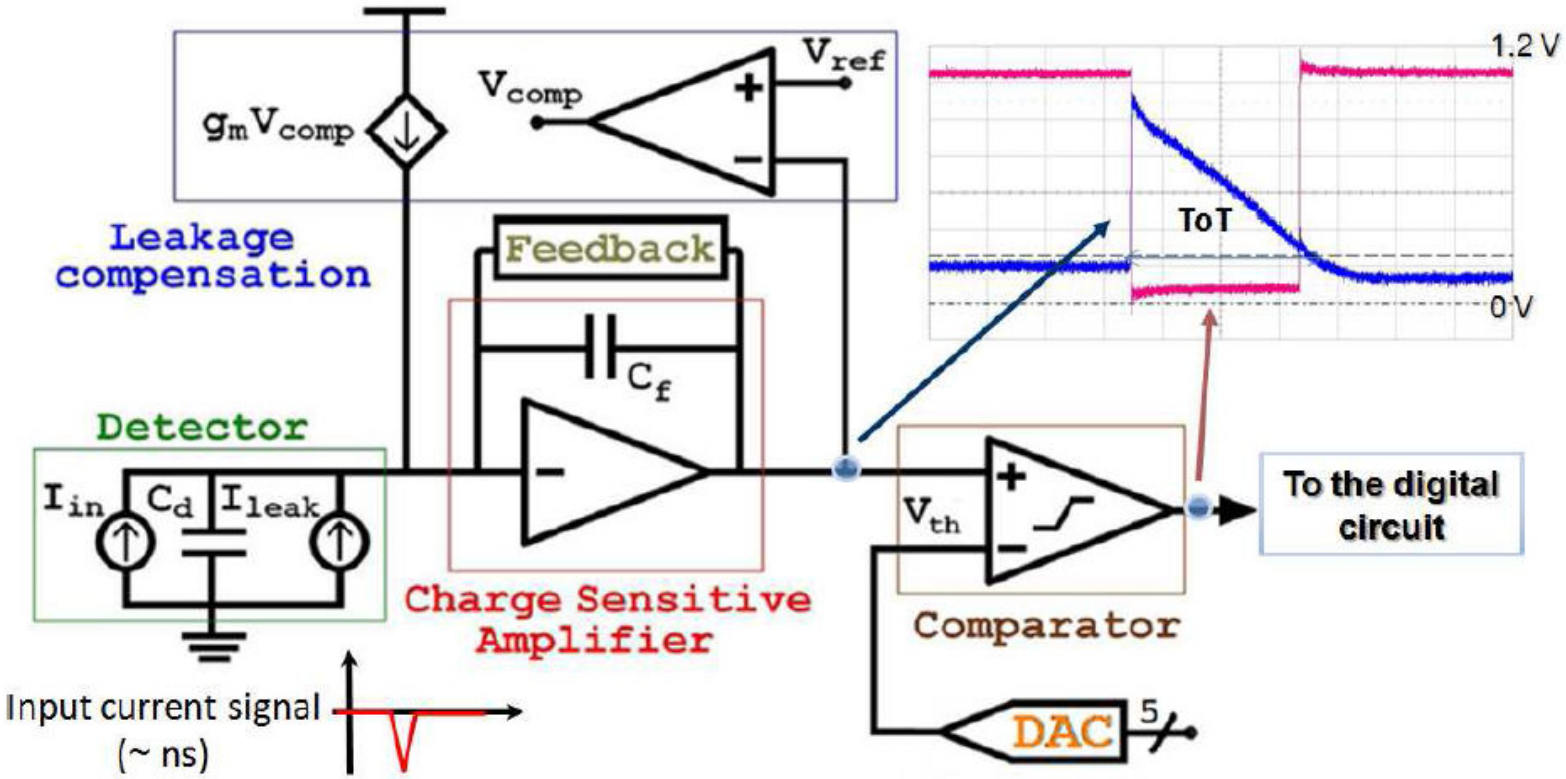
Solution B



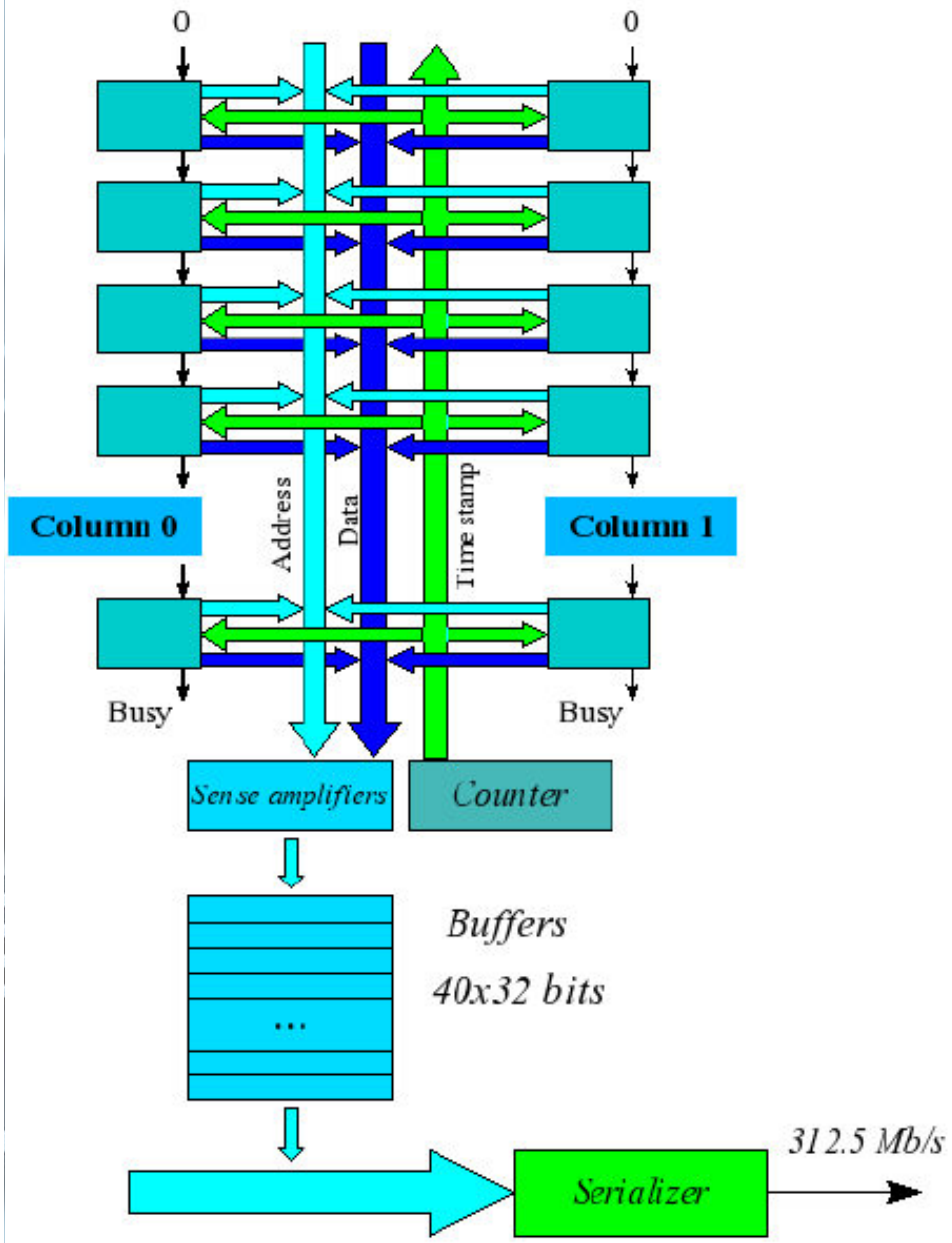


DC: generator 2

The analogue pixel Architecture



The ASIC for Hybrid Pixel Detectors



Measurements	Hit position Energy loss Time
Pixel Size	100 µm x 100 µm
Time/charge digitization	At pixel level
ASIC Size	Fixed by the pixel size
Input Polarity	Selectable

System Clock	155.52 MHz
Time resolution	<10 ns
Trigger	Self triggering
Power Consumption	< 20 µW
Noise Level	200 e^- rms
Linear dynamic range	Up to 50 fC