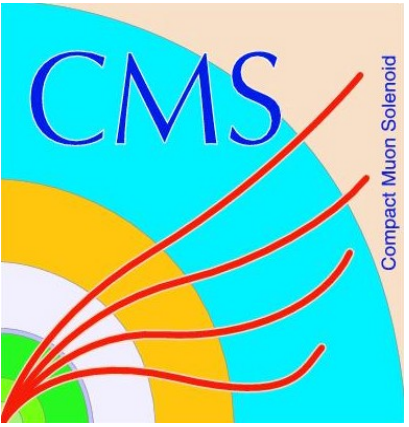


Front-End Amplifiers in 65nm CMOS technology for the upgrade of the pixel detector of the CMS experiment

***Candidate*: Monteil Ennio**

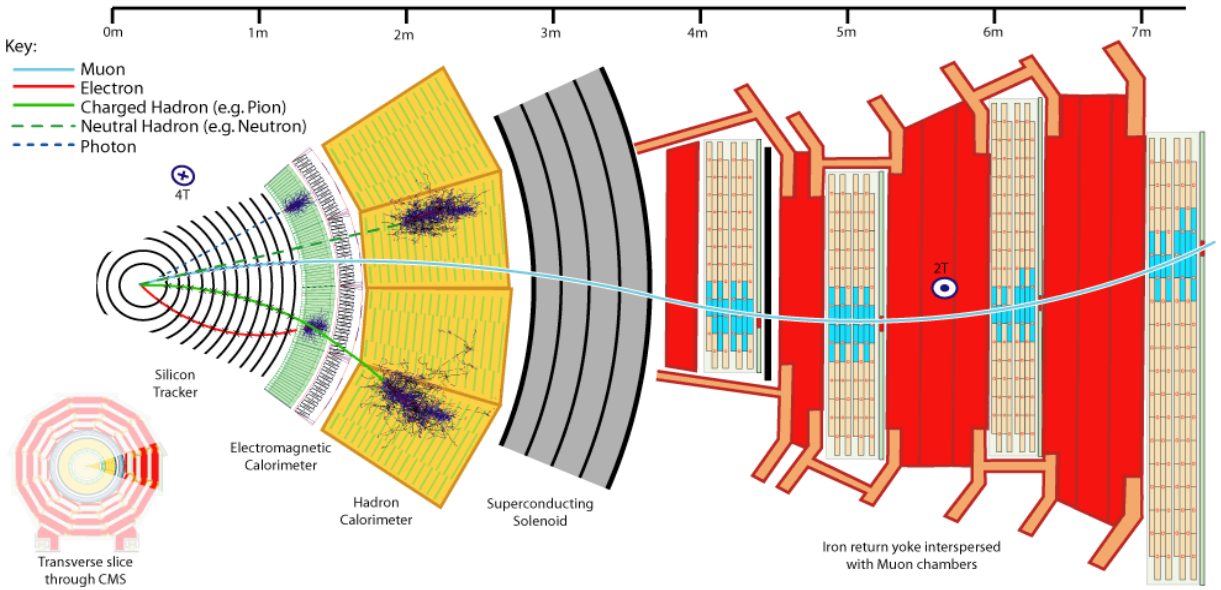
***Supervisor:* Prof. Angelo Rivetti**

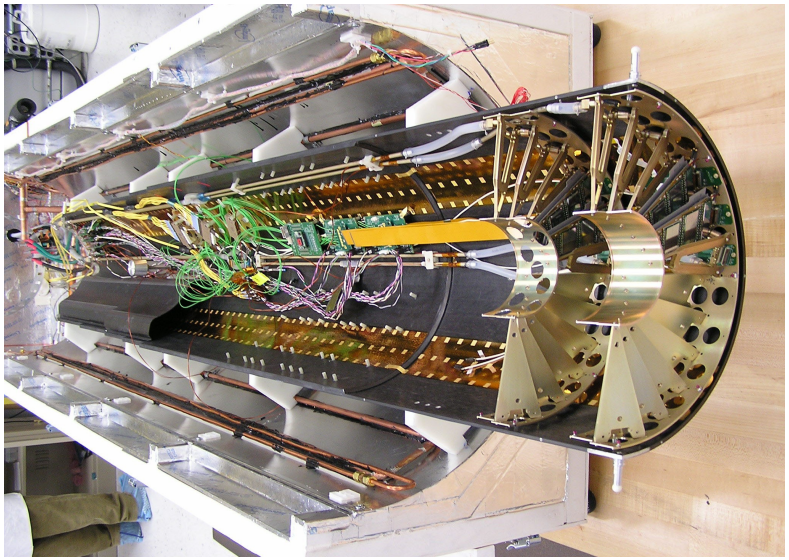
Torino, October 9, 2013

Outline

- CMS pixel detector upgrade plans
- Analog design in 65nm CMOS technology
- Front-End architectures
- Noise optimization
- Feedback implementation
- Summary and outlook

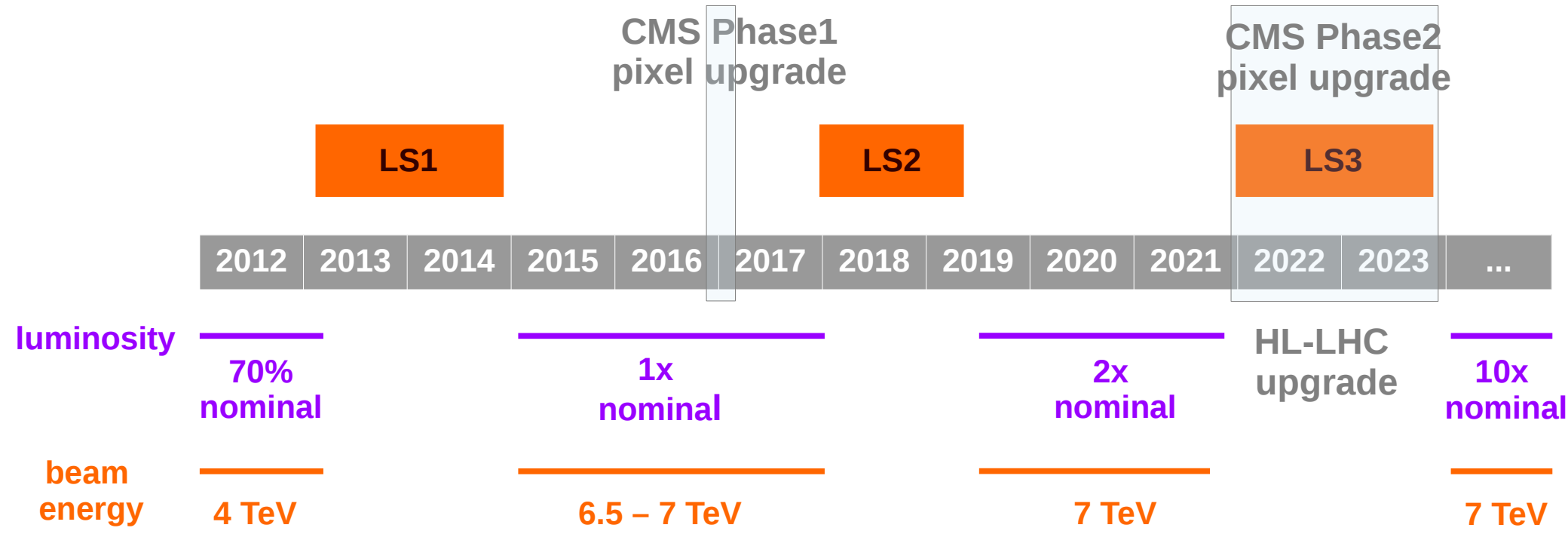
CMS Silicon Pixel Detector





- 3 barrel layers (BPIX) + 2 disks each side (FPIX)
- R = 4.4 cm, 7.3 cm and 10.2 cm, $|\eta| < 2.5$, ~ 1 m^2, 66 Mpixels

LHC timeline



- **nominal** luminosity → 10^{34} cm^{-2} s^{-1}, 23 fb^{-1} per year in 2012
- HL-LHC upgrade → 10^{35} cm^{-2} s^{-1}, foreseen 300-500 fb^{-1} per year
  - unprecedented **Pile-Up (PU) conditions**
  - unprecedented **radiation levels**

Phase2 Pixel Upgrade - motivations

PARAMETER or FEATURE	1st generation LHC phase 0	2nd generation LHC Phase 1	3rd generation LHC Phase 2
Max Particle Flux	~50 MHz/cm^2	~200 MHz/cm^2	~500 MHz/cm^2
Max Pixel Flux	200 MHz/cm^2	600 MHz/cm^2	2 GHz/cm^2
Rad. Hardness	1.5 MGy	3.5 MGy	10 MGy
Pixel Dimension	100x150 mm^2 50x400 mm^2	100x150 mm^2 50x250 mm^2	25x150 mm^2 50x100 mm^2
Signal Threshold	2500-3000 e$^-$	1500-2000 e$^-$	~1000 e$^-$
L1 Trigger Latency	2-3 us	4-6 us	6-20 us
Power Budget	~0.3 W/cm^2	~0.3 W/cm^2	<0.4 W/cm^2
Electronics technology node	250nm CMOS	250nm CMOS (CMS) 130nm CMOS (ATLAS)	65nm CMOS

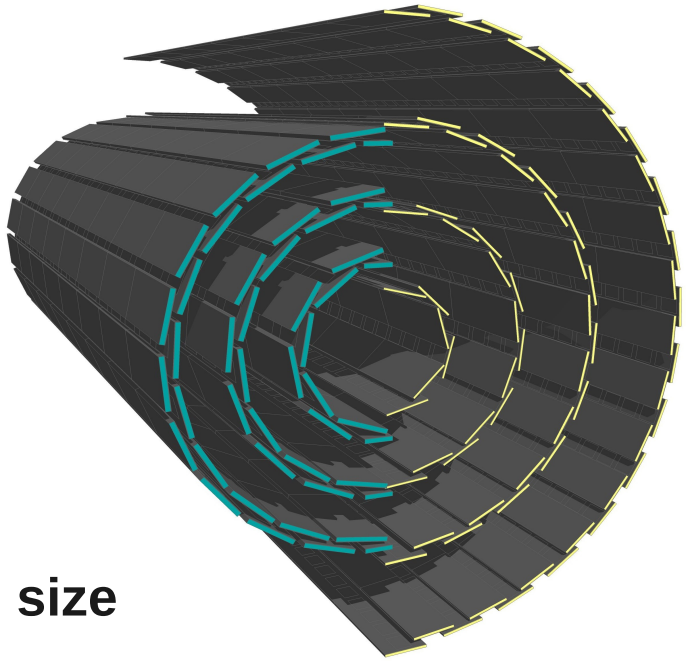
- **HL-LHC upgrade** will introduce unprecedented operating conditions

- We want to maintain or improve **tracking performance** in terms of:
  - spatial resolution and tracks separation → reduced **pixel size**
  - hit efficiency > 99.9% → reduce the data loss

→ ***design of a new pixel readout chip required !***

Phase2 Pixel Detector

- CMS **Phase1** pixel detector (end of 2016)
  - BPIX: 3 → 4 layers
  - FPIX: 2 → 4 disks
  - pixel ASIC (ROC): PSI46 → PSI46DIG



- CMS **Phase2** pixel detector (~2022)
  - **geometry** similar to Phase1 (4 barrel layers)
  - possible extension in the disk part
  - improvement in **granularity** → reduced **pixel size**
  - **new pixel ASIC** !
  - **thinner sensors** to increase radiation tolerance

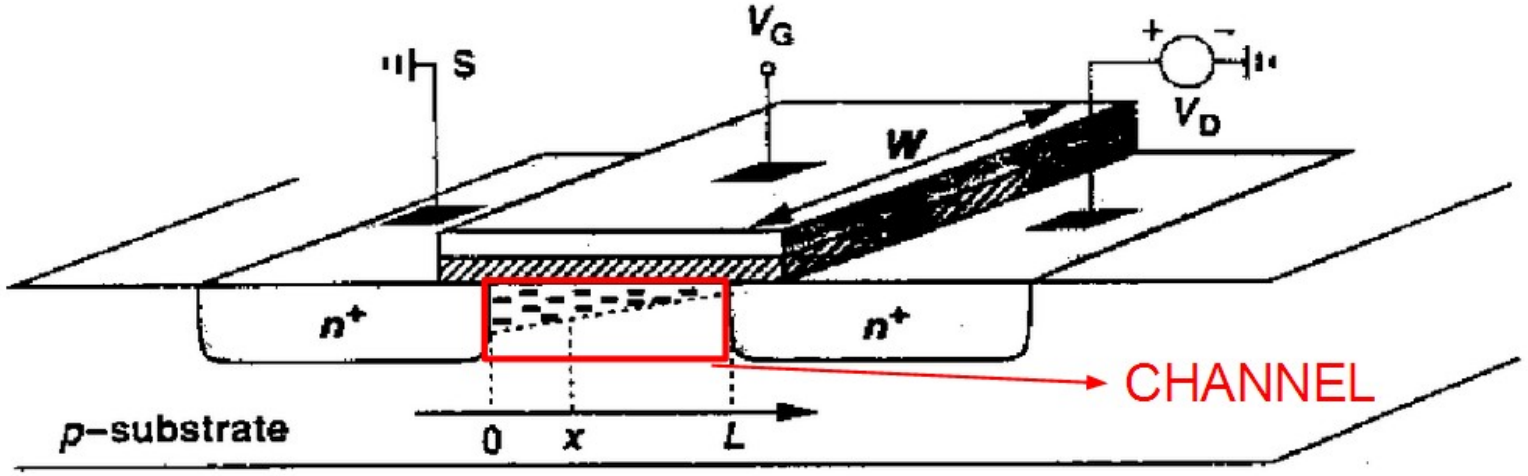
- **sensor choice** not yet finalized
  - Very likely planar silicon sensors in the outer layers 3 and 4
  - Ongoing studies for layers 1 and 2 (**planar sensors? 3D sensors?**)

RD on 65nm technology

- Electronics requirements:
  - **speed**, **low-noise, low-power consumption, rad. tolerance**
  - more on-chip intelligence and local data storage capabilities
  - **sensor-independent** front-end electronics

- why 65nm ?
  - demonstrated to be **radiation tolerant** up to 2 MGy, better than 130nm (to be confirmed up to 10MGy)
  - higher integration density
  - improved speed
  - low power (1.2V supply)
  - mature technology (introduced ~10years ago, long term availability)

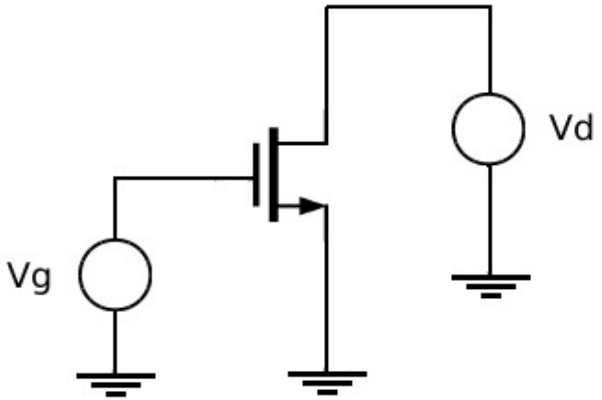
CMOS submicron technologies

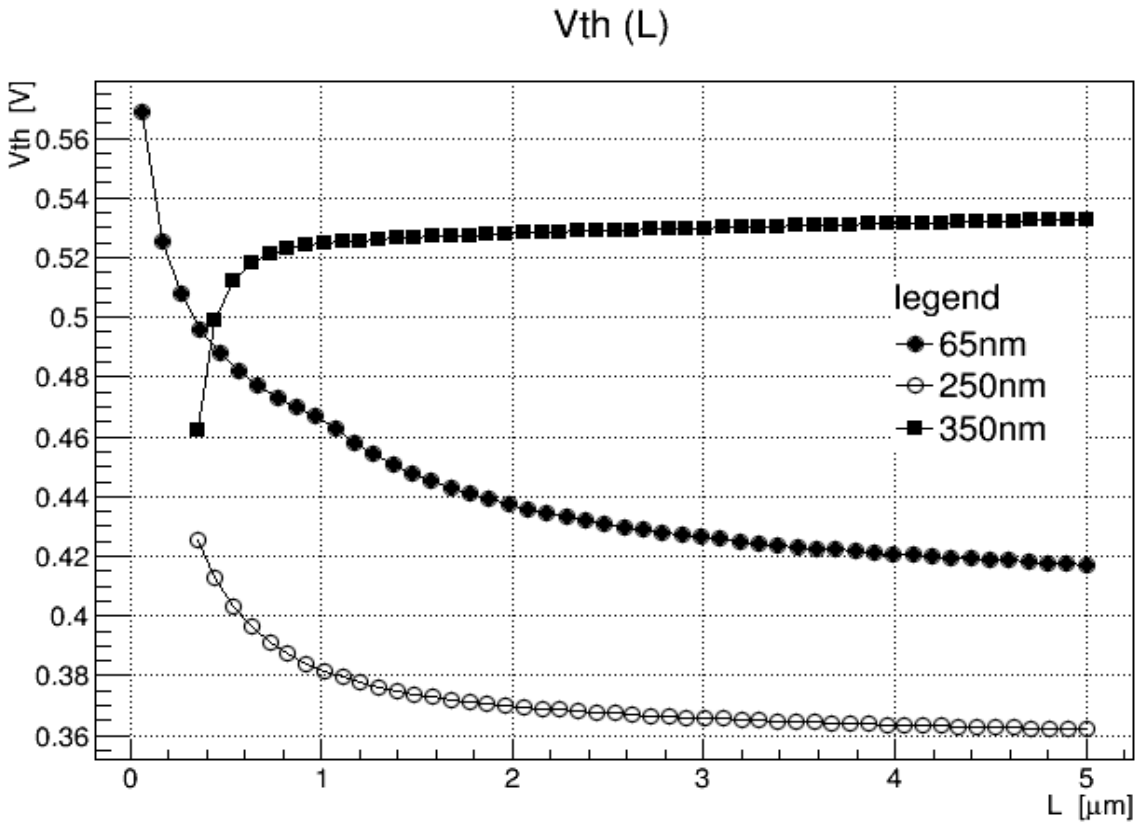


- **Short channel effects** degrade analog performances
  - Threshold voltage variation with Vgs,L
  - Output impedance variation

- Usually $\mathbf{L_{min}}$ **is not used** due to
  - Increased noise effects
  - Low output resistance

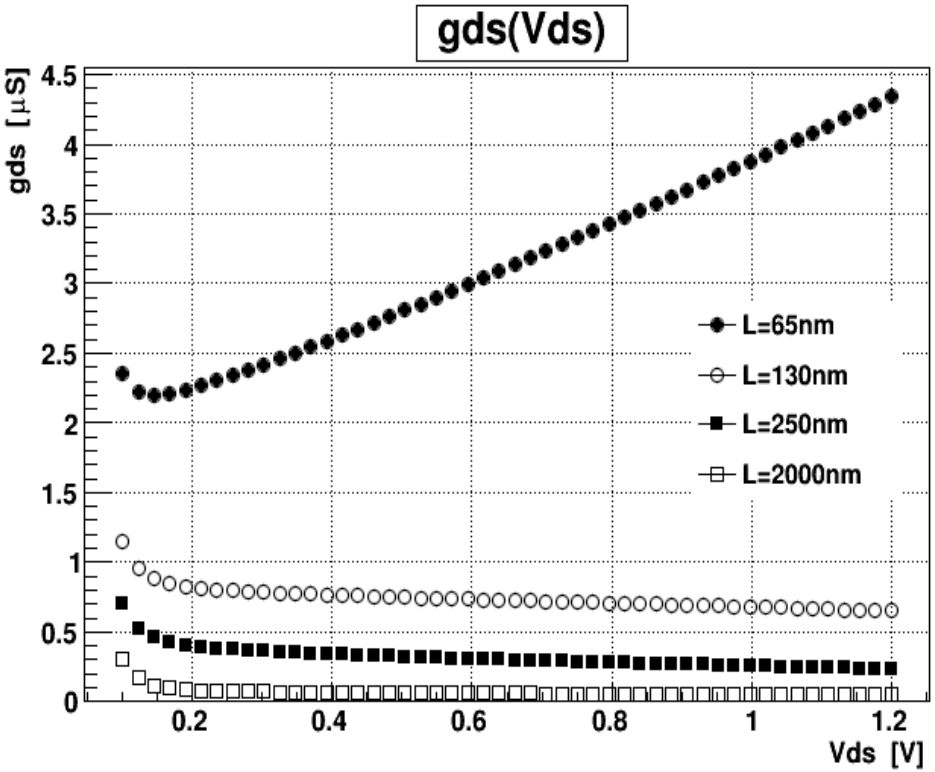
Threshold voltage



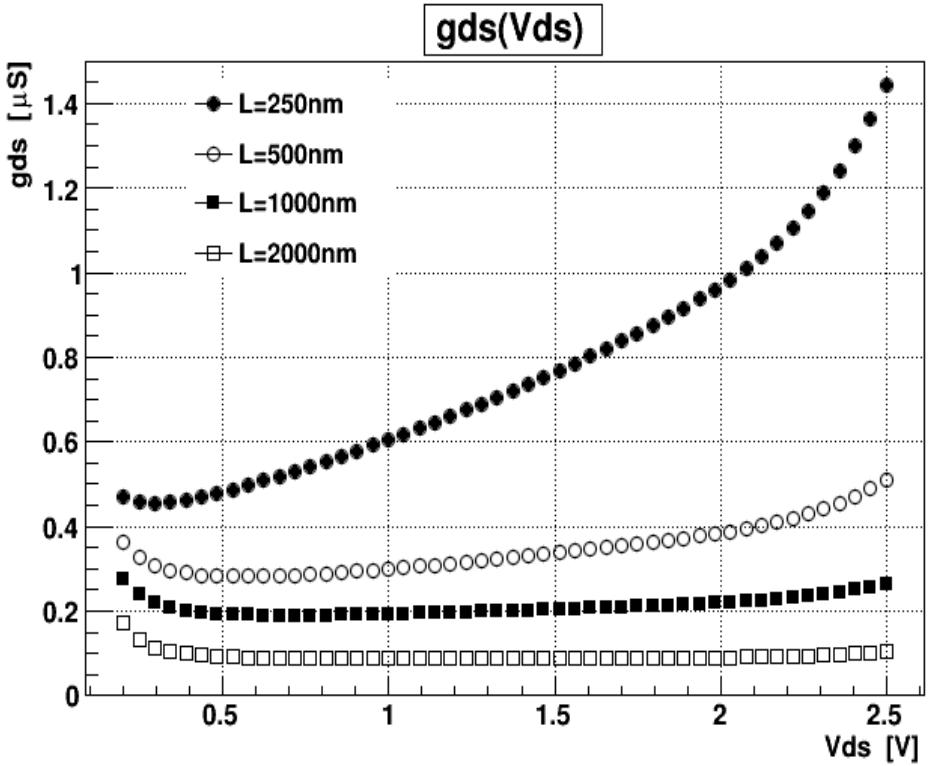


- Very different trend between 350nm technology and the others due to **halo doping**

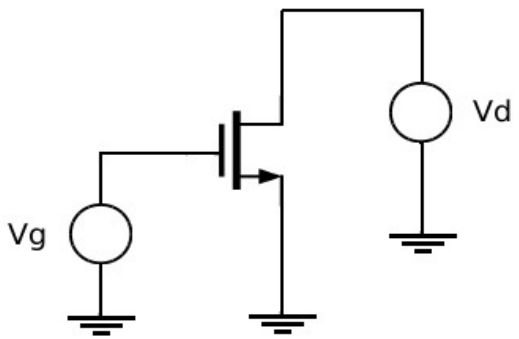
Output conductance



65 nm CMOS technology



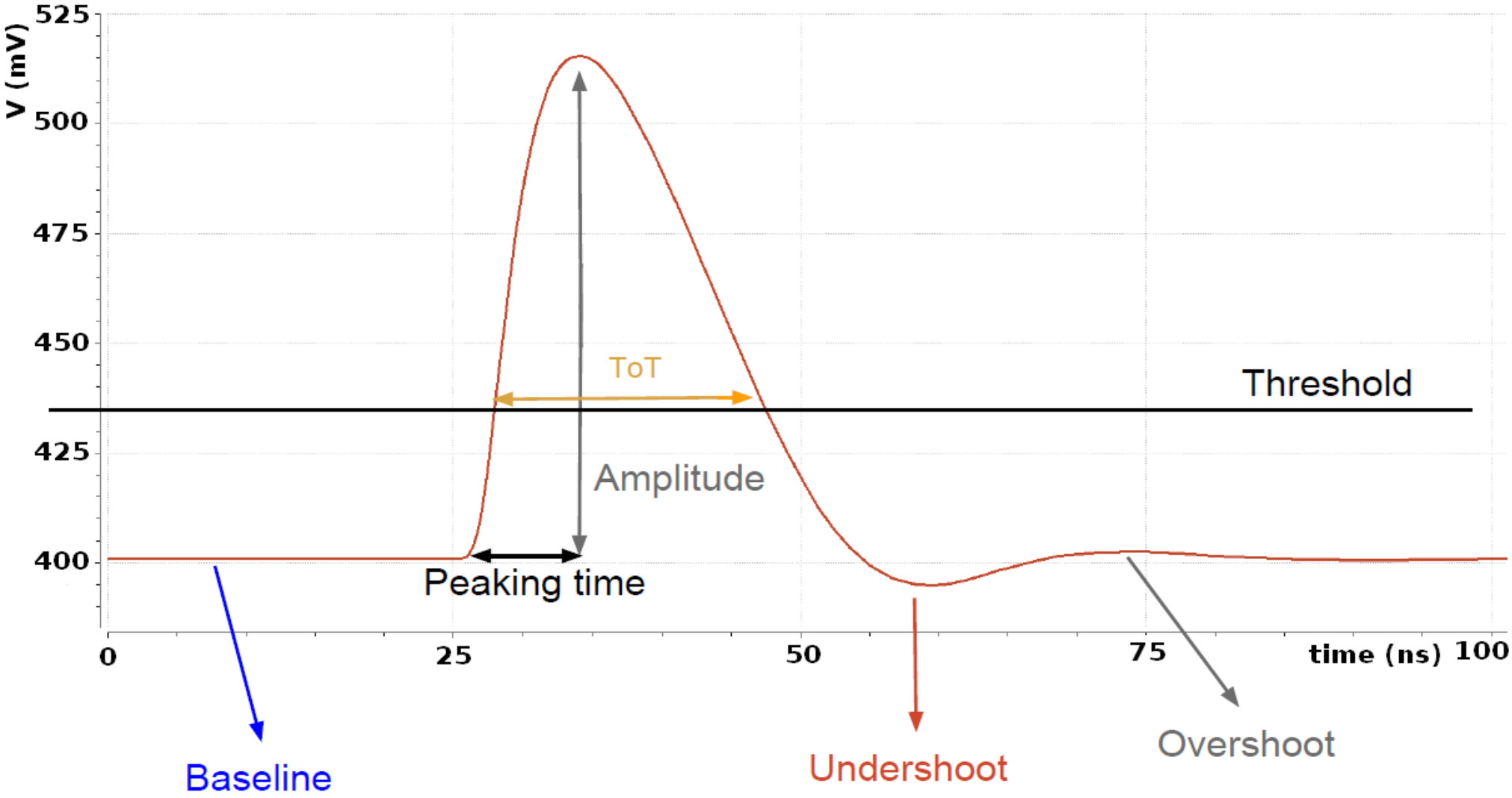
250 nm CMOS technology



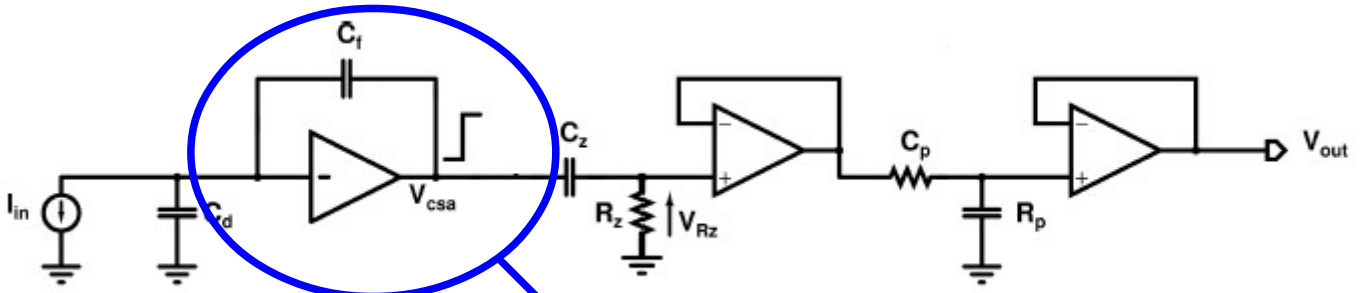
L_{min} → Very different behavior

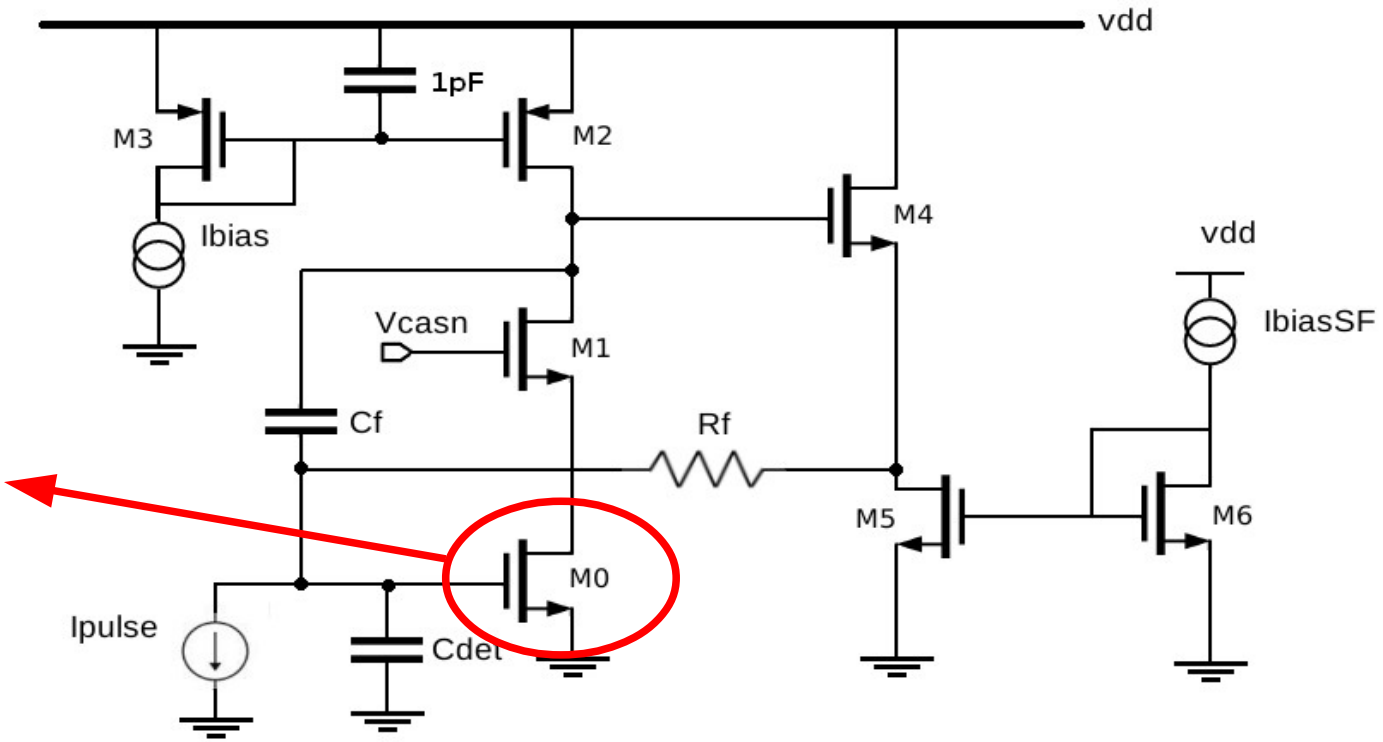
usually not chosen

Output signal



Charge Sensitive Amplifier





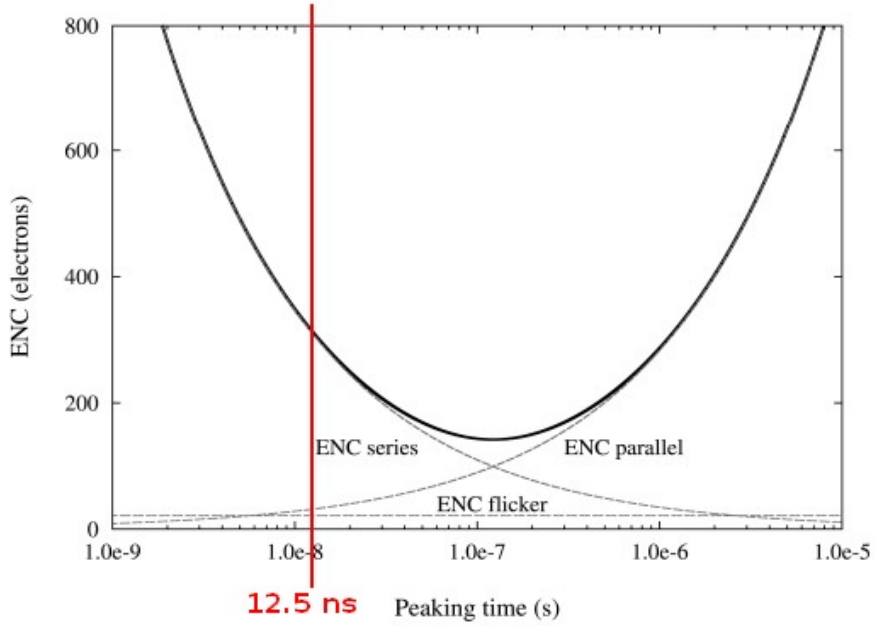
INPUT TRANSISTOR

CSA noise analysis

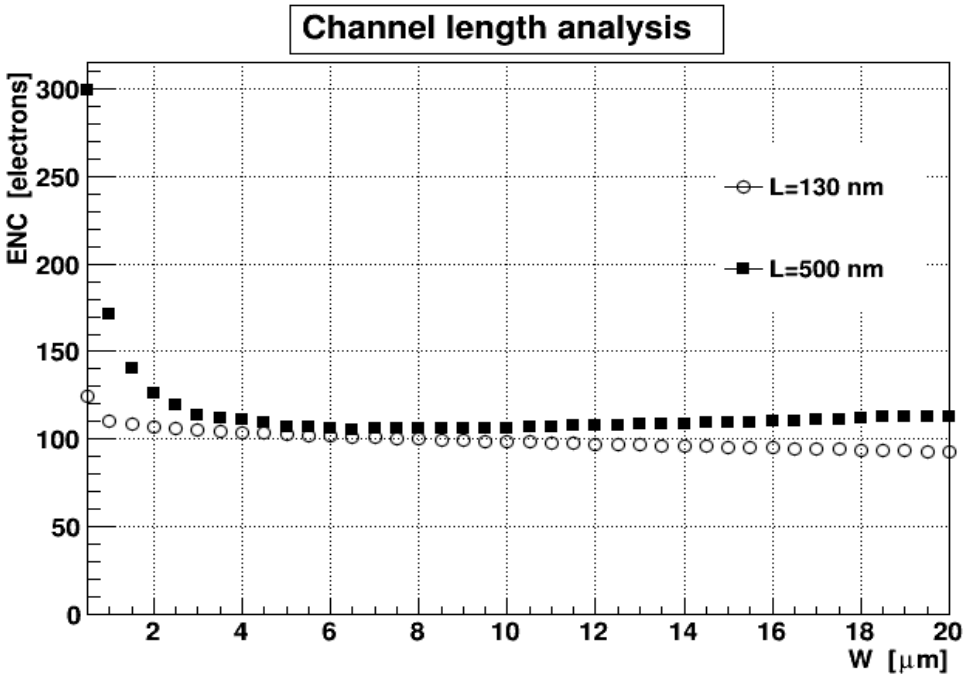
- Crucial to have the best **SNR (Signal to Noise Ratio)**
- Expressed in ENC (Equivalent Noise Charge in units of electron charge)

$$ENC = \frac{1}{q_e}\frac{1}{Gain}\sqrt{\int_{f_{min}}^{f_{max}} df \quad \frac{d < v_n^2 >}{df}\Big|_{out}}$$

- Main noise sources:
  - **Series noise** $\propto C_{tot}$, $\frac{1}{\sqrt{T_{peak}}}$
  - **Parallel noise** $\propto \sqrt{T_{peak}}$
  - **Flicker noise** $\propto \frac{1}{f}$



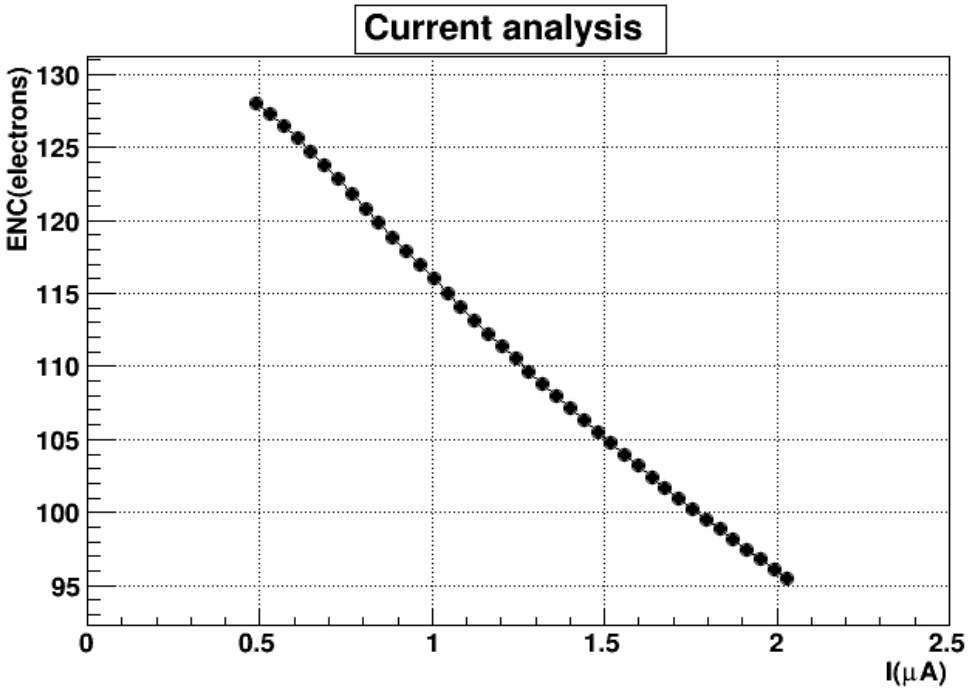
CSA noise analysis



Constraints:

- Peaking time T_p = 12.5 ns
- $C_{detector}$ = 100 fF
- I = 1.6 uA

Noise increases with the channel length

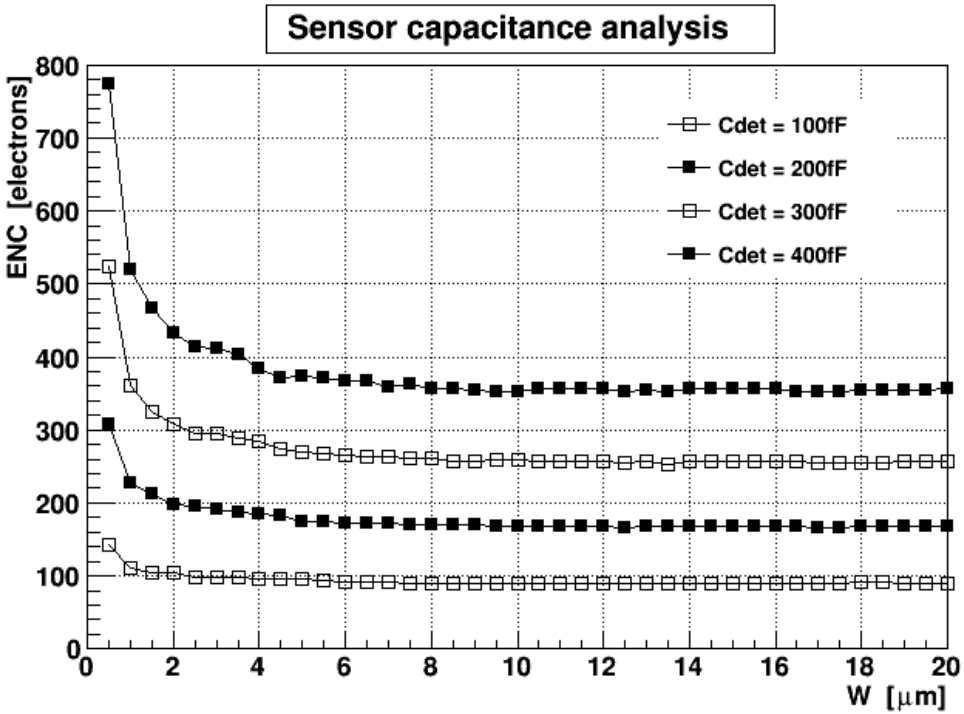


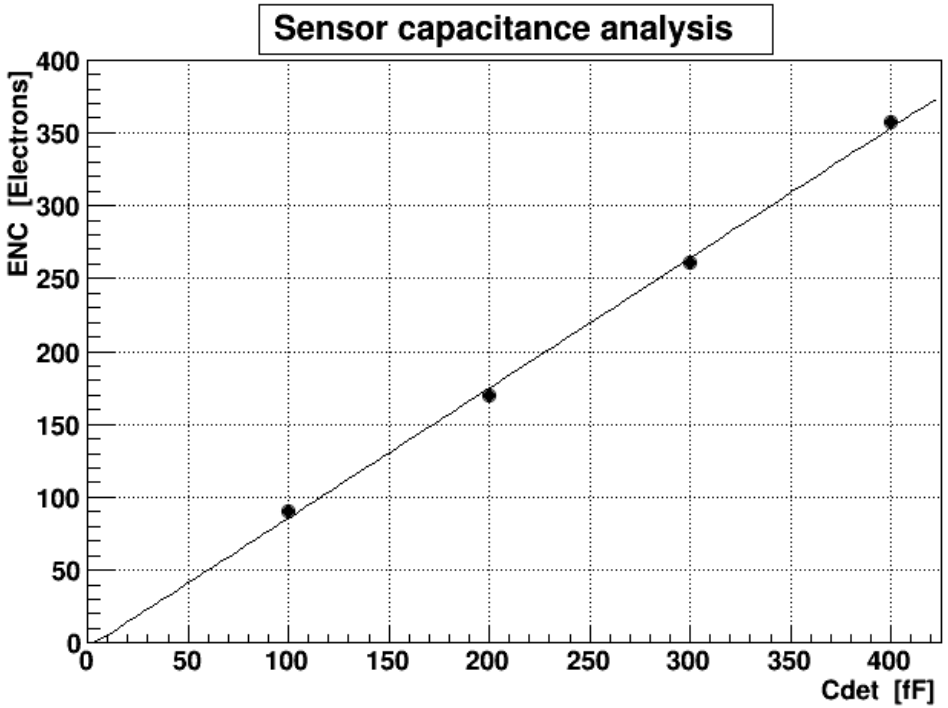
Constraints:

- W = 8um, L = 130 nm
- Peaking time T_p = 12.5 ns
- $C_{detector}$ = 100 fF

Noise increases reducing power consumption

CSA noise analysis





Constraints:

- Peaking time T_p = 12.5 ns
- L = 130 nm
- I = 1.6 uA

ENC **linearly dependent** on sensor capacitance

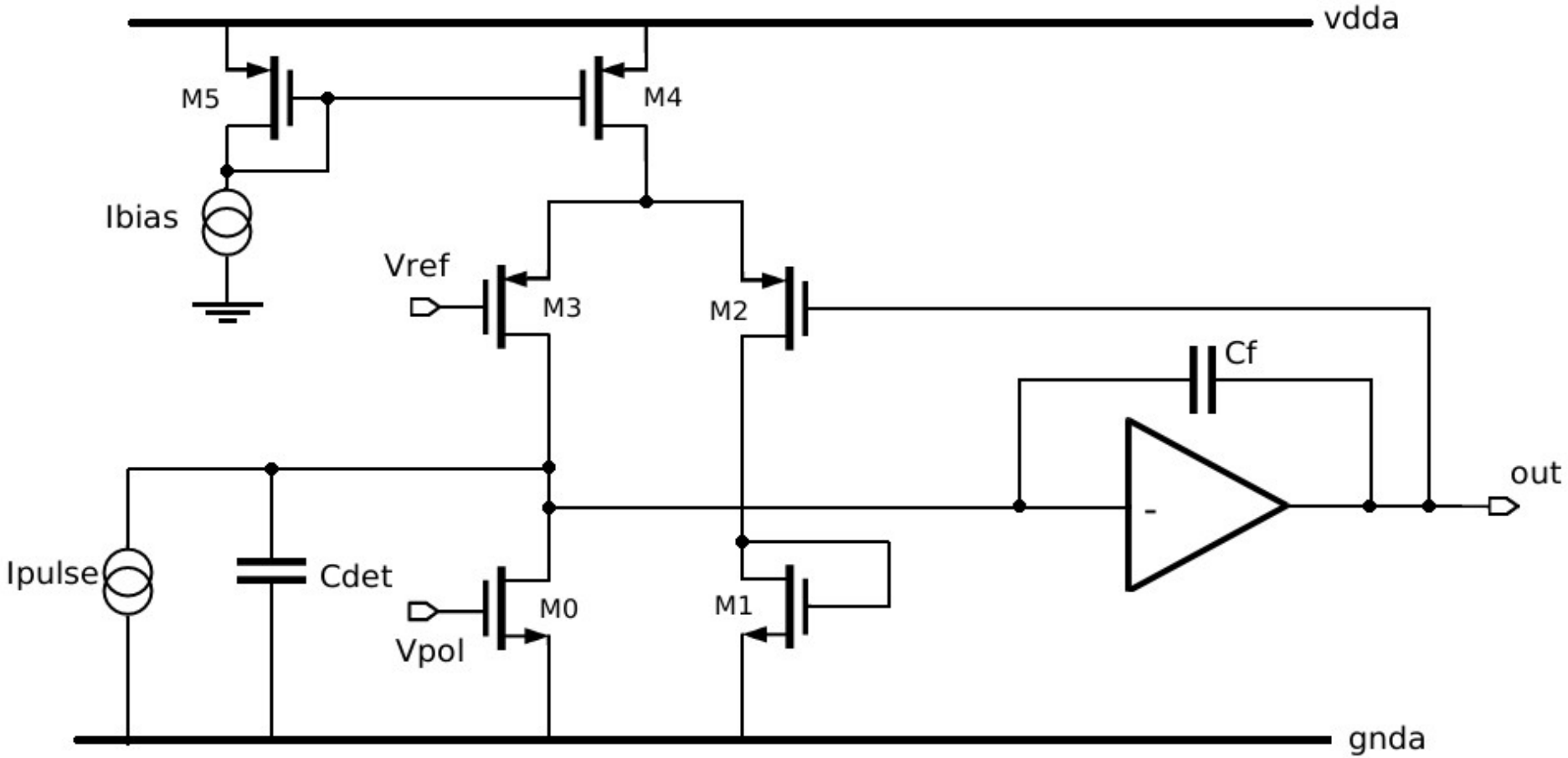
Studied architectures

- Passive resistors are not used in the real implementation of Integrated Circuits

- Two different **feedback network** implementations compared
  - Power consumption
  - Linearity
  - Noise
  - Mismatch effects

- **Time-variant Charge Sensitive Amplifier**

Feedback implementation



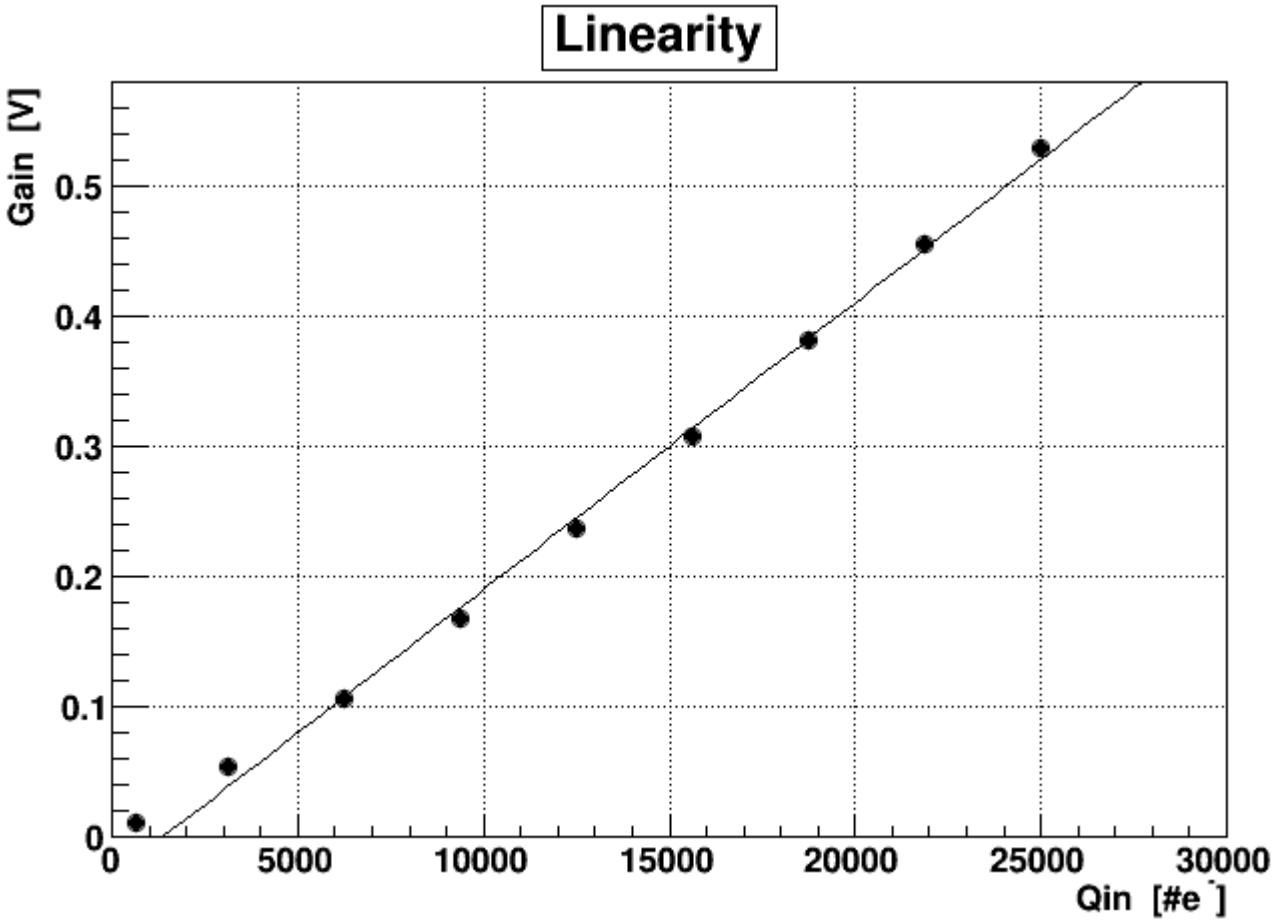
- Total stage power consumption 2 µW

Linearity

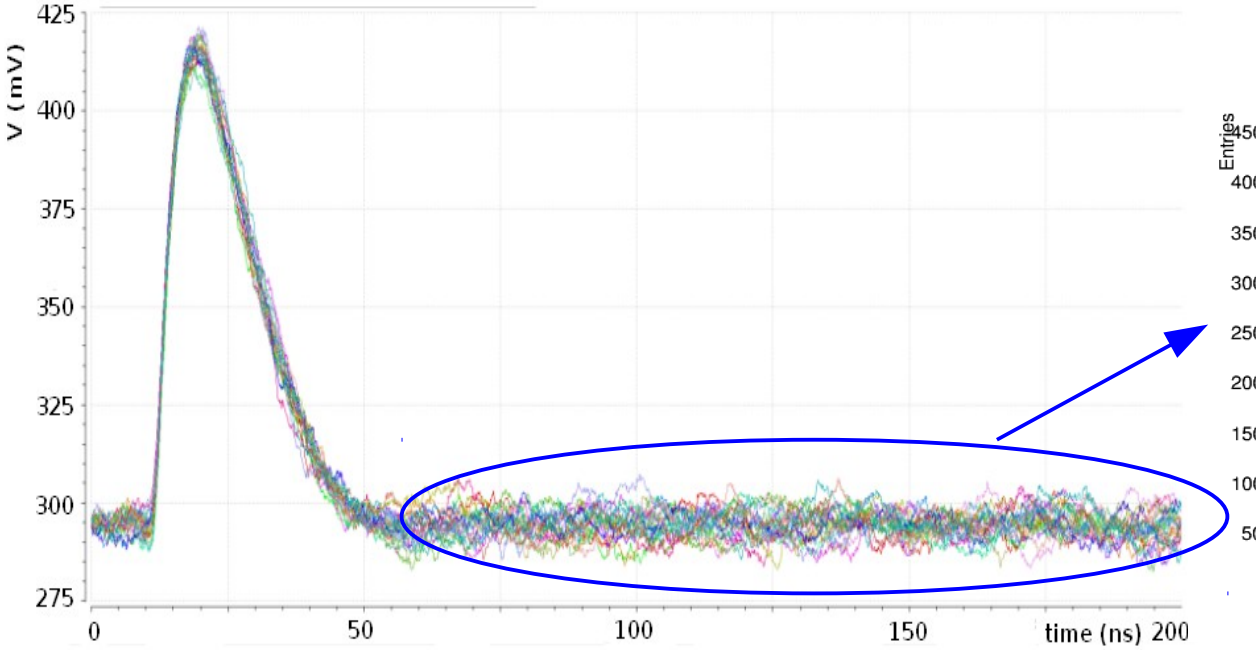
MIP produces ~ 100 e-/h pairs per μm of silicon on average

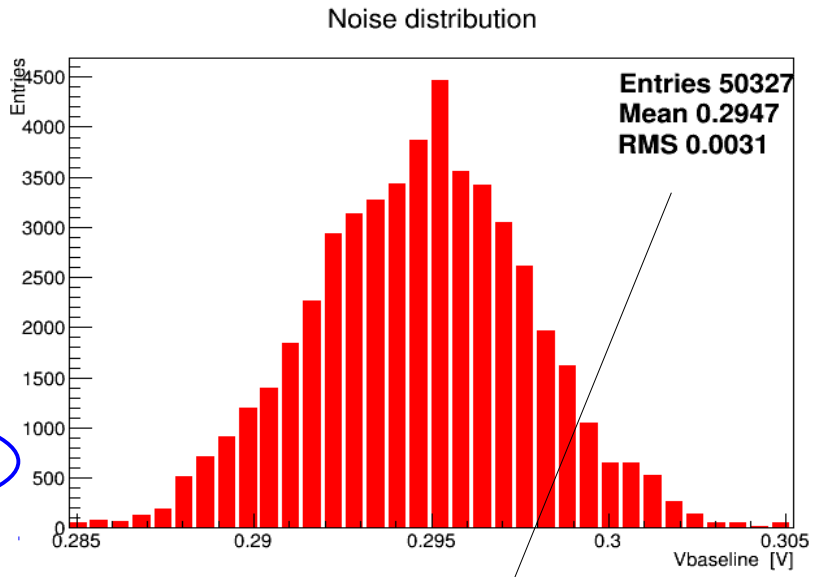
Pixel thickness ~ 100 μm

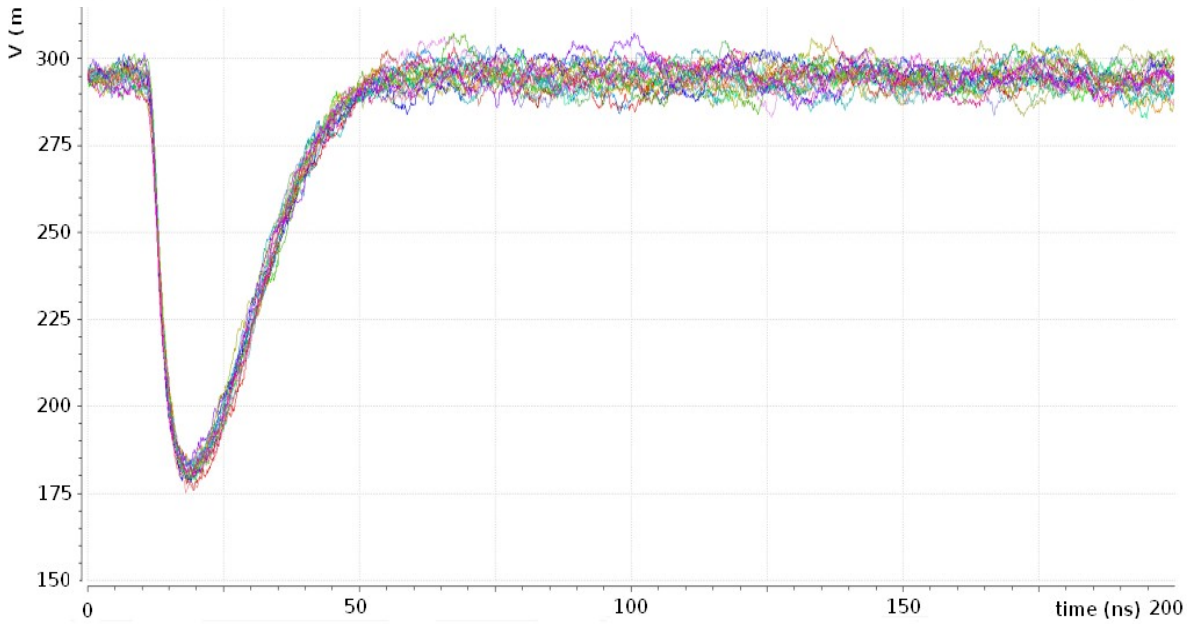
Average signal ~ 10000 e-



Transient noise







RMS ~ 3 mV ~ 180 e-

Threshold = 15 mV ~ 900 e-

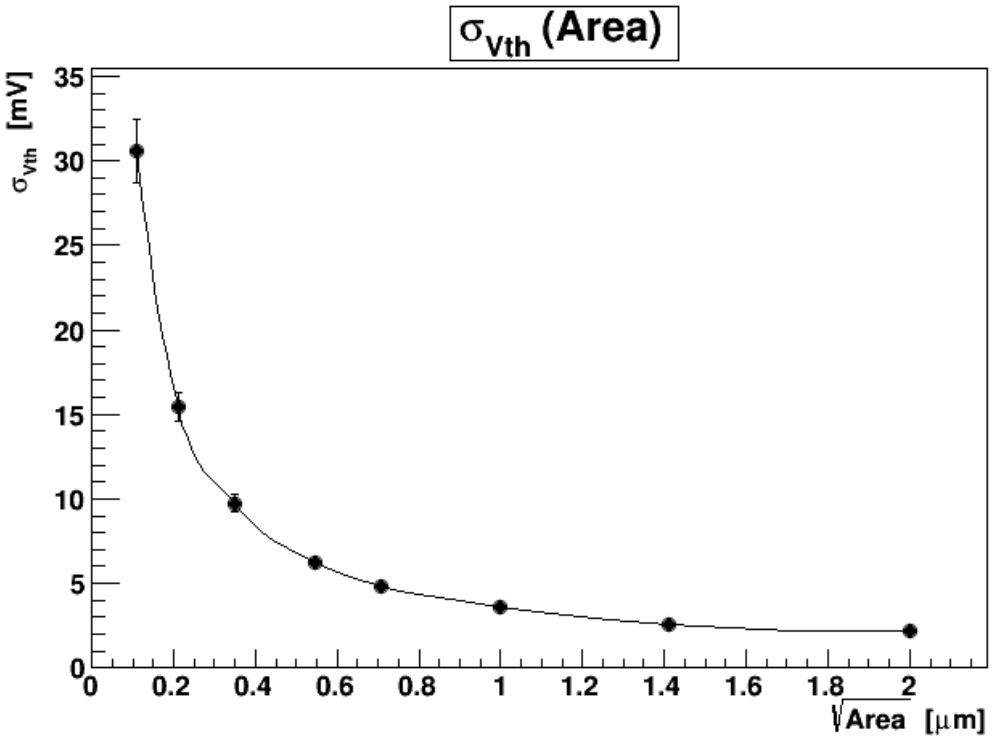
Mismatch simulation

- **Mismatch**: transistors with identical design have electrical parameters fluctuations

- **Manufacturing fluctuations**:
  - Dopant concentrations
  - Oxide thickness

$$\sigma \propto \frac{1}{\sqrt{WL}}$$

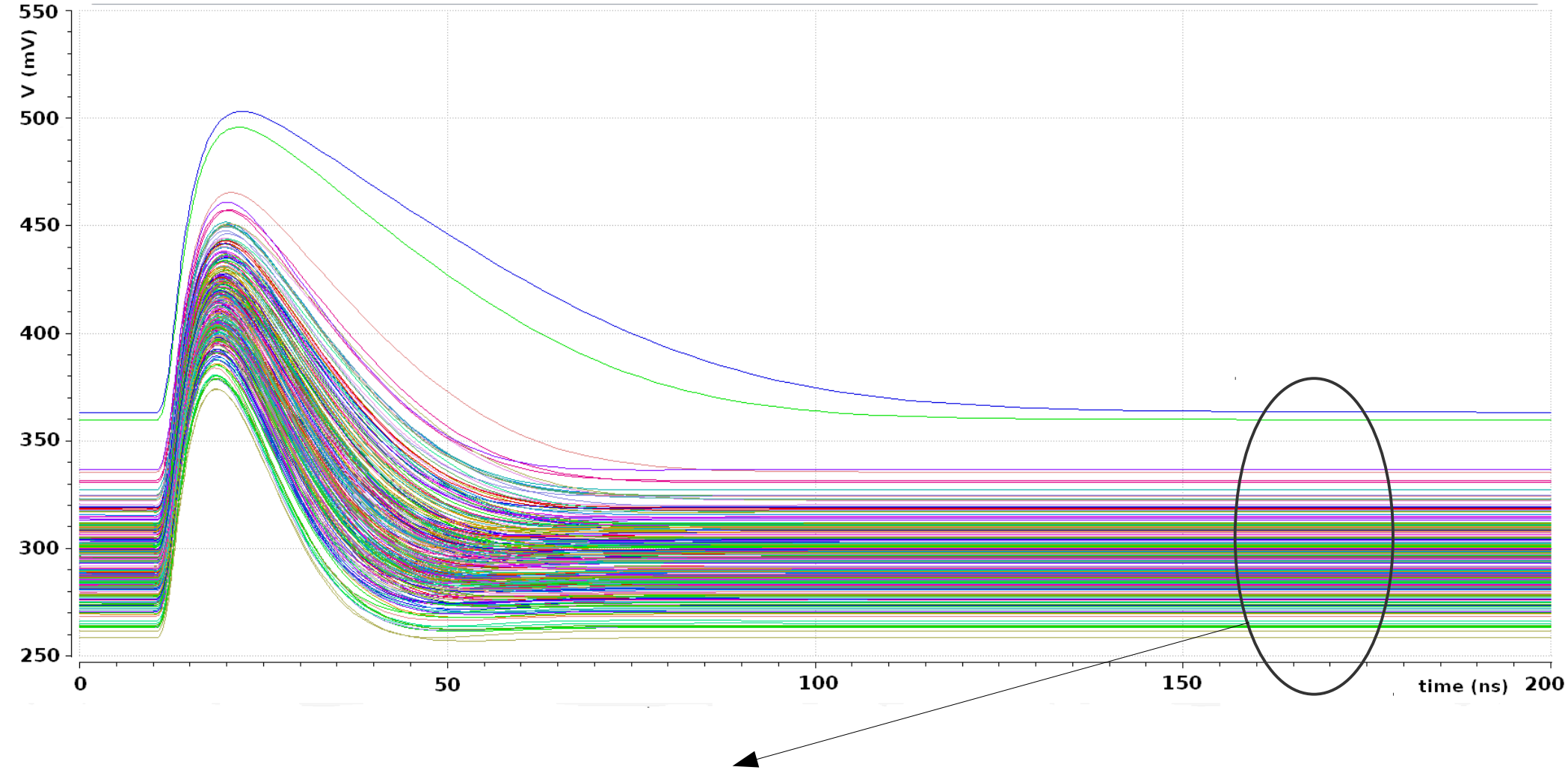
Mismatch simulation in 65 nm



- **Monte Carlo mismatch analysis**:

  Single transistor parameters extracted from their distributions

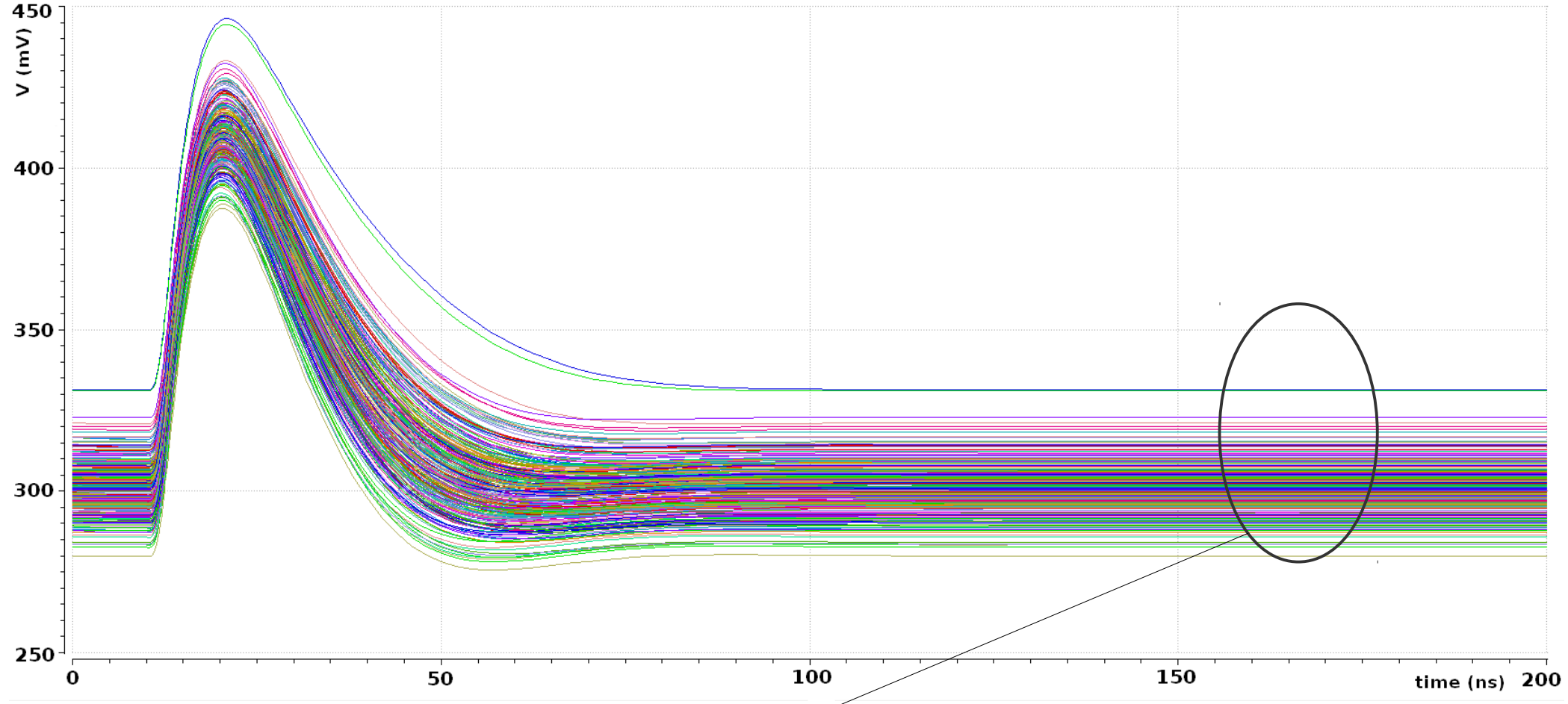
Mismatch simulation



- Huge **baseline fluctuations**

Mismatch simulation

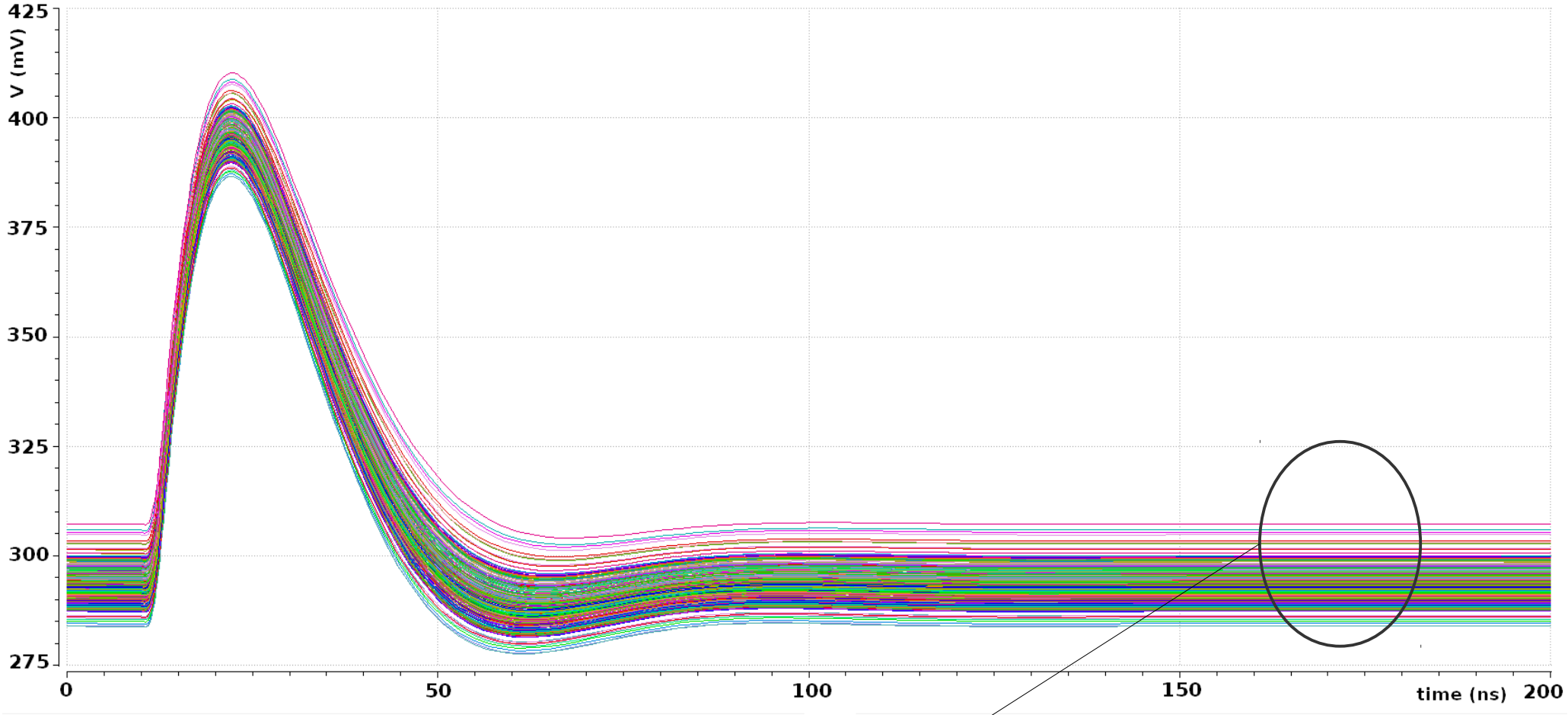
- Doubled W,L values



- **Reduced** mismatch effects

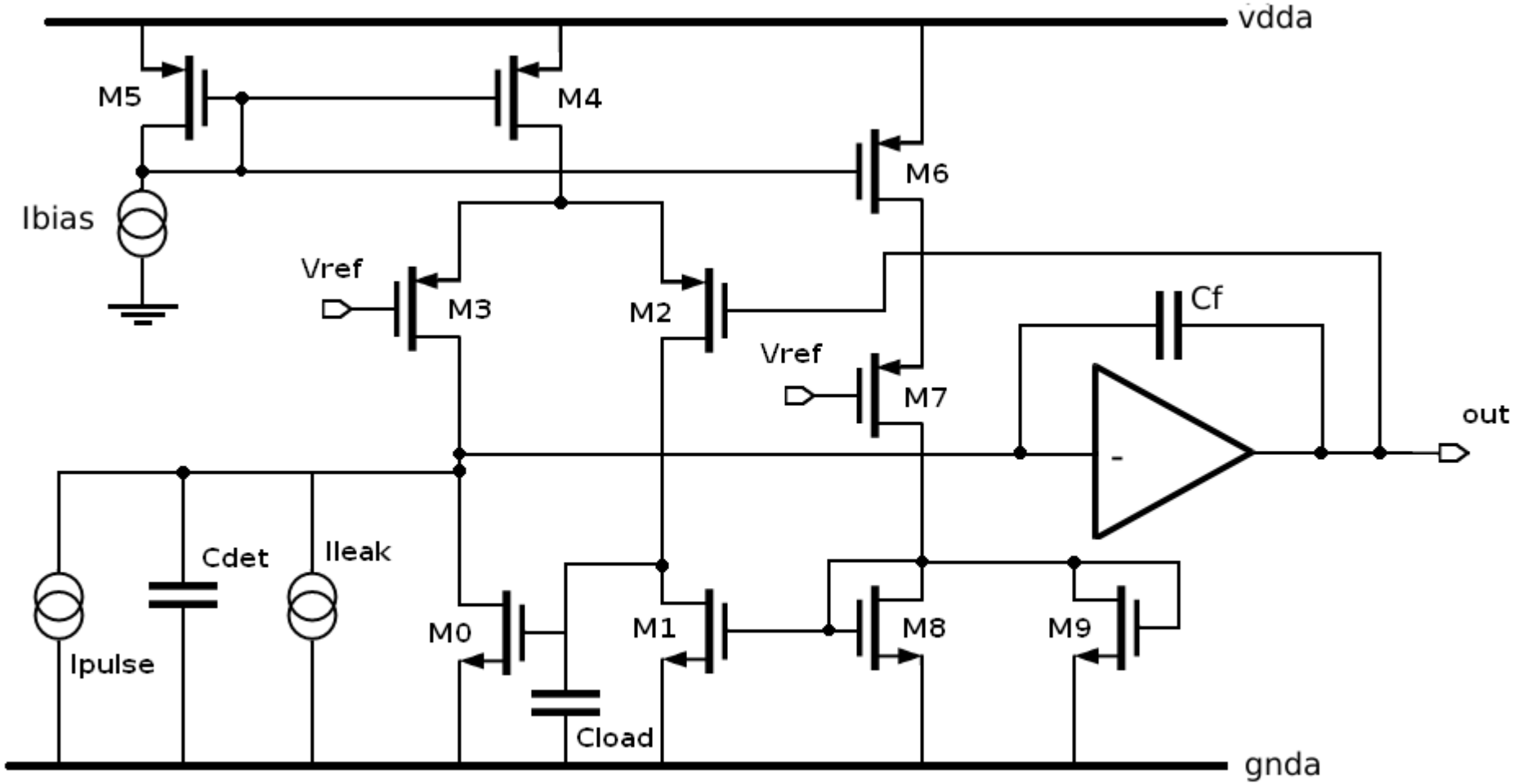
Mismatch simulation

- Further optimization



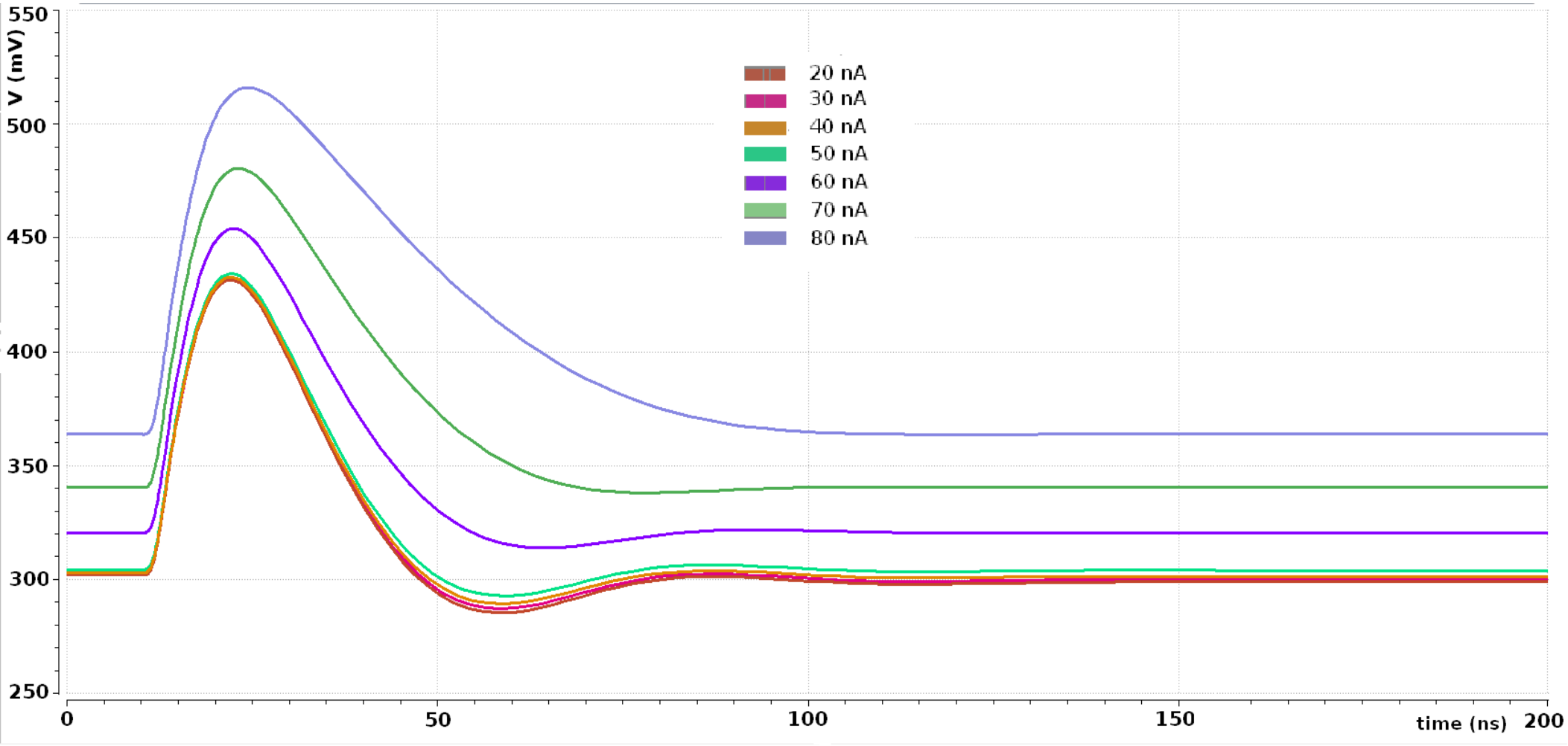
- Mismatch effects more than halved

Leakage compensation



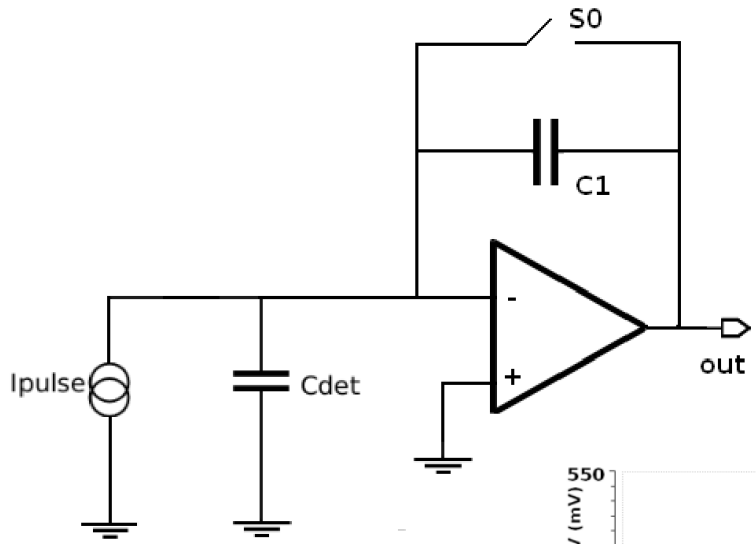
- Leakage current compensated up to 50 nA

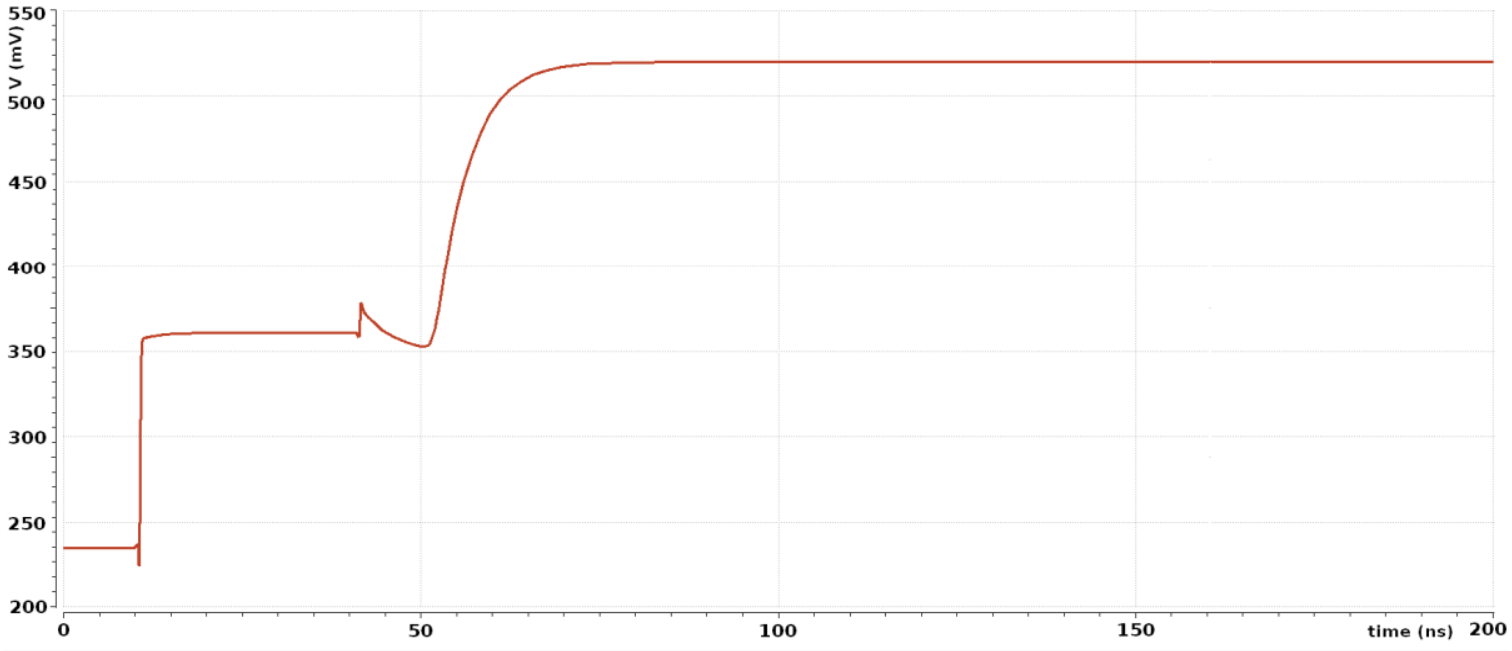
Leakage compensation



- Leakage current compensated up to 50 nA

Time-variant CSA





- Signal rise time consistent with requirements

Conclusions

- **Similarities** in terms of:
  - Power consumption (~ 2 μW)
  - Noise
- **Differences** in terms of:
  - Mismatch effects
  - Leakage compensation
- **Time variant Charge Sensitive Amplifier** is again a suitable choice
- In principle all these architectures can be used in the upgrade

Next steps

- Realization of the **layout** of these architectures
  - Estimation of the area occupation

- Analyze more in detail the **time-variant Charge Sensitive Amplifier**

- Connect the preamplifier to the **comparator** to build a complete analog Front-End chain


Thanks for your attention!

References

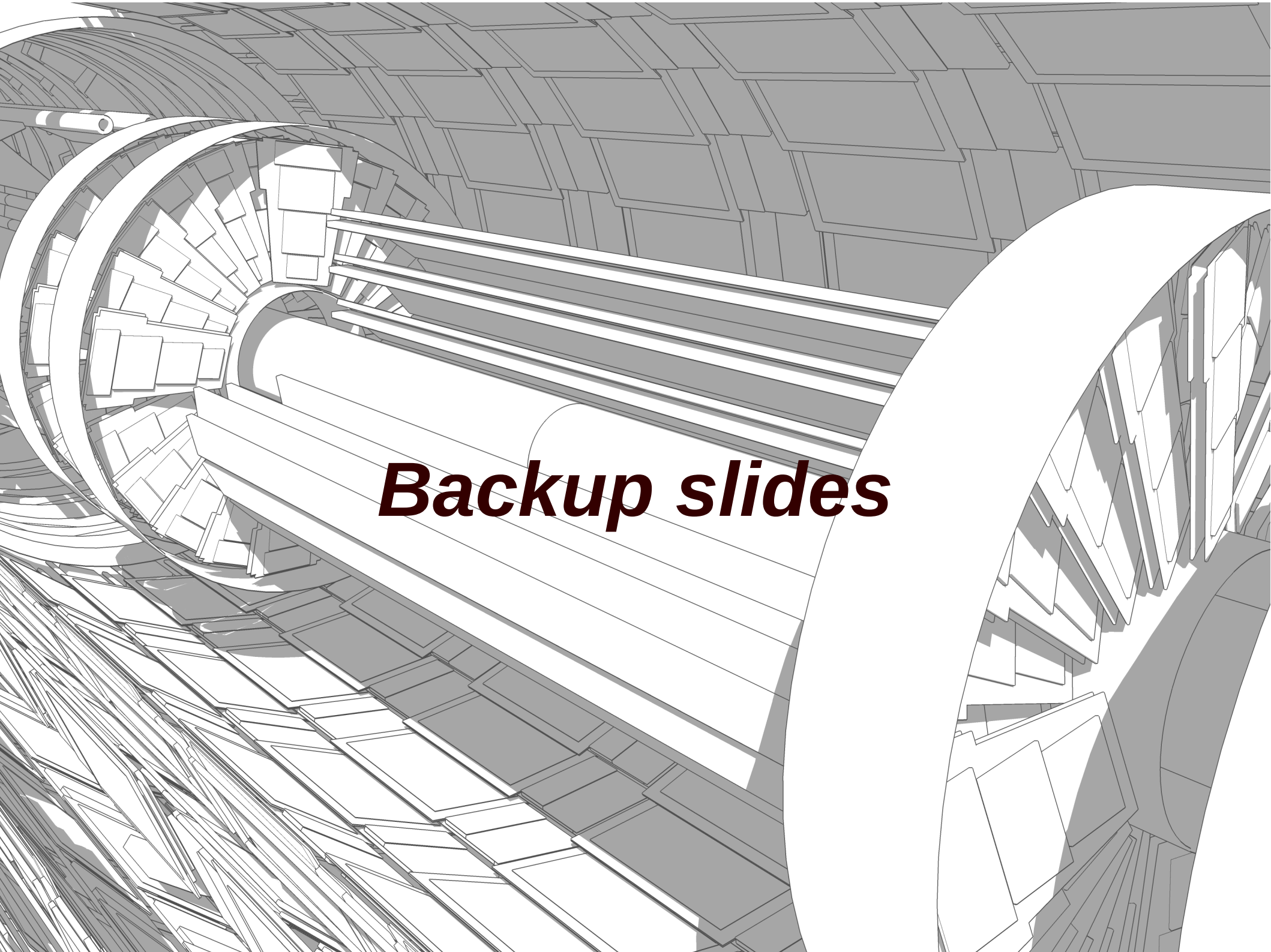
- F. Silveira, D.Flandre, P.Jespers, "A g_m/I_D based methodology for the design of CMOS analog circuits..." , IEEE 1996

- B.Razavi, "Design of analog CMOS integrated circuits", McGrawHill

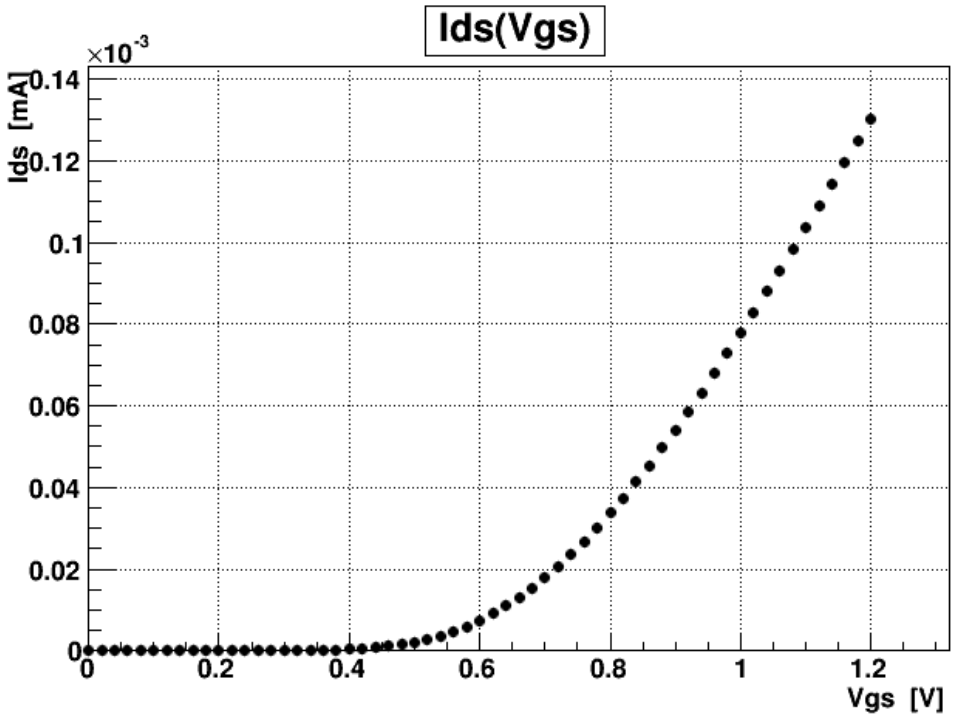
- L.Rossi, "Pixel Detectors from fundamentals to Applications", Springer

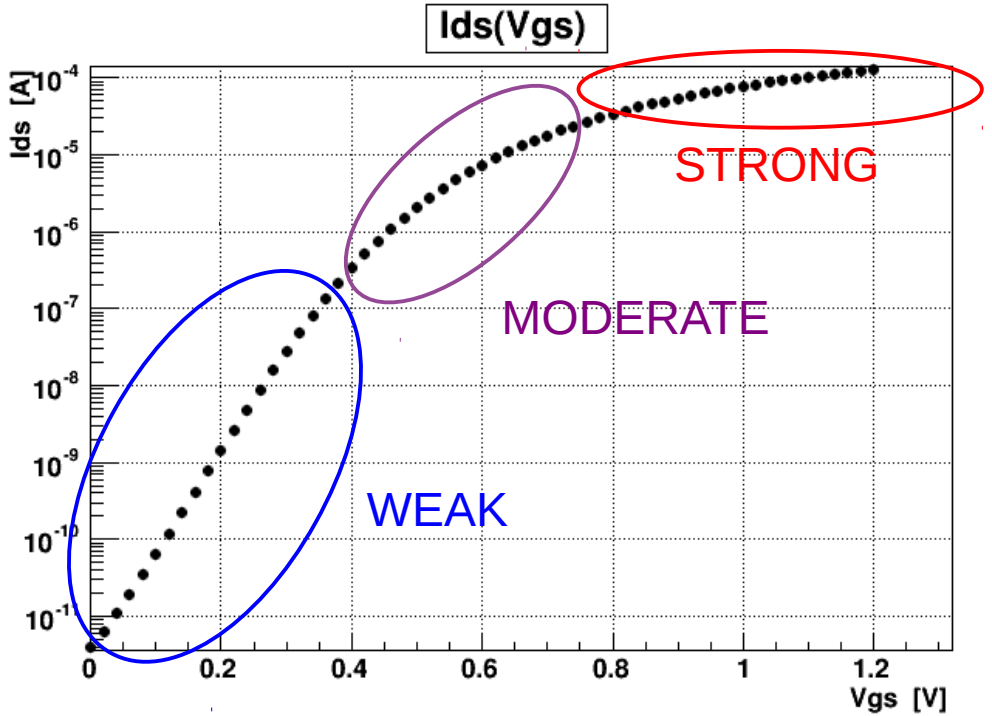
- C.Enz, F. Krummenacher, E. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to Low-Voltage and Low-current applications", article

- P. O'Connor, "Future trends in Microelectronics - Impact on detector readout"


Backup slides

MOS operating regions





- The **Inversion Coefficient** discriminates between the different operating regions:

$$IC = \frac{I_D}{2n\mu C_{ox}\frac{W}{L}\phi_T^2}$$

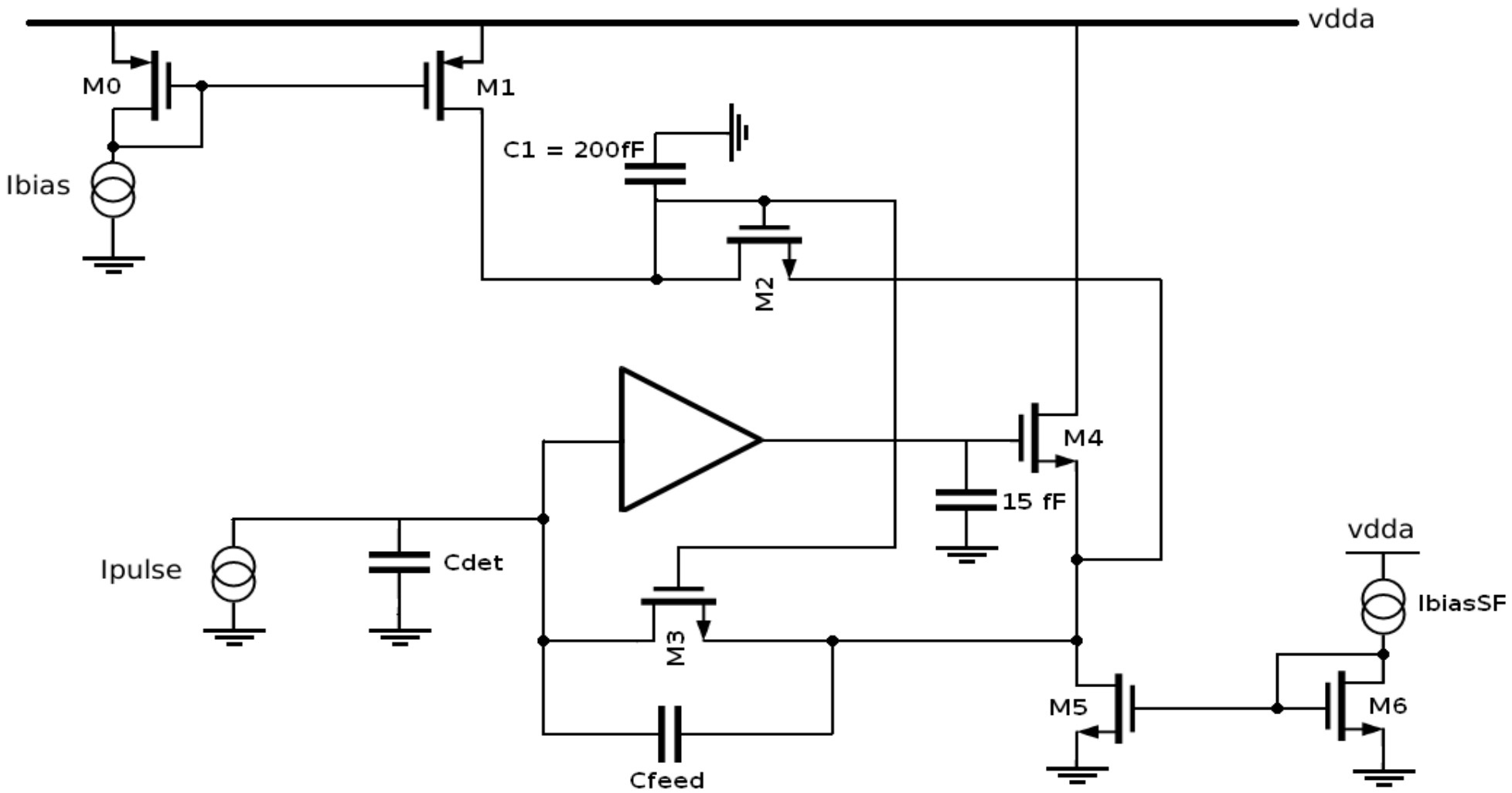
- IC < 0.1 WEAK INVERSION
- 0.1 < IC < 10 MODERATE INVERSION
- IC > 10 STRONG INVERSION

CMOS submicron technologies

- **Short channel effects** degrade analog performance
  - Threshold voltage variation with Vgs,L
  - Mobility reduction
  - Velocity saturation
  - Output impedance variation

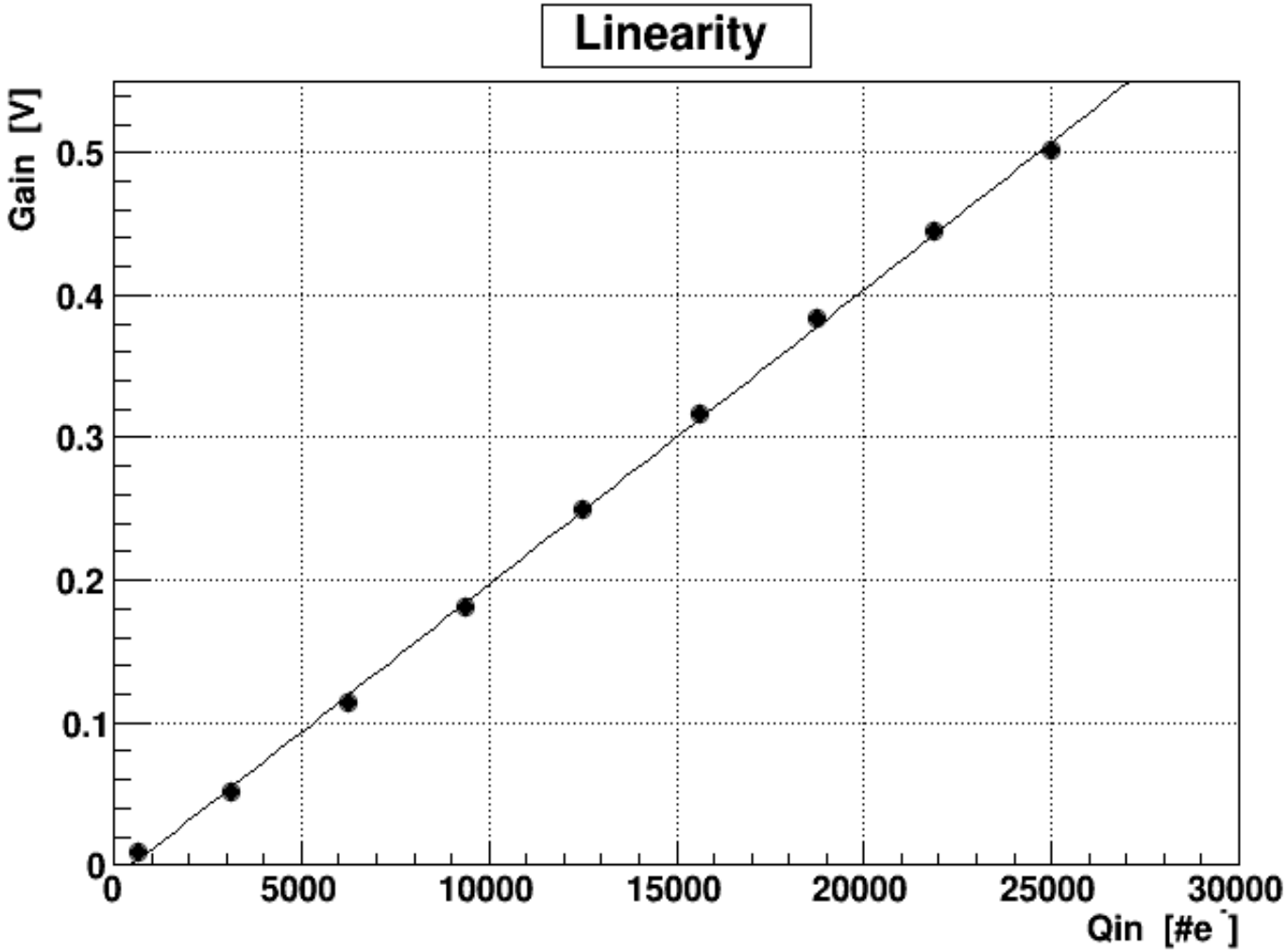
- Best compromise between speed and consumption -> **Moderate inversion region**

Feedback implementation



- Total stage power consumption ~ 2 µW

First architecture - Linearity



First architecture - Mismatch