CRYOGENIC CMOS FRONT-END FOR DARK MATTER DETECTION

RESEARCH AND DEVELOPMENT

INFN
Istituto Nazionale di Fisica Nucleare

SIGIL. VNIVERS. AVGVSTAE TAVRINORVM

DARKSIDE

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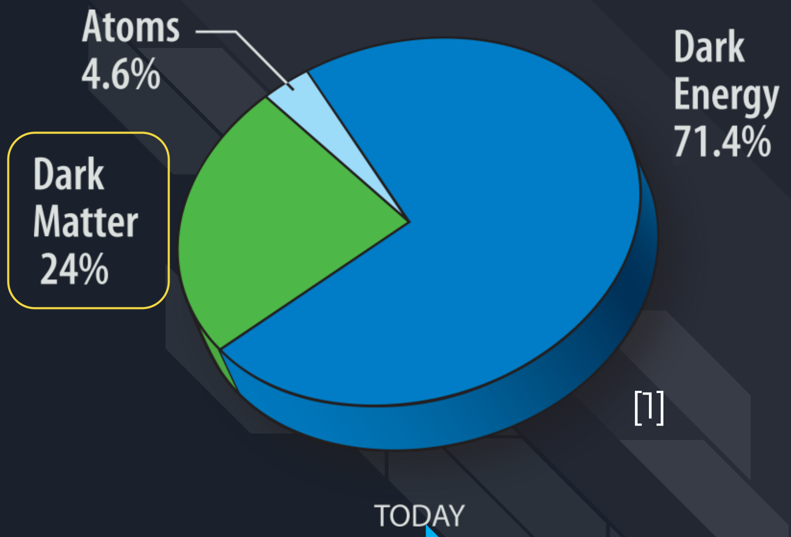
What is Dark Matter?

Dark matter is believed to be composed by some form of a non-luminous* non-baryonic particles.

The only observable interaction with normal baryonic matter is through it's *gravitational* field.



[1]

*Non-Luminous ⇒ No interaction with e-m field

Dark Matter phenomenology

There are many phenomena that are only explainable using DM, some of these are:

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- Gravitational Lensing; [1]

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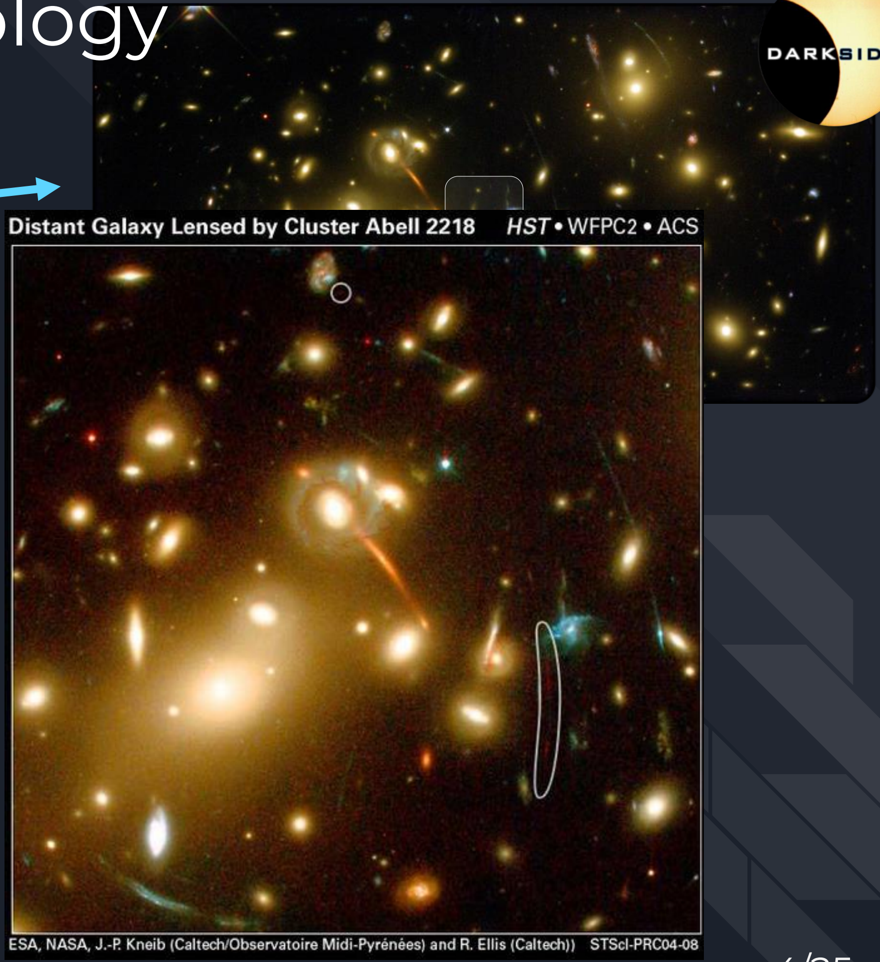


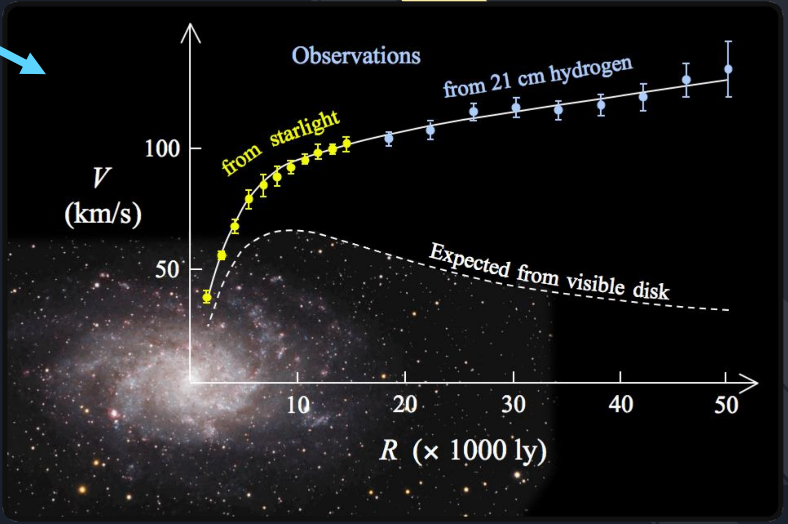
Distant Galaxy Lensed by Cluster Abell 2218 *HST* • WFPC2 • ACS

ESA, NASA, J.-P. Kneib (Caltech/Observatoire Midi-Pyrénées) and R. Ellis (Caltech)) STScI-PRC04-08

Dark Matter phenomenology

There are many phenomena that are only explainable using DM, some of these are:

- Gravitational Lensing; [1]
- Galaxy Rotational Speed; [2]



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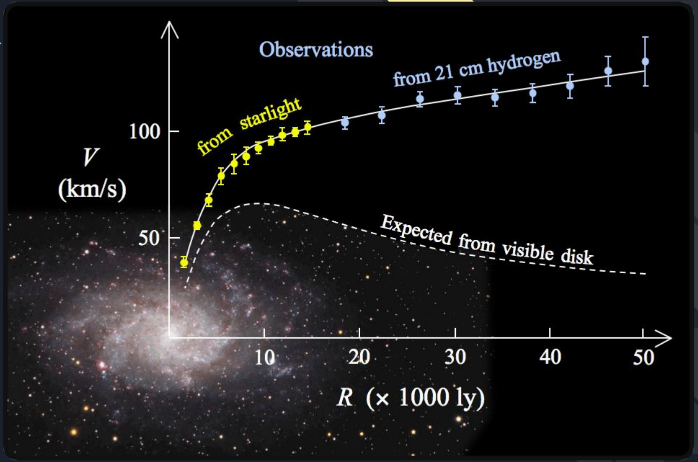
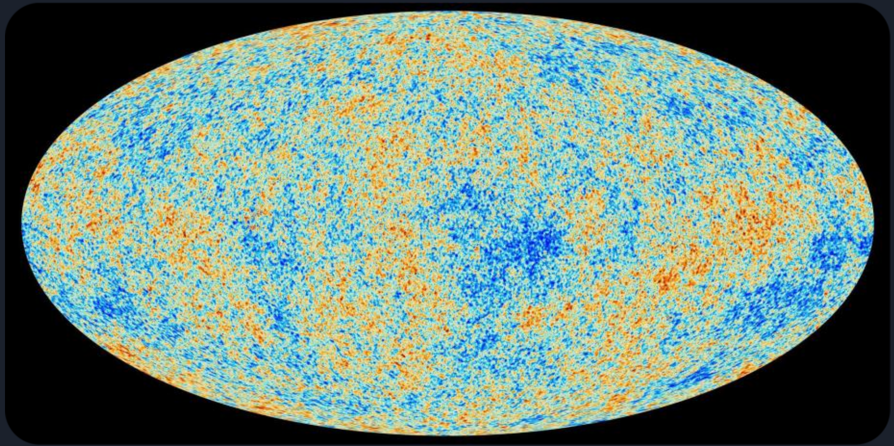
Dark Matter phenomenology

There are many phenomena that are only explainable using DM, some of these are:

- Gravitational Lensing; [1]
- Galaxy Rotational Speed; [2]
- Cosmic Microwave Background anisotropies. [3]





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How do we detect Dark Matter?

- *Direct* detection via shielded *underground* detectors;
- *Indirect* detection via WIMP *annihilation signals* captured by satellites, balloons or ground-based *telescopes*;
- *Direct* production of dark matter in high energy *particle accelerators*.

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DARKSIDE

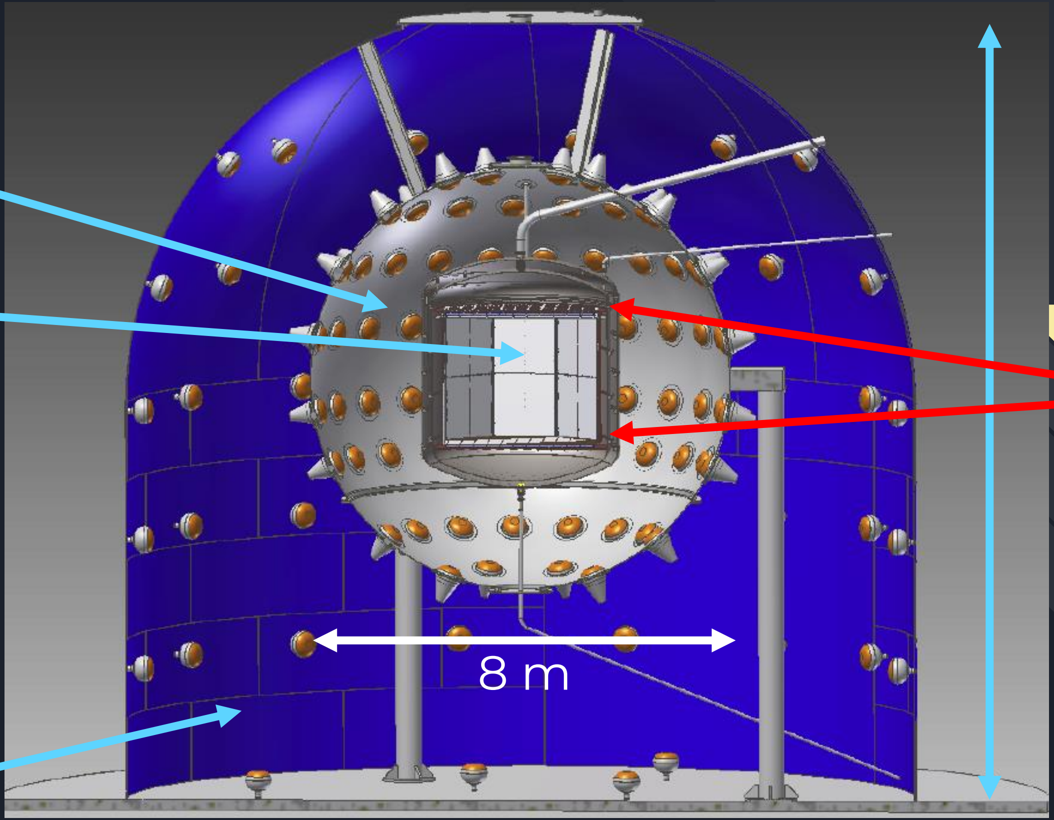
What is DarkSide?[4]

Liquid Boron scintillator tank used as an *active neutron veto*

20 ton liquid Argon TPC tank used for detecting DM, operating @

T = 87 K

Ultra-pure water tank used as an *active muon veto*



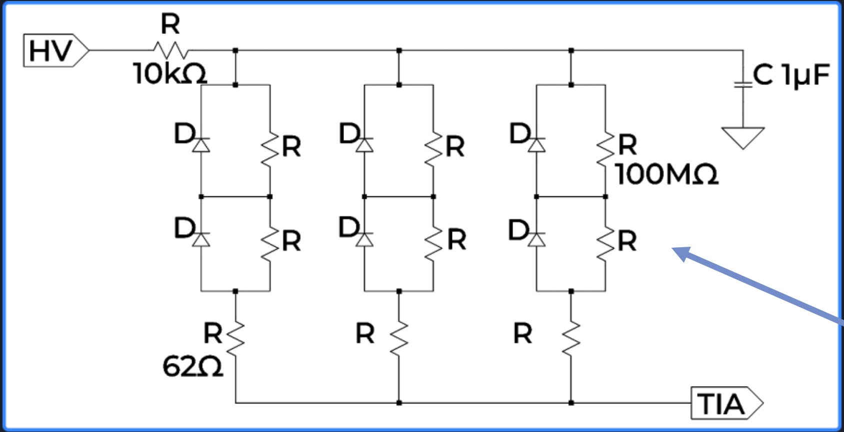
Height = 14.65 m

Base diameter = 15 m

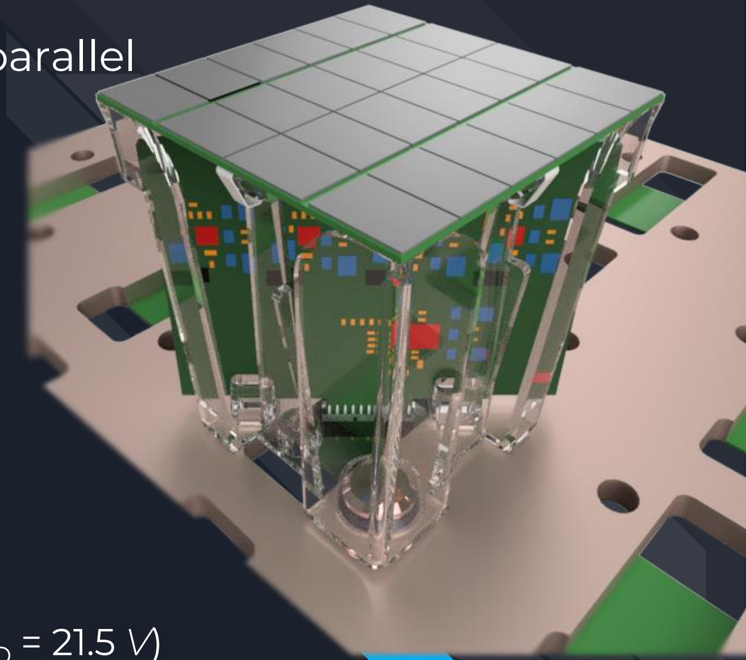
SiPM array

DarkSide PhotoDetector Module (PDM)[5]

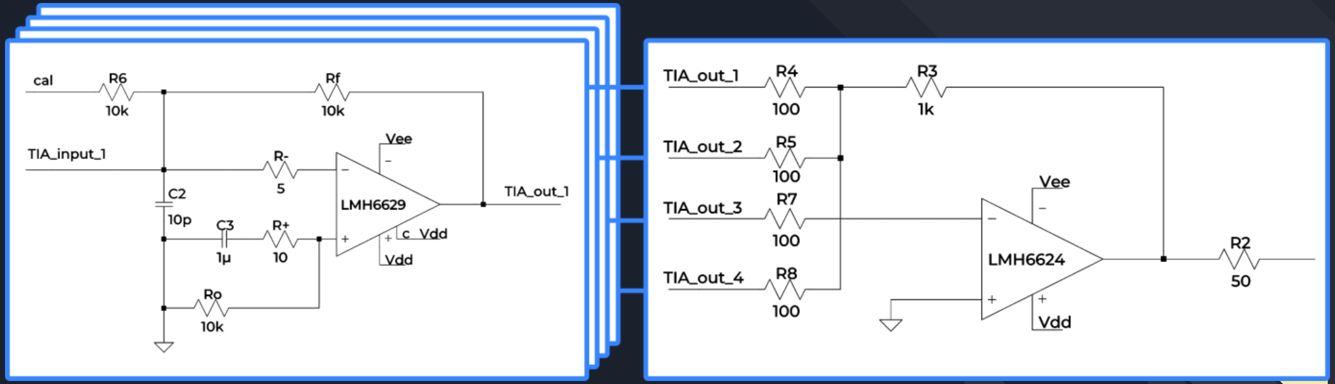
- Basic PDM: 24 independent sensors
- Each quadrant has 6 SiPMs: 2 in series and 3 in parallel
- Total sensing area: 24 cm^2
- SNR @ 77K for 1 PE: 10
- Time resolution: 20 ns
- Channel power consumption: 250 mW



OV = 5 V (V_{BD} = 21.5 V)
SPAD with 30 μm cell size
DCR ≈ 5 × 10^{-3} Hz/mm^2



DarkSide current DISCRETE Front-End [5]



- 4 independent TIAs followed by a Summing Amplifier
- Bipolar SiGe operational amplifiers
- Single analog differential output per channel
- Power consumption: 250 mW

INTEGRATED vs DISCRETE Front-End

IC vs discrete PROS:

- Simplification of chip handling: 1 component vs 40 per channel
- Improved performance using an ad-hoc design of the core building blocks
- Less interconnection between parts with local signal processing and multiplexing
- Greatly diminished power consumption: 77 mW vs 250 mW

PROBLEM: IC technology isn’t modelled outside military temperatures -55 ÷ 125 °C

Device characteristics are extrapolated by the simulator

Cryogenic operation could be different from simulations

Cryogenic CMOS: advantages and issues

ADVANTAGES

- Mobility increases
- Transconductance* increases
- Thermal noise decreases

Higher SNR

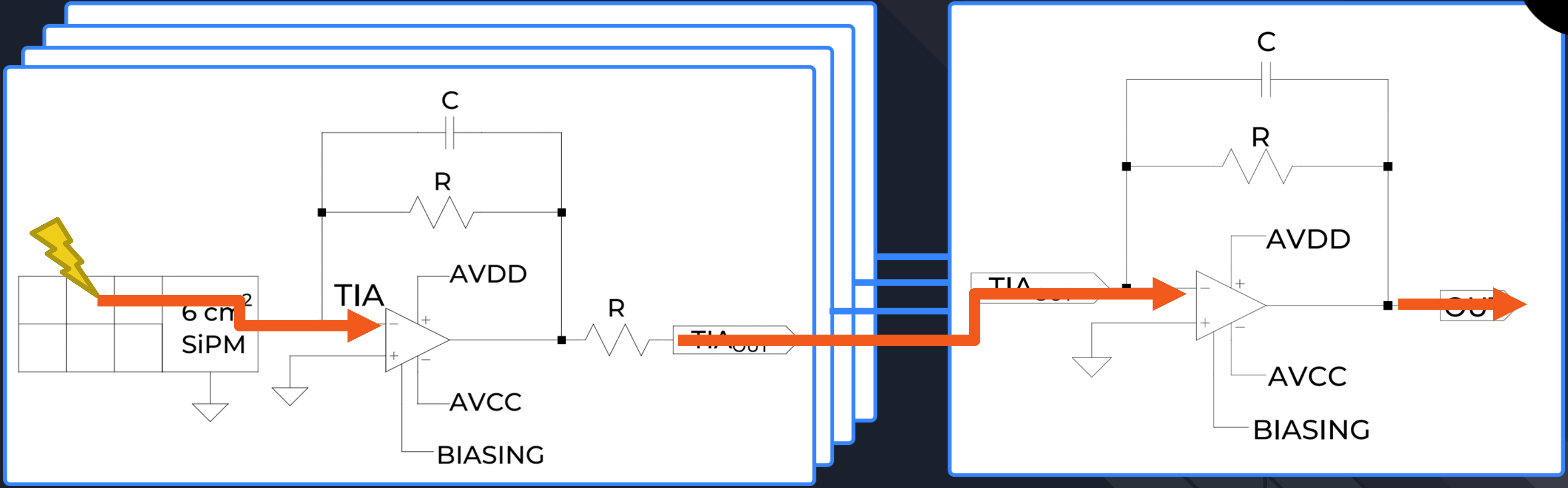
DISADVANTAGES

- Threshold voltage increases
- Hot electron effect increases (more energetic carriers)

- Quicker Si-SiO_2 interface degradation
- Oxide trapped carriers ⇒ threshold voltage shift
- Worsened Gate leakage current (due to channel interface degradation)

$$* = g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_{DS}}$$

DarkSide CMOS Front-End: Top Level



0. DM-LAr scattering generates a photon
1. SiPM detects this photon
2. TIA amplifies signal from SiPM
3. Amplified signal goes to summing amplifier
4. Summed signals are output to processing circuitry

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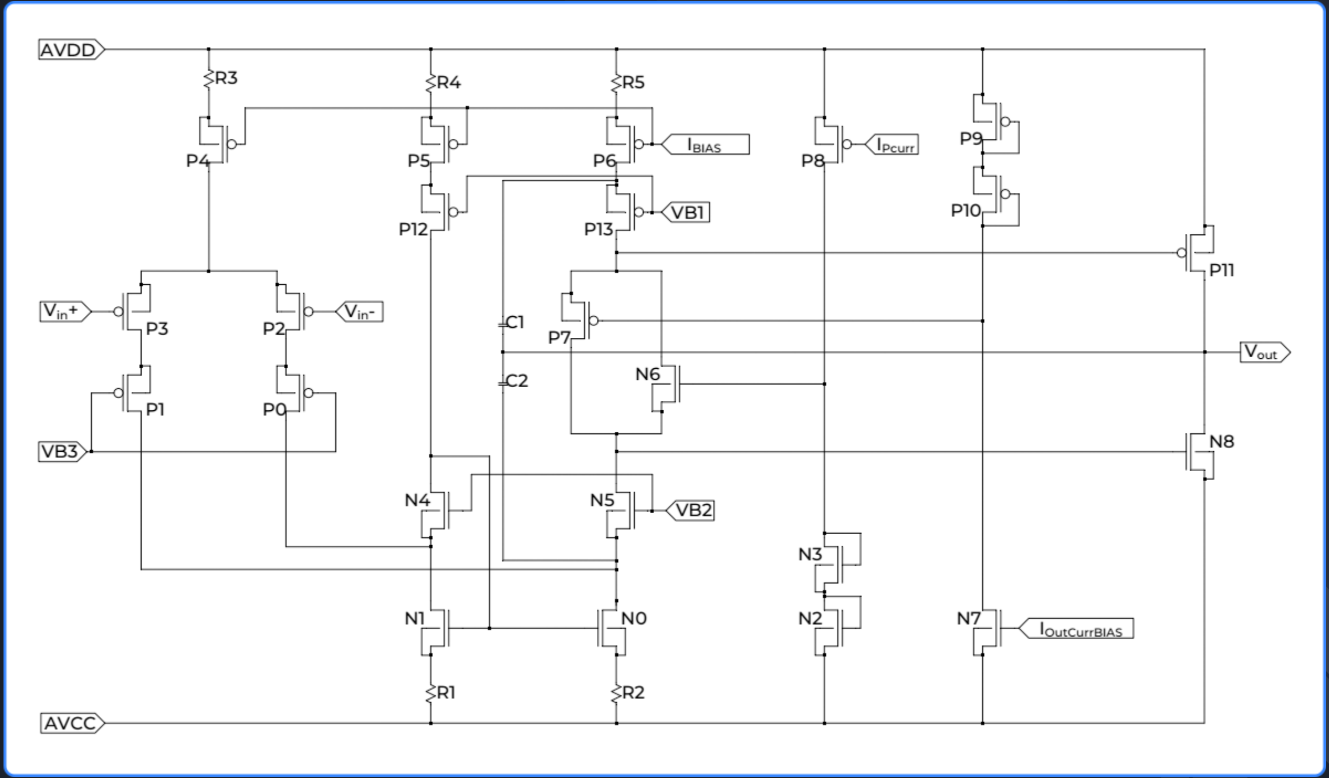
DarkSide CMOS Front-End: Single Op-Amp

- Class-AB amplifier
- Low Bias currents
- High output range
- Gain scalability
- Dual Rail 2.5V supply



DarkSide CMOS Front-End: Single Op-Amp

- Thin oxide, wide area, *input* transistors for better transconductance and lower noise
- Voltage drop on input transistors reduced by using cascode transistors
- All other transistors designed with a thick oxide to enable 2.5V operation @77K and to generate lower noise

White Noise

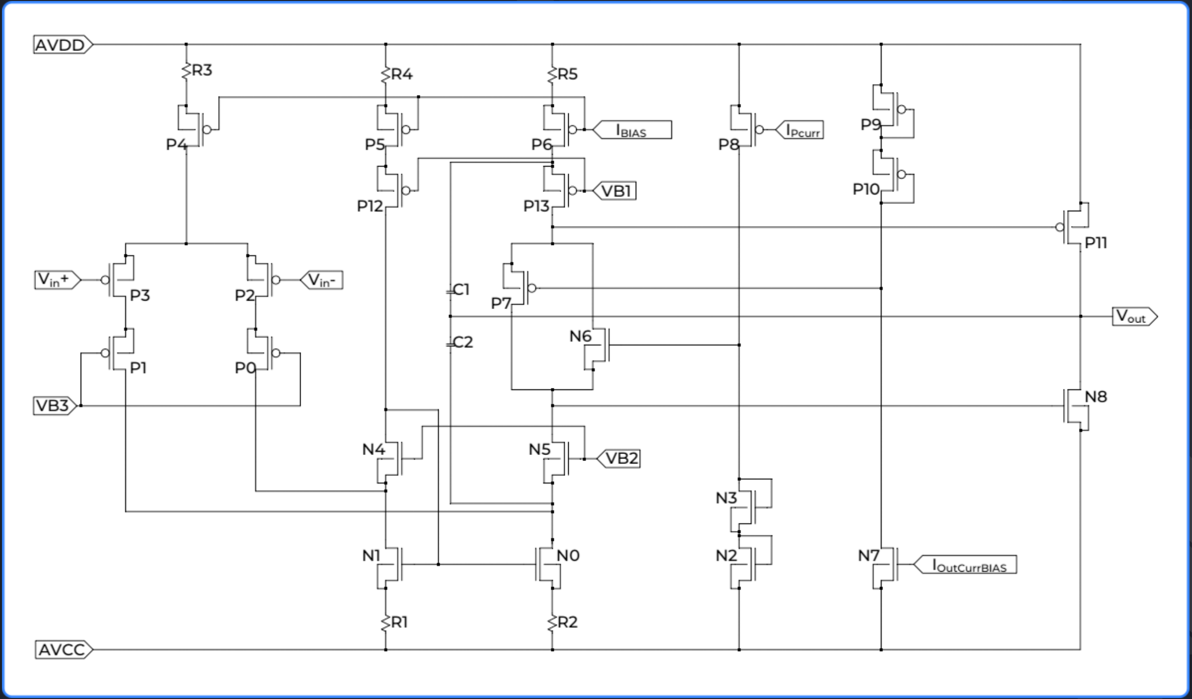
$$v_{n,w}^2 = 4k_BT\alpha_w\gamma\frac{1}{g_m}$$

Flicker Noise

$$v_{n,f}^2 = \frac{K_f(I_C,L)}{C_{ox}WL}\frac{1}{f^\alpha}$$

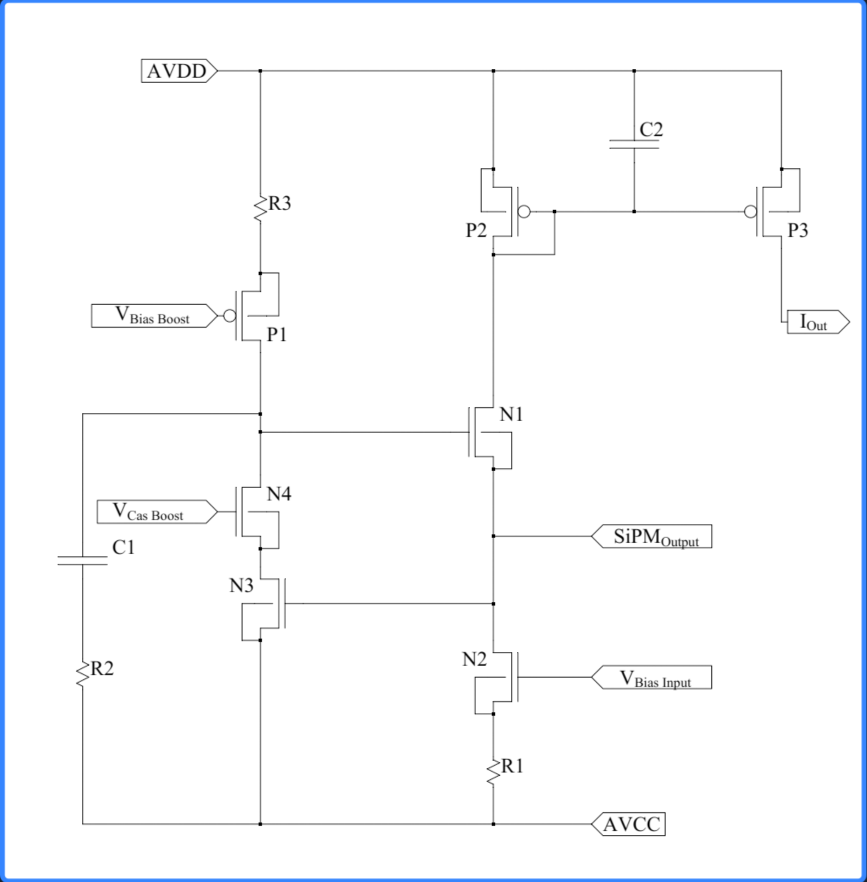
Noise on the x^{th} transistor

$$v_{n,x}^2 = 4k_BT\alpha_{w,x}\gamma_x\frac{g_{m,x}}{g_{m,in}^2}$$



CMOS Front-End: Regulated Common Gate

- N1 acts as a *common gate amplifier*
- N3 is used as a common source amplifier to reduce the input impedance
- P2 mirrors out the amplified current to P3
- P3 *outputs the current* to a shaper which transforms the current in a measurable voltage



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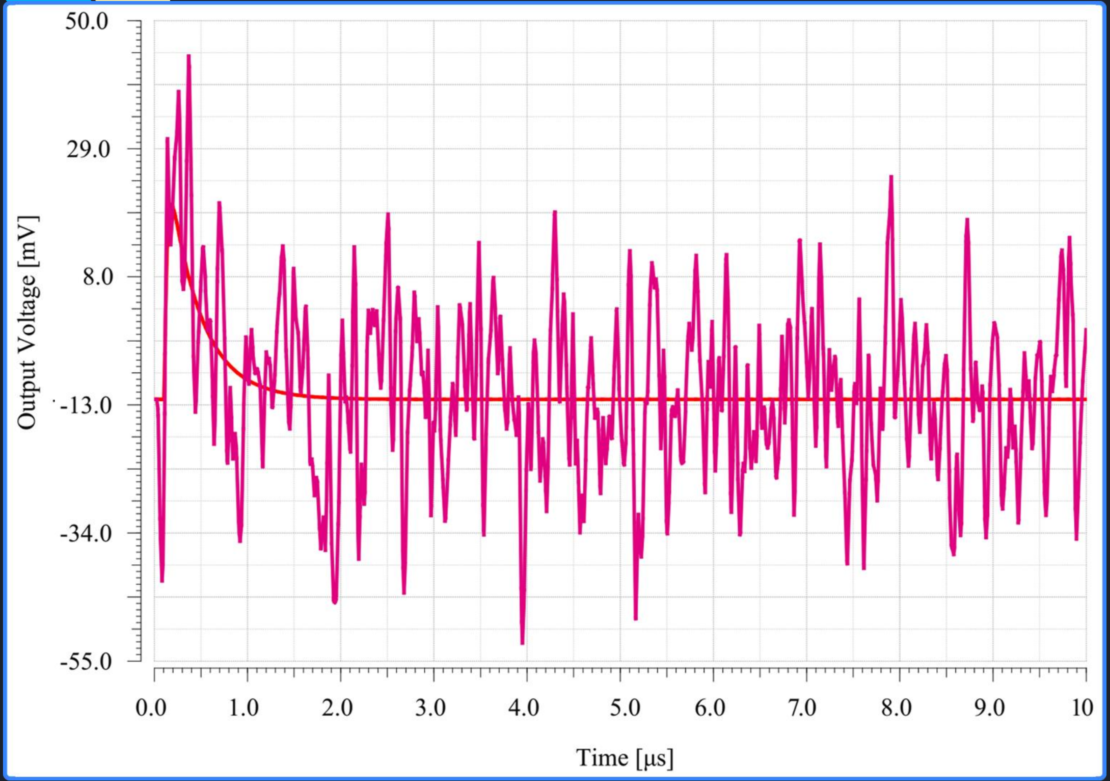
Discrete FE simulations

Temperature* = 300*K*

- ▶ Output signal
- ▶ Superimposed noise



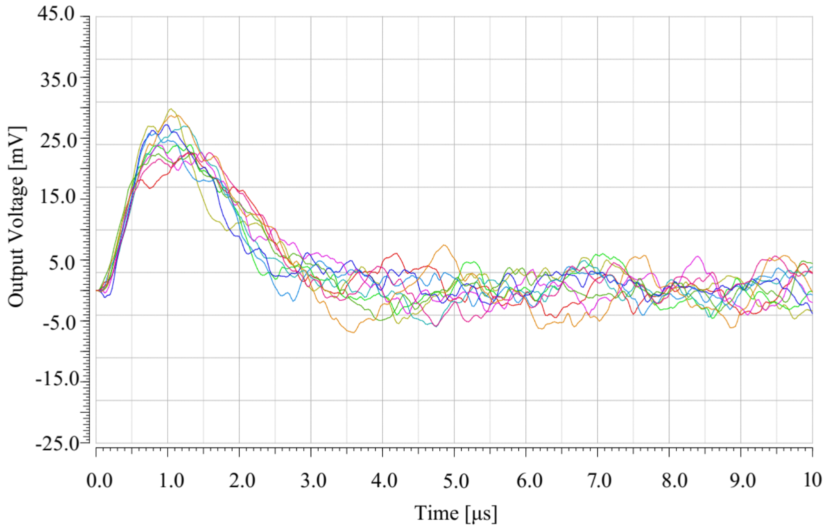
Characteristics

- ○ V_{pp} = 31.9 *mV*
- ○ $V_{noise}{}^*$ = 16.1 *mV*
- ○ SNR* ≈ 2
- ○ Jitter* = 213 *ns*
- ○ F_{co} = 487 *kHz*
- ○ Power = 188 *mW*
- ○ Dynamic Range = 50

* *Caveat*: available SPICE files of LMH6629/4 do not model noise behavior at cryogenic temperatures.

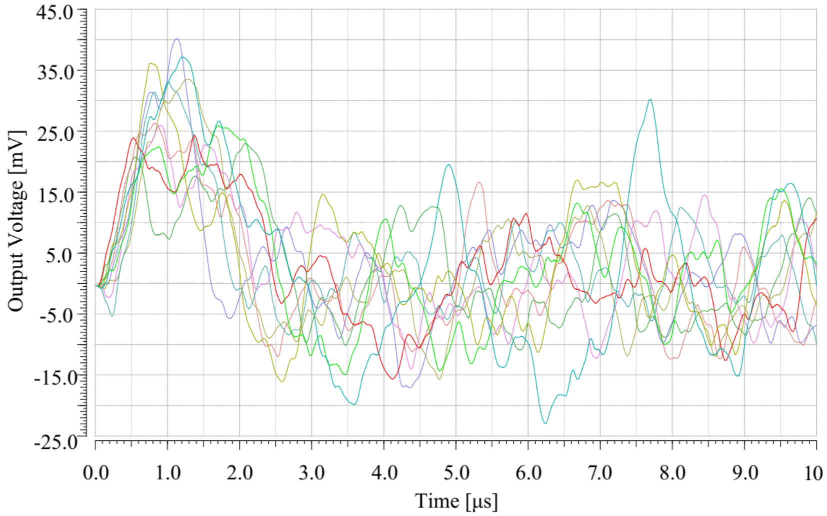
OPAMP FE simulations

Temperature = 77K



- $V_{pp} = 24.50\ mV$
- $V_{noise} = 2.67\ mV$
- SNR = 9.19
- Jitter = 56 ns
- Power = 79.96 mW
- Dynamic Range = 45

Temperature = 300K

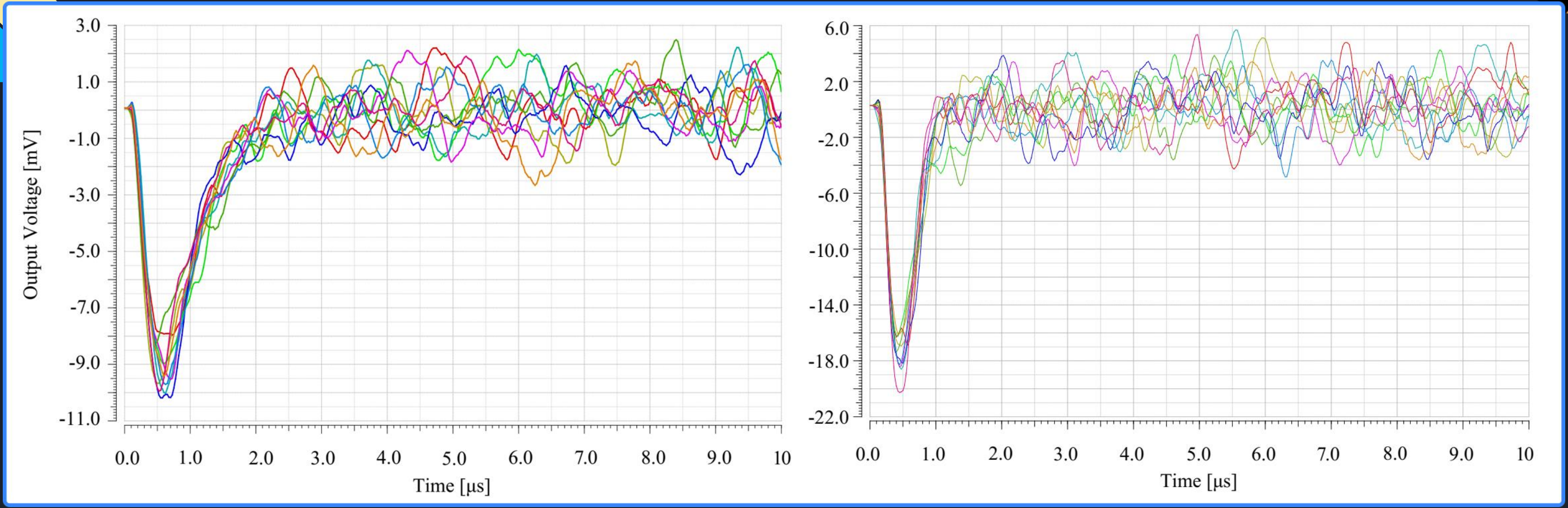


- $V_{pp} = 25.56\ mV$
- $V_{noise} = 8.16\ mV$
- SNR = 3.13
- Jitter = 145 ns
- Power = 71.47 mW
- Dynamic Range = 35

RCG FE simulations

Temperature = 77K

Temperature = 300K

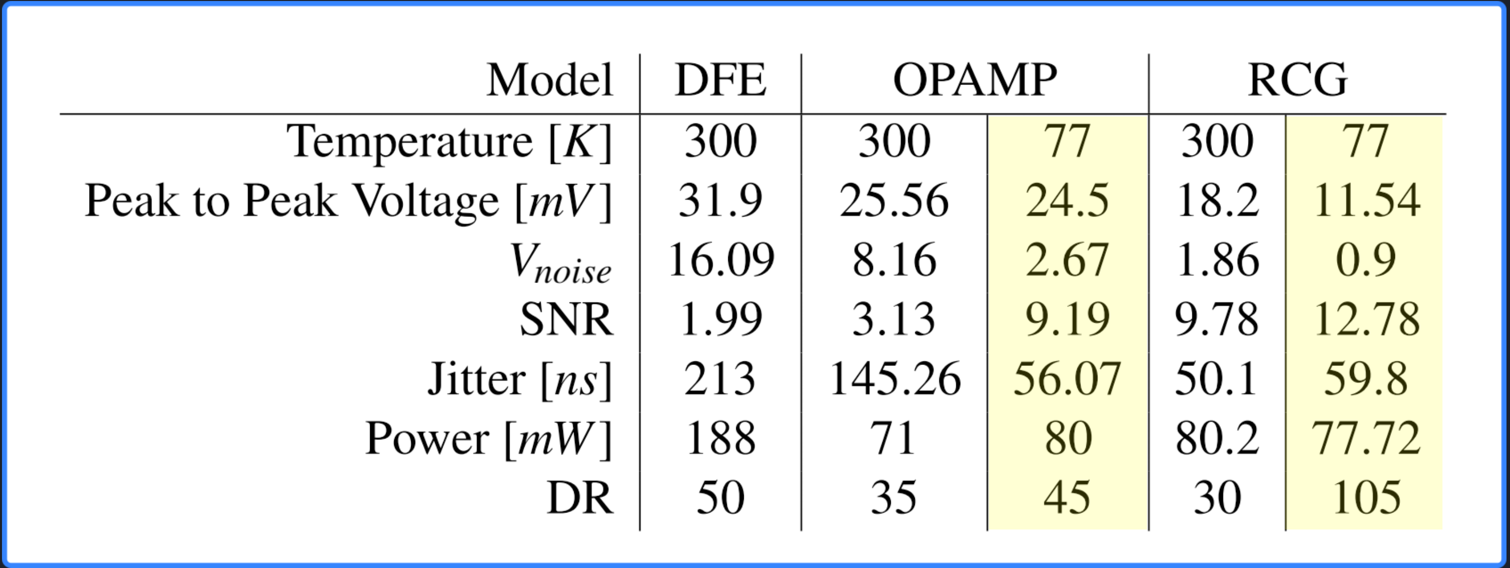


- $V_{pp} = 11.54\ mV$
- $V_{noise} = 0.9\ mV$
- SNR = 12.78
- Jitter = 59.8 ns
- Power = 77.72 mW
- Dynamic Range = 105

- $V_{pp} = 18.2\ mV$
- $V_{noise} = 1.86\ mV$
- SNR = 9.78
- Jitter = 50.1 ns
- Power = 80.2 mW
- Dynamic Range = 30

DarkSide FE simulations

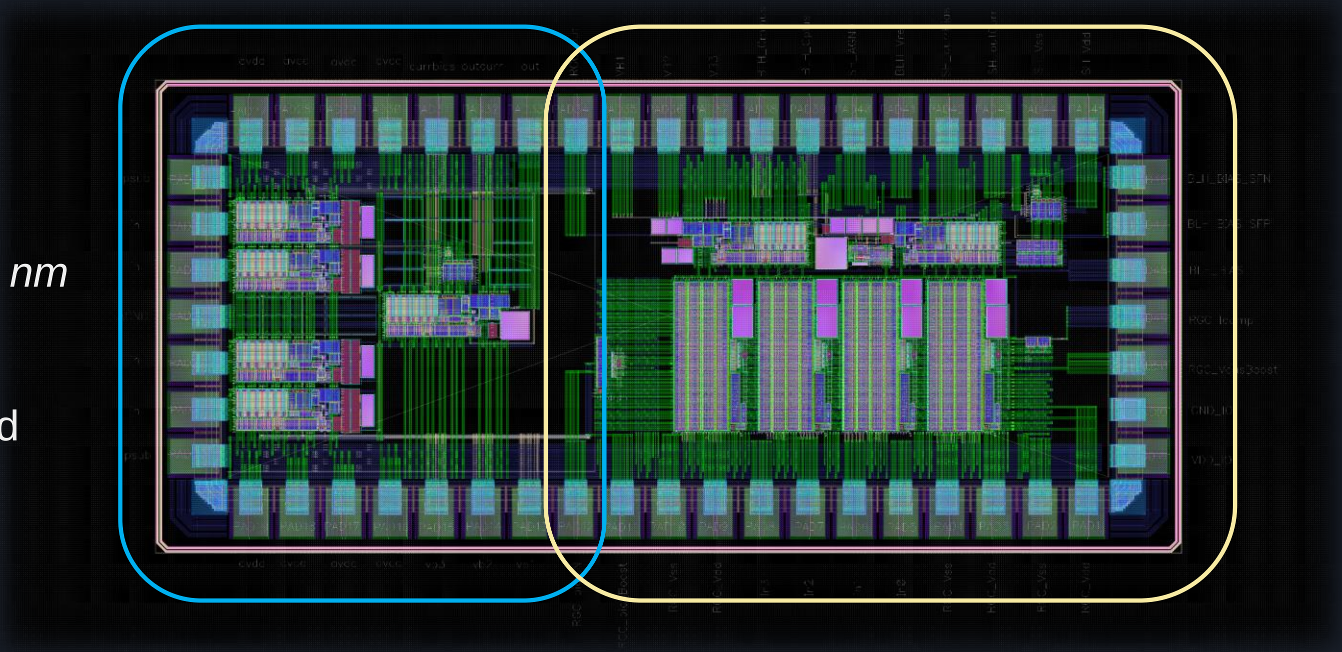
Summary



Model	DFE	OPAMP		RCG	
Temperature $[K]$	300	300	77	300	77
Peak to Peak Voltage $[mV]$	31.9	25.56	24.5	18.2	11.54
V_{noise}	16.09	8.16	2.67	1.86	0.9
SNR	1.99	3.13	9.19	9.78	12.78
Jitter $[ns]$	213	145.26	56.07	50.1	59.8
Power $[mW]$	188	71	80	80.2	77.72
DR	50	35	45	30	105

CMOS FE LAYOUT

- Submitted LAYOUT
- Technology UMC 110 *nm*
- ETA: end of April
- 1 mm x 2.5 mm
- OPAMP: 21 pads used
- RCG: 31 pads used



DS20K CMOS FE

To-Do List

- Characterize the physical front-end
- Biasing study
- Individual cryogenic circuit parts testing

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DS20K CMOS FE

Thank you for your attention

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References

1. Nasa Wilkinson Microwave Anisotropy Probe
2. The Extended Rotation Curve and the Dark Matter Halo of M33
3. Cosmic Microwave Background Anisotropies
4. Development of electronics for a single-channel, 24 cm^2, SiPM-based, cryogenic photodetector
5. Cryogenic Lifetime Studies of 130 nm and 65 nm CMOS Technologies for High-Energy Physics Experiments