University of Turin

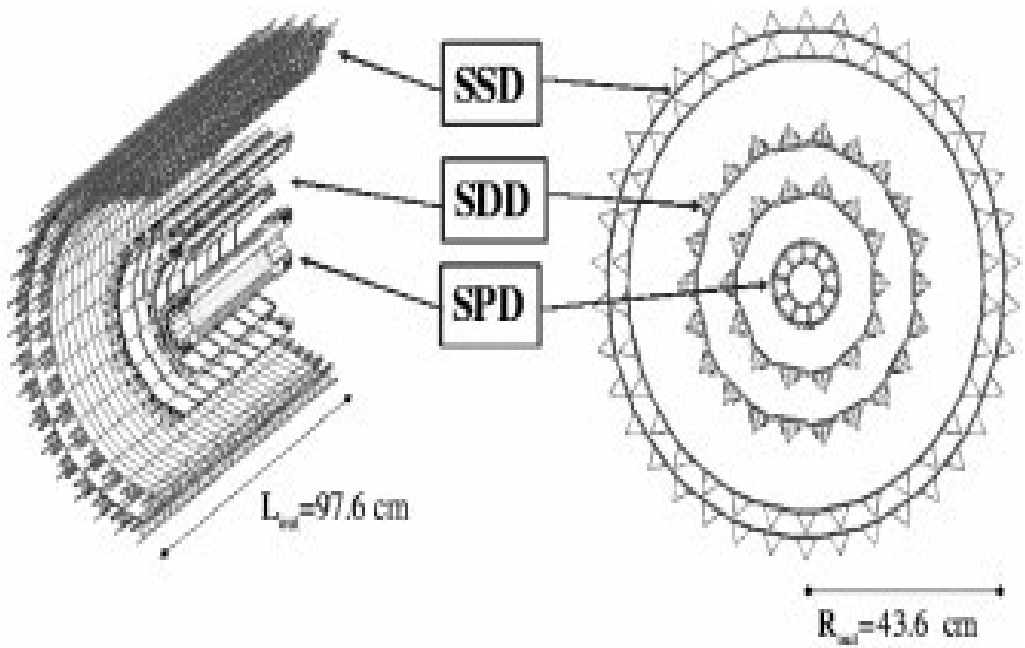
Physics Degree Thesis

Development of Integrated Electronics for Monolithic Detectors in Qwell CMOS Technology

Supervisor: A. Rivetti
Co-Supervisor: G. Mazza

Candidate: A. Lattuca

Inner Tracking System



USE:

- Primary Vertex Localization;
- Secondary Vertex Reconstruction;
- Particle Identification;

Six Layers:

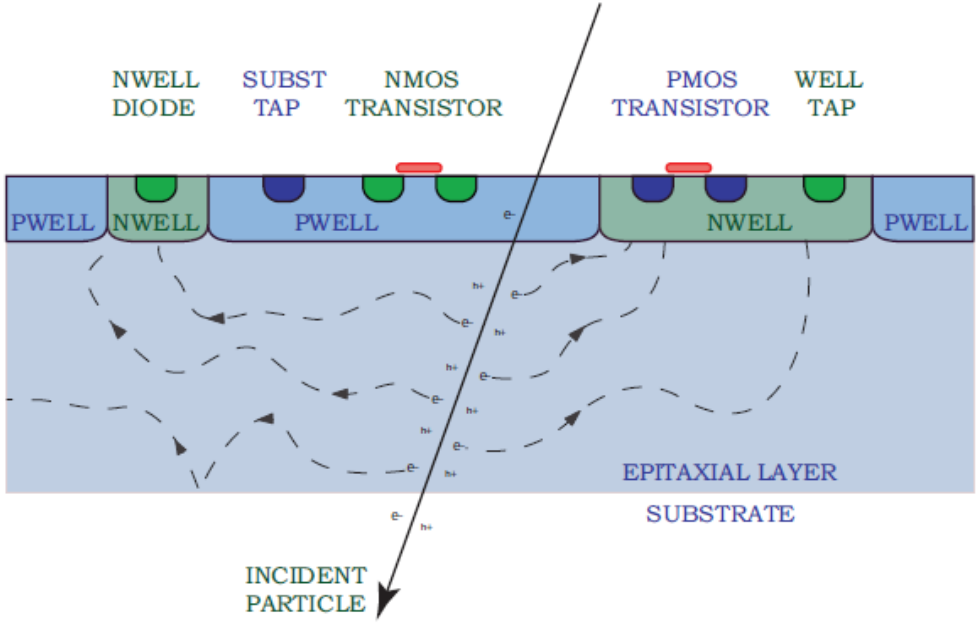
- In the two inner layers: SPD
- In the two intermediate layers: SDD
- In the two outer layers: SSD

Requirements for the new ITS

Parameter	Present ITS	New ITS
First layer radius	3.9 cm	2.2 cm
Pixel size	50 μm x 425 μm	20 μm x 20 μm
Material budget per layer	1.14 % X_0	0.3 % X_0
Power consumption	500 mW/cm^2	< 300 mW/cm^2
Read out rate	1 kHz	50 kHz

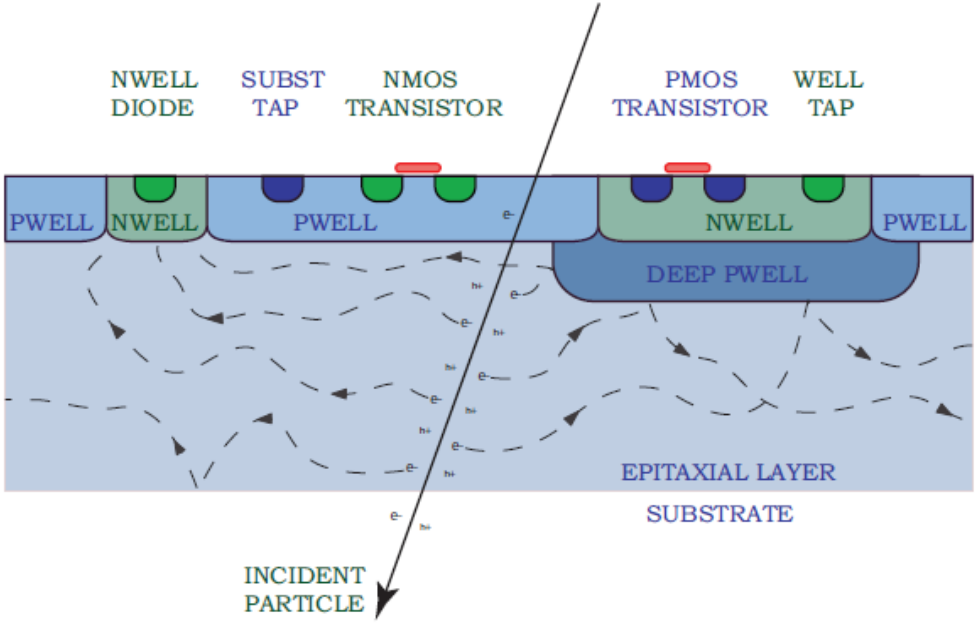
Monolithic Active Pixel Sensors (MAPS)

Comparison between standard and quadruple well process



Standard

- ✯ **Thermal Diffusion**
- ✯ **Nwell diode**
- ✯ **No p-type transistors**



Quadruple well

- ✯**Thermal Diffusion**
- ✯**Nwell diode**
- ✯**Deep Pwell - p-type transistor implementation**

Monolithic Active Pixel Sensors - MAPS

Benefits

- Sensor and electronics on the same wafer
- Minimum multiple scattering
- Reduction of pixel size

Drawbacks

- Collection time ~ 100ns
- Signal ~ 1000e per MIP

ALICE R&D

- TOWERJAZZ - 0.18um Qwell CMOS technology
- International Collaboration: INFN, CERN (Ginevra), IN2P3 (Strasbourg);
- 20 μm x 20 μm sensor
- Functional blocks
- 1.8 V supply voltage

ICs Development and Fabrication

☆Design	(1) Definition of the drawing (2) Implementation (3) Simulation	One Year

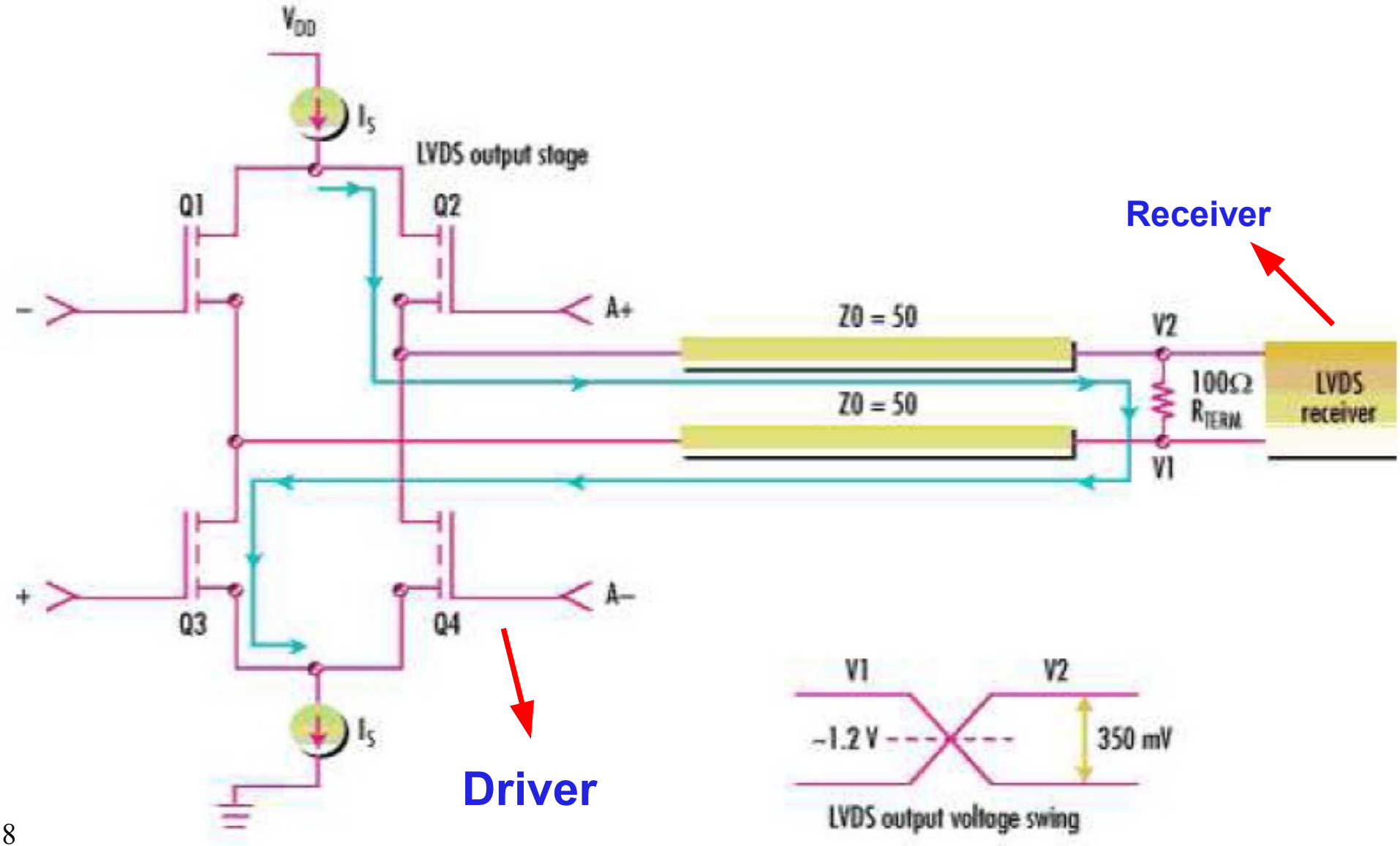
☆ Fabrication
(Four Months)

(1) Wafer Processing
(2) Several litographyc steps
(3) Oxidation
(4) Ion Implantation
(5) Deposition and Etching

- Prototype Costs:
  50.000€
- IC Prod. Costs:
  200.000€ - 2.000.000€

☆ Characterization

Low Voltage Differential Signaling (LVDS) trasmission system

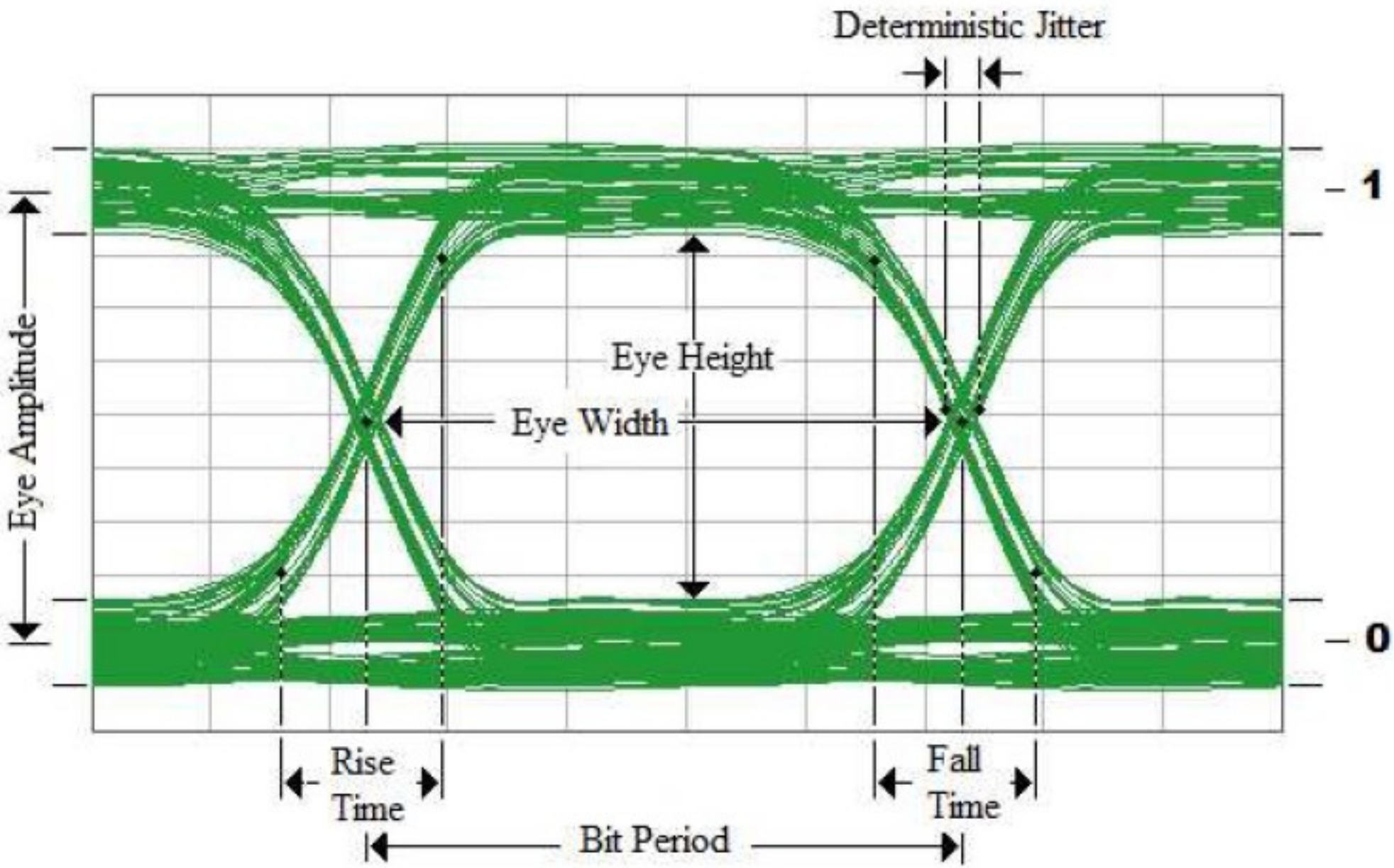


LVDS specifications:

- High trasmission rate (> 500 Mbit/s)
- Low power consumption
- Differential signal
- Low voltage swing, V_{VS} = 200 to 400 mV

- V_{DD} : (2.5 -3.3) V
- V_{CM} = 1.2 V
- $V_{OH} = V_{CM} + (V_{VS}/2)$
- $V_{OL} = V_{CM} - (V_{VS}/2)$

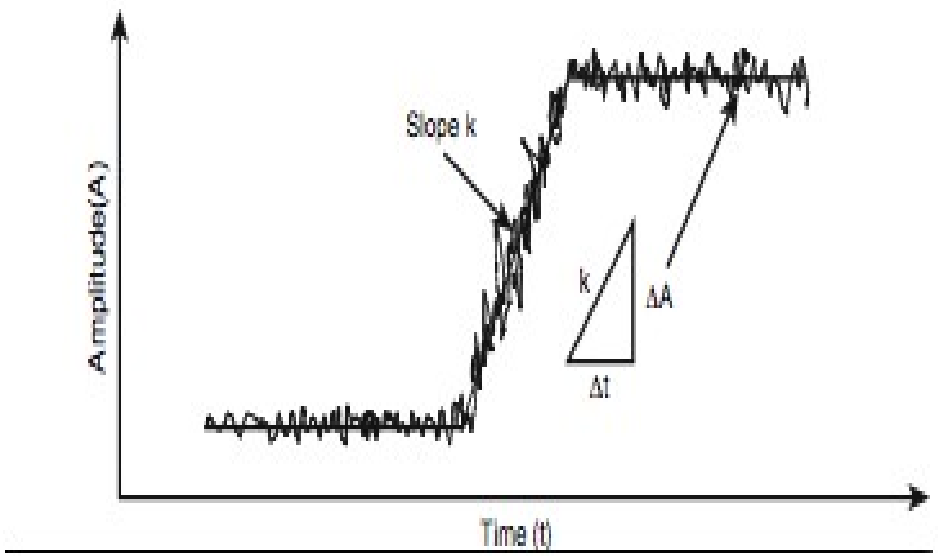
Analyzing Signals : Eye Diagram

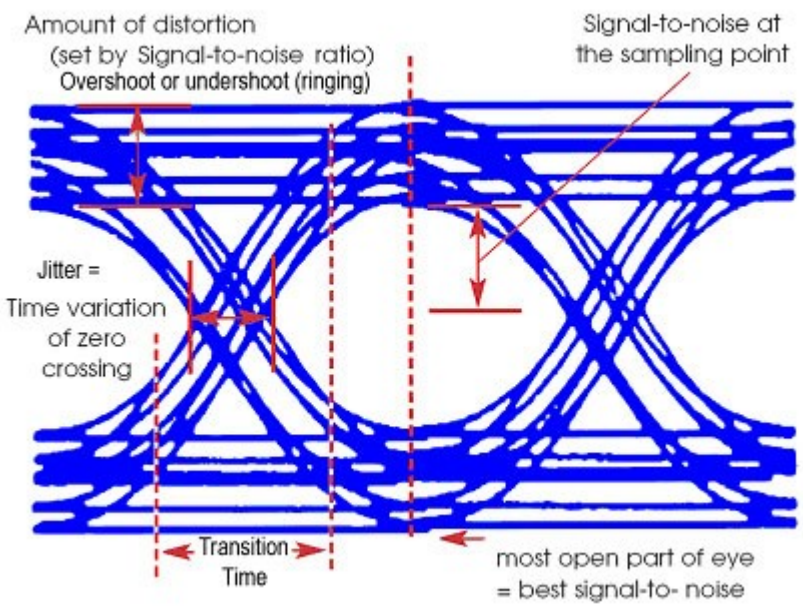


Jitter

$$\Delta t = \frac{\Delta A}{\partial A_0 / \partial t} = \frac{\Delta A}{k}$$

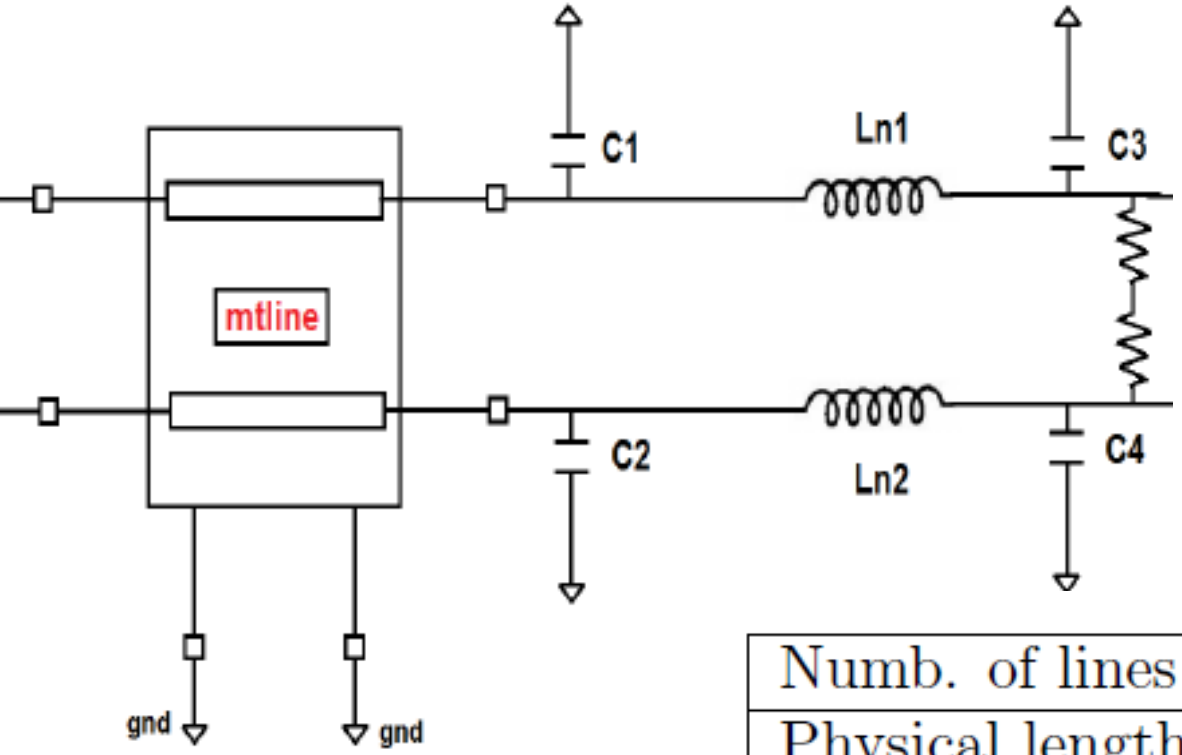
"Jitter is defined as the short-term variations of a digital signal's significant instants from their ideal positions in time. Significant instants could be (for example) the optimum sampling instants."





$$T_j = D_j + nR_j$$

Deterministic Jitter **Random Jitter**



Transmission line model

Parasitic Components

Ln1 = Ln2 = 1.5nH

C1 = C2 =250fF

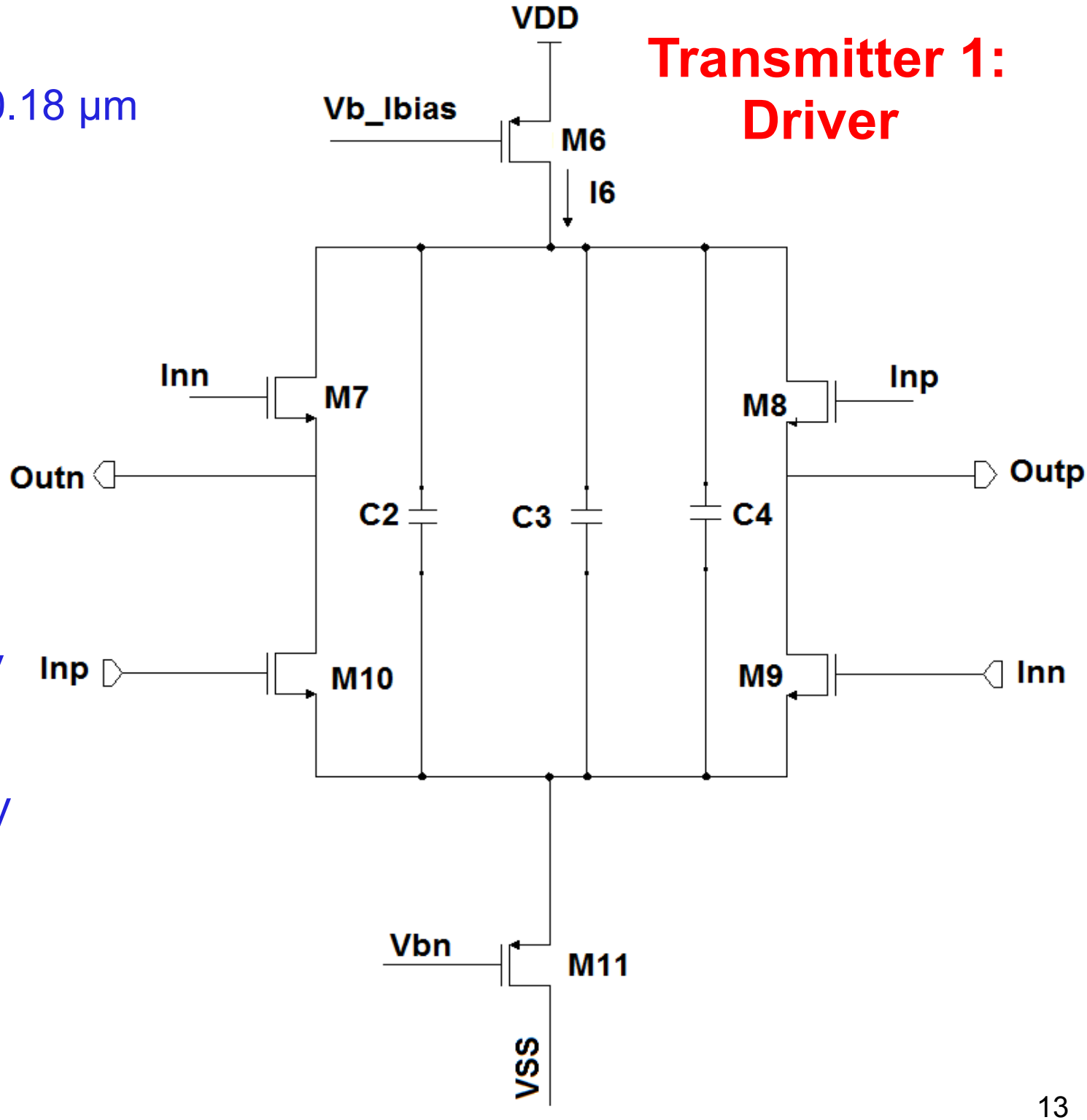
C3 = C4 = 600fF.

Numb. of lines	2
Physical length (L)	50 cm
Multiplicity factor	1
Rel. dielectric constant of layers (er)	4.45
Dielectric layer thickness	150 μm
Signal line width	280 μm
Signal line thickness	9 μm
Signal line height (h)	9 μm
Signal line spacing	280 μm
Ground plane Thickness	9 μm
Signal line conductivity	33.3 MS

Transmitter 1: Driver

Technology: CMOS 0.18 µm

VCM = 900 mV

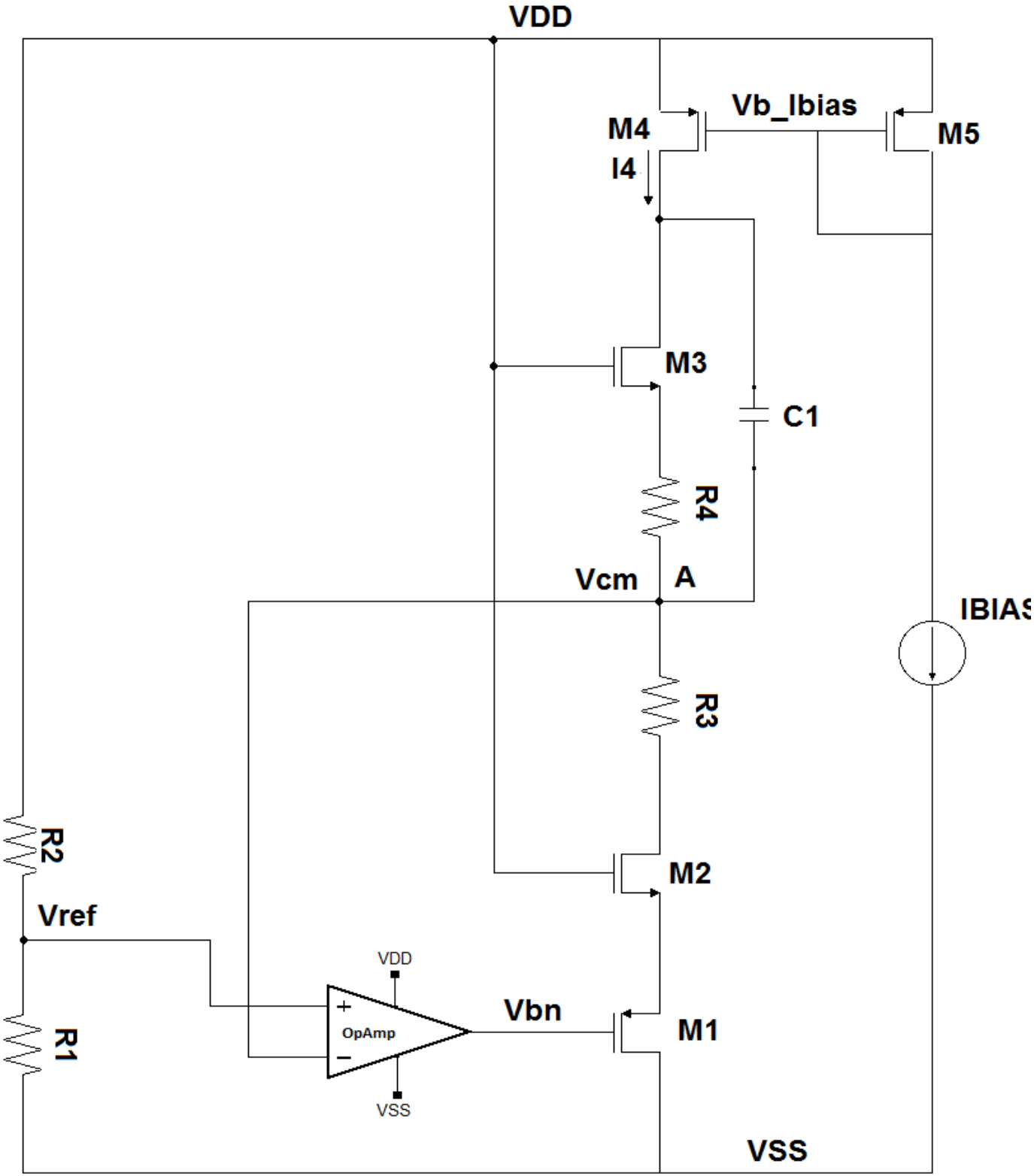


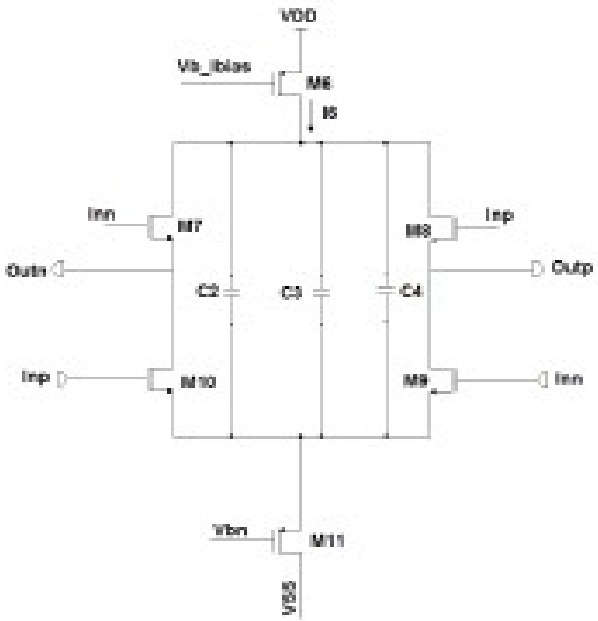
Power supply voltage Vdd = 1.8V

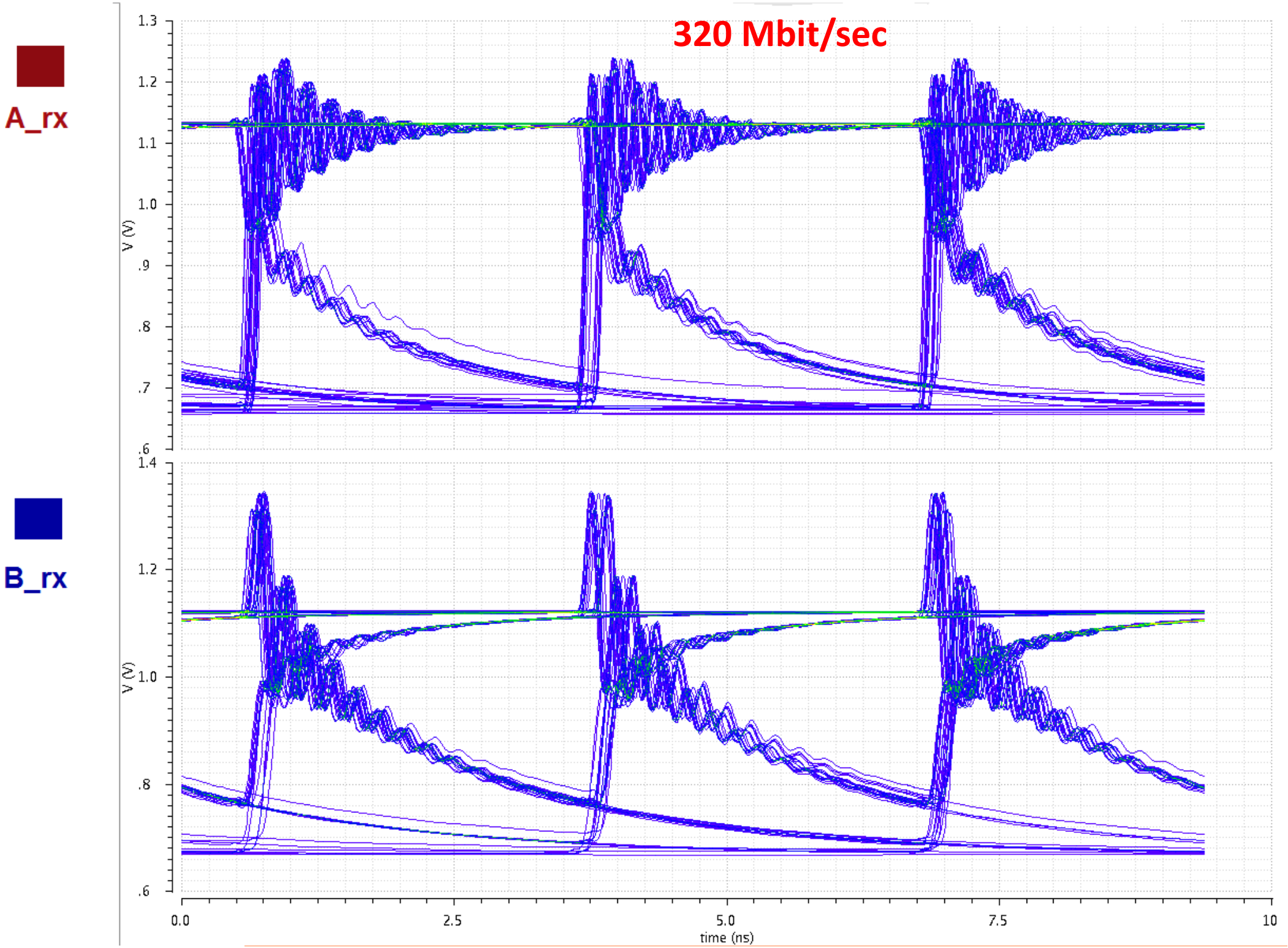
Power supply voltage Vss = 0.0 V

Transmitter 1

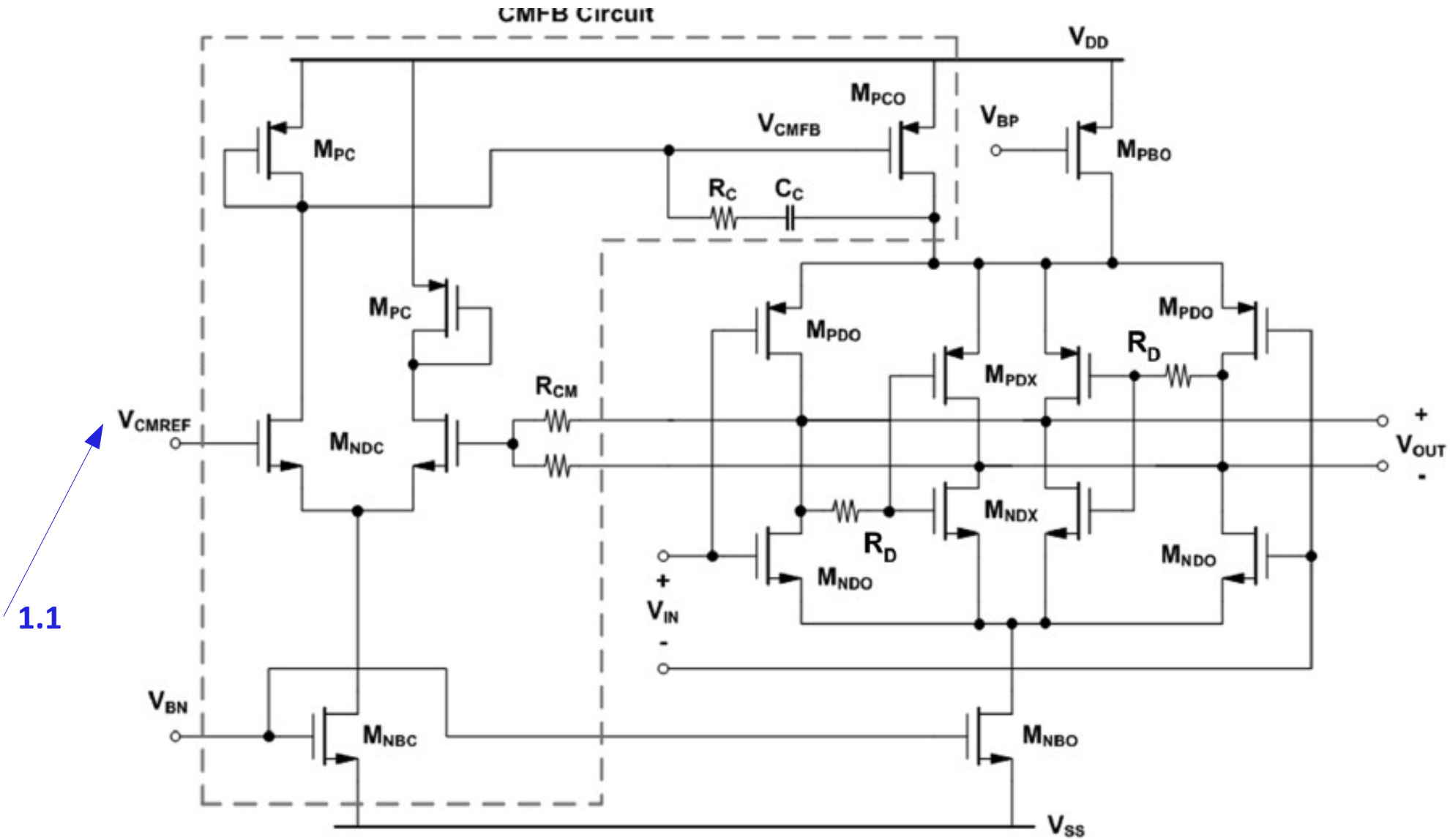
Replica Bias Circuit

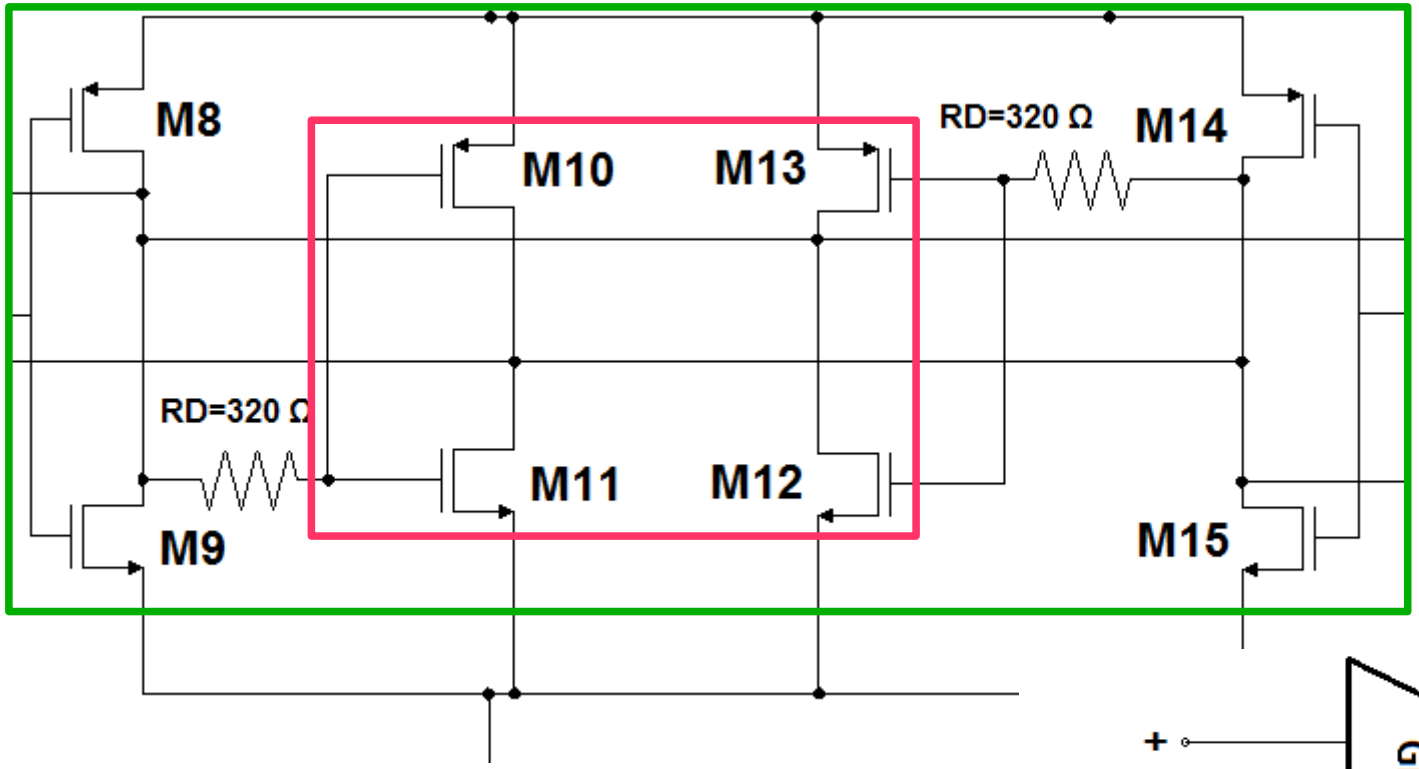





320 Mbit/sec
A_rx
B_rx
V (V)
1.3
1.2
1.1
1.0
.9
.8
.7
.6
1.4
1.2
1.0
.8
.6
0.0
2.5
5.0
7.5
10
time (ns)

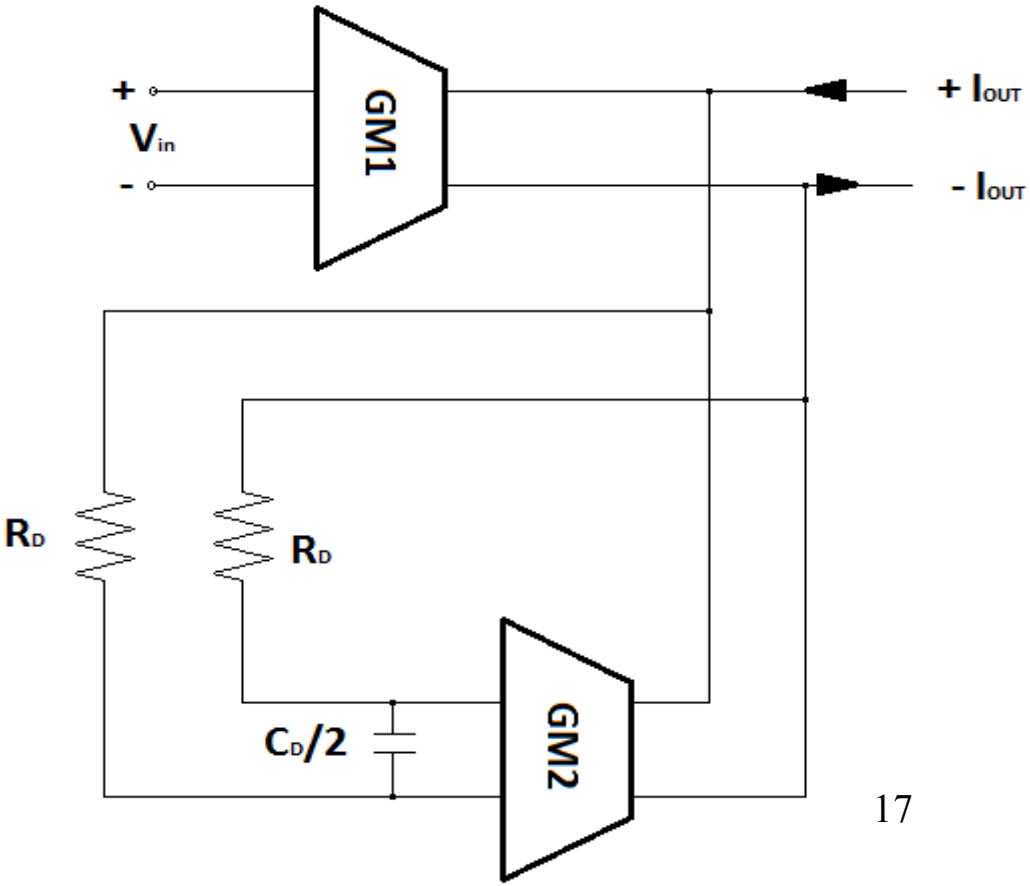
Transmitter 2





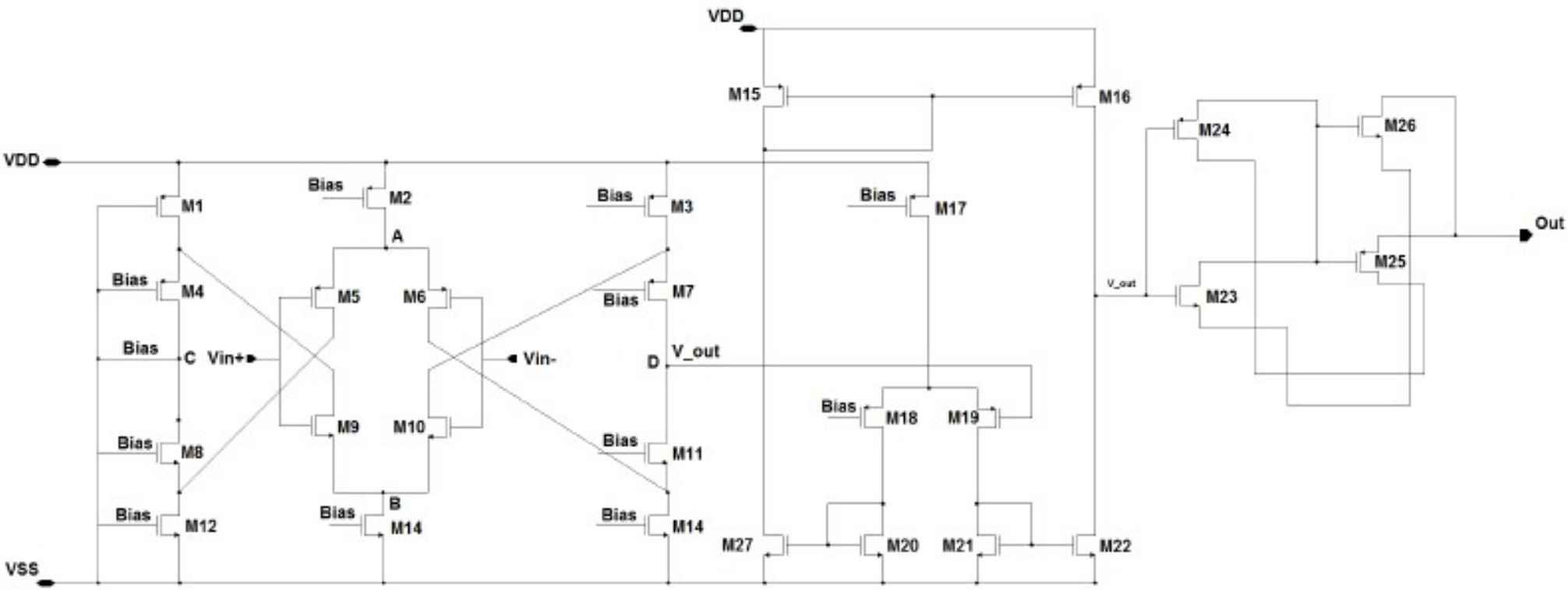
GM1

GM2



- Technology: CMOS 0.18 µm
- Power supply voltage Vdd = 1.8V
- Power supply voltage Vss = 0.0 V
- VCM = 1.1 V
- IS : (2.5 – 4) mA
- Vvs : (250 – 400) mV

Receiver



- **0.18 µm CMOS technology**
- Self biased rail-to-rail scheme

- VDD = 1.8 V
- VSS = 0 V
- Vvs =(0 – 1.8) V

Simulation Test Bench

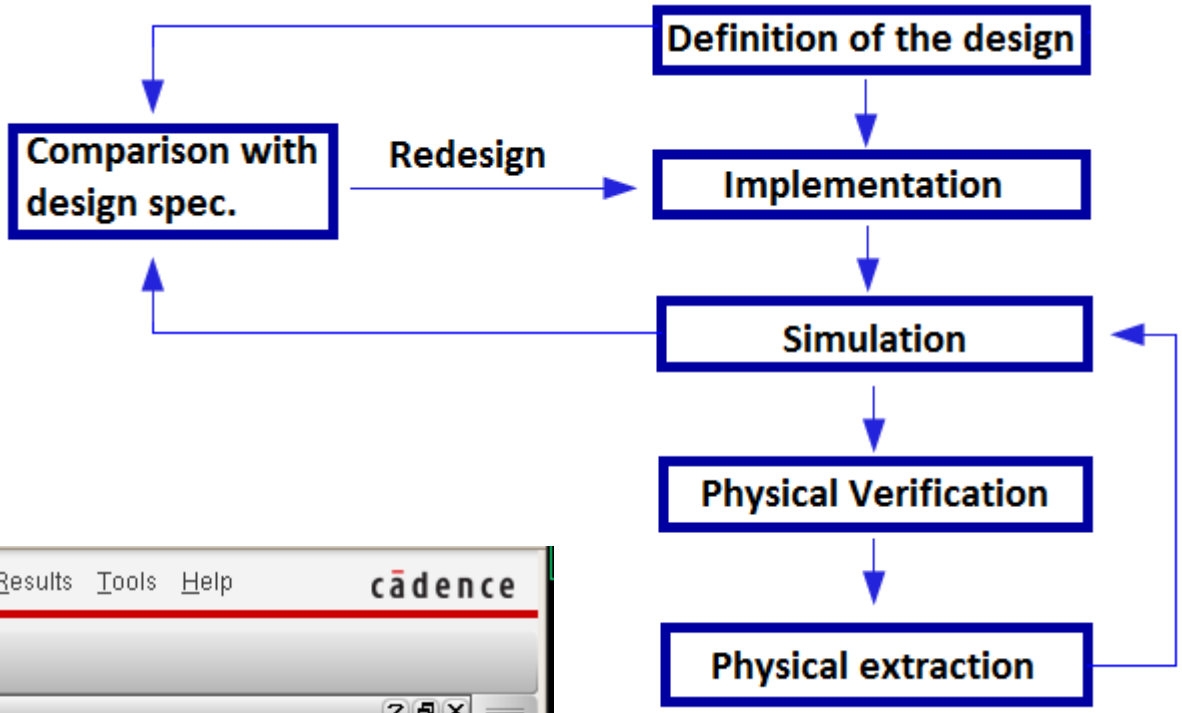
Square Waves: 320 Mbit/s, 640 Mbit/s, 1 Gbit/s

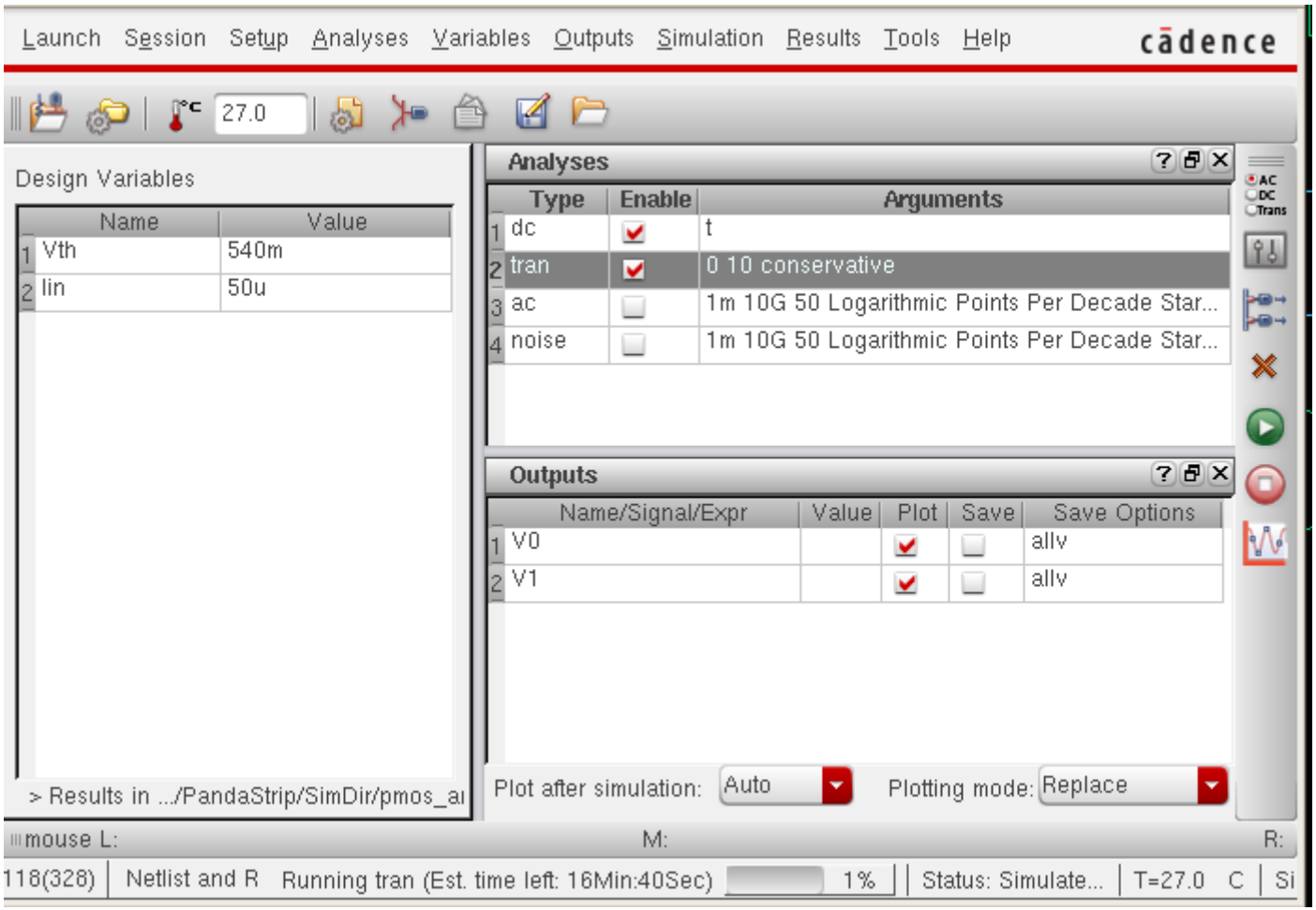
Pseudo Random Bit Sequence (PRBS): 320 Mbit/s, 640 Mbit/s, 1 Gbit/s

Transient noise

Corner Analysis (Monte Carlo simulations, temperature variations, Etc..)

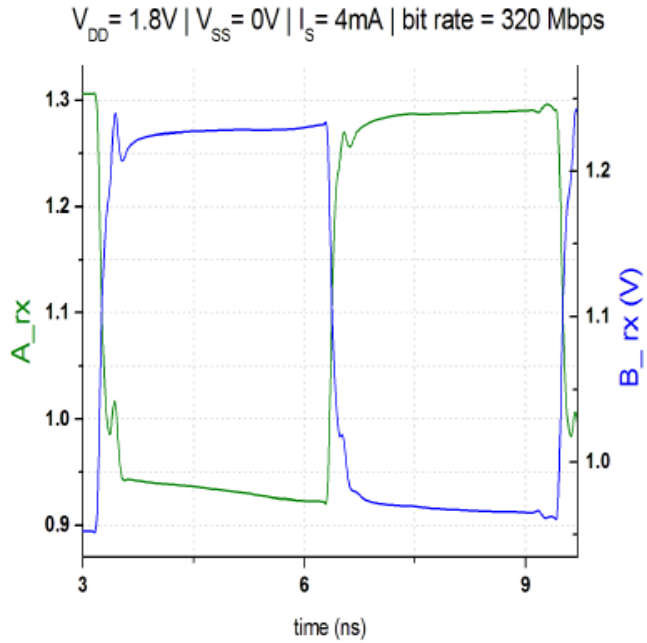
Design Steps



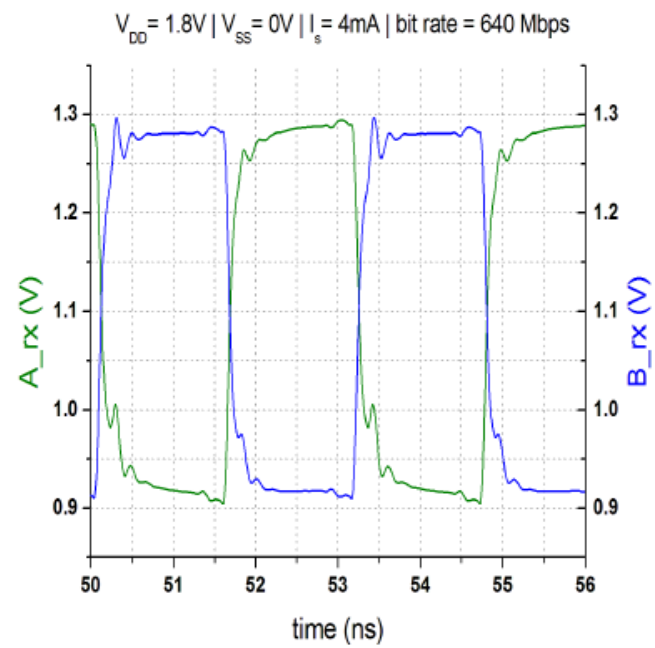


Cadence Tools

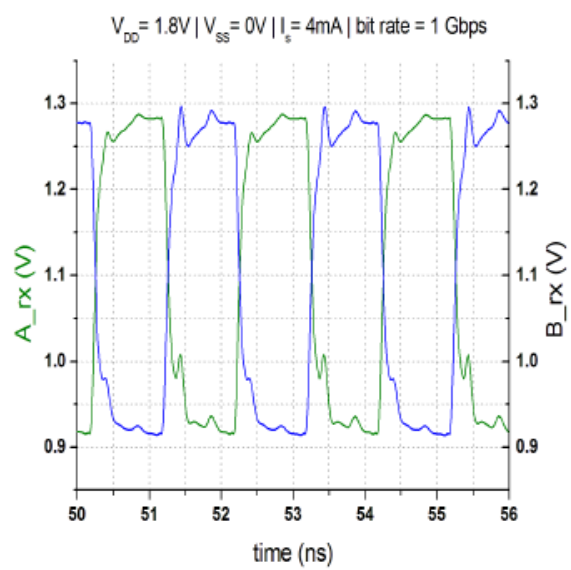
Simulated Square Waves



(a) Simulated 320 Mbit/s square wave

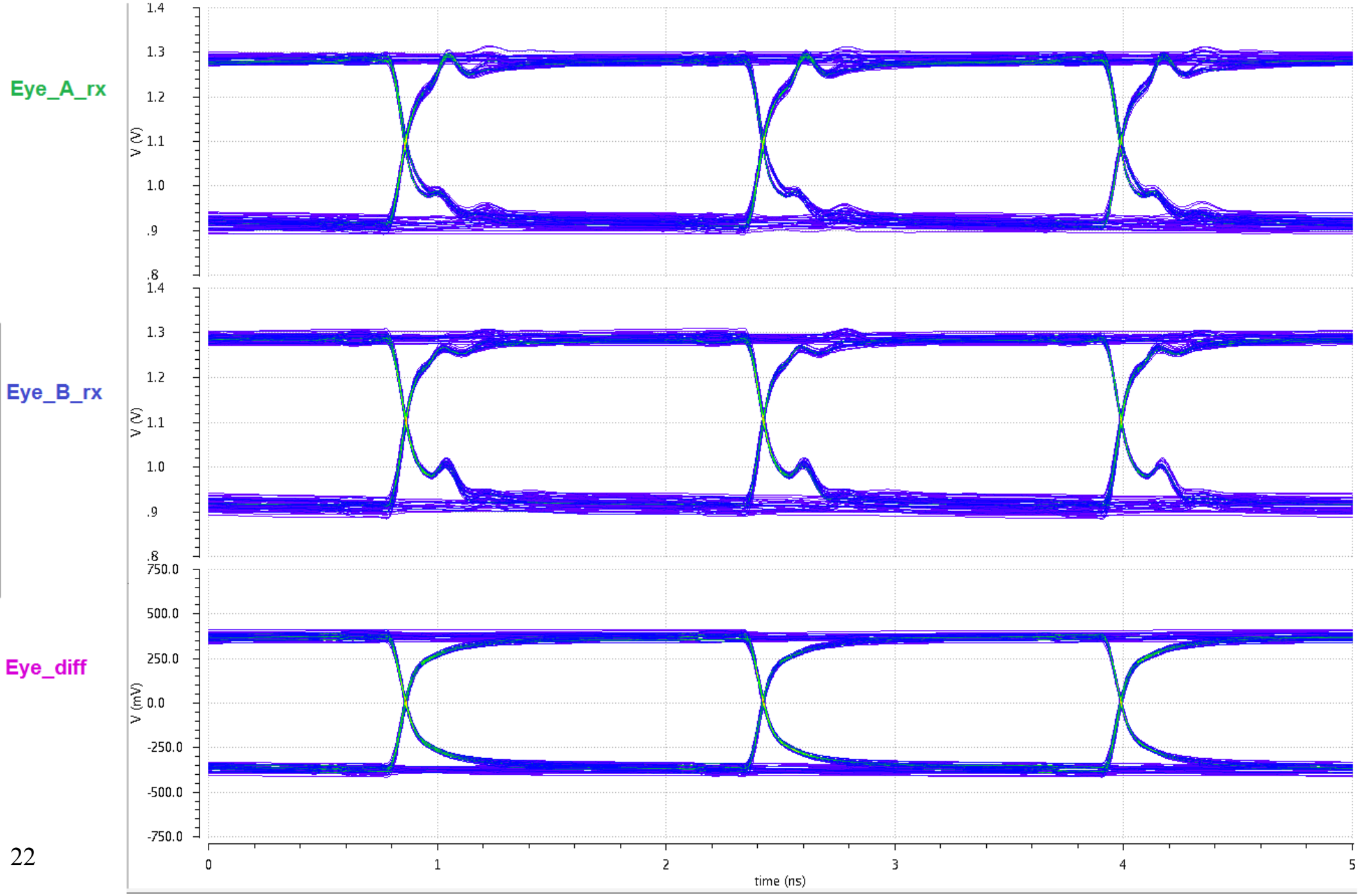


(b) Simulated 640 Mbit/s square wave



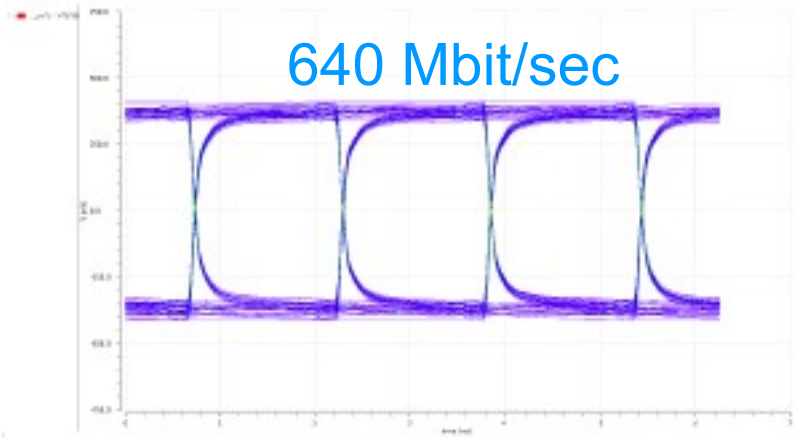
(c) Simulated 1Gbp/s square wave

640 Mbit/sec PRBS – Eye Diagrams

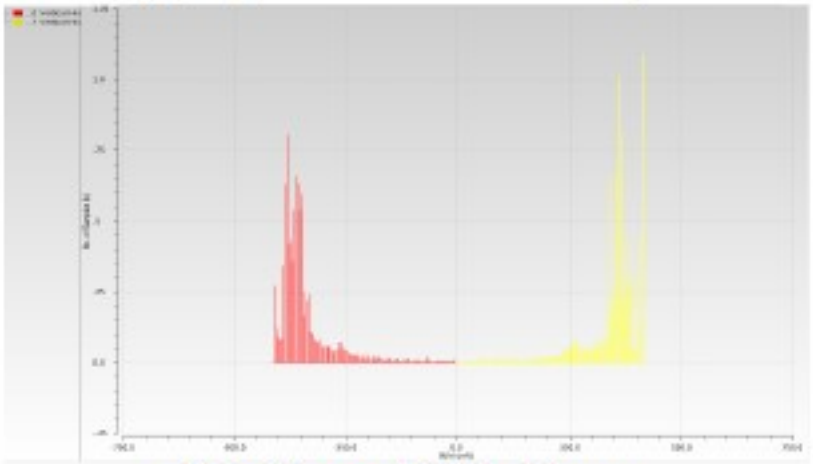


Eye Diagrams of the outputs difference – IS = 4mA

640 Mbit/sec

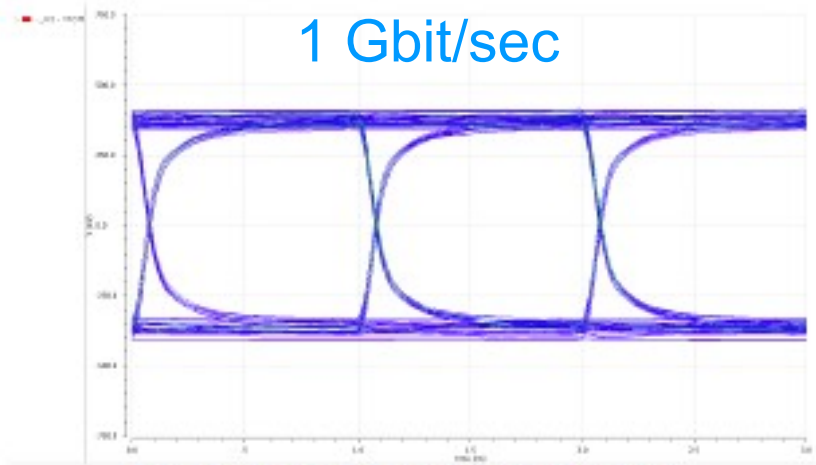


(a) Eye Diagram of the difference between the driver outputs

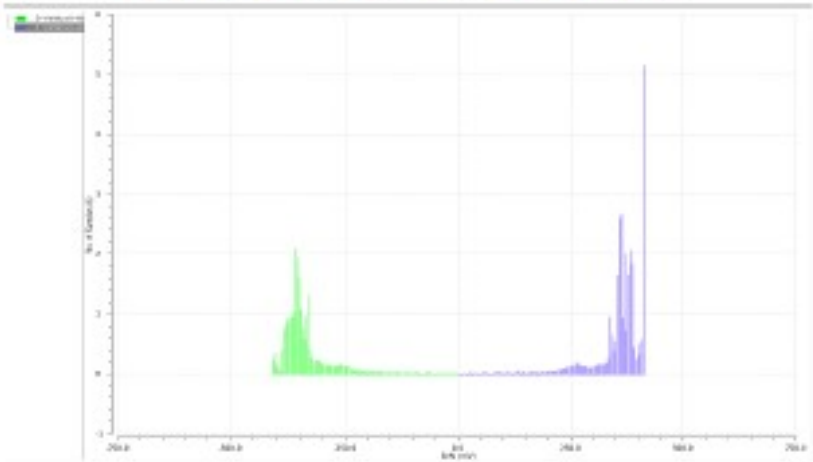


(b) Vertical Histograms - The number of Bins is 100

1 Gbit/sec



(a) Eye Diagram of the difference between the driver outputs



(b) Vertical Histograms - The number of Bins is 100

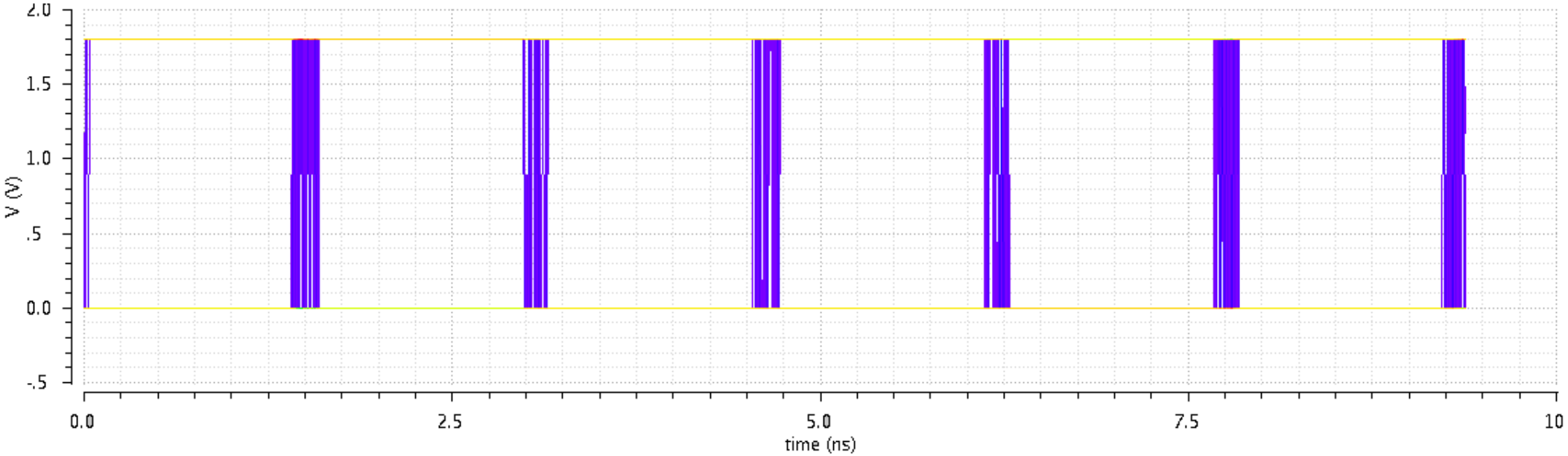
Eye amplitude = 0.5 V

T_j = 13 ps

Eye amplitude = 0.6 V

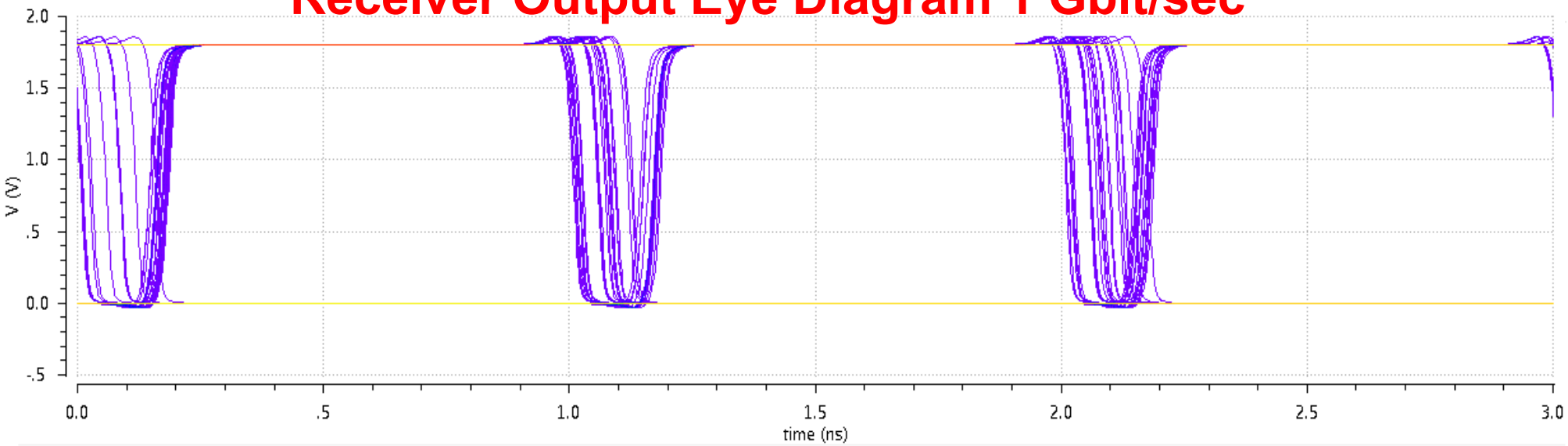
T_j = 21 ps

Receiver Output Eye Diagram 640 Mbit/sec

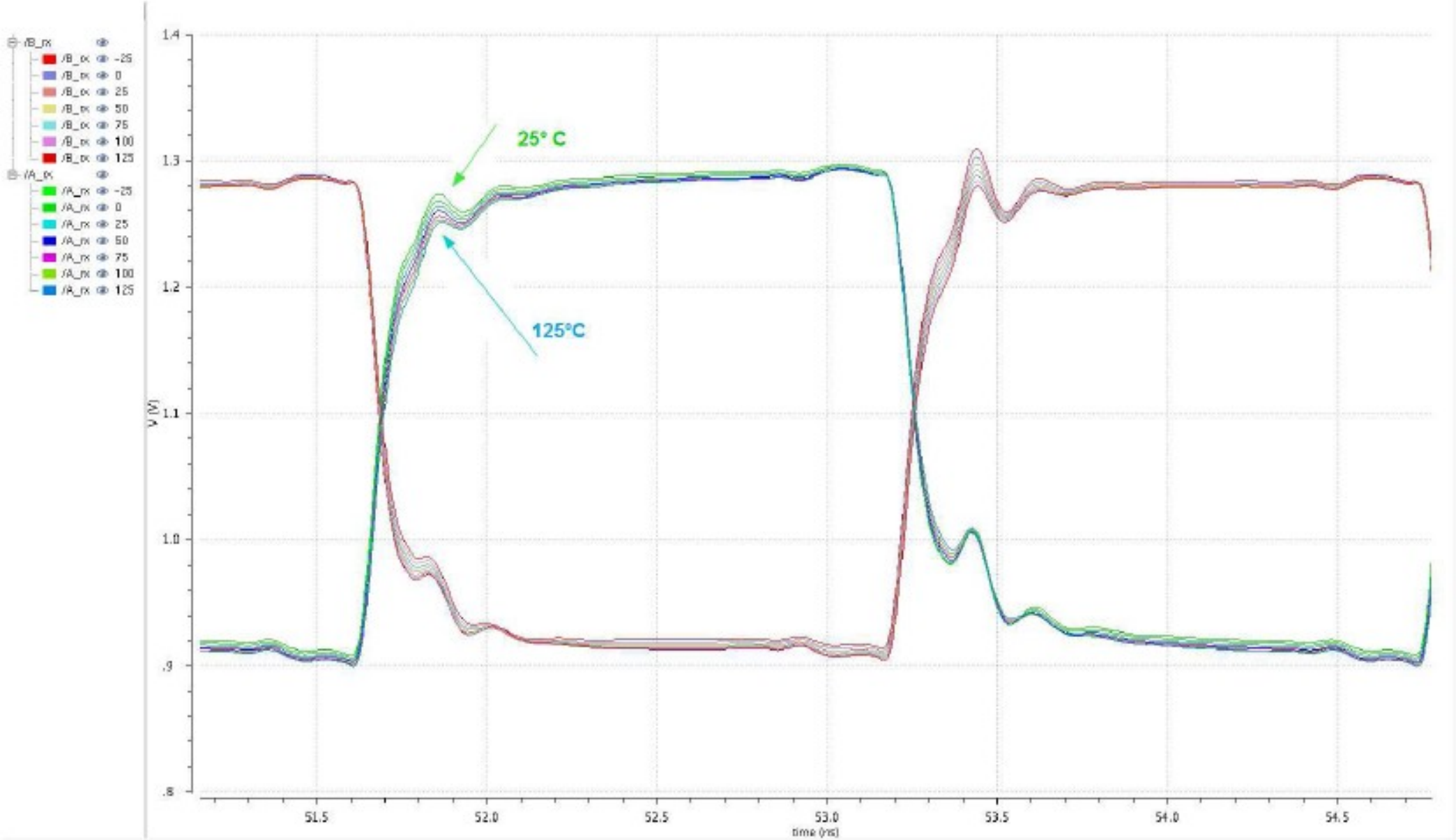


T_j~ 330 ps

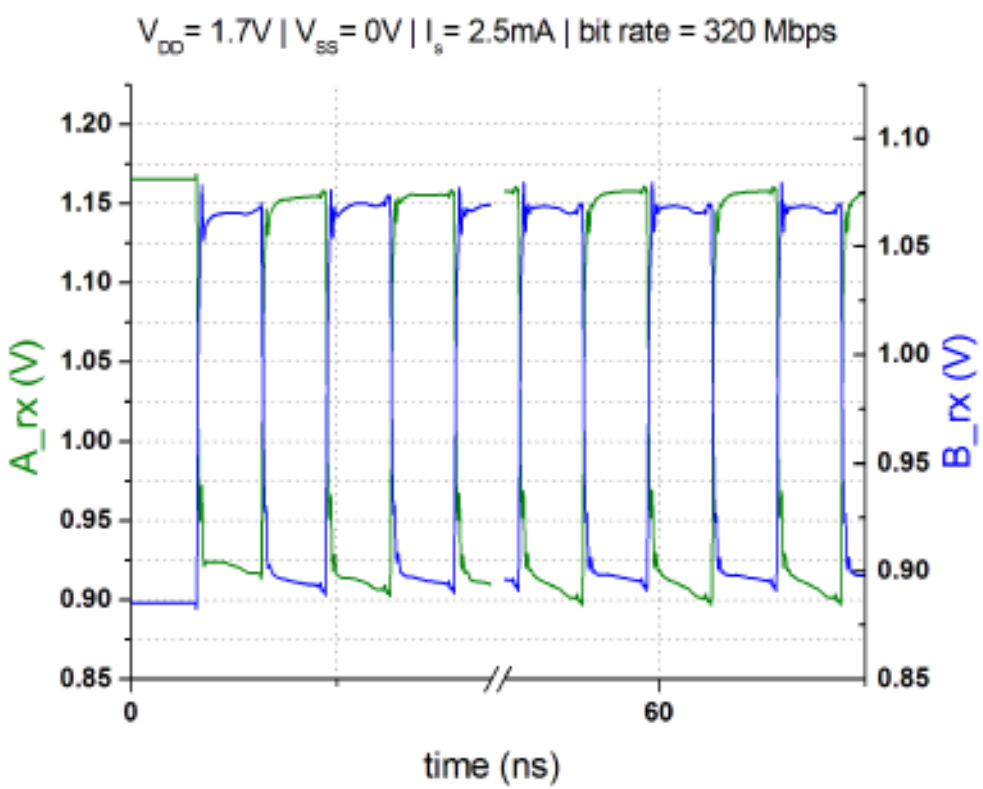
Receiver Output Eye Diagram 1 Gbit/sec

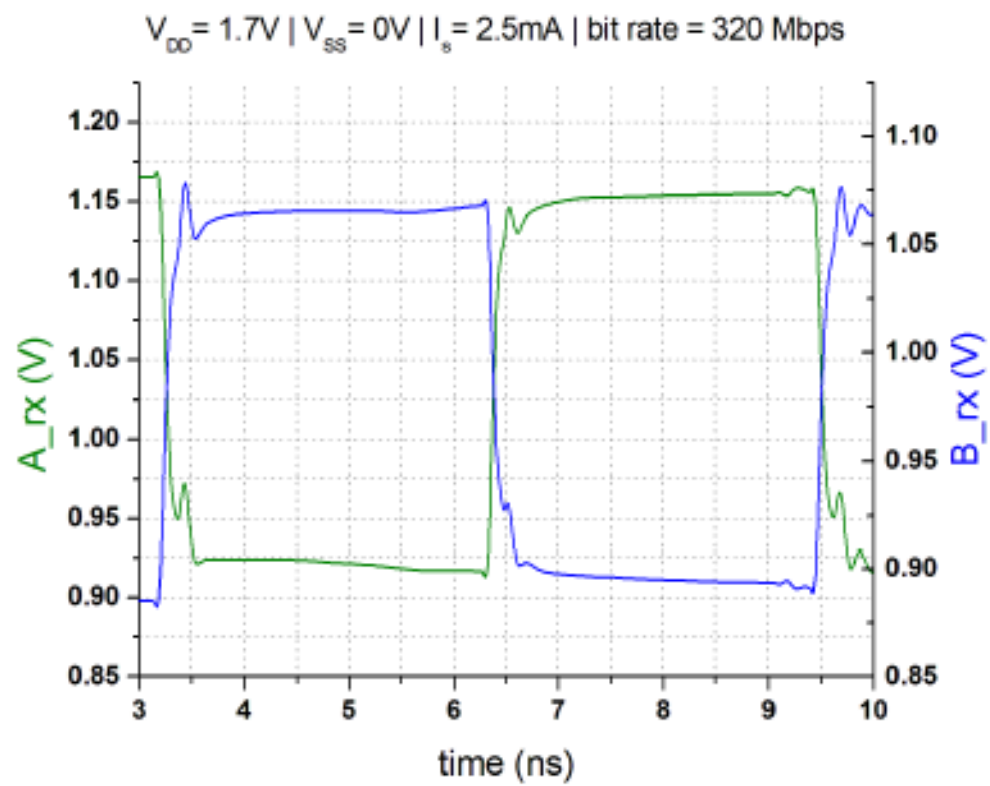


Simulated 640 Mbit/sec Square Wave – Temperature Variations (-25°C – 125 °C)

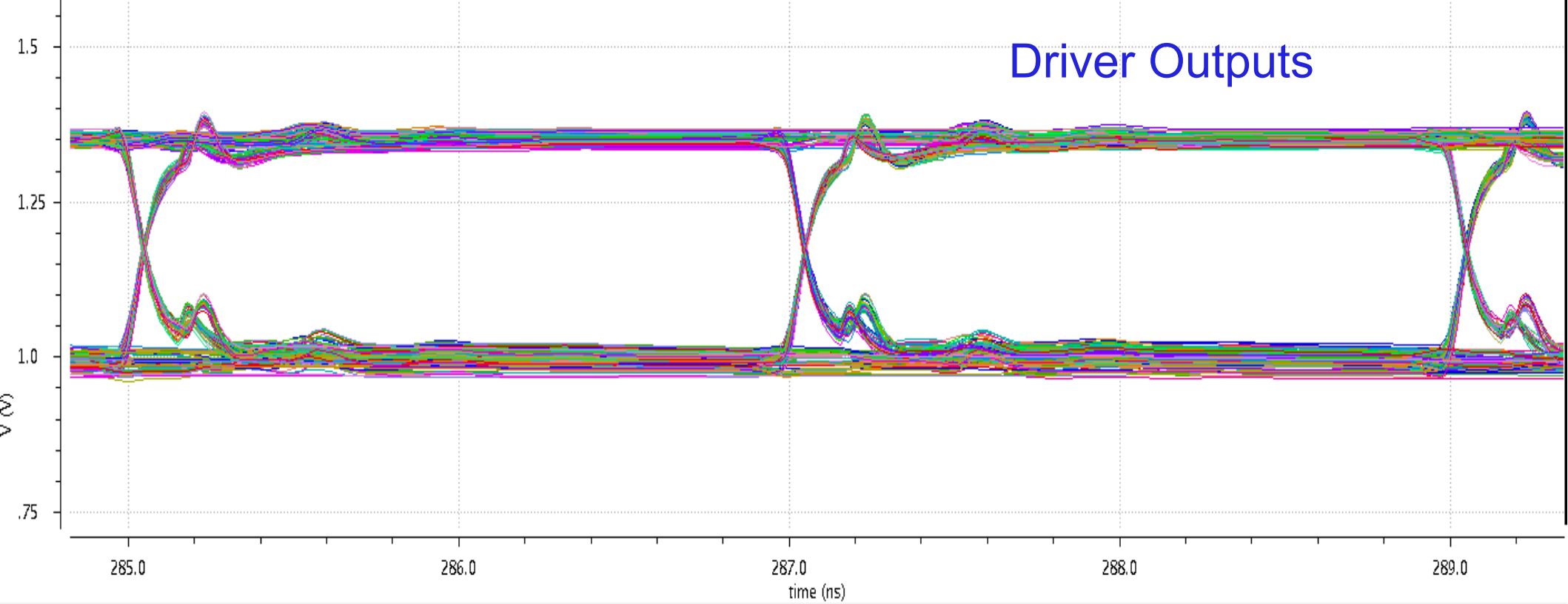


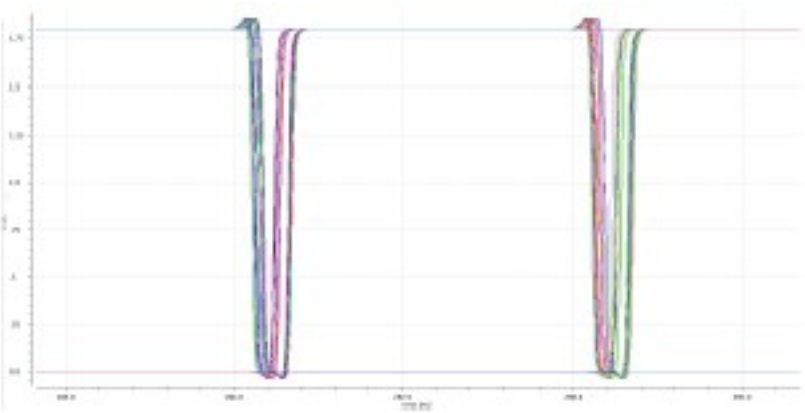
Voltage Supply Variation: VDD = 1.7 V





Simulated 320 Mbit/s Square Wave





Receiver Output

Monte Carlo Simulation

1Gbit/s PRBS

Conclusioni

Link LVDS in 0.18 µm Q-well CMOS technology with 1.8 V supply voltage.

- Transmitter 1 – no satisfactory perfomances already to 320 Mbit/s
- Transmitter 2 – good performance up to 1 Gbit/s
- Receiver – adequate for less than 1Gbit/s
- Ready for the production

Grazie per l'attenzione