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Study of an FPGA interface for a serial communication link at high speed

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Abstract

The GBT project ("GigaBit Transceiver"), born at CERN in view of the LHC upgrade, has been developed to provide an innovative and higher performing data transmission between on-detector and off-detector components in high energy physics experiments. The purpose of this architecture is to establish a point-to-point, bidirectional optical and serial connection with a large data rate (4.8 Gbit/s), to be used simultaneously for data readout, trigger and timing control and experiment monitoring. Since the counting room and front-end electronics are placed in different radiation environments, the GBT system is implemented by a combination of custom developments and commercial components (FPGAs).
In this work, the GBT project is applied to the readout chain of the hybrid pixels modules of the microvertex detector for the $\overline{\text{P}}$ANDA experiment. After a brief introduction about the experiment (Chapter 1) and the communication link description (Chapter 2), the third chapter introduces and analyses the GBT project, focusing on the communication protocol and on the structure of the GBT-FPGA Firmware project. The forth and fifth chapters deal with the GBT-FPGA code optimization for the specific application, the implementation on hardware and the performed tests. These consists in debugging the circuit, directly inspecting the internal signals, and in transferring data via an Ethernet port, through a LabView interface. In the end, the characterization of the pixel readout circuit is described (Chapter 6), with a particular attention to the last ASIC solution designed at INFN-Torino for the sensor readout of the hybrid silicon pixel (ToPix v4).
This research has been carried out at the Electronics Laboratory of INFN-Torino.

Abstract

Il progetto GBT ("GigaBit Transceiver") nasce al CERN in vista dell'upgrade di LHC, con l'intento di fornire un sistema di comunicazione innovativo e più performante per la trasmissione di dati dall'interno all'esterno del rivelatore nell'ambito degli esperimenti di fisica delle alte energie. Tale architettura si propone di stabilire una connessione puntuale, bi-direzionale e ottica, che possa trasmettere in seriale simultaneamente dati, informazioni sul tempo e sul trigger e informazioni di controllo con un ampio data rate (4.8 Gbit/s). Poichè l'elettronica di front-end e quella della componente esterna al rivelatore sono soggette a differenti condizioni di irraggiamento, il sistema GBT è implementato da una combinazione di componenti specifiche e dispositivi commerciali (FPGA).
In questo lavoro il progetto GBT è applicato alla catena di readout dei moduli a pixel ibridi del rivelatore a microvertice dell'esperimento $\overline{\text{P}}$ANDA. Dopo una breve introduzione sull'esperimento (Capitolo 1) e la descrizione del canale di comunicazione utilizzato (Capitolo 2), il terzo capitolo introduce e analizza il progetto GBT, concentrandosi sul protocollo di comunicazione e sulla struttura firmware del progetto GBT-FPGA. Il quarto e il quinto capitolo trattano l'ottimizzazione del codice del GBT-FPGA per la specifica applicaazione, l'implementazione su hardware e i test svolti. Questi consistono nel debug del dispositivo attraverso l'ispezione diretta dei segnali interni e nel trasferimento di dati da FPGA a computer via Ethernet, attraverso una interfaccia Labview. Infine, l'ultimo capitolo presenta alcuni test per la caratterizzazione del circuito di readout per i pixel ibridi, con attenzione particolare all'ultima soluzione ASIC per il readout del sensore a pixel ibridi disegnato presso l'INFN di Torino (ToPix v4).
Il lavoro è stato condotto in collaborazione con il laboratorio di elettronica dell' INFN di Torino.

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Chapter 1

$\overline{\text{P}}$ANDA experiment

The $\overline{\text{P}}$ANDA Experiment will be one of the key experiments of the FAIR (Facility for Antiproton and Ion Research) complex, which is under construction on the GSI Helmholtzzentrum für Schwerionenforschung area in Darmstadt, Germany. The experiment's main goal, as the acronym "*antiProton ANnihilation at DArmstadt*" suggests, is the study of antiproton-proton annihilations and reactions of antiprotons with nucleons in heavy nuclear targets, in order to explore the nature of the strong interaction in the non-perturbative regime and to obtain a significant progress in our understanding of the quantum chromodynamics (QCD) spectrum and hadron structure. This is made possible by the technological progress of the FAIR facility.

FAIR is a multi-purpose accelerator facility, built by an international cooperating community of countries and scientists to study a wide range of physics topics, from atomic and plasma physics to nuclear and hadron structure. The present structure will be upgraded in order to obtain a new state-of-the-art, multipurpose accelerator facility, whose core is a double-ring accelerator (SIS100 heavy ion synchrotron) with a complex system of cooler and storage rings. Thanks to SIS100, the parallel operation of different scientific programmes can be realised (an overview of the project is given in Fig. 1.1).

The new complex will be able to deliver protons, antiprotons and ion beams, all characterized by high energy, high intensity and high quality, which are essential properties for high precision physics esperiments. The protons will be accelerated in the linear accelerator LINAC up to 70 MeV, in the SIS18 synchrotron at 4 GeV and then in the SIS100 ring at 30 GeV. Reached this energy, the protons will be sent on a copper target and the antiprotons will be produced by the collision. The antiprotons, collected in the CR (Collector Ring) and cooled in the RESR (Recuperated Experimental Storage Ring) , will finally be injected into the HESR (High Energy Storage Ring) with a momentum of 3.7 GeV/c; here protons could be accelerated or decelerated in a momentum range between 1.5 GeV/c and 15 GeV/c by

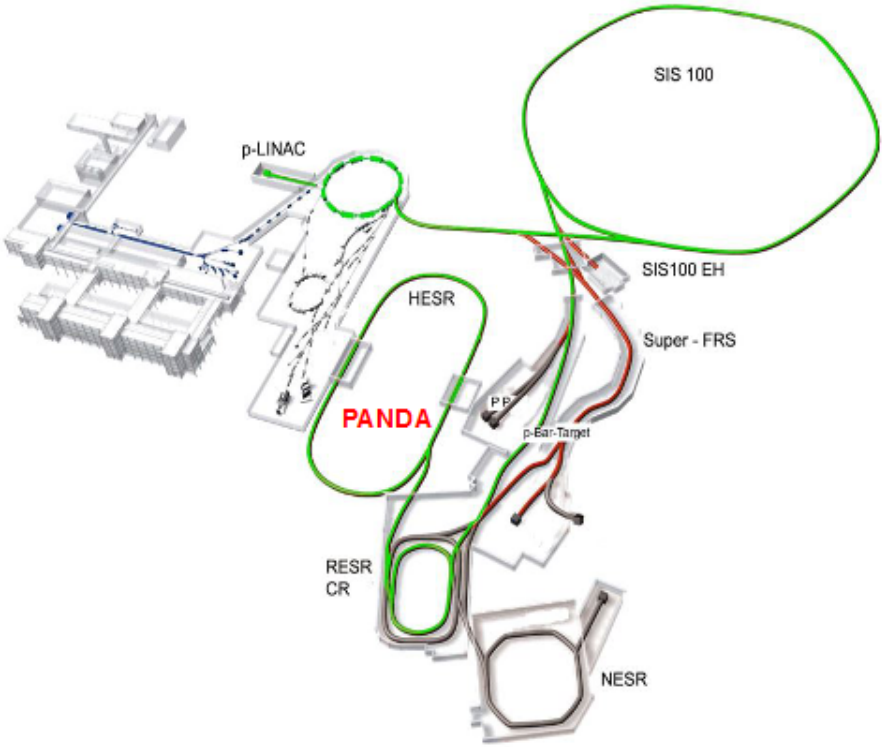


Fig. 1.1 FAIR layout; the new facility is highlighted in green, the pre-existing one in blue.

Radio Frequency (RF) cavities. The storage ring will be able to operate in two different modes: with high luminosity ($2 \cdot 10^{32}$ cm^{-2}s^{-1} and resolution of $\frac{\delta p}{p} = 10^{-4}$), or with high resolution ($\frac{\delta p}{p} = 10^{-5}$ and a luminosity of $2 \cdot 10^{31}$ cm^{-2}s^{-1}).

1.1 Physical case

The $\overline{\text{P}}$ANDA programme encompasses various topics related to the properties of the strong interaction: from the charmonium spectroscopy to the search for exotic hadrons and the study of nucleon structure, from the study of in-medium modifications of hadron masses to the physics of hypernuclei (see Fig. 1.2). To explore the broad physics programme, a state-of-the-art general purpose detector has been devised to study annihilation reactions of antiprotons with protons ($\overline{\text{p}}$p) and in nuclear matter (pA). The principal aspects of $\overline{\text{P}}$ANDA physical program are listed in the following paragraphs [18].

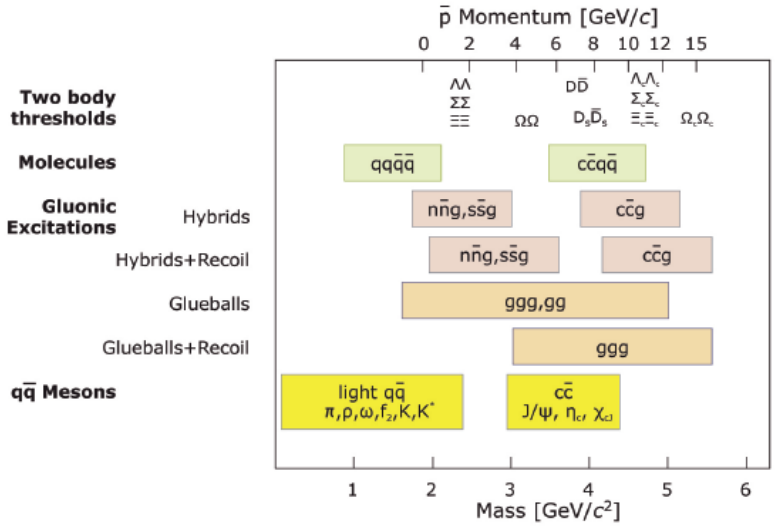


Fig. 1.2 Accessible mass range of hadrons for $\overline{\text{P}}$ANDA. The upper scale indicates the corresponding antiproton momentum.

Charmonium spectroscopy

Charmonium ($c\bar{c}$) spectroscopy allows the precise measurement of mass, width and decay branches of all charmonium states, to extract information on the quark-confining potential. Even though the 8 charmonium states below open charm threshold are known, the measurements of their parameters is not complete. Instead, above threshold very little is known, but recent findings of states around 4 GeV/c^2 show that the spectrum yields much more than has been expected.

At full luminosity, $\overline{\text{P}}$ANDA will collect several thousand $c\bar{c}$ states per day, making possible the measurement of masses with an accuracy of the order of 100 keV and widths up to 10%. The measurement will be lead accelerating the p beam to the energy of the resonance, which will be subsequently scanned by changing the beam momentum in small steps. The benefit in using protons is that $\overline{\text{p}}$p reactions allow to produce all combinations of the initial quantum numbers and not only as decay products of other particles (as in $e+e-$ annihilation). This allows us to obtain a more precise and detailed knowledge of all states below and above open charm threshold, fundamental for a better understanding of the confinement part of the QCD potential.

Gluonic excitations

The search for gluonic excitations has been one of the main challenges of hadron physics, i.e. hadrons in which the gluons can act as principal components and which cannot be fully

described in terms of quantum numbers. Two categories of states for gluonic hadrons can be itemized:

- glueballs: states where only gluons contribute to the overall quantum numbers,
- hybrids: states where in a $q\bar{q}$ bound state the gluons carry additional excitation degrees of freedom.

These exotic hadrons are hypothetical color neutral particles not predicted by the quark model with exotic quantum numbers that, in the Standard Model, are forbidden for normal mesons and other fermion-antifermion systems . Antiproton-proton annihilations provide a very favourable environment to look for gluonic hadrons.

Multi-quark states

These are states which cannot be assigned to an arrangement of three quarks or a $q\bar{q}$ pair as the baryons and mesons. As in the gluonic excitations mentioned above, their clearest signature would be possible exotic quantum numbers. They could be interpreted as hadronic molecules or octet couplings.

Open charm spectroscopy

The HESR, running at full luminosity and at antiproton momenta larger than 6.4 GeV/c, will produce a large number of D meson pairs. The high yield and the well defined production kinematics of D meson pairs would allow a significant charmed meson spectroscopy programme which would include, for example, the rich D and D_s meson spectra.

Study of hadrons in nuclear mattery

The aim of the study of medium modifications of hadrons embedded in hadronic matter is to understand the origin of hadron masses in the context of spontaneous chiral symmetry breaking in QCD and its partial restoration in a hadronic environment. The high intensity of the antiproton beam (up to 15 GeV/c) will allow an extension of the study from the widely studied light quark sector to the charm sector for hadrons with both hidden and open charm. The in-medium masses of these states are expected to be affected primarily by the gluon condensate. Moreover, J/ψ and D meson production cross sections in $\bar{\text{p}}$p annihilation on a series of nuclear targets can be studied. The comparison of the resonant J/ψ yield when using different nuclear targets allows to deduce the J/ψ nucleus dissociation cross section,

which is a fundamental parameter to understand J/ψ suppression in relativistic heavy ion collisions.

1.2 $\overline{\text{P}}$ANDA detector

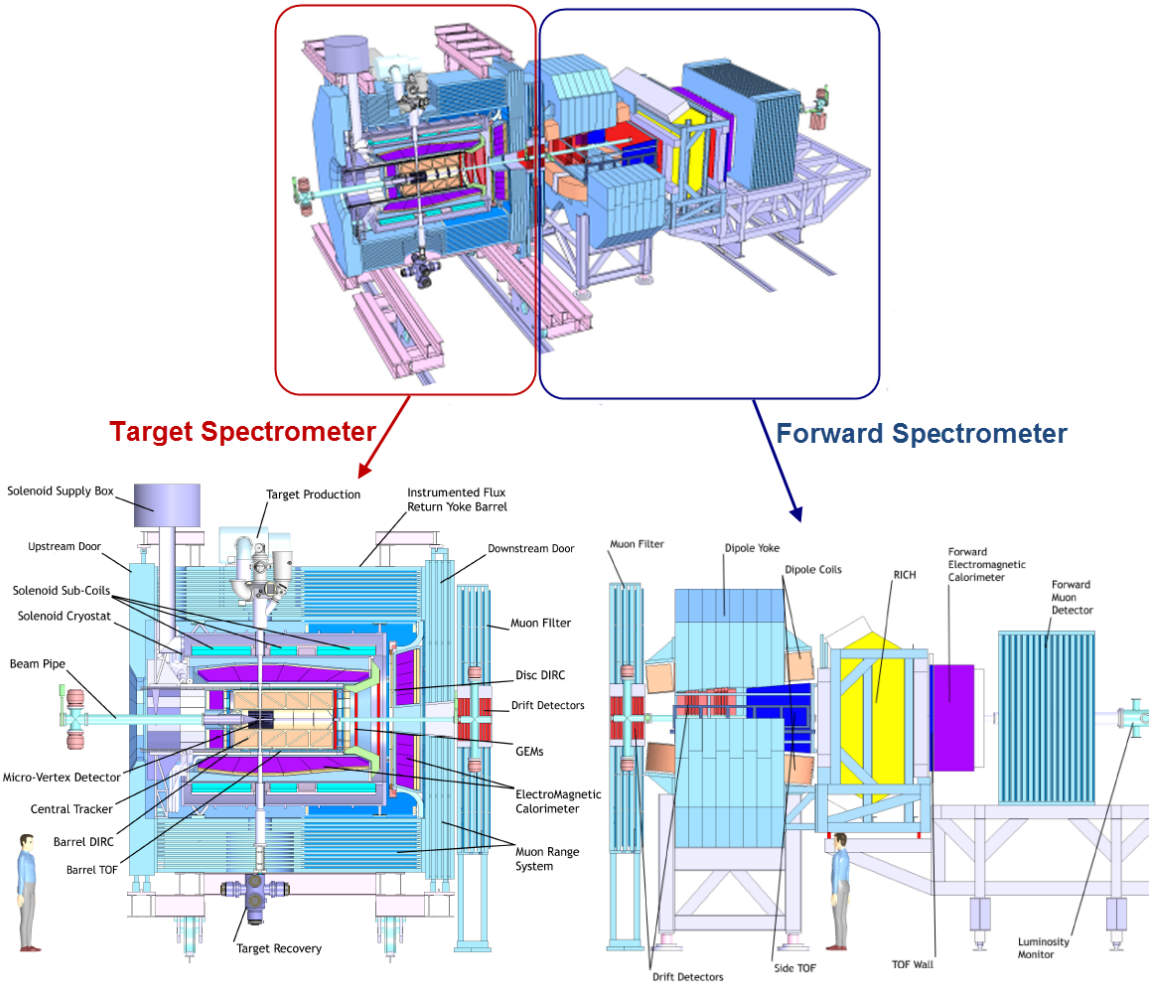


Fig. 1.3 $\overline{\text{P}}$ANDA detector layout; the Target Spectrometer, surrounding the interaction region, and the Forward Spectrometer in the forward region are rappresented. The HESR antiproton beam enters the apparatus from the left side.

To realize the described physics program, the $\overline{\text{P}}$ANDA detector satisfies the following tasks:

- full angular coverage and good angular resolution for charged and neutral particles;

- particle identification in a large range of particles (leptons, muons, kaons, etc.) and energies;
- high resolution in a wide range of energies;
- high rate compatibility;
- triggerless readout.

$\overline{\text{P}}$ANDA consists of two spectrometers: a *Target Spectrometer* (TS) and a *Forward Spectrometer* (FS). The TS, surrounding the interaction region with a superconducting solenoid, is able to detect particles at large polar angles; while the FS with a dipole is used for small angle tracks. The spectrometers singularly allow the detection, identification, and energy/momentum reconstruction for charged and neutral particles, while their combination takes into account the wide range of energies and momenta. According to the project, the anti-proton beam interacts with the target at the cross point with the target pipe and the emitted particles are measured in the TS if they have a polar angle larger than 10° and 5° in the horizontal and vertical direction respectively, otherwise they are collected in the FS (Fig. 1.3).

In the space between the downstream side of the FS and the dipole , a *Luminosity Monitor* is placed, to reconstruct the direction of elastically scattered antiprotons with polar angle between 3 and 8 mrad with respect to the beam axis [12].

1.2.1 Target Spectrometer

The Target Spectrometer is an onion-shell structure consisting of several detectors placed around the interaction region with a cylindrical symmetry around the beam pipe; the beam pipe intersects the target pipe in the centre of the spectrometer defining the interaction region. The whole structure is surrounded by a superconducting solenoid magnet, giving a 2 T magnetic field.
The TS main components are described in the next paragraphs.

Tracking Detectors

The main goal of the tracker is to reach:

- a momentum resolution of the order of percent in tracking the expected high fluxes of particles, covering nearly the complete solid angle around the interaction region;

- a good efficiency in the reconstruction of secondary vertexes, with a wide range of decay lengths spread over different orders of magnitude (from the order of cm for strange hadrons to the order of tens of μm for charmed mesons).

For these purposes, the tracker consists of three separate detectors: a Micro Vertex Detector (MVD) surrounding the interaction point, a Straw Tube Tracker (STT) around it and three sets of Gas Electron Multiplier (GEM) trackers covering the forward direction [9].

Micro Vertex Detector

The Micro Vertex Detector (MVD), shown in Fig. 1.4, is the innermost $\overline{\text{P}}$ANDA detector and is optimized for the detection of secondary vertices and maximum acceptance close to the interaction point, in order to reconstruct the decays of short-lived particles [19]. The MVD layout foresees four concentric barrels surrounding the interaction region and six wheels in the forward direction, on which are placed radiation hard silicon pixel detectors with fast individual pixel readout circuits and silicon strip detectors (the two inner barrels and the most inner of the disks are covered by the silicon pixels, the other portions by the strips).
A deepened description of the MVD is reported in paragraph 1.3.

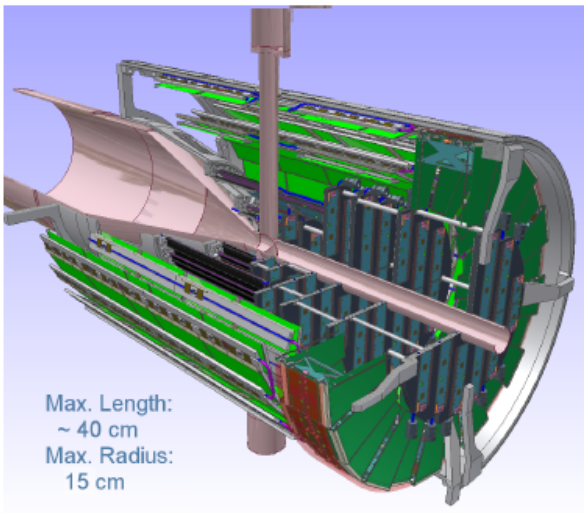


Fig. 1.4 Micro Vertex Detector section; the structure of concetric barrels and forward disks is visible.

Straw Tube Tracker

The Straw Tube Tracker (STT) is designed with the prospect of a good detection efficiency for secondary vertices which can occur outside the inner vertex detector, in combination with the MVD. The STT consists of 10mm-diameter tubes of aluminized Mylar (straws), self supporting by the operation at 1 bar overpressure, and with a central anode of 20 μm gold plated tungsten wire. The straws are arranged in cylindrical layers around the beam pipe

at radial distances between 15 cm and 42 cm with an overall length of 150 cm [19]. The gas chosen for the straw tubes is a mixture of 90% Ar and 10% CO_2 and it is a compromise between the minimization of the material budget and the quality of the spatial resolution. At the extremes of the gas filled volume a potential difference is applied: when a crossing charged particle ionizes the gas, under the effect of the field the ion drifts towards the tube and the electron drifts towards the anode; in this way an avalanche multiplication in the immediate vicinity of the wire is created and it induces an electric signal.
The gain is no greater than 10^5 to warrant long term operation; the expected spatial resolution is of about 150 μm in $r-\phi$ direction and of about 3 mm in z direction.

Gas Electron Multiplier

The Gas Electron Multiplier stations, placed 1.1, 1.4, 1.9 m downstream of the target, are used to detect the particles emitted at angles below 22°, which do not enter the STT. Each of the three station consists of double planes with two projections per plane and is equipped with Gaseous micro-pattern detectors based on Gas Electron Multiplier (GEM) foils as amplification stages. These detectors have a sufficiently high rate capability to cope with the enhanced particle flux in the forward detector region.

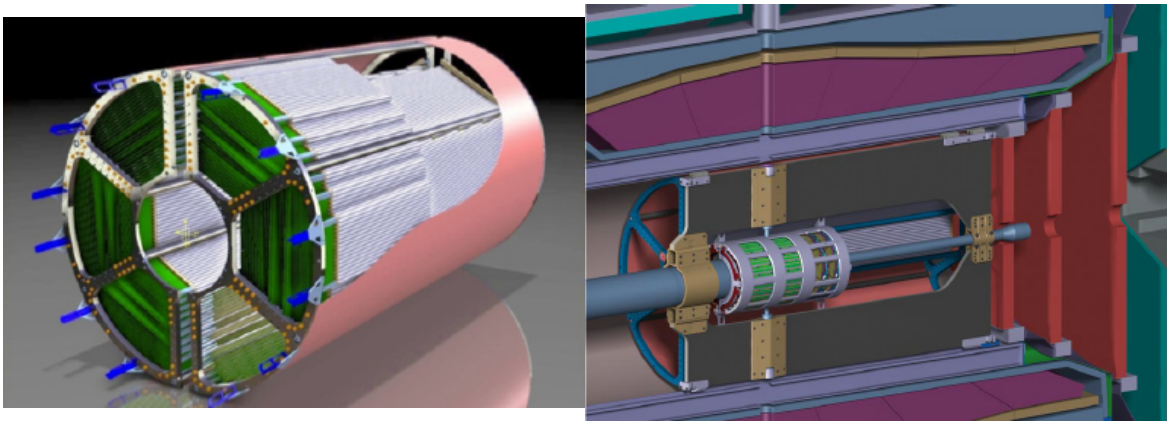


Fig. (a) Fig. (b)

Fig. 1.5 a) Straw Tube Tracker (STT) layout; b) Gas Electron Multiplier (GEM) layout, next to the other components of the $\overline{\text{P}}$ANDA tracking system.

Particle identification system

Particle identification for hadrons and leptons over a large range of solid angles and momenta is an essential requirement for meeting the $\overline{\text{P}}$ANDA physics objectives and in many cases

only the combination of information from many detectors can provide a complete particle identification. There are several dedicated items which, complementary to the other detectors, provide means to identify particles.
The experiment foresees: a Cherenkov detector composed of a barrel part and a forward end cap and a Time-of-Flight barrel, able to cover most of the momentum spectrum. Moreover, in certain ranges particle identification will be done by using energy losses in the detectors (e.g. MVD for slow charged particles).

Cherenkov detectors
The Cherenkov detectors inspect particles in a momentum range between 800 MeV/c and 5 GeV/c; their operating principle is based on Cherenkov radiation, that is emitted when a charged particle reaches a velocity greater than the speed of light in the traversed medium (i.e. $\beta > \beta_{threshold}$, with $\beta_{threshold} = 1/n$ and $n =$ refraction index of the medium).
The direction of the emitted radiation is given by the formula: $\theta = arcos(1/(\beta n))$; knowing the particle momenta and measuring the θ angle, the particle can be identified.
The project foresees a system of DIRC (Detection of Internally Reflected Cherenkov light), Fig. 1.6, consisting in two different parts [22]:

- The *Barrel DIRC* covers the polar angles between 22° and 140° and is expected to provide pion-kaon separation for particle momenta up to 3.5 GeV/c. Its concept is based on a BaBar DIRC and consists of 80 slabs of fused silica (artificial quartz), surrounding the beam line at a radius of 45 cm - 54 cm;

- The *Forward End-Cap DIRC* is made of the same material employed for the Barrel DIRC and it is projected to detect particles between 5° and 22°. This detector has the shape of an octagonal disk and provides pion – kaon separation up to 4 GeV/c momenta.

The advantages of this type of detector are the compact design and the possibility of a $3-$dimensional spatial reconstruction from the expected light pattern.

Time-of-Flight detector
The Time-of-Flight (ToF) detector covers angles between 22° and 140°, using a barrel layout around the central tracker at $42-45$ cm radial distance. The TOF main purpose is to identify slow particles at large polar angles, with a good time resolution (between 50 and 100 ps).

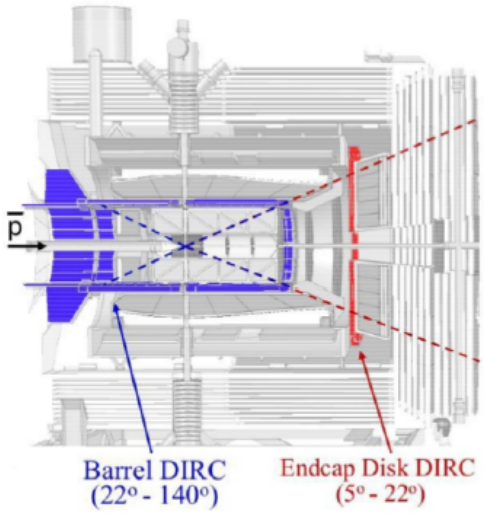


Fig. 1.6 DIRC layout; the barrel DIRC and the Forward End-Cap DIRC are represented.

Electromagnetic Calorimeters

The Electromagnetic Calorimeters (EMC), showed in Fig. 1.7, consists in a barrel, a forward and a backward end caps, placed around the DIRC detectors. For the building of the EMC, in order to find a compromise between a high rate and a compact design, the project foresees a fast scintillator material with short radiation length (X_0) and a Molière radius. The EMC must have an energy resolution below 2% at 1 GeV; this is achievable thanks to the employed tapered crystals. With an inner radius of 57 cm the barrel part of the calorimeter requires 11360 tapered crystals with a front face of 2.1x2.1 cm^2 and a side of 20 cm (i.e. $22X_0$), while the backward and forward end caps respectively require 592 and 3600 tapered crystals. An ample area of photodiodes in the barrel and a vacuum phototriodes in the end caps complete the EMC structure.

Muon Detectors

The range system to detect muons consists in a series of aluminium rectangular Mini Drift Tubes (MDTs), which are drift chambers with additional capacitive coupled strips, used to provide a longitudinal information. Every tube is 16 cm wide, 2 cm thick and 2.5 m long. The muon detector is composed of two main parts:

- a *Barrel*, which is segmented in 13 MDT layers, alternated with iron layers (each strata is 3 cm thick); this segmentation allows to distinguish energy loss of muons and pions from background;

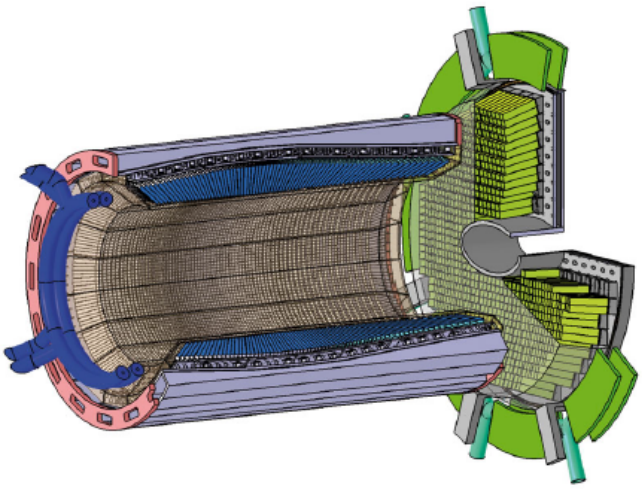


Fig. 1.7 EMC layout; the barrel is represented in blue and the forward end cap in green.

- a *Forward end cap*, which is made of thicker absorber layers (6 cm), in order to absorb pions.

The project foresees an additional muon filter with four iron layers and five MDT layers to be placed between the target and the forward spectrometer, with the double aim to increase the muon detection and provide an additional magnetic screen between solenoid of the TS and the dipole magnet of the FS. The muons momentum is determined by the tracker of the Target Spetrometer. The information coming from the muon detectors will allow the determination of the position for matching with the tracker system and the ToF to suppress random coincidences. A further background suppression will be done through dE/dx information.

Hypernuclear detectors

Hypernuclear studies at $\overline{\text{P}}$ANDA require to remove the backward EMC and the MVD and to insert a dedicated setup, which consists in a modular structure. The first module is made of a primary carbon target, on which $\overline{\text{p}}$ at 3 GeV/c momentum interact to produce a large number of $\Xi\overline{\Xi}$ pairs, and a secondary active target consisting in a stratified structure of absorbing material and silicon microstrips along the beam pipe. The result is a copious production of double hypernuclei [13] [18]. The second module consists of the central tracker, used for detection of the products from the Ξ decay and of low momentum K+.
Finally, an existing and upgraded germanium-array is used for the spectroscopy of the nuclear decay cascades of hypernuclei.

1.3 Micro Vertex Detector

The MVD is the innermost detector of $\overline{\text{P}}$ANDA and its main task is to reconstruct primary and secondary vertex of particle decays and the momentum of charged particles, with high precision in space and time. In order to satisfy this task, the **requirements** for the MVD are:

- Spatial Resolution:
  a resolution not larger than 100 μm in z and about 60 μm in the r plane is required in order to resolve efficiently secondary vertexes;

- Time resolution and readout speed:
  a time resolution of about 6 ns is necessary to an efficient collection, considering that the average interaction rate is $2 \cdot 10^7$ s^{-1} and the mean time between two antiprotons annihilations is 50 ns. The readout system is triggerless and a 155.52 MHz clock is delivered to all detectors to allow continuous data collection;

- Particle identification:
  the particle identification is made possible by the measurement of the energy loss along the track, i.e. a measurement of the deposited energy in the MVD (see Fig. 1.8);

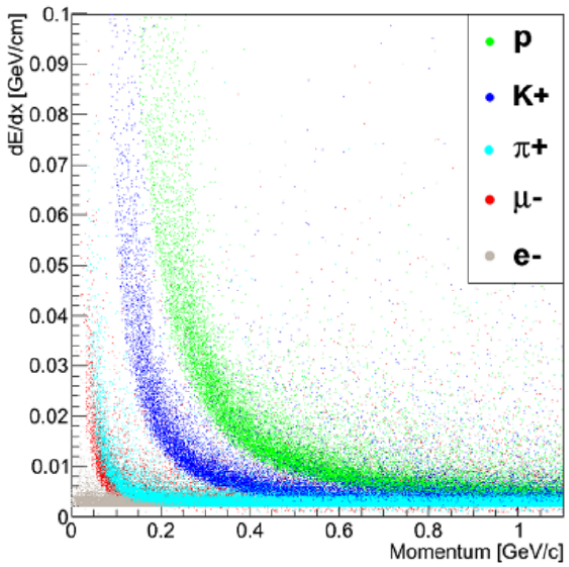


Fig. 1.8 Energy loss distribution in the MVD with respect to the momentum.

- Limited material budget:
  to optimise the radiation length the share of the material budget should not exceed 10% over all the detector acceptance. This is due to the large number of low momentum particles generated by decays, whose multiple scattering affects the MVD resolution;

- Radiation hardness:
  a good radiation hardness for detectors and front-end electronics is of high importance because of the close proximity to the interaction point;

- Geometrical constraints:
  minimum distance from the beam axis for the innermost layer of the MVD is given by the beam pipe outer radius (1 cm), while limit of the outermost layer by the inner radius of the central tracker (15 cm). Moreover the cone shape of the beam pipe in the backward direction is necessary to achieve the required vacuum in the interaction region.

To fulfil the physical necessities, a specific **layout** has been designed for MVD: the structure consists in four concentric barrels around the interaction point, coaxial to the beam line, and six transverse disks in the forward part. The pixel disks are of two different dimensions: the first two are smaller than the last four (respectively 75 and 150 mm of outer diameter). The structure has a maximum radius of 15 cm and an extension along the beam of 40 cm from interaction point. The detector is designed to provide some position information for tracks with a polar angle between 3° and 150°, and a minimum of four hit points for tracks between 9° and 140°:

- the *barrel part* covers polar angles between 40° and 150° and its dimension and position respects the MVD geometrical constraints (radius range between 2.5 and 13.5 cm);

- the *disk layers* covers polar angles between 3° and 40° and the first layer is positioned 2 cm beyond the interaction region.

The MVD layout is shown in Fig. 1.9.
The inner layers of the MVD (the first two barrels and the central area of forward disks) are instrumented with hybrid pixel detectors, able to support the high particle rate expected for the experiment, while the outer layers are covered with double-sided silicon strip detectors, whose main benefit is a lower material budget [1].
The hybrid pixel silicon detectors require $10.3 \cdot 10^6$ readout channels, fifty times more than the microstrip requirements ($2 \cdot 10^5$ readout channels).

1.3.1 Double-Sided Silicon Microstrip Detector

The wide use of silicon microstrip detectors in nuclear and particle physics experiments is due to their features: good spatial resolution, low material budget and good radiation

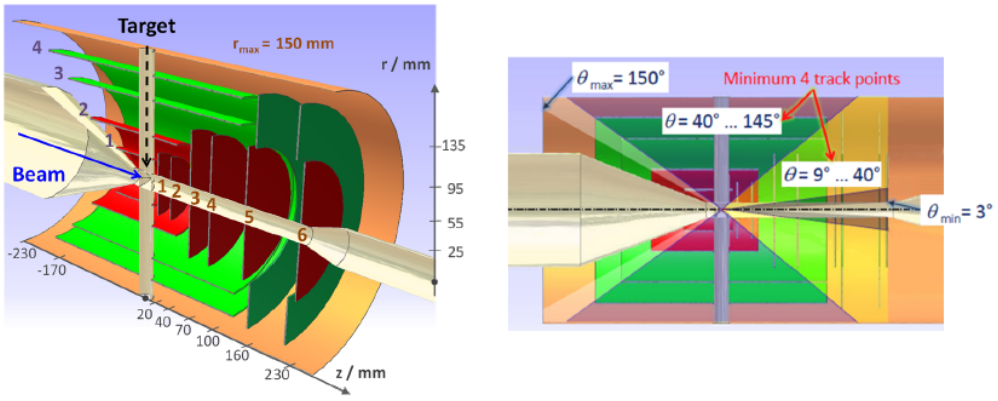


Fig. 1.9 MVD layout; in the left image: the parts equipped with silicon hybrid pixel sensors are coloured in red and those with silicon micro-strip detectors in green, while in the right image there is a side vision of the MVD, illustrating the polar angle coverage.

tolerance. The strips are realised in p^+ type silicon on the front side and in n^- type silicon on the back, both grown on n-type substrate. Since the strips are silicon sensors, their working principle is a reverse-biased junction, in which the produced electron-hole pairs are collected and then amplified by the readout electronics. To get a 2D spatial information, two strip layers, oriented respectively along the horizontal and vertical axis, are used.

In the PANDA experiment, in order to reduce the material budget, the two sets of strips are implemented on the same sensor, creating a Double-Sided Strip Detector (Fig. 1.10).

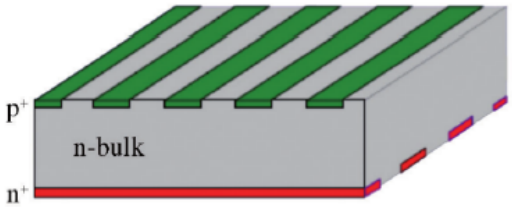


Fig. 1.10 Double-Sided Strip Detector structure.

The strips limit is the sustainable particle rate, lower than the pixels one, mostly due to the ghost hit effect, which takes play when two or more particles hit the detector at the same time. If two particles arrive on the sensor at the same time, four hits are reconstructed combining in different ways the x-y coordinates registered by the two layers, without possibility of discrimination of ghosts from real events. For this limitation, the strips detectors are used in the outer part of MVD where the density particle is lower.
In the structure of the MVD, as shown in Fig. 1.11, three different types of strips are foreseen:

- rectangular and square for the barrel part;

- trapezoidal for the disk part.

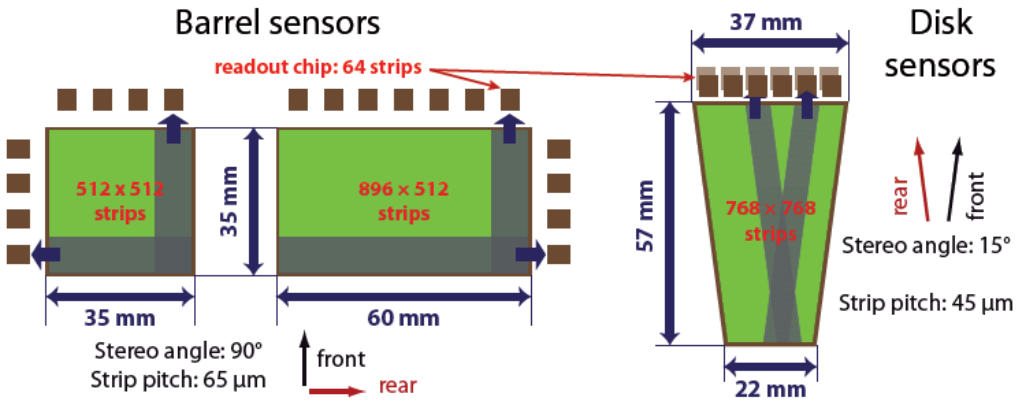


Fig. 1.11 Basic sensor geometry in the MVD strip part.

1.3.2 Hybrid Pixel Detector

The hybrid pixels technology has been largely used in high energy physics experiments, e.g. in LHC experiments, and has been chosen for $\overline{\text{P}}$ANDA since it satisfies the requirements for the vertex reconstruction: spatial resolution, timing precision and radiation hardness. The hybrid pixels detector is made of two different parts: a silicon sensor arranged in a 2-dimensional matrix of pixels and a readout chip, whose cells are singularly connected to each sensor pixels by a In or Sn-Pb bump (Fig. 1.12).

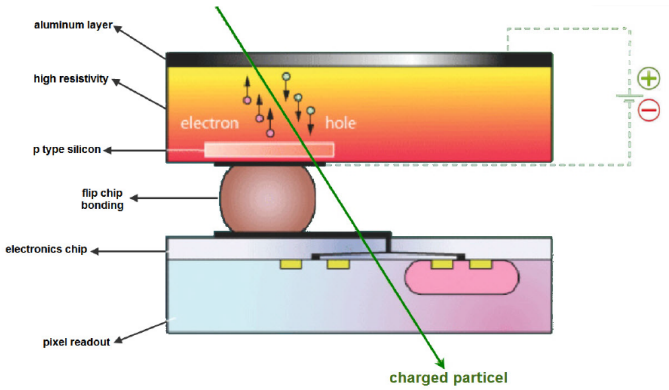


Fig. 1.12 Scheme of the Hybrid Pixel Detector elementary unit; on the top there is the reverse biased sensor, connected to the readout chip.

Silicon sensor

The working principle of the sensor is based on a reverse biased silicon diode: when a

charged particle enters the depletion region, it creates electron-hole pairs by ionization; the generated charge is gathered thanks to the voltage applied at the edge of the junction, creating a current. The signal is then collected and amplified by the readout electronics and transmitted outside the detector. The pixel detectors in $\overline{\text{P}}$ANDA use an n-type epitaxial silicon with high resistivity ($2 \div 4k\Omega\cdot$ cm), grown on a low resistivity ($0.01\Omega\cdot$cm) n^+ Czochralski substrate. A 100 μm x 100 μm pixels matrix (100 x 116 pixels) is realized on the wafer; each pixel consists of a p^+-type implant realized on the n-type epitaxial layer. Finally, the sensor will be surrounded by a p^+ guard ring [5], [34].
After the production, the Czochralski substrate will be thinned to achieve an overall thickness of 100 μm, allowing a good signal-to-noise ratio for particle identification studies and a good radiation tolerance.

Readout chip

The readout chip is an ASIC (Application-Specfic Integrated Circuit) called ToPix and developed in 130 nm CMOS tecnology. The readout cell size is 100 μm x 100 μm arranged in a rectangular 100x116 pixels matrix, in order to match the pixel sensor cells. To fulfil the $\overline{\text{P}}$ANDA requirements, the chip must be radiation tolerant, self-trigger and have a continuous data transmission of the events above a fixed voltage threshold. The charge information with 12 bit resolution is obtained through the Time-over-Threshold (ToT) technique.

The rectangular pixel sensor with its readout chip is the smaller independent electronic unit; composing two, four, five and six units, four different sized detectors are created to be placed in the barrels and the disks, as shown in Fig. 1.13.

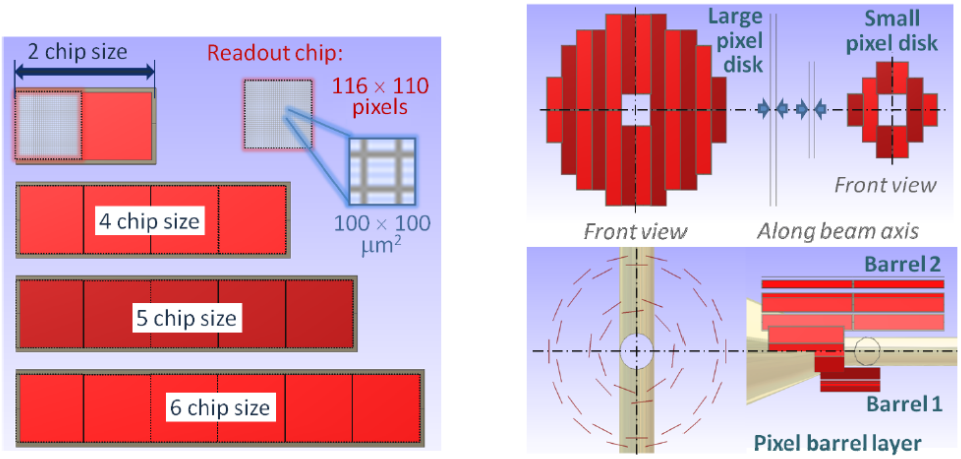


Fig. 1.13 Hybrid Pixel Detector modular structures are represented in the left figure; on the right their placement on barrels and disks is figured.

The readout architecture of the pixel modules is based on a three layers communication structure: the first two layers consist in the silicon sensor bonded, as described, to the ToPix chip; the serial inputs and outputs from this chip are connected through wire bonding to the multilayer bus (third layer) placed on top of the detector. The structure needs to be connected to a service board, able to perform the multiplexing and the electrical-to-optical conversion, in order to communicate with the off-detector transmitting the big amount of acquired data. This communication link must be used in both directions: to receive data from the detector and to send the clock and control parameters to the front-end.

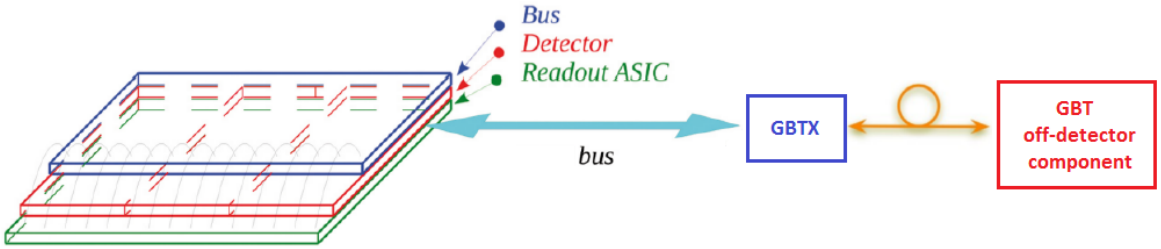


Fig. 1.14 Communication link representation.

Chapter 2

Versatile Bi-Directional Optical Links for HEP

The High Energy Physics (HEP) experiments, like $\overline{\text{P}}$ANDA, generate high volumes of data; therefore an high bandwidth is required in order to transmit information about all the events, necessary for a proper analysis. An other critical issue to be considered is that the experimental setup is subject to harsh radiation levels due to the high number of colliding particles; the components which are sit inside or in the proximity of the detectors have to be radiation hard [4]. Therefore, a communication link like an optical serial link seems to be an excellent solution to these two requests. It presents many secondary advantages, such as galvanic isolation, low electromagnetic interference, low atomic number of the materials involved, and low cabling weight.

The chosen communication link is a *Versatile Bi-Directional Optical Serial Link*, which has been drawn up by the LHC team at CERN, in view of the future upgrade of the experiment, leading to a luminosity improvement of a factor ten. To this purpose, a new optical transmission system is being developed in which the link is bidirectional and adaptable to different link configurations and functionalities. This new project takes its name from the designed ASIC GigaBit Transceiver (GBT); a transceiver is a device comprising both a transmitter and a receiver (transmitter-receiver) which are combined and share common circuitry or a single housing. The new technology for GBT implementation allows an important speed improvement compared to the previous systems, with a data rate of 4.8 Gbit/s to be used simultaneously for data readout, trigger and timing control and experiment monitoring. Since the counting room and front-end electronics are placed in different radiation environments, the GBT system is implemented by a combination of custom developments (ASIC solutions) and commercial components (FPGAs), commonly off-the-shelf, in order to guarantee functionality and reliability.

Moreover, the new LHC link will be subject to higher error rates compared to the old systems due to exposure to higher levels of radiation and due to the higher speed of the link: a strong system for the error correction has been implemented.
In this chapter the specifics of a Versatile Bi-Directional Optical Serial Link will be analized.

2.1 Serial communication

In actual communication systems, the speed limit, in terms of transmitted/received data rate, has been pushed well beyond the traditional 1 Gbit/s barrier, giving the possibility of development for HEP experiments. In this contest, a proper communications must be chosen in order to have maximum flexibility in terms of distance, noise immunity and radiation tolerance.
Digital data transmission can occur in two basic modes: *parallel* or *serial*. In parallel mode, multiple bits are sent simultaneously on different channels (wires) and synchronized to a clock. While, in serial mode, bits are sent sequentially on the same channel: this reduces costs for wire but also slows the speed of transmission. Serial transmission can be either synchronous (groups of bits are combined into frames and frames are sent continuously) or asynchronous (groups of bits are sent as independent units with start/stop flags and no data link synchronization) [24].

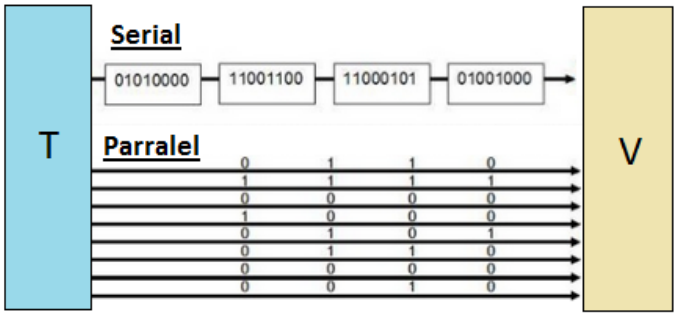


Fig. 2.1 The scheme represents a serial and a parallel communication channel between transmitter (T) and receiver (R).

Although a serial link may seem inferior to a parallel one, since it can transmit less data per clock cycle, there are several reasons making a serial link preferable for data transmission in HEP. The serial links can be clocked considerably faster than parallel links in order to achieve a higher data rate, because clock skew does not affect different communication channels. A serial connection requires fewer interconnecting cables (i.e. wires/fibres) and

hence occupies less space and the extra space allows better isolation of the channel from its surroundings. The ElectroMagnetic Interference (EMI), and consequently the crosstalk phenomenon, are also reduced, since in serial links there are fewer and better insulated conductors in proximity. In serial links the circuit board routing is simpler, as only two serial lines need to be routed, replacing a wide bus and the associated clock; this makes the system more resistant to damages and cheaper to be implemented.
Moreover, the parallel communication, because of its shared-bus topologies, has a primary limiting factor: a failure in any single pin or connection will cause the whole interface to fail.

For the $\overline{\text{P}}$ANDA experiment application, the use of a serial communication is also required in order to respect the low material budget contraints. In fact, simulations performed in order to estimate the contribution to the material budget introduced by the MVD, measured in radiation length units, have shown (Fig. 2.2) that the major contribute is given by the cables (37.7%) and the support structure (28.5%), making necessary the use of a number as little as possible of communication channels.

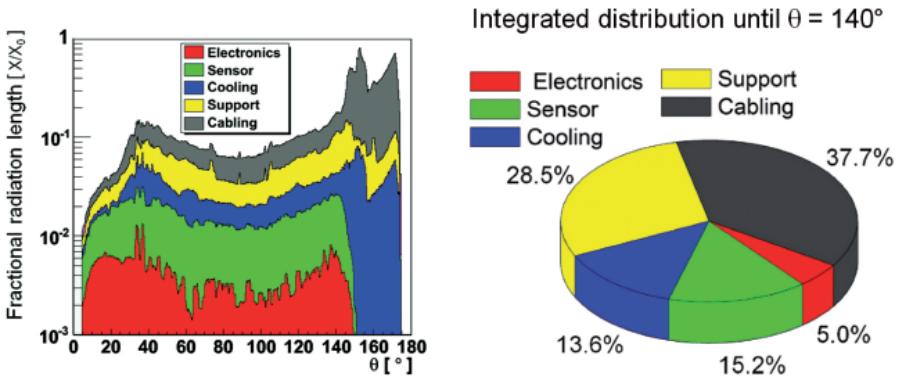


Fig. 2.2 Map of the material budget by radiation length simulations. The figure on the left shows the stacked profile along θ of the material budget; the figure on the right the contribution of the various components.

2.2 Optical link

The use of optical links in HEP has become more popular with the advancement of research and the reduction of prices. The use of optical fibres as a transmission medium has the following advantages [21]

- *low losses*, since optical fibres don't need the presence of repeaters along the path to be covered, making the system cheaper and easier to implement;

- *high bandwidth*, since the transmission bandwidth is a few percent of the carrier frequency (so depends on the used material). For an optical carrier frequency is typically at $\sim$ 200 THz, then optical communication systems have the potential of carrying information at bit rates of $\sim$ Tb/s;

- *minimum interaction* with the particles to be detected, which is a fundamental characteristic to work in a radiative environment. This is due to the low atomic number materials making the optical fibre (silicon and oxygen in the glass, carbon, hydrogen and oxygen in the plastic coatings);

- *small size*, which makes the detector's spatial constraints easy to be respected;

- *immunity to Electro-Magnetic Interference* (EMI), as the signal is constituted of light, and the front end and back end electronics are electrically isolated.

2.2.1 System components

A generic link is made of three principal components: a transmitter, a receiver and a communication channel which connects them.
The transmitter transforms the information to be transferred into a signal, suitable for the communication media. After having traveled through the channel, the signal arrives to the other side of the link, where the receiver converts back the information.

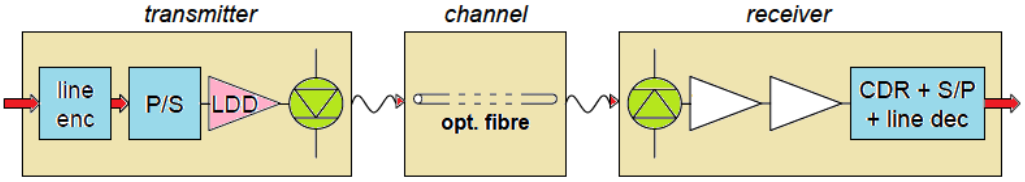


Fig. 2.3 System components of the optical link. In the transmitter: line encoding, parallel-to-serial conversion (P/S), laser diode driving (LDD) and electrical-optical conversion are performed. The optical fibre constitutes the communication channel. In the receiver the photodiode performs optical-electrical conversion, the signal is then amplified and arrives in the clock and data recovery (CDR); finally serial-to-parallel conversion (S/P) and line decoding are performed.

The communication channel

The communication channel transports the signal from transmitter to receiver with the least possible distortion. In optical links the channel is the optical fibre, which guides the beam transmission through a confinement of light based on the principle of total reflection. The basic structure of an optical fiber (Fig. 2.4) consists of three parts; the core, the cladding, and the coating or buffer.

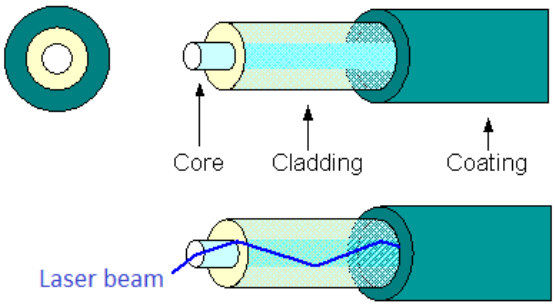


Fig. 2.4 Structure of a basic optical fibre.

The core is a cylindrical rod of dielectric material, generally glass, with an index of refraction n_1 and is surrounded by a second layer of dielectric material, called the cladding, with an index of refraction n_2. The difference in the two refractive indexes ($n_2 \gg n_1$) and the propagation angle prevent the light from leaking out from the core/cladding interface when launched into the core. For extra protection from physical damage, the cladding is enclosed in an additional plastic layer called the coating.

The transmitter

The transmitter function is to convert the electrical input signal into an optical signal to be transmitted serving the same information as the original electrical signal. The main transmitter functions are the serialization (P/S) and optimization of the signal stream for transmission (different line codings are chosen depending on the kind of information and the environment where the experiment takes place). The signal serial stream is often applied to the driving circuit of the laser diode (*Laser Diode Driver*, LDD), so that the laser output is directly modulated by the signal.

The receiver

The receiver block functionality is complementary to that of the transmitter: it converts back the information from a serial optical signal to a parallel electrical one. Its main functions are the reconstruction and de-serialization (S/P) of the received signal. The optical signal is first converted to electrical by a photodetector, often a photodiode, which responds to the incident optical power with a proportional photocurrent (the proportionality constant is called "responsivity"). The electrical signal enters in a cascade of two amplifying stages: a TransImpedance Amplifier (TIA) and a Main Amplifier (MA, an automatic gain control or limiting amplifier), that brings the small signal from the TIA at a level that is sufficient for the next operations.

After amplification, the voltage signal enters in the *Clock and Data Recovery* (CDR) circuitry,

where it is deserialized and decoded in order to reconstruct the transmitted signal in its original form. The CDR circuit extracts the clock frequency and demodulates the digital data, using a *local oscillator*, which locally recreates the transmitter clock, and a *Phase/Frequency Detector* (PFD), which is sensitive to phase/frequency differences between the local oscillator and the incoming data stream. However, in order to have a meaningful PFD output, the transmitted encoded serial bit stream must have enough embedded clock information.

2.2.2 Line encoding

The role of line encoding is to convert source data to a digital form, resistant to noise, matching the data stream to the characteristics of the channel; at the same time the coding must be reasonably economical in the use of bandwidth. In the transmission process, the coding operation is generally implemented by the combined work of a scrambler and an encoder (their functionality will be deeply described in chap.3) [6].
The main line code property is the *transparency*, which implies that the chosen encoding does not alter the content of the transmitted message. If the link channel is an optical fibre, there are several constraints on the code to be respected for a proper communication:

- *bit sequence independence*: the line code must adequately encode any source bit sequence;
- *small low frequency content*: the transmitted signal should be balanced (ideally containing an equal number of ones and zeros);
- *transmission of adequate timing information*: the encoded bit stream must produce a high density of level transitions to allow for proper operation of the clock recovery circuitry;
- *small number of equal consecutive bits*: this reduces the low frequency content of the transmitted signal;
- *high efficiency*: introduced redundancy should be kept to a minimum;
- *low error multiplication*: an error which occurs during transmission should not result in many decoded errors;
- *low systematic jitter*: the sequence of transmitted bits must ensure that pattern dependent jitter is kept low;
- *possibility to guarantee the frame alignment*: in case of a framed data stream the boundaries of a frame must be located at the receiver.

Two fundamental parameters to evaluate the bandwidth utilized by a specific code are the *redundancy* (R) and the *efficiency* (E). The redundancy is defined as:

$$R = n - k$$

where n is the number of bits used to transmit a message and k is the number of bits of actual information in the message.
The efficiency is the number of information bits divided by the number of bits required to encode them:

$$E = \frac{k}{n}$$

The concepts of redundancy and efficiency are complementary: redundant bits allow to transmit supplementary pieces of information in addition to the real data string (e.g. they are used for the forward error correction), making the transmission more precise but reducing the bandwidth usable for effective data and so reducing the efficiency [20]. A good balance between these two parameters allows to obtain the optimum code to be used.
There are several commercial line codes designed to match the specific link requirements and the type of its communication channel; the three used codes for the $\overline{\text{P}}$ANDA link will be described in the following chapter.

2.2.3 Radiation effects and hardening techniques

The way in which high energy ionizing radiation interacts with the circuit components depends on the nature of the incident particles and the solid materials on which they collide. The main consequences of this interaction, in which incident particles lose energy passing through matter, are an alteration in data transmission or a permanent damage of the communication system components.

The radiative effects can be grouped in two classes: *nuclear displacement*, provoked mainly by neutral and massive particles (such as neutrons), and *ionization effects*, whose principal responsible are charged particles (such as photons and electrons). When a particle passes through a semiconductor, it can collide with a nucleus and displace it from its normal position, thus altering the regular crystalline structure of the semiconductor material. This effect is called displacement damage because the disruption in the lattice structure causes variations in the behaviour of the device. The stable lattice defects cause the introduction into the semiconductor bandgap between valence and conduction bands of new energy levels, acting as generation, recombination or trapping centres, which alter the intrinsic properties of the material (e.g. can reduce the mobility of carriers).

Therefore the displacement damage strongly affects optoelectronic devices, while it is relatively unimportant for MOS transistors.

Ionization phenomena occur when a highly energetic particle removes one electron from its parent atom producing an electron-hole pair. The number of electron-hole pairs created is proportional to the quantity of energy deposited in the material, which is expressed through the total absorbed *dose* (energy absorbed locally per unit mass as result of irradiation by energetic particles). So, considering the different irradiation effects on a generic electronic system, it is important to distinguish between:

- *Total Dose Effects* (TDE). They are due to the cumulative damage of the semiconductor lattice caused by ionizing radiation over the exposition time and they could affect both analog and digital devices;

- *Single Event Effects* (SEE). They are due to a high-energy particle which travels through the semiconductor leaving an ionized track behind and affects mainly the digital devices, causing different effects, such as a benign glitch in output, which causes one cicle comunication errors and thus are called *Single Event Upset* (SEU), or a less benign bit flip in memories or registers, which can cause a permanent damage.

Since, as seen, a general system radiation effect can cause malfunctioning and at least the permanent damage of some electronic or optic components, it is necessary to find proper protection and correction techniques to make the system resistant to radiations.
The creation of custom radiation-hardness components corresponds to a very high cost, because of the use of non-standard technology with a little demand in the commercial world, compared to which the HEP community is too small to be able to modify general trends or to afford unusual processes. The alternative choice could be the use of some design tricks and layout to obtain a good level of tolerance to radiations, using standard CMOS technology processes. In order to increase the radiation-hardness of a system, there are several different techniques, which can be gathered in three groups: radiation hardening by architecture, by process and by layout. The first implies the use of commercial parts in redundant and duplicative configurations, the second the employment of specific material and processing procedure and the third the design of dopant wells and isolation trenches into the chip layout. Considering the specific final application, it is possible to select one of these techniques to develop a radiation-tolerant system, because each technique has pros and cons.

Concerning **optical components** in the link, passive devices (i.e. fibres and connectors) are more responsive to ionization phenomena, while active devices like lasers and photodiodes are more responsive to displacement damages. Moreover, the photodiode is strongly sensitive

to Single Event Effect (SEE) by virtue of its low input signal level (few microwatts at rates into the Gbps/s regime), which makes it sensitive to false signals created by direct ionization by incident protons. A radiation particle produces a diode reaction similar to a light impulse coming from the transmitter.
The positive perspective is that the implementation of an optical system may leverage on Commercial-Off-The-Shelf (COTS) technologies, which minimize the developing cost, but it must undergo very careful design cycles where a detailed understanding of component and subsystem radiation performance is mandatory. For example extensive testing is required to verify radiation tolerance over the desired amount of time and radiation doses.

Concerning **ASIC components** in the link, MOS transistors are almost entirely insensitive to displacement damage, while ionizing radiation instead has an effect on their structure, and in particular in the silicon dioxide. The two used hardening techniques are by layout and by architecture. The choice of a specific layout is important since a scaling of technology helps in reducing damage due to the TDE. In fact reducing the gate oxide thickness improves the radiation tolerance of the device: in particular for the used 130 nm technology, the transistors seem to be more tolerant with respect to the previous technology.
A proper architecture is used to protect he system from SEE.

2.3 Versatile Bi-Directional link

The idea of a Versatile Bi-Directional Link is to develop a link solution that can be adapted and used for different data acquisition (DAQ) systems to transmit and receive: events data and pieces of information for timing and synchronization of the detectors, for triggering and for experiment control. The objective is to build a system based on a little chip set of ASIC, the *GigaBit Transceiver* (GBT), and a limited number of optoelectronic components, to optimize the link development and test. The complete DAQ system is a modular structure composed by multi-chip modules, the elementary unit is represented in Fig. 2.5.
The link proposed by LHC, thanks to the technological upgrade, can implement different link topologies, has bidirectional capability and has high bandwidth. It would also be guaranteed to robustly handle irradiation effects, for both total dose and SEU, as the ASIC would be designed with radiation hardening techniques and the optoelectronic components would be qualified for use in a radiation environment.

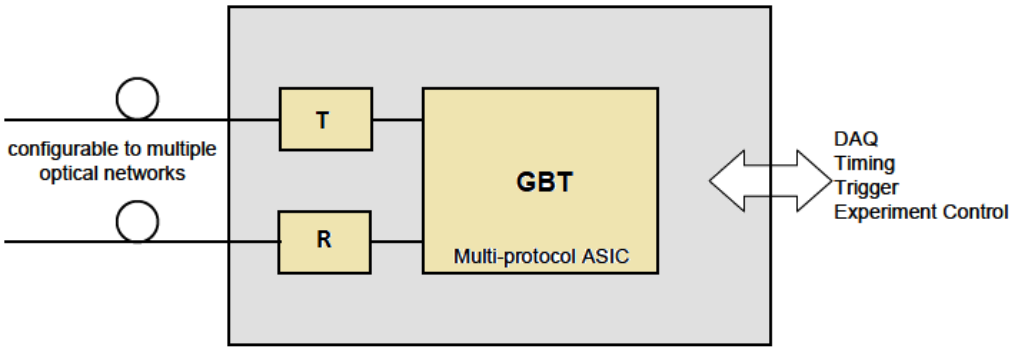


Fig. 2.5 Scheme of the GBT modular unit. The unit containing the ASIC, qualified optoelectronic components and optical and electrical connectors.

2.3.1 Link configurations

The same ASIC transceiver has to handle different link topologies and different modes of operation, in order to be versatile. It can operate both in continuous or packet mode, as:

- *general purpose link*, which implies that the full data bandwidth is available for data transmission, without any restrictions on the data contents. In this case, transmitter and receiver pairs are fully synchronous and the transmission is synchronous;

- *TTC (Time and Trigger Control) link*, which implies that the data contents of the transmission are preallocated so that trigger functions and control commands can be implemented. In this mode two different links must be distinguished: the down-link, which transmits a continuous stream of data (broadcast to many destinations), and the up-link, which transmits bursts of data for talking to a single destination. The transmission occurs in packet mode.

The main used network connection is shown in Fig. 2.6, but some other network topology is also possible, as shown in Fig. 2.7 .

The point-to-point configuration (Fig. 2.6) is used for bidirectional data transmission without any restriction on the data contents. The link operates in continuous mode and its main purpose is data transmission; this configuration is so proper for a general purpose link. While the Fig. 2.7 configuration is used to implement a TTC link, since it uses a tree network in which the trigger-continuous down-link broadcasts data from one master transmitter to N slave receivers and the up-link uses a similar optical passive tree to collect data from several slave transmitters to a single destination (N-to-1), the master receiver. The slave transmitters

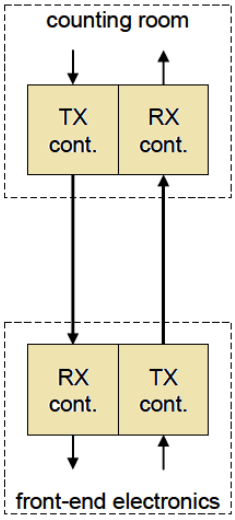


Fig. 2.6 Point-to-point connection.

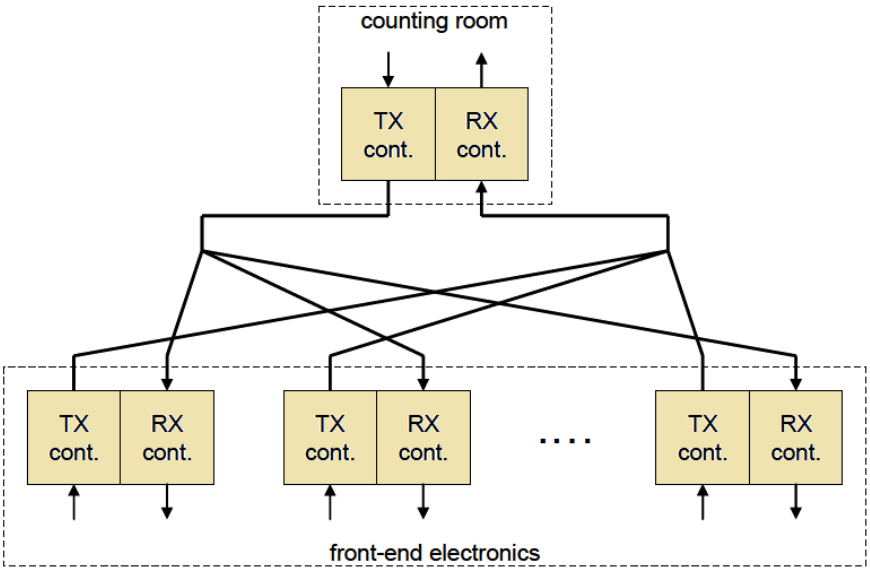


Fig. 2.7 Bidirectional One-to-N/N-to-One link.

operate in packet mode. The master transmitter arbitrates the access of the slave transmitters to the up-link optical tree [20].

2.3.2 Frame format

Different frame formats are foreseen for the GBT communication, due to the two link option previously described: the TTC and the general purpose link, combined with continuous

and packet mode transmission. All these frame formats, that will be fully described in the Chapter 3, have the general structure shown in Fig. 2.8.

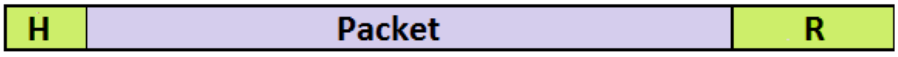


Fig. 2.8 General frame structure for transmitted and received data; it is composed by the header (H), the data packet and the redundant bits (R).

The frame, whose length depends on the usable line rate, is formed by adding to the data: a header (generally 4 or 8 bit) and some redundant bits, to be used for different purposes (e.g. for forward error correction). According to the link functionality and taking into account the specific operation characteristics for the different transmission mode, the central data bits can vary. For a point-to-point link, for example, the full bandwidth is available to the data transmission, while to implement the up-link and the down-link a part of the bandwidth is dedicated to other pieces of information (Fig. 2.9).

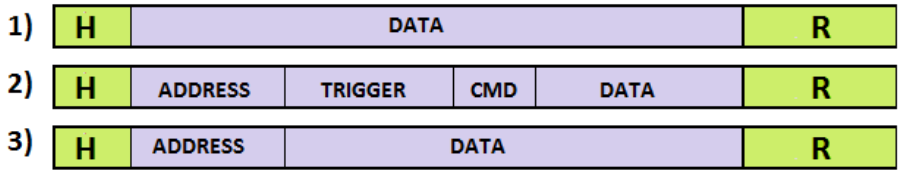


Fig. 2.9 Specific frame structure for the general link (1), for the down-link (2) and for the up-link (3).

Chapter 3

The GBT project

The goal of the GBT project is to produce the appropriate fibres and opto-electronic components and to develop the specific chips that can be used to implement multipurpose high speed optical links (4.48 Gb/s bandwidth) for high-energy physics experiments. This architecture will allow a single bidirectional optical (two fibres) link to be used simultaneously for data readout, trigger data, timing control distribution, and experiment slow control and monitoring. The information from the three data paths (TTC, DAQ and slow control) will be merged on a single point-to-point connection that can function with very high reliability in the harsh radiation environment typical of HEP experiments.

Because of the very different radiation environments, the project is conceptually divided into two distinct but complementary parts (Fig. 3.1):

- *The GBT ASIC*
  It is the on-detector component of the link and, working in a hostile radiation environment, requires custom made components. The GBT ASIC is part of the GBT chipset composed of several electrical and opto-electronical components, including the Laser Driver (GBLD) and the GBTX link ASIC, that implements all the needed functions of the data and timing transceiver.

- *The GBT FPGA*
  It is the counting room component, operating in a radiation free environment. Thus it can be implemented by COTS (Commercial-Off-The-Shelf) components, whose use allows this part of the link to take full advantage of the latest commercial technologies in FPGA's evolution, enabling efficient data concentration and data processing from many front-end sources to be implemented in very compact and cost efficient trigger and DAQ interface systems.

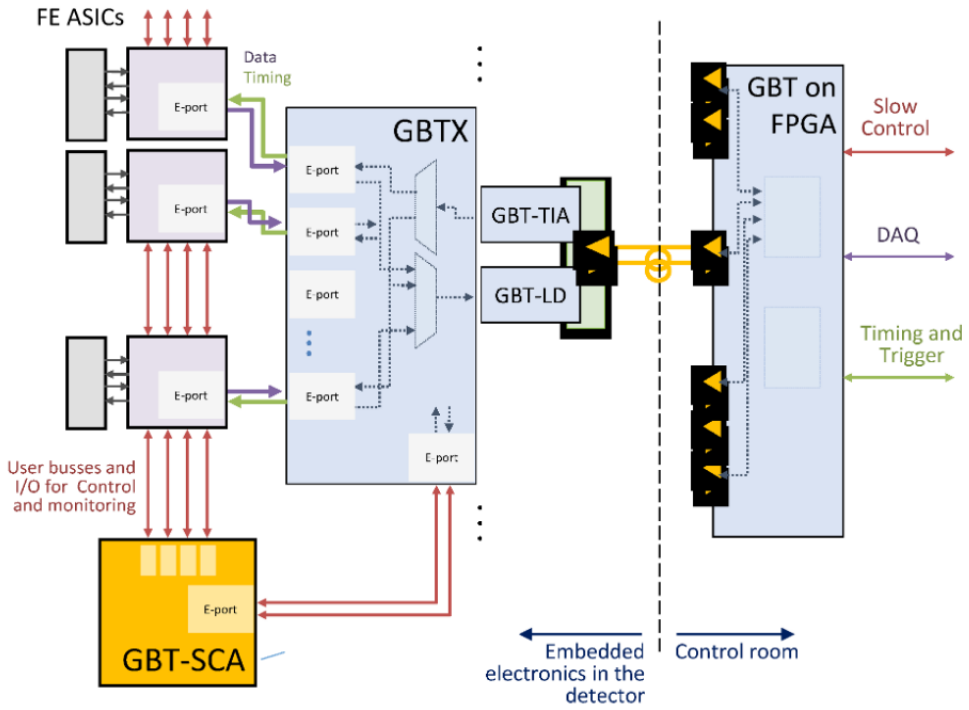


Fig. 3.1 GBT optical link implementation scheme; the two different parts, the GBT ASIC and the GBT FPGA, are visible.

3.1 The GBT ASIC

3.1.1 Structure

The GBT ASIC block is a chip set composed, as shown in Fig. 3.1, by the following circuits: [17]

- **GBTX**
  The GigaBit Transceiver (GBTX) is a serializer-de-serializer circuit receiving and transmitting serial data at 4.8 Gb/s. It encodes and decodes the data into the GBT protocol and provides the interface to the detector front-end electronics. An appropriate description of its architecture and implementation aspects will be the subject of the following sections.

- **GBTIA**
  The GBTIA is a trans-impedance amplifier receiving the 4.8 Gb/s serial input data from a photodiode. This device was specially designed to cope with the performance degradation of PIN-diodes under radiation. In particular the GBTIA can handle very

large photodiode leakage currents (a condition that is typical for PIN-diodes subjected to high radiation doses) with only a moderate degradation of the sensitivity. The device integrates in the same die the transimpedance pre-amplifier, limiting amplifier and 50 Ω line driver. The GBTIA was fabricated and tested for performance and radiation tolerance with excellent results.

- **GBLD**
  The GBLD is a laser-driver ASIC, working up to 5 Gb/s with modulation and bias currents ranging from 2 to 24 mA and 2 to 48 mA respectively, to modulate 4.8 Gb/s serial data on the optical fibre. Thanks to the large current ranges, the GBLD is conceived to drive both edge-emitters or VCSEL lasers [1], which require respectively high and low bias and modulation currents. Pre- and de-emphasis functions are implemented in order to compensate for high external capacitive loads and asymmetric laser diode response. The emphasis function is independently programmable for the rising and falling edge of the signal and can be varied in the range from 0 to 12 mA with a resolution of 0.8 mA [16].
  The chip is designed in a commercial CMOS 0.13 μm technology and its configuration can be controlled via an I^2C serial interface.

- **GBT-SCA**
  The GBT-SCA is a chip designed to provide the slow-controls interface to the front-end electronics. Its main functions are the adaptation of the GBT to the most commonly used control buses in HEP and the monitoring of detector environmental quantities such as temperatures and voltages.

To implement reliable links the on-detector components have to be tolerant to total radiation doses and to single event effects, e.g. transient pulses in the photodiodes and bit flips in the digital logic. These undesired effects are mitigated in the GBT chipset using an extensively radiation qualified commercial 130 nm CMOS technology and following special layout techniques. Considering that SEU effects are one of major cause of errors in HEP data transmission, the GBTX uses a particular robust line coding and error correction scheme, capable of correcting both single bit and bursts errors caused by SEU's and transmission errors. In its standard mode of operation $\sim$ 30% of the optical link bandwidth is assigned to the transmission of a Forward Error Correction (FEC) code. Furthermore the GBT chips use dedicated design methodologies (Triple Modular Redundancy, TMR) to resolve SEUs in internal logic and registers.

[1] VCSEL is the acronym for Vertical-Cavity Surface-Emitting Laser.

3.1.2 GBTX architecture

The GBTX is based on a 4.8 Gb/s Serialiser/Deserialiser circuit able to convert the input data received from the front end electronics into a serial stream with the GBT format and to deserialise the GBT frame transmitted from the counting room, providing data to the front end electronics.

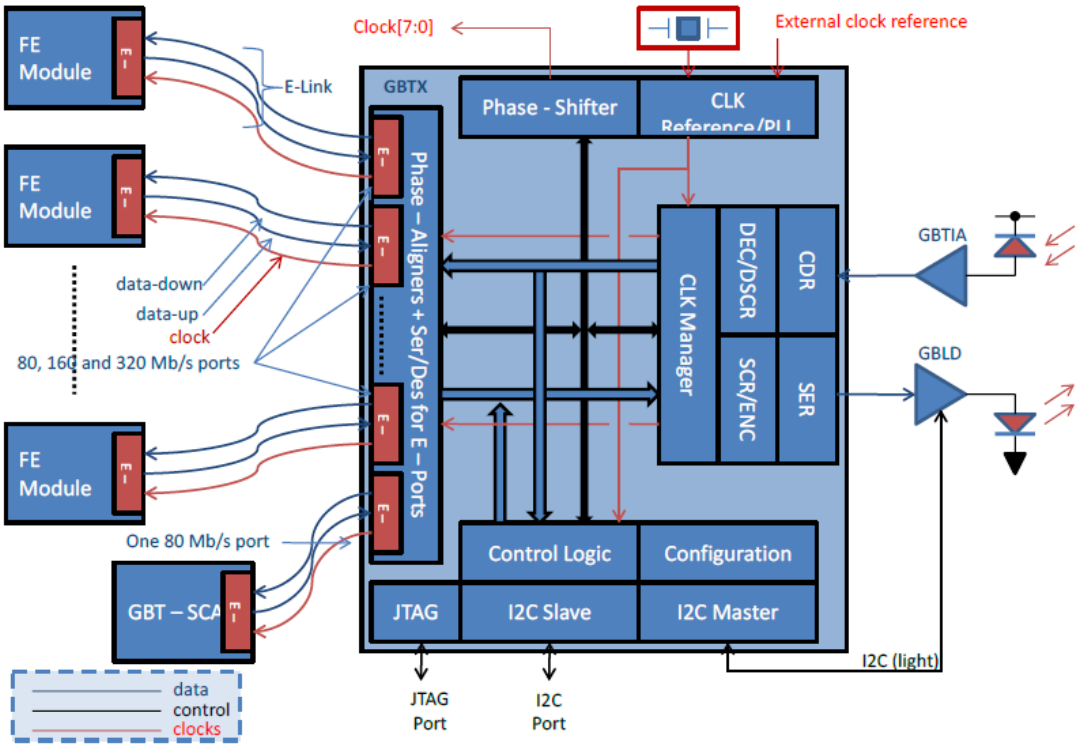


Fig. 3.2 Generic GBTX architecture and interfaces; in the counting room direction the GBTX is connected to the GBLD laser driver and to the GBTIA trans-impedance amplifier, whereas it communicates with the front-end modules using the E-Links.

The architecture of the GBTX ASIC and its interfaces are displayed in Fig. 3.2.
In the transmitter part the data to be transmitted are SCRambled, to obtain DC balance [2], ENCoded with a specific code and then serialized (i.e. converted from parallel to serial form) and sent to the GBLD laser driver. In the receiver part, the high speed serial data coming from the GBTIA are received by the CDR, that recovers and generates an appropriate high speed clock to correctly sample the incoming data stream. In the CDR, the incoming serial data are de-serialized, DECoded, with appropriate error corrections, and finally DeSCRambled.
The other principal components of the GBTX are: the clock manager circuit, which takes care

[2]DC balance is obtained when the number of ones and zeros in the signal are equal; for signals with a good DC-balancing it is possible to pass the information with minimal degradation in contents.

of generating and managing the different clocks needed by the circuit, the general control and monitoring logic and a programmable Phase Shifter, which can generate, if necessary, 8 external user clocks with programmable frequency and phase (external clocks are used, for example, during start-up as a locking aid for the CDR circuit). Initial configuration information is taken from the on chip e-Fuses and can then be modified via the optical link itself or via an I^2C slave interface. A JTAG interface is available for boundary scan [8].
On the other side of the chip, the connections to the front-end modules are made through sets of local Electrical Links (E-Links). E-Links use Low-Voltage Differential Signalling standard (LVDS), with signal amplitudes programmable depending on the distances to be covered by the transmission link, on bit rate and power consumption. The E-Links, whose number and data rate are programmable, are driven by a series of ePorts on the GBTX and are associated with E-link ports in the front-end modules.

It is possible to use GBTX for both bidirectional and unidirectional data transmission/reception, configuring and initializing the link in a proper way. The three possible connections, as simple transmitter, simple receiver and transceiver, are reported in Fig. 3.3 and in all cases the GBTX establishes independently a working link connection.

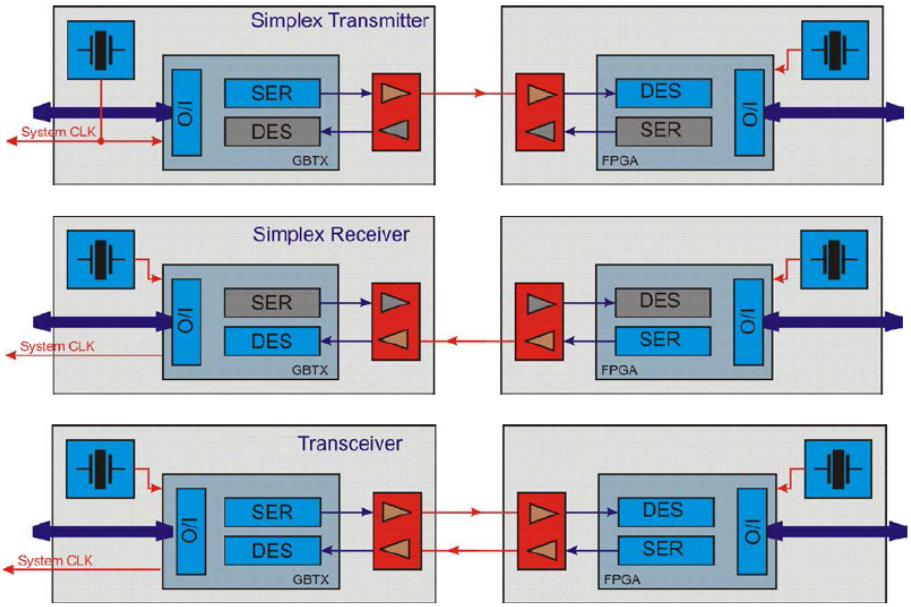


Fig. 3.3 The three possible GBTX communication modes are presented: simple transmitter, simple receiver and transceiver.

To the experiment purpose, the transceiver communication mode is the most significant one: in this mode the GBTX works as a full link transceiver with bidirectional data communication between the front-ends and the counting room. The GBTX delivers the global system clock

reference, coming from the counting room and reconstructed by the CDR, to all front-end components. In this mode, the ePort receivers feed data to the serializer and the ePort transmitters receive data from the CDR circuit.

3.1.3 Frame code and encoding

Three different frame codes for the serial communication link have been implemented for the GBTX. The communication is based on the transmission/reception of frames of 120 bits, during a single LHC bunch crossing interval (25 ns), resulting in a line rate of 4.8 Gb/s. The first reported frame code is highly recommended because conceives a robust scheme (32 bits of Forward Error Correction) to protect the data transmission against mismatch due to link noise and single event upsets.

GBT FRAME encoding

The 120-bit "GBT FRAME" is divided in: a 4-bit header, 84-bit data and 32-bit Forward Error Correction (FEC), as displayed in Fig. 3.4. Having 84 bits for effective data transmission, the real available bandwidth is reduced from 4.8 to 3.36 Gb/s. The efficiency of the code is given by the ratio between the payload (80 bits of data) and the full packet size (120 bits of frame), resulting in 67% (80/120). This can be considered very efficient for a code that obtains this high level of immunity to single bit and long bursts of errors.

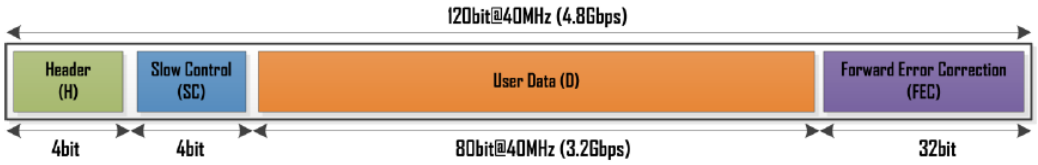


Fig. 3.4 The GBT FRAME encoding scheme.

The *Header* field is transmitted at the beginning of each frame, with the purpose of data stream synchronization. This means that the repeated identification of a valid header indicates correct frame-locking, while consecutive non-valid headers indicate that frame synchronization has been lost and that a frame synchronization cycle has to be initiated. Since the header bits are transmitted unscrambled, the valid header codes are chosen to be DC-balanced. Two different header codes can be chosen:

- idle $\rightarrow$ 0110
- data $\rightarrow$ 0101

In a transmitted frame the type of header is selected by a data-valid input signal (txDataValid), whereas a received frame the header type is indicated by a data-valid output (rxDataValid) signal, which is high if the header is 'data' (0101).

In the *Data* field, 4 bits are always reserved for Slow Control information (2 for Internal Control and the other 2 for External Control), leaving 80-bits for user Data transmission, that can be used indistinguishably for Data Acquisition, Timing and Trigger Control and Experiment Control applications. Data transmitted have fixed latency in both directions enabling its efficient use for trigger information and timing control.

To protect all the other fields in the frame against transmission errors, the *FEC* field is used. The implemented FEC algorithm is a 2 times interleaved *Reed-Solomon* code: the code is built by interleaving two Reed-Solomon encoded words with 4-bit symbols, each capable of correcting a double symbol error. This in practice means that a sequence of up to 16 consecutive corrupted bits can be corrected. The Reed-Solomon code is a type linear cyclic code for errors detection and correction. It is based on the oversampling on a polynomial which is constructed from the data to be transmitted. The polynomial is then calculated in a number of points bigger than the number sufficient to uniquely identify it; the value of these points is transmitted. This makes possible the errors correction in the reception phase.
A secondary task of the FEC code is to provide the required DC-balancing of the serial data stream, in combination with the scrambler [8].

The coding creation process is sketched in in Fig. 3.5

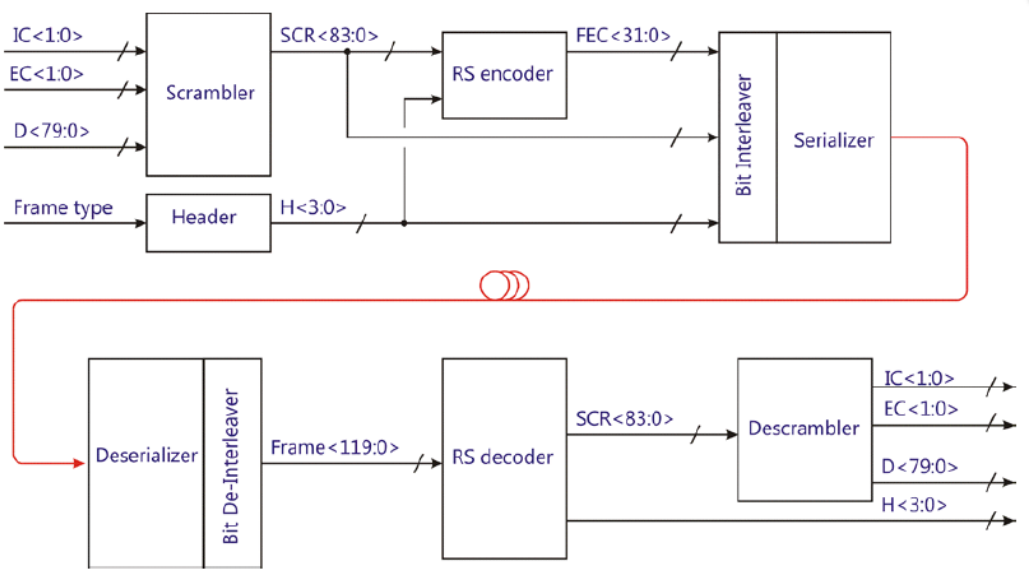


Fig. 3.5 GBTX components for the code frame construction.

The 84 bits of data enter in the scrambler, which reorganizes the data structure to have short

sequences of consecutive equal bits and guarantees the DC balance, and then the 4-bit header is added. The generated 88-bits line is processed by the encoder, that adds the 32 bits for Forward Error Correction. The 120-bit frame is finally interleaved, serialized and transmitted. The equivalent and inverse operations are made in reception phase.
In the 130 nm CMOS technology used for the GBTX, both the encoding and decoding operations can be done within a single machine clock cycle, having a minimal impact on the transmission latency.

8bit/10bit encoding

The 120-bit link frame consists of 12 words, codified with a 8bit/10bit encoding, of which the first is always a comma character required for the receiver synchronization (Fig. 3.6).

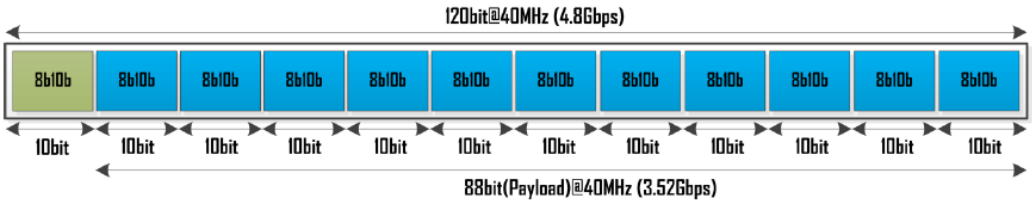


Fig. 3.6 The 8b10b encoding scheme.

No error correction and only very limited error detection capability is possible with this format. The 88 bits ($11x8 = 88$) available for data transmission are already DC balanced and thus do not need to pass the scrambler. Since the effective number of user bits is 88, the coding efficiency is $88/120 = 73\%$, little better than the standard GBT frame.
An other limit is that the 8bit/10bit encoding option is available only in the transmitter part of GBTX, i.e. from the detector to the counting room direction. So, the main justification to use it is to reduce resources needed in the counting room FPGAs to implement the normal GBT forward error correction.

WIDE BUS encoding

The “wide bus” encoding is the solution thought to transmit a big amount of user data in a frame, cutting off completely the FEC field. That is, the space taken by the FEC code in the GBT frame is used in the wide frame mode to transmit data (Fig. 3.7).
The consequence of elimination of the FEC functionality is a transmission efficiency increased to 93% (112/120), really high when compared with the GBT frame format. However this is done at the cost of having no SEU error protection on the transmitted data.

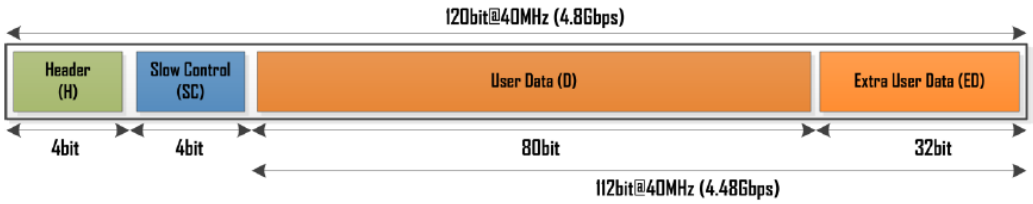


Fig. 3.7 The WIDE BUS encoding scheme.

3.2 The GBT FPGA

3.2.1 GBT-FBGA core overview

The off-detector part of the GBT system consists of a Field-Programmable-Gate-Array (FPGA), programmed to be compatible with the GBT protocol and to provide the interface to off-detector systems. The firmware required to allow the communication between the FPGA and the GBTx and the ASIC chipset design have been developed concurrently. Therefore the GBT-FPGA core is now a full library, targeting FPGAs from ALTERA and XILINX [3], allowing the implementation of one or several GBT links, which can be configured to provide any encoding mode offered by the GBTx (GBT-Frame, 8b10b and Wide-Bus mode). In order to facilitate the in-system implementation, the different components of the Core have been integrated in a single module called *"GBT Bank"* (Fig. 3.8). Being the top entity of the GBT core, it must have independent resources in terms of logic and timing. The clocking resources are provided from external to the GBT Bank so the user can connect the different clocks as desired. The configuration of the GBT Bank and its properties, such as the encoding mode, are transferred to all the internal components. The GBT Bank may include several *"GBT Links"*, whose number depends on the targeted FPGA model, as shown in Fig. 3.8. Each GBT Link manages a serial line communication and is so composed by a transmitter, a receiver and a Multi-Gigabit Transceiver (for the detailed analysis of the link structure see section 3.2.2).
In GBT-FPGA project, two types of implementation for the transmitter and the receiver are foreseen: the *Standard* version, for non-time critical applications and the *Latency-Optimized* version, ensuring a fixed, low and deterministic latency of the clock and data (at the cost of a more complex implementation) [7].
Table 3.1 depicts a comparison between Standard and Latency-Optimized modes.

[3] ALTERA and XILINX are the two main commercial producers of FPGAs.

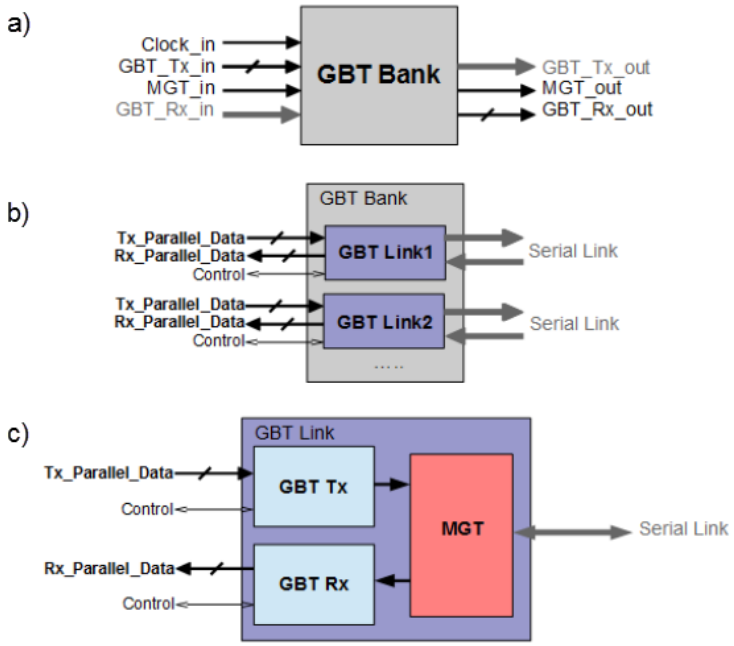


Fig. 3.8 GBT FPGA core overview: the GBT Bank (a), the GBT Links inside the GBT Bank (b), the structure inside a GBT Link (c) are displayed.

Table 3.1 Standard VS Latency-Optimized modes.

	Standard	**Latency-Optimized**
Logic Resources Utilization	Non fixed, Non deterministic	Fixed, Deterministic
Clocking Resources Utilization	Low	High
Clock Domain Crossing	Don't care	Critical
Implementation	Simple	Complex

3.2.2 GBT Link structure

The structure of the off-detector part of the GBT system consists of an FPGA, programmed to be compatible with the GBT protocol and to provide the interface to off-detector systems. The structure for data transmission and reception over the optical fibre is similar to the one described for the GBT ASIC. In the same way, before nibble serialization, the DC balance is ensured by scrambling the data and the FEC by encoding the data using a Reed-Solomon code [4] .

Commercial FPGA devices embed serial Multi-Gigabit Transceivers (MGT), configurable for several standard telecommunication protocols. Since these transceivers, which are hard blocks on FPGA, are configured by vendor specific configuration files, they do not include

neither scrambler, nor encoder and their word alignment modules, in receiver mode, are not flexible enough to fit the GBT requirements. To solve these problems, the GBT protocol has been implemented on FPGA using a combination of custom functions, developed in the FPGA logic cells, and the transceiver primitive component, used in the most basic way (SER/DESER function), as represented in Fig. 3.9.

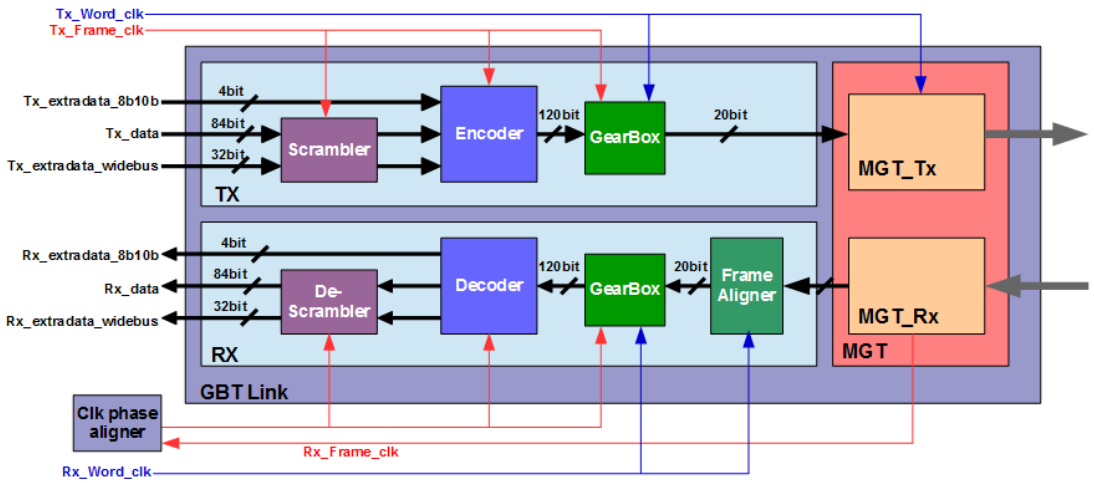


Fig. 3.9 GBT FPGA architecture and interfaces; the implemented component are connected to the internal transceiver, used to serialize and deserialize the frame.

In addition to scrambler and encoder, a *"Gear box"* has been implemented in order to match the specific input request of the transceiver. The gear box working principle is based on the use of two different clocks:

- a frame clock (40 MHz), used for the frame flowing in the custom blocks (from encoder to gear box);
- a word clock (120 or 240 MHz), used for the transceiver logic.

Thanks to the double clock domain, the gear box segments the 120-bit frames at 40 MHz in 40-bit words at 120 MHz, or 20-bit words at 240 MHz, that can be properly sent in the transceiver input. The choice between the two possible word clocks, as that for the word length, is determined by the different FPGA commercial standards for the transceiver configuration; it is necessary to consult the targeted datasheet.

In the receiver part, two additive components have been designed: a *clock phase aligner*, to maintain the correct phase of the frame clock reconstructed after transmission in Latency-Optimized mode, and a *frame aligner*, that reorganizes the continuous data stream coming

from the transceiver in 40-bit (or 20-bit) words to be sent to the gear box. The frame aligner carries out search of header pattern and alignment functions, using a barrel shifter, that allows to bit shift the incoming data, and a state machine looking to the expected header position in the frame.

3.2.3 The GBT-FPGA *Example design*

The GBT-FPGA project offers the opportunity to understand, fully test and really implement the proposed code, delivering an *Example design* for selected FPGAs and the most common FPGA development kits. The idea is to implement some supporting component to emulate the GBTX and to check the accuracy of the transmitted patterns, testing both the transmitter and the receiver functions.
There are two types of *Example design*, with the same structure but different number of implemented GBT links. The one described in this work is a single-link project, consisting in one GBT Bank implementing one GBT Link. The transmitter is connected to a pattern generator, designed to recreate various 120 bit frames, and the receiver is connected to a pattern checker, to verify that the reconstructed frames are equal to the sent one. In the simpler configuration, transmitter and receiver are connected in loopback (as shown in Fig. 3.10), otherwise the serial lane can connect two GBT compatible devices, one used in transmitter and the other in receiver mode.

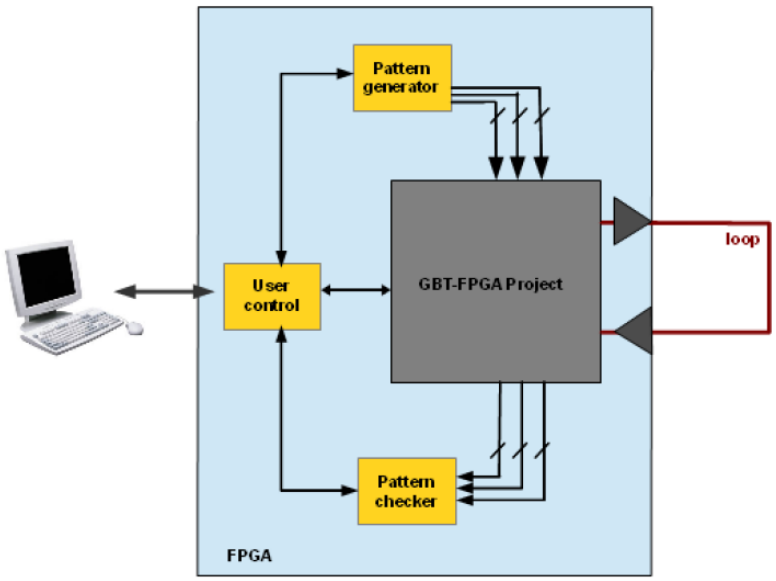


Fig. 3.10 GBT-FPGA *Example design* in single-link configuration.

The user can set the same feature on the GBT bank, such as the type of communication

(Standard or Latency-Optimized) or the type of encoding (GBT-Frame, Wide-Bus or 8b10b). The control of the *Example design* is done through a PC using specific cores and software provided by the FPGA vendors (e.g. Xilinx's ChipScope).

Chapter 4

Implementation of the *GBT-FPGA* *Example design*

The GBT-FPGA code has been developed in *VHDL*. The "VHDL", acronym for VHSIC (Very High Speed Integrated Circuits) Hardware Description Language, is a language for describing structure and functionality of integrated circuits (IC). It arose out of the United States Government's VHSIC program to create a standard language for the expanding IC technologies.
The VHDL main advantage is the high number of abstraction levels that can be used in the circuit description, dealing with constructs typical of the programming languages (if, for structures), and the possibility to define parallel processes as in the hardware. This allows to easily model the different functional blocks of the system and their interactions (i.e. exchanges of control signals and data). The level of abstraction of the code is then reduced by a chain of processes, as described in section 4.1.1. In the lowest level the description is made by interconnected logic gates.
The code has been implemented on Xilinx Virtex6 FPGA, placed on a ML605 Evaluation Board, and optimized for our resources utilization.

Before the implementation two parallel studies have been carried out, concerning the knowledge of the VHDL code and of the available hardware resources, as shown in the scheme Fig. 4.1.
The chapter starts from the VHDL code description, introducing the ISE design tool (provided by Xilinx to manage the code) and then passes to the resources study, focusing on the used FPGA, on the evaluation board and on the optical transceiver.
The last section describes the effective implementation and the used resources.

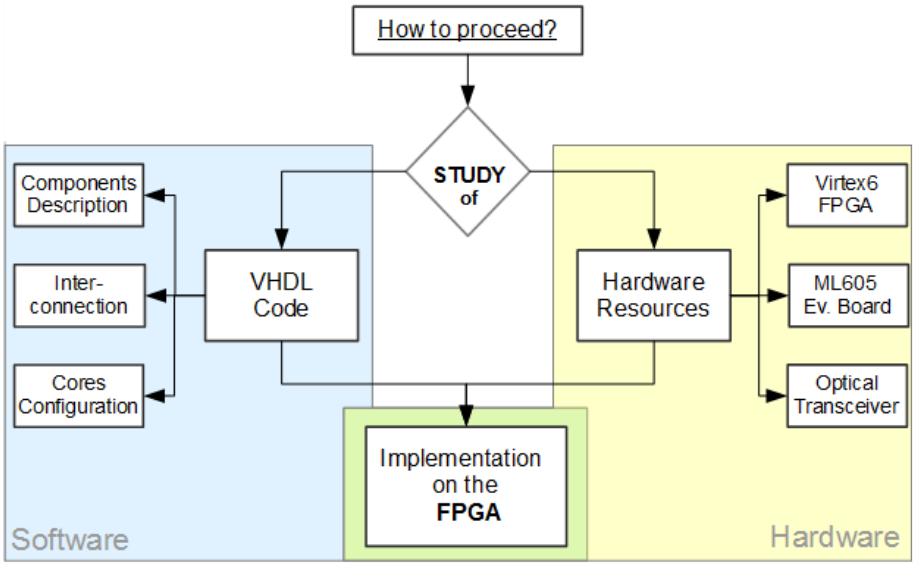


Fig. 4.1 Scheme of the followed procedure for the implementation.

4.1 Analysis of the VHDL code of the *Example design*

4.1.1 ISE software

ISE (Integrated Software Environment) is a suite of software and design environments for FPGA, provided by Xilinx. It is conceived to assist the users in all the steps of the development flows, from the system design to the verification through simulation, from the code implementation to the programming of the chosen Xilinx device.
The first step is the creation of a design project, where all the other files created in the development phase will be stored and organized. The choice of different schematic forms is foreseen by ISE, in order to have a software versatile and adaptable to a wide range of needs. The top-level design source file can be: an Hardware Description Language (HDL), such as VHDL or Verilog, file, a Schematic (SCH), an Embedded processor (XMP) or an Electronic Design Interaction Format, if the synthesis process is done outside the Project Navigator. In HDL and schematic top-level designs, for the lower-level source files different types are available depending on project properties (top-level module type, device type, synthesis tool, and language); some source types launch additional tools to help the user to create the file [32].
The choice for the GBT project is a net-list of VHDL files, organized hierarchically from the top architecture to the lower components.
During the creation of the design project, ISE requires to enter the information about the

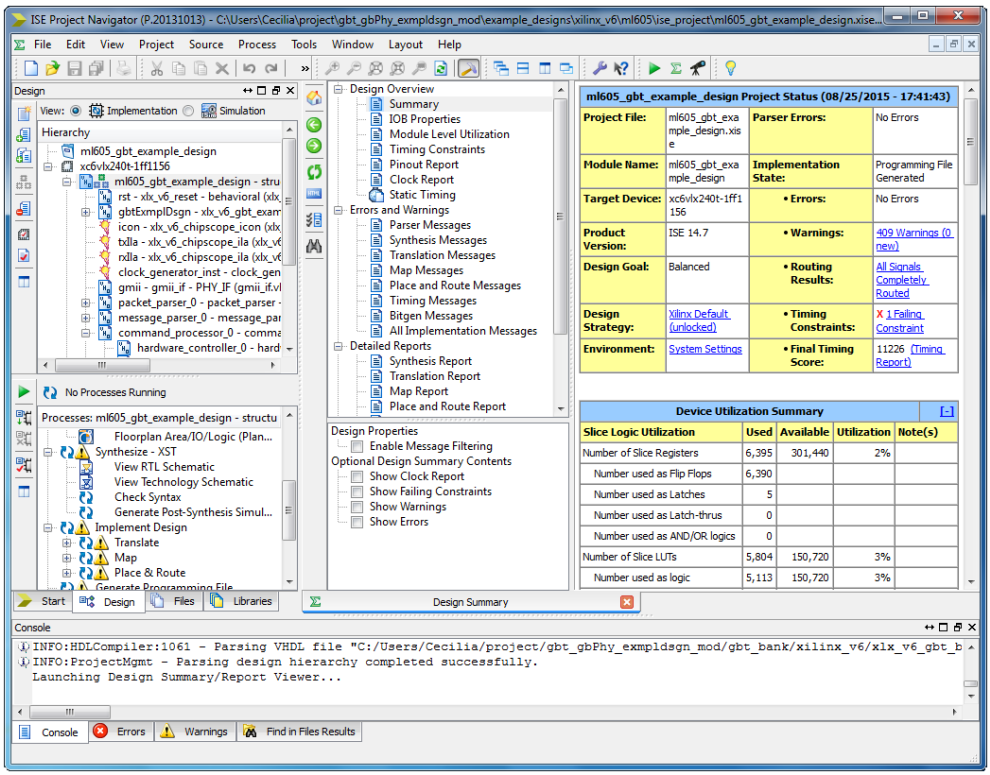


Fig. 4.2 ISE user interface. The program gives the possibility of managing different source files and organizing them in a hierarchical structure. The objective is to create a bit-file to program on hardware.

design, such as the top level format and the description language adopted, and the information about the device on which the code will be implemented. After the completion of these settings, it is possible to add new files to the project, to import existing files from other projects or to edit the already existing files.
The chain of processes necessary to implement the code in a Xilinx device is displayed in Fig. 4.3.

Development chain

The aim of the *synthesis process* is to compile the design in order to transform the VHDL sources into an architecture specific net-list, generating a file to be used in the next steps of the implementation. The synthesis accomplishes the following list of operations: it analyses the code, checking the syntax errors and attempting to recognize all the logical structures, translates the behavioural description into a gate-level net-list, using the standard cells provided by the software library, and generates a Register Transfer Level (RTL) and a Technology schematic of the circuit. The *RTL* schematic is a representation of the circuit made in terms of generic symbols that are independent of the target Xilinx devices (adders,

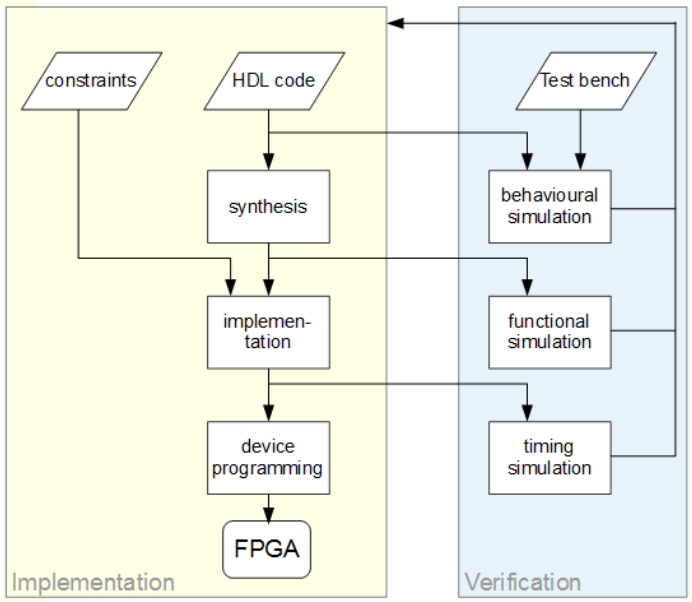


Fig. 4.3 ISE chain of processes.

multipliers, counters, AND and OR gates). The *Technology* schematic, created after the optimization and technology targeting phase of the synthesis process, is a representation of the design in terms of logic elements optimized to the target Xilinx device (for example in terms of Look Up Tables, carry logic, I/O buffers, and other technology-specific components). While the RTL schematic is used to understand the interpretation of the code and the resulting usage of resources, the Technology schematic allows to recognize the best available structure to obtain the best performance circuit, accordingly to the synthesis constraints.

The *implementation process* follows the synthesis and is made up of three steps:

1. Translate
2. Map
3. Place and Route

The Translate process merges all of the input net-lists and design constraint details and it outputs a Native Generic Database (NGD) file, that can be mapped to the targeted device family. The Map program maps the logic defined in the NGD files into a specific FPGA element, e.g. Configurable Logic Blocks or Input/Output Blocks (see section 4.2.1), generating a Native Circuit Description (NCD) file. Finally the Place and Route process takes a mapped NCD file and places and routes the design, obeying the imposed timing and spatial constraints. It produces a NCD file to be used by the programming file generator.

The last process, *"Generate Programming File"*, recasts the NCD file to produce the bitstream file, finally used to program the FPGA. After the generation of programming file, the target Xilinx device must be configured; this operation can be directly done from a host-computer with a download cable, using iMPACT. *iMPACT* is a Xiling supporting tool, operating in Boundary-Scan mode to manage the configuration and the programming of several devices (FPGAs, CPLDs and PROMs).

Simulation

To verify the logical functionality and the correct timing of the design, the synthesized code can be simulated using the provided *ISIM* simulation software. To this purpose, a specific VHDL code, called *test-bench*, has to be written; the test-bench code contains the definition of the Unit Under Test (UUT), i.e. the chosen component to be analysed, and of the stimulus required to activate the process.
As shown in Fig. 4.3, other two simulation stages in different steps of implementation are available: the functional and the timing simulation. The functional simulation allows to check the circuit functionality, independently of the component used and the signal propagation delays. While the timing simulation is the closest emulation of the design that will be downloaded to a device. It allows to check that the implemented design meets all functional and timing requirements and behaves as expected. Performing a thorough timing simulation ensures that the finished design is checked, to avoid post-synthesis and implementation functionality changes, or missing and improperly applied timing constraints.
Functional and timing simulation are performed after the implementation process.

Constraints

The Constraints are conditions imposed on the synthesis or implementation processes. Implementation constraints are the main important type for our purposes; they consist in instructions given to the FPGA implementation tools to define the guidelines for mapping, placement and routing processes [33].
In this work, since the pin assignment of a top-level I/O ports and the specifics of clock properties are two important issues to pinpoint, the following kinds of constraints are used:

- Placement constraints
- Timing constraints

During the implementation process, the I/O (Input/Output) signals of the top-level module must be mapped to a physical pin of the FPGA device, taking into account that peripherals'

I/O signals are already permanently connected to the designated FPGA pins on the used prototyping board. This is done by the specification obtained with the placement constraints and by information about operational voltage of each pin (taking in account that all the I/O pins in a specific area of the FPGA share the same voltage). To help the setting and modification of the placement constraints, Xilinx provides the Plan Ahead tool, which performs the analysis of device resources and the assignment of I/O pins.

Timing constraints, concerning the information about clock period, input jitter and selection of the clock active edge, set how the logical delay and route are constrained. Also the relation between the clock signal and data input or output can be configured using a proper timing constraint: to control the propagation delay of data, an offset value is set. For input signals, it is related to the setup time and it represents the minimum duration the signal must be stable before the clock edge; whereas for output signals it is the time taken by a signal to become valid after the clock edge.
The timing constraints are editable directly from the project navigator, or by using the constraints editor.

The constraints information is stored in a text file with an extension UCF (User Constraint File).

4.1.2 GBT-FPGA code study

The *Example design* follows the same concept of unification as the GBT-FPGA Core: all the targeted projects share the same structure and the source files implementing the standard components, while vendor specific files, such as those referred to the MGT configuration, are not shared. The first step for implementation is to create the project made of a long description list, containing all the HDL source files (with their hierarchical concatenation), the resources to manage the system clocks and the constraints files.
The design has been configured, entering the Top-Level source type (HDL) and the specifics for the used FPGA (family, device code, package and speed).
The top level of the GBT-FPGA *Example design* ("ml605_gbt_example_design.vhd"), thought for interfacing the design with the external technologies, shows the connectivity between the *Example design* and the hardware components of the FPGA-based evaluation board.
In the top architecture the main file is the "xlx_v6_gbt_example_design.vhd", that contains the GBT Bank and the other support modules, including:

- the reset, to manage the synchronous reset for each component inside this level;
- the Tx-PLL (Phase-Locked Loop), to generate the clock resources;

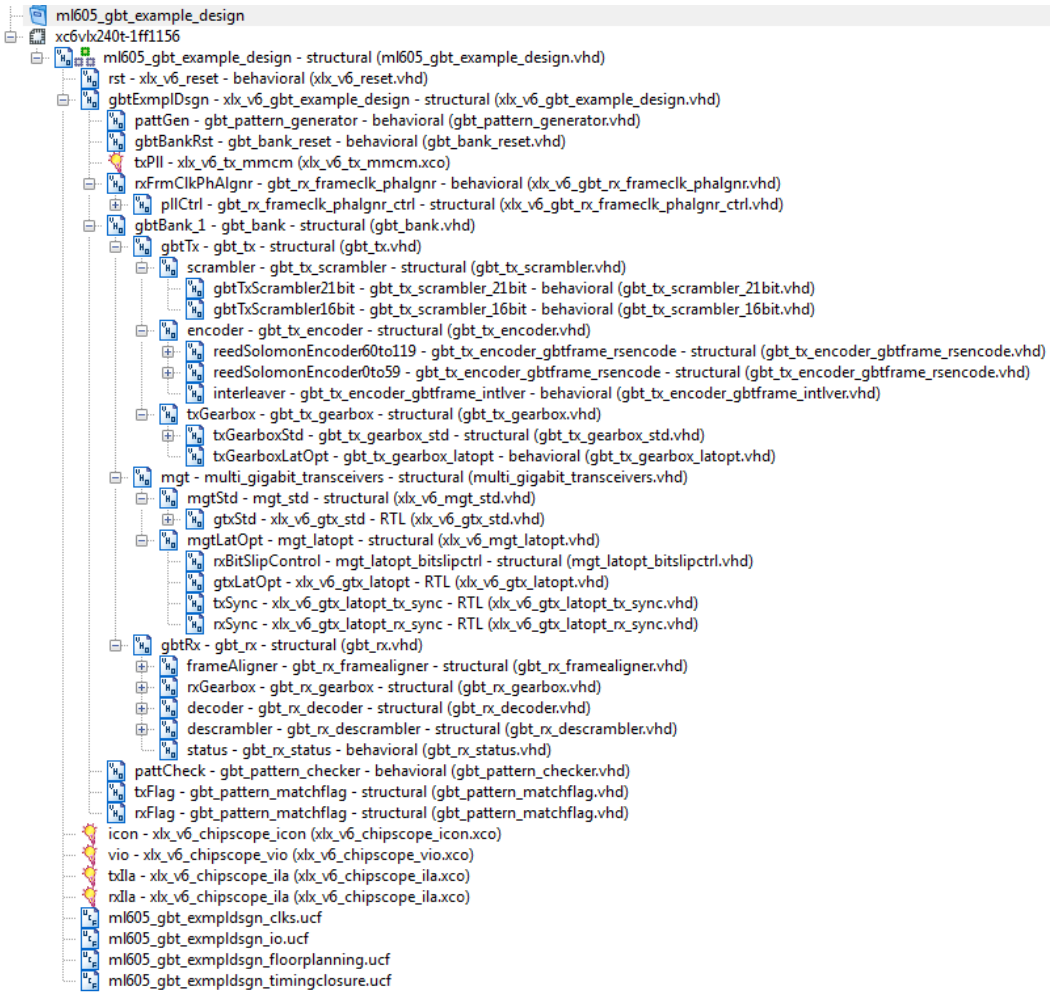


Fig. 4.4 Hierarchical distribution of the source files for the GBT-FPGA *Example design*.

- the clock phase aligner, to reconstruct the clock signal after transmission in Latency-Optimized mode;
- the pattern generator and the pattern checker, to emulate the data incoming from the GBTx and verify their right transmission;
- the match-flags components, to have further control on the occurred transmission and reception.

The study of this file gives a complete understanding of the interaction and connectivity between the GBT Bank and the other modules of the *Example design* [7].

To configure the communication link, a user setup file, gathering all the device dependent constant and attributes, is provided for all the GBT-Banks. The idea is to keep each GBT Bank as an independent entity in terms of logic and clocking resources. Considering the

architectural limitation of each targeted FPGA, the maximum number of GBT Links per GBT Bank is device dependent: for the Xilinx Virtex6 FPGA, every GBT Bank can contain at maximum 4 GBT Links. If the application requires more than 4 Links, it is possible to instantiate GBT Banks in parallel, in number depending on the FPGA.
As displayed in Fig. 4.5, the chosen configuration is one GBT Bank including one GBT Link, operating in Standard mode. For transmission and reception the GBT Frame encoding has been selected.

```
--================================================================================================--
--###################################   Package Declaration   ####################################--
--================================================================================================--
package gbt_banks_user_setup is
   --================================== GBT Banks parameters ==============================--

   --======================--
   -- Number of GBT Banks --
   --======================--
   constant NUM_GBT_BANKS                      : integer := 1;

   --==================--
   -- GBT Banks setup --
   --==================--
   constant GBT_BANKS_USER_SETUP : gbt_bank_user_setup_R_A(1 to NUM_GBT_BANKS) := (

      -- GBT Bank 1:
      --------------

      1 => (NUM_LINKS                          => 1,
            ------------------------------------
            TX_OPTIMIZATION                    => STANDARD,
            RX_OPTIMIZATION                    => STANDARD,
            ------------------------------------
            TX_ENCODING                        => GBT_FRAME,
            RX_ENCODING                        => GBT_FRAME,
            ------------------------------------
            STD_MGT_REFCLK_FREQ                => FREQ_240MHz,
            ------------------------------------
            SPEEDUP_FOR_SIMULATION             => false)
   );

   --================================================================================--
end gbt_banks_user_setup;
--================================================================================================--
--################################################################################################--
--================================================================================================--
```

Fig. 4.5 The link configuration is set in the "xlx_v6_gbt_bank_package.vhd" package file. It is possible to set: the number of GBT Banks and Links, the optimization mode, the encoding for transmitter and receiver and the reference clock for the MGT.

Clock scheme

The usage of clocking resources strongly depends on the chosen designs: device, operation mode (Standard or Latency-Optimized), number of links and general scheme of the system play an essential role in the clocks definition.
Since the device foresees different clock domains, the principal source of latency uncertainty issues is the clock domain crossing (CDC), which consists in the transition made by a signal in a synchronous digital circuit from one clock domain to another. So, in order to minimize the impact of CDCs, one of the most critical aspects in logic design is a proper study of the

clock resources to reduce the number of clock domains as much as possible. The bigger source of uncertainty is the MGT component, for its complex internal and not modifiable scheme, that requires a high number of clock domains. The optimization for MGT has been performed by selecting the frequency of the different clocks and the width of the data buses.

The system needs three principal clocks (Fig. 4.6):

- *the fabric clock*
  it is a 125 MHz clock, used by the external reset;

- *the frame clock*
  it is a 40 MHz clock, used by the logic components of transmitter and receiver and by the support modules of the system. It is generated by the TxPLL, dividing the external *"MGT_ref_clock"* (240 MHz) by a factor 6;

- *the word clock*
  it is a 240 MHz (or 120 MHz clock) clock, used by the transceiver logic. It is generated inside the MGT itself from the *"MGT_ref_clock"*.

It is interesting to note that the frame and word clock domains are generated multiplying, dividing and recovering a single clock source. This allows the system to maintain the fixed phase relationship between clocks required for the right functionality. The non-deterministic phase difference between the derived and source clocks is avoided synchronizing the reset of the generated clocks with the rising edge of the source.
In cases where this approach is not possible (e.g. the receiver clocks are recovered from the data stream), there is a reference signal to indicate when the rising edge of the source clock occurs. For example, the synchronization of the reconstructed Rx_frame clock is based on a flag signal, active every time that the header of the data frame (which is aligned with the rising edge of TX_frame clock) is detected by the GBT RX control logic.

It is important to remark that the clocks scheme of the latency-optimized version is far more complicated than the presented one, because it requires dedicated clock phase monitors and aligners for the correct functioning of the GBT Links. In addition, in multi-link implementations of latency-optimized version the clocking resources utilization is higher compared with the standard-version, since the dedicated clock resources cannot be shared by the different GBT Links from the same GBT Bank.

Reset scheme

The *Example design* project provides two consecutive reset blocks, configured to execute the reset sequence of the GBT-FPGA Core. The first block is a *General Reset*, governed by

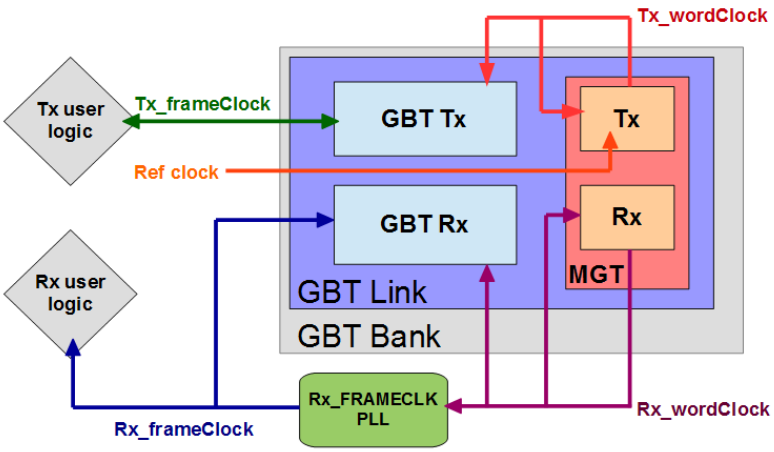


Fig. 4.6 Clocks scheme for single-link implementation of standard version.

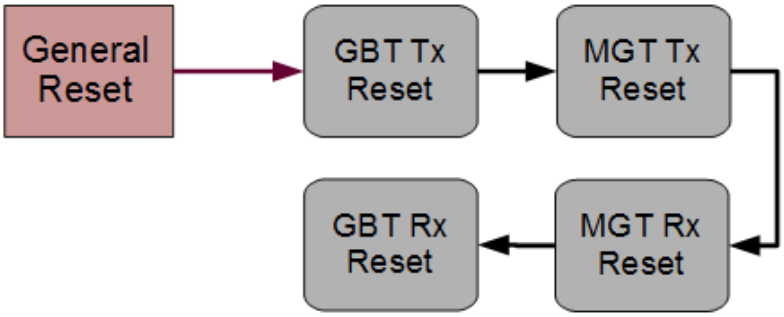


Fig. 4.7 Reset scheme.

the Fabric clock, that activates the second block, the *GBT Bank Reset*. It performs a reset sequence based on four sequentially steps at 40 MHz (Fig.. 4.7).
The structure of the reset sequence has been designed in order to have a proper and sequential initialization of the different components of the link. It consists in:

1. reset of the transmitter user logic and its supporting components (pattern generator and $Tx_{matchflags}$), to provide stable data to the MGT;

2. reset of the transmitter component of the MGT, to send a correct and stable data stream to the receiver;

3. reset of the receiver component of the MGT, to initialize the CDR, enabling the separation from the incoming data and the reconstruction of the clock signal for the receiver logic;

4. reset of the receiver, to synchronize its operations with the MGT, and of the Rx support components.

Each of these steps can be also singularly executed, in case of loss of synchronization or alignment in the data coming from the transmitter.

4.2 Study of the Virtex6 FPGA

4.2.1 FPGAs overview

Since the early '70s, a branch of electronics has been evolving to satisfy the demand for more and more performing chips whose key feature is the programmability of different logic functions. By programmability, we mean the ability of a designer to affect the logic behaviour of the device after it has been produced in the factory. Historically, the first improvement in the direction of programmability came with the introduction of gate arrays, which were chips filled with NAND ports interconnected as needed during the production to generate different logic functions. The next step was the introduction of Programmable Logic Arrays (PLAs) in the 1980s. A PLA is a two-level AND-OR structure with user-programmable connections. An improvement in performance and cost over the PLA structure were the *Programmable Array Logic* (PAL) devices. Today, these devices are collectively called *Programmable Logic Devices* (PLDs). Later *Complex Programmable Logic Devices* (CPLDs), that are clusters of PLD circuits, were developed to satisfy the increasing demand of programmable logic in a chip, required by the technology growth [23].

The last progress stage is represented by the the *Field Programmable Gate Arrays* (FPGAs), introduced for the first time in the market by Xilinx in 1985. A typical FPGA consists of three main resources: the configurable logic blocks, their programmable interconnections and the I/O block to configure the device pins. The FPGA logic blocks are generally organized in a two-dimensional array and connected by horizontal and vertical routing channels, as shown in Fig. 4.9. The routing channels include programmable switches that allow to configure the interconnection between the logic and I/O blocks.
In addition, modern FPGAs typically include other support blocks, such as static Random Access Memories (RAMs), components for the clock management (Digital Clock Managers and Phase Locked Loops) and hardwired Intellectual Property (IP) cores for functions recurrent in many designs.
The specific FPGA architecture depends on the firm producing the design; actually the main producers are: Altera, Microsemi and Xilinx. The latter fulfills nowadays half of the entire programmable logic market (51%).

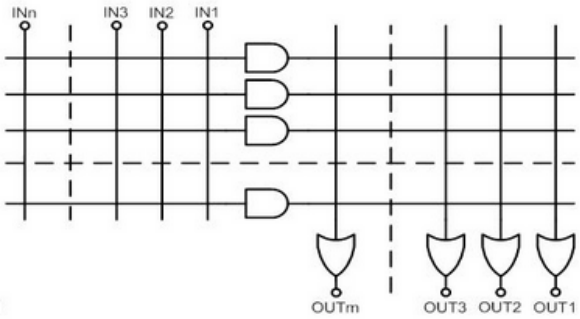


Fig. (a)

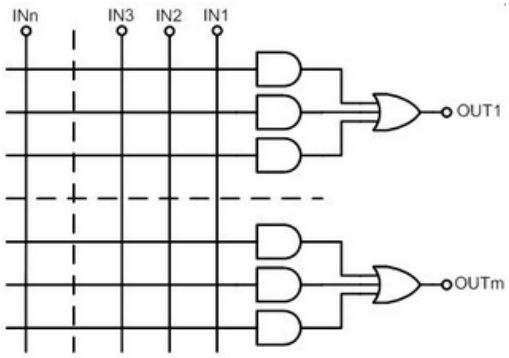


Fig. (b)

Fig. 4.8 PLA (fig.a) and PAL (fig.b) circuits.

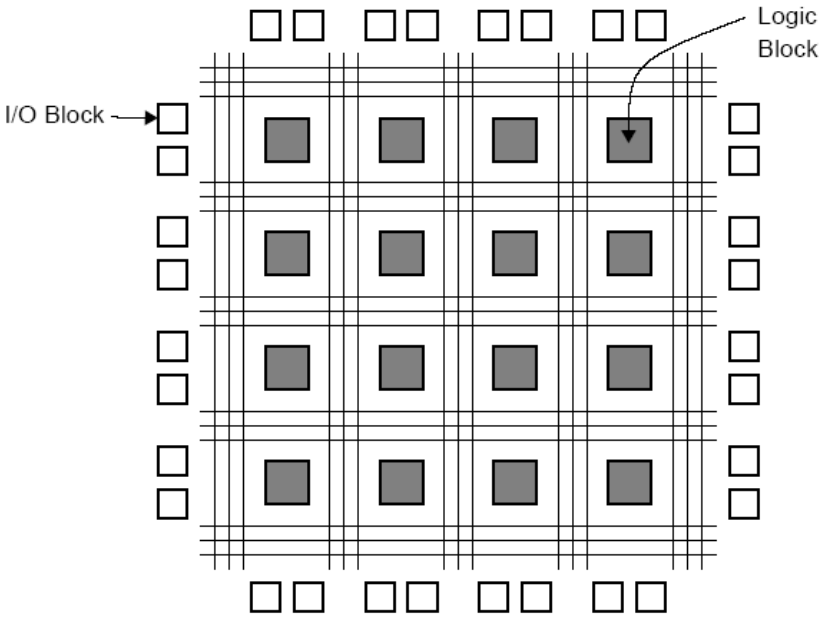


Fig. 4.9 Schematic representation of a generic FPGA architecture.

The chosen device for the GBT-FPGA implementation is an FPGA of the **Virtex6** family from Xilinx. This high performing FPGA family, built on a 40 nm copper process technology, is divided in three distinct sub-families (LTX, SXT, HXT) that incorporate different features to address the needs of a wide variety of advanced logic design. The architecture and the system blocks of the used FPGA are described in the following section.

Device	Total Slices	SLICELs	SLICEMs	Number of 6-Input LUTs	Maximum Distributed RAM (Kb)	Shift Register (Kb)	Number of Flip-Flops
XC6VLX75T	11,640	7,460	4,180	46,560	1,045	522.5	93,120
XC6VLX130T	20,000	13,040	6,960	80,000	1,740	870	160,000
XC6VLX195T	31,200	19,040	12,160	124,800	3,140	1,570	249,600
XC6VLX240T	37,680	23,080	14,600	150,720	3,770	1,885	301,440
XC6VLX365T	56,880	40,360	16,520	227,520	4,130	2,065	455,040
XC6VLX550T	85,920	61,120	24,800	343,680	6,200	3,100	687,360
XC6VLX760	118,560	85,440	33,120	474,240	8,280	4,140	948,480
XC6VSX315T	49,200	28,840	20,360	196,800	5,090	2,545	393,600
XC6VSX475T	74,400	48,840	30,560	297,600	7,640	3,820	595,200
XC6VHX250T	39,360	27,200	12,160	157,440	3,040	1,520	314,880
XC6VHX255T	39,600	27,400	12,200	158,400	3,050	1,525	316,800
XC6VHX380T	59,760	41,520	18,240	239,040	4,570	2,285	478,080
XC6VHX565T	88,560	63,080	25,480	354,240	6,370	3,185	708,480

Fig. 4.10 Table of the FPGA of the Virtex6 family; in red the used one is highlighted.

4.2.2 Virtex6 specifics

Architecture

The Virtex FPGAs' elementary resource is the *Configurable Logic Block* (CLB). Each CLB is connected to a switch matrix for the access to the general routing matrix [25]. The internal structure of a CLB element, as shown in Fig. 4.11, consists in two *slices* arranged in columns, with no direct connections to each other and independent carry chains.

The slices are characterized by big sets of elements and connections to provide logic, arithmetic, and ROM functions; some slices also support two additional functions: storing data using distributed RAM and shifting data with 32-bit registers. Slices that support these additional functions are called SLICEM; others are called SLICEL.

Each slice contains three block types, connected by specific carry logics:

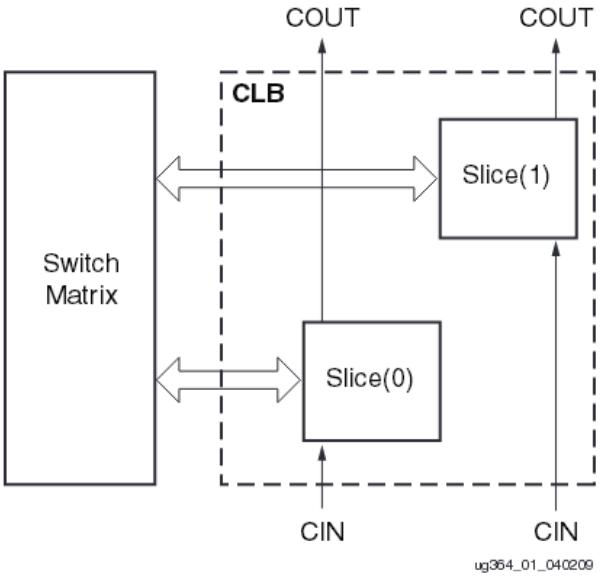


Fig. 4.11 CLB structure; for each CLB, slices in the bottom are labeled as SLICE(0), and slices in the top of the CLB are labeled as SLICE(1).

- *four logic-function generators*
  Each function generator is a look-up table with six independent inputs and two independent outputs. These blocks can implement one arbitrary six-input Boolean function or two five-input Boolean functions, that share the same inputs. For the six-input function, only the second output is used, while both outputs are employed for the five-input ones. Signals from both the outputs can exit the slice, while only the second output is connected with an XOR dedicated gate, the tone of the multiplexers or their carry-logic and the input of a storage element.

- *three wide-function multiplexers*
  The multiplexers (F7AMUX, F7BMUX, and F8MUX) are used in addition to the basic LUTs, to combine up to four function generators to provide up to eight-input functions in a single slice. Functions with more than eight inputs can be implemented using multiple slices.

- *eight storage elements*
  Even if the storage elements have common control signals clock (CLK), clock enable (CE), and set/reset (SR), they are divided in two different groups: four storage elements configurable as edge-triggered D-type flip-flops or level-sensitive latches and four additional storage elements that can only be configured as edge-triggered D-type

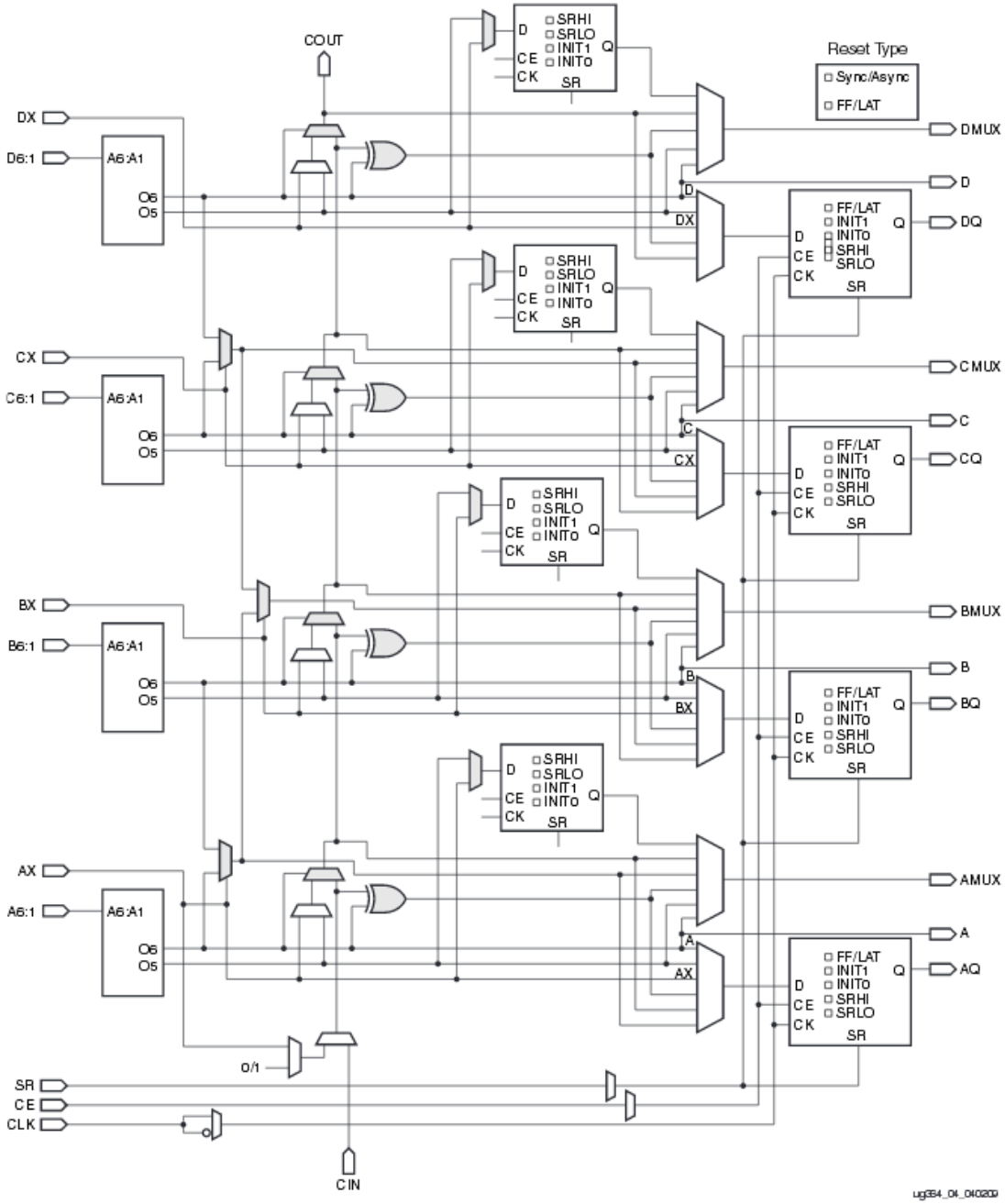


Fig. 4.12 SLICEL structure.

flip-flops. When the original 4 storage elements are configured as latches, these 4 additional storage elements can not be used.

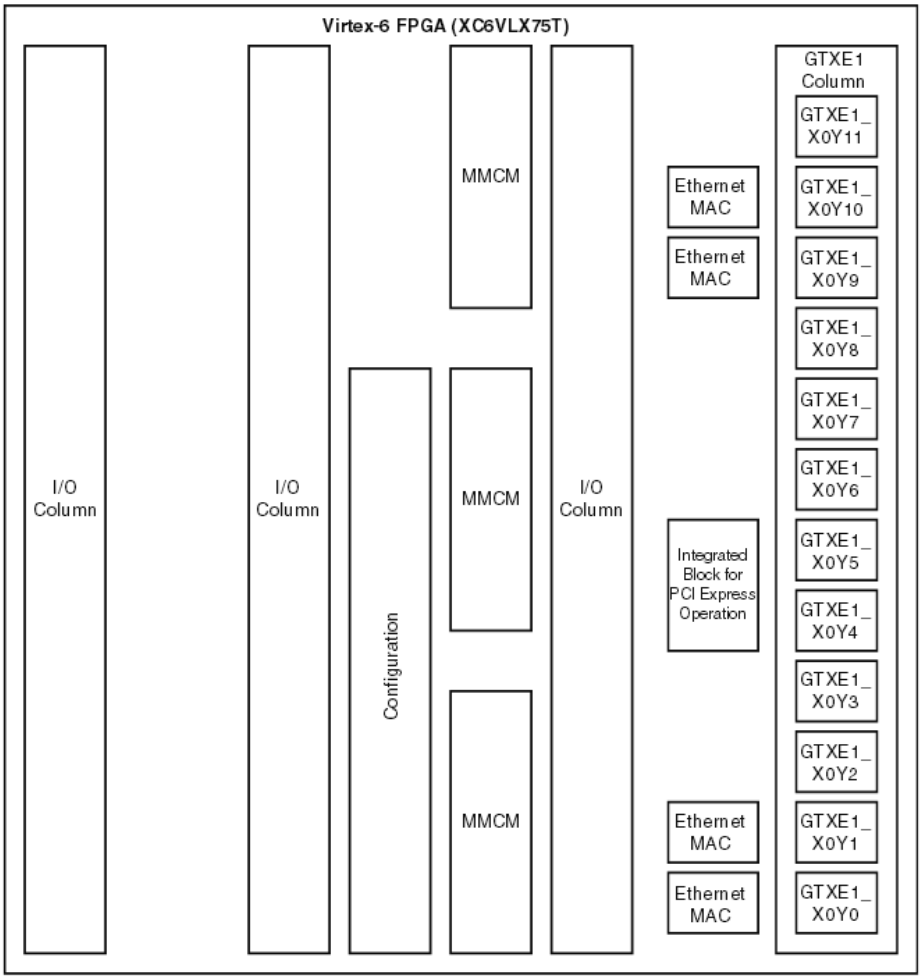


Fig. 4.13 Virtex6 fundamental functional blocks consist in I/O blocks, MMCM, configuration and GTX components.

It is also important to mention the Mixed-Mode Clock Managers (MMCMs), the Configuration component and the GTX transceivers, as shown in Fig. 4.13 [30].
The MMCMs serve for the general management of the clock signals, thus having as main functions the frequency synthesis for a wide range of frequencies, the jitter filtering for either external or internal clocks, and the clocks deskewing [26].
The Configuration module stores the configuration data bitstream, generated by the BitGen process of ISE. The bitstream is loaded on the Configuration module by a non-volatile memory device or by an external source as a microprocessor or a PC. Since the information is memorized in CMOS latches, the FPGA must be reconfigured after it is powered down.

Moreover special configuration bits must be set depending on the chosen boot path for the FPGA.
Finally, the GTX transceivers are the Virtex6-specific MGT devices. Playing an essential role in the GBT implementation, a detailed description will be given in the next paragraph.

GTX transceiver

On the used Virtex6 there are twenty GTXs, organized in five sets of four transceivers sharing two differential clock pin pairs. These components are highly configurable to support many different protocols or to allow the user to create a custom one. Each GTX transceiver includes an independent transmitter and receiver (Fig. 4.14), which have a similar structure: both consist of a Physical Coding Sublayer (PCS) and a Physical Medium Attachment (PMA).

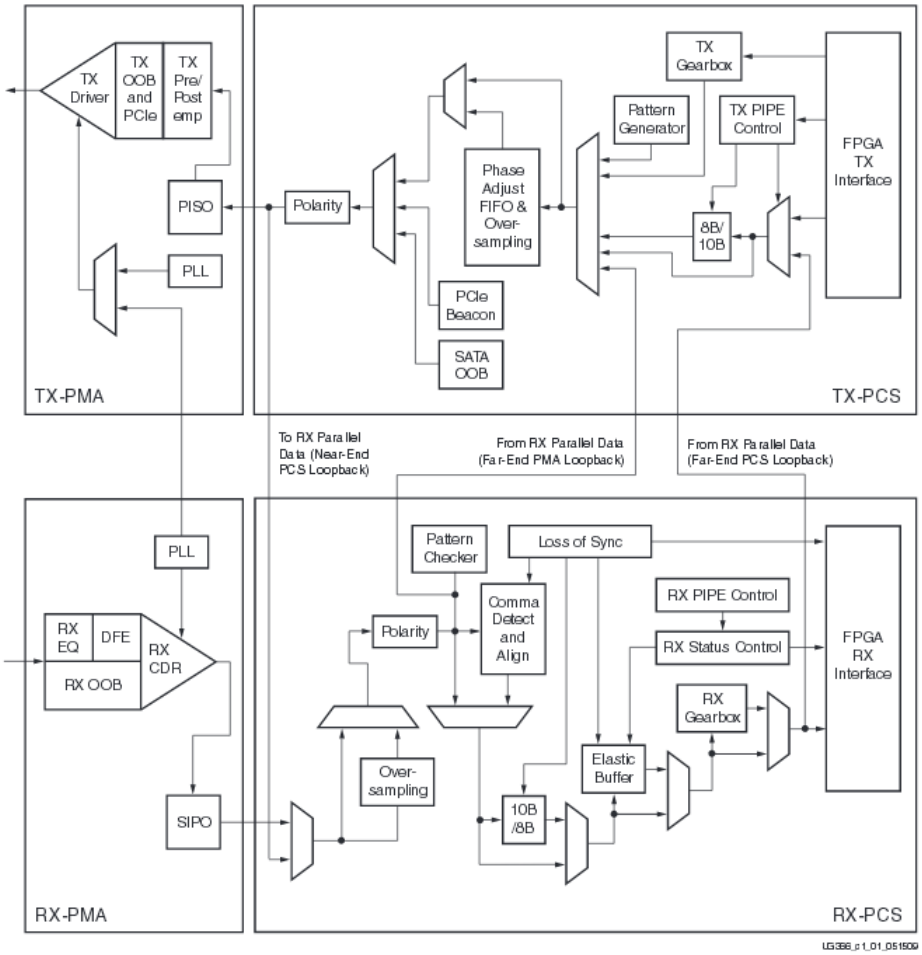


Fig. 4.14 GTX internal transmitter and receiver.

The PCS sublayer is responsible for the coding or decoding procedures, functions not

used in the GBT configuration. The PMA, instead, is the lowest sublayer maintaining the independence from the physical medium and manages the data serialization and de-serialization [27].
Parallel data flow from the FPGA into the transmitter interface, through the PCS and PMA, and then out the Tx-driver as high speed serial data, with line rates from 600 Mb/s to 6.6 Gb/s and fixed latency mode. The opposite operations are carried out by the receiver.
To configure the transceiver interface and its clock resources a several number of attributes is set during the phase of design implementation. Data to be serialized enter in the GTX on the rising edge of *"TXUSRCLK2"* from the TXDATA port, whose width is configurable by the TX_DATA_WIDTH attribute (8, 10, 16, 20, 32, and 40 bits).
The TX data path, which can consist of 1, 2 or 4 bytes, has two internal parallel clock domains: the PMA parallel clock domain (XCLK) and the TXUSRCLK domain, that could imply a phase difference. To resolve this problem, the GTX transceiver includes a TX buffer and a TX phase-alignment circuit. The first has the advantage to be robust and easy to operate, while the second requires extra logic and additional constraints on clock sources but can precisely work with a critical situation of low latency. For this reason the use of the buffer is preferred in the standard mode of the GBT-FPGA. The buffer is used also as oversampling circuit when a low line rate is required, because, being the GTX designed for high line rate, it is necessary to have a supplement component to allow the transmission and to maintain at the same time parallel and serial clock in the valid PLL frequency range.
In some operating modes, a second parallel clock (TXUSRCLK) must be provided for the internal PCS logic in the transmitter.

The generation of serial and parallel clocks used by the PMA and PCS blocks is made by a Phase-Locked Loop (PLL), Fig. 4.15. Each GTX transceiver contains one TX PLL and one RX PLL, which allow the TX and RX data paths to operate in asynchronous frequencies using different reference clock inputs [27]. For applications where the TX and RX data paths operate in the same line rate range, the RX PLL can be shared between the TX and RX, but only if they are placed in the same transceiver.
The PLL has a nominal operation range between 1.2 to 2.7 GHz for -1 speed grade devices, such as our Virtex6, but this value can be modified using the attribute "TX-PLL_DIVSEL_OUT".
The PLL operating mode is based on a loop circuit composed by two main blocks: a Phase Frequencies Detector and a Voltage Controlled Oscillator (VCO). The PFD compares the reference clock and the VCO feedback clock, generating an error signal. This signal is used by the VCO to determine if the desired frequency has been achieved or if corrections are necessary.

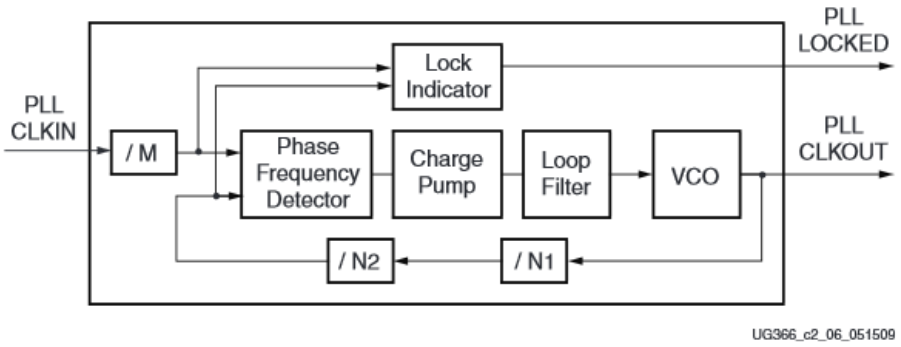


Fig. 4.15 PLL scheme.

The input clock can be divided by a factor of M before feeding into the phase frequency detector. The feedback dividers, N1 and N2, determine the VCO multiplication ratio and the PLL output frequency.

$$F_{PLL-ClkOut} = F_{PLL-ClkIn} \cdot \frac{N_1 \cdot N_2}{M}$$

The PLL output can be further divided by a factor D (1, 2 or 4) to produce the desired line rate.

$$F_{linerate} = \frac{F_{PLL-ClkOut} \cdot 2}{D}$$

The PLL output frequency, divided by the internal data width, constitutes the timing reference for loading the parallel data on the PMA parallel clock (PISO). The PMA clock can be extracted from the GTX using the multiplexer and the extracted clock is the TXOUTCLK, mentioned before. In the GBT design this clock is brought outside the MGT and becomes the word clock of the system.

$$TXOUTCLK = \frac{F_{PLL-ClkOut}}{2 \cdot D \cdot InternalDataWidth}$$

4.2.3 Hardware resources

ML605 evaluation board

To facilitate the user interfacing with the FPGA and the test, the device is inserted in an evaluation board provided by Xilinx. The *Virtex6 FPGA ML605 Evaluation Kit*, including

all the basic components of hardware, design tools and IP, is thought for system designs that demand high-performance, serial connectivity and advanced memory interfacing [29].

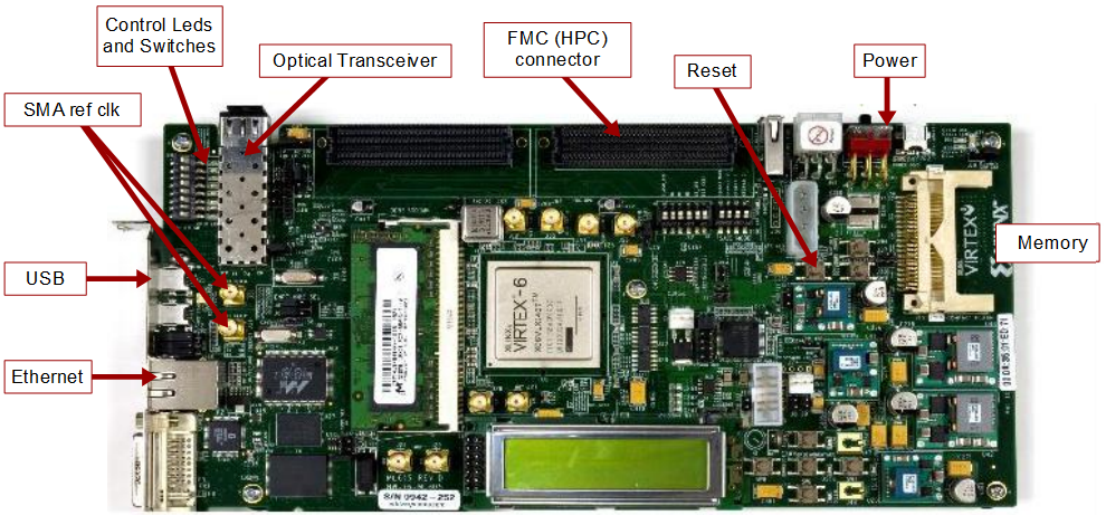


Fig. 4.16 ML605 evaluation kit; in the figure the more relevant component of the borard are indicated.

As shown in Fig. 4.16, among the ML605 features, which are commonly used by many embedded processing systems, those of more interest for the GBT are:

- the *JTAG cable connector (USB Mini-B) and JTAG download circuit* are used for the code implementation on the FPGA. The JTAG cable makes also possible the communication with the PC in the debug phase;
- the *Ethernet port and PHY component* are used to create a high speed (1 Gb/s) communication link between the PC and the FPGA. A significant part of the performed tests is based on this link (see sec. 5.2);
- the *SMA pair connectors for the external clocking resources* serve the user to provide a 240 MHz differential clock;
- the *Integrated Circuit System for the 125 MHz clock* provides the clock signal that manages the general reset;
- the *Leds, buttons and switches* are used to manage the resets (it is possible to singularly reset one of the GBT Link components or to initialize the reset chain), to perform several controls on transmitter, receiver and MGT and to set some link properties (e.g. the transmission mode);

- the *FMC (FPGA Mezzanine Connector) high pin count (HPC) connector* is employed for the study of the transmitted and reconstructed clocks, since it is possible to connect to this pin external oscilloscope probes;
- the *Small form-factor pluggable (SFP) connector and cage assembly* are used for the optical conversion and light transmission/reception. In fact, this component is connected to the MGT Bank on the FPGA and the cage accepts SFP modules in order to connect the optical transceiver and the optical fibre.

AVAGO optical transceiver

An *AVAGO optical transceiver*, inserted in the SFP, is employed for the electrical-optical conversion and as support for the connection of the optical fibre.
The optical transceiver is composed by a transmitter section and a receiver section. The first includes a 850 nm VCSEL (Vertical Cavity Surface Emitting Laser) light source, and a commercial integrated circuit which converts a differential digital signal into an analog current for driving the laser diode. While the second contains a photodiode and a custom trans-impedance preamplifier, located at the optical interface, and a custom IC that provides post-amplification and quantization [2].

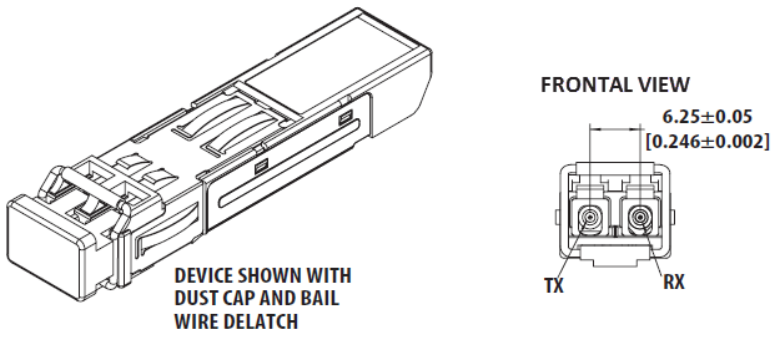


Fig. 4.17 Avago AFBR 5710LZ optical transceiver; the right figure shows the two connectors for the optical fibre.

Since the right working of the device is guaranteed up to 1.25 Gb/s, a study on the transceiver performances has been directed, using a Bit Error Ratio Tester (BERT). The BERT consists of a test pattern generator and a receiver used in pair. They are respectively connected to the transmitter and receiver part of the transceiver to be tested and the transceiver is loopback connected at the other end, using an optical fibre. Sending a known sequence from the pattern generator and verifying its correctness at the receiver, it is possible to

evaluate the transceiver Bit Error Ratio (BER).
It is the number of bit errors divided by the total number of transmitted bits, integrated on a time interval:

$$BER = \frac{number\,of\,error\,bits}{number\,of\,transmitted\,bits}$$

The results of this measure (reported in Tab. 4.1) show the necessity to decrease the GBT line rate. For this reason, the tests described in the chapter 5 have been carried out using a proper configuration of the GBTX and clocks resources in the FPGA to have a halved data rate (2.4 Gb/s).

Table 4.1 BER value for different data rates, obtained using the data pattern type "PRBS $2^{31}-1$" and having a gating time of ten seconds; the measures are integrated on a time of 40 min, which is enough to make the obtained values reliable with a confidence level of 95%. The data rate of 3.33 Gb/s is the BERT limit rate.

Data Rate (Gb/s)	**BER**
1.06	0
1.25	0
2.13	$4.6 \cdot 10^{-10}$
2.49	$7.4 \cdot 10^{-9}$
2.67	$2.3 \cdot 10^{-8}$
3.33	$4.5 \cdot 10^{-7}$

4.3 Implementation of the *Example design*

The Virtex6 FPGA has been implemented by loading the GBT bitstream, generated by ISE, into the internal memory, through a USB connection between the device and the PC. Before the implementation the hard cores of the FPGA (i.e. the GTX transceiver and the clock resources) have been configured to obtain the desired data rate for the link.
During the test, two configurations were used:

- 4.8 Gb/s configuration → Although it is the suggested configuration to obtain the nominal data rate, for our current resources it presents a significant number of error-bits in the data transmission. This configuration was thus replaced by the second in the debug phase;
- 2.4 Gb/s configuration → This guarantees a transmission with a negligible number of errors: supposing the optical transceiver to be the unique source of errors, the transmission takes place with a BER of $\sim 10^{-9}$.

In order to program the device downloading the bitstream file on FPGA, the used configuration mode is the *JTAG boundary scan*. This solutions uses the fewest FPGA pins, has flexible I/O voltage support, and is fully supported by *iMPACT* [1].
The JTAG boundary scan is used also for the debugging. In fact, devices containing boundary-scan logic, as the Virtex6, can send data out on I/O pins to test connections between devices at the board level and can be used to send signals internally to test the device-specific behaviour. In addition to testing, boundary-scan offers the flexibility for a device to have its own set of user-defined instructions.

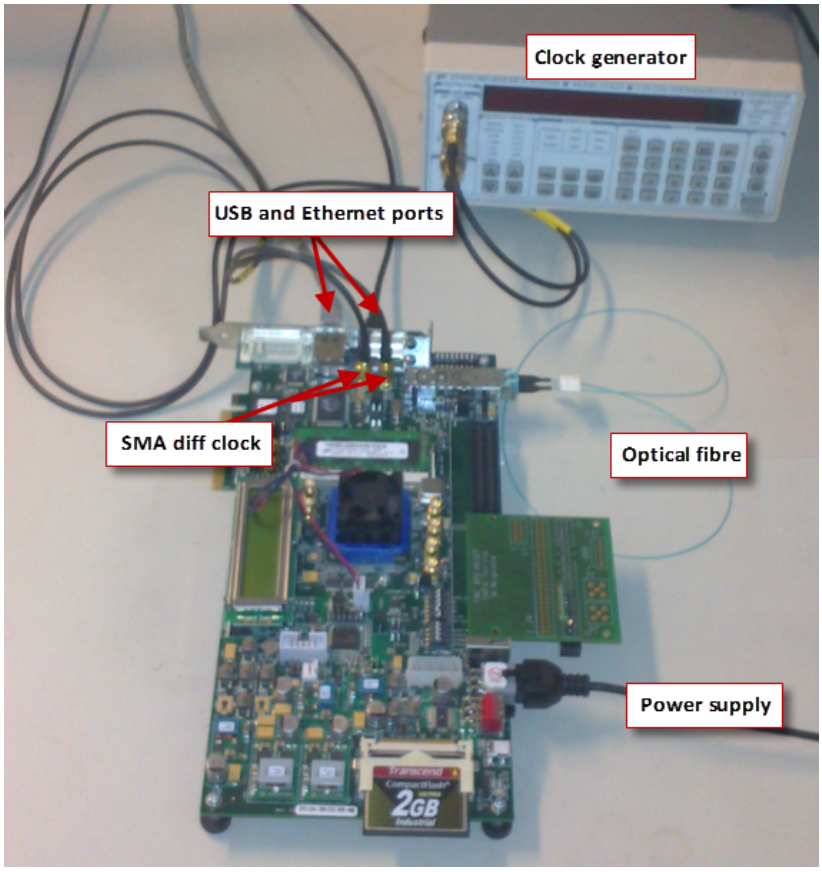


Fig. 4.18 Implementation setup.

[1] iMPACT is the Xilinx JTAG-based programming software; it allows to program the device, downloading the contents of BIT file, and verify the previous operation, reading back the contents of the device configuration and comparing them with the BIT file.

4.3.1 Cores configuration and resources utilization

Cores configuration

The study of the **GTX** interface made possible to evaluate the proper parameters to be inserted in the transceiver configuration in order to obtain the two line rates desired (2.4 and 4.8 Gb/s), as reported in Fig. 4.19.

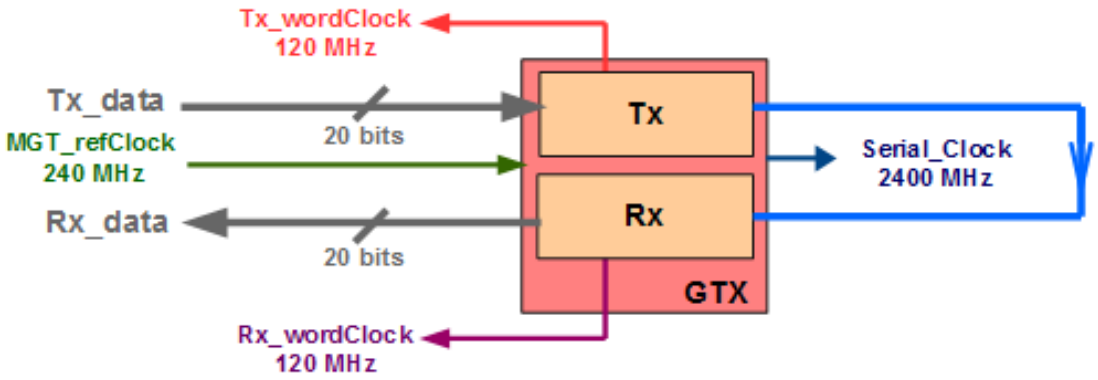


Fig. 4.19 GTX configuration scheme for the 2.4 Gb/s configuration; to obtain the nominal data rate of 4.8 Gb/s the Tx_wordClock and Rx_wordClock frequencies must be set at 240 MHz and the Serial_Clock one at 4800 MHz.

The *GTX transceiver wizard* for the Virtex6 FPGA was used to configure the GTX transceiver and to generate a VHDL GTX wrapper and a MMCM module to provide the required clock. The principal set parameters are listed in Tab. 4.2.

The second table shows the values of $F_{PLLclkOut}$, $F_{linerate}$, $F_{TXOUTCLK}$ (see section 4.2.2).

Table 4.2 GTX settings for the chosen GBT-FPGA configuration.

GTX attributes

attribute	value	effect
TX_DATA_WIDTH	20	20-bit input
InternalDataWidth	5	
D	1	$(2.4 \leq$ line rate $\leq 6.6)$ Gb/s
	2	$(1.2 \leq$ line rate $\leq 2.7)$ Gb/s
TXOUTCLK_CTRL	DIV2	2 byte of tx data path
TX_BUFFER_USE	TRUE	buffer used

GTX configuration

frequency	**settings**	**value**
$F_{PLLclkOut}$	N1=2 N2=5 M=1	2400 MHz
$F_{linerate}$	D=1 D=2	4800 MHz 2400 MHz
$F_{TXOUTCLK}$	$IntDataWidth$=5 and D=1 $IntDataWidth$=5 and D=2	240 MHz 120 MHz

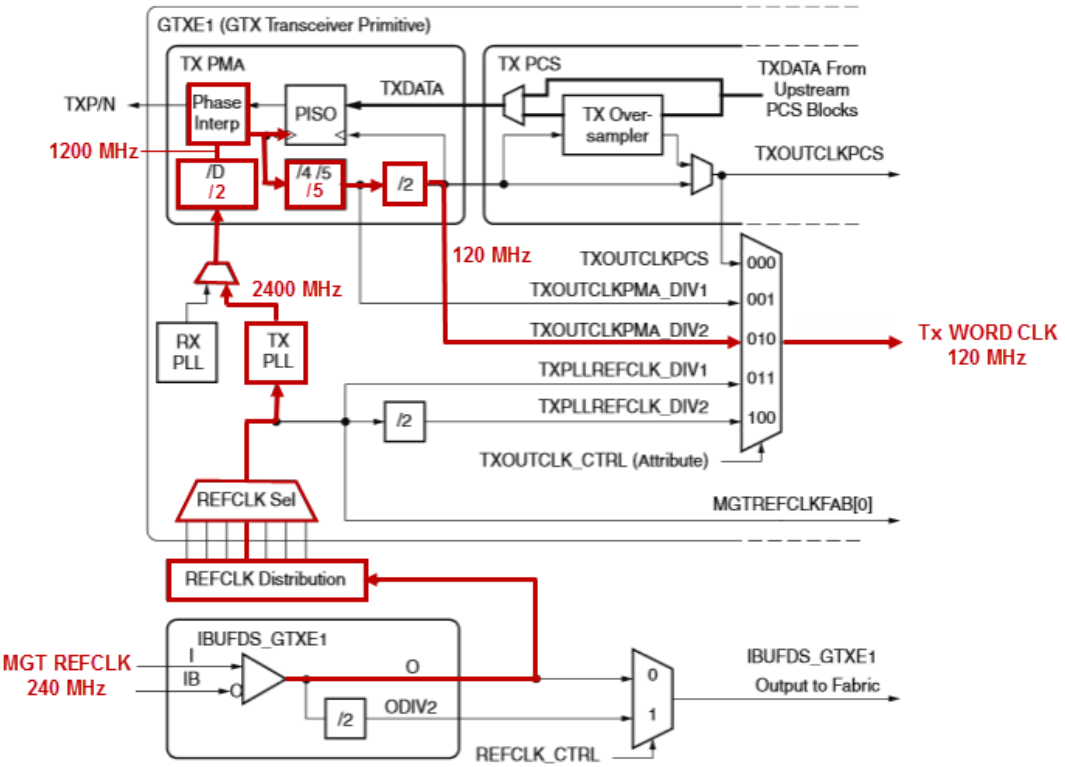


Fig. 4.20 Clock distribution network inside the GTX transceiver. In red, the followed path and the set parameters to obtain a line rate of 2.4 Gb/s are reported. The *MGT REF CLK* (240 MHz) in input defines the value of the *SERIAL CLK* (1200 MHz) and of the *Tx WORD CLK* (120 MHz).

Strictly adhering to GTX configuration rules which determine the frequency of the word clock, a proper setting of the **TxPLL** (section 4.1.2) is required, in order to maintain the desired relation between the frame and the word clocks. It is necessary to have a factor of 6 between the two clocks to have the gear-box segmenting the 120-bit frames in 20-bit words; this implies that:

- if the word clock frequency is 240 MHz, then the TxPLL must provide a 40 MHz clock (configuration for 4.8 Gb/s);
- if the word clock frequency is 120 MHz, then the TxPLL must provide a 20 MHz clock (configuration for 2.4 Gb/s).

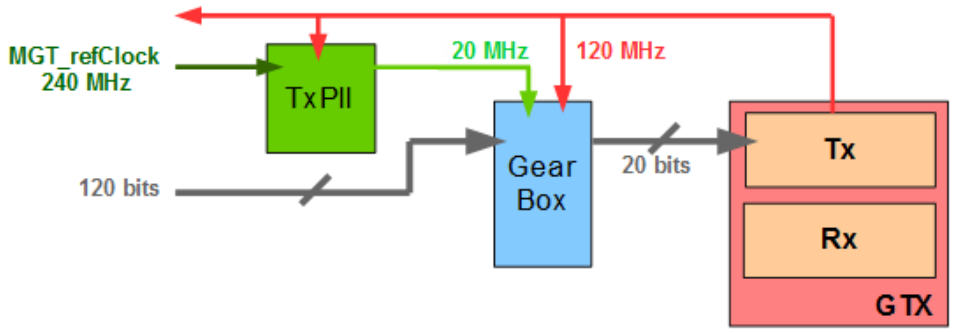


Fig. 4.21 TxPLL configuration scheme for the 2.4 Gb/s configuration; for 4.8 Gb/s configuration the TxPLL output must be 40 MHz since the wordClock frequency is 240 MHz.

Resources utilization

After the implementation, ISE automatically provides a *summary report*. By default, the Design Summary appears in the Workspace when the user opens a project, and it displays information specific to targeted devices and software tools, allowing to quickly access design overview information, reports, and messages.
Table 4.3 reports the device utilization summary after the implementation of the GBT *Example design* on the Virtex6 FPGA.
It is interesting to note that the implementation of a single GBT Bank with a single Link requires a low amount of the total Virtex XC6VLX75T resources. This is clearly visible also in Fig. 4.22, that depicts a schematic representation of the FPGA highlighting the used areas.

Table 4.3 Device utilization summary; the data are extrapolated from the Summary of the Design Overview reported by ISE after the implementation processes

Slice logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	2,240	301,110	1%
Number of Slice LUTs	2,441	150,720	1%
number used as logic	1,856	150,720	1%
number used as Memory	349	58,400	1%
Number of bonded IOBs	16	600	2%
number of LOCed IOBs	16	16	100%
Number of bonded IPADs	6	6	100%
Number of RAM/FIFO 36E1	16	416	3%
number of RAM 36E1	16		
number of FIFO 36E1	0		
Number of RAM/FIFO 18E1	2	832	1%
number of RAM 186E1	2		
number of FIFO 186E1	0		
Number of BUFG	9	32	28%
Number of GTXE	1	20	5%
Number of BUF_GTXE	2	12	16%

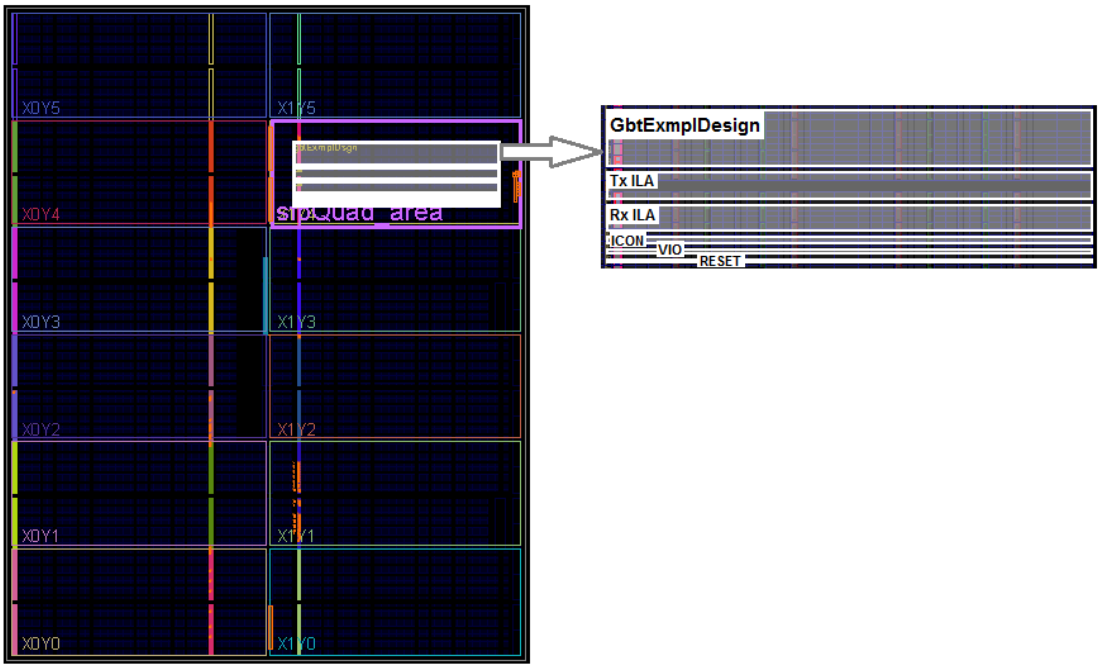


Fig. 4.22 Usage of Virtex6 resources; the map has been obtained using the PlanAhead tool from Xilinx.

Chapter 5

Analysis of the implemented code

The test consists in two main phases: the debugging of the circuit, directly inspecting the internal structure through the use of the ChipSchope Xilinx development tool, and the data transfer via an Ethernet port. In this second phase, an acquisition system has been created and a communication interface has been developed using the LabView control software. The procedure carried out for the test is shown in Fig. 5.1.

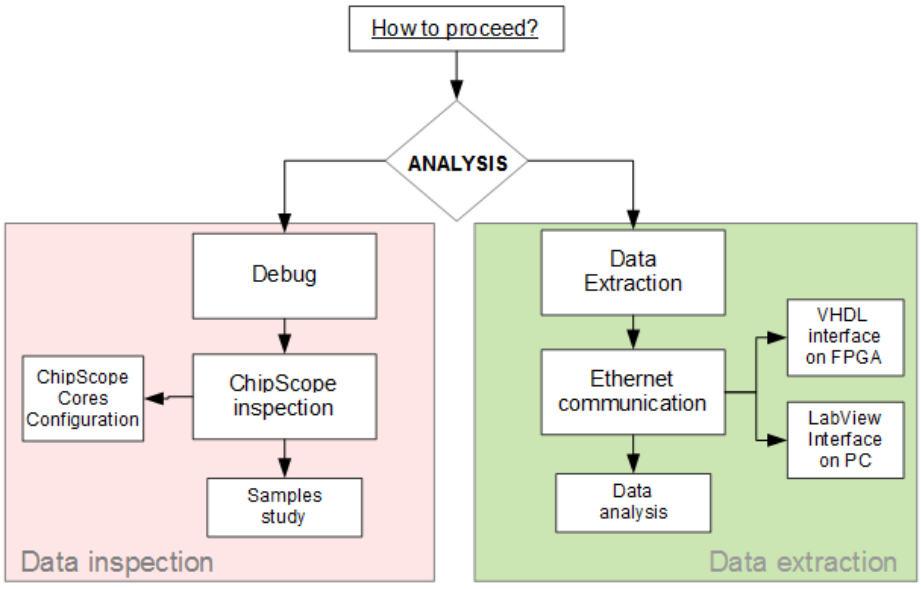


Fig. 5.1 Scheme of the followed procedure for the implementation.

5.1 Debug

5.1.1 CHIPSCOPE cores overview

The debug of the GBT-FPGA code has been performed using the ChipScope Pro tools, provided by Xilinx. ChipScope performs the role of an integrated logic analyzer software, allowing to supervise a set of components inserted with the target design inside the supported Xilinx FPGA devices. The tools communicate with these components and provide the designer with an interface in which the inspected signals are reported, for the behaviour exploration and debug of the design [28].
The software uses three main different cores, collectively called the ChipScope Pro cores, generated by the CORE Generator tool and instantiated into the VHDL source code:

- Integrated CONfiguration (ICON),
- Integrated Logic Analyzer (ILA),
- Virtual Input/Output (VIO).

These cores are implemented during the ISE Place and Route process and the generated bitstream is then downloaded into the device under test and analysed with the *ChipScope Pro Analyzer* tool. The described method to use Chipscope is just one of the possible implementations; it has been chosen for the GBT because, although it requires the user to modify the original source code, full control of all IP core parameters and design signals is guaranteed. All the cores use the JTAG boundary scan port to communicate to the computer via a JTAG download cable.

The ICON core provides a communications path between the JTAG boundary scan port of the target FPGA and up to 15 ILA and VIO cores. This core is fundamental for the management of ILA and VIO through dedicated bi-directional control ports; the exchanged information includes a JTAG clock, input and output data and control signals necessary to configure and communicate with the target core.

The ILA core is a customizable logic analyzer core that can be used to monitor any internal signal of the design. Being synchronous to the monitored design, the ILA obeys all the clock constraints applied to the design . The core consists of three major logic blocks: the data capture probes defined by a sample depth and an input width specified by the user, the control and status components, connected to the ICON, and the input and output triggers. Each probe, implemented using regular FPGA logic, is connected to a trigger comparator capable of performing different operations, including to match patterns and to detect the

signals edge transition.
The signals to be inspected are attached to the probe inputs, sampled at design speed and stored using an on-chip block RAM, until they are uploaded by the ChipScope Analyzer tool when the trigger occurs. After the design is loaded on the FPGA, the software is used to set up a trigger event for the ILA measurement and to view data on a waveform window. The general trigger condition, taking into account all the input probes, is the outcome of a Boolean calculation (i.e. combination of AND and OR ports) of the trigger comparator results.
Each ILA core can capture data using two capture modes: Window and N samples. The window capture mode uses a single trigger condition event (i.e. a Boolean combination of the individual triggers) to collect enough data to fill a sample window. After a sample window has been filled, the trigger condition of the ILA core is automatically rearmed and continues to monitor for trigger condition events. This process is repeated until all sample windows of the sample buffer are filled or until the user halts the ILA core. The N Samples capture mode is different: the number of samples per window can be any integer N in the range from 1 to the sample buffer size minus 1. The N sample capture mode is useful for capturing the exact number of samples needed per trigger without wasting valuable capture storage resources.

The VIO core is a customizable core that can both monitor and drive internal FPGA signals in real time. Unlike the ILA core, no on- or off-chip RAM is required. Two kinds of signals are available in the VIO core: asynchronous or synchronous input and output. Signals connected to the asynchronous inputs are sampled using the JTAG clock, read back periodically and displayed in the ChipScope Analyzer tool, while those connected to the synchronous ones are sampled using the design clock. Both the kinds of input have additional cells to capture the presence of inspected signals transitions. Because the design clock will most likely be much faster than the sample period of the ChipScope tool, it is possible for signals to be monitored many times between successive samples. The activity detectors capture this behavior and the results are displayed along with the value in the ChipScope Pro Analyzer tool.
The logical 1 or 0 value for the asynchronous output ports is defined by the user in the Analyzer tool and driven out of the core to the surrounding design; if the output is synchronous, then an operation of synchronization to the design clock is added. Moreover, every synchronous output has the ability to output a pulse train of successive values. A pulse train is a 16-clock cycle sequence of 1's and 0's that drives out of the core on successive design clock cycles. The pulse train sequence is defined in the software and executed only one time after it is loaded into the core.

5.1.2 GBT configuration and data inspection

The GBT-FPGA Chipscope structure,outlined in Fig. 5.2, is composed by four cores:

- two ILAs, one to inspect the input data bus coming from the pattern generator and entering in the transmitter (*Tx ILA*) and the other to inspect the output of the receiver (*Rx ILA*);
- one VIO, to set up and display various controls;
- the ICON, to manage ILAs and VIO.

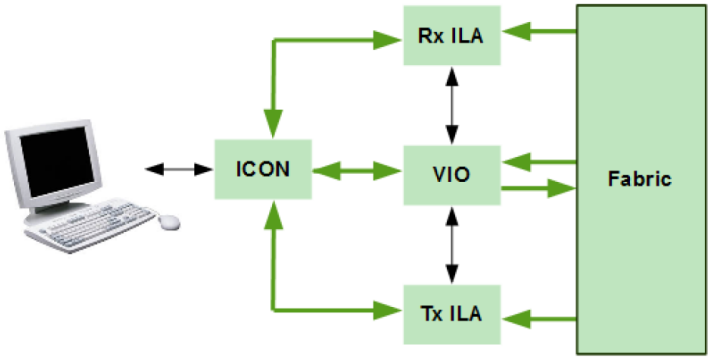


Fig. 5.2 ChipeScope schematic structure for the GBT-FPGA; ILAs and VIO are interconnected with the design logic and controlled by the ICON, which manages the interface with the PC.

VIO and ILAs configuration

The number of bit for data transmission in the 120-bit frame of the GBT is different depending on the type of encoding: 84 bits for GBT Frame, 88 for the 8b/10b and 116 for the Wide Bus. Thus, Tx ILA presents three different probes to inspect with independent triggers three data bus: data (84 bits), 8bit/10bit (4 bits) and wide bus (32 bits). It is synchronized to the transmitter frame clock. Rx ILAs share the same structure, but with the receiver frame clock. It is important to remember that, using the recommended GBT FRAME encoding, only the 84bit sequence of data is provided by the pattern generator.

The VIO contains a set of asynchronous inputs, arranged in a 18-bit bus, and a 12-bit set of outputs synchronous to the transmitter frame clock. The following tables itemize the VIO inspected signals (Tab. 5.1) and configurable parameters (Tab. 5.2); these constitute respectively the input and the output ports of the core.

Table 5.1 VIO asynchronous input for the GBT.

Asynchronous input

Bit	Map
0	RX_DATA_FLAG
1	TX_FRAMECLOCK_LOCKED
2	LATENCY OPTIMIZED TX
3	MGT_READY
4	RX_WORDCLOCK_READY
10:5	RX_BITSLIP
11	RX_FRAMECLOCL_READY
12	GBT_RX_READY
13	GBT_RX_READY_LOSTFLAG
14	RX_DATA_ERROR_SEEN
15	RX_EXTRADATA_WIDEBUS_ERROR_SEEN
16	RX_EXTRADATA_8B10B_ERROR_SEEN
17	LATENCY OPTIMIZED RX

Table 5.2 VIO synchronous output for the GBT.

Synchronous output

Bit	Map	Value
0	GENERAL RESET	active high
1	SMA clock mapping	0 → Tx word clock 1 → Tx frame clock
3:2	TEST_PATTERN_ SEL	01 → dynamic pattern 10 → static pattern
6:4	LOOPBACK configuration	000 → normal operation 001 → near-end-PCS 010 → near-end-PMA 100 → far-end-PMA 111 → far-end-PCS
7	RESET_DATA_FLAG	active low
8	RESET_RxLOST_FLAG	active low
9	Tx HEADER_DATA_ SEL	0 → IDLE header pattern 1 → DATA header pattern
10	MANUAL_RESET_TX	active low
11	MANUAL_RESET_RX	active low

It is possible to observe that the VIO input signals are control flags, provided by the GBT design in order to verify: general properties, such as the operation mode (LATENCY-OPT TX and RX) and the connection of the reference clock provided by the user (TX_FRAMECLOCK

_LOCKED), the right components initialization (MGT_READY, GBT_RX_READY, RX _FRAMECLOCK_READY) and the correct reception of transmitted data (RX_DATA_FLAG, RX_DATA, EXTRADATA_WIDEBUS and EXTRADATA_8B10B_ERROR_SEEN).
Among the output signals, the user can find: resets, properties of the transmitted pattern, value for MGT configuration and the clock mapping for an additive control with an external oscilloscope. In addition to the general reset, provided by a logical combination of the ChipScope output (GENERAL RESET) and the status of a button on the evaluation board, the VIO output set allows to carry out the reset of single components (RESET_TX and RX for transmitter and receiver, RESET_RxLOST_FLAG for the matchflag reset,..). Significant is also the " LOOPBACK configuration" parameter, that establishes the type of loopback connection to be used in the MGT. Loopback modes fall into two broad categories: near-end loopback modes, that transmit data back in the transceiver closest to the traffic generator, and far-end loopback modes, when loop receives data back in the transceiver at the far end of the link (Fig. 5.3).

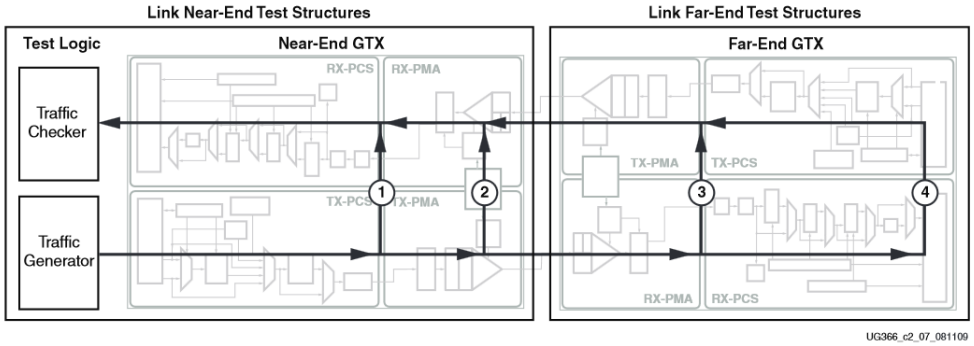


Fig. 5.3 GTX loopback configurations; in order from 1 to 4 Near-End PCS Loopback, Near-End PMA Loopback, Far-End PMA Loopback, Far-End PCS Loopback are displayed.

Eventually the two parameters used to characterize the pattern generator sequence are: Tx HEADER_DATA_ SEL and TEST_PATTERN_ SEL; the first allows to choose between the idle and data header (see Sec. 3.1.3) and the second to set the kind of sequence generated. There are two possible sequences of bits provided by the pattern generator:

- dynamics pattern, which is composed by the combination of a 20-bit counter, repeated four time to emulate the 80 bits of data coming from the GBTX, and another counter to be used for the four bit of slow control in the GBT frame encoding or for the extra data in the other two possible encodings;

- static pattern, which is constituted by a fixed data path.

Performed tests

Several tests have been performed, varying the VIO configuration and inspecting the transmitted and received data.
Our hardware actual resources, because of the commercial optical transceiver, do not cover the whole range of the data line rate (up to 4.8 Gb/s). For this reason, during the debug phase the MGT interface properties have been modified in order to halve the nominal data rate frequency, as discussed in section 4.2.3.
For illustrative purpose, a typical measurement setup and analysis are reported; using ChipScope is not possible to perform a thorough statistic study on the quality of the transmitted/received patterns, since the tool allows to export and evaluate no more than one consecutive data sample, composed of only 1024 words at maximum.

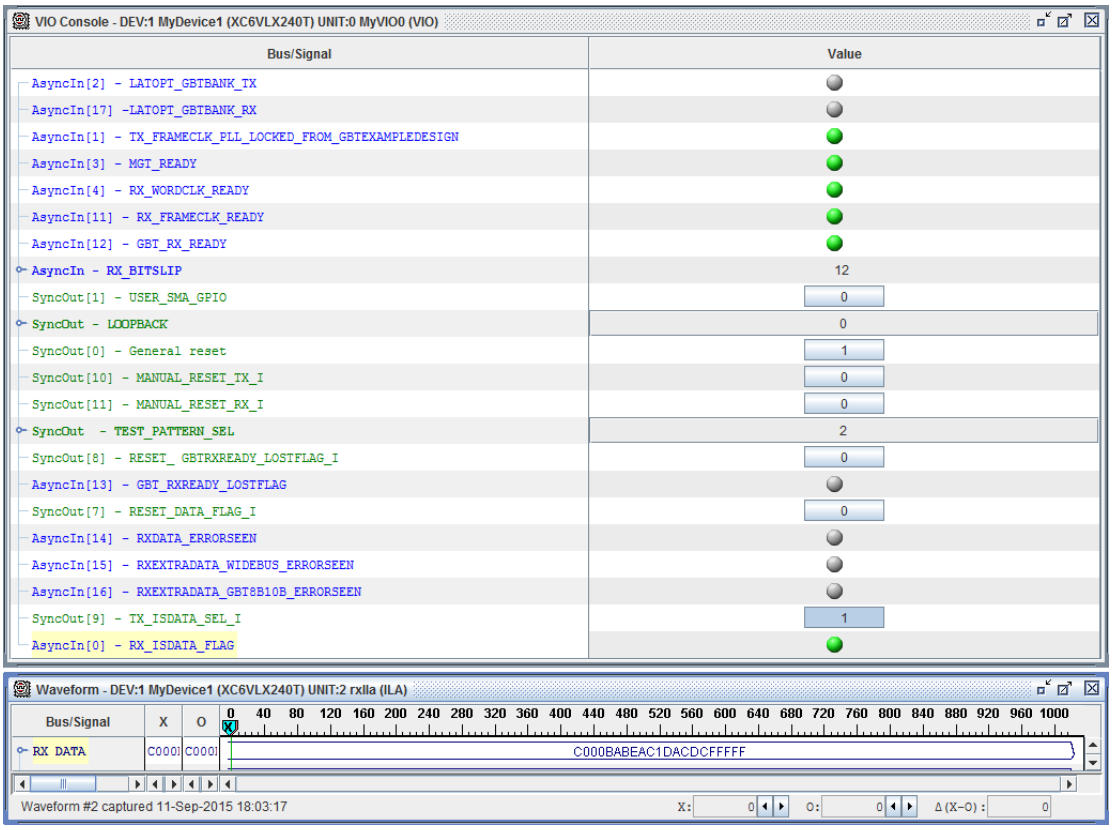


Fig. 5.4 chipscope interface, used during the acquisition.

The ILAs have been programmed, in order to trigger the data in correspondence of a generic variation from zero of the 84-bit data frame, and to memorize 1024 consecutive frames. The exported samples have been checked to understand if error bits were present and how frequent they were.

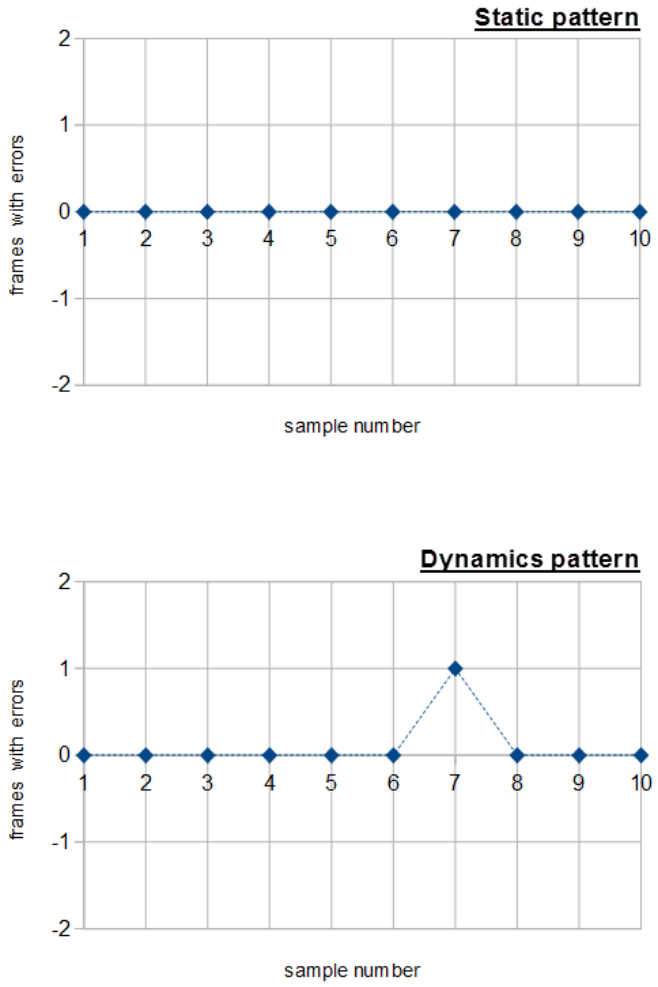


Fig. 5.5 Study on 20 samples collected from the Rx ILA. The first ten samples were collected setting the pattern generator to produce the static sequence, the other ten the dynamics one.

5.2 Data extraction via Ethernet

5.2.1 Ethernet connection and DAQ overview

The idea was to create an interface to permit the data extraction from the GBT-FPGA, providing the opportunity to save them on the PC disk, to perform a proper analysis. To this purpose, an acquisition system based on an Ethernet communication channel has been created.

On the PC end of the link, the main machine interface has been developed using LabView, which is a graphical programming environment including all the tools necessary for DAQ, data analysis and presentation of results. On the FPGA link end the connection to the GBT design has been performed by an HDL interface, taking advantage of the *GbPhy* component

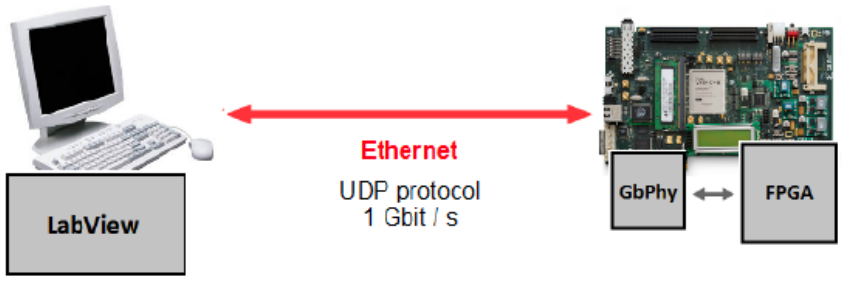


Fig. 5.6 Ethernet communication link; the transmission use a UDP protocol.

provided by Xilinx on the ML605 evaluation board. It must be gigabit capable and must automatically configure itself at power-up for 1Gb/s full duplex communication.
GbPhy, abbreviation for Gigabit Physical layer, is the chip that implement the hardware functions of transmission and reception of the Gigabit Ethernet; where for Gigabit Ethernet it is meant the set of technologies for transmitting Ethernet frames at a rate of 1 Gbit/s. The GbPhy, interfacing between the analog domain of Ethernet line modulation and the digital domain of the link-layer packet signalling, is the lowest layer of the used communication Protocol. It provides a UDP-based Ethernet control link with the additional features of high bandwidth and autonomous data transmission.
The User Datagram Protocol (UDP) is the simplest Ethernet communication protocol. It is a connectionless protocol which provides only the basilar services of the transport layer: the multiplexing of connection, through ports assignment, and the checksums for data integrity. There is no guarantee of delivery, ordering, or duplicate protection, and so it cannot be considered as reliable as other largely used protocols (e.g. TCP). The main advantage in UDP use is the fast transmission and, thus, it is preferable for the applications that need an high bit rate (like the GBT-FPGA data transfer).
The VHDL and LabView interfaces have been created modifying and adapting to our purposes a pre-existing, available open source project [31].

The current system allows up to 8 different boards (like ML605), corresponding to 8 different addresses, to be connected to a single host via a gigabit switch. Two different communication structures are implemented on two separate UDP ports:

- a *bidirectional standard communication* for commands, based on a fixed length 8-byte protocol, to every 8-byte message always corresponds an 8-byte reply, allowing the verification of eventual packet loss;

- an *unidirectional* (FPGA to CPU) *communication* for events, allowing data transmission from the GBT-FPGA at a speed beyond 80MByte/s.

VHDL basic structure

The VHDL design foresees three main components: a *Packet Parser*, a *Message Parser* and a *Command Processor*, as shown in Fig. 5.7.

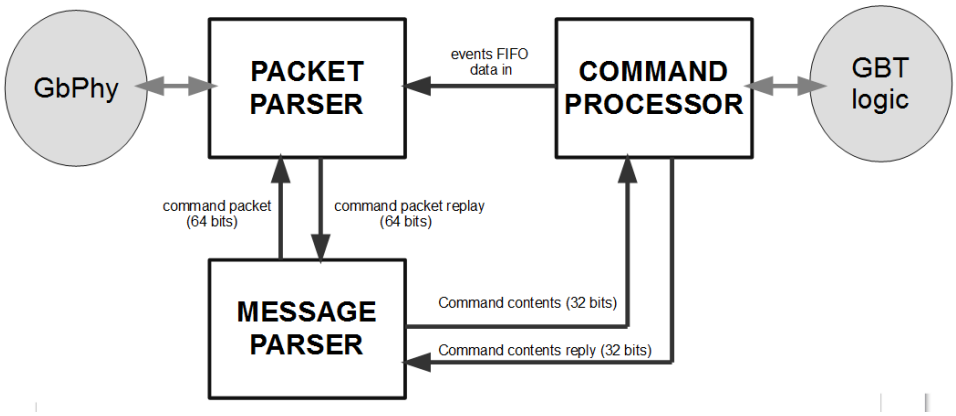


Fig. 5.7 VHDL structure for UDP communication.

The Packet Parser block interacts with the GbPhy to receive and transmit Ethernet packets. It passes the payload of correctly addressed UDP packets to the Message Parser and, when receives reply data, it encodes these data into a UDP packet and transmit them. The Message Parser manages the command packets, transferring their contents to the Command Processor and reorganizing the Command Processor reply to be sent to the Packet Parser. Additionally, in the Packet Parser the event data that have to be transmitted are managed through an "events FIFO", encoded into a UDP packet and transmitted either after filling the maximum packet size or after timing out. A double buffering allows one event packet to be transmitted while a second one is being filled. The Command Processor is the block that interacts with the GBT logic, imposing the received commands, answering to their requests and extracting the data that will fill the "events FIFO" of the Packet Parser.
All the communication between these three components is clocked at 125 MHz, but the internal operations of the Command Processor are synchronised with the GBT frame clock, because it has to deals with the GBT frames at the relative rate.

Command logic

The Command logic is based on a 32-bit command provided by the Message Parser to the Command Processor, and a 32 bits long reply in the opposite direction. Since different subsystems require different clocks, the project foresees two possible targets, hardware and events. The hardware target manages all the basic hardware interactions (such as checking

configuration switches), clocked at 125MHz. The events target is generally used for the operation on the user logic (in this case the GBT logic) and requires a specific clock frequency (20 MHz). The communication between the 125 MHz and the 20 MHz clocked subsystems is performed in the Command Processor by a “CPU to EVENTS FIFO”, for the information transit from the Ethernet hardware logic to the GBT logic, and a “EVENTS to CPU FIFO”, for the opposite data flux.
The 32-bit code for command is thus sub-divided as follows:

→ *command(31 downto 28)* ⇒ *sub-system target*
→ *command(27 downto 20)* ⇒ *sub-system command*
→ *command(19 downto 0)* ⇒ *sub-system data*

To give an **example**: the command for enabling the events transmission is the hexadecimal string **"4 83 00001"** where:

- **4** is the sub-system target; it indicates that the command must interact with the GBT logic (the other available target value is for commands that interact only with the GbPhy logic);

- **83** is the sub-system command; it points to a specific process into the Command processor;

- **00001** is the effective command content.

A 32 bits command reply corresponds to each 32 bit command and it is managed by the Command Processor and transmitted to the Message Parser.

This component encodes the command message in conformity with the UDP protocol: each 8-byte command is divided in:

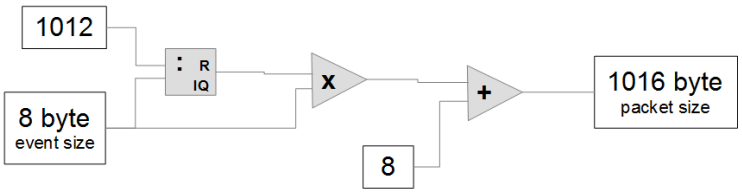
Byte 0 (MSB) ⇒ the “software” target,
Byte 1 ⇒ the actual "software" command,,
Bytes 2 and 3 ⇒ a 16-bit packet ID for packet loss verification,
Bytes 4 to 7 ⇒ a 32-bit payload word that can be transmitted to / received from the user logic.

The Message Parser reply packet contains the same first four bytes of the command packet plus four reply bytes [31].

In the case of multiple commands, a single reply packet is generated once all commands have been completed.

Event logic

The event packets are made of up to 64 8-byte messages. The events are transmitted when the packet buffer reaches its maximum size or it reaches the timing out. Given the size in byte of the actual single event, the maximum size in byte after which the filling packet will be considered full is programmable so that an event will not be split between two packets. For the GBT, considering as event the last 64 bits of the 84-bit data for a total length of 8 byte, the transmission maximum packet can be calculated as follows:



Every events packet presents a 8 bytes header followed by the event data messages; the header is defined as:

→ *header[0] = 0xDC;*
→ *header[1] = 0xBA + boardID;*
→ *header[2] = (packetNumber & 0xff000000) » 24;*
→ *header[3] = (packetNumber & 0x00ff0000) » 16;*
→ *header[4] = (packetNumber & 0x0000ff00) » 8;*
→ *header[5] = (packetNumber & 0x000000ff);*
→ *header[6] = (eventBytes & 0xff00) » 8;*
→ *header[7] = (eventBytes & 0x00ff);*

After a first fixed byte, whose static hexadecimal value is “DC”, the second byte provide information about the board addresses used in the connection. To have memory of the previous transmission and to verify packet loss, four bytes of the header report the packet number, which is incremented by one for every successive packet. Finally the last two bytes of the header constitute the number of bytes in a packet, to perform a further control.

In order to transmit data from the GBT receiver to the CPU via Ethernet, it was necessary to reduce the transmission rate at least of a factor ten (from the 4.8 Gb/s to about 0.5 Gb/s). For this aim, a process inside the Command Processor manages the writing on the “events FIFO” of the precise number of events to fill an events packet and then interrupts the events transfer waiting a time sufficient for the FIFO emptying and for the packet transmission to the computer.

With this method, sequences of 127 consecutive events interleaved by space of interrupted communication are reported.

LabView interface

On the other side of the communication link, the LabView interface allows the decoding of the packets and the writing on a binary file of the sequences of event data coming from the GBT receiver, enabling and disabling the event transmission to the computer. The figure Fig. 5.8 displays the created LabView interface.

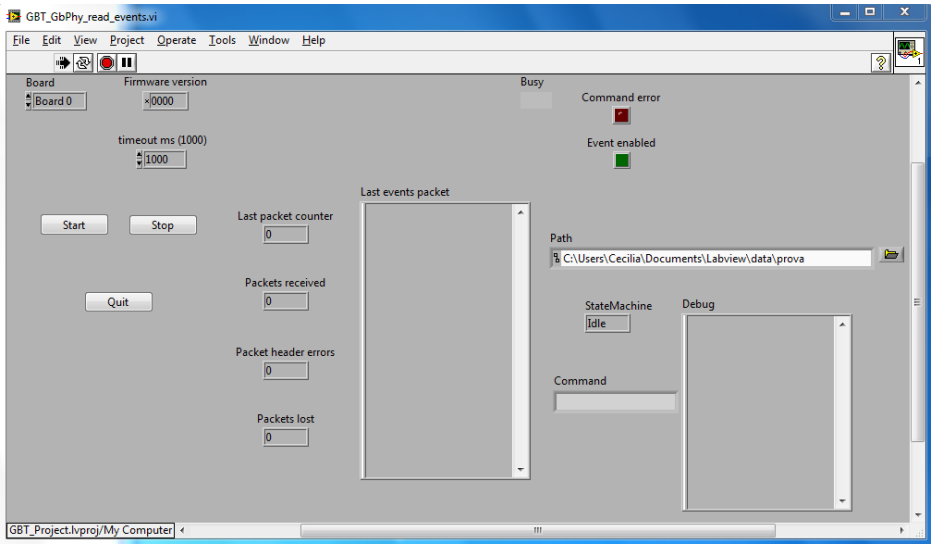


Fig. 5.8 LabView interface for the data extraction; the program presents two buttons for start and stop writing the events from the FPGA.

5.2.2 Data analysis

In order to test the GBT transmission, the GBT-FPGA *Example design* and the GbPhy VHDL code have been integrated in a single ISE project and the ChipScope cores have been deleted, avoiding the occupancy of FPGA unused resources. The VIO output and input signals, needed for the GBT resets and for the match-flags controls, have been mapped on the buttons and leds of the ML605 board. The pattern generator has been modified to transmit a fixed 84-bit path easy to be recognized: the 64 bits analyzed by the system present the sequence "123456789ABCDEF0".
The resulting code allows to extract 126 consecutive pattern for a total size of 1008 bytes,

that summed to the 8 bytes of header completely fill a packet. Each packet is sent when the timer reaches $\sim 300\ \mu$s, thus the transmission rate is:

$$\frac{1016 \cdot 8 \text{ bit}}{300\ \mu\text{s}} = 27\text{Mbit/s}$$

In Fig. 5.9 the behavioural simulation of the system is reported.

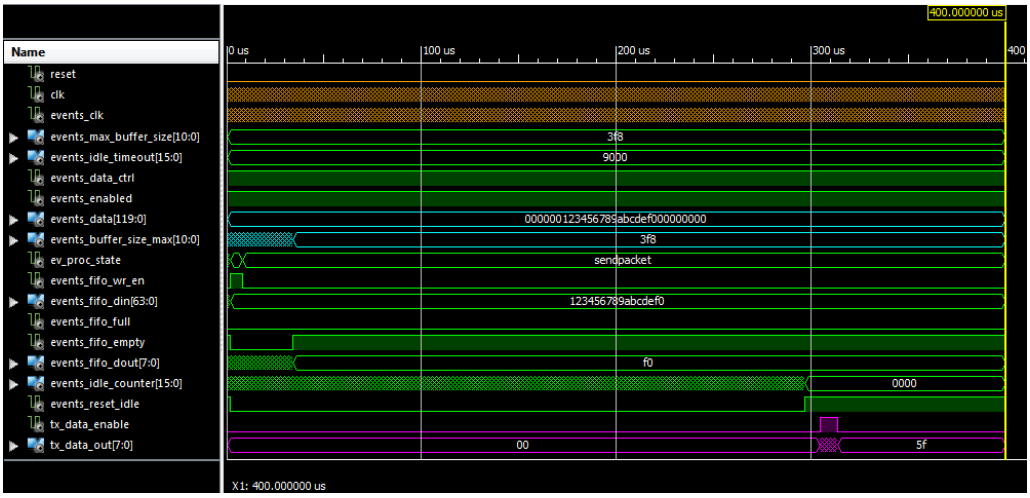


Fig. 5.9 Behavioural simulation: the mechanism of data transmission is reported.

The code has been implemented on the Virtex6 FPGA, connected via Ethernet to the LabView interface. Using the interface, several samples of about 1000 packets have been stored in binary files. In order to convert these files in text files, giving them a note structure, an other LabView program has been created. The obtained text files have been analyzed, verifying that the transmitted 64-bit event frames for every packet remained constant at value "123456789ABCDEF0".
All the analyzed packets do not present errors in transmission.

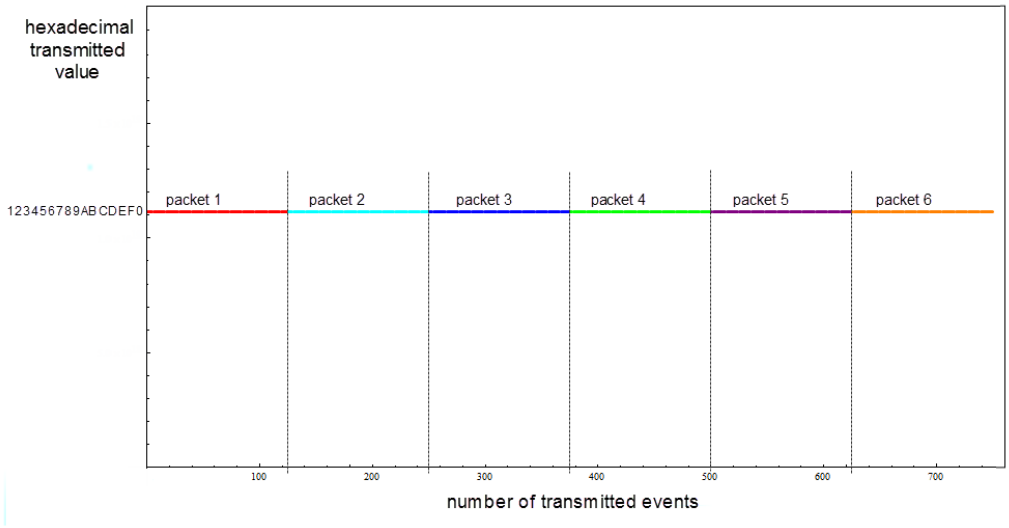


Fig. 5.10 The figure reports, as example, the procedure used to analize the stored packets. To clearly understand the structure only six 127-byte packets are reported.

Chapter 6

Beam tests

The GBT link project will permit the communication between the counting room and the front-end electronics of the $\overline{\text{P}}$ANDA MVD. In fact, in the future it is foreseen to interface the GBT-FPGA part of the link to a control main machine, to be managed by the user during the measuring time, whereas the GBTX part will be connected to the on detector blocks of the readout electronics by the E-links' system (section 3.1.2).
With the aim to connect the three main blocks of the acquisition system (the front-end chip, the GBT ASIC and the GBT-FPGA), a work related to the characterization and test of some readout components of the $\overline{\text{P}}$ANDA electronic circuits was carried out in parallel.

In particular, I focused my attention on the calibration of the last hybrid pixel prototype ToPix v4 and on the study of Single Event Upset for the chip and the GBLD (the laser driver for the ASIC component of the GBT link). The calibrations have been carried out in view of the two programmed tests for the chip characterization and the verification of its tracking performances. The first test was performed in May 2015 at *COoler Synchrotron* (COSY) facility in the *Juelich Forschungzentrum* (Germany) and a proton beam with a momentum of 2.9 GeV/c has been used. The second beam test was performed in July 2015 at CERN, using a proton beam with variable momentum (range between 20 and 150 GeV/c).
Moreover, for the SEU study, the ToPix and GBLD circuits were tested at the *SIRAD* (SIlicon Radiation Damage) irradiation facility in the INFN laboratory of Legnaro (Padova), in June 2015.

After a brief introduction on the ToPix v4 architecture, this chapter describes the calibration procedure, defining step by step the obtained results, and the experimental setup used during the tests for the chip characterization.
Then, since the SEU effects play an essential role in the readout electronic performances, the attention is focused on the SEU study, describing the experimental setup and the performed measurements. Finally the main results of the SEU test are presented.

6.1 Calibration of the hybrid pixel prototypes

The ToPix ASIC is the custom solution for the readout of the silicon pixel sensors for the Micro Vertex Detector. It has been developed in 0.13 μm CMOS technology for its high level of integration and the intrinsic radiation tolerance of deep submicron technologies. ToPix is designed for the triggerless environment foreseen in $\overline{\text{P}}$ANDA and totally fulfils the MVD requests, providing position, time and energy measurement of the incoming particles.
As mentioned in the first chapter, the chip will consist of a 116×110 pixel matrix arranged in 55 double columns and managed by the same number of column controllers. A Chip Control Unit (CCU) multiplexes the data from the controllers and sends them to the GBT board via two 320 Mb/s serial links [15].

In order to test the chip performances, a reduced version of the final ASIC has been produced.
These assembly prototypes are composed by the ToPix v4 readout chip and a dedicated pixel sensor made on epitaxial silicon, with 640 pixels organized in 4 folded columns of different lengths. Each sensor cell is connected to a frontal ToPix cell by a solder-lead bump; with respect to the electronic readout logic, the sensor and the chip are in a mirror configuration.
A testing board hosts the assembly prototype. It is connected to a ML605 Xilinx evaluation board equipped with a Virtex6 (equal to the one used for the GBT-FPGA project), which manages the data transmission interfacing the assembly with a data acquisition system based on a Labview program.

6.1.1 Topix v4 architecture

The ToPix v4 is the last prototype for this ASIC solution, designed at the INFN Electronic Laboratory of Turin. The prototype includes 640 cells arranged in 2x128 and 2x32 double columns with a size of 100x100 μm^2, a 160 MHz time stamp distribution circuit to measure both particle arrival time and released energy (via Time over Threshold technique) and a full control logic. Each cell contains both analog and digital electronics, needed respectively to amplify the signal coming from the silicon sensor and to perform time and charge digitization.
The pixel matrix is controlled by a peripheral logic, which writes the configuration on a specific register and reads the data stored on the pixel registers; at last the data are multiplexed on the serializers.
Digital input and output are based on the Low Voltage Differential Signaling (LVDS), in order to be compatible with the single 1.2 V power supply.

The architecture is based on the Time over Threshold (ToT) technique, which consists in measuring the injected charge by estimating the time necessary to discharge a capacitor

through a constant current feedback. Since the relationship between charge and time remains linear as long as the discharge current is constant, the ToT advantage is to provide a linear measurement on a wide range of charges, even when the main amplifier is saturated.

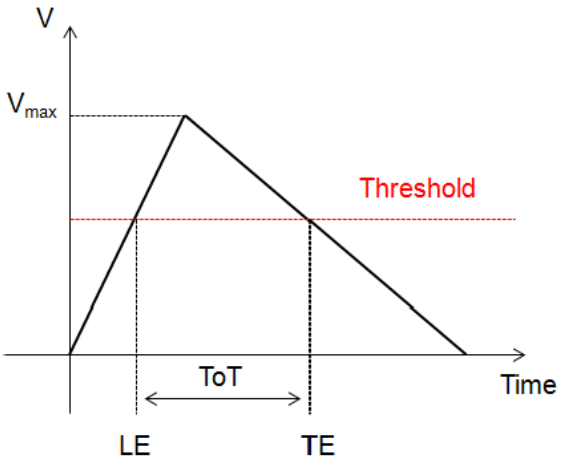


Fig. 6.1 The pulse generated by a comparator has a width proportional to the amplitude of the signal. The rising edge is called leading edge (LE), while the falling edge is the Trailing Edge (TE).

Pixel cell structure

A simplified schematic of the pixel cell is reported in Fig. 6.2.

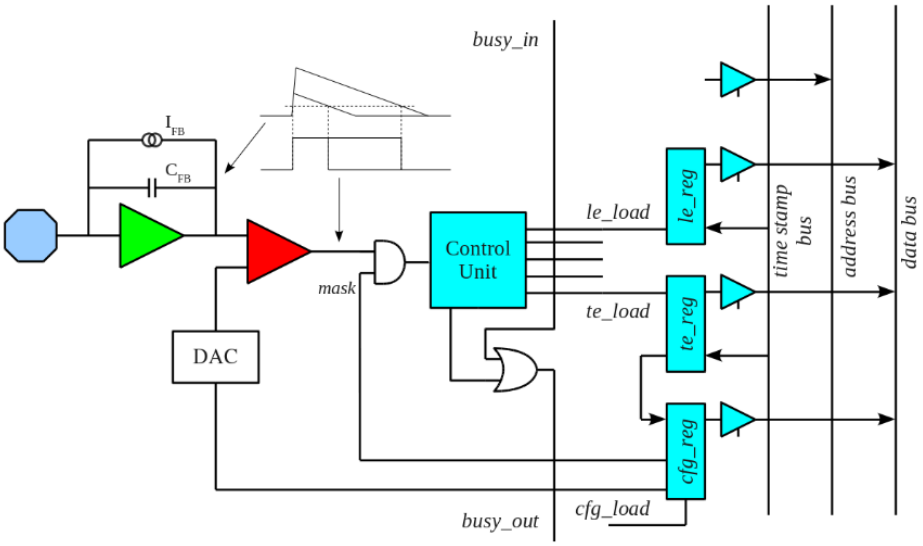


Fig. 6.2 Simplified schematic of the ToPix v4 pixel cell; the figure shows the analog chain for the ToT measurement and the register logic for the data transmission.

The current from the detector is integrated in a preamplifier with a nominal 12 fF feedback capacitor and a constant current discharge circuit. The output enters then in a comparator, where is compared to a threshold value, fixed externally but fine-tunable, pixel by pixel, with a 5-bit DAC. The Control Unit detects the rising and the falling edges of the comparator output and stores their value in two 12-bit registers. The difference between time stamps of the trailing and leading edges provides a measure of the charge released by the particle in the detector. Once the leading and trailing edge information has been loaded in the registers, the Control Unit issues a busy signal which is propagated to the column controller, that enables the hit pixel to write its address and data on the corresponding readout bus.
A fast-OR chain manages the propagation of the busy signal to the column controller and fix the readout priority among pixels.

The pixel cell logic includes an 8-bit configuration register, used to store the configuration of the circuit: 5 bits are used for the local threshold DAC, 2 bits for test features and 1 bit to mask the comparator output in case of a noisy pixel.

For all the registers of the pixel cell, the scheme of Triple Modular Redundancy (TMR) for error detection is employed, in order to protect them from Single Event Upset. In addition the configuration register employs a feedback for automatic error correction, since a failure in this register could lead to the improper setting of fundamental parameters in the readout circuit.

Peripheral logic

The peripheral logic is placed outside the active area of the chip and is based on 32-words FIFOs, connected to the readout buses of the columns by a sense amplifier, to improve the readout time. The pixel cells are arranged in 4 double columns, controlled by the Column Readout Control Unit (CRCU) and served by 3 buses: the *time stamp bus* distributes time information by a Gray counter, the *data out bus* transmits both the Leading Edge and Trailing Edge pieces of information and *addr out bus* sends out the hit pixel information.
The CCU reads the data stored in the FIFOs and sends out the data via the 320 Mb/s serial link, as shown in Fig. 6.3. The CCU also provides the time stamp generation and the upload of configuration data via a dedicated serial interface [15].
Each event that has to be transmitted consists of 32 bits: 8 bits for the pixel address (1 bit to select between the two columns and 7 bits to address the 116 cells in a column), 12 bits for the leading edge time stamp and 12 bits for the trailing edge time stamp.

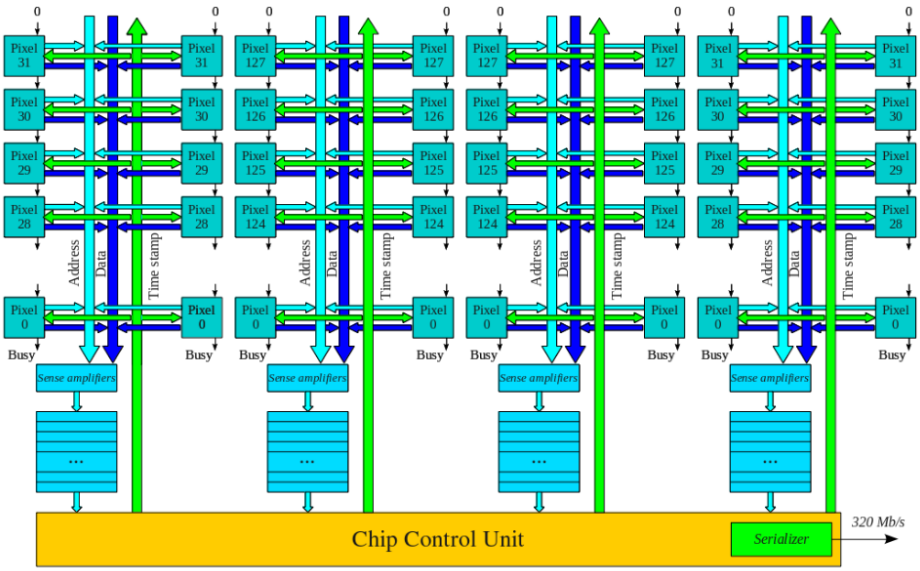


Fig. 6.3 ToPix v4 schematic. The double column readout buses are connected via sense amplifier to 4 32-words FIFOs; each fifo is connected to the CCU.

To protect the transmitted events from mistakes due to the SEU, the 32-bit data are Hamming encoded [1] in a 37-bit data word [3].

6.1.2 Calibration of the pixel assemblies

An accurate calibration of the assembly has been carried out before the beam tests, in order to find out the best working parameters for the ToPix v4 chip. The experimental setup consists in the testing board on which the assembly is placed, the ML605 evaluation kit connected to a computer, and two power suppies for the board and the sensor. The board, for the ToPix pixel assembly and the other service functions requires a 5 V power supply, while the sensor is powered at 100 V. Several prototype assemblies were tested in order to verify their performances and to select the boards to be used during the measurements under beam. The performed tests, with a brief description, are listed hereafter:

- **Channel check**
  ToPix has an internal calibration system: it is possible to inject a current pulse into the preamplifier to test the circuit response. The injected current wants to simulate the charge released in the sensor by a colliding particle.
  In order to check the correct functionality of the chip readout cells, the pixels answer to

[1] Hamming codes are a family of linear error-correcting codes that, adding a limited redundancy to the data stream, can detect up to two-bit errors or correct one-bit errors.

the internal test pulse has been analysed. The LabView program *"ToPix_TP_loop.vi"* was used to scan the pixel response to a sequence of eight test pulses. All the signals are sent at the same time (with a fixed delay respect to the reset) and with the same charge.

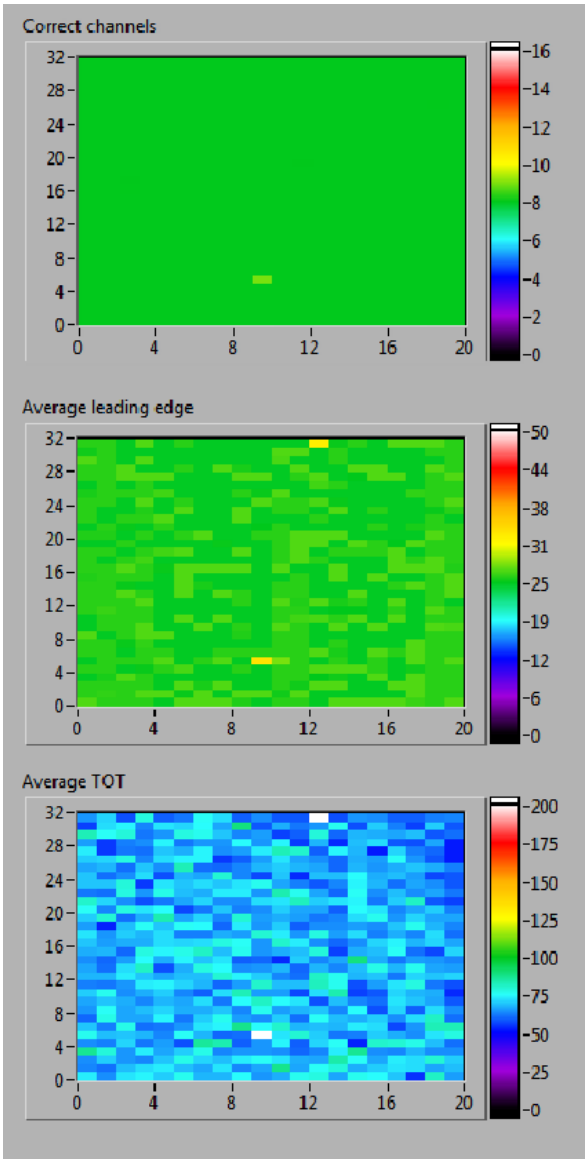


Fig. 6.4 ToPix v4 pixel maps from ToPix_TP_loop.vi; from the top: the Correct Channels, Average LE and ToT are reported. The values are referred to the chip assembly number 6.

- **Baseline calibration**

  To calibrate the baseline a s-curve method has been used. This is based on the idea that the ratio between the number of the chip discriminator outputs (N_D) and the total

number of signals feeding the discriminator (N_T) can be decribed as function of the threshold voltage (V_{th}).

$$r = \frac{N_D}{N_T}$$

For an hypothetical circuit the curve obtained representing r as a function of V_{th} should look like a step function, equal to 1 when the V_{th} is smaller than the input signal voltage (V_{sign}) and to 0 when is greater. Because of the noise, the real s-curve is a sigmoid curve, as shown in Fig. 6.5.

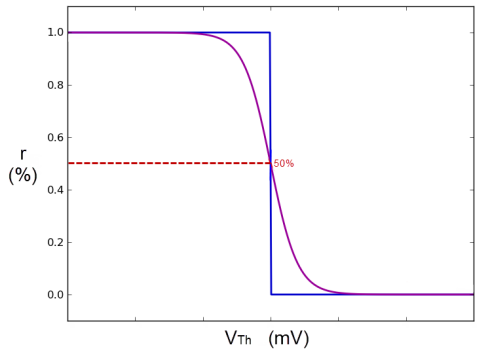


Fig. 6.5 S-curve shape: in blue the theoretical curve and in violet the real one. The mean corresponds to the 50% of the s-curve and the sigma gives information about the dispersion.

Since the external trashold voltage is common to all pixels, in order to deal with the problem of the channel dispersion, a local 5-bit DAC (1 for the sign and 4 for the s-curve) allows a fine tuning of the threshold on a pixel by pixel basis. So, starting from the nominal baseline value (700 mV), for each pixel a correction factor is evaluated in order to redress the fluctuations. The baseline calibration is automatically performed by the LabView program *ToPix_BaselineScan.vi*.
The program makes 31 s-curve measurements for all the 640 pixels and takes the 50% s-curve value as correction for the 700 mV baseline. The corrections are stored in a file (*DAC file*), which is loaded on the respective assembly before measuring, in order to reduce the dispersion. As example, Fig. 6.6 reports the baseline distribution with and without the DAC file correction.

- **Feedback Capacitance evaluation**
  The feedback current (I_{fb}) and the signal tail slope (TS) are fundamental for the C_f measurement, whose nominal value is 12 fF. The TS, which is the slope of the output signal depending on the feedback capacitor value and the feedback current, can be measured for each pixel with the LabView program *ToPix_ChannelShapeScan*. It is

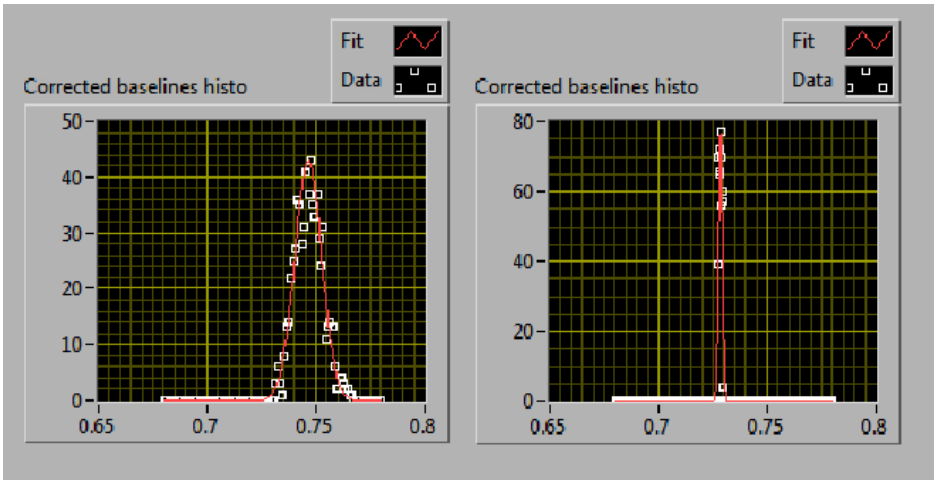


Fig. 6.6 Baseline distribution for the 640 pixels; on the right the DAC correction has been inserted. The values are referred to the chip assembly number 6.

necessary, before the measuraments, to load the DAC file obtained for the specific board. After the discharge signal has been reconstructed simulating the readout cell with a voltage input level (100 mV), the TS is extrapolated for each pixel by a linear fit of the 10 last points of the falling edge.

Since, for a single cell, the TS is defined as:

$$TS = \frac{V_{OUT}}{t}$$

where V_{OUT} is the maximum voltage in the feedback circuit, then the feedback capacitance can be calculated as:

$$C_{fb} = \frac{Q}{V_{OUT}} = \frac{Q}{TS \cdot t} = \frac{I_{fb}}{TS}$$

(Q is the injected charge and I_{fb} the current in the feedback circuit).
To evaluate the I_{fb} value, the measurement of an external resistor ddp (V_{ext}) on the testing board is performed; taking into account that the circuit has an amplification factor of $K = 80$ and that the resistor is $R_{ext} = 510$ kΩ, the current value is given by:

$$I_{fb} = \frac{1}{K} \cdot \frac{V_{ext}}{R_{ext}}$$

Therefore, knowing V_{ext} and TS, the C_{fb} can be evaluated as:

$$C_{fb} = \frac{I_{fb}}{TS} = \frac{1}{K} \cdot \frac{V_{ext}}{R_{ext}} \cdot \frac{1}{TS}$$

- **Threshold voltage in e- evaluation**

  Knowing the C_{fb}, it is possible to convert the threshold voltage (V_{th}), set externally and referred to the baseline, in a value expressed in charge:

  $$Q_{th} = C_{fb} \cdot V_{th}$$

  The threshold voltage can then be expressed in number of electrons (n_{th}), knowing that the electrone charge is $e = 1.602 \cdot 10^{-19}$C,

  $$n_{th} = \frac{Q_{th}}{e} = \frac{C_{fb} \cdot V_{th}}{e}$$

  This conversion is very convenient for comparison, with respect to the input signal and the noise.
  Tab. 6.3 shows the values for the threshold voltage corresponding to the number of electrons, obtained from the relation:

  $$V_{th} = \frac{n_{th} \cdot e}{C_{fb}} = n_{th} \cdot e \cdot G_{charge}$$

  where G_{charge} is the charge gain and is defined as the inverse of the feedback capacitor. N_{th} and e are considered theoretical values (without errors), while G_{charge} is the resulting value from the mean of the Gaussian distribution of the 640 pixels' values for the gain. The standard deviation has been used to establish the error on G_{charge} and this error has been propagated to the V_{th} values. Two significant digits have been left to the measures to appreciate the small fluctuation dependance in the analyzed chip.

Table 6.1 ToPix $V_{baseline}$; the values and errors are obtained using the *ToPix_BaselineScan.vi*

Baseline values				
Vbaseline (mV)				
Chip 04	**Chip 05**	**Chip 06**	**Chip 09**	**Chip 10**
731 ± 1	736 ± 1	729 ± 1	724 ± 1	733 ± 1

- **ToT measurement**

  The trend of the ToT as linear function of the charge can be verified using the LabView program *"ToPix_ToTscan.vi"* . The slope of the line ToT vs charge represents the ToT gain. The ToT gain for the whole readout circuit is extrapolated from the mean value of the 640 slopes, which follow a Gaussian distribution.

Table 6.2 ToPix voltage threshold in electrons and corrispondent V_{th} values; knowing the V_{th} value it is possible to find the voltage value to set on the assembly (*VREF_D* from the formula: $V_{th} = VREF_D - V_{baseline}$. The table refers to the chip prototypes used during the tests.

Threshold values

electrons	***Vth (mV)***				
	Chip 04	**Chip 05**	**Chip 06**	**Chip 09**	**Chip 10**
1000	14.7 ± 1.8	14.6 ± 1.4	14.9 ± 1.6	14.9 ± 1.6	14.2 ± 1.6
1100	15.7 ± 1.9	16.0 ± 1.6	16.4 ± 1.8	16.4 ± 1.8	15.7 ± 1.8
1200	17.1 ± 2.1	17.5 ± 1.7	17.9 ± 1.9	17.9 ± 1.9	17.1 ± 1.9
1300	18.5 ± 2.3	18.9 ± 1.9	19.3 ± 2.1	19.3 ± 2.1	18.5 ± 2.1
1400	19.9 ± 2.5	20.4 ± 2.0	20.8 ± 2.2	20.8 ± 2.2	19.9 ± 2.2
1500	21.4 ± 2.6	21.8 ± 2.2	22.3 ± 2.4	22.3 ± 2.4	21.4 ± 2.4

Table 6.3 ToPix chips configuration values. the tables reports the values of TS, C_{fb} and ToT gain obtained for the assemblies used during the tests.

Chip 04		***Chip 05***	
TS (mV/s)	$69{\cdot}10^4 \pm 8{\cdot}10^4$	TS (mV/s)	$68{\cdot}10^4 \pm 7{\cdot}10^4$
C_{fb} (fF)	11 ± 1	C_{fb} (fF)	11 ± 1
G_{charge} (mV/fC)	92 ± 10	G_{charge} (mV/fC)	91 ± 9
Chip 06		***Chip 09***	
TS (mV/s)	$70{\cdot}10^4 \pm 8{\cdot}10^4$	TS (mV/s)	$70{\cdot}10^4 \pm 7{\cdot}10^4$
C_{fb} (fF)	11 ± 1	C_{fb} (fF)	11 ± 1
G_{charge} (mV/fC)	93 ± 10	G_{charge} (mV/fC)	93 ± 9

Chip 10	
TS (mV/s)	$67{\cdot}10^4 \pm 7{\cdot}10^4$
C_{fb} (fF)	12 ± 2
G_{charge} (mV/fC)	89 ± 10

6.1.3 Pixel tracking station

In order to keep the prototypes well aligned and to support all the needed cable for the interconnection, a custom structure has been created. The pixel tracking station (Fig. 6.7) hosts four boards (4 assembly) and two Xilinx evaluation kits for the data management and transmission. The distance between two consecutive board is 6 cm, for a total length of the tracking station of ∼20 cm.

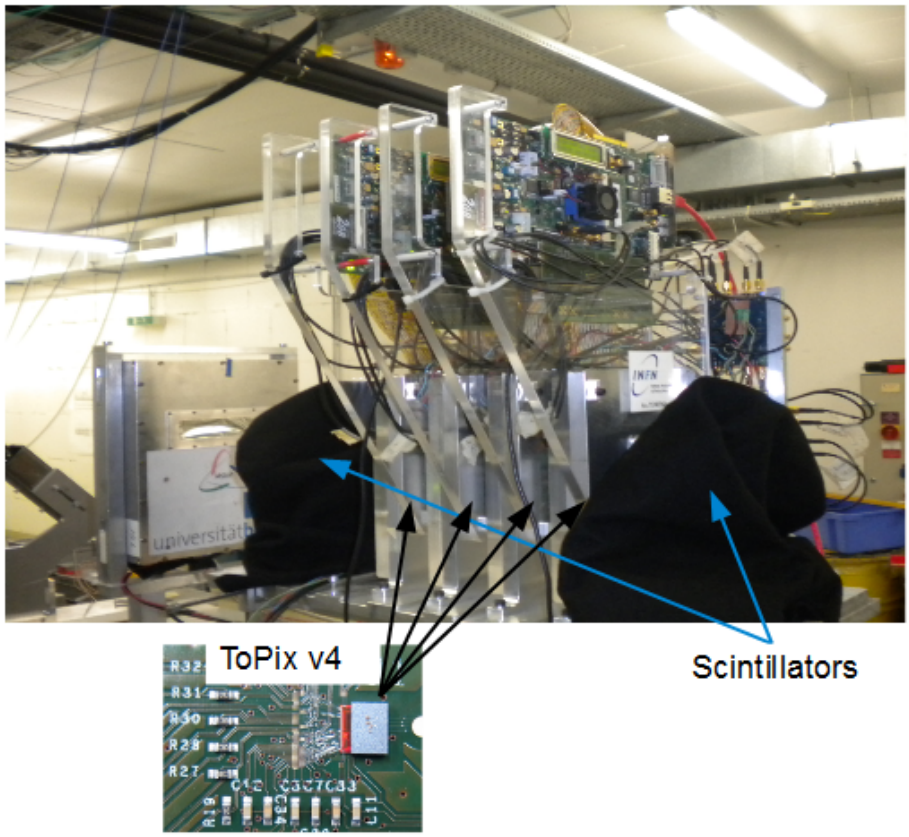


Fig. 6.7 Picture of the Tracking station; the arrows indicate the four assemblies and the scintillators, which have been covered with black rag to increase their efficiency.

In addition to the four boards, the tracking station foresees the pillars for the scintillators. These components are used to know about the beam presence, direction and intensity. The acquisition is performed by a Xilinx evaluation board with a Spartan6 FPGA; this device belongs to an inexpensive family with respect to the Virtex series but its features are adequate to the assigned task. In Fig. 6.8 a scheme of the tracking station is reported.

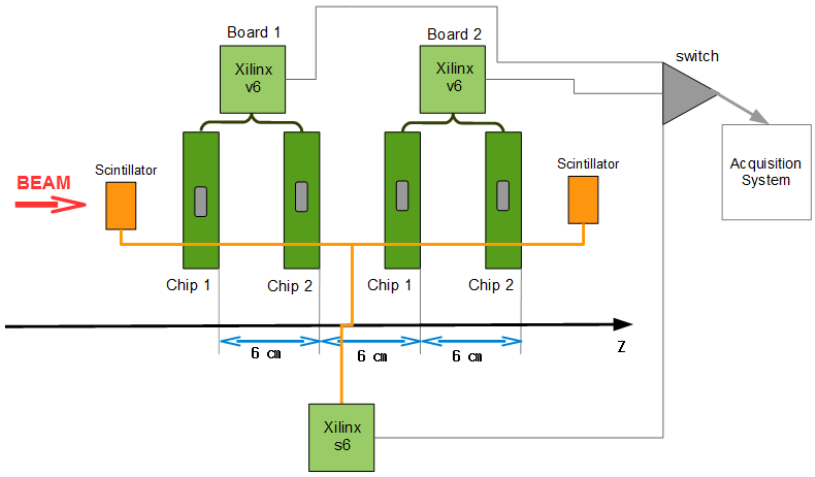


Fig. 6.8 Tracking station scheme.

6.2 Tests for the Single Event Upset

6.2.1 SIRAD facility

The SEU test has been performed in the SIRAD, which is a facility dedicated to studies of electronic devices and of bulk damage in semiconductor components at the INFN laboratories in Legnaro. The structure includes a Tandem-XTU accelerator with two stripper stations. Ions are generated inside an external source and are extracted with a weakly positive charge state; before entering the tandem they cross a charge-exchange region, becoming negative charged. The Tandem accelerates the ions and inject them in the vacuum beam pipe. The ions in the pipe are driven under the effect of both magnetic deflectors and lenses and distributed towards the selected target station, where the measurement apparatus is located [11], as shown in Fig. 6.9.
Specifically, there are an analyzing magnet ([1] in figure), that allows to select ions with only one energy $E(q_1, q_2)$, and a switching magnet ([2] in figure) to deviate the monochromatic ions to the experimental beam [10]. In this case, the switching magnet deviates the beam of $+70°$ to the SIRAD experimental line.

At the end of the line, the irradiation chamber is placed. As shown in Fig. 6.10, it contains: a movable sample holder of 33 x 10 cm^2, a diodes' board for dosimetry on a fixed support and a quartz for the beam measurement and alignment. On the sample holder the device under test and an other diodes' board are positioned.
To improve the test quality, in the irradiation chamber a vacuum of $\sim 8 \cdot 10^{-6}$ mbar is pumped. After the vacuum formation, the sample holder is motor controlled from the counting room in order to expose the different devices under the beam.

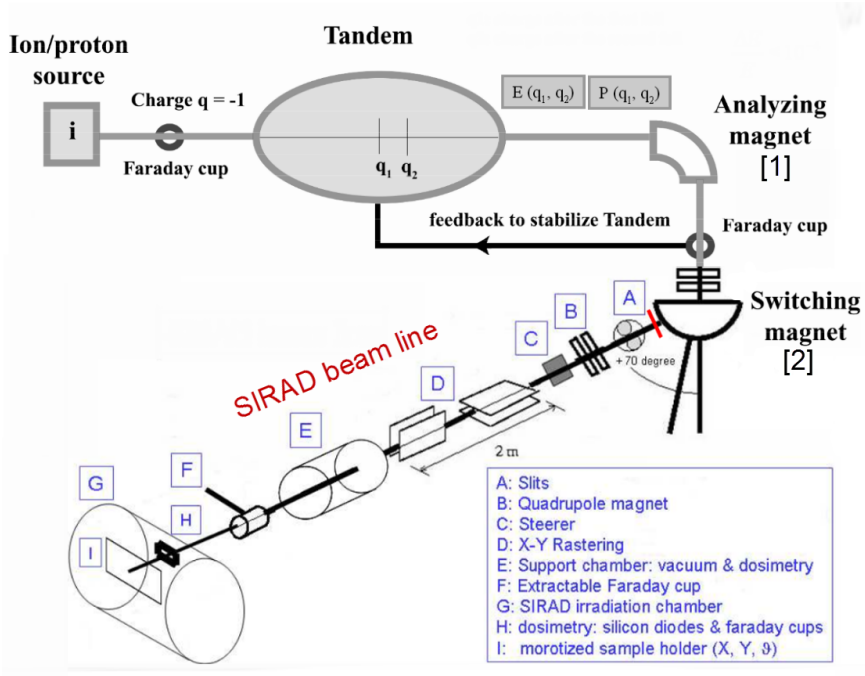


Fig. 6.9 SIRAD facility; the beam coming from the Tandem is deviated of $+70°$, then a system of wires and a Faraday cup allow to control and direct the beam to the irradiation chamber.

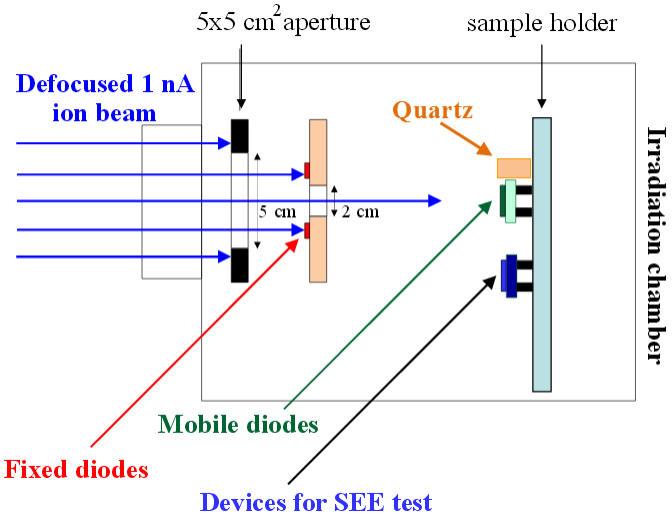


Fig. 6.10 Scheme for the irradiation chamber at SIRAD.

Energy of the beam

The ion energy at the exit of the Tandem can be calculated as:

$$E = E_{inj} + V_0 \cdot [1 + q_1 \cdot 0.25 + q_2(1 - 0.25)]$$

Where:

- E_{inj} = 0,18 MeV is the energy of the ion injected into the Tandem;
- V_0 = 11 $\leftrightarrow$ 15 MV is the operation voltage;
- q_1 and q_2 are the ion charges after the first and the second stripper foil, evaluated in unit of electron charge.

The available beams at SIRAD and their typical energies are listed in Tab. 6.4: the energy value refers to the most probable q_1 and q_2 values and with the Tandem operating at 14 MV. The table also reports the values of range in silicon and Linear Energy Transfer (LET), obtained with SRIM simulation [2] [10]. The LET is the energy deposited in the matter per unit length ($\frac{\delta E}{\delta x}$) and target silicon density, measured in MeV cm2/mg and related to the incident ion energy by the Bethe-Bloch formula.

Table 6.4 Availabe ions and relative energies at SIRAD. The ions beams are from proton (^{1}H) up to gold (^{197}Au) covering a wide range of LET.

Ion Species	Energy (MeV)	q_1	q_2	Range in Si (μm)	Surface LET in Si (MeV×cm^2/mg)
^{1}H	28	1	1	4390	0.02
^{7}Li	56	3	3	378	0.37
^{11}B	80	4	5	195	1.01
^{12}C	94	5	6	171	1.49
^{16}O	108	6	7	109	2.85
^{19}F	122	7	8	99.3	3.67
^{28}Si	157	8	11	61.5	8.59
^{32}S	171	9	12	54.4	10.1
^{35}Cl	171	9	12	49.1	12.5
^{48}Ti	196	10	14	39.3	19.8
^{51}V	196	10	14	37.1	21.4
^{58}Ni	220	11	16	33.7	28.4
^{63}Cu	220	11	16	33.0	30.5
^{74}Ge	231	11	17	31.8	35.1
^{79}Br	241	11	18	31.3	38.6
^{107}Ag	266	12	20	27.6	54.7
^{127}I	276	12	21	27.9	61.8
^{197}Au	275	13	26	23.4	81.7

[2] The software package SRIM, provided by the SIRAD group, is a Monte Carlo simulation code that allows the calculation of ion deposition profiles in materials exposed to a ions beam.

Dosimetry

The dosimetry analysis is necessary in order to know the fluence per cm^2 on the device, which is a fundamental parameter, together with the error number, in the evaluation of the SEU cross section. The SIRAD dosimetry system for low flux (10^2 - 10^5 ions/cm^2·s) irradiation is performed by two batteries of four diodes, which are placed inside the irradiation chamber . One battery is mounted on a fixed frame with a central square aperture of 2 x 2 cm^2 surrounding the device under test to monitor the beam during the measuring time. The other one is mobile and in the calibration phase it is placed on the testing sample position (see Fig. 6.11).

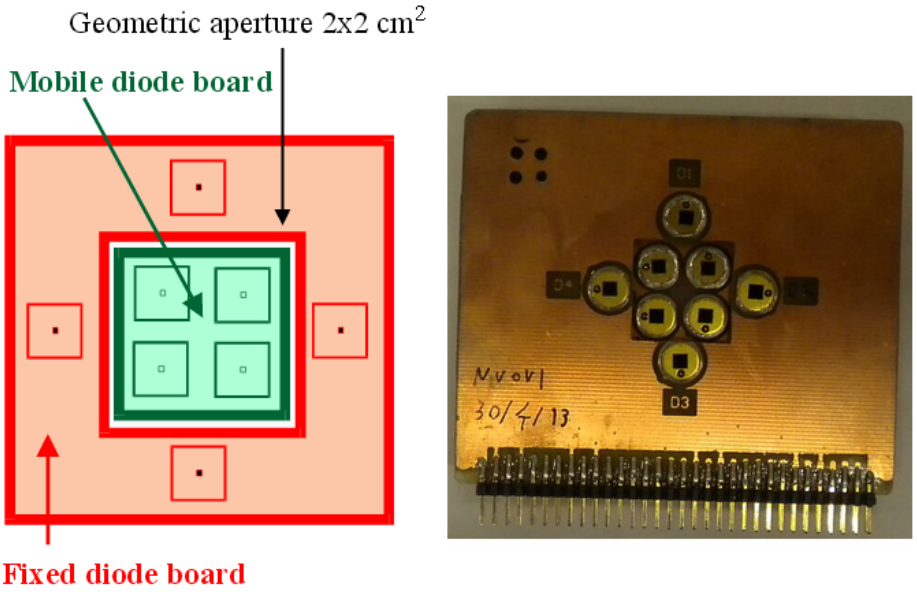


Fig. 6.11 Diodes disposition at SIRAD; on the left, a scheme of the two batteries is reported, while on the right there is a picture of the used diodes, their dimension is 5 x 5 mm^2.

Before the data acquisition, an evaluation of the beam fluence is carried out with both the diode batteries and the ratio between the fluxes on the fixed (external) and mobile (internal) diodes is stored in the dosimetry analysis program. In this way it is possible to estimate the internal fluence during the run time, when the device under test replaces the mobile diodes, just deducing it from the measurement of the fixed diodes and the ratio evaluated in advance. The beam set up procedure with all the eight diodes must be made before every set of run.

6.2.2 Data acquisition and analysis

Data acquisition

During the test of the prototypes, several ion beams, generated by different multi-sources, have been used:
→ multi- source 1: O, Si, Ni;
→ multi- source 2: F, Cl.
The incidence angle of the beam could be changed to increase the path in the target, but in these measurements has been maintained at 0° for all the acquisitions.

In case of change of position or ion, the calibration procedure has been performed, aligning the beam with the prototype using the quartz and making it uniform with the eight diodes system. After this procedure, the sample was moved under the beam and the run could start. During the test the following components have been tested:

- *ToPix 8-bit Configuration Register*, which is protected from SEU by the Triple Modular Redundancy. It means that there are three identical logic circuits performing the same process; the result is then processed by a majority vote to produce a single output. If one of the system fails, the other two can mask the problem. A correction asynchronous circuit is also foreseen to re-load the correct value in the registers when an error is detected.

- *ToPix 32-bit FIFOs*, which are protected with the Hamming encoding. The 32 bits of the cells FIFOs are encoded in a 37 bit sequence, allowing to have five redundant bits, called "parity bits", to identify SEU errors.

- *GBLD v4 56-bit I^2C Register*, which is protected, as the ToPix Configuration Register, by TMR.

Two different setups have been used to test the two devices.

In order to test ToPix, it has been connected to a ML605 Xilinx evaluation board that provides all the controls on the chip and can communicate with the computer where the system is controlled by a program developed in LabView. The clock was set to 80 MHz during the test. This study is performed by the LabView program, which controls the FPGA to carry out the following tasks:

1. it writes the configuration register with a legal bit sequence composed of alternated 0 and 1;

2. it waits for 2s;

3. it checks the register value with respect to the original ones, if it is changed then the error counter is increased and it goes to step1;

4. it goes to step 2.

Also for the FIFO structures, the process is managed by the FPGA: a test pulse with the same timing with respect to the internal reset for the time stamp ad with the input amplitude is sent periodically to four of the 640 pixels. When a wrong code is detected an error signal is generated. The number of times, in which at least one of the four signal outputs has a mismatch due to a SEU, is counted.

The acquisition system for the GBLD is composed by two programs. The first one controls the BERT, that transmits a pseudo random bits sequence to the GBLD input and receives back the data stream from the GBLD output. The second is the LabView program that gives information on SEU errors on the I^2C register. Every time that the sequence of one register in a specific event is different from the initial one, an error occurs. To calculate the SEU cross section just the total number of errors is considered, together with the total integrated fluence.

Data analysis

To evaluate the SEU rate for the two devices, the SEU cross section (σ_{SEU}) has been calculated. The σ_{SEU} is defined as the ratio of the upset number with respect to the particle fluence and is a function of the linear energy transfer (LET).

$$\sigma_{SEU} = \frac{N_{errors}}{\Phi \cdot N_{bit}}$$

where: N_{errors} is the number of SEU upsets and Φ is the fluence. The fluence has been evaluated as:

$$\Phi = F_{internal} \cdot F_{run} \cdot cos(\theta) \cdot C_{diodes}$$

where the internal factor ($F_{internal}$), used as correction parameter for the beam shape, and the fluence of the run (F_{run}) are calculated as:

$$F_{internal} = \frac{\Sigma F_{int\ diodes}}{\Sigma F_{ext\ diodes}}$$

$$F_{run} = F_{stop} - F_{start}$$

θ is the incidence angle between the beam line and the prototype surface and C_{diodes} is the correction factor depending on the diodes dimension. For a specific device, all the runs

featuring the same ion are considered to obtain the final number of errors. The tables Tab. 6.5, Tab. 6.6, Tab. 6.7 report the obtained values for SEU cross section. The σ_{SEU} error has been calculated using the Poisson formula for the single factor and then summing the results in quadrature.

Table 6.5 Values of σ_{SEU} for the ToPix v4 configuration registers. The LET values are estimated without errors.

Topix configuration register

Ion	*LET* ($\frac{MeV \cdot cm^2}{mg}$)	σ_{SEU} ($\frac{cm^2}{bit}$)
Ni	28.6	$(3.4 \pm 0.6) \cdot 10^{-9}$
Cl	13.9	$(2.3 \pm 0.3) \cdot 10^{-9}$
Si	8.90	$(1.14 \pm 0.24) \cdot 10^{-9}$
F	4.16	$(1.2 \pm 0.4) \cdot 10^{-10}$
O	3.18	$(3.2 \pm 1.2) \cdot 10^{-11}$

Table 6.6 Values of σ_{SEU} for the ToPix v4 data FIFOs.. The measurement with the nichel ion has not been performed.

Topix FIFOs

Ion	*LET* ($\frac{MeV \cdot cm^2}{mg}$)	σ_{SEU} ($\frac{cm^2}{bit}$)
Cl	13.9	$(8.1 \pm 0.4) \cdot 10^{-8}$
Si	8.90	$(6.9 \pm 0.4) \cdot 10^{-8}$
F	4.16	$(2.93 \pm 0.18) \cdot 10^{-8}$
O	3.18	$(2.69 \pm 0.21) \cdot 10^{-8}$

Table 6.7 Values of σ_{SEU} for the GBLD.

GBLD

Ion	*LET* ($\frac{MeV \cdot cm^2}{mg}$)	σ_{SEU} ($\frac{cm^2}{bit}$)
Ni	28.6	$(1.3 \pm 0.7) \cdot 10^{-9}$
Cl	13.9	$(4.5 \pm 2.2) \cdot 10^{-10}$
Si	8.90	$(3.6 \pm 1.5) \cdot 10^{-10}$
F	4.16	//
O	3.18	//

The calculated SEU Cross Sections have been charted with respect to the LET (Linear Energy Transfer). The functional relationship between the two quantity has been found using the Weibull function.

$$\sigma = \sigma_0 \cdot [1 - e^{(\frac{LET - LET_{th}}{W})^S}]$$

where

- σ_0 is the maximum probability to have a SEU;
- LET_{th} is the threshold LET for the effect occurrence;
- W is a scale parameter;
- S is a shape parameter called Weibull modulus and indicates the strength of the material; this parameter was fixed at 3, to allow the fit to follow the increasing of the cross section with the LET.

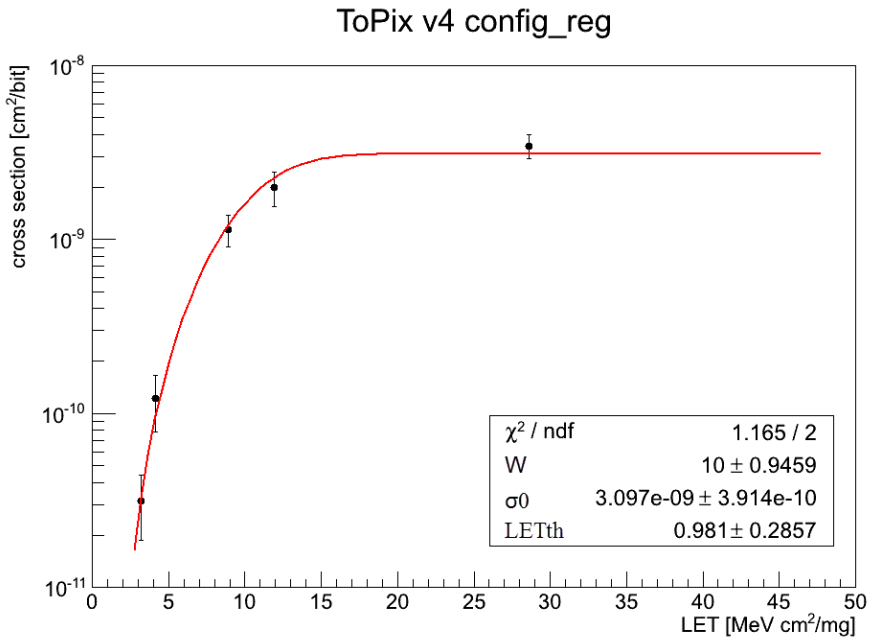


Fig. 6.12 SEU cross section versus LET for ToPix confuration registers. The low χ^2 value indicates an overestimation of the errors on the values.

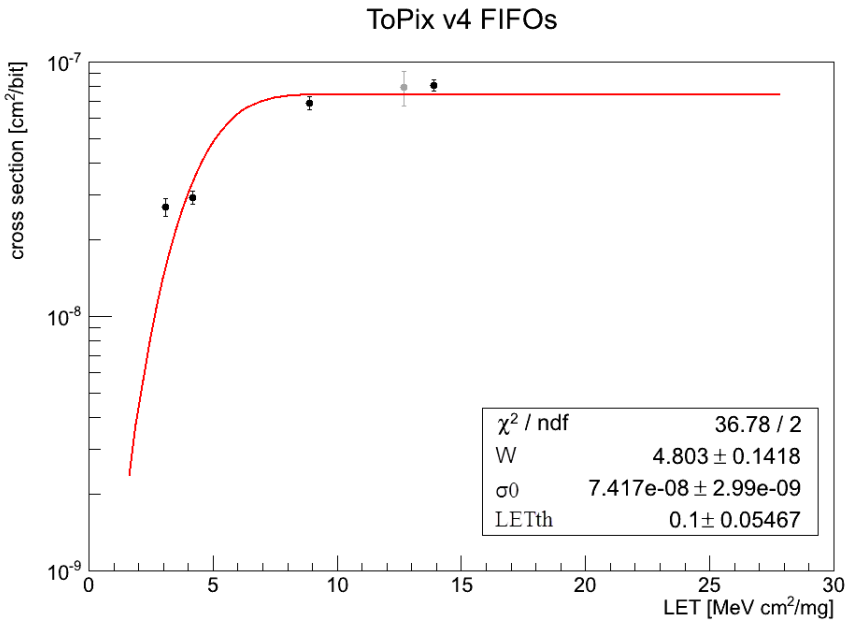


Fig. 6.13 SEU cross section versus LET for ToPix data FIFOs. In grey an extra data referred to a previous test is reported, in order to have a number of points adequate for the fit. The high χ^2 value is probably due to the value obtained for the oxygen ion, that does not fit properly with the other data. This can be due to an error during the acquisition and so the fit can be improved re-acquiring the value for this ion.

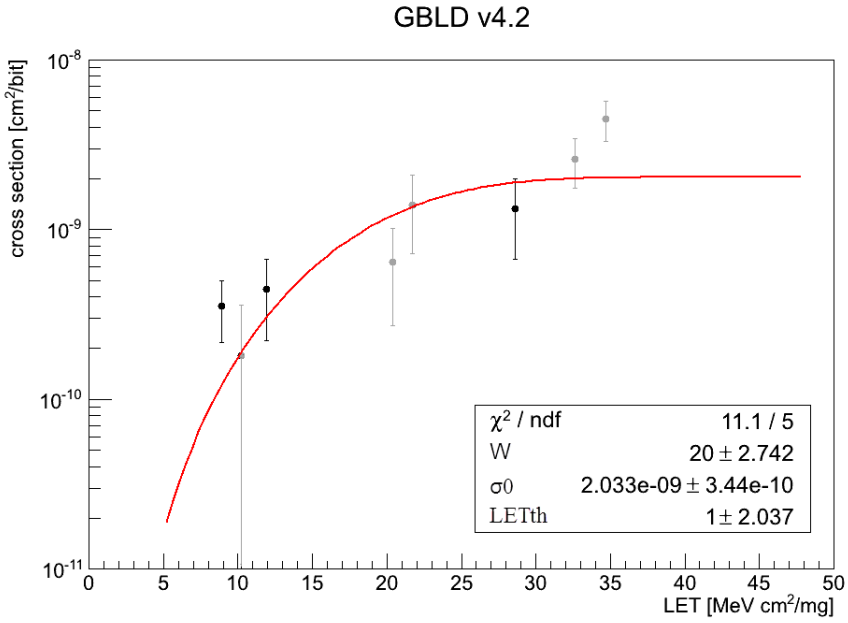


Fig. 6.14 SEU cross section versus LET for the GBLD. The chart reports two sets of data: the black data are those obtained in the test, while the grey set has been added in order to have a number of points adequate for the fit (for the S ion the large error is due to the acquired low statistics).

Results

The tests have made possible to define the saturated cross sections for the prototypes, which are:
$\sigma_0 = (3.1 \pm 0.4) \cdot 10^{-9}$ cm^2/bit for the ToPix configuration register,
$\sigma_0 = (7.4 \pm 0.3) \cdot 10^{-8}$ cm^2/bit for the ToPix FIFO,
$\sigma_0 = (2.0 \pm 0.3) \cdot 10^{-9}$ cm^2/bit for the GBLD.

Moreover, concerning the threshold of Linear Energy Transfer, the last data taken on the GBLD prototypes show that no errors have been registered with the oxigen and the flourine ions. This suggests that the LET relative to the flourine ion (4.16 MeV$\cdot$cm^2/mg) indicates a treshold value for the GBLD circuit.

Chapter 7

Conclusions

This work has introduced the GBT project for the creation of a versatile bidirectional optical link at high rate (4.8 Gb/s) to be used in HEP experiments. The communication link, developed at CERN in prevision of the future LHC upgrade, has been adapted to the $\overline{\text{P}}$ANDA MVD.

The attention has been focused on the off-detector component of the GBT, that, placed outside the radiative zone, can be realized implementing a commercial FPGA. The study of the *Example design* code and of the available hardware resources has allowed to configure the device internal cores and to successfully implement the code on the Virtex6 FPGA, placed on the ML605 evaluation kit.
The first tests, consisting in the data inspection through the Xilinx ChipScope tool, have shown that the communication between a single GBT link transmitter and receiver (connected in loopback by an optical fibre) is right established, that the clock is correctly reconstructed from the serial data stream and the received pattern corresponds to the one generated by the internal pattern generator.
During the second test, an Ethernet link with UDP protocol was used in order to establish a FPGA-PC communication link. The user interface at the PC ends of the link has been created using LabView, while the other interface has been implemented on the FPGA and has been developed in VHDL. This second test has permitted the data extraction and analysis, strengthening the results of the first test: the analyzed packets sent from the GBT receiver to the computer do not present errors.
In parallel to the main study, a work of characterization and test of the readout chip prototype for the MVD has been carried out, to check the actual state of progress in the detector development.

The future plane foresees the interconnection of the GBT-FPGA part of the link with the GBT ASIC chip, developed and already tested at CERN, and the GBT connections to the front-end modules through a set of local fully programmable E-Links.

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