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Modelling, implementation and self-calibration methods for a 12-bit SAR ADC

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Abstract

The purpose of this thesis is the study of some calibration techniques for a fully differential 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC).
The argument is introduced through some simple element about the ADCs' performances like the ideal characteristics and the quantization error in order to estimate the SNR expected. Afterwards is shown a first model, implemented in a C++ code, of a single ended SAR ADC, highlighting the more realistic features of this device as the capacitance mismatch. Therefore a fully differential model is illustrated analyzing in detail its conversion steps and the showing the common mode voltage characteristics. Due to its importance, it is also briefly explained the comparator behaviour, although it was not modelled. A paragraph about the noise shows the main sources that were taken into account in this work.
A chapter is dedicated to five important paremeters that describe the static errors: the Offset and Gain Error, the Differential Non-Linearity (DNL), the Integral Non-Linearity(INL) and the Total Unadjusted Error (TUE). These parameters caracterize the goodness of the converter linearity. In this section are shown both simulations and a real data acquisition studied with an histogram test.
Subsequently it is explained how to implement and to perform a Discrete Fourier Transform (DFT) in order to do a spectral analysis of a sinusoidal signal test. The spectral leakage offers the opportunity to show two ways to solve the problem: a proper choosing of the sampling rate and the windowing technique. In a realistic case, this dynamic perfermance test outlines the secondary and spurious harmonics which corrupt the Effective Number Of Bit (ENOB).
Later are illustrated two calibrations techniques: the Double Offset Calibration and the Density Code. Even in this section, for each technique analyzed is implemented a C++ code to study the efficiency of these algorithms and to compare them about the area employed and the number of samples required. A CR-RC model terms this chapter to show the responde of these models to a realistic signal input.
The final purpose was to obtain a synthesizable SAR ADC circuit using the Verilog language: a chapter is dedicated to explain how it was realised and the results. In the appendix there is a list of codes of this work (C++ for the simulations, PyROOT for the graphical representation and SystemVerilog code) accompanied by short explanations.