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A Charge and Time Encoder for the Microstrip Sensors of the $\overline{\text{P}}$ANDA Experiment at FAIR

Relatore:
Prof. ANGELO RIVETTI

Candidato:
ALBERTO RICCARDI

Controrelatore:
Prof. FERRUCCIO BALESTRA

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Abstract

$\overline{P}$ANDA (antiProton ANnihilation at DArmstadt) is a fixed target trigger-less subnuclear experiment that will be part of the FAIR (Facility for Antiproton and Ion Research) facility, now under construction in Darmstadt. The task of this experiment is the study of the Quantum Chromo Dynamic (QCD) in particular the explored channels are the Hadron spectroscopy, Hadrons in nuclear matter, Hypernuclei and Proton structure. The $\overline{P}$ANDA detector can be subdivided in two different subsystems, the Forward Spectrometer and the Target Spectrometer. Our interest is focused on the Target Spectrometer and in particular on the Micro Vertex Detector (MVD). The MVD employs two different kinds of sensors: silicon pixels and double-side silicon microstrips. These sensors are arranged in barrels and forward disks. This detector is the closest component to the interaction point so the event rate per channel is high. This thesis is concerned with the design of the front-end electronics for the microstrip sensors, that, owing to the high number of channels, must be implemented in the form of an integrated circuit.

The main task of this front-end ASIC is to time-stamp the event with a good time resolution and measure the signal charge with a dynamic range of at least 8-bits. To achieve these goals with a limited power consumption the Time-over-Threshold technique has been considered. The ToT technique consists in connecting a front-end amplifier to a leading edge discriminator and measuring the duration of the comparator output, which is proportional to the signal charge. The technique can be implemented with mostly digital components and it is particularly suited for modern CMOS technologies that operate with low power supply voltages. The front-end principles have been discussed with a look at the further implementation of the ToT architecture, using a preamplifier, a shaper chain and at the end of the chain, the ToT structure. The last structure is composed by a high gain amplifier, a current feedback, a baseline restorer and a comparator.

In the $\overline{P}$ANDA environment, the strip system must cope with hit rates up to 50 kHz per channel. Therefore, the front-end output signal must be relatively short. This implies that only the clock resolution is not enough to measure the signal duration, so it is necessary to use a Time to Digital Converter. The front-end and the TDC structure are designed in a $0.11\mu m$ CMOS process, a cost-affordable

technology which has recently appeared on the market.

The goal of the thesis was the design of the TDC block. In the first part of the thesis the basic concepts of TDC operation are reviewed and different TDCs architectures are briefly examined. Among the many possible topologies, a scheme based on an analog clock interpolator has been chosen because it combines good time resolution with a fairly simple implementation and low power consumption. Furthermore, this type of TDC allow for an easy calibration of the converter imperfections. The thesis reports in details the design of of the TDC building blocks and the results of extensive computer simulations done to validate the design.

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Chapter 1

$\overline{P}$ANDA

1.1 Introduction

The $\bar{P}$ANDA (antiProton ANnihilation at DArmstadt) experiment shown in figure is one of the most important project of FAIR (Facility for Antiproton ad Ion Research). Is planned to be completed in 2018, it will study the proton-antiproton annihilation and reaction of antiprotons with nucleons of heavier nuclear target. It will investigate the physics of strong interaction for understanding the way which it generates the hadron mass and quark confinement.

Still there are many fundamental questions which remain basically unanswered, for example the confinement of quarks, the origin of the masses of hadrons in the context of the breaking of chiral symmetry are long-standing puzzles and represent the intellectual challenge in our attempt to understand the nature of the strong interaction and of hadronic matter.

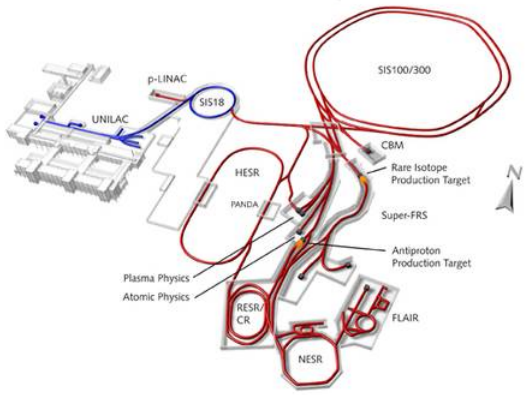

Figure 1.1: Overview of the FAIR. Is the upgrade of the GSI (blue) where the new accelerator and storage rings are in red

As we can see in Figure 1.1 the first accelerator which the particles meet is the p-LINAC, where the particles are injected and accelerated with an energy around 70 MeV in the SIS18. Here the proton can be accelerated up to 2GeV. The particles then go into the SIS100, a ring of about 1083.6m circumference length this system $4 * 10^{13}$ proton can be accumulated in a single bunch of $25ns$ time width gaining an energy of 39 GeV. Now the protons are directed in the external antiprotons produced on target. From a single bunch are produced around 10^8 antiprotons, that are select with the help of some magnets. Antiprotons are accumulated in the Collector Ring, using fast stochastic cooling that leads to have a beam momentum of 3 $\frac{GeV}{c}$ and a momentum spread of $\frac{\delta p}{p} = 3 \cdot 10^{-3}$. Antiprotons can finally go into the HESR (High Energy Storage Ring) after being in the accumulator ring (RESR) where the bunch becomes bigger, indeed the RESR is able to accommodate up to 10^{11} antiprotons[2].

In the HESR antiparticles can be accelerated between 1.5 $\frac{GeV}{c}$ and 15 $\frac{GeV}{c}$. in this accelerator we can find one of the most important components: the cooling system which employ both electronic and stochastic methods[9]. The peculiarity is given by the fact that we can use only the electronic system or both of them. The electronic cooling system injects some electrons in the beam pipe with the same phase which have the task to take out the antiprotons which are far from the beam. This solution improves the momentum resolution. Using only the electronic cooling the beam can achieve 15 $\frac{GeV}{c}$ and a resolution equal to $\frac{\triangle p}{p} = 10^{-4}$ obtaining a high intensity. If we use both systems, the resolution becomes $\frac{\triangle p}{p} = 10^{-5}$, the antiprotons momentum goes from 1.5 $\frac{GeV}{c}$ to 8.9 $\frac{GeV}{c}$ and the beam is said to be in the high resolution mode.

As of today these studies have been carried out mainly by electron machines for they clean reactions, having on the other hand low set of final states and low cross-sections. $\bar{P}$ANDA's aims to improve statistics and to further explore the physics in the charm quark's field. It will be able to benefit from the LHC experiment where there was a significant progress in the detector technology due to the new concepts and instruments. So the $\bar{P}$ANDA innovation is due to high luminosity and very good collimation of beam which allows to have large number of events and more accurate statistics.

In the $\bar{P}$ANDA apparatus, the particles emitted at large angles or in the backward direction are measured by the Target Spectrometer (TS). Particles emitted at angles between 0 and 20 degrees are measured by the Forward Spectrometer (FS). This complex setup in necessary to reconstruct the complete set of final states.

1.2 Physics channels

The purpose of $\bar{P}$ANDA is the measurements of interactions of antiprotons with nuclei in a fixed target setup and the protons-antiprotons annihilation: among the various topics concerning the properties of the strong interaction, a special attention will be given to the study of strange and charmed quarks[7].

The key of the experiment is the availability of high intensity ($L \sim 2\ 10^{32} \frac{1}{cm^2 s}$), cooled antiproton beams ($\frac{\delta p}{p} \sim 10^{-5}$) of the HESR in a momentum range between 1.5 $\frac{GeV}{c}$ and 15 $\frac{GeV}{c}$. With these characteristics it's possible to cover a wide range of studies in particular: hadron spectroscopy, hadrons in nuclear matter hypernuclei and proton structure.

The first and the second physics channels are briefly discussed in the following.

- **HADRON SPECTROSCOPY**

With the Hadron spectroscopy is possible to investigate four fields: Charmonium states, D-mesons, Baryon spectroscopy and Hybrid mesons and glueballs.

Charmonium states

Analysis of the strong interacting bound states is of primary importance for the quantitative understanding of QCD. A bound state of strong interacting quark-antiquark pair is a meson, since the strong interaction is flavor independent. All bound systems are suitable for the study of the QCD potential.The light mesons are mixtures of u, d and s and it is not possible to use the perturbation theory so is necessary the relativistic approach.

Charmonium $c\bar{c}$ and bottomonium $b\bar{b}$ are two examples of mesons without flavor. The charmonium spectrum has energy levels described by an effective central potential. It is possible to extrapolate experimentally the coupling strength, and tune the potential models on the basis of spectroscopy measurement. Precision measurements of the mass and width of the charmonium spectrum are powerful tools for the study of confinement potentials in QCD. The charmonium spectroscopy is performed accelerating the $\bar{p}$ beam to the energy of the resonance, and then performing an energy scan with a fine tuning of the beam momentum. In the directly formed resonances of the charmonium state, the precision of the mass and width measurement only depends on the accuracy on the determination of the initial $p\bar{p}$ state energy, thus on the beam momentum spread. The detector is used to identify the final states and measure the formation rate for a given resonance.

The experiments at Fermilab have shown that it is possible to conduct a precise charmonium spectroscopy with a cooled antiproton beam. The charmonium spectroscopy was performed in the 2.9 GeV $-$ 3.7 GeV energy range. Thus the

charmonium states above the open charm threshold (at 3.73 GeV) were not explored.

The open charm threshold at 3.73 GeV is the energy required to produce a D and a $\overline{D}$. The D mesons are the lightest particle containing charm quarks, paired with an up or down or strange antiquark. Above the D$\overline{D}$ threshold, the charmonium system is energetically allowed to decay into D and $\overline{D}$ meson: from the c$\overline{c}$ bound system, a pair of charmed meson and antimeson is created.

$\bar{P}$ANDA's aims are to improve and to extend the high precision measurements done at Fermilab. Its detector allows for a higher angular coverage, with the ability to detect both the electromagnetic and hadronic decay modes. $\bar{P}$ANDA will perform measurements on the entire charmonium spectrum, below and above the open charm threshold. Thanks to the small beam momentum spread ($\frac{\delta p}{p} \approx 10^{-5}$) it can study the spectrum with a resolution lower than 100 keV[6].

D-mesons

The D mesons are heavy-light QCD bound systems, containing a c quark and a lighter antiquark or viceversa. Study of these mesons gives information about the spin dependence of the quark antiquark potential at long distances. There are four ground states $D^+(c\overline{d})$, $D^0(c\overline{u})$, $\overline{D}^0(d\overline{c})$, $D^-(u\overline{c})$, the ground state and the first state observation are compatible with the theoretical prediction. The nature of these states is unclear, a precise measurement of the widths and a determination of the decay branching ratio is required in order to give a theoretical explanation. A beam momentum higher than 6.4 GeV/c allows the production of D meson pairs. The production cross section of the D meson pairs close to the threshold is related to the masses and the widths of the respective D mesons. Thus with an energy scan close to the threshold values it is possible to calculate the width of the D meson states and with a beam momentum spread of $\frac{\delta p}{p} \approx 10^{-5}$, allows a resolution of 100 keV. The large D mesons production gives the possibility to observe rare decays. This allows to investigate physics aspects connected to the weak interaction probing the Standard Model and the study of the rare decays of the D mesons are important to probe symmetry violations.

Baryon spectroscopy

The baryon spectrum is poorly understood and there is a low agreement between spectroscopy measurements and the quark model predictions. Some of the low lying states are shifted, and there is no experimental validation of the prediction of the higher lying states. In p$\overline{p}$ collisions there is a large cross section for the production of a baryon antibaryon final state: with a p beam momentum of 3

GeV/c there is an equal production rate of baryonic and mesonic final states. In addition to that, the p$\overline{p}$ annihilations are well suited for the study of strange and charmed baryons, since is not required the production of K or D mesons for the conservation of strangeness or charm. In the Λ and Σ spectrum there are new observed states waiting for confirmation and interpretation. The experimental knowledge on the multi-strange Ξ and Ω states is very poor. The production yield of the Ξ ground state and the Ξ^* resonances allows for good statistics studies.

Hybrid mesons and glueballs

The meson with gluonic excitation are called Hybrid Meson (q$\overline{q}$g) and the gluonic excitations within a neutral color bound system are allowed by QCD. The gluons carry units of angular momentum that are proportional to their excitation, thus they contributes to the total quantum number of the bound system. QCD also allows, for neutral bound state made entirely of gluons, the glueballs (gg or ggg), their properties are determined by the long-distance features of the strong interaction. There is not yet a precise identification of their quantum numbers for an exactly theoretical interpretation but in the experimental field there are several observation of gluonic hadrons candidates.

The experimental confirmation is very important for the understanding of dynamics of low energy in QCD and the structure of QCD vacuum. $\overline{P}$ANDA will investigate the gluonic hadrons mass range with the high luminosity modality in order to observe the candidates states, then with a cooled antiproton beam will be performed high precision measurements in the interesting mass region. Finally, spin-orbit analysis and a fully exclusive reconstruction will be executed for the determination of the quantum numbers of the observed states.

The light hybrid mesons, constituted by u, d and s quarks are expected to have strongly overlapping states with wide resonances and to form mixing states with the ordinary hadrons. For these reasons their experimental investigation and clear identification are difficult.

The gluon has two color-excitation modalities, the lower energetic mode is the Transverse Electric (TE) and the higher energetic mode is the Transverse Magnetic (TM). The gluon angular momentum coupling generates 8 states, 3 of them exhibits exotic quantum numbers, the observation of exotic states will be a clear sign of gluonic excitation. The hybrid states with non exotic quantum numbers are important because they can be directly formed in p$\overline{p}$ annihilations, in this way it is possible the precise measurement of their mass and width.

- **HYPERNUCLEI**

A hyperon is a nucleon where one or more quarks u or d are replaced with a strange quark. Hypernuclei are nuclei where one or more nucleons are replaced by hyperons, introducing a new flavor: the strangeness.

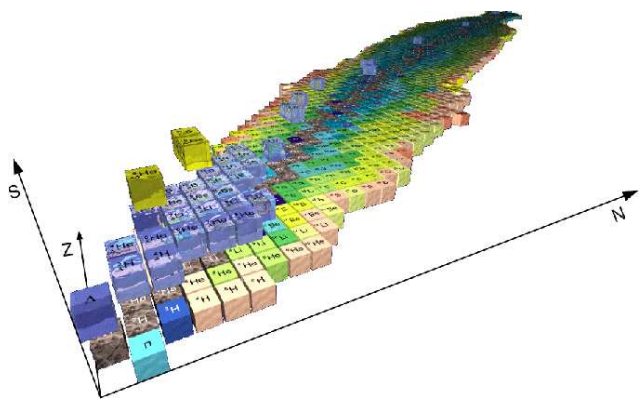

Figure 1.2: Hypernuclei table (from [2])

The S = 0 plane contains the ordinary nuclei, the S = −1 plane contains the nucleons with Λ or Σ hyperons and the S = −3 plane contains the nucleons with ΛΛ or Ξ hyperons. The hyperon ground state could decay only by weak interaction, the lightest hyperon is the Λ^0 (uds). The access of the hyperon to these nuclear energy levels is not restricted by the Pauli principle. This principle offers the opportunity for nuclear spectroscopy and the study of the hyperon nucleon interaction, in particular the spin-dependent part of the nuclear potential. The central part of the $\bar{P}$ANDA detector can be replaced with an experimental setup for the precision γ ray spectroscopy of single and double hypernuclei. Since it is a multistage process, the spectroscopic information are obtained by the identification of the weak decay products. The γ-ray detection from the disexcitation of the bound hypernuclei within the nuclear potential allows an unique identification of the double hypernuclei. A γ-rays detection with a resolution of 3.4 keV will be performed with an array of germanium detectors close to the target.

1.3 The $\bar{P}$ANDA detector

The most important detector requirement are the 4π angle coverage, high resolution for tracking, particle identification high rate capabilities and versatile readout[10]. The $\bar{P}$ANDA detector is composed by two magnetic spectrometers, the first one based on a superconducting soleonid magnet surrounding the

interaction point for the measure at the large polar angles, called TARGET SPECTROMETER (TS). The second one, the FORWARD SPECTROMETER (FS), based on a dipole magnet for the measure at the small angles. A representation of the two detector is shown in Figure 1.3

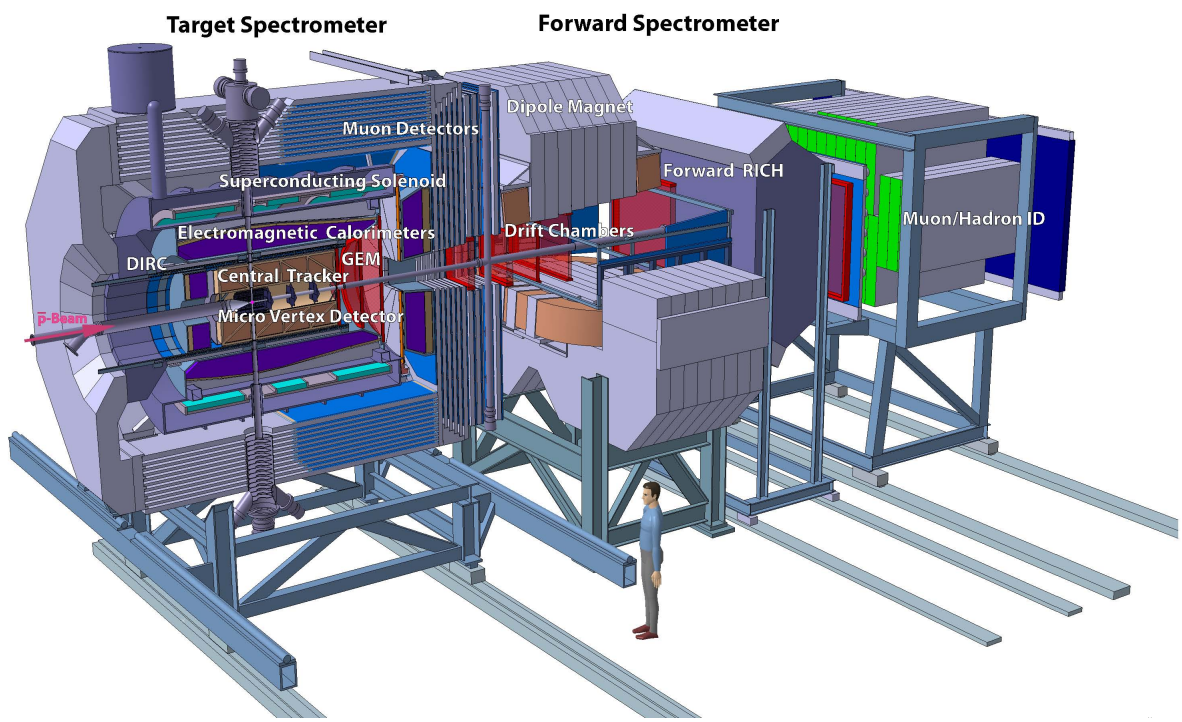

Figure 1.3: $\overline{P}$ANDA detectors (from [2])

The Target Spectrometer

As already said, the Target Spectrometer will surround the interaction point and measure charged tracks in a highly homogeneous solenoidal field, the pipe target will have to cross the spectrometer perpendicularly to the beam pipe. The target Spectrometer will consist of three parts. The first on is the barrel covering angles between 22 degrees and 140 degrees, the second one is the forward and cap extending the angles down 5 degrees and 10 degrees in the vertical and horizontal planes, and the third one is the backward end-cap covering the region between 145 degrees and 170 degrees[1]. The setup includes the subsystems MVD, CENTRAL TRAKER, CHERENKOV DETECTORS, CALORIMETERS and MUON DETECTORS.

- Solenoid Magnet

It has the task of generating a very homogeneous solenoid field of 2 T with fluctuations of less than 2%. This supercunducting coil has a length of 2.8m and inner diameter of 90 cm. The cryostat for the solenoid coils is required to have tow warm bores of 100mm diameter for the indention of the internal target.

- Micro Vertex Detector (MVD)

It is the detectors closer to the interaction point and is made by pixel and double sided microstrip and is optimized for the detection of the secondary vertex. There are two barrel of pixel detector, two barrel of microstrip and six disc arranged perpendicularly to the beam pipeline.

- Central Tracker

Its goal is to obtain a good efficiency in the tracking of secondary vertex. There are two methods to reach it: the first one use STraw Tubes (STT), the second is based on three sets of GEM trackers to include particles below 22° which are not covered by STT.

- Čerenkov Detector

A Čerenkov detector is a particle detector using the mass-dependent threshold energy of Čerenkov radiation. This detector allows a discrimination between a lighter particle, which does radiate, and a heavier particle, which does not radiate.

- Electromagnetic Calorimeter

There are a complex scintillators formed by lead-tungstate, because this materiel have a good resolution in photon, electron and hadron defection and also have a fast response.

- Muon Detector

Is formed by 72 strips of scintillator counter behind the target spectrometer and an equal number of strips are placed perpendicular to the beam axis.

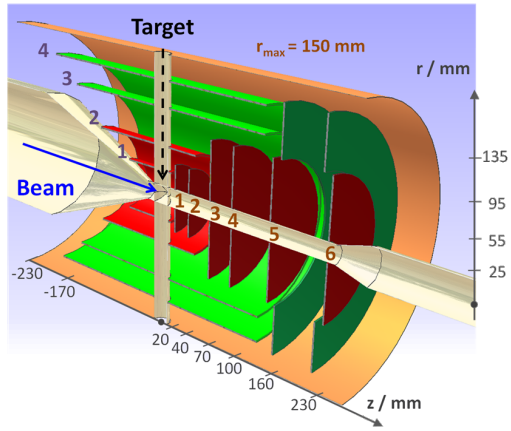

Figure 1.4: Micro Vertex Detector outline (from [2])

The concept of the MVD is based on radiation hard silicon pixel detectors with fast individual pixel adopt circuits and silicon strip detectors. The layout foresees a four layer barrel detector with an inner radius of 2.5 cm and an outer radius of 13 cm.

In particular, the pixel sensors cover the 1st and 2nd barrels and the central part of the forward disks for an area of 0.11 m^2, with 11 M readout channels. In the other region the particle flux is lower so it is used a double sided strip sensor (DSS) in order to reduce the material budget. The DSS sensors will cover the 3rd and 4th barrel and the external region of the 5th and 6th forward disks, for an area of 0.5 m^2, with 200 k readout channels.

1.4 Principles of detection system

In this system it is necessary that the sensor and the Front-end register which particle hits and where. In particular, this thesis is focused on the Strip detector. In this kind of detectors the magnitude of the measured signal on a given electrode depends on its relative position compared to the site of charge formation. Angled tracks will deposit charge on two or more strips. Evaluating the ratio of charge deposition allows interpolation of the charge track to provide position resolution better than expected from the electrode pitch alone.

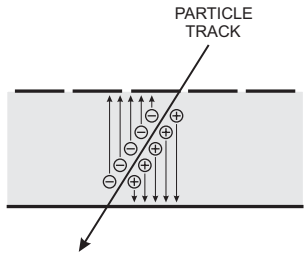

Figure 1.5: Electron-Hole pair generation in a silicon strip

Two-dimensional position revelation is more simple using crossed strips, but has problems at high hit densities. Each hit generates an x- and a y-coordinate. However, n tracks generate n x-coordinates and n y-coordinates, simulating n^2 hits of which $n^2 -$ n are fake.

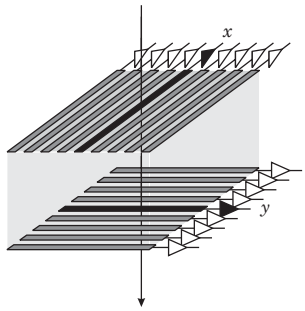

Figure 1.6: Space coordinates system of silicon strips

The "ghost" can only be eliminated with additional information which allows the exclusion of coordinates not consistent with tracks. Clearly this is a formidable task in a mixture of stiff and soft tracks with low momentum particles looping in a magnetic field. A compromise solution that is often adequate utilizes "small angle stereo", where the strips subtend a small angle, rather than 90°. The area

subtended by two sensing elements (strips) of length L_1 and L_2 arranged at an angle 90° is A = $L_1 L_2$. So a hit in a given strip can form combinations with hits on all of the transverse strips and leading to maximum probability of "ghosting". However, if the angle α subtended by the two strip arrays is small enough (and their lengths L are approximately equal), the capture area is now

$$A \approx L^2 \frac{p_2}{p_1} tan\,\alpha + L\,p_2 \tag{1.1}$$

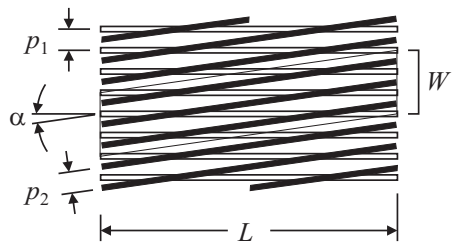

Figure 1.7: Strip setup to avoid the ghost hit

The probability to have multiple hits within the acceptance area and hence the number of "ghosts", is reduced as α becomes smaller, but at the expense of resolution loss in the longitudinal coordinate [15].

Chapter 2

Front-end

The first building block of a readout chain is the front-end. This structure allows to modify the input signal shape in order to simplify the extraction of the information of interest. The first device is a charge sensitive amplifier, which is composed by an amplifier with a feedback capacitance converting the input current signal into a voltage step. However it is necessary to shunt the capacitor with a resistance in order to guarantee the amplifier feedback in DC. With this configuration the output signal has an exponential decay. The introduction of this resistance involves a pole in the transfer function so it is necessary to include a pole-zero cancellation network. In order to measure the charge collected by the detector, we use the Time over Threshold (ToT) technique, where the information is extrapolated from the signal length. Once a threshold is set, we want to measure the time during which the signal stays over this value, since the charge is directly proportional to the signal length. The ToT stage can saturate but this is not an issue, since the information about the length and hence the charge, is not compromised. After the ToT amplifier the signal goes into a comparator which gives a high voltage signal when its input rises above the fixed threshold, and falls down when the amplitude value is lower.

2.1 Charge Sensitive Amplifier (CSA) and Shaper

As introduced above, the task of the Charge Sensitive Amplifier is to do a first process of the signal from the detector[16]. This structure is made by a high gain amplifier with a feedback capacitor that integrates the input charge, and a resistance providing a feedback DC path. The described architecture is like this:

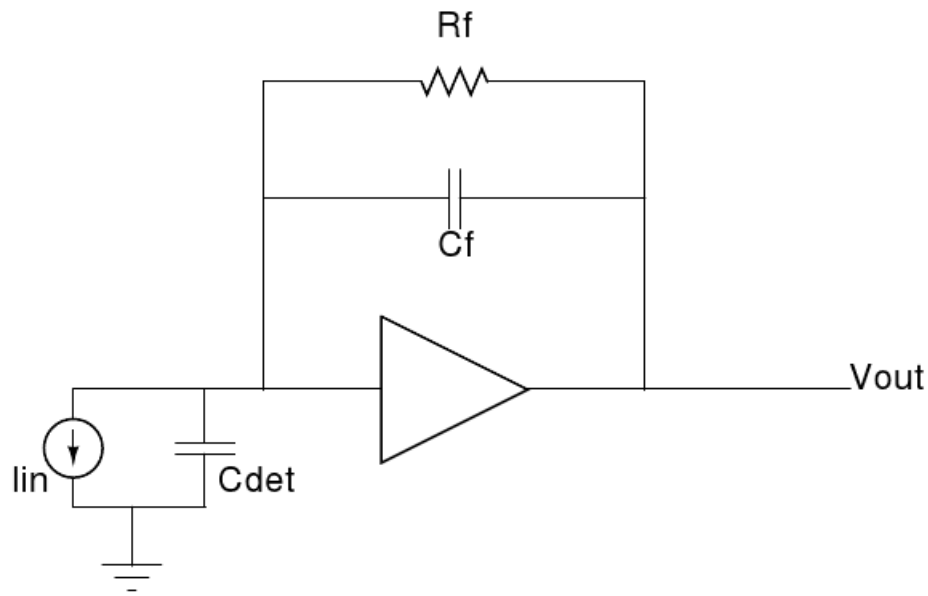

Figure 2.1: Charge sensitive Amplifier schematic

To understand better its behavior, we can do some approximations:

- The input signal is a Dirac δ pulse, so the current is $i(t) = Q_{in}\,\delta(t)$
- The amplifier has infinite bandwidth
- The amplifier has infinite gain
- The R_f has an infinite value, so its contribution can be neglected

Under these hypothesis, the output of the CSA is:

$$V_{out} = \frac{1}{C_f} \int i(t)\,dt \tag{2.1}$$

since $i(t) = Q_{in}\,\delta(t)$ we obtain:

$$V_{out} = \frac{Q_{in}}{C_f}\,\Theta(t) \tag{2.2}$$

where $\Theta(t)$ is the Heaviside function.

As previously written, the task of the complete chain is to measure the signal length, but the CSA output doesn't return to the base line value. So it is necessary to use another stage to modify the signal shape: this circuit is the CR-RC SHAPER. The simplest shaper structure is shown in the following figure:

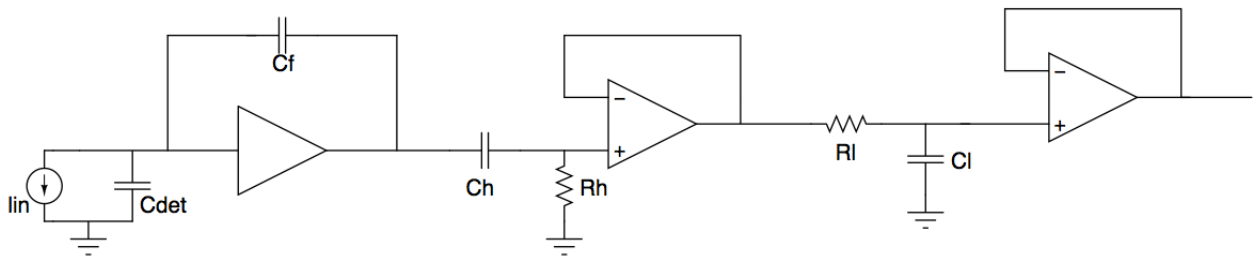

Figure 2.2: Schematic of general CSA and CR-RC shaper

It is composed by high-pass and low-pass filters. These are separated by a buffer to decouple their time constants. The global transfer function is just optioned by multiply the transfer functions of the individual blocks. The first architecture that we find is the high-pass filter, which gives the following output:

$$V_{RHF}(s) = \frac{V_{CSA}}{s} \frac{s\, C_h\, R_h}{(1 + C_h\, R_h)} \tag{2.3}$$

We can observe that the pole introduced by the CSA is eliminated by the high pass filter. Taking the inverse Laplace Transform we obtain: is:

$$V_{RHF} = \frac{Q_{in}}{C_f}\, e^{-\frac{t}{\tau_h}} \tag{2.4}$$

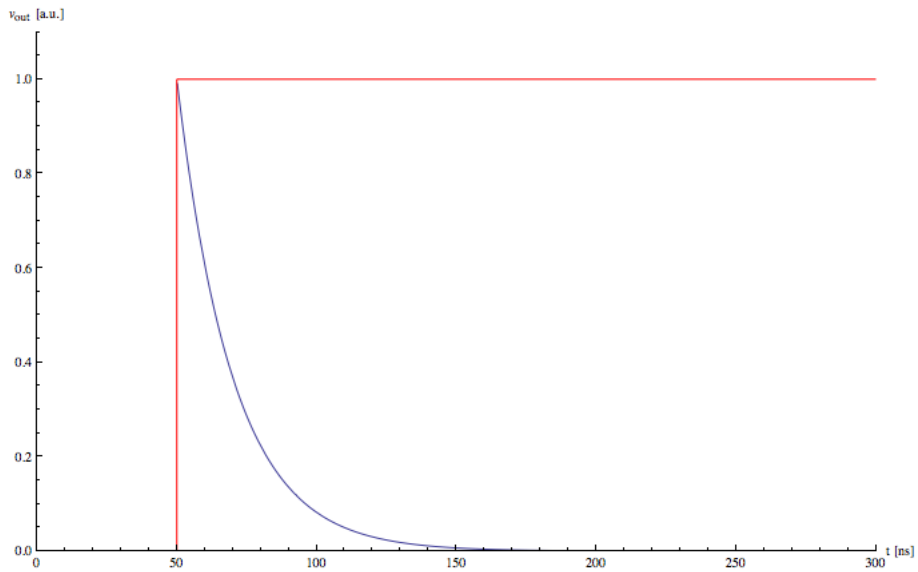

Figure 2.3: Output before at the CSA and output after the CR

As we can see from the graphic the signal now reaches the baseline value in a finite time and the maximum value is $\frac{Q_{in}}{C_f}$. The goals of this circuit are two: the first one is to improve the SNR and the second one is to allow the signal to reach as fast as possible the baseline value in order to reduce the possibility of having the pile up effect. However the analysis of this kind of signal results difficult since it has a very narrow peak and then it is complex to sample it involving in a greater jitter error. To solve this problem we can use a low pass filter which increases the peak length as shown in figure. The output in the Laplace domain is given by:

$$V_{CLF}(s) = \frac{Q_{in}}{C_f} \frac{\tau_h}{(1 + s\,\tau_h)\,(1 + s\,\tau_l)} \tag{2.5}$$

where $\tau_l = R_l\,C_l$. If we now use the inverse Laplace Transform we can pass from the s domain to the time domain and the output becomes:

$$V_{CLF}(t) = \frac{Q_{in}}{C_f} \frac{\tau_h}{\tau_h - \tau_l} \left(e^{-\frac{t}{\tau_h}} - e^{-\frac{t}{\tau_l}}\right) \tag{2.6}$$

As we can see in the following figure if we change the time τ_l , with fixed τ_h, the signal length changes too

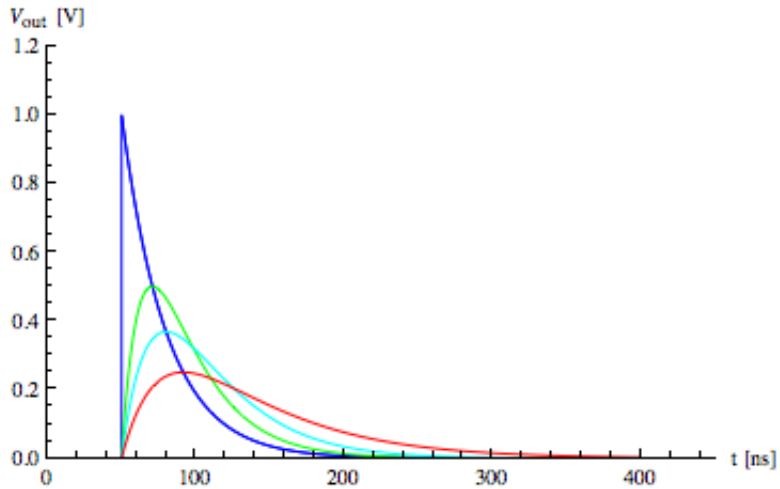

Figure 2.4: Variations of the Shaper output for different τ_l

The question now is: what is the best value for $\frac{\tau_h}{\tau_l}$?
As we can see in the above figure the best result is achieved when the ratio is equal to 1, because we have a good compromise between the peak amplitude and the time duration. We can also define another important parameter, called peaking time, which corresponds to the time when the signal reaches its maximum value. Considering the best condition $\tau = \tau_l = \tau_h$ the signal is

$$V_{out}(t) = \frac{Q_{In}}{C_f}\,\frac{t}{\tau}\,e^{-\frac{t}{\tau}} \tag{2.7}$$

and to evaluate the peaking time we need to solve the following equation:

$$\frac{d\left(V_{out}(t)\right)}{dt} = \frac{1}{\tau}\,e^{-\frac{t}{\tau}} - \frac{1}{\tau^2}e^{-\frac{t}{\tau}} = 0 \tag{2.8}$$

thus $T_P = \tau$

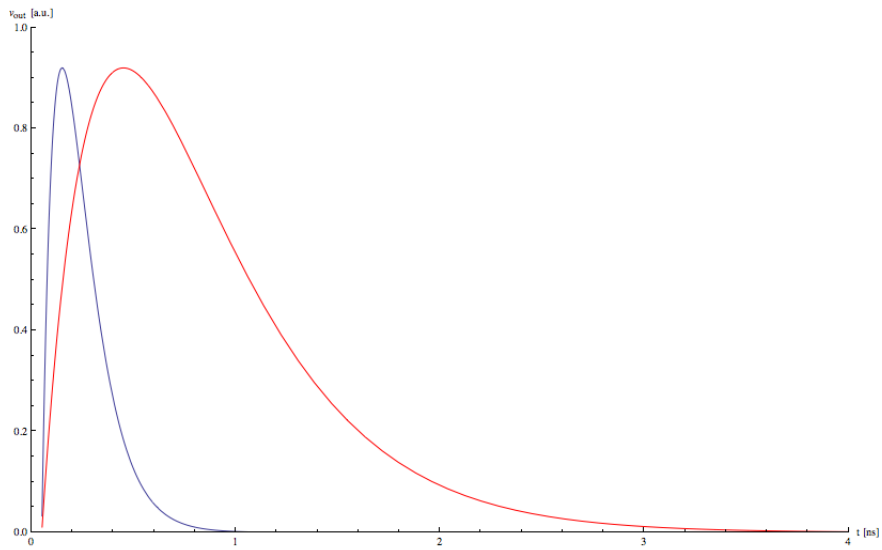

Figure 2.5: The same signal with different peaking time

this is an important result since the peaking time coincides with the shaping time τ, meaning that we can control the peaking time value thought the R C product.

2.2 Real Amplifier

We now study what happens when some of the approximations made before are relaxed.

2.2.1 Polo zero cancellation

The first case that we explore concerns the finite value of the feedback resistor R_f,which implies that the signal has an undershoot as shown in the figure below:

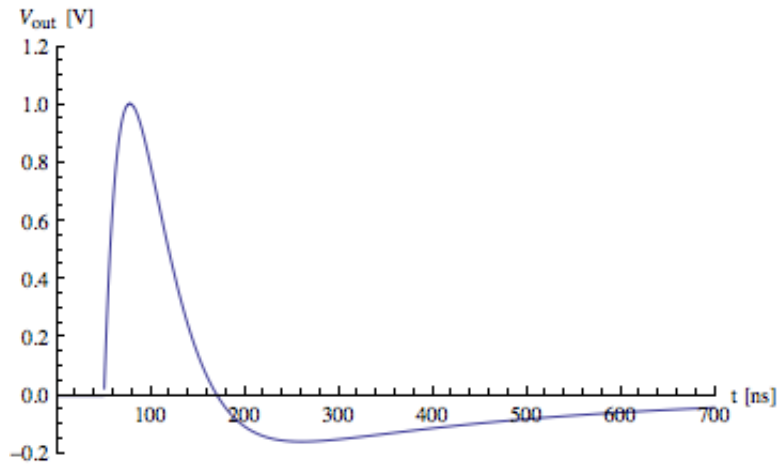

Figure 2.6: Signal at the output of the shaper with a real resistance in the CSA

The undershoot derives from the fact that the CSA output is not a voltage step. After the signal reaches its maximum value, it falls down with a decay time that depends on R_f: the bigger it is, the slower the trailing edge of the signal will be. This is because the resistor displaces the pole form the origin so that it does not coincide anymore with the zero given by the high pass filter. The technique that is used to circumvent this effect is called polo zero cancellation. The problem of the undershoot is given by the fact that it generates a baseline shift effect at high rate, which must be removed. Since R_f is not negligible the output becomes:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \frac{C_f\, R_f}{(1 + s\, C_f\, R_f)} \frac{\tau}{(1 + s\, \tau)^2} \tag{2.9}$$

As we can see in the equation we have displaced the CSA pole, in order to eliminate this effect we need to insert another resistance in parallel with C_h, as shown in figure.

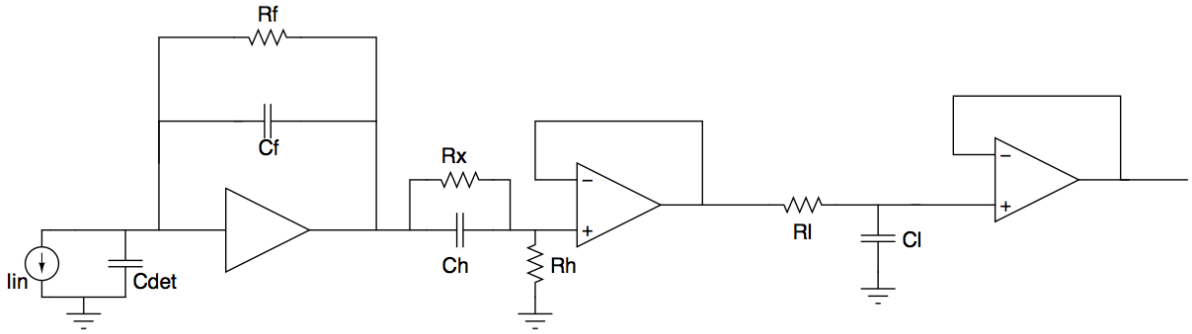

Figure 2.7: Schematic for the compensation due to real value of R_f

The transfer function becomes:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \frac{\tau_f}{(1 + s\,\tau_f)} \frac{R_h\ (1 + s\,C_h\,R_x)}{R_h\,(1 + s\,C_h\,R_x) + R_x} \frac{1}{(1 + s\,\tau)} \tag{2.10}$$

In this case if we place the time constant, given by $R_x\,C_h$, equal to the constant time τ_f, we can eliminate the pole induced by the finite value of R_f and the transfer function becomes:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \frac{C_f\,R_f\,R_h}{R_h\,(1 + s\,C_h\,R_x) + R_x} \frac{1}{(1 + s\,\tau)} \tag{2.11}$$

2.2.2 Finite Gain

We consider now the case where the amplifier has a finite gain. For simplicity R_f is negligible involving that we can no longer consider that the amplifier has a virtual ground in the input and its transfer function is:

$$\frac{V_{out}}{I_{in}} = -\frac{A_0}{s\,[C_T + (1 + A_0)\,C_f]} \tag{2.12}$$

Before, when the gain was infinite, the transfer function was simply:

$$\frac{V_{out}}{I_{in}} = \frac{1}{s\,C_f} \tag{2.13}$$

The finite gain of the amplifier can lead to cross talk. In fact in a multi-channel system having no longer a perfect virtual ground can couple the channels through their mutual capacitance C_M[4]. This situations is shown in the following figure we see that injecting a signal on one channel induces a signal also on its neighbor:

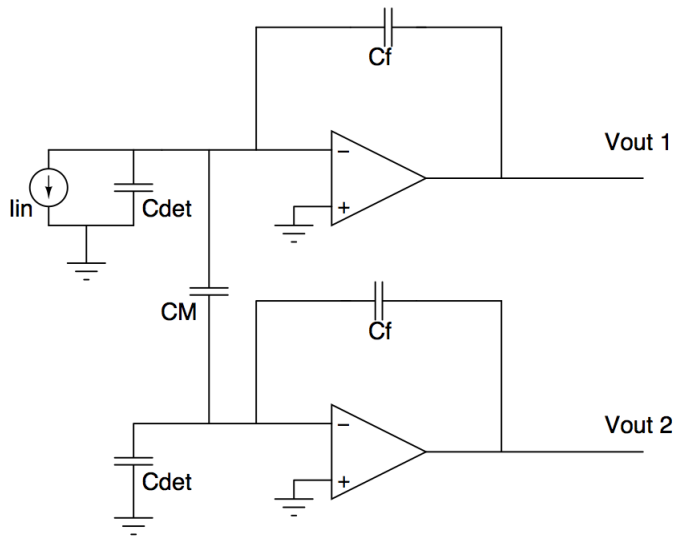

Figure 2.8: Multichannel representation

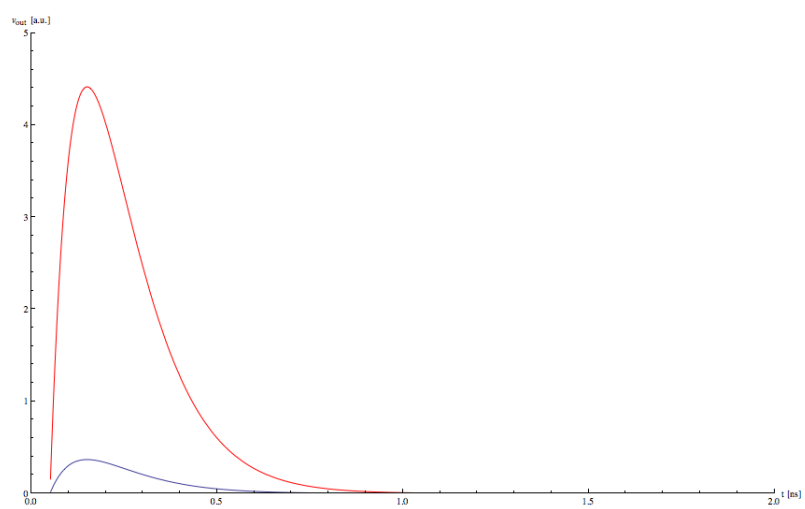

Figure 2.9: V_{out2} for two different gain value

2.2.3 Finite Bandwidth

To study the effect of the bandwidth limitation of the amplifier we use the small signal model. This study involves to considering a capacitor C_L between the output and ground.

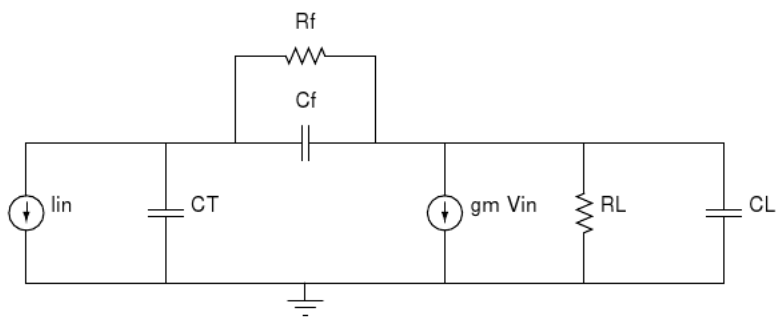

Figure 2.10: Small signal model of the CSA

If we neglect R_f the transfer function of this model is

$$\frac{V_{out}}{I_{in}} = \frac{\left(1 - s\,\frac{C_f}{g_m}\right)}{s\,C_f\,\left[1 + s\,\frac{C_L\,C_T + (C_T + C_L)\,C_f}{g_m\,C_f}\right]} \tag{2.14}$$

while in the time domain is

$$\frac{V_{out}}{I_{in}} = -\frac{Q_{in}}{C_f}\,\left(1 - e^{-\frac{t}{\tau_r}}\right) \tag{2.15}$$

where $\tau_r = \frac{C_L\,C_T + (C_T + C_L)\,C_f}{g_m\,C_f}$. So as we can see in the formula the signal is not a voltage step, it doesn't reach the maximum value instantly but in a time equal to τ_r. Now if we also consider the finite value of R_f the output becomes:

$$V_{out} = \frac{Q_{in}}{C_f}\,\frac{\tau_f}{\tau_r - \tau_f}\,\left(e^{-\frac{t}{\tau_r}} - e^{-\frac{t}{\tau_f}}\right) \tag{2.16}$$

and the peaking time is:

$$\frac{dV_{out}}{dt} = 0 -> T_p = \frac{\tau_f \, \tau_r}{\tau_f - \tau_r} ln \left(\frac{\tau_r}{\tau_f} \right) \tag{2.17}$$

replacing this value in the output equation we obtain the maximum reachable value:

$$V_{out}(T_p) = \frac{Q_{in}}{C_f} \left(\frac{\tau_f}{\tau_r} \right)^{\frac{\tau_r}{\tau_r - \tau_f}} \tag{2.18}$$

We can observe that the maximum value is proportional to the ratio between the two time constants representing the rise and the fall times. The resulting effect is that once a value of τ_f is fixed, if τ_r is big the signal doesn't have time to reach the maximum value before the discharging process begins driven by τ_f. If τ_r is small the signal can reach the maximum value.

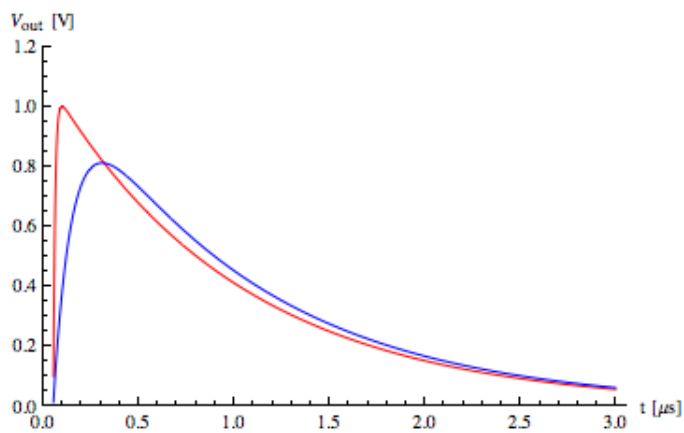

Figure 2.11: Balistic deficit effect

The difference between the maximum voltage value reached and the ideal maximum voltage value is called ballistic deficit.

Now the signal has been fairly processed so can be analyzed through the Time Over Threshold technique.

2.3 Time Over Threshold

As mentioned before, in order to measure the deposited charge in the sensor it is possible to use several techniques, but we use the Time Over Threshold (ToT) technique. This method uses the amplitude of signal coming from the Front-end stage, and so the time duration, proportional to the deposited charge in the strip. We want to measure the time which the signal stays above fixed voltage threshold and the schematic is showing here:

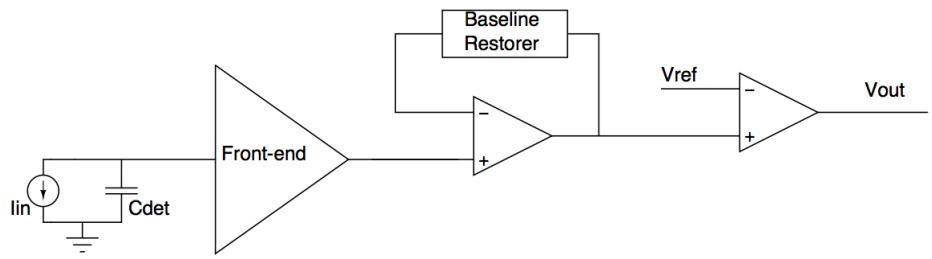

Figure 2.12: Complete schematic of front-end and ToT

A peculiarity if this architecture is that we can use an amplifier with a very fairly high gain. In fact it is not important if one stage saturated provided that the duration of the signal is still proportional to the charge. This consideration does not apply the first stage. In fact if one amplifier saturates its gain is drastically reduced. As we discussed before a reduction of the open loop gain in the charge sensitive amplifier implies an increase in cross talk. Therefore it is exactable that all the stages in the chain but the first one saturated.

In principle the duration of a signal can be measured by counting the system clock cycles. In $\overline{P}$ANDA a clock of 160MHZ will be distributed to all the subsystems. Each strip channel will have to cope with a signal rate in axes of 50kHZ wile encoding the charge over a 10 bits dynamic range. Therefore using the clock to measure the time imply that the longest signals will take $6.25ns \cdot 2^{10} = 6.4\mu s$ to be digitize. Furthermore the smallest signals wood be encoded with only a few bits and also since the event rate for each strip is $30KHz$ and this involves that we have big problem with the pile-up effect. To address this issue one can increase the resolution of the time digitization beyond what allowed by a simple clock counting skims. This allows to reduce the duration of the front-end pulse and to increase the resolution. However to improve the resolutions behind the clock limit a time to digital converter is needed. It is very important that such a TDC as very low power consumption and area. The design of this building block is the specifics focus of this theses.

Chapter 3

Time to Digital Converter

The task of the Time to Digital Converter (TDC) is to convert a signal from the time domain to the digital domain. There are two kinds of TDCs: the Analog TDCs, which convert the signal from the time domain to an analog domain and then to the digital domain, and the digital TDCs that use digital parts.

3.1 Analog Time to Digital Converters

A classical structure of an Analog TDC is like the one shown in figure, where the difference between the start signal and the stop signal represents the time which we want to convert. At this point an integrator change the impulse into a voltage signal which is converted by an ADC [5].

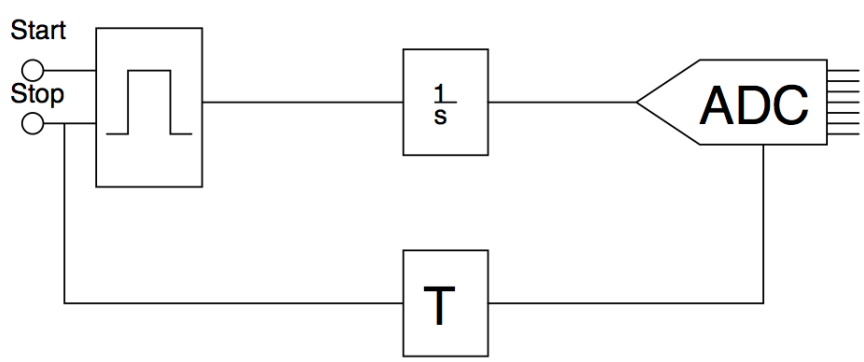

Figure 3.1: Block Digram of Analog TDC

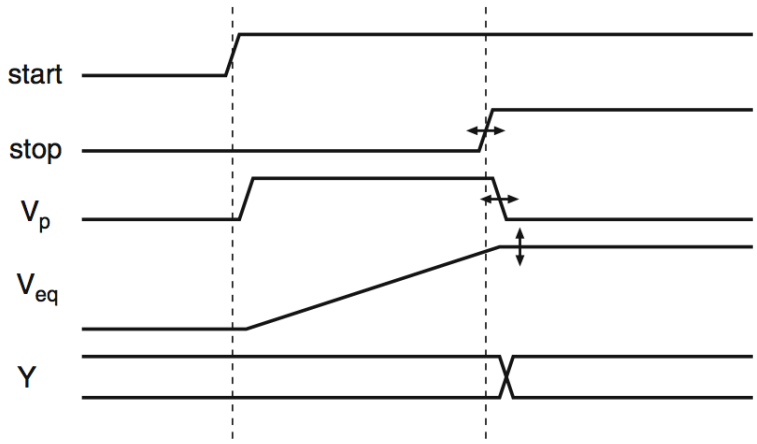

Figure 3.2: Signal evolutions of Analog TDC

An important parameter is the Dynamic Range (DR) indicating the maximum time that the circuit can convert with N bits and T_{LSB} resolution:

$$DR = 2^N \, T_{LSB} \tag{3.1}$$

As we can see, using the same number of bits we need to measure shorter time in order to have a more accurate measure results, decreasing the dynamic range. To have a better resolution it is possible to introduce several conversion stages but, obviously, involving a larger power consumption and a bigger area.

The drawbacks of this approach are the relatively low speed and the effect that all devices must ensure the linearity for the full conversion range.

3.2 Fully Digital Time to Digital Converters

As written above the purpose of the implementation of a TDC is to have a precise time measure. For this reason we can improve the TDC resolution using only digital components, in principle it is enough to have a clock and a counter.

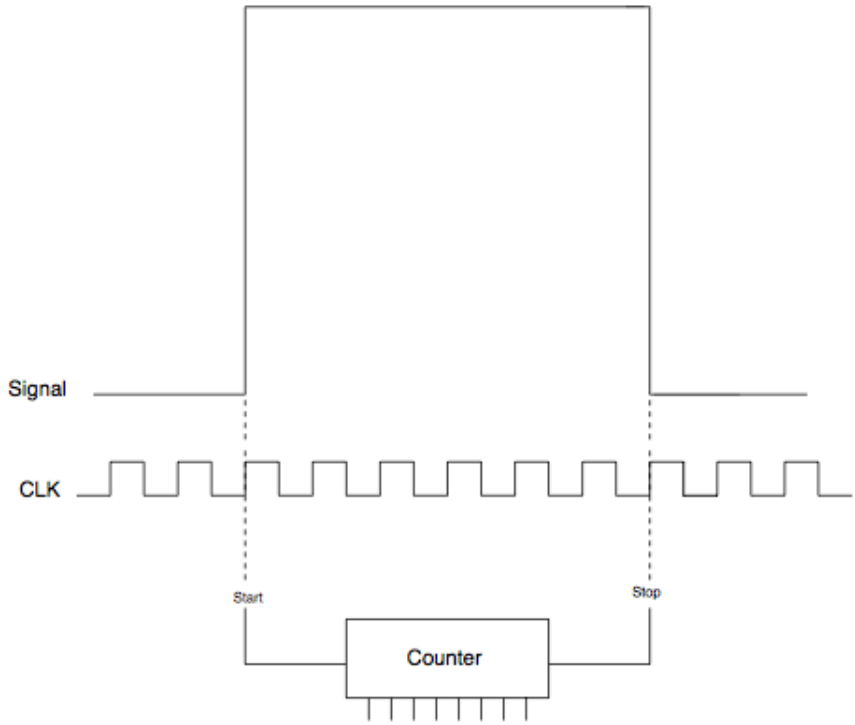

Figure 3.3: Base principle of a Digital TDC

The start and the stop may be asynchronous, involving the introduction of an error on the measure, leading to a time measure:

$$\triangle T = N\,T_{CP} + \triangle T_{stop} - \triangle T_{start} = N\,T_{CP} + \varepsilon_{\tau} \tag{3.2}$$

where N is the counts number and $\varepsilon_{\tau}\,\epsilon\,[-T_{CP}; T_{CP}]$ is the quantization error.

A high clock frequency is necessary to reach an high resolution, this involves a bigger power consumption. As an alternative we can divide the clock period into small asynchronous intervals. Now the time measurements becomes:

$$\triangle T = N\,T_{CP} + (T_{CP} + \triangle T_{stop}) - (T_{CP} - \triangle T_{start}) \tag{3.3}$$

where

$$\triangle T_{start} = N_1 \frac{T_{CP}}{k} - \varepsilon_1 \tag{3.4}$$

$$\triangle T_{stop} = N_2 \frac{T_{CP}}{k} - \varepsilon_2 \qquad \varepsilon_1 = \varepsilon_2\,\epsilon\,[0; \frac{T_{CP}}{k}] \tag{3.5}$$

the resolution is $\frac{T_{CP}}{k}$, now improved by a factor k indicating the number of intervals where the clock was subdivided into: N_1 and N_2 are the start and the stop position in the respective clock period.

In order to divide the clock period, we can use either Digital Delay Line or Inverter. The two structures have similar schematics but in the fist case there are some simple flip-flops while in the second one jk flip-flop are needed.

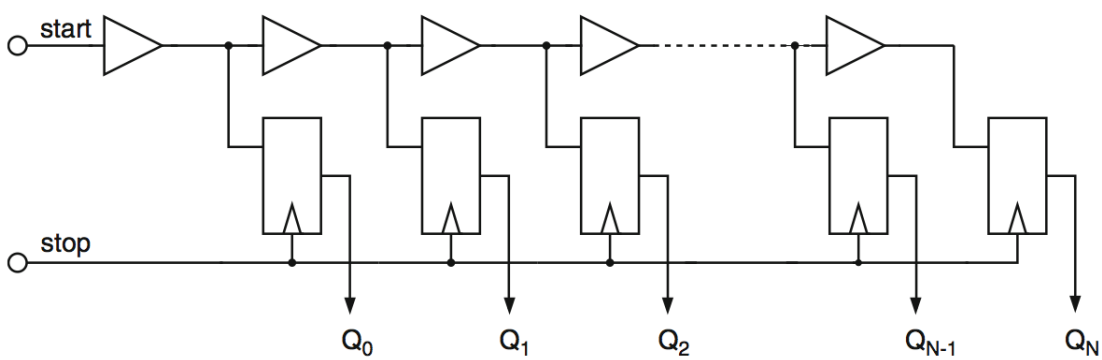

Figure 3.4: Digital Delay Line architecture

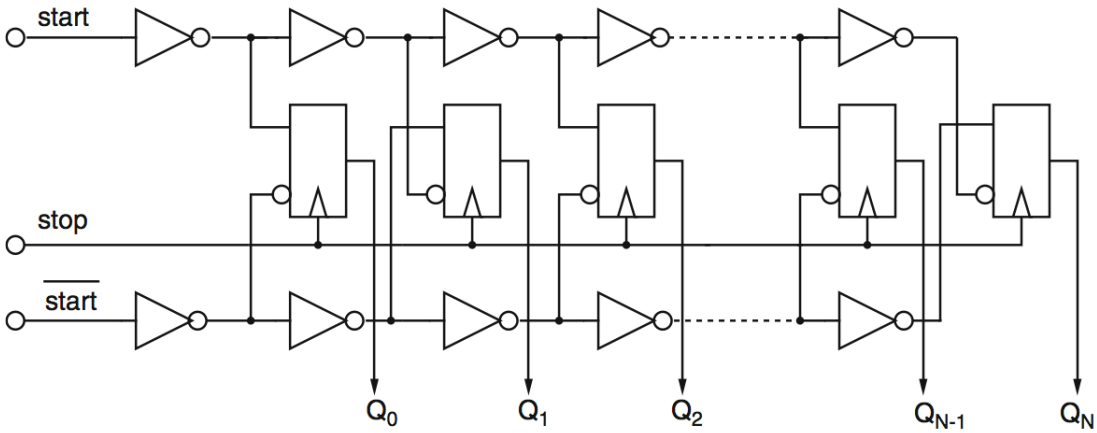

Figure 3.5: Inverter architecture

In the first structure, the start signal propagates in a buffer line and when the stop signal arrives, the value of the delay line is sampled. In the second case the start signal is sleeted and propagated in two coupled chains of inverter and at the stop signal the status of the inverter chains is sampled.

Comparing the two methods, we can notice that the Digital Delay Line resolution is equal to $T_{LSB} = t_{buffer} = 2t_{inverter}$, where t_{buffer} and $t_{inverter}$ are respectively the propagation delay of an inverter and a buffer stage. The resolution of the Inverter structure is $T_{LSB} = t_{inverter}$ so the resolution is double in the latter case. The drawback of the inverter base architecture is that it requires more elements to achieve the same DR of the Digital Delay. Another advantage of the Digital Delay structure is that it has a low power consumption ad it's easy to control.

3.3 TDC theory

To describe the TDC behavior it is necessary to considerate its characteristic obtained sending at the input a continuos variation of time intervals[14]. The response is a succession of step as we can see in figure

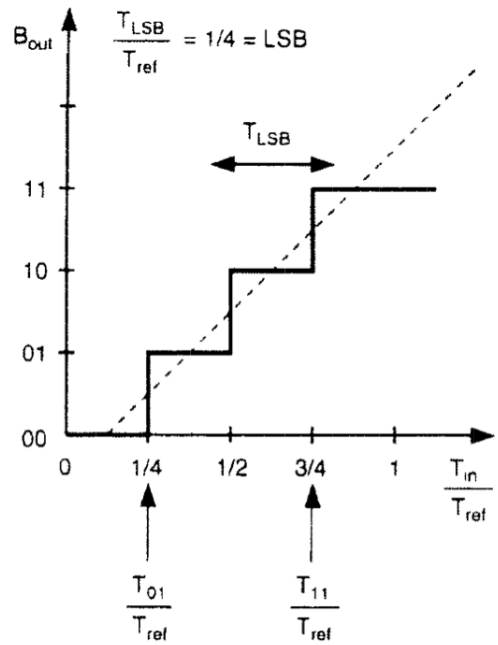

Figure 3.6: Output response of a general Time to Digital Converter

All the time intervals smaller the T_{LSB} produce the same output code. The characteristic can be described as follow:

$$T_{in} = B_{out}\, T_{LSB} + \varepsilon \tag{3.6}$$

where $\varepsilon \,\epsilon\, [0, T_{LSB})$ is the quantization error. In an ideal case this error is equally distributed and its contribution is only related to the noise of the baseline. However this is true only if the input signal changes fast and by an adequate amount.

As we can notice the TDC characteristic is very similar to the one of ADC except that the ADC input is a voltage variation and a zero mean quantization error because the quantization error is usually included within $-\frac{1}{2}\, V_{LSB}$ and $\frac{1}{2}\, V_{LSB}$. In the TDC the quantization error mean is:

$$< \varepsilon >= \frac{1}{T_{LSB}} \int_{0}^{T_{LSB}} \varepsilon \, d\varepsilon = \frac{1}{2} T_{LSB} \tag{3.7}$$

where the noise power spectrum is given by

$$< \varepsilon^2 >= \frac{1}{T_{LSB}} \int_{0}^{T_{LSB}} \varepsilon^2 \, d\varepsilon = \frac{1}{3} T_{LSB}^2 \tag{3.8}$$

The characteristic proposed above is ideal but in the reality there are two kinds of distortion: linear and not-linear.

3.3.1 TDC linear distortion

There are two types of linear distortion about the characteristic: offset error and gain error.

The offset error translates in the horizontal axis the first transition, which ideally show occurs at one LSB from the origin. All the transition point are shifted of the same amount. The offset error can be calculated as:

$$E_{off} = \frac{T_{00...01} - T_{LSB}}{T_{LSB}} \tag{3.9}$$

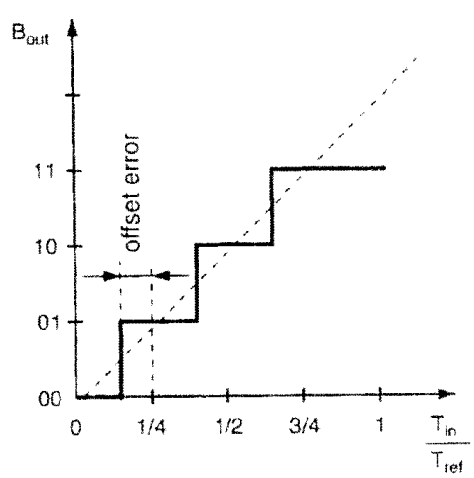

Figure 3.7: Characteristic of a TDC with a offset error

Mathematically we can define the gain as the characteristic slope

$$k_{TDC} = \frac{\triangle B}{\triangle T} \tag{3.10}$$

where delta B is the variation of the output code and the delta T is the variation of the input time and in the ideal case is equal to $\frac{1}{T_{LSB}}$. Therefore the gain error is the variation of the LSB from its ideal value, measured after the offset error has been corrected. We can define it as

$$E_{gain} = \frac{(T_{11..11} - T_{00...01})}{T_{LSB}} - (2^N - 2) \tag{3.11}$$

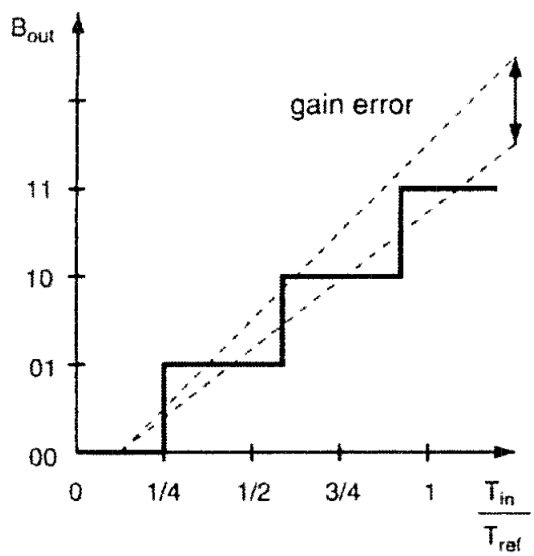

Figure 3.8: Characteristic of a TDC with a gain error

As we can see in the figure the gain error changes the slope of the characteristic, hence we can better define the gain using as following:

$$k_{TDC} = \frac{2^N - 2}{(2^N - 2)\,T_{LSB} + E_{gain}\,T_{LSB}} \approx \frac{1}{T_{LSB}} \left(1 - \frac{E_{gain}}{2^N - 2}\right) \tag{3.12}$$

These kinds of distortion are not a major concern, because they are linear imperfection and can be easily correctly with an appropriating calibration.

3.3.2 TDC not linear distortion

The non linear distortions modify the shape of output characteristic. The simplest one is the Integral Non-Linearity (INL). This is a macroscopic effect involving the bending of the TDC transfer curve. It is defined as the maximum variation between the true characteristic and the straight line interpolates the end points, as shown in the following figure:

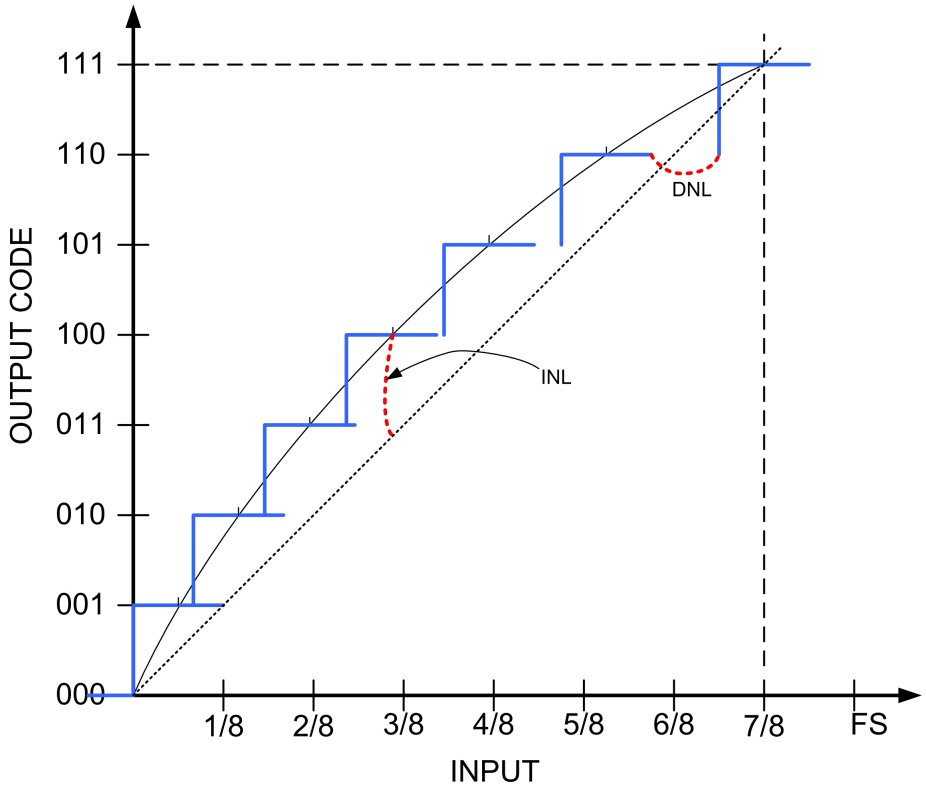

Figure 3.9: Representation of a characteristic with INL and DNL

The microscopic effect is given by the Differential Non-Linearity (DNL) which describes the variation of each step from its ideal value, normalized to the LSB.

The words Integral and Differential may lead to the belief that the first one is simply the sum of the other, but this is only true if the gain and offset errors have been corrected.

3.3.3 Noise contribution and characterization

An important parameter to discuss is the Signal to Noise Ratio (SNR) which is defined by the ten times the logarithm of the ratio between the signal power and the noise power. For any input sinusoid we have:

$$SNR = 10 \log \left(\frac{P_{signal}}{P_{noise}} \right) = (6.02\ N + 1.76)\, db \tag{3.13}$$

where N is the number of bit. It is also possible to take into account in the noise definition also harmonics, introducing a figure called SNDR (Signal to Noise and Distortions Ratio).

Though the SNDR it is possible to define the Effective Number Of Bits (ENOB), due to distortions or the noise or both. It's also possible that some codes are lost, giving one or more missing codes.I n this case the converter has a number of bits smaller then the nominal value. The ENOB is define as:

$$ENOB = \frac{max(SNDR) - 1.76\, db}{6.02\, db} \tag{3.14}$$

In principle we could use the same characterization technique developed for ADCs but this is not practical because it wood require to create an interval time sinusoid with a precision better then the one of the TDC. The alternative strategy is called Single Shot Experiment and consist in having a fixed time interval (T) which is repeatedly sent to the converter. Obviously this measure without noise wood always bee the same, but with noise this value changes. The standard deviation of this parameter is called Single Shot Precision (SSP) and it is the index of the reproducibility of the measure. Generally the SSP is dependent on the pulse length, because for a bigger signal the delay contribution of each elements is bigger.

To understand if there is some correlation between the measurement of two time intervals it is possible to use the double shot experiment, where two different time intervals are sent to the TDC. These time intervals are alternating and we can see that the lesser is the difference between the two time durations, the lesser is the contribution of the delay line and bigger is the correlation.

In addition the measure of the dynamic range is not trivial like the ADC so it is defined as the maximum time interval which we can measure without saturating the device.

Until this point we have not been concerned about the noise in the quantization error. We assumed that the quantization error, without noise, is equally

distributed between $-\frac{1}{2}T_{LSB}$ and $\frac{1}{2}T_{LSB}$. If we consider also the noise contributions, this interval is not so well defined. If we consider a specific time interval T we can define through a Gaussian distribution the delay deviation τ from the effective value T as:

$$p_\tau(\tau) = \frac{1}{\sqrt{2\,\pi}\,\sigma_\tau}\, e^{-\frac{\tau^2}{2\,\sigma_\tau^2}} \tag{3.15}$$

If we call k the nominal value of the interval measure T without noise, $T - k\,T_{LSB}$ is the position within the quantization error. Its probability density with the noise induced by τ is defined as:

$$p(T - k\,T_{LSB}, \tau) = \frac{1}{T_{LSB}}\,\frac{1}{\sqrt{2\,\pi}\,\sigma_\tau}\, e^{-\frac{\tau^2}{2\,\sigma_\tau^2}} \tag{3.16}$$

The quantization error instead can be described as:

$$\varepsilon(T - k\,T_{LSB}, \tau) = \sum_{n=-\infty}^{\infty} T - k\,T_{LSB} + n\,T_{LSB} \tag{3.17}$$

with

$$\left(-\frac{1}{2}\,T_{LSB} - n\,T_{LSB}\right) \leq T - k\,T_{LSB} < \left(\frac{1}{2}\,T_{LSB} - n\,T_{LSB}\right) \tag{3.18}$$

so it is now possible to define the noise power taking into account the physical condition:

$$< \varepsilon^2 >= \int_{-\frac{1}{2}T_{LSB}}^{\frac{1}{2}T_{LSB}} \int_{-\infty}^{\infty} \varepsilon^2(T - k\,T_{LSB}, \tau)\; p(T - k\,T_{LSB}, \tau)\, d\tau\, d(T - k\,T_{LSB}) \tag{3.19}$$

which using one variable change form $T - k\,T_{LSB}$ to T' we obtain:

$$\frac{1}{\sqrt{2\,\pi}\,\sigma_\tau\,T_{LSB}} \int\limits_{-\frac{1}{2}T_{LSB}}^{\frac{1}{2}T_{LSB}} \sum_{n=-\infty}^{\infty} (T' - n\,T_{LSB})^2 \int\limits_{\left(n-\frac{1}{2}\right)T_{LSB}-T'}^{\left(n+\frac{1}{2}\right)T_{LSB}-T'} e^{-\frac{\tau^2}{2\,\sigma_\tau^2}}\,d\tau\,dT' \;=\; \tag{3.20}$$

$$= \frac{1}{T_{LSB}} \int\limits_{-\frac{1}{2}T_{LSB}}^{\frac{1}{2}T_{LSB}} \sum_{n=-\infty}^{\infty} (T' - n\,T_{LSB})^2 \left\{ \frac{1}{2}\,erf\left[\frac{\left(n+\frac{1}{2}\right)\,T_{LSB} - T'}{\sqrt{2}\,\sigma_\tau}\right] - \frac{1}{2}\,erf\left[\frac{\left(n-\frac{1}{2}\right)\,T_{LSB} - T'}{\sqrt{2}\,\sigma_\tau}\right] \right\} dT' = \tag{3.21}$$

$$= \frac{1}{T_{LSB}} \sum_{n=-\infty}^{\infty} \int\limits_{-\frac{1}{2}T_{LSB}}^{\frac{1}{2}T_{LSB}} (T' - n\,T_{LSB})^2\,p_n(T')\,dT' \tag{3.22}$$

For a nominal quantization error T' the probability density function $p_n(T')$ describes the probability that the measure result is $k + n$. In the following figure there is the error quantization probability density function for some σ_τ value, we can see as if the sigma converges to zero the quantization function is confined in the interval $\left[-\frac{1}{2}T_{LSB}, \frac{1}{2}T_{LSB}\right]$

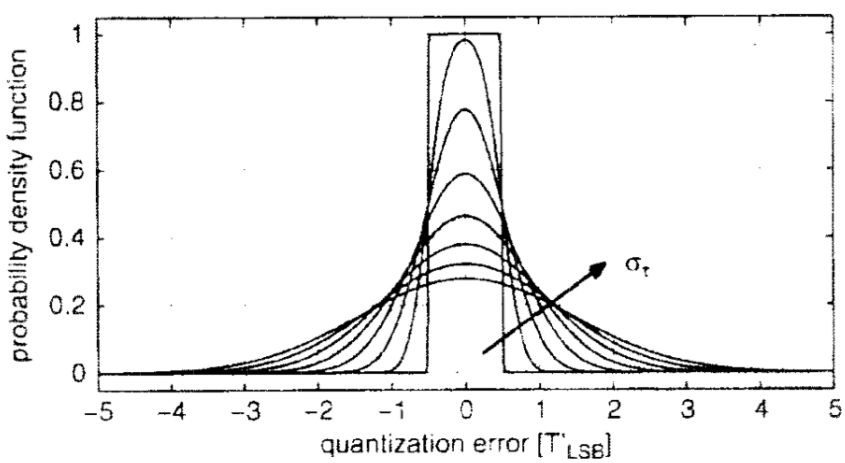

Figure 3.10: curves at different σ_τ

The quantization noise power spectrum without physical noise is given by the $<\eta>^2 = \frac{T_{LSB}^2}{12}$ equation. This ideal value can be separated from the power noise spectrum in the following way:

$$= \frac{T_{LSB}^2}{12} \frac{12}{T_{LSB}^3} \sum_{n=-\infty}^{\infty} \int_{-\frac{1}{2}T_{LSB}}^{\frac{1}{2}T_{LSB}} (T' - n\,T_{LSB})^2\, p_n(T')\, dT' = \frac{(T_{LSB}\, RDC)^2}{12} \tag{3.23}$$

where the Resolution Degradation Coefficient (RDC)

$$RDC = \sqrt{\frac{12}{T_{LSB}^3} \sum_{n=-\infty}^{\infty} \int_{-\frac{1}{2}T_{LSB}}^{\frac{1}{2}T_{LSB}} (T' - n\,T_{LSB})^2\, p_n(T')\, dT'} \tag{3.24}$$

is the index for the increasing of the T_{LSB} due to the physical noise. We can, also, redefine the ENOB as:

$$ENOB_{TDC} = log_2\left(\frac{DR}{T_{LSB}\, RDC}\right) = M - log_2(RDC) \tag{3.25}$$

where M is the ideal resolution. In addition we can defined two figure of merits for a TDC relating the speed, the number of bits and the area or power of the device:

$$FOM_P = \frac{<P>}{f\, 2^{ENOB}} \tag{3.26}$$

$$FOM_A = \frac{<A>}{f\, 2^{ENOB}} \tag{3.27}$$

3.4 Process Variations in TDCs

During the production of any chip, the characteristic can not be exactly reproduced. This is easy to understand thinking that the a lot of performance depend on the silicon doping of each transistor, that has a statistical behavior. Another important part is made by the voltage supply and the temperature variation.

These variations involve a variation of the gate delay in the delay line and in the buffer tree of the stop signal and so influence the TDC offset, the gain and the resolution. As mentioned before the offset error is not a problem but if the gain changes this is a major problem, so the gain must be accurately controlled and eventually calibrated. This calibration can be made by a digital calibration through a dynamically characterization measuring a known reference time interval T_R. If the TDC is linear the input and the output are related by

$$B = [k\,T] + B_{offset} \tag{3.28}$$

where B is the digital output, T is the time interval, k is the TDC gain and B_{offset} is the digital word when $T = 0$. To do this analysis one measure is not sufficient because in principle we don't know both the gain and the offset, so it is necessary to use two measures. In general if we measure T_1 and T_2 we can find the B_{offset} as following since the gain it canceled:

$$\frac{T_1}{T_2} = \frac{B_1 - B_{offset}}{B_2 - B_{offset}} \tag{3.29}$$

3.4.1 Local process variations on Delay-Line

These variations entails a modification of the delay of each gate so the delay line can be modeled by $T_{d,i} = T_{LSB} + \varepsilon_i$ where ε_i is the delay error. Usually this error, which can be positive or negative, is modeled as a Gaussian process with zero mean, but for this case this kind of approach does not appears to be correct, because if ε_i becomes smaller than $-T_{LSB}$, the delay becomes negative. However for our discussion isn't necessary to have a specific distribution structure but is sufficient to have a mean free distribution. So we can write

$$t_n = \sum_{i=1}^{n} t_{d,i} = n\,T_{LSB} + \sum_{i=1}^{n} \varepsilon_i \tag{3.30}$$

and the standard deviation, if $std(\varepsilon_i) = std(\varepsilon)$ is given by:

$$std(t_n) = std(\varepsilon)\sqrt{n} \tag{3.31}$$

Throughout this definition of the delay error we can rigorously define the DNL and the INL:

$$DNL_n = \frac{t_{n+1} - t_n - T_{LSB}}{T_{LSB}} = \frac{\varepsilon_{n+1}}{T_{LSB}} \tag{3.32}$$

if the delay line is composed by N delay elements we have $t_N = N\,T_{LSB} + \sum_{i=1}^{N}\varepsilon_i$ and so we can redefine the gain error as:

$$E_{gain} = \frac{1}{T_{LSB}}\,(t - t_1) - N + 1 = \sum_{i=2}^{N}\varepsilon_i \tag{3.33}$$

To define the INL we need to fix the reference step positions as:

$$t_n^{'} = t_1 + \frac{n-1}{N-1}(t_N - t_1) \tag{3.34}$$

and so the INL becomes:

$$INL_n = \frac{1}{T_{LSB}}(t_n - t_n^{'}) \tag{3.35}$$

and using all the above formulas, we have:

$$t_n - t_n^{'} = n\,T_{LSB} + \sum_{i=1}^{n}\varepsilon_i - t_1 - \frac{n-1}{N-1}\left(N\,T_{LSB} + \sum_{i=1}^{n}\varepsilon_i + \sum_{i=n+1}^{N}\varepsilon_i\right) + \frac{n-1}{N-1}\,t_1 = \tag{3.36}$$

$$= T_{LSB}\left[n - \frac{N(n-1)}{N-1}\right] + \sum_{i=1}^{n}\varepsilon_i\left[1 - \frac{n-1}{N-1}\right] - t_1\left[1 - \frac{n-1}{N-1}\right] - \left(\frac{n-1}{N-1}\right)\sum_{i=n+1}^{N}\varepsilon_i = \tag{3.37}$$

$$= \left(\frac{N-n}{N-1}\right)\left[T_{LSB} + \sum_{i=1}^{n}\varepsilon_i - t_1\right] - \left(\frac{n-1}{N-1}\right)\sum_{i=n+1}^{N}\varepsilon_i = \tag{3.38}$$

$$= \sum_{i=2}^{n}\varepsilon_i\left[1 - \frac{n-1}{N-1}\right] - \left(\frac{n-1}{N-1}\right)\sum_{i=n+1}^{N}\varepsilon_i \tag{3.39}$$

so we can conclude that the INL is given by:

$$INL_n = \frac{1}{T_{LSB}}\left\{\sum_{i=2}^{n}\varepsilon_i\left[1 - \frac{n-1}{N-1}\right] - \left(\frac{n-1}{N-1}\right)\sum_{i=n+1}^{N}\varepsilon_i\right\} \tag{3.40}$$

For a better understanding this formula is useful to calculate the standard deviation that is:

$$std(INL_n) = \frac{std(\varepsilon)}{T_{LSB}}\sqrt{(n-1)\frac{N-n}{N-1}} \tag{3.41}$$

and the maximum is achieved when:

$$n = \frac{1}{2}(N+1) \tag{3.42}$$

and it is proportional to the square of the number of elements since:

$$max(std(INL_n)) = \frac{std(\varepsilon)}{2\,T_{LSB}}\sqrt{N-1} \tag{3.43}$$

so a good linearity can be achieved without calibration only if the chain is short.

3.5 Other TDC architectures

3.5.1 Analog TDC

The most simple analog TDC is shown in the Figure 3.11:

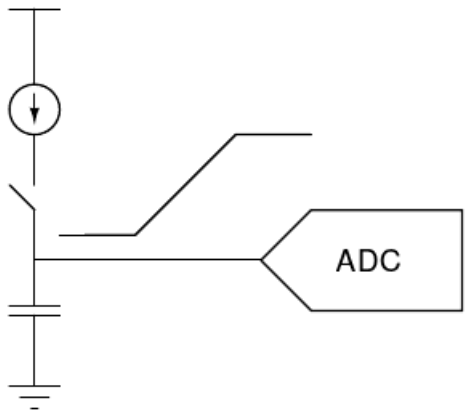

Figure 3.11: Principle of Analog TDC

It is composed by a constant current source, a switch, a capacitor and an ADC. The time information which we want to convert is given by the time during the switch stays closed. In particular in the start configuration we have a voltage value in the capacitance node called baseline. When we close the switch the constant current charges the capacitance and its voltage value rises up. If we now open the switch again a new voltage value is hold in the capacitance node and we have converted the time information from the time domain to the analog domain. Now with the ADC we converted the analog information given by the difference between the new voltage value and the baseline value, so the time information is finally in the digital domain.

3.5.2 Bipolar Digital TDC

In most cases the TDC measures just positive time intervals since the start signal comes before the stop signal so the TDC structure is an asymmetrical one. But in some cases it is necessary to measure the difference between two signals which doesn't have a precise chronological order. In this case a conventional TDC measures an interval time equal to zero.

To do this measurement we can skew the stop time so, if the difference between the start and stop signal is zero or slightly negative, the stop signal becomes the second one which the TDC receives. This technique is not a good solution because it introduces an unknown offset error and is more sensitive to process variations and operating conditions. Furthermore the skew elements give some problems because to implements this structure extra area and power are required increasing the uncertainty of the SSP.

The structure that we can use is similar to that shown in Figure 3.12.

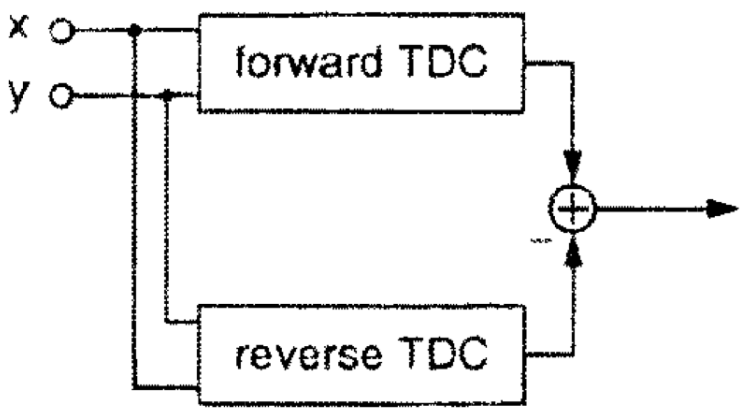

Figure 3.12: Block diagram of the simples Bipolar TDC

This architecture consists of two conventional TDCs. The first is called Forward TDC and its task is to measure the differences between the signal x and the signal y. The second device is called Reverse TDC and its task is to measure the differences between the signal y and the signal x. Since this are traditional TDCs, if the first signal arrives after the second one (x signal for the Forward TDC and y signal for the Reverse TDC) the time measure is zero, this involves that neither TDCs has to measure negative input. To obtain the true time information it is necessary to subtract the output in particular the Forward output minus the Reverse output, the complete architecture is shown below.

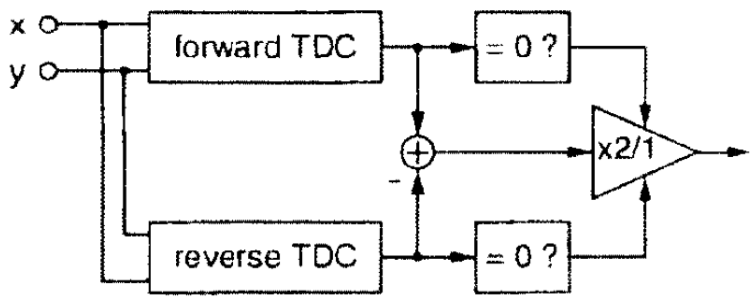

Figure 3.13: Block diagram of the final Bipolar TDC

We can notice that around $\triangle t = 0$ the gain is double because this region is the overlap region so each TDCs give a result, this situation compromise the linearity but in many cases it is not a problem.

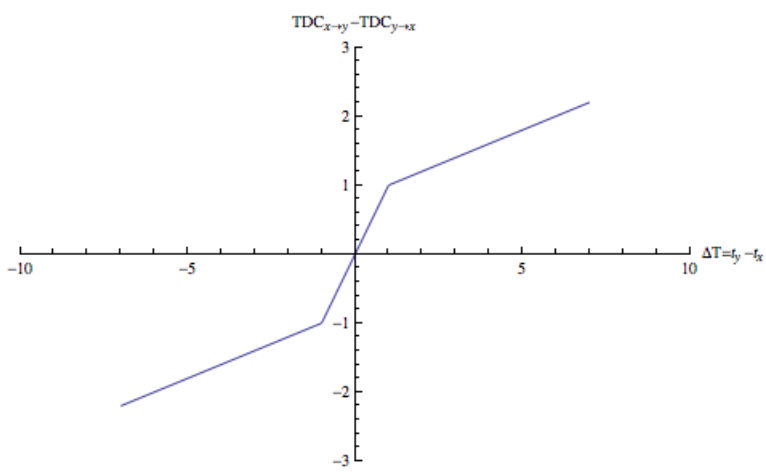

Figure 3.14: Block diagram of the final Bipolar TDC

3.5.3 Looped Digital TDC

Until now we have study only a linear TDC , for this kind of TDC the length and so the area grows with the maximum time interval to be measured. In the Looped TDC the delay line is short and the signal goes inside it many times. We can see an example of the looped TDC in the following figure

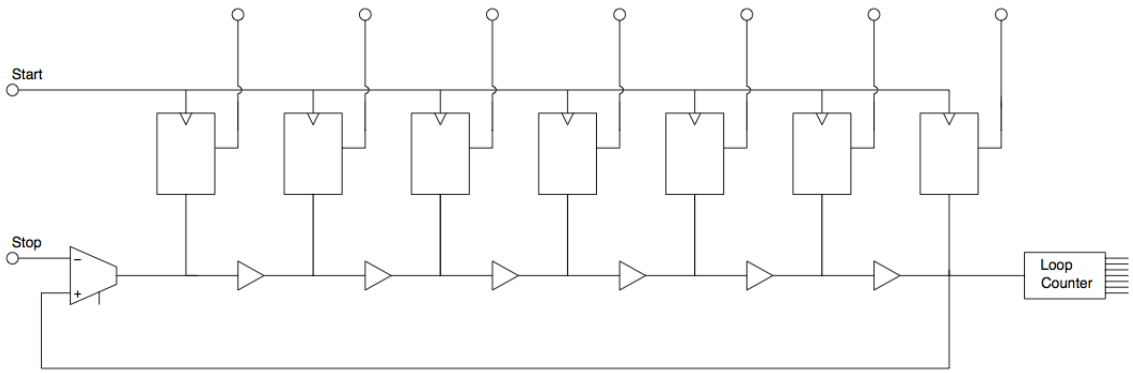

Figure 3.15: Loop architecture

As we can see above there is a counter which counts how many times the signal passes through the end of the chain before the stop signal comes[13]. We can indicate the value B_{cnt} as the coarse time value and the fine time value is given by the delay line value, so if we have M delay elements the complete words we can obtain as:

$$B = M\, B_{cnt} + B_{TDC} \tag{3.44}$$

The time measurements takes place in the following way: first an external control enables the multiplexer to send the start signal to delay line. So the signal passes trough the delay line and when it comes to the end of the delay line the counter increases its value and the signal is reported at the starting multiplexer. This process goes on until the stop signal arrives. This signal enables the flip-flop chain and the delay line status is sampled, and the TDC is now ready to the next measurement. The most critical part in this process is when the stop time comes,

because the stop time and the time event in the loop are asynchronous and it is not easily detected which is the precise status of the loop chain when this signal arrives.

As told above one of the advantages is the low area consumption but it is not the only one. An additional benefit is the reduction of the time uncertainty because it increases with the increasing of the chain length. Having a short delay line implies that only few local variations can accumulate so it is easier to achieved a high dynamic range. However the linearity can be easier compromised because it is very difficult to switch the delay line to a close loop maintaining the symmetry and also the input multiplexer gives another non-linearity.

Whit this architecture in principle it's possible to measure an arbitrary long time interval, but, in practice, the asymmetry gives the parasitic pulse shrinking effect that shortens the time interval until it completely vanishes. This effect give us the limit on the maximum measurement interval.

3.5.4 Hierarchical Digital TDC

The particularity of this structure is that it doesn't measure the complete time interval with the full resolution, with consequent low power consumpion. This involves that the long time interval can be measured, an example of this structure is show in the following figure:

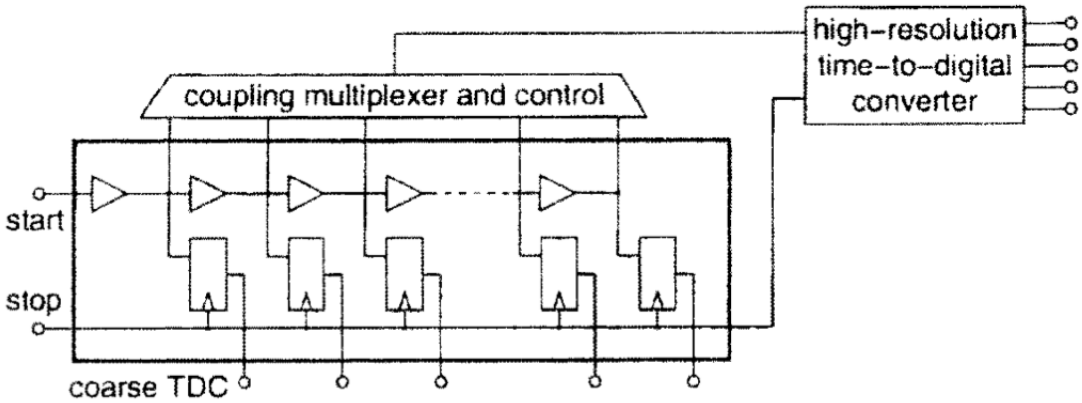

Figure 3.16: Simples Hierarchical TDC architecture

This architecture consist of two levels[5, 3]. In the first one uses a coarse TDC that has the task to make a first coarse conversion, while the second one is used to minimize the quantization error. The second TDC has a high resolution but

a small dynamic range which coincides with the less significant bit of the coarse TDC. This architecture is useful to measure long time intervals with a good resolution and a low power and area consumption, because the first TDC has a big dynamic range but low resolution and the second one has a low dynamic range but high resolution. The problem of this architecture is given by the coupled logic, which is composed by a large multiplexer and it is difficult to to implement.

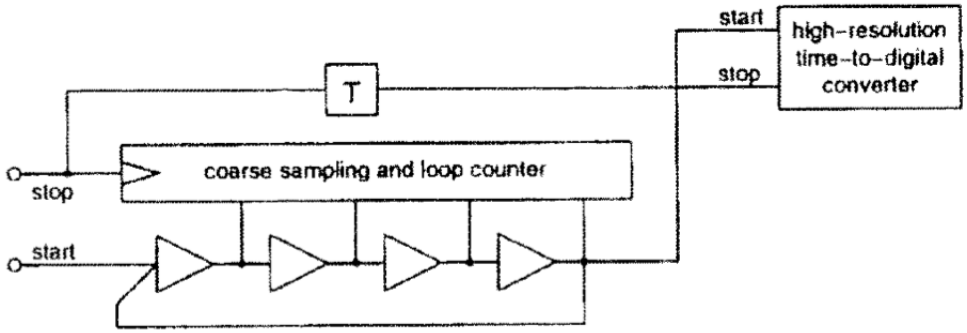

Figure 3.17: Hierarchical structure without multiplexer

The first level, as we can see in the figure above, consist of a short delay line which achieves big dynamic range because has a feedback and so we can recognize the loop structure. The delay line is coupled with the second stage and the signal time is injected periodically into the fine TDC, when the stop signal arrives both the coarse and the fine line are sampled. This structure has a good linearity but the power consumption is high so we can easily understand that is not the best configuration.

The largest power consumption is due to the fine stage receiving the time signal to convert, each time this one reaches the end of the delay line. To avoid this waste of power the configuration can be modifier as show in the following figure:

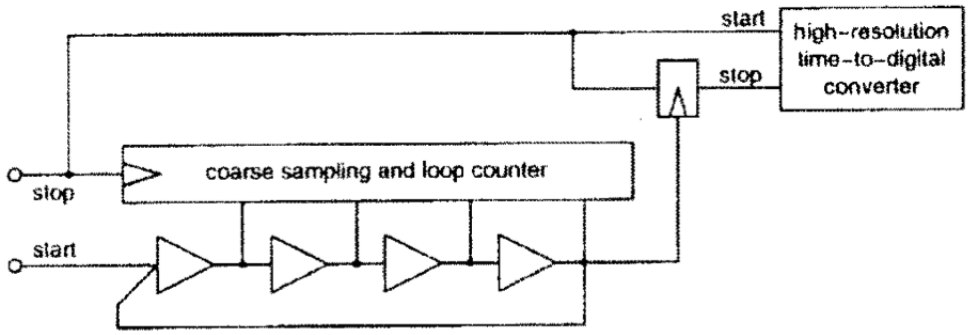

Figure 3.18: Hierarchical structure with low power consumption

Now the fine TDC measures only one time interval and not every cycles, so the power consumpion is considerably reduced, but there is another problem: the area consumption. To reduce the used area and get a symmetrical layout it is useful to connect each delay elements with the coupled stage which now is a multiplexer and use a counter to count the cycles as follows:

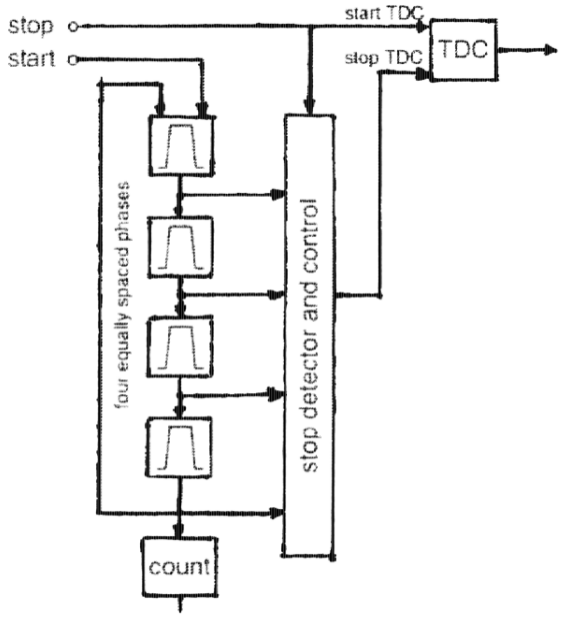

Figure 3.19: Hierarchical structure with a low power and low area consumption

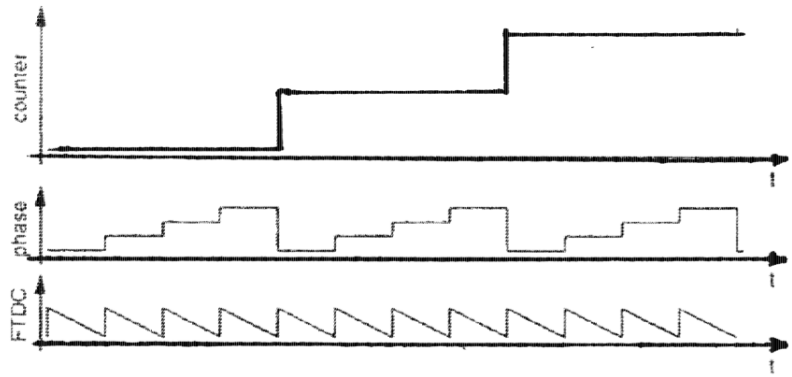

Figure 3.20: Characteristics of a hierarchical structure

The output world of the hierarchical TDC is define as following:

$$B_{out} = B_{cnt} + \frac{1}{4}\,B_{phase} + \left(\frac{1}{4} - \frac{1}{4}\,k\,B_{FTDC}\right) \tag{3.45}$$

where B_{cnt} is the counter value, B_{phase} is the phase in the delay line when the stop signal comes, B_{FTDC} is the value of the fine TDC and k is the calibration coefficient of the first and second stage.

3.6 TDC choice

Until now we have been describing different kinds of architecture, each of them is optimized for a particular performance figure. For example the bipolar structure is useful if we want minimize the offset error, the loop structure is used to measure medium time interval and so on. But there isn't a single structure that can be optimized for all applications, each one have some drawbacks as show in figure.

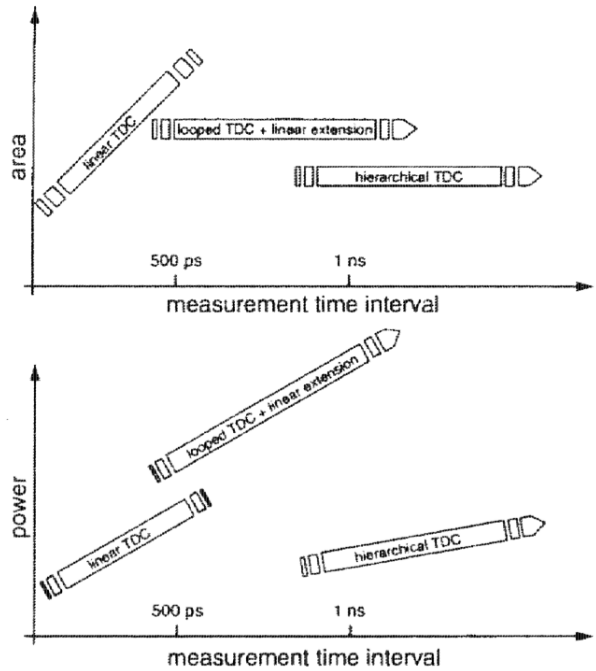

Figure 3.21: Representation of the different kinds of TDC

For the microstrip detector of the $\overline{P}$ANDA MVD moderate resolutions and speed are required, while area and power consumptions are important therefore the ANALOG TDC based on time to amplitude converter has been chosen as a starting point. The requrements of the Front-end and the TDC are:

- $C_{det} = 20\,pF$
- Rate per channel ~ 30 KHz
- Power consumption ~ 4 mW per channel
- The circuit must be triggerless
- Preserve the charge information
- We want only digital output

Chapter 4

TDC Implementation

In the previous chapters we have seen that a TDC is needed in order to carry out Time Over Threshold measurements in $\overline{P}$ANDA with a sufficient time resolution and speed. We have also seen that Time to Digital Converters based on analog Time to Amplitude interpolators offers a good compromise between power consumption, area and speed. Therefore this topology has been chosen as baseline for the feasibility studies of the strip front-end. In this chapter we describe the architecture of the TDC and the most relevant design issues.

4.1 TDC architecture

To obtain the time information we use two different resolutions, the coarse one and the fine one. The coarse resolution is given by the clock period which is bound with a counter called TIME STAMP, which is the reference time throughout the whole experiment. The fine resolution is given by the TDC, which measure the difference between the ToT edges and the following clock positive edge as we can see in Figure 4.1

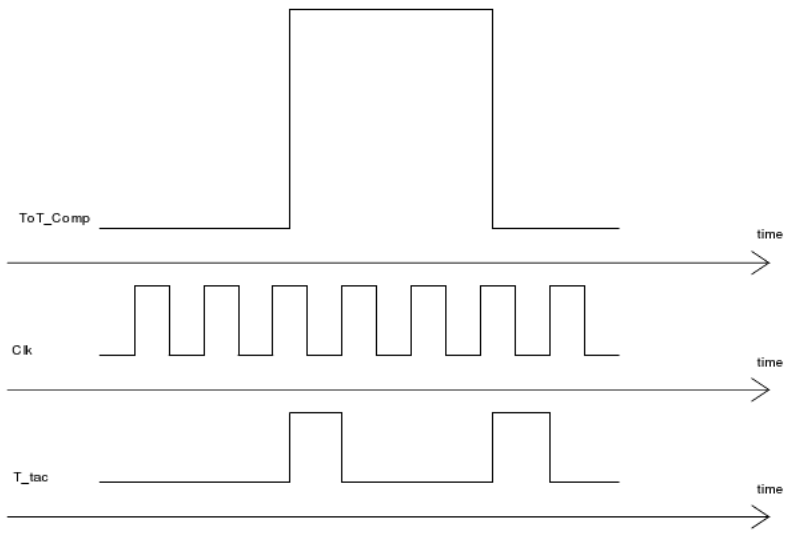

Figure 4.1: Time evolution of the signal

The time between the signal and the nearest clock edge is interpolated by connecting a current source to a capacitor, the analog value resulting is then digitized by a Wilkinson ADC. To measure the ToT, the leading and trailing edges of the comparator are measured independently respect to the clock signal. This has two advantages when compared to the direct measurement of the duration of the comparator signal. On one hand, the time that the TDC has to interpolate is shorter, thus reducing the dynamic range required to the TDC. On the other hand there is no strong constrain put by the TDC on the maximum interval which can be measured in this way. Since the final ASIC will incorporate at least 64 channels, only one global counter will be used. The counter output is Gray encoded and distributed to all the channels. When a hit is detected in one channel the comparator fires triggering the latching of the counter word into local registers task providing the first coarse time measurement.

Since an Analog TDC is a fairly slow block, two TDCs per channel are needed: one to capture the leading edge and another one to measure the trailing edge. As shown in Figure 4.2.

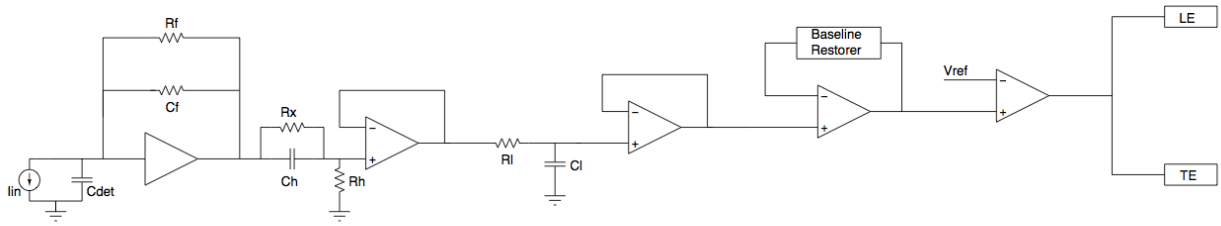

Figure 4.2: Complete schematic

To do this kind of TDC there are many ways, we chose the following architecture because it is the best solution in our case and it was already implemented in another technology and for another field, in particular the medical one[8, 12]. So we study this architecture and we modify it to achieved our tasks. The analog interpolator is formed by three building blocks, the Currents generator, the Time to Amplitude Converter (TAC) and the Analog to Digital Converter (ADC).

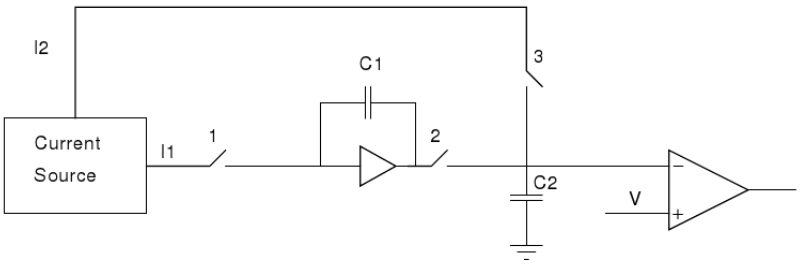

Figure 4.3: TDC building blocks before the measure

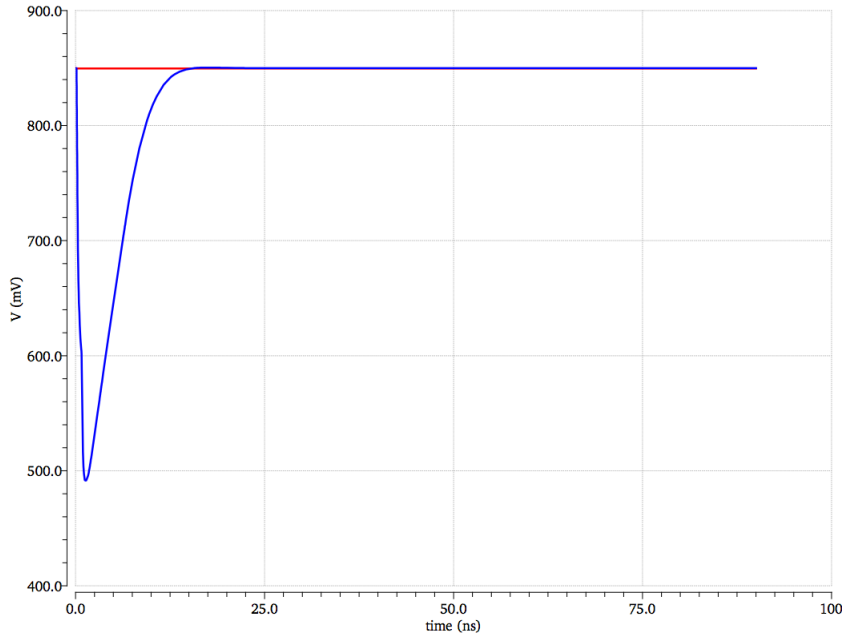

Figure 4.4: The TAC output signal and the comparator input signal

As we can see in Figure 4.4 there are 2 signals, the blue one is the TAC output and the red one is the latch comparator input. If we send a reset signal to the TAC its output falls down and reaches the baseline value in less than $20ns$. To understand how this circuit works we can see the following figures

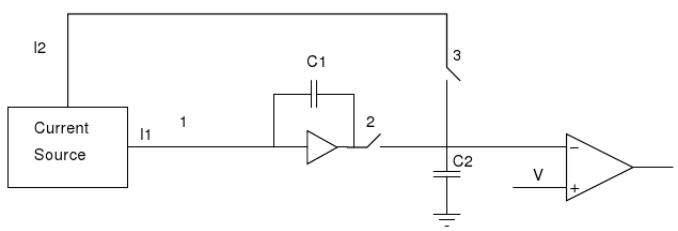

Figure 4.3: TDC building blocks at the start of the measure

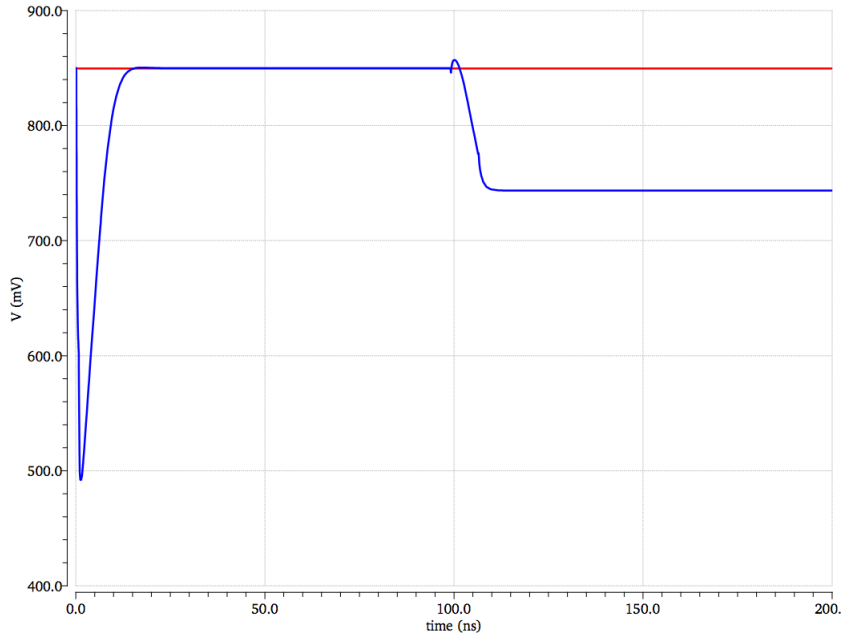

Figure 4.4: The TAC output signal and the comparator input signal

After the reset signal has been sent, we close the switch number 1 and the TAC output fall down since the constant current I_1 discharges the capacitance C_1. When we open again the switch number 1 we can see that the new TAC voltage value is hold.

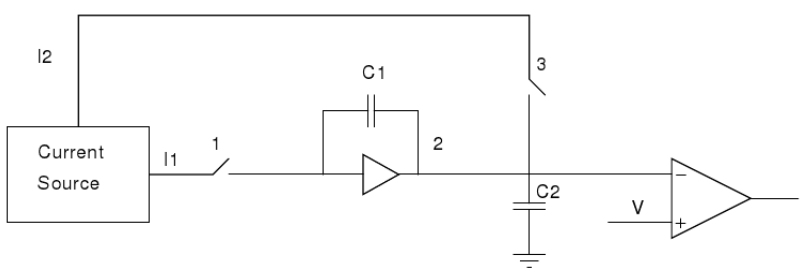

Figure 4.5: TDC building blocks at the middle phase

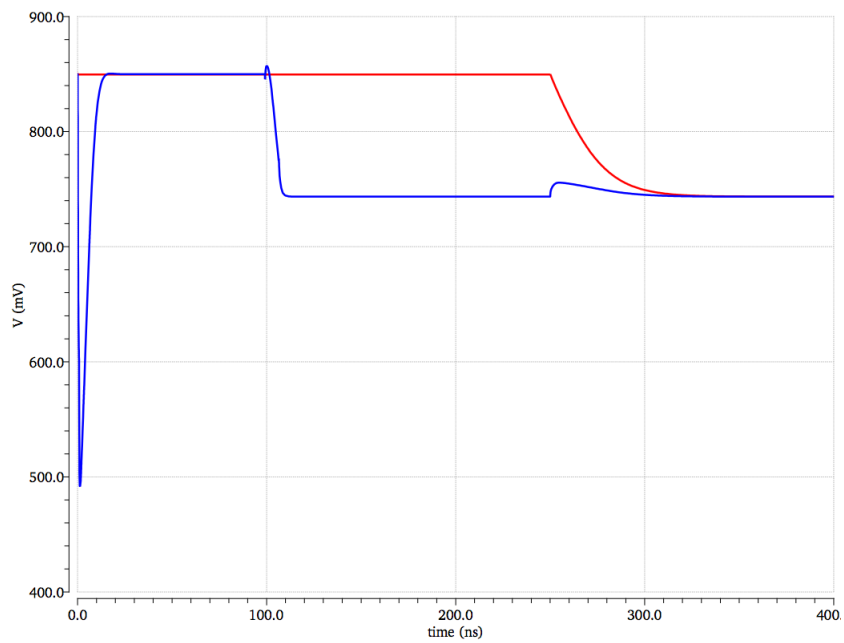

Figure 4.6: The TAC output signal and the comparator input signal

If we now close the switch number 2 the TAC amplifier drives capacitance C_2 to its output voltage. We can notice that signals reaches a stable value value in about $100ns$. Now we can convert the analog time information opening the switch 2 and closing the switch 3. The current i_2 recharges the capacitance C_2 until the baseline voltage is reach.

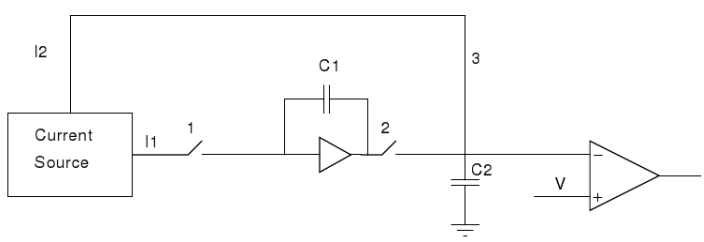

Figure 4.7: TDC building blocks at the conversion through the ADC

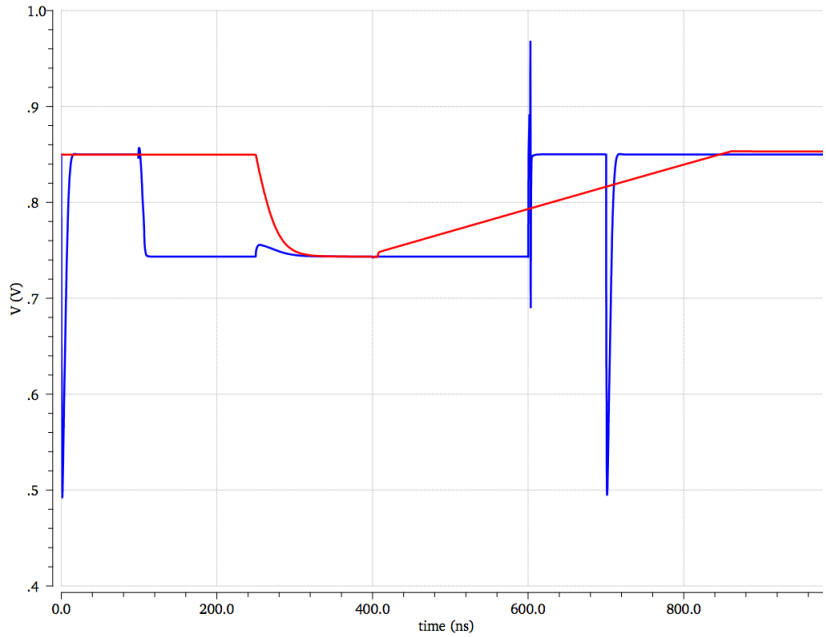

Figure 4.8: The TAC output signal and the comparator input signal

We can also see that if we send a reset signal to the TAC, the ramp is not affected because the two circuits are completely insulated. We can notice that the recharging ramp is longer than the discharging one. Indeed $C_2 = 4\,C_1$ and $i_1 = 32\,i_2$ then, as anticipated, the resolution is $\frac{6.24ns}{32 \cdot 4} = 48.75ps$.

There is a problem which we haven't considered yet. If the comparator output changes near the positive clock edge, the switch number 1 could remain closed for a very short time. So when we convert this information, the error that we have is not negligible anymore because there is a charge injection in the capacitance given by the switch and the signal is too small to be distinguished. To avoid this problem the switch number 1 closes when the comparator signal comes and opens again on the first positive clock transition following a negative one. In this way an offset of half a clock cycle is introduced, avoiding that the current source is connected to the capacitance for a too short time.

4.2 Current generator

This block generates the two currents and since the ratio of these currents is an important parameter for the conversion, it must be very accurately designed[11]. The simplest structure that we could consider as a current source is the current mirror that we can see in Figure 4.9:

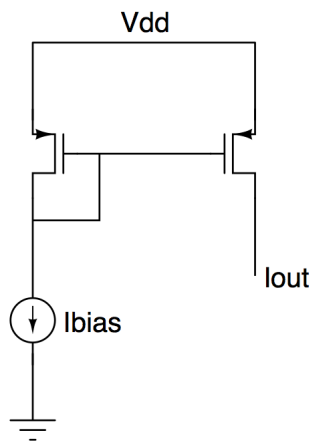

Figure 4.9: Current mirror

Since the transistor current is $I_{DS} = \frac{1}{2}\,\mu_p\,C_{ox}\,\frac{W}{L}\,(V_{SG} - V_{th})^2\,(1 + \lambda\,V_{SD})$, and the sources and gates have the same voltage for construction, the ratio between the two currents depends exclusively on the transistors dimensions. This is a good current source because if the transistors are in the saturation region the current has a weak dependence on V_{SD}. In this applications the matching between the charging and discharging currents has primary importance. Therefore to scale the currents, just one fundamental unit is used and bigger currents are obtained by connecting a suitable number of these units in parallel.

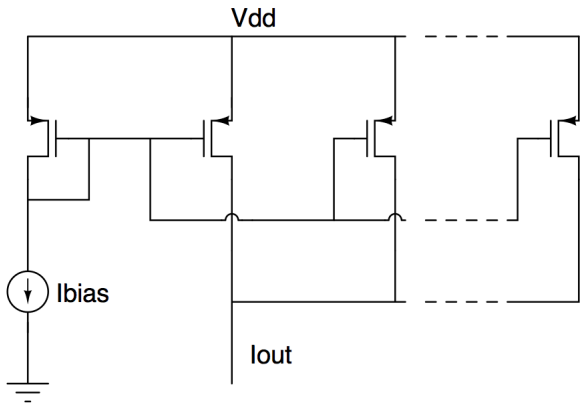

Figure 4.10: Parallel current mirrors to achieved a big current

Another important parameter of an ideal current generator is the output resistance value, which must be as high as possible. For this reason a triple cascode configuration is used. To calculate the output resistance we use the following configuration:

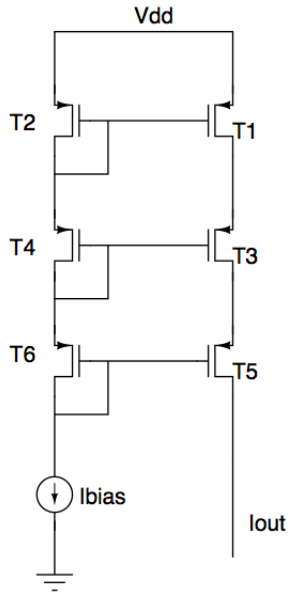

Figure 4.11: Parallel current mirrors to achieved a big current

For the sake of simplicity we use just one branch and the small signal model becomes:

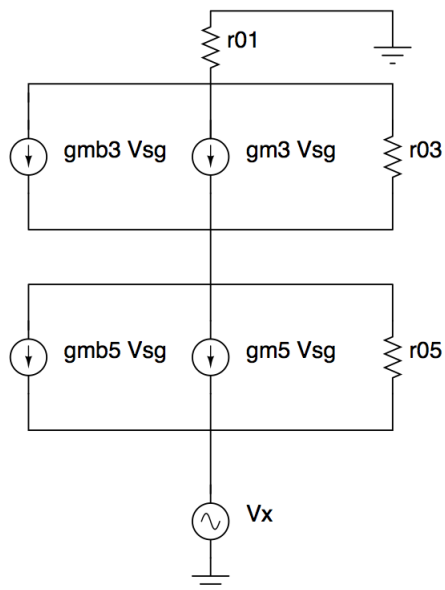

Figure 4.11: Small signal model of the one branch of above current mirror

the resulting equations are:

$$\begin{cases} g_{m3}\, v_{s3} + g_{mb3}\, v_{s3} + \frac{v_{s3}}{r_{01}} + \frac{v_{s3}-v_{s5}}{r_{03}} = 0 \\ -g_{m3}\, v_{s3} - g_{mb3}\, v_{s3} - \frac{v_{s3}-v_{s5}}{r_{03}} + g_{m5}\, v_{s5} + g_{mb5}\, v_{s5} + \frac{v_{s5}-v_X}{r_{05}} = 0 \\ -g_{m5}\, v_{s5} - g_{mb5}\, v_{s5} - \frac{v_{s5}-v_X}{r_{05}} - i_X = 0 \end{cases} \tag{4.1}$$

the resulting output resistance is:

$$\frac{v_X}{i_X} = R_x = r_{05} \left\{ 1 + \frac{[r_{03} + r_{01} + (g_{m3} + g_{mb3}) r_{01}\, r_{03}] \cdot [1 + (g_{m5} + g_{mb5}) r_{05}]}{r_{05}} \right\} \tag{4.2}$$

If we consider that the output resistance of the individual transistors, as well as their transconductance, is with each other comparable, and we assume that the $g_m\, r \gg 1$, the resistance becomes:

$$R_X \backsim \left(r^2 g_m\right)^2 \backsim 10^8 \tag{4.3}$$

so this resistance becomes is very high and comparable to infinite. Practically, phenomena like weak avalanche may limit the output resistance to substantially low values. Therefore it is important to carefully evaluate the output resistance in computer simulations.

As we can see in the complete TDC picture the currents generator provides both currents i_1 and i_2. This because the ratio between these two currents is more important for it defines the gain of the TDC. However the current ratio is much sensitive than the capacitance one, so is a very good choice to generate each current in the same building block. Therefore, given a current bias, the structure can be the one shown in Figure 4.12:

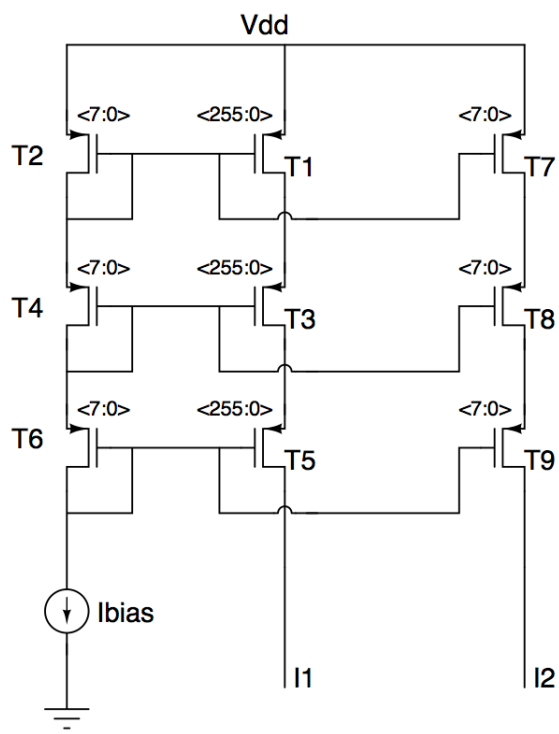

Figure 4.12: Basic current generator

The transistors that provides the current i_1 don't have the width 32 times bigger than the one of the transistors which deliver i_2 but, as written above, they are made by connecting in parallel 32 equal devices. However mismatch arising in the fabrication process can significantly modify this ratio. For this reason, we used the structure shown in the Figure 4.13. The number of transistors connected in parallel can be programmed, so that the desired current ratio can be achieved even if the matching is not perfect.

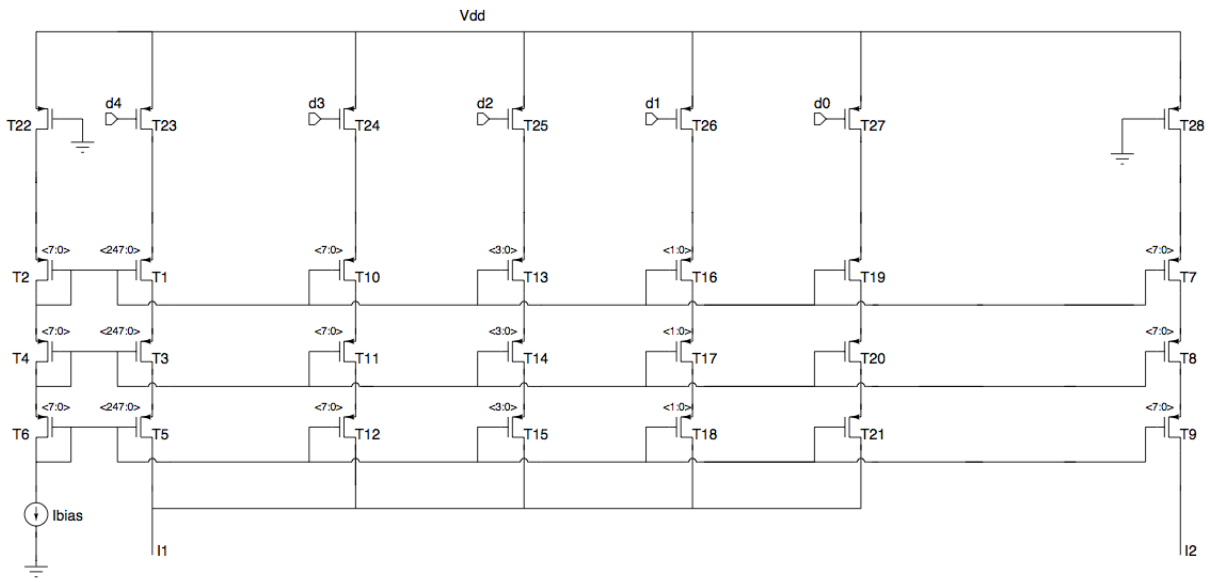

Figure 4.13: Current generator with a tuning

It were added four new branches, these ones having different multiplicity, to tune the ratio. Also the i_1 branch changes multiplicity, now is just 31 times the I_{bias} branch. In fact the new first branch has multiplicity 1, the second has multiplicity 0.5, the third 0.25 and the fourth 0.125.

We can also see that we used another transistor line, the p-switch, useful for choosing which tuning branch we want to use. The last element inserted is the capacitance network which task is to filter the noise, as we can se in Figure 4.14, the upper network is the most important one because it couples the voltage power supply variation with the ground one in order to fix this difference.

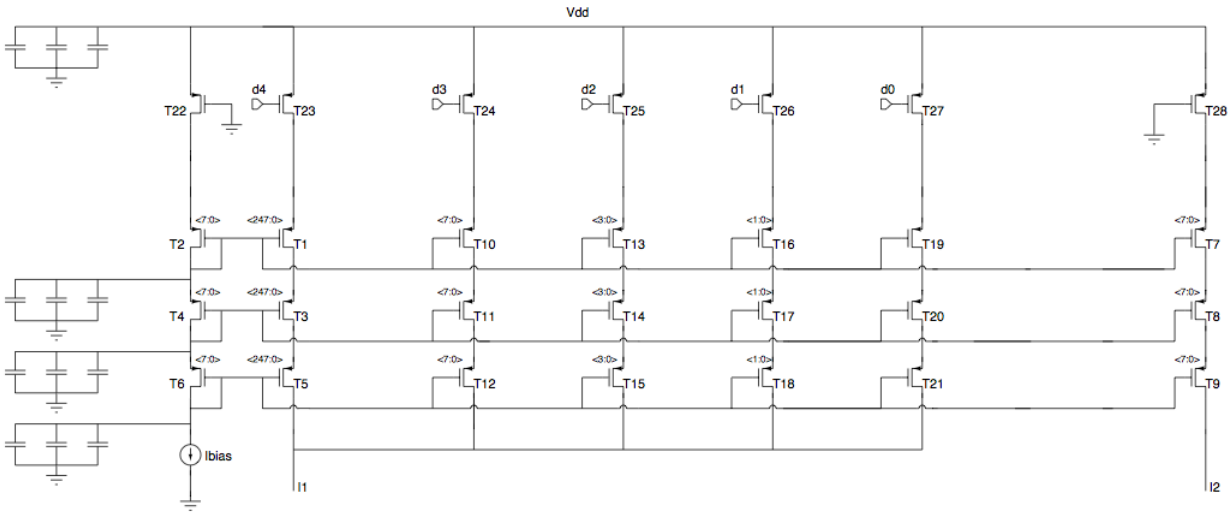

Figure 4.13: Complete current generator

$(W/L)_{T_1}$	$2.5\,\mu m\,/10\,\mu m$
$(W/L)_{T_2}$	$2.5\,\mu m\,/10\,\mu m$
$(W/L)_{T_3}$	$1\,\mu m\,/1\,\mu m$
$(W/L)_{T_4}$	$1\,\mu m\,/1\,\mu m$
$(W/L)_{T_5}$	$1\,\mu m\,/1\,\mu m$
$(W/L)_{T_6}$	$1\,\mu m\,/1\,\mu m$
$(W/L)_{T_7}$	$2.5\,\mu m\,/10\,\mu m$
$(W/L)_{T_8}$	$1\,\mu m\,/1\,\mu m$
$(W/L)_{T_9}$	$1\,\mu m\,/1\,\mu m$
$(W/L)_{T_{10}}$	$2.5\,\mu m\,/10\,\mu m$
$(W/L)_{T_{11}}$	$1\,\mu m\,/1\,\mu m$
$(W/L)_{T_{12}}$	$1\,\mu m\,/1\,\mu m$
$(W/L)_{T_{13}}$	$2.5\,\mu m\,/10\,\mu m$
$(W/L)_{T_{14}}$	$1\,\mu m\,/1\,\mu m$

$(W/L)_{T_{15}}$	$1\,\mu m\,/1\,\mu m$
$(W/L)_{T_{16}}$	$2.5\,\mu m\,/10\,\mu m$
$(W/L)_{T_{17}}$	$1\,\mu m\,/1\,\mu m$
$(W/L)_{T_{18}}$	$1\,\mu m\,/1\,\mu m$
$(W/L)_{T_{19}}$	$2.5\,\mu m\,/10\,\mu m$
$(W/L)_{T_{20}}$	$1\,\mu m\,/1\,\mu m$
$(W/L)_{T_{21}}$	$1\,\mu m\,/1\,\mu m$
$(W/L)_{T_{22}}$	$8\,\mu m\,/200\,nm$
$(W/L)_{T_{23}}$	$246\,\mu m\,/200\,nm$
$(W/L)_{T_{24}}$	$8\,\mu m\,/200\,nm$
$(W/L)_{T_{25}}$	$4\,\mu m\,/200\,nm$
$(W/L)_{T_{26}}$	$2\,\mu m\,/200\,nm$
$(W/L)_{T_{27}}$	$1\,\mu m\,/200\,nm$
$(W/L)_{T_{28}}$	$4\,\mu m\,/200\,nm$

I_{bias}	$500\,nA$
I_1	$16\,\mu A$
I_2	$504\,nA$

4.3 Time to Amplitude Converter

The capacitor C_1 is put in feed-back of a voltage amplifier. This choice has two purposes. First, in this way the current source is connected to the amplifier input which behaves approximately as a virtual ground. Moreover, the drain voltage of the current source experiences only limited voltage variations, thus improving the linearity. In fact, the current i_1 is higher, therefore the output impedance of the associated current source is not extremely high and it is advisable to have too many voltage swings across it. Second, the amplifier is used to drive the capacitance C_2 to which the output voltage is copied. In this way, the voltage is the same, but the charge stored in C_2 is four times the one stored in C_1, hence reducing the necessary ratio between i_2 and i_1.

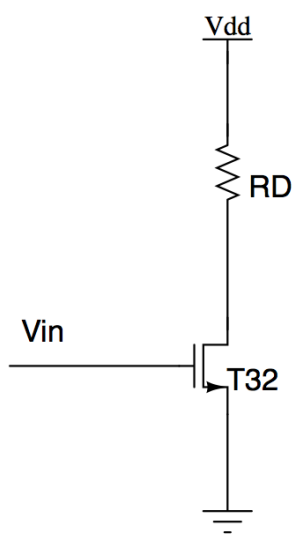

Figure 4.14: Passive load amplifier

To improve this schematic we can use an amplifier with the capacitance in feed-back. The simplest amplifier we can use is a transistor with a passive load. It is a transimpedance amplifier since at input voltage variation the corresponding current variation at the output the amplification is

$$A = -R_D \cdot g_{m32}$$

It is easy to understand that the achievement of a major amplification values is necessary to have a high values of R_D, but this involves that using big R_D we

increase the area consumption so this isn't a good solution. To avoid this problem we need to use an active load like that one shown in Figure 4.15

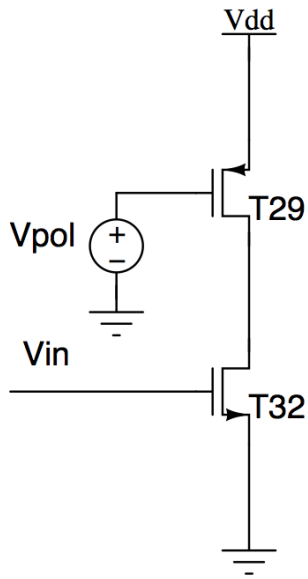

Figure 4.15: Active load amplifier

Now the amplification is

$$A = -r_{29} \cdot g_{m32} \tag{4.4}$$

With this configuration we can achieve higher gain values with a lower area consumption, but this architecture is not yet the best solution because it doesn't achieve neither very high amplification nor a high output resistance, indeed is just r_{29}. To further increase the gain we use a double cascode configuration as shown in Figure 4.16

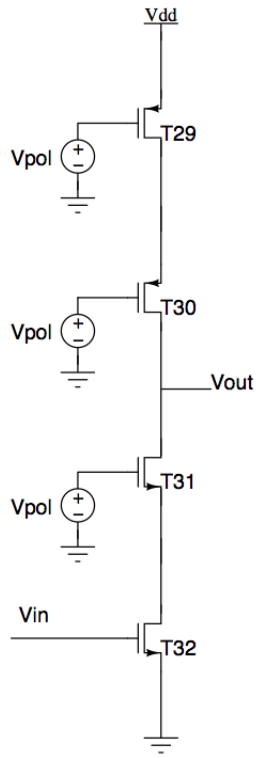

Figure 4.16: Cascode configuration

The resulting r_{out} can be calculated with this small signal model

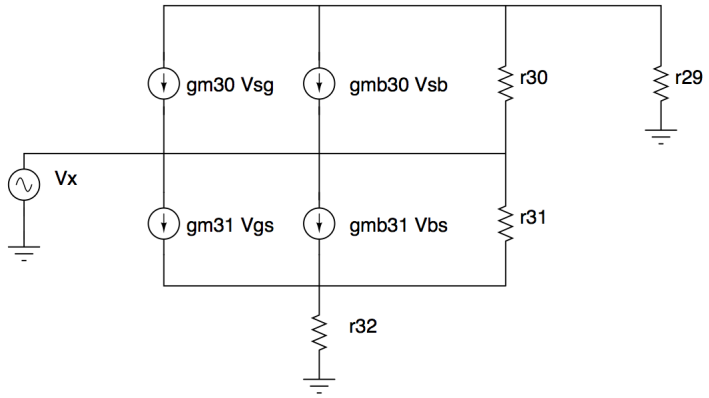

Figure 4.17: Cascode small signal model

the resulting equations are:

$$\begin{cases} (g_{m30} + g_{mb30})\, v_{s30} + \frac{v_{s30}-v_x}{r_{30}} + \frac{v_{s30}}{r_{29}} = 0 \\ -(g_{m30} + g_{mb30})\, v_{s30} - \frac{v_{s30}-v_x}{r_{30}} - (g_{m31} + g_{mb31})\, v_{s31} + \frac{v_x-v_{s31}}{r_{31}} - i_X = 0 \\ (g_{m31} + g_{mb31})\, v_{s31} - \frac{v_x-v_{s31}}{r_{31}} + \frac{v_{s31}}{r_{32}} = 0 \end{cases} \tag{4.5}$$

the resulting output resistance is:

$$\frac{v_X}{i_X} = R_x = \frac{[r_{30} + r_{29} + (g_{m30} + g_{mb30})r_{29}\, r_{30}] \cdot [r_{32} + r_{31} + (g_{m31} + g_{mb31})r_{31}\, r_{32}]}{[r_{30} + r_{29} + (g_{m30} + g_{mb30})r_{29}\, r_{30}] + [r_{32} + r_{31} + (g_{m31} + g_{mb31})r_{31}\, r_{32}]} \tag{4.6}$$

The gain resulting from this is the r_{out} already multiplied per g_{m32}

$$A = -r_{out} \cdot g_{m32} \sim 10^4 \tag{4.7}$$

such gain and output resistance are now high enough.

As mentioned before, in the TAC we have two switches, called switch 1 and switch 2. These switches are both represented as p-mos transistors. The first one is driven by a multiplexer which has a digital control that choses a low voltage value or an high value if we want open or close the switch. The second one has just a digital control so the final architecture is the one shown in the following picture:

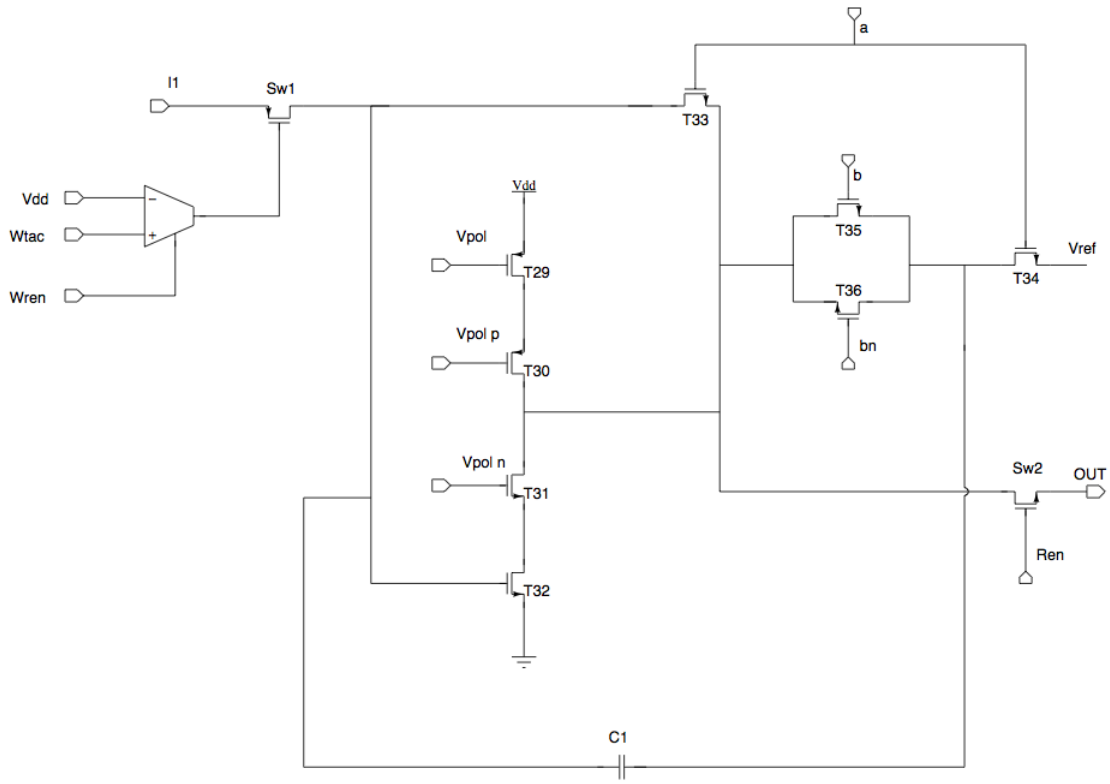

Figure 4.18: Complete TAC structure

The rightmost part has the task to reset the capacitance voltage, this is given by appropriate digital signals which open or close the two p-mos switches. The transistors dimensions are shown in the table

$(W/L)_{T_{29}}$	$10\,\mu m\,/1\,\mu m$
$(W/L)_{T_{30}}$	$20\,\mu m\,/500\,nm$
$(W/L)_{T_{31}}$	$32\,\mu m\,/300\,nm$
$(W/L)_{T_{32}}$	$8\,\mu m\,/300\,nm$
$(W/L)_{T_{33}}$	$1\,\mu m\,/300\,nm$
$(W/L)_{T_{34}}$	$32\,\mu m\,/300\,nm$
$(W/L)_{T_{35}}$	$8\,\mu m\,/300\,nm$
$(W/L)_{T_{36}}$	$16\,\mu m\,/3\,\mu m$
$(W/L)_{Sw1}$	$1\,\mu m\,/200\,nm$
$(W/L)_{Sw2}$	$16\,\mu m\,/200\,nm$

$Vpol$	$700\,mV$
$Vpol_p$	$300\,mV$
$Vpol_n$	$550\,mV$
I_{pol}	$25\,uA$

4.4 Analog to Digital Converter

The third building block is the ADC, as we can immagine there are several kinds of ADCs, it is important understand which one we need to use. An important feature is the low area consumption since the complete TDC will be directly mounted on the strip. One of the most compact ADCs is the Wilkinson ADC, that is composed by a constant current source, a capacitance and a comparator, as we can see in Figure 4.19:

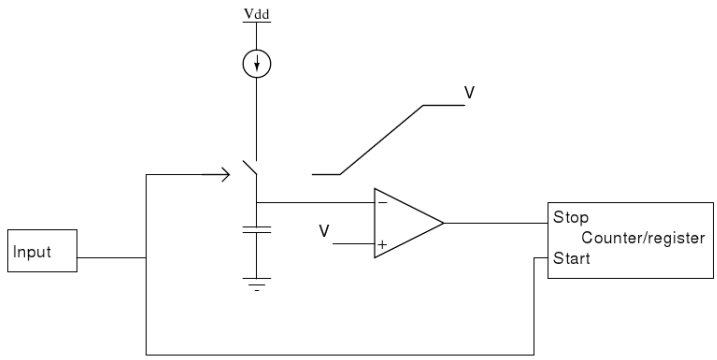

Figure 4.19: Principle of analog TDC

One input of the comparator is connected to the capacitor and the other one to a reference voltage. When the current i_2 is connected to the capacitor, the recharging ramp starts. The value of the coarse counter corresponding to the start of the recharging phase, is stored into a local register, providing the beginning of conversion.

The comparator continuously monitors the voltage on C_2. To maximize the speed, a synchronous comparator embedding positive feed-back is used. When the value on C_2 reaches back the baseline, the comparator flips, storing the corresponding value on the Gray counter into another register. This value provides the end of conversion. The difference between the End and Start of conversion yields to a measurement of the analog voltage stored in the TAC and hence the fine time.

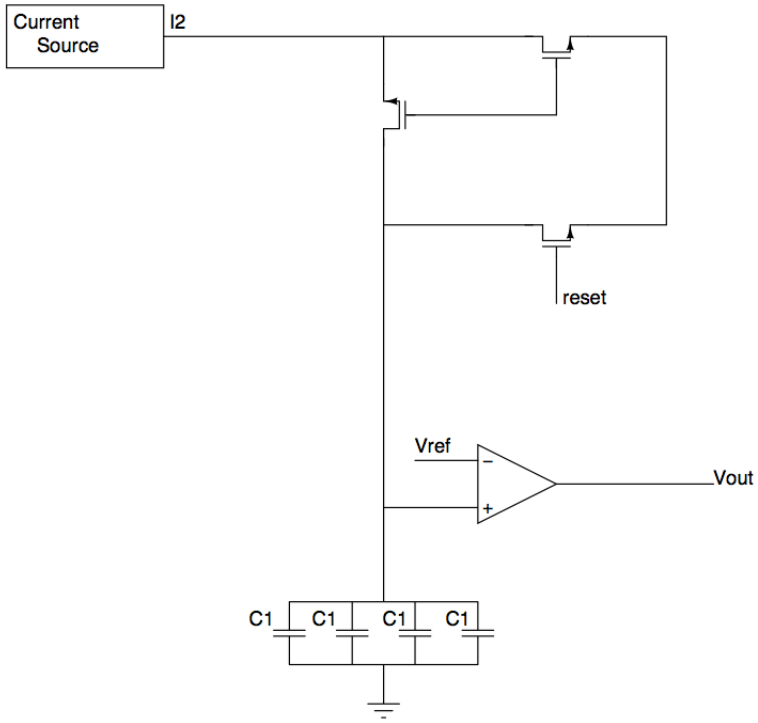

Figure 4.20: Wilkinson implementation

When the conversion is over, C_2 is reset to V_{ref} to avoid any hysteresis between different conversion cycles. Then a new conversion can take place.

The complete TDC is shown in Figure 4.21

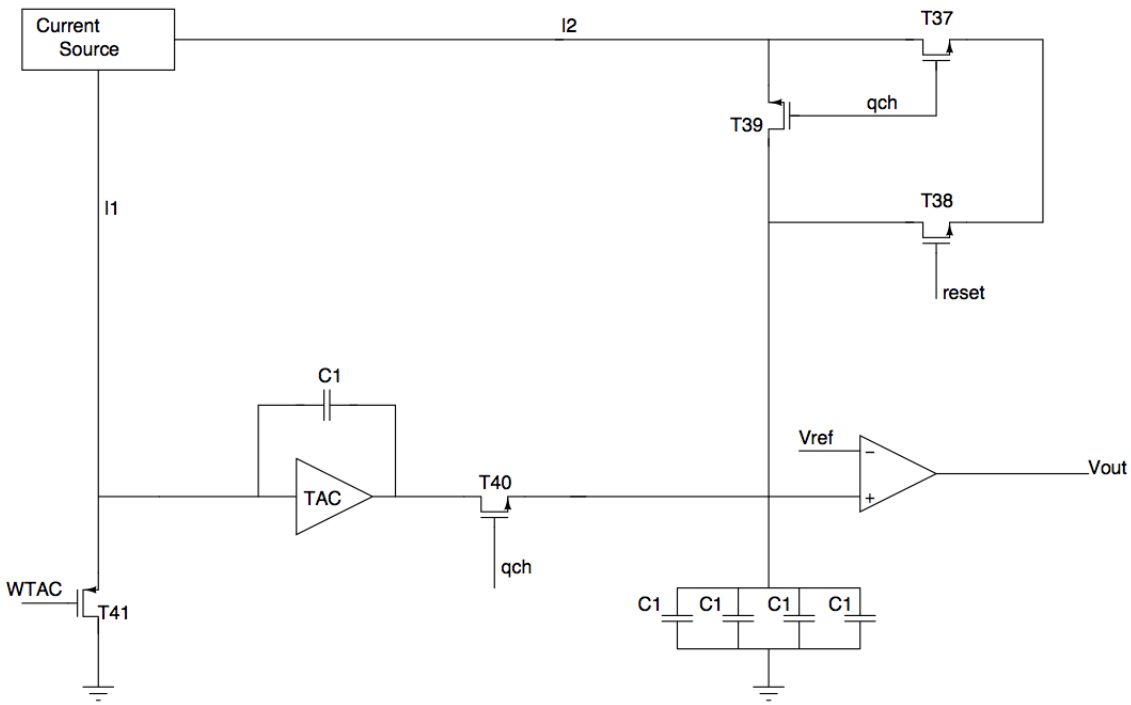

Figure 4.21: Complete TDC structure

$(W/L)_{T_{37}}$	$2\,\mu m\,/120\,nm$
$(W/L)_{T_{38}}$	$2\,\mu m\,/120\,nm$
$(W/L)_{T_{39}}$	$2\,\mu m\,/120\,nm$
$(W/L)_{T_{40}}$	$2\,\mu m\,/120\,nm$
$(W/L)_{T_{41}}$	$2\,\mu m\,/120\,nm$
C_1	$510.5\,fF$

Chapter 5

Simulations

In this chapter we study the performance of the TDC, to do this we employ a Computer Aided Design (CAD) software which allows a detailed simulation of the circuit. In particular we use the CADENCE software, which is one of the most used professional CAD for the integrated circuit design. The tool allows to perform different types of analysis. The DC analysis allows to study the bias point of the circuits. The AC analysis is used to investigate the frequency domain behavior through linearized small signal models. Transient simulations are instead time domain simulations which employ the full characteristics of the devices. Therefore they allow to study issues such as non-linearity and saturation of the circuit. Furthermore, all the simulations can be run by changing the temperature and study the effects of the unavoidable uncertainties which affect the circuit fabrication.

5.1 Currents Source

The first analysis aims to understand if the ratio between the currents used to discharge and recharge the feed-back capacitor in the TAC is really fixed or not. To do so we can use a Monte Carlo simulation: this analysis changes several random parameters in each transistor leading to changes in the associate currents. The program output is a current ratio histogram which has in the x coordinate the current ratio and in the y coordinate the counts. We have done this Monte Carlo simulation with 100 point and the current source generates a current I_1 32 times I_2. The result is reported in Figure 5.1:

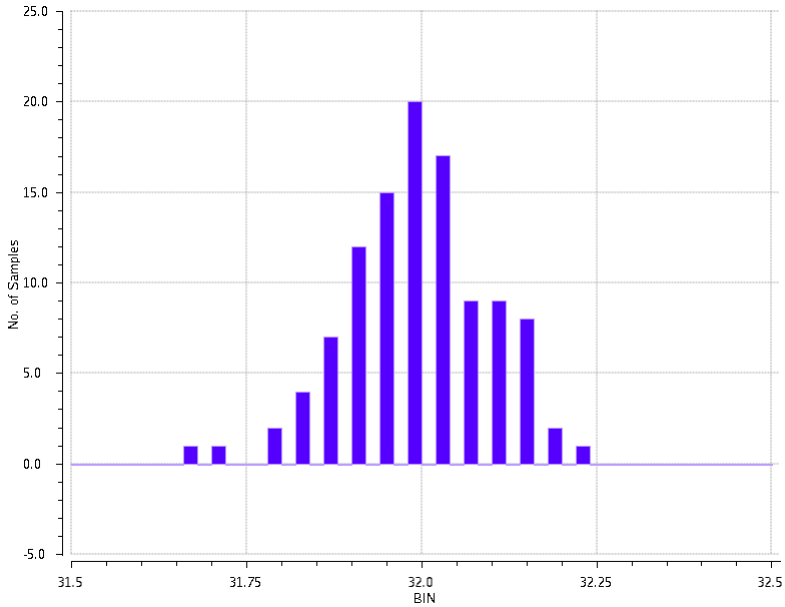

Figure 5.1: Montecarlo simulations of the current ratio

To understand the goodness of the result we use the gaussian fit which allows us to calculate which is the mean and the standard deviation. This fit has been done whit another program: Mathematica. This is a calculation program allowing to analyze a large number of data. The results is shown in Figure 5.2:

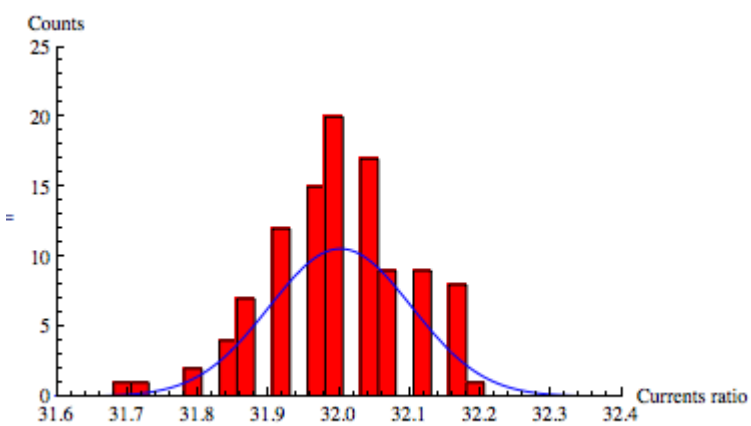

Figure 5.2: Analysis with Mathematica of the Montecarlo simulations

This circuit works with a principle similar to the one used in an application that was already developed and implemented in a $0.13\,\mu m$ CMOS technology. It is therefore interesting to compare the accuracy of the two circuits. The Monte Carlo analysis done with the parameters of the $0.13\,\mu m$ process is reported in Figure 5.3

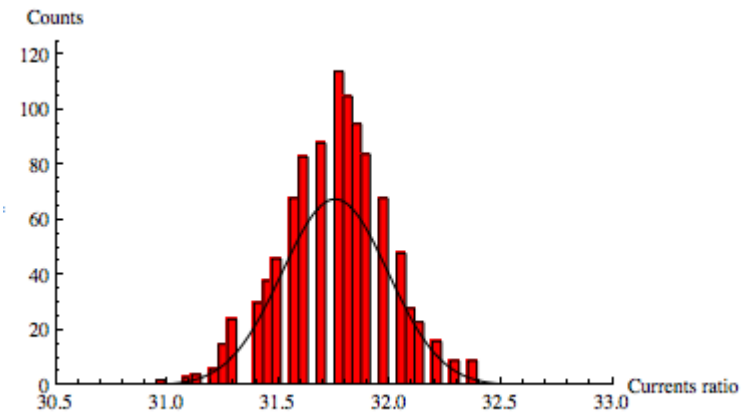

Figure 5.3: Monte Carlo simulations of the current ratio in the old technology

The results of this comparison are compiled in the following table. It must be pointed out that the Monte Carlo simulations with the $0.13\,\mu m$ technology were done with a higher number of iterations (1000 versus 100).

	Old Technology	New Technology
Mean	31.75	32.00
Standard deviation	0.24	0.10

The standard deviation error for the first simulation with 1000 points is:

$$\sigma_{sd} = \frac{0.24}{\sqrt{2(N-1)}} = 0.022 \tag{5.1}$$

For the second simulation with 100 points the standard deviation error is instead:

$$\sigma_{sd} = \frac{0.10}{\sqrt{2(N-1)}} = 0.071 \tag{5.2}$$

As we can see from the above formulas the two standard deviations are different, so we can conclude that with the new technology the currents ratio is less influenced by the transistors variations.

To allow a proper working of the TDC, the current source should be as ideal as possible, which means that we need to maximize its output impedance. To study this property, we change the voltage at the output of the currents source with a voltage generator called V_x and we measure the corresponding change in current. Ideally, we should not observe any variation. The current I_1 is connected to the input of the TAC amplifier. This input behaves approximately as a virtual ground, therefore we do not aspect big variation of this potential. Thus we chose to sweep the best voltage V_x from 400 mV to 520 mV in 12 steps. The measured current is shown in Figure 5.4

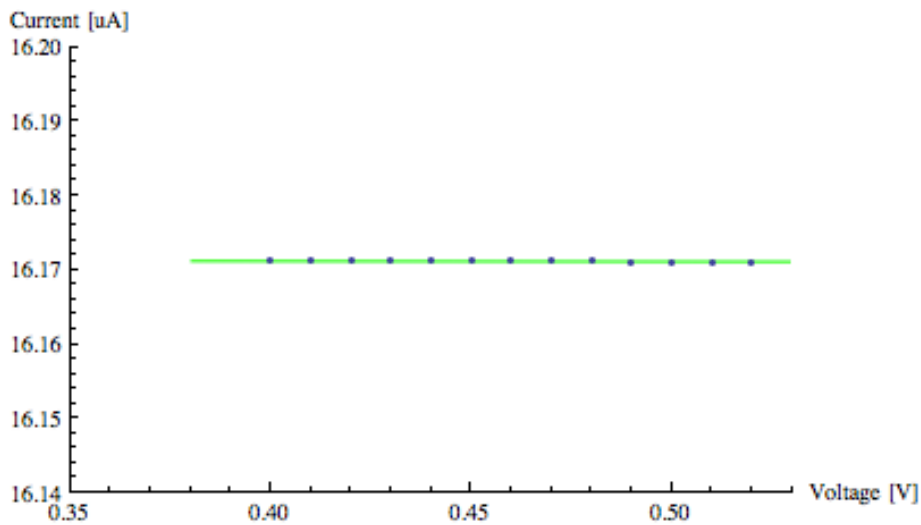

Figure 5.4: Fit of the I_1 for the different value of V_x

To understand if this current source is good enough we need to know how much error we can tolerate. This is defined by the 9 bits resolution required to the TDC. Hence we can tolerate a maximum error of 0.00195. Since the simulations are not affected by any kind of error we can't estimated the χ^2 but just the goodness of the fit, which is reported below:

$$f(x) = 16.1714 - 0.00055x \tag{5.3}$$

$$Err = \left(\sum_i \left| \frac{(I_{th})_i - (I_{exp})_i}{(I_{th})_i} \right| \right) * 100 = 0.000025\% \tag{5.4}$$

In order to evaluate the current variation, we divided the b coefficient by the mean value. We can conclude that is a good current generator for the I_1 branch from 400 mV to 550 mV, indeed we have a current variation per mV of 0.034‰. To have a complete analysis we also change the V_x from ground to the voltage power supply and the result is shown in Figure 5.5

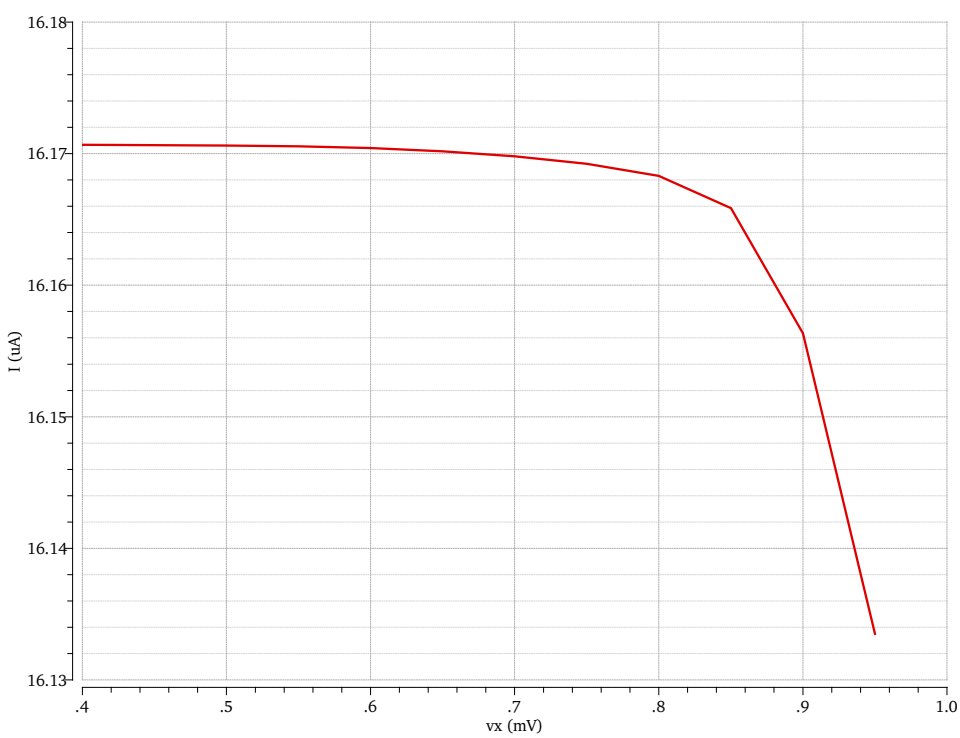

Figure 5.5: Complete characteristic of the current I_1

This is a very interesting result because we can see very well when each cascode transistor goes in the linear region leading to a change in the current slope. At 800 mV the first cascode is pushed in the linear region and the current decreases a little,

at 850 mV the second cascode goes in the linear region and the current decreases again and the slope now is much steeper. Finally, at 900 mV voltage value also the third transistor is in linear region and the current falls down abruptly.

For the second current the dynamic region is different. This current is the recharging one, so the DC value varies form about $600mV$ to $800mV$ which is the V_{ref} set on the comparator. To have a complete study we start the V_x from $500mV$ and we stop at $900mV$ within 9 steps, the results are reported in Figure 5.6

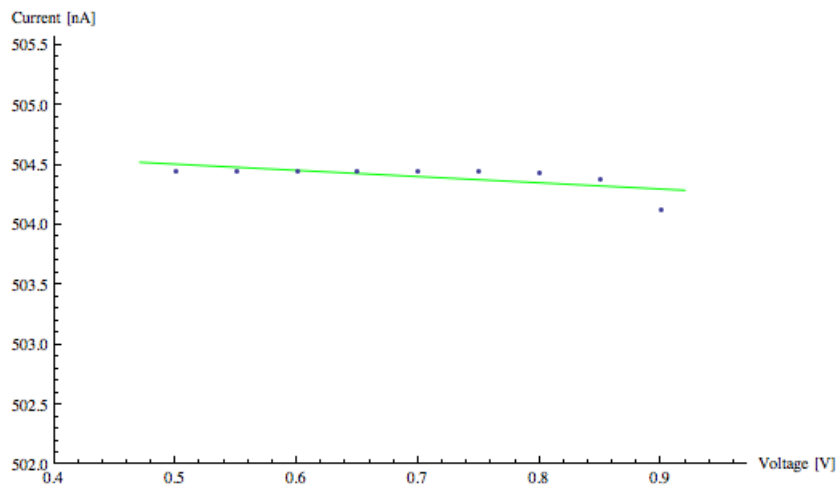

Figure 5.6: Fit of the I_2 for the different value of V_x

Also in this case there is a weak deviation from the linearity:

$$f(x) = 504.766 - 0.5187x \tag{5.5}$$

and the goodness of the fit is:

$$Err = \left(\sum_i \left| \frac{(I_{th})_i - (I_{exp})_i}{(I_{th})_i} \right| \right) * 100 = 0.026\% \tag{5.6}$$

The current variation per mV in this last range is 1.02‰. Despite the fact that we have a worse trend of obtained data, in terms of linearity, the current variation is not dramatically affected. This loss of linearity is due to the fact that in this voltage range the transistors begin to go in the linear region so the current falls down as we can se in Figure 5.7:

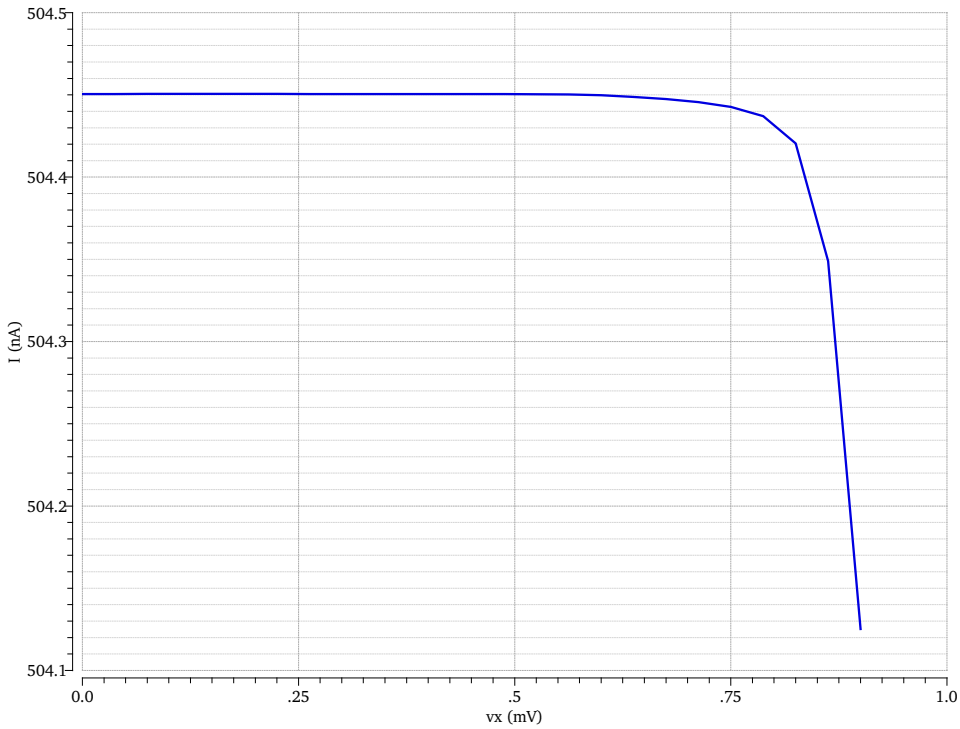

Figure 5.7: Complete characteristic of the current I_2

This is confirmed if we do the last analysis until 850 mV. The fit equation and its goodness become:

$$f(x) = 504.531 - 0.1370x \tag{5.7}$$

$$Err = \left(\sum_i \left| \frac{(I_{th})_i - (I_{exp})_i}{(I_{th})_i} \right| \right) * 100 = 0.0023\% \tag{5.8}$$

and the current variation per mV becomes 0.27‰.

Since the process to make the transistors is not an exact process but is a statistical one, it is necessary to simulate the circuit in the extreme cases, this analysis is called Corner analysis. The Fast Fast (FF) case, where the first "F" refers to the n-mos transistors and the second one to the p-mos transistors, is the case where all transistors have the maximum speed. The Slow Slow (SS) case is the opposite case where all transistors have a slow behavior and the mixed cases are the Fast Slow (FS) and the Slow Fast (SF).

For our currents source we have only p-mos transistor so we have done just the simulation for the FF case and the SS one. For the current I_1 the results are showed in Figure 5.8 where the green straight line is the case already discussed, the blue one is the FF case and the red one is the SS case

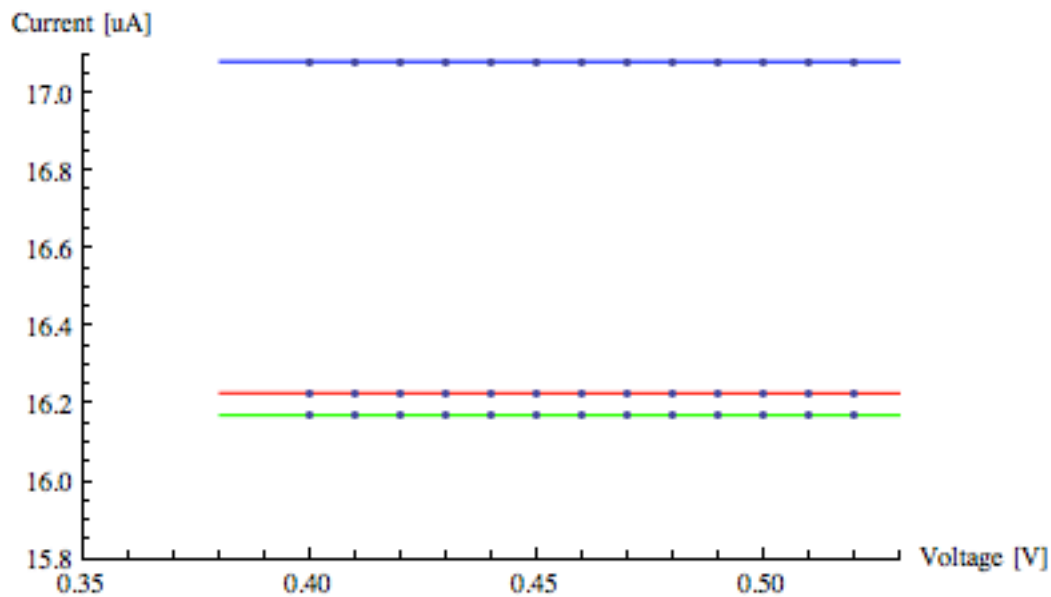

Figure 5.8: Fit of the I_1 for the different value of V_x and difference corners

The relative b coefficients are:

$$f_{FF}(x) = 17.0824 - 0.0020x \tag{5.9}$$

$$f_{SS}(x) = 16.2297 - 0.0036x \tag{5.10}$$

the fit goodnesses are:

$$Err_{FF} = \left(\sum_i \left| \frac{(I_{th})_i - (I_{exp})_i}{(I_{th})_i} \right| \right) * 100 = 5.629\% \tag{5.11}$$

$$Err_{SS} = \left(\sum_i \left| \frac{(I_{th})_i - (I_{exp})_i}{(I_{th})_i} \right| \right) * 100 = 0.352\% \tag{5.12}$$

and the current variations per mV are: for the FF case 0.12‰ and for the SS case 0.22‰.

We can notice that the linearity is maintained and this result is not surprising because the voltage range is in the region where all transistors are saturated.

For the current I_2 we have done the same analysis and the results are reported in Figure 5.9:

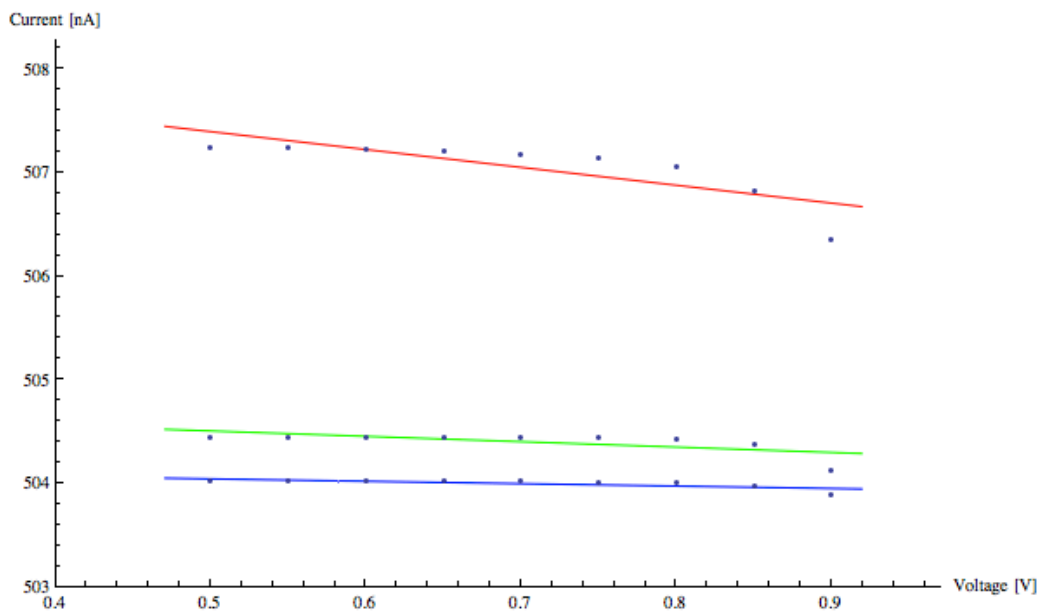

Figure 5.9: Fit of the I_2 for the different value of V_x and difference corners

The fit functions are:

$$f_{FF}(x) = 504.160 - 0.2312x \tag{5.13}$$

$$f_{SS}(x) = 508.257 - 1.7241x \tag{5.14}$$

while the fit goodnesses are:

$$Err_{FF} = \left(\sum_i \left| \frac{(I_{th})_i - (I_{exp})_i}{(I_{th})_i} \right| \right) * 100 = 0.0866\% \tag{5.15}$$

$$Err_{SS} = \left(\sum_i \left| \frac{(I_{th})_i - (I_{exp})_i}{(I_{th})_i} \right| \right) * 100 = 0.5249\% \tag{5.16}$$

The current variations per mV are: for the FF case 0.46‰ and for the SS case 3.40‰.

With the analyses already done we can extrapolate another important parameter which is the output resistance R_{out}. This parameter must be very high and this should be guaranteed by the cascode structure. To calculate the output resistance we use the following formula

$$\frac{\Delta V_x}{\triangle I} = R_{out} \tag{5.17}$$

The results are represented in the following graphs:

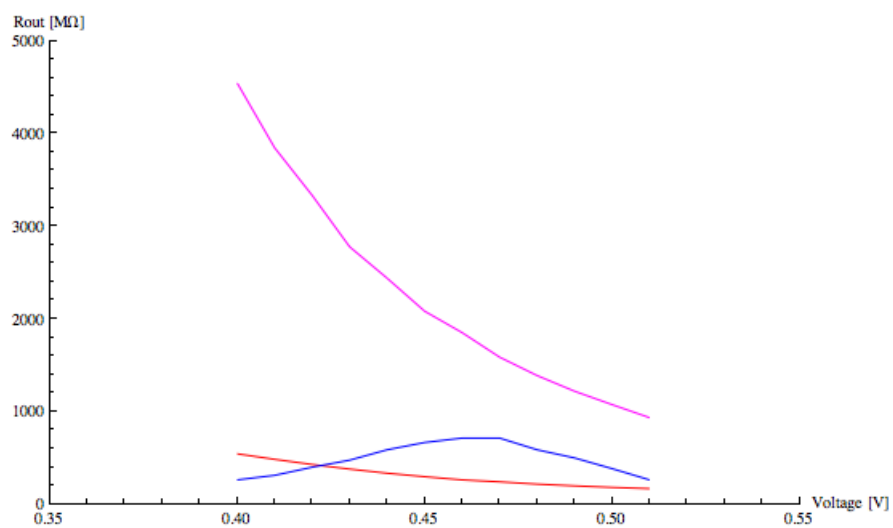

Figure 5.10: Output resistances for the I_1 current branch

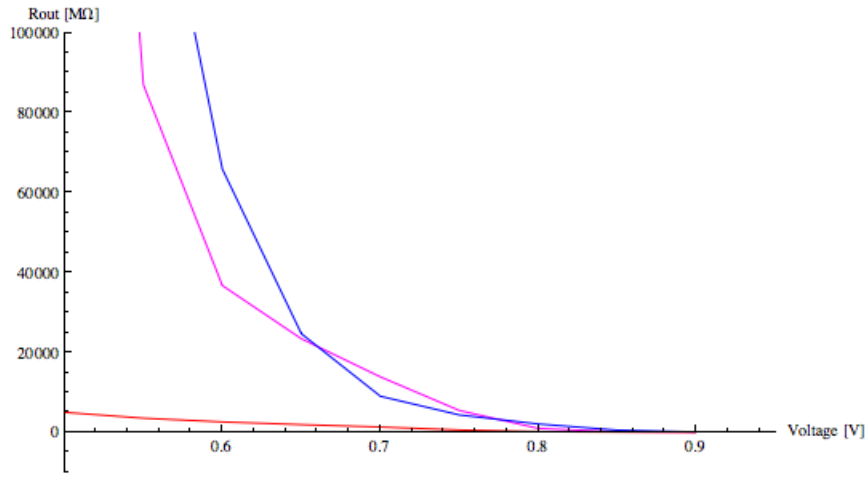

Figure 5.11: Output resistances for the I_2 current branch

As in the current cases the red one are the SS cases, the blue one are the FF cases and the purple one are the nominal cases. For the I_1 branch R_{out} is above $10^8\,\Omega$ while for the I_2 branch the R_{out} is between $10^{11}\,\Omega$ and $10^7\,\Omega$.

5.2 Time to Amplitude Converter

This structure is made by a cascode amplifier, a capacitor and some switches, as we have before. We want now to study if our circuit fulfills the specifications discussed in the previous chapters. First of all we implemented the following structure:

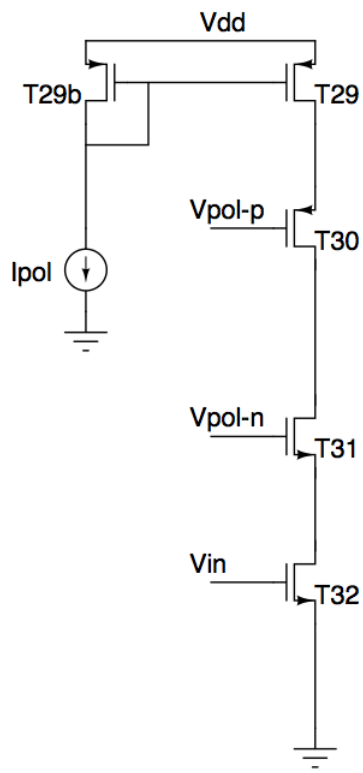

Figure 5.12: Cascode configuration with the smallest dimensions

with the parameters given in the table:

$(W/L)_{T_{29}}$	$2\,\mu m\,/120\,nm$
$(W/L)_{T_{30}}$	$2\,\mu m\,/120\,nm$
$(W/L)_{T_{31}}$	$2\,\mu m\,/120\,nm$
$(W/L)_{T_{32}}$	$2\,\mu m\,/120\,nm$

$Vpol_p$	650 mV
$Vpol_n$	550 mV
I_{pol}	$100\,\mu A$

The dimensions are as small as possible in order to have a small area consumption. The first study is done to understand which is the output resistance, and we use the configuration shown in Figure 5.13:

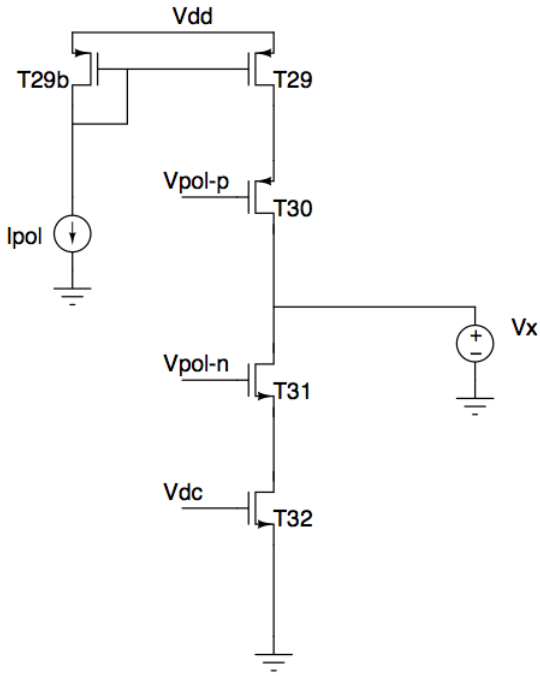

Figure 5.13: Configuration to study the output resistance

We vary V_x from 500mV to 800mV because the recharging ramp stay in this voltage range. Using the formula 5.17 we obtain the results which are reported in the following figure

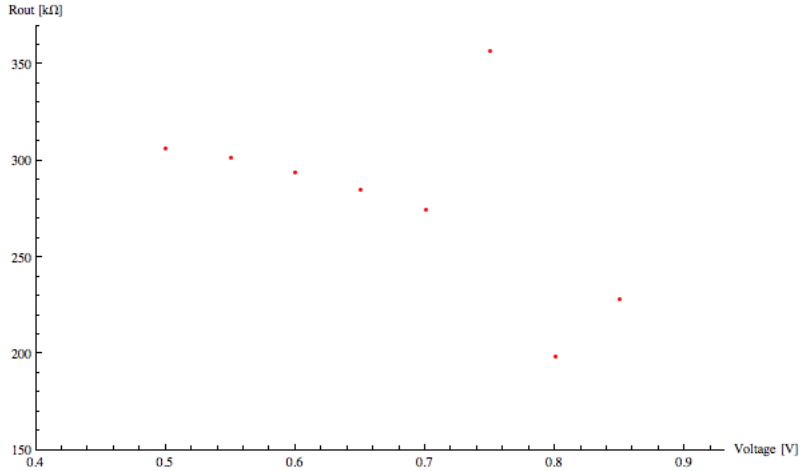

Figure 5.14: Output resistance for the cascode configuration

So the r_{out} is about $250\,k\Omega$

The second analysis is carried out to quantify the gain. In particular we want to study the open loop gain and for analysis we need to know at which input voltage we have the maximum amplification. So we sweep the input voltage from ground to the voltage power supply. The voltage output is shown in Figure 5.15

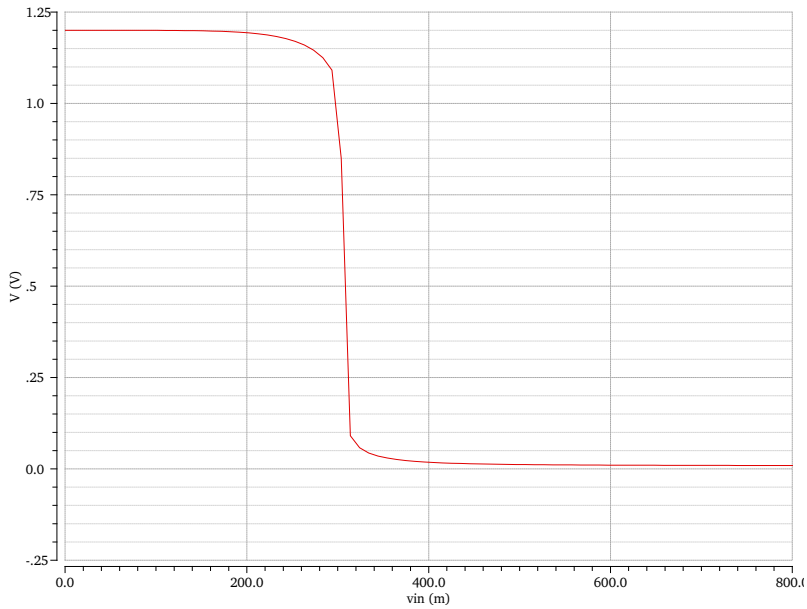

Figure 5.15: Output response to find the operating point

Now we need to find which input value has the maximum slope. To have a better resolution we reduce the range of the input. When we find this value, we set the DC voltage input with this value and this is the operation point. Now we can insert 1V as AC value and we can plot the Bode diagram. The result is reported in Figure 5.16:

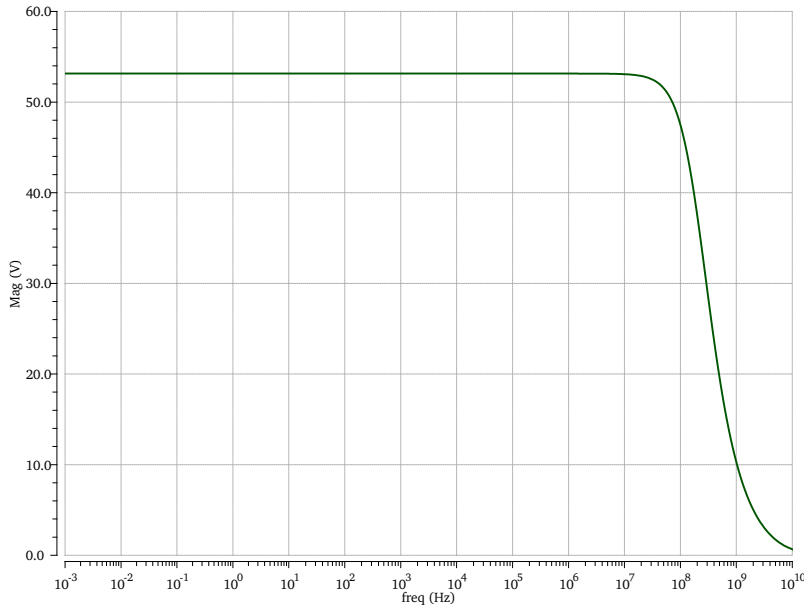

Figure 5.16: Bode diagram

Since we have put 1V in the AC value the gain is the value in the figure above directly, and is 52. This value does not satisfy us because is too low.

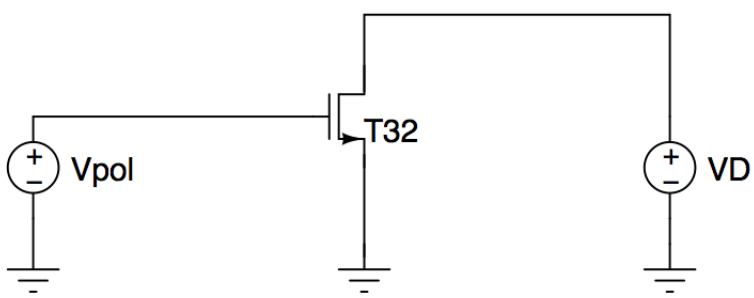

Figure 5.17: Architecture for the study the L dimension

So we need to change the transistors dimensions to achieved a better r_{out} and especially the gain. To understand which is the best condition we study the configuration shown in Figure 5.17. We set the $v_{pol} = 400\,mV$, the $v_D = 400\,mV$

to guarantee the saturation and we change the L dimension from 120 nm to 700 nm and we evaluate the r_{32}. The result is report in the following figure:

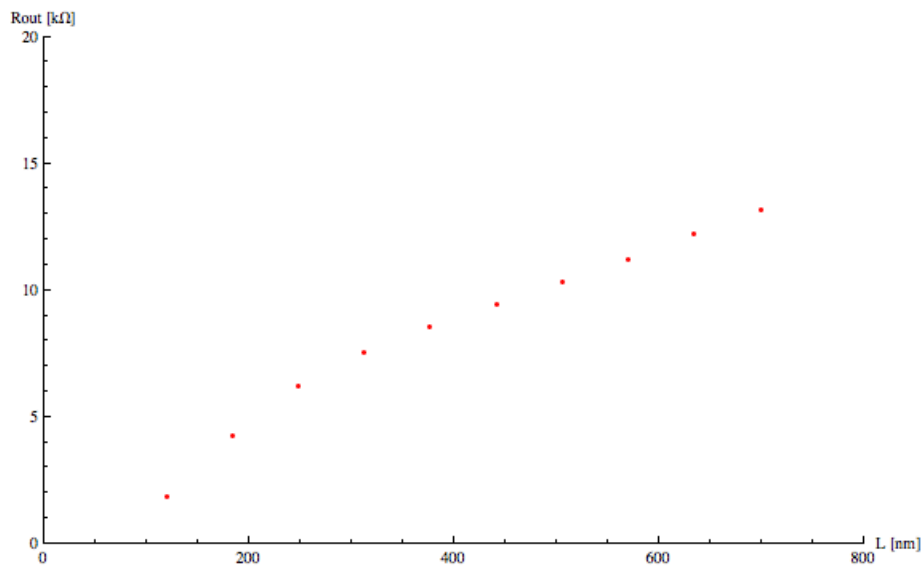

Figure 5.18: Output resistances for difference L value

We can see that if we increase the L value the output resistance rises up but if we increase too much, the transistor has a big area consumption, so we choose the value 240 nm which give us a r_{out} about 6 $k\Omega$. However the transistor changes a lot its characteristics with the v_D variations also if the transistor is in the saturation region. If we fix the L and change the v_D from 30 mV to 300 mV we can notice, in Figure 5.19, that the output resistance increases with the v_D value so we need to achieved this value in the cascode configuration.

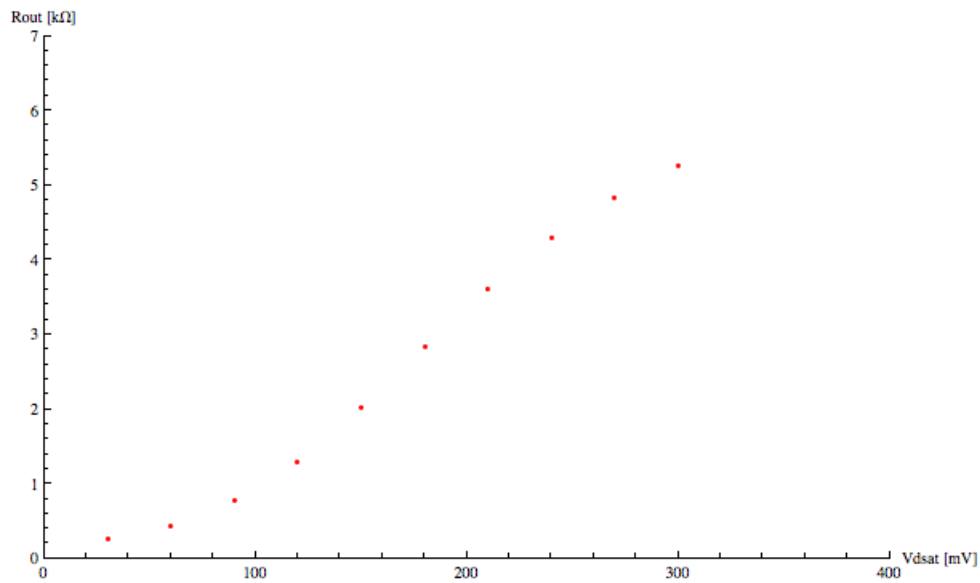

Figure 5.19: Output resistances for different V_{dsat} with a fixed length

We can't increase a lot this one because the n-transistor which cascode the input could go in the linear region. So the structure has the dimensions shown in the following table:

$(W/L)_{T_{29}}$	$20\,\mu m\,/500\,nm$
$(W/L)_{T_{30}}$	$20\,\mu m\,/240\,nm$
$(W/L)_{T_{31}}$	$20\,\mu m\,/240\,nm$
$(W/L)_{T_{32}}$	$50\,\mu m\,/240\,nm$

$Vpol_p$	600 mV
$Vpol_n$	500 mV
I_{pol}	$100\,\mu A$

The DC operation point for this circuit is 300.16 mV and the r_{out} find with the v_x generator is reported in the Figure 5.20:

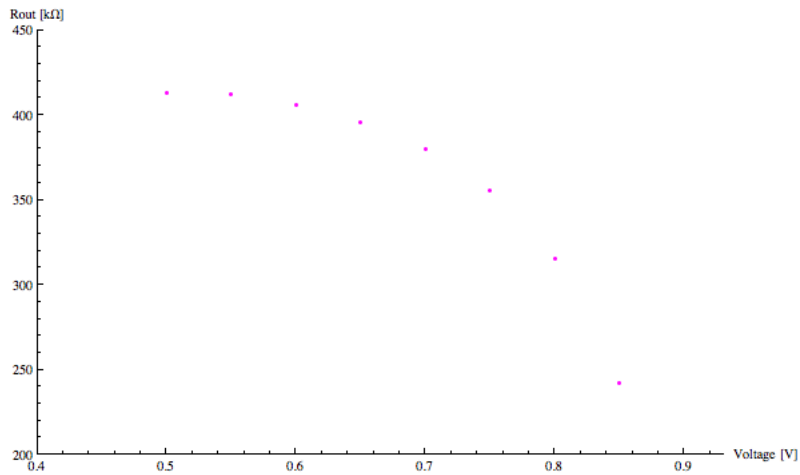

Figure 5.20: Output resistances for the mirror current equal to $100\,\mu m$

The resistance is about $350\,k\Omega$, is higher than before. To understand which is the gain we run the AC analysis and we obtain the following Bode diagram:

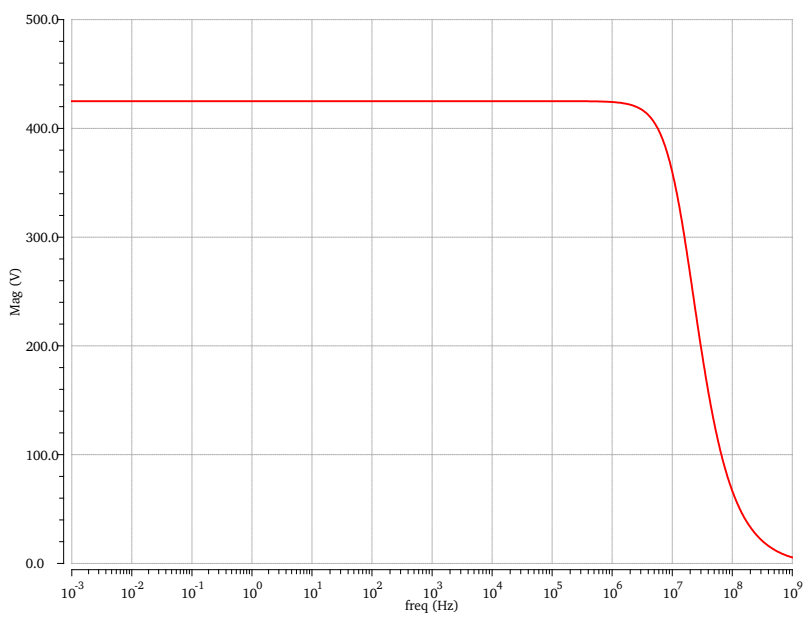

Figure 5.21: Bode diagram

As we can see the gain now is 424.9 and this result doesn't satisfies us so we have to optimize the circuit and the new dimensions and polarize value are reported in the table referred to Figure 4.18. Now the Bode diagram for the new operation point, which is 351.538 mV, is :

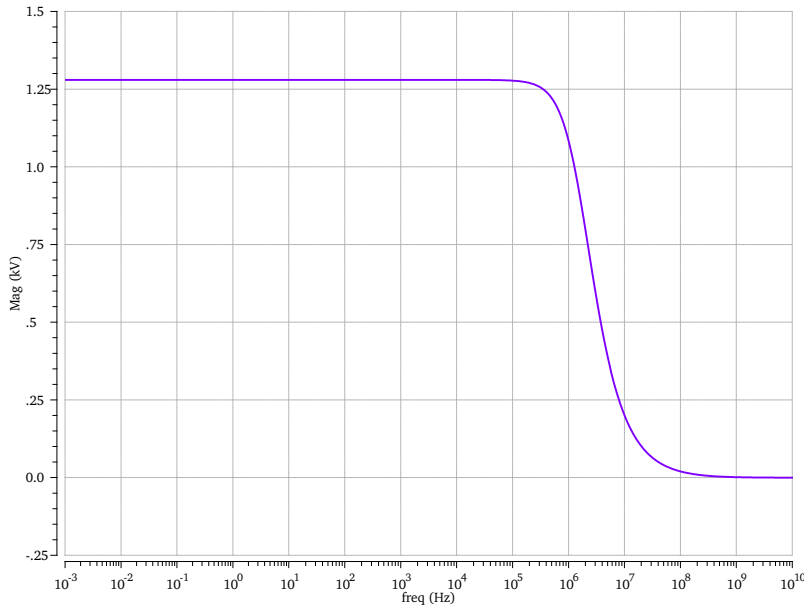

Figure 5.22: Bode diagram for the final configuration

So the gain is now 1250. In the SS case the DC operation point changes in 305.026 mV and the gain is 860 as we can see in the following figure:

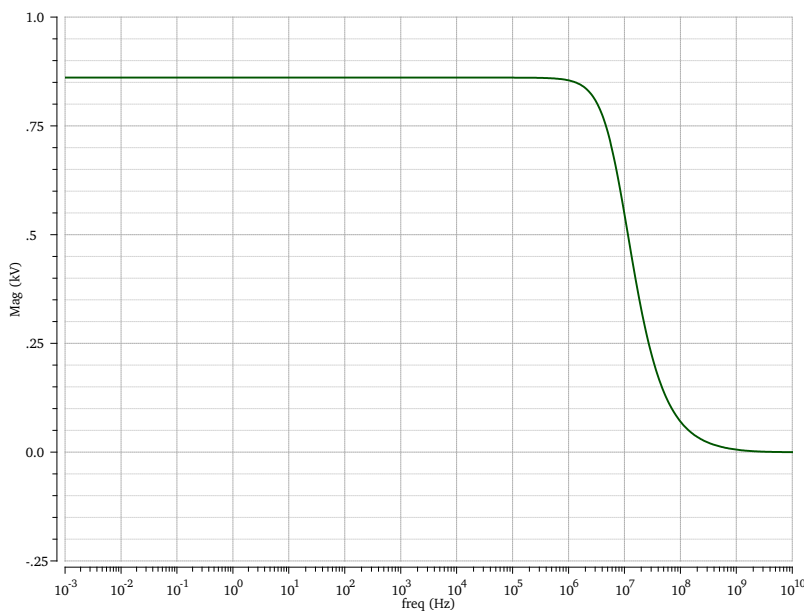

Figure 5.23: Bode diagram for the final configuration in the SS case

In the FF case the DC operation point is 305.028 mV and the gain is 861 as we can see in the Figure 5.24:

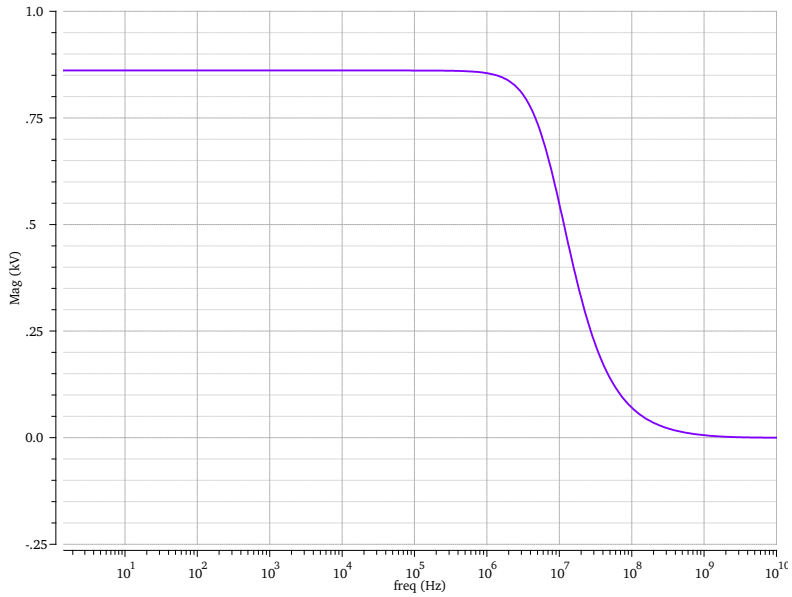

Figure 5.24: Bode diagram for the final configuration in the FF case

To understand if this configuration is a good one it is necessary to calculate the output resistance. The resistance trend is shown in the following figure:

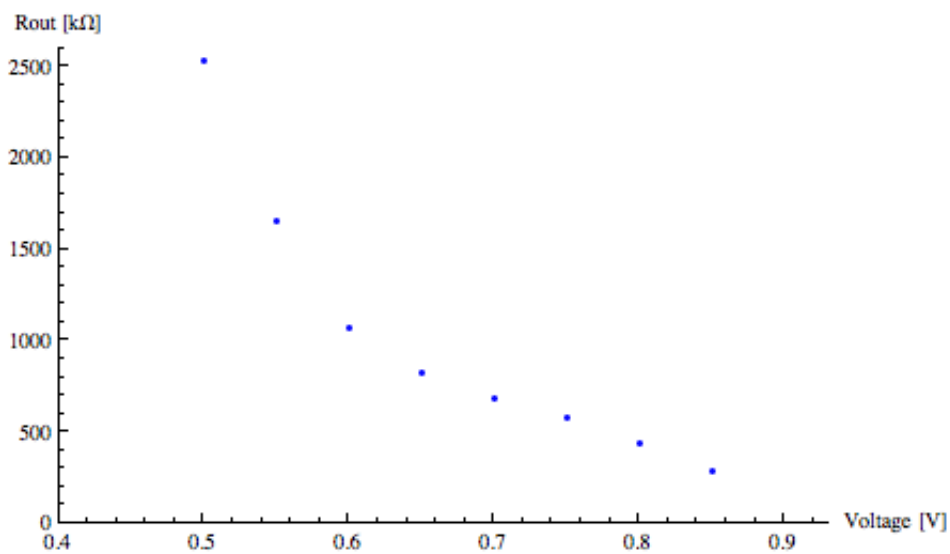

Figure 5.25: Output resistance for the final configuration

we can also verify the r_{out} (formula 4.6) obtained in the previous chapter. With the CAD program we can see each operation point and so we can insert each value. For $v_x = 500mV$ we obtain:

r_{29}	$809.9\,k\Omega$
r_{30}	$75.4\,k\Omega$
r_{31}	$67.9\,k\Omega$
r_{32}	$15.3\,k\Omega$
g_{m30}	$340.9\,\mu\Omega^{-1}$
g_{mb30}	$67.9\,\mu\Omega^{-1}$
g_{m31}	$610.3\,\mu\Omega^{-1}$
g_{mb31}	$69.2\,\mu\Omega^{-1}$

Therefore the resistance is:

$$\frac{v_X}{i_X} = R_x = \frac{[r_{30} + r_{29} + (g_{m30} + g_{mb30})r_{29}\,r_{30}] \cdot [r_{32} + r_{31} + (g_{m31} + g_{mb31})r_{31}\,r_{32}]}{[r_{30} + r_{29} + (g_{m30} + g_{mb30})r_{29}\,r_{30}] + [r_{32} + r_{31} + (g_{m31} + g_{mb31})r_{31}\,r_{32}]} = 2.8\,M\Omega \tag{5.18}$$

This is a confirmation that the above formula is correct and so the small signal model too.

So for the next simulation we use this architecture.

5.3 Linearity

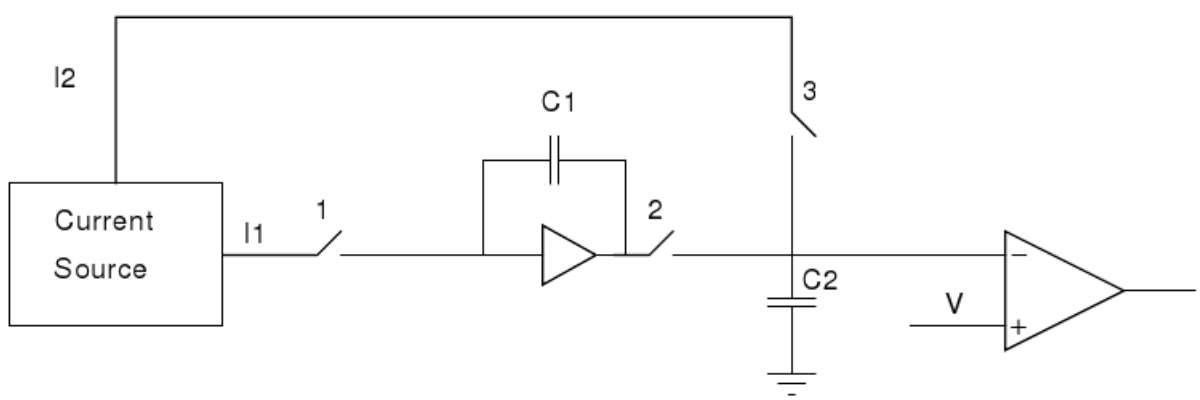

Figure 5.26: TDC building blocks

We now study the linearity of the full TAC which is represented in Figure 5.26. For this analysis we simulate that the circuit receives the ToT edge in equidistant time intervals, between $87.5ns$ and $100ns$. We must send just one signal at a time because it is necessary to set the time during which the switch number 1 stays closed. The results are shown in the following figure.

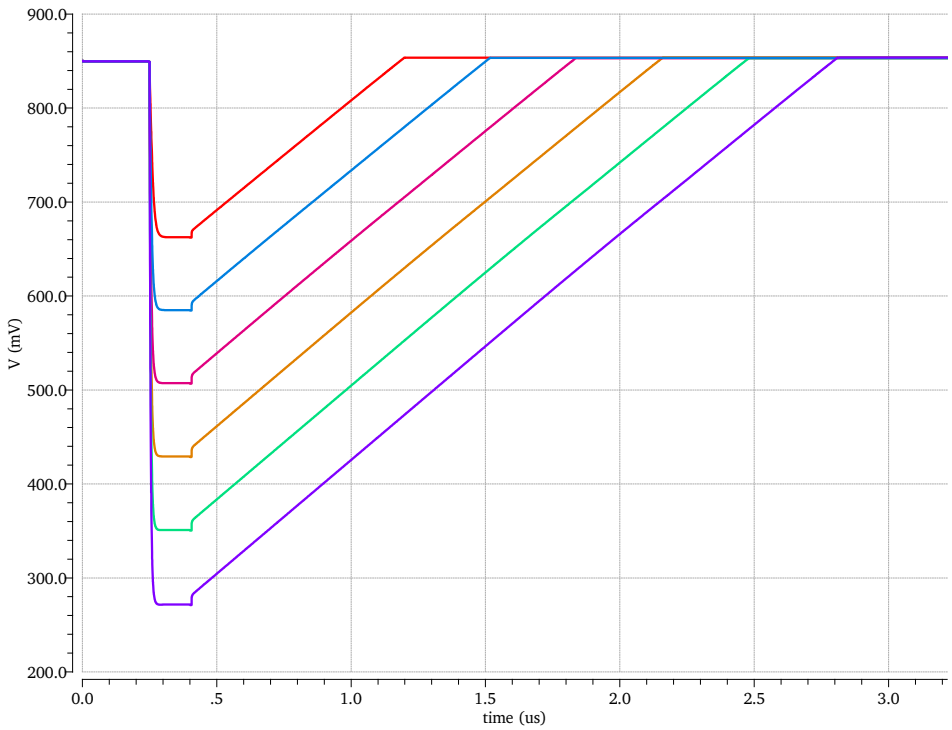

Figure 5.27: Signal for equidistant time intervals

To understand if the circuit has a linear behavior we used a counter to analyze the time between the start, when the signal falls down, and the stop, when the signal reaches the baseline value. So this time is plotted versus the time during which the switch number 1 stays closed and the result is in Figure 5.28

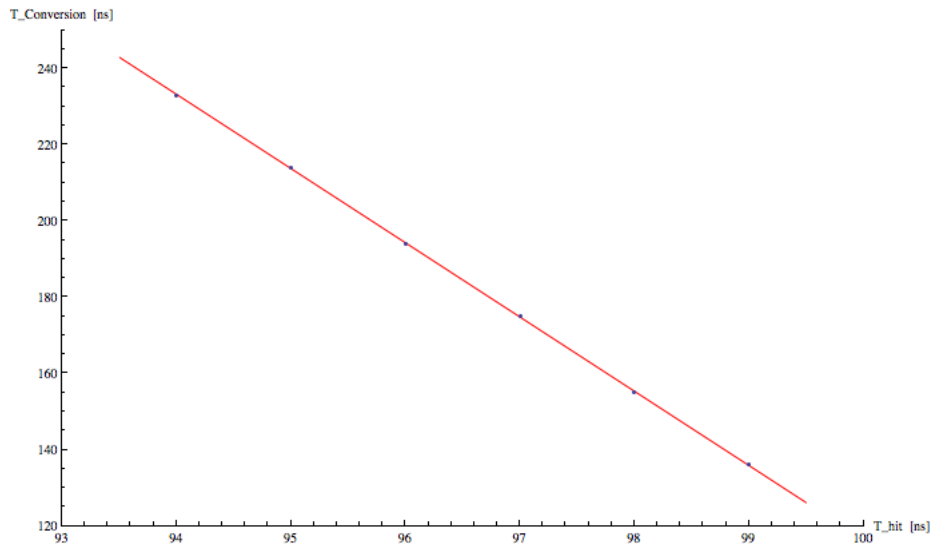

Figure 5.28: Fit of the TDC linearity

There aren't the error bars because these are simulations data affected only by rounding, but it is necessary to know how this circuit is linear, so we use the following formula which gives us the goodness of fit:

$$Err = \left(\sum_i \left| \frac{(T_{th})_i - (T_{exp})_i}{(T_{th})_i} \right| \right) * 100 = 0.13\% \tag{5.19}$$

The error which we commit is 0.13% thus we can say that the circuit is linear. We can study if this linearity is given by a two different non-linearities since the process can be divided in two: the discharging and the recharging process.

To investigate these aspects we carried out two different analysis. For the discharging process we took the difference between the capacitance C_1 voltage, which is the voltage value to reach before the recharging ramp, and the baseline value as we can see in Figure 5.27. We plot this difference to vary the time intervals and the result is shown in the following figure.

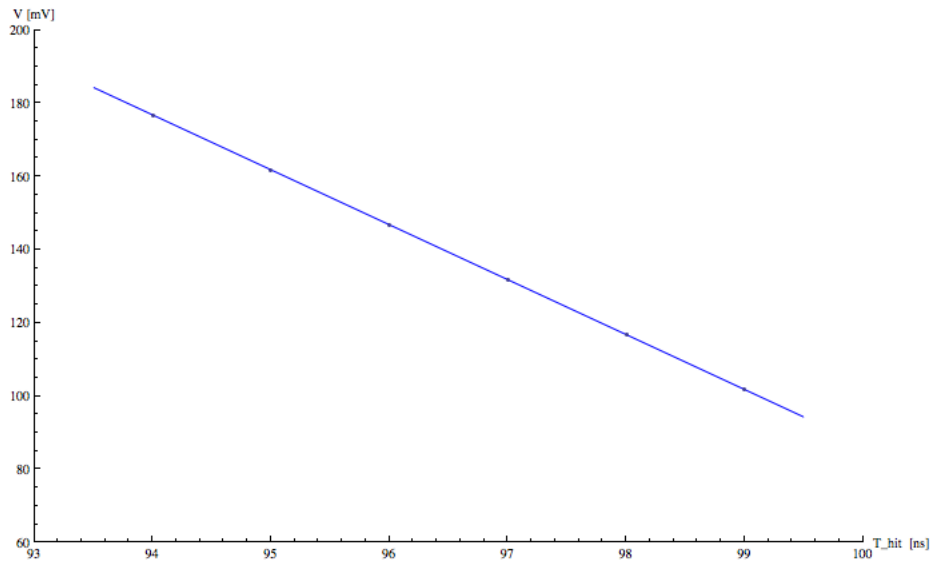

Figure 5.29: Fit of the TDC linearity in the discharging process

The fit goodness is:

$$Err = \left(\sum_i \left| \frac{(T_{th})_i - (T_{exp})_i}{(T_{th})_i} \right| \right) * 100 = 0.02\% \tag{5.20}$$

Therefore we can conclude that the discharging process is linear.

For the recharging process we need to measure if each recharging ramp has a linear behavior. In Figure 5.30 is reported just one ramp as an example.

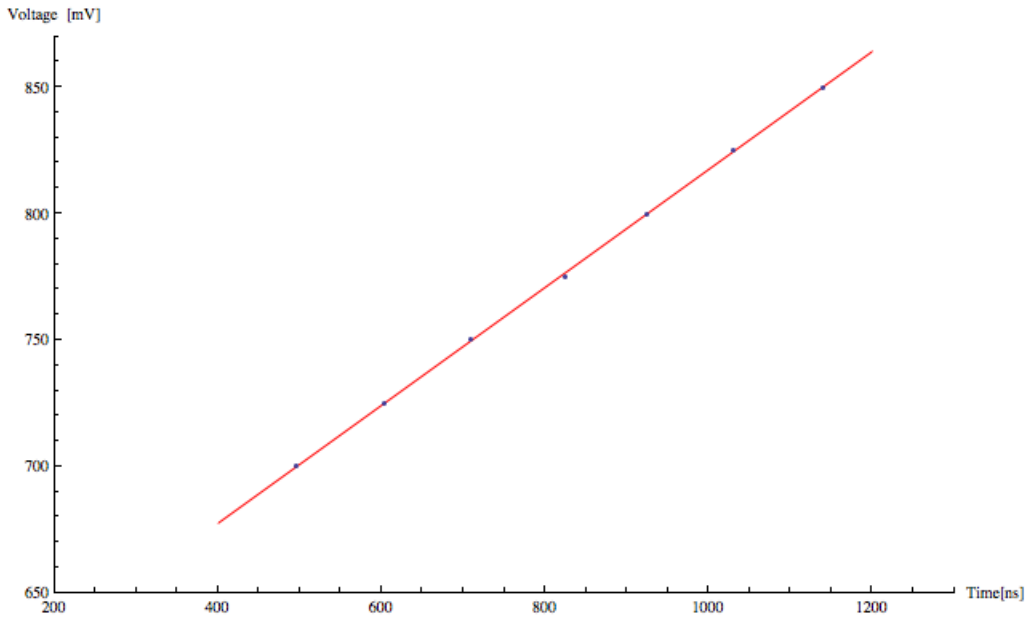

Figure 5.30: Fit of the TDC linearity in the charging process

The goodness for the other cases in each fit is reported in this table:

T_hit	Fit goodness(%)
99	0.021
98	0.025
97	0.030
96	0.005
95	0.008
94	0.011

So we can conclude that the TDC is linear since both processes are.

As introduced in chapter 3 the analog TDC is a slow component. For this reason we change a little the current source adding another branch with a multiplicity 15 in other to have a currents ratio equal to 16. In this way the discharging and so the recharging processes are faster. To understand if this is a good solution we measure the recharging process linearity and the fit goodness are reported below:

T_hit	Fit goodness(%) 16x
99	0.015
98	0.013
97	0.030
96	0.006
95	0.034
94	0.060

Now we know that the TDC has a linear behavior but it is necessary to understand if this linearity is kept for different conditions. In particular we studied how it behaves for different temperatures. To do this analysis we use a counter, that measure the number of clock pulses between the time when the switch number 1 is open and the time when the ramp reaches the baseline value. We change the temperature from 0 °C to 125 °C and the ramp variations are show in Figure 5.31:

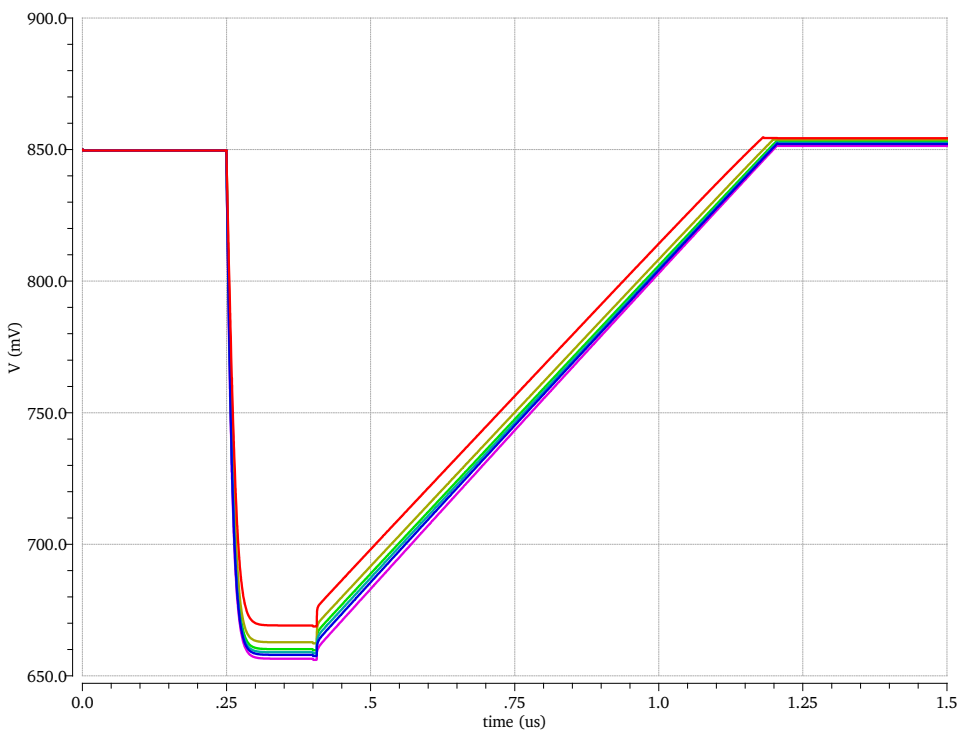

Figure 5.31: TDC response for different temperature

The comparator measures are reported in the following table

Temperature (°C)	Counter value
0	0010111101
25	0011000000
50	0011000001
75	0011000001
100	0011000001
125	0011000001

As we can see in the table from 50 °C to 125 °C the counter has the same output, for 25 °C the value differs only for one count but this difference is exactly the LSB. For the 0 °C the value differs for 3LSB but this is not an issue because the circuit works at room temperature. So we can say that the circuit is temperature insensitive. This is an important result because as we can see in Figure 5.31 the C_1 voltage value is not the same for each temperature involving that the charge I_1 changes with the temperature. However the charge I_2 changes too and since they are generated by the same currents source, this variation is compensated so the net measurement is insensitive to the temperature.

The last analysis which we have done are the corners analysis to see how linearity changes. For the FF case the ramp is show in Figure 5.32

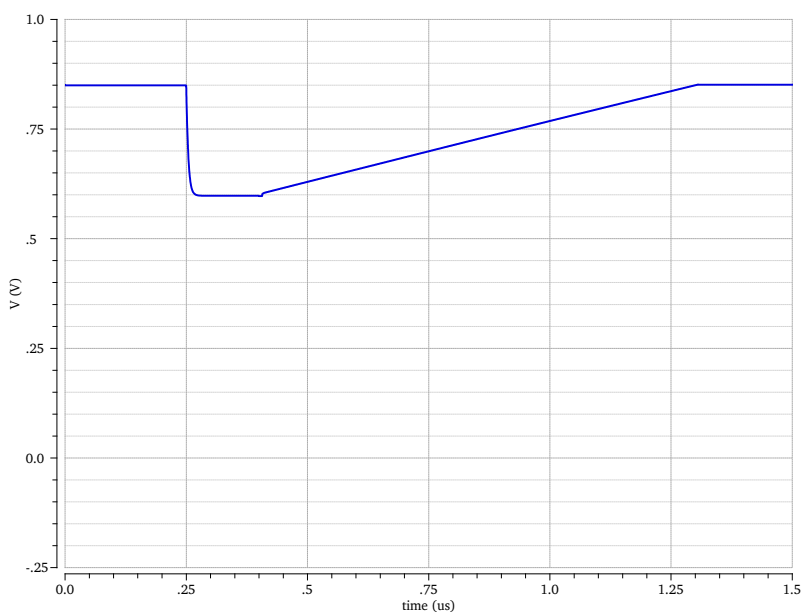

Figure 5.32: TDC output for the FF case

As we can see the linearity is maintained and it has a good behavior. For the SS case as we can see in Figure 5.33, the linearity is not very good because the recharging ramp bends near the baseline value.

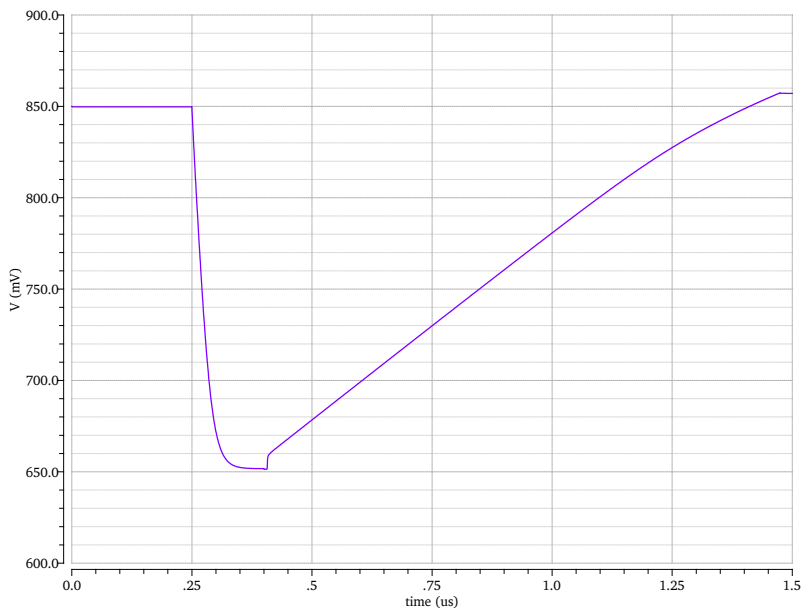

Figure 5.33: TDC output for the SS case

This means that the DC bias point needs to be adjusted.

Conclusion

In this work we have studied the possibility of reading out microstrip detectors with a fast time based readout. The work was done in the context of the $\overline{P}$ANDA experiment, which is now under construction at the new FAIR facility at GSI. In $\overline{P}$ANDA, microstrip sensors are used to equip two barrel layers and the outer part of two forward disks in the Micro Vertex Detector (MVD).

The baseline architecture for the chip is based on the Time over Threshold. This method consists in extracting the charge information from the width of the output signal of a leading edge comparator that follows the front-end amplifier.

It is an attractive solution because has a low power consumption and can fit in a small area. However the strip must be very fast to avoid pileup. Therefore the front-end signal must be adequately short and the system clock resolution of 160 MHz may not provide adequate charge resolution. Hence it is necessary to measure the duration of the comparator signal with Time to Digital Converter. This building block is the focus of this thesis.

As a starting point, we have analyzed different TDC architectures and we have chosen one based on analog interpolators because it combines small area and power with enough resolution for our purpose. In addition, a similar design has already been developed in a $0.13\,\mu m$ technology in the framework of a medical physics application.

Based on this previous experience, we have studied the adaptation of this concept to the $\overline{P}$ANDA environment.

Furthermore, we have ported the design to a new $0.11\,\mu m$ CMOS technology which offers a significantly lower cost. To study this circuit we use the CAD program which allows us to design the circuit and to simulate its behavior.

The TDC is made by three building blocks: the current generator, which generates two related currents, the Time to Amplitude Converter (TAC) and the Wilkinson ADC to convert the analog signal in a digital word. The first analysis which we have done is the Montecarlo simulation to understand if the current source has the desired properties when implemented in the new technology.

Since we had the circuit trend in the old technology, we compared ours results with the old ones and we could see that the new technology has even better

performance.

The other studies aim at verifying if the circuit works matching with the desired specifications. First of all we have studies the output resistance of the current source.

For the first current no particular issues were found. For the second one we noticed that some optimization is required in one of the process corner. The Time to Amplitude Converter was also designed. This required to optimize a low-power cascode amplifier. One of the characteristics of deep sub-micron technologies is the degraded output conductance. Therefore obtaining large gains is not trivial even if cascode configurations are used. A careful selection of transistor sizing and bias point was necessary to achieve a DC gain below 1.000 in all the process corners, which guarantee the desired 9 bit resolution in the TDC.

The linear behavior was carefully checked for all the blocks, as well as the performance at different temperatures. This was done by simulating a full conversion cycle while changing the temperature. In the range 0-125 °C the full scale range of the TDC changes by at most 3 LSB. This is not a major issues, because the circuit will work in the experiment at a constant temperature, maintained between 25 and 30 °C by a suitable cooling system.

Some degradation of the linearity has been observed in one of the process corner, but it can be recovered of a suitable adjustment of one reference voltage.

The performance globally obtained so far from this building block are satisfactory and now shop stopper was found that could compromise its use in the intended application.

The future work should concentrate in making the circuit more robust to process fluctuations.

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