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Low-Power High Dynamic Range Front-End Electronics for the Hybrid Pixel Detectors of the $\overline{\text{P}}$ ANDA MVD

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*In memory of the Tamils who have lost their life
during the Genocide committed by the Sri Lankan government.*

Abstract

ToPix is the ASIC for the readout of the hybrid pixel sensors of the $\overline{\text{P}}\text{ANDA}$ (antiProton ANnihilation at DArmstadt) Micro Vertex Detector (MVD). The $\overline{\text{P}}\text{ANDA}$ experiment, foreseen at the new FAIR facility at GSI, Darmstadt, will investigate the physics of strong interaction and the hadron structure, acquiring understanding of the mechanism of hadron mass generation, quark confinement and probing the existence of glueballs and hybrids. The MVD is the closest detector to the interaction point and its inner layers will be equipped with hybrid pixel sensors. The $\overline{\text{P}}\text{ANDA}$ detector is triggerless and all the data have to be readout. In addition, high track density, low material budget and mechanics constraints have concurred to the choice of a custom solution for the front-end chip. The ASIC is designed in a CMOS $0.13\ \mu\text{m}$ technology with a power supply of 1.2 V. The readout architecture is based on the Time-over-Threshold technique which allows to combine low-power charge measurement with high dynamic range. In fact, one peculiarity of the $\overline{\text{P}}\text{ANDA}$ pixels with respect to previous developments is that they will contribute also to particle identification with specific energy loss measurements. The front-end has been designed to process input charges up to 50 fC, with a dynamic range of 11 bits with respect to the noise floor. Each cell, in an area of $100\ \mu\text{m} \times 100\ \mu\text{m}$ embeds the analog and digital electronics necessary to amplify the detector signal and to digitize the charge information. The cells are arranged in columns which are readout and controlled by a peripheral logic. In the thesis, the ASIC architecture is described and the results obtained on the first two prototypes are discussed. From the gained experience the final version of the readout has been designed. The analog building blocks are discussed in detail, focusing the attention on the main design challenges. The most significant simulation results are presented, selecting from the large set of simulations performed to check the circuit reliability for different working conditions. The specific contribution of this work has been in the definition of the overall architecture and in the design of the front-end cell. In this context, a novel baseline restorer which occupies a minimum silicon area and is able to compensate sensor leakage currents up to 50 nA without affecting the quality of the charge measurement has also been developed.

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Chapter 1

The $\overline{\text{P}}\text{ANDA}$ experiment

1.1 Introduction

$\overline{\text{P}}\text{ANDA}$ (antiProton ANnihilation at DArmstadt) is an experiment planned at the future international Facility for Antiproton and Ion Research (FAIR), an extension of the existing Center for Heavy Ion Research (Gesellschaft für Schwerionenforschung (GSI)) in Darmstadt, Germany. $\overline{\text{P}}\text{ANDA}$ will investigate the physics of strong interaction and the hadron structure, acquiring understanding of the mechanism of hadron mass generation, quark confinement and probing the existence of glueballs and hybrids.

The experiment will perform several measurements of antiprotons interactions with protons and nuclei in a fixed target setup, in order to collect high-quality data that allow a precise test of the Quantum Chromodynamics (QCD) between the perturbative and non-perturbative regime. An antiproton beam in the momentum range of $1.5 \text{ GeV}/c - 15 \text{ GeV}/c$ gives access to a center of mass energy range from $2.2 \text{ GeV}/c^2$ to $5.5 \text{ GeV}/c^2$ in $p - \bar{p}$ annihilations. The key ingredient of the experiment is the high quality beam of anti-protons provided by the High Energy Storage Ring (HESR), in terms of intensity ($L \lesssim 2 \times 10^{32} \frac{1}{\text{cm}^2 \text{s}}$) and momentum resolution ($\delta p/p \sim 10^{-5}$).

The $\overline{\text{P}}\text{ANDA}$ collaboration, composed of more than 450 scientist from 17 countries, is engaged in the research and development activities for the general purpose $\overline{\text{P}}\text{ANDA}$ detector. All components have to be carefully designed and tuned in order to enable the multi-purpose physics program. Large scale simulation studies are being performed to validate the performance of all individual detector components and guide the detector optimization. A detailed report on the physics accessible at $\overline{\text{P}}\text{ANDA}$ with the expected performance has been published [1]. The experiment is planned to start its operation in 2018.

1.1.1 The Standard Model of particle physics

The elementary particles and their interactions are described by a quantum field theory, the Standard Model of particle physics [2] [3] [4]. The current formulation was developed in the 1970s, and over the time it has become established as a well tested physics theory, explaining a wide variety of experimental results and giving successful high precision predictions. The standard model is not the complete theory of fundamental interactions since it does not incorporate the physics of gravitation.

The fundamental particles that make up the matter can be organized in two groups, the quarks and the leptons. They are point like particles with $\frac{1}{2}\hbar$ spin, elementary fermions, divided into three generations. In the first generation there are the lightest and most stable particles. In the second and third generations there are the heaviest and less stable particles. All stable matter in the Universe is made from particles that belong to the first generation, any heavier particles quickly decay into lower-generation particles by means of weak interactions.

Leptons

There are 6 types of leptons with the corresponding antileptons (Tab. 1.1). The antileptons have the same mass but the leptonic number and the electric charge have equal magnitude with opposite sign of their respective leptons. The charged leptons are electron-like particles, the neutral leptons are known as neutrinos. Leptons are subject to the weak interaction. In the Standard Model, leptonic family number would be preserved if neutrinos were massless. However, neutrino oscillation experiments have shown that neutrinos do have mass. Mass terms for the neutrinos can be added to the standard model by hand. This has implication in the conservation of individual lepton number, making it an approximate law.

Quarks

There are 6 types of quark with the corresponding antiquarks (Tab. 1.2). All quarks have a flavor quantum number: the isospin third component (I_3) in u and d quarks, the strangeness (S) in s quarks, the charm (C) in c quarks, the bottomness (B') in b quarks, and topness (T) in t quarks. The convention is that the flavor of a quark has the same sign as its electrical charge, which is given by the generalized Gell-Mann-Nishijima formula in units of elementary charge e : $Q = I_3 + \frac{1}{2}(B + S + C + B' + T)$. Where B is the baryon number. The antiquarks have the same mass but the flavor, the electric charge and the baryon number have equal magnitude with opposite sign of their respective quarks. The quarks carry color charge and for this reason they are subject to the strong interaction. Quarks are subject also to the weak interaction.

Gen.	Particle		Charge [e]	Family number	Mass [MeV/c^2]
I	electron	e^-	-1	$L_e = +1$	$0.511 \pm 13 \cdot 10^{-9}$
	anti-electron	e^+	$+1$	$L_e = -1$	
	electron neutrino	ν_e	0	$L_e = +1$	$\leq 2 \cdot 10^{-6}$
	electron anti-neutrino	$\overline{\nu}_e$	0	$L_e = -1$	
II	muon	μ^-	-1	$L_\mu = +1$	$105.66 \pm 4 \cdot 10^{-6}$
	anti-muon	μ^+	$+1$	$L_\mu = -1$	
	muon neutrino	ν_μ	0	$L_\mu = +1$	≤ 0.19
	muon anti-neutrino	$\overline{\nu}_\mu$	0	$L_\mu = -1$	
III	tau	τ^-	-1	$L_\tau = +1$	1776.82 ± 0.16
	anti-tau	τ^+	$+1$	$L_\tau = -1$	
	tau neutrino	ν_τ	0	$L_\tau = +1$	≤ 18.2
	tau anti-neutrino	$\overline{\nu}_\tau$	0	$L_\tau = -1$	

Table 1.1: The 6 leptons (l) and 6 anti-leptons (\bar{l}) of the Standard Model [5]. All leptons have spin $\hbar/2$. Leptons carry lepton number $L=+1$ and anti-leptons carry lepton number $L=-1$.

Gen.	Particle		Charge [e]	Flavor	Mass [MeV/c^2]
I	up	u	$+2/3$	$I_3 = +1/2$	$2.49^{+0.81}_{-0.79}$
	anti-up	\bar{u}	$-2/3$	$I_3 = -1/2$	
	down	d	$-1/3$	$I_3 = -1/2$	$5.05^{+0.75}_{-0.95}$
	anti-down	\bar{d}	$+1/3$	$I_3 = +1/2$	
II	strange	s	$-1/3$	$S = -1$	101^{+29}_{-21}
	anti-strange	\bar{s}	$+1/3$	$S = +1$	
	charm	c	$+2/3$	$C = +1$	1270^{+70}_{-90}
	anti-charm	\bar{c}	$-2/3$	$C = -1$	
III	bottom	b	$-1/3$	$B' = -1$	4190^{+180}_{-60}
	anti-bottom	\bar{b}	$+1/3$	$B' = +1$	
	top	t	$+2/3$	$T = +1$	$(172.0 \pm 0.9 \pm 1.2) \cdot 10^3$
	anti-top	\bar{t}	$-2/3$	$T = -1$	

Table 1.2: The 6 quarks (q) and 6 anti-quarks (\bar{q}) of the Standard Model [5]. All quarks have spin $\hbar/2$. Quarks carry baryon number $B = +1/3$ and anti-quarks baryon number $B = -1/3$.

Force carriers

The fundamental fermions build up matter, but their properties are given by their interactions through the exchange of gauge bosons (Tab. 1.3), point like particles with integer spin in units of \hbar . In accordance with the energy-time uncertainty principle, $\Delta E \cdot \Delta t \geq \hbar$, a particle of mass $M = \Delta E/c^2$ can exist as part of an intermediate state for a time Δt . From the mass of the force carrier boson it is

possible to calculate the maximum interaction range $\hbar c/Mc^2$.

Force	Particle		Mass [MeV/c ²]	Range [fm]	Timescale [s]
Electromagnetic	photon	γ	0	∞	$\sim 10^{-16} \div 10^{-21}$
Weak	Z boson	Z^0	91.1876 ± 0.0021	$\sim 10^{-3}$	$\sim 10^{-6} \div 10^{-13}$
	W boson	W^\pm	80.399 ± 0.023		
Strong	gluon	g	0	~ 1	$\sim 10^{-22} \div 10^{-24}$

Table 1.3: Force carriers [5].

The photon is the force carrier for the electromagnetic interaction between electrically charged particles. It has no rest mass and allows for interactions at long distances. The phenomena involving the electromagnetic interaction is described in the theory of Quantum Electrodynamics (QED).

The weak interaction is mediated by three heavy bosons. Two types of W bosons, the W^+ with an electric charge of $+1e$, its antiparticle the W^- with an electric charge of $-1e$, and the electrically neutral Z^0 boson. The weak interaction acts on the flavor of the particles, and it is the only force that can violate the flavor conservation. The high masses of the weak interaction bosons limit the range of the weak force at $\sim 10^{-18}$ m.

The strong interaction is carried by massless particles called gluons and couples to the color charge of the particles. There are eight independent gluons (color octet), they carry color charge which means that they can interact among themselves. For this reason, even if the gluon is a massless particle, the strong force has a range about 10^{-15} m. The strong force is described in the theory of the Quantum Chromodynamics (QCD).

Symmetries

There are three symmetries that plays an important role in the Standard Model:

- Parity, under the space reflection (P). This operation reverses the momentum of a particle, but conserves the direction of its spin. The system has an even parity ($P = +$) if the spatial part of its wave function is symmetric under the parity operation. The system has an odd parity ($P = -$) if it is antisymmetric under the parity operation. For a composite system, the parity is given by the parity of its constituents: $P = P_1 P_2 (-1)^L$.
- C-parity, under the charge-conjugation transformation (C). This operation transform particles in antiparticle and vice versa, conserving the direction of the spin. Only those systems where all quantum charges and magnetic moment are neutral, are eigenstates of charge parity. For a system of free particles, the

C parity is the product of C parities for each particle. For bosons it is given by $C = (-1)^L$, while for fermions it is given by $C = (-1)^{L+S}$. Where L is the angular momentum of the composite system and S is the spin.

- T-parity, under the time reflection (T). This operation changes the direction of time, but keeps all other quantities conserved. A system that remains unchanged by this operation is said to be time-reversal invariant.

The CPT invariance is a fundamental symmetry of physical laws under transformations that involve the inversions of charge, parity, and time simultaneously. When all these are performed simultaneously, the resultant process or interaction is indistinguishable from the original. The CP violation, is the violation of the combined conservation laws associated with charge conjugation and parity by the weak force. In this case also the T symmetry is violated allowing for the preservation of CPT symmetry.

1.1.2 The quark model of hadrons

The hadrons are composite particles made of quarks bound by the strong interaction mediated by gluons. The ordinary hadrons are classified according to the quark model [6], a classification scheme derivable from the theory of quantum chromodynamics. The hadrons are described in terms of their valence quarks which determine the quantum numbers of the hadrons. In addition to that the hadrons contain also virtual quark-antiquark pairs known as sea quarks. Although quarks also carry color charge, hadrons must have zero total color charge because of a phenomenon called color confinement. Hadrons have a physical size, with a radius of $\sim 10^{-15}$ m. Since hadrons are composed of quarks, they participate in both the weak and strong interactions. Hadrons with net electric charge also participate in the electromagnetic interaction. All free hadrons except the proton and antiproton are unstable. The mass of a hadron is two orders of magnitude larger than the sum of the masses of the valence quarks. The main contribution to hadron mass comes from the kinetic energy of the interacting quarks and gluons. The mass of the hadrons is not described by the standard model and it could be calculated by using phenomenological models. Hadrons have excited states known as resonances. Each ground state hadron may have several excited states where the quark content is the same, but the dynamics of the quarks are different and this explains the difference in mass, spin and other quantum numbers. Resonances decay extremely quickly ($\lesssim 10^{-23}$ s) via the strong nuclear force.

Baryons

Baryons are hadrons with baryon number $B = 1$. The known baryons are made of three valence quarks (qqq). Baryons are fermions since they have an odd number of quarks and consequently an odd half-integer spin. Baryons are color neutral particles, since the three quarks have different colors. Each baryon has a corresponding antiparticle (antibaryon) where quarks are replaced by their corresponding antiquarks. Baryons are classified into six groups according to the number of quarks belonging to the first generation (u and d) and their isospin (I):

- Nucleons (N), with three first generation quarks and $I = 1/2$.
The nucleons are best known for constituting atomic nuclei. The proton (p) is made of 2 up quarks and 1 down quark, has electrical charge 1 e , and a mass of 938.3 MeV/ c^2 . The proton is the only stable baryon. The neutron (n) is made of 2 down quarks and 1 up quark, has 0 electrical charge, and a mass of 939.6 MeV/ c^2 . Free neutron decays through weak interaction in protons $n \rightarrow p + e^- + \overline{\nu}_e$ with a mean lifetime of 14.8 minutes. Neutrons within a nucleus are stable, since it is energetically impossible for them to decay within a stable nucleus.
- Delta (Δ), with three first generation quarks and $I = 3/2$.
The Δ family consists of four different particles distinguished by their electrical charges specified in the superscript: Δ^{++} (uuu), Δ^+ (uud), Δ^0 (udd), Δ^- (ddd). They all have nearly the same mass (1232 MeV/ c^2). Deltas could be treated as the same particle and the difference in charge being due to the particle being in different isospin projection state. In the quark model, the Deltas can be thought of as the excited states of the nucleons.
- Lambda (Λ), with two first generation quarks and $I = 0$.
They contain an up quark, a down quark, and a third heavier quark: strange quark in Λ^0 , charm quark in Λ_c^0 and bottom quark in Λ_b^+ .
- Sigma (Σ), with two first generation quarks and $I = 1$.
They contain any combination of two up and down quarks, and a third heavier quark. If the third quark is not a strange quarks its identity is given by a subscript (Σ , Σ_c , Σ_b). The superscript identifies the electrical charge.
- Xi (Ξ), with one first generation quark and $I = 1/2$.
They contain one up or down quark and two heavier quarks. One or two subscripts are used if one or both of the remaining quarks are heavy and non strange. For example the Ξ_b^- is made of down, strange and bottom quarks with a charge of -1e.

- Omega (Ω), with no first generation quarks and $I = 0$.

The lightest Omega baryon is Ω^- which contains three s quarks. Subscripts indicate any heavy quark content and the superscript the charge.

A baryon that decays strongly has its mass expressed in MeV as part of its name.

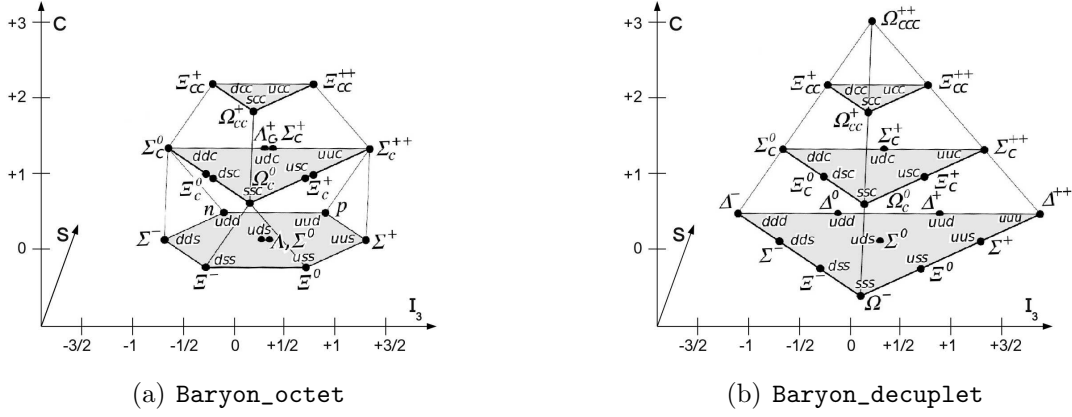


Figure 1.1: SU(4) multiplets of baryons made of u , d , s , c quarks [5]. (a) The 20-plet with an SU(3) octet, (b) The 20-plet with an SU(3) decuplet.

Mesons

Mesons are hadrons with baryon number $B = 0$. The known mesons are made of one valence quark and one valence antiquark ($q\bar{q}$). Mesons are bosons since they have an even number of quarks and consequently an integer spin. For this reason they can act as force mediating particles on short distances playing a part in the nuclear interaction processes. Mesons are color neutral particles since a quark of one color and an antiquark carrying the corresponding anticolor. Each meson has a corresponding antiparticle (antimeson) where quarks are replaced by their corresponding antiquarks and vice-versa. All mesons are unstable, with the longest-lived lasting for only 10^{-8} s. Mesons are also typically less massive than baryons, meaning that they are more easily produced in experiments.

The $q\bar{q}$ system description is based on the atomic spectroscopy notation. There is a principal quantum number for radial excitation n , orbital angular momentum L , spin S and overall spin J . The spin of the system made of one fermion and one antifermion is 0 (antiparallel spin) or 1 (parallel spin) in units of \hbar . The overall spin is $\vec{J} = \vec{S} + \vec{L}$, allowing the states in the range $|L - S| \leq J \leq |L + S|$. If we neglect the weak interactions of quarks, then parity is a good quantum number. If a quark and an antiquark are in a bound state with orbital angular momentum L ,

then the state has parity $P = (-1)^{L+1}$. If the quark and antiquark have the same flavor, the state is neutral with a charge conjugation parity $C = (-1)^{L+S}$. The constituent quark model restricts the accessible meson quantum numbers to a set of allowed J^{PC} combinations. Mesons are classified in J^{PC} multiplets. The $L = 0$ states are the pseudoscalar meson ($J^P = 0^{-+}$) and the vector meson ($J^P = 1^{--}$). The $L = 1$ states are the scalar meson ($J^P = 0^{++}$), pseudovector meson ($J^P = 1^{++}$ and $J^P = 1^{+-}$), and the tensor meson ($J^P = 2^{++}$).

The meson nomenclature depends on their flavor, quark content, isospin (I), total angular momentum (J), parity (P) and C-parity (C):

- Light unflavored mesons, $I = 1$. They are composed of first generation quarks, they form an isospin triplet state and the third component isospin equal to charge of the particle ($I_3 = +1, 0$ or -1). The Pi mesons (π or Pion) are the lightest mesons and they have total spin $J = 0$. The π^0 is the combination of quark and antiquark of the same flavor $\frac{1}{\sqrt{2}}(u\bar{u} - d\bar{d})$, the π^+ is made of $u\bar{d}$ and π^- is made of $\bar{u}d$. Pions play an important role in explaining the low energy properties of the strong nuclear force. The Rho meson is a short lived hadronic particle, with the same quark content of the Pi meson and total spin $J = 1$. The isospin triplet states are denoted as ρ^+ , ρ^0 , ρ^- .
- Light unflavored neutral mesons, $I = 0$. The eta (η) and eta prime meson (η') are mesons made of a mixture of up, down and strange quarks and their antiquarks. The η composition is $\frac{1}{\sqrt{6}}(u\bar{u} + d\bar{d} - 2s\bar{s})$ and the η' composition is $\frac{1}{\sqrt{6}}(u\bar{u} + d\bar{d} + 2s\bar{s})$. The omega meson (ω) is a neutral vector meson $\frac{1}{\sqrt{2}}(u\bar{u} + d\bar{d})$. The phi meson (ψ) is a neutral vector meson formed of a strange quark and a strange antiquark ($s\bar{s}$).
- Quarkonia are mesons formed from a quark and the corresponding antiquark. The charmonium ($c\bar{c}$) is a bound state of a charmed quark and antiquark. The charmed eta meson (η_c) is the lightest charmonium state, the J/Ψ is the first excited state of charmonium. The bottomonium ($b\bar{b}$) is a bound state of a bottom quark and antiquark. The bottom eta meson (η_b) is the lightest charmonium state, the Upsilon (Υ) is the first excited state of bottomonium. The top quark is too heavy to form a similar meson due to its very fast decay.
- Flavorful mesons are mesons made of pair of quark and antiquarks of different flavors. The main symbol depends on the heavier quark, the superscript depends on the charge, and the subscript depends on the lighter quark. The K-meson (kaon) contains a strange quark (or antiquark), paired with an up or down antiquark (or quark). The D mesons are the lightest particle containing charm quarks, paired with an up or down or strange antiquark. B mesons are composed of a bottom antiquark and either an up (B^+), down

(B^0), strange (B_s^0) or charm antiquark (B_c^+). The combinations with top quark is not thought to be possible because of the top quark's short lifetime.

For states with spin parity in the normal series ($J^P = 0^+, 1^-, 2^+, 3^-, \dots$) a superscript * is added.

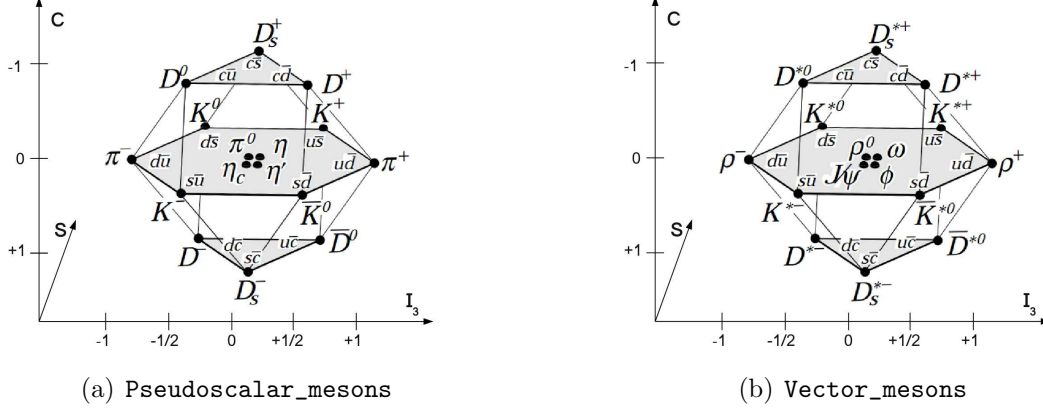


Figure 1.2: SU(4) weight diagram showing the 16-plets for the pseudoscalar (a) and vector meson (b) made of the u , d , s and c quarks as a function of isospin I , charm C and strangeness S [5]. The nonets of light mesons occupy the central planes to which the $c\bar{c}$ states have been added.

Exotics

The structure of hadrons is more complicated than the quark model reveals. The full quantum mechanics wave function of any hadron must include virtual quark pairs as well as virtual gluons. Apart from the conventional mesons and baryons, QCD also allows for states with an explicit gluonic component. Exotic hadrons are hypothetical color neutral particles made of quarks and gluons, not predicted by the quark model.

Exotic hadrons can be searched for by looking for particles with quantum numbers forbidden to ordinary hadrons. Other exotic may have coinciding quantum number of ordinary hadrons but different valence structure (hidden exotic hadrons). The hypothetical exotic hadrons are:

- Tetraquarks ($q\bar{q}q\bar{q}$), hypothetical mesons composed of two valence quark antiquark pairs. It can be thought of as a bound state of two mesons quark constituents.
- Pentaquarks ($qqqq\bar{q}$), hypothetical baryons composed of four valence quarks and one valence antiquark. It can be thought of as a bound state of a baryon and a meson quark constituents.

- Dibaryons ($qqqqqq$), hypothetical particles that would consist of six quarks of any flavors.
- Hybrid mesons ($q\bar{q}g$), composed of one valence quark, one valence antiquark and one more gluons.
- Hybrid baryons ($qqqg$), composed of three valence quarks as well one or more gluons.
- Glueballs (gg), compounds of gluons with no valence quarks at all. This state is possible because gluons carry color charge and experience the strong interaction.

1.1.3 Asymptotic freedom and color confinement

The QCD describes the strong interaction through the exchange of gluons between particle carrying color charge. Figure 1.3 shows Feynman diagram for the exchange of a gluon with momentum Q between two quarks, on the basis of the color charge of the quark, this exchange results in an attraction or a repulsion between both quarks. The strength of this interaction is proportional to a factor $g^2 = 4\pi\alpha_s$, each one of the two vertices where the gluon and the quark get in touch contributes a factor of g . The factor α_s is the strong interaction coupling constant, which varies with the gluon momentum Q . This is reflected by the dependence of the strong coupling constant as function of the distance between interacting objects.

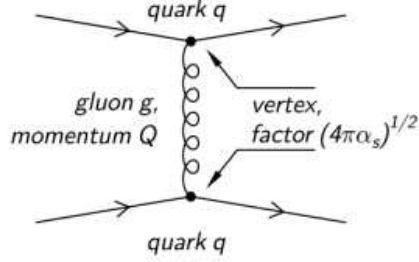


Figure 1.3: Strong interaction.

Figure 1.4(a) shows the relationship between the coupling constant α_s and the distance of the strong interacting objects. For small distance interaction, where the energy of the exchanged gluon is high, the coupling constant is small. This phenomena is called asymptotic freedom [7], and it means that quarks are nearly free. QCD is well understood at short distance scales, it is possible to apply the perturbation theory obtaining high precision quantitative predictions. Increasing the interaction distance, thus decreasing the energy of the exchanged gluon, the coupling constant increases. The QCD field equations are non-linear, since the gluons that mediate the interaction carry color charge, and hence interact among themselves. As the coupling constant rises, QCD becomes a strongly-coupled theory, a different theoretical approach is required since the perturbative expansions diverge. A non-perturbative approach to solve numerically the QCD in the strong coupling regime

is the Lattice QCD, where the calculation is performed on a discretized space-time grid.

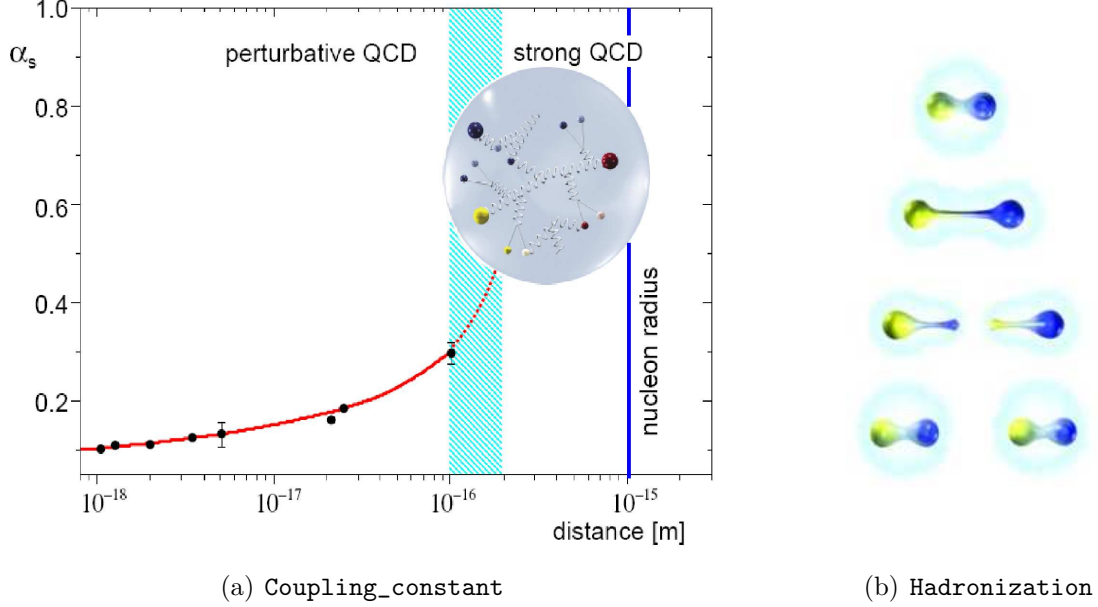


Figure 1.4: (a) Coupling constant of the strong interaction α_s as a function of distance. The data points represent experimental values [5]. The transition region between perturbative QCD and strong QCD is highlighted in light blue. (b) Hadronization process: when a quark antiquark pair is separated two pairs are created.

For distances between quarks comparable to the nucleon size (~ 1 fm) the interaction becomes so strong that quarks cannot be further separated and hadrons are formed. This phenomena is called color confinement, this means that color charged particles quarks never appear in isolation, they are always confined in compound systems which extend over distances of about 1 fm.

If a quark is moved away from a quark compound system, the binding force strengthens until becomes energetically favorable the formation of a new antiquark from the vacuum which couples with the quark allowing the separation. This process is called hadronization and it is depicted in Figure 1.4(b). There is no analytic proof that shows why the quantum chromodynamics should be confining, and the hadronization is one of the least understood processes in particle physics.

1.2 $\overline{\text{P}}\text{ANDA}$ experimental program

The $\overline{\text{P}}\text{ANDA}$ experiment, equipped with a general purpose detector, will perform precise measurements of antiproton-proton annihilations and interactions of antiprotons with nuclei in a fixed target setup. The $\overline{\text{P}}\text{ANDA}$ experimental program includes various topics related to the properties of the strong interaction, extending from the test of fundamental symmetries to the investigation of QCD. Special attention will be given to the study of strange and charmed quarks, in the transition regime between the perturbative QCD at short scales and strong QCD, providing a link between nuclear and hadron physics. Many measurement are foreseen in order to achieve significant progress thanks to the precision of the data and improvement in statistics.

The key feature of the experiment is the availability of high-intensity ($L \lesssim 2 \times 10^{32} \frac{1}{\text{cm}^2 \text{s}}$), cooled antiproton beams ($\delta p/p \sim 10^{-5}$) of the High Energy Storage Ring (HESR) in a momentum range between 1.5 GeV/c and 15 GeV/c. Such a beam gives access to a center of mass energy range from 2.2 GeV/c² to 5.5 GeV/c² in $p\overline{p}$ annihilations. Figure 1.5 shows the accessible mass range of hadrons at the $\overline{\text{P}}\text{ANDA}$ experiment in relation to the antiproton momenta required in the fixed target collisions. In this energy range the available experimental data are not sufficient, most of the data have been obtained with electromagnetic probes [8]. Experiments with antiprotons have proven to be a rich source of information in hadron physics [9]. At the Low Energy Antiproton Ring facility (LEAR) of CERN [10] the light meson mass region has been investigated with an antiproton beam momentum up to 2.2 GeV/c. With the accessible energy region at HESR it is possible to cover a broad range of studies:

- High precision spectroscopy of all charmonium states and search of exotic hadrons with gluonic excitation, for a quantitative understanding of the confinement part of the QCD potential.
- Investigation on the behavior of hadronic particles in nuclear matter for understanding the origin of hadron masses.
- Precise gamma ray spectroscopy of hypernuclei for extracting information on their structure and their interactions with nucleons.
- Studies of the proton structure by measuring Generalized Parton Distributions (GPDs), transverse parton distribution functions, and electro-magnetic form factors in the time-like region.

The key physics items will be briefly discussed in the following.

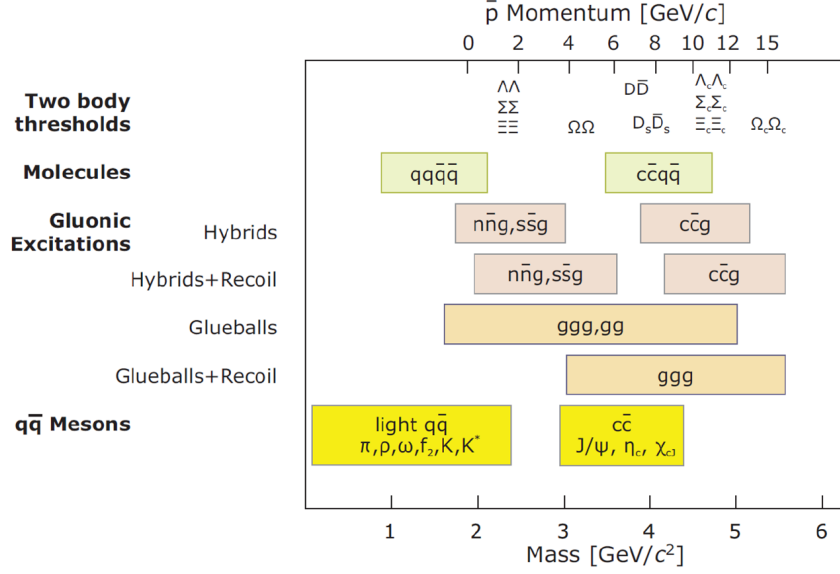


Figure 1.5: Mass range accessible at $\overline{\text{PANDA}}$ ($2.2 \text{ GeV}/c^2 - 5.5 \text{ GeV}/c^2$). The upper scale indicates the corresponding antiproton momenta required in a fixed target setup.

1.2.1 Hadrons spectroscopy

Charmonium states

The analysis of the strong interacting bound states plays a primary role in the quantitative understanding of QCD. A simple two body system is the meson, a bound state of strong interacting quark antiquark pair. Strong interaction is flavor independent, so in principle, all bound systems are suitable for the study of the QCD potential.

The light quarks (u, d, s) have small mass differences. The light mesons are mixtures of all these three flavors, and present strongly overlapping states with small spacing and large widths ($\Gamma \approx 200 \text{ MeV}$). Moreover given the high value of the strong interaction coupling constant ($\alpha_s \gtrsim 0.6$) it is not possible to use the perturbation theory, and the light quarks dynamics requires a relativistic approach. Heavy quarkonia are flavor neutral meson made of quark and the correspondent antiquark: charmonium $c\bar{c}$ and bottomonium $b\bar{b}$. Since charmonium has a net zero charm, it is referred as a hidden charm state. The states with a net charm are referred as open charm states. The larger mass difference between the charm, the bottom and the lighter quarks results in well defined states. Given the heavy mass of the c quark $m_c = 1270_{-90}^{+70} \text{ MeV}/c^2$, it is possible to describe the dynamical properties of the charmonium in terms of non relativistic potential ($\langle v^2/c^2 \rangle \approx 0.1 - 0.2$). In addition

to that, the coupling constant assumes a low value ($\alpha_s \approx 0.2 - 0.3$) allowing for the perturbative approach. The charmonium spectrum has energy levels described by an effective central potential. It is possible to extrapolate experimentally the coupling strength, and tune the potential models on the basis of spectroscopy measurement. Precision measurements of the mass and width of the charmonium spectrum are powerful tools to study the confinement potential in QCD.

The J/Ψ is the first charmonium state discovered in 1974 by two independent research groups, one at the Stanford Linear Accelerator Center (SLAC) and one at the Brookhaven National Laboratory (BNL). The earlier studies of charmonium states were performed in electron positron colliders. In the $e^+e^- \rightarrow \gamma \rightarrow c\bar{c}$ process, the directly formed states must have the quantum numbers of the intermediate virtual photon. For this reason the direct production is limited only to vector states $J^{PC} = 1^{--}$, the J/Ψ , Ψ' and $\Psi(3770)$ resonances. All the other states, like the charmonium ground state η_c with $J^{PC} = 0^{-+}$, cannot be formed directly and are studied through other production mechanism with a lower cross section.

In $p\bar{p}$ annihilations, states of all quantum numbers can be directly formed through the annihilation of the three quarks in the proton with the respective antiquarks in the antiproton. This lead to an higher charmonium production yield. The charmonium spectroscopy is performed accelerating the \bar{p} beam to the energy of the resonance, and then performing an energy scan with a fine tuning of the beam momentum. In the directly formed resonances of the charmonium state, the precision of the mass and width measurement depends only on the accuracy on the determination of the initial $p\bar{p}$ state energy, thus on the beam momentum spread. The detector is used to identify the final states and measure the formation rate for a given resonance.

The experiments E760 and E835 at Fermilab [9] have shown that it is possible to conduct a precise charmonium spectroscopy with a cooled antiproton beam. The charmonium spectroscopy was performed in the 2.9 GeV – 3.7 GeV energy range. Thus the charmonium states above the open charm threshold (at 3.73 GeV) were not explored. Fermilab experiments did not succeed in providing very good results for the total width of the charmonium ground state η_c and the singlet resonances. The main reason is the low statistics, in addition there was not a charged particle tracking system, and it was possible to detect only the electromagnetic reaction neglecting the charged hadron decays of any charmonium resonances.

Figure 1.6 shows the spectrum of charmonium states. The open charm threshold at 3.73 GeV is the energy required to produce a D and a \bar{D} . The D mesons are the lightest particle containing charm quarks, paired with an up or down or strange antiquark. There are eight narrow states below the open charm threshold. These states are theoretically and experimentally well established. Above the threshold several resonances are predicted but the experimental knowledge is poor. Above the $D\bar{D}$ threshold, the charmonium system is energetically allowed to decay into D and

conservation they cannot decay in $D\overline{D}$. New resonances have been found, but not all of them fit in the charmonium scheme. These states have been labeled as X, Y, Z states, with their mass in the bracket. Possible interpretation for these states are charmonium states, DD molecules or charmed hybrid states. One of the most established state in this energy range is the $X(3872)$ discovered by the Belle collaboration [12] in 2003 and later confirmed by several other collaborations. It has a mass of $m_{X(3872)} = 3872.3 \pm 0.8$ MeV with a small width $\Gamma_{X(3872)} = 3.0^{+2.1}_{-1.7} \pm 0.9$ MeV, the main hadronic decay modes are $\pi^+\pi^-J/\Psi$ and $D^0\overline{D}^0\pi^0$. The nature of this state is unclear and different theoretical interpretations have been proposed, such as the $D^0\overline{D}^{*0}$ molecule, and the 2^3P_1 1^2D_2 charmonium states. An accurate measurement of its width and decay modes are needed.

Panda aims to improve and extend the high precision measurements done at Fermilab. Its detector allows for a higher angular coverage, with the ability to detect both the electromagnetic and hadronic decay modes. $\overline{\text{PANDA}}$ will perform measurements on the entire charmonium spectrum, below and above the open charm threshold. Thanks to the small beam momentum spread ($\delta p/p \approx 10^{-5}$) it can study the spectrum with a resolution lower than 100 keV.

Hybrid mesons and glueballs

Gluonic excitations within a color neutral bound system are allowed by QCD, the gluons carry units of angular momentum proportional to their excitation, thus they contribute to total the quantum number of the bound system. Quantum numbers that are not allowed in the quark model for $q\overline{q}$ states could be reached by the additional gluonic degree of freedom. The mesons with gluonic excitations are called hybrid mesons ($q\overline{q}g$). QCD allows also for neutral bound state made entirely of gluons, the glueballs (gg or ggg). The properties of gluonic hadrons are determined by the long-distance features of the strong interaction. There are several experimental observation of gluonic hadrons candidates, but a clear identification of their quantum numbers for a precise theoretical interpretation is still missing. The experimental confirmation is very important for the understanding of dynamics of low energy QCD and the structure of QCD vacuum. $\overline{\text{PANDA}}$ will investigate the gluonic hadrons mass range with the high luminosity modality in order to observe the candidates states, then with a cooled antiproton beam high precision measurements will be performed in the interesting mass region. Finally, spin-orbit analysis and a fully exclusive reconstruction will be execute for the determination of the quantum numbers of the observed states.

The light hybrid mesons, constituted by u , d and s quarks are expected to have strongly overlapping states with wide resonances and to form mixing states with the ordinary hadrons. For these reasons their experimental investigation and clear identification are difficult. The hybrid state with a charm quark the charmed

hybrids, and in particular the charmonium like states ($c\bar{c}g$), are predicted to be narrower than the light hybrid mesons. The exotic charmonium states are expected in the $3 \text{ GeV}/c^2 - 5 \text{ GeV}/c^2$ mass range, fully accessible by $\overline{\text{PANDA}}$.

The gluon has two color-excitation modalities, the lower energetic mode is the Transverse Electric (TE) with axial quantum number $J^{PC} = 1^+$, the higher energetic mode is the Transverse Magnetic (TM) with axial quantum number $J^{PC} = 1^-$. Table 1.4 reports the total angular momentum due to a gluonic excitation of the $q\bar{q}$ states without angular momentum excitation. The gluon angular momentum coupling generates 8 states, 3 of them exhibits exotic quantum numbers forbidden for an ordinary meson. The observation of exotic states will be a clear signal of gluonic excitation. According to the prediction from LQCD the hybrid mesons with non exotic quantum numbers are identifiable from the ordinary mesons through their distinctive decay modes. The hybrid states with non exotic quantum numbers are important because they can be directly formed in $p\bar{p}$ annihilations, thus the precise measurement of their mass and width is possible.

$q\bar{q}$ state	Gluon excitation	
	1^- (TM)	1^+ (TE)
$^1S_0, 0^{-+}$	1^{++}	1^{--}
$^3S_1, 1^{--}$	$0^{+-} \leftarrow \text{exotic}$	0^{-+}
$^3S_1, 1^{--}$	1^{+-}	$1^{-+} \leftarrow \text{exotic}$
$^3S_1, 1^{--}$	$2^{+-} \leftarrow \text{exotic}$	2^{-+}

Table 1.4: Coupling of the gluon excitation with the ground $q\bar{q}$ state.

Experimental searches for bound states of gluons have produced only controversial signals. Since the $p\bar{p}$ annihilation is a gluon rich processes, in $\overline{\text{PANDA}}$ the glueballs could be formed directly or produced together with another particle.

Figure 1.7 shows the most reliable prediction of the glueball spectrum from Lattice QCD calculations [13]. The lightest glueball state $J^{PC} = 0^{++}$ has a mass of $\approx 1.7 \text{ GeV}^2$. The calculations are made without taking into account that the low energy glueball states have quantum numbers accessible also for ordinary mesonic states. In this case mixed states of glueball and meson are allowed, therefore altering the glueball mass spectrum. Mixed states will result in broad structures experimentally difficult to observe.

The region of ground state was investigated by LEAR, where a first indication for the tensor state $J^{PC} = 2^{++}$ around $2.2 \text{ GeV}/c^2$ was found [14], but there was not enough statistics for a reliable determination. Glueballs with exotic quantum numbers are called oddballs. Since they cannot mix with normal mesons they are predicted to present a narrow state and thus easy to find. The lightest oddball is

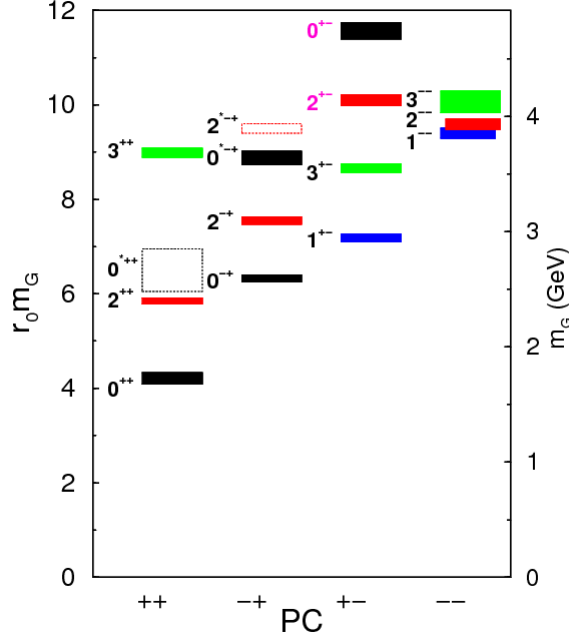


Figure 1.7: Glueball spectrum from lattice QCD calculations [13].

the state $J^{PC} = 2^{+-}$ with a mass of $4.5 \text{ GeV}/c^2$, another oddball accessible in the $\overline{\text{P}}\text{ANDA}$ energy range is the state $J^{PC} = 0^{+-}$.

D mesons

The D mesons are a heavy-light QCD bound system, containing a c quark and a lighter antiquark or vice versa. Given the large mass difference of the two components, according to the heavy quark limit approximation, the spin of the charm quark has a negligible effect on the mass of the system. The study of the D meson states gives information about the spin dependence of the quark antiquark potential at long distances.

There are four D mesons $J^P = 0^-$ ground states: D^+ ($c\bar{d}$), D^0 ($c\bar{u}$), \overline{D}^0 ($\bar{c}d$), D^- ($\bar{c}u$). The first excited states D^* have $J^P = 1^-$. The measurement of the D mesons ground state and their excitations are in good agreement with the quark model predictions.

The D_s states are strange charmed mesons. The ground states with $J^P = 0^-$ are D_s^+ ($c\bar{s}$) and D_s^- ($\bar{c}s$) mesons, the first excited states $D_s^{*\pm}$ have $J^P = 1^-$. Figure 1.8 shows the observed states and the comparison with the theoretical predictions. The ground state and the first state observation are compatible with the theoretical

prediction. In addition to that, two states above the D^*K threshold have been successfully identified, the $D_s(2536)$ with $J^P = 1^+$ and the $D_s(2573)$ with $J^P = 2^+$. Two narrow states have been observed at BaBar and CLEO [15], but their masses are in disagreement with the theoretical predictions. The $D_s^\pm(2317)$ with $J^P = 0^+$ is little below the DK threshold and $D_s^\pm(2460)$ with $J^P = 1^+$ is little below the D^*K threshold. The nature of these states is unclear, a precise measurement the widths and a determinations of the decay branching ratio is required in order to give a theoretical explanation.

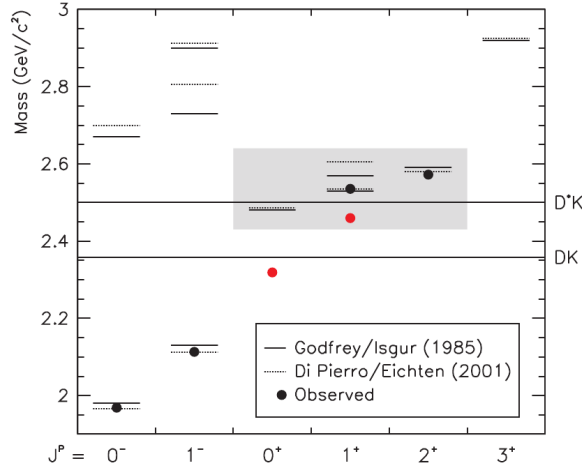


Figure 1.8: Theoretical predictions and experimental measurement of the D meson spectrum [15].

A \overline{p} beam momentum higher than 6.4 GeV/c allows for the production of D meson pairs. The production cross section of the D meson pairs close to the threshold is related to the masses and the widths of the respective D mesons. Thus with an energy scan close to the threshold values it is possible to calculate the width of the D meson states. A beam momentum spread of $\delta p/p \approx 10^{-5}$ allows for a resolution of ~ 100 keV.

The large D mesons production gives the possibility to observe rare decays. This allows to investigate physics aspects connected to the weak interaction probing the Standard Model. The study of the rare decays of the D mesons are important to probe symmetry violations. Lepton flavor number violations will be searched through decays like $D^0 \rightarrow \mu e$ or $D^\pm \rightarrow \pi \mu e$. The mixing of a particle with its antiparticle is a signal of CP violation. It has been well measured in the neutral K system and observed in neutral B meson decays [16]. The CP violation in the D^0 system is predicted small, and a large deviation from the prediction can be easily identified.

Baryon spectroscopy

The baryon spectrum is poorly understood. The agreement of the spectroscopy measurements with the quark model predictions is very small. Some of the low lying states are shifted, and there is no experimental validation for the prediction of the higher lying states. In $\overline{p}p$ collisions there is a large cross section for the production of a baryon antibaryon final state. With a \overline{p} beam momentum of 3 GeV/c there is an equal production rate of baryonic and mesonic final states. At a high beam momentum the production yield of baryonic final states increases, with a beam momentum of 12 GeV it is 2.2 times larger than the mesonic final states. In addition to that, the $\overline{p}p$ annihilations are well suited for the study of strange and charmed baryons, since it is not required the production of K or D mesons for the conservation of strangeness or charm.

In the Λ and Σ spectrum there are new observed states waiting for confirmation and interpretation [17]. The experimental knowledge on the multi-strange Ξ and Ω states is very poor. The production yield of the Ξ ground state and the Ξ^* resonances allows for good statistics studies. The production cross section of Ω is reduced by the fact that an additional $s\overline{s}$ pair has to be created. For the non charmed baryons the maximum available center of mass energy allows for the complete spectroscopy of the discrete part of the spectrum. For the charmed baryon Λ_c it is possible to produce a state with an excitation of 0.93 GeV/c² above the ground state and for the charmed baryon Σ_c it is possible to produce a state with an excitation of 0.76 GeV/c² above the ground state.

1.2.2 Hadrons in nuclear matter

$\overline{\text{P}}\text{ANDA}$ foresees the possibility to study antiproton annihilations on fixed heavy nuclear targets in the later stage of the experiment. These reactions are ideally suited to investigate the modification of hadronic mass in nuclear matter and unravel the origin of hadronic mass.

The QCD vacuum is characterized by quark and gluon condensate. The chiral symmetry [18] in QCD is spontaneously broken by the fact that the quarks do have mass. The light quark masses are much smaller than the hadronic scales masses, for this reason the chiral symmetry may be considered an approximate symmetry of the strong interactions. A partial restoration of chiral symmetry is expected in dense nuclear matter and at high temperatures for the light quarks due to the change of the quark condensate. This should therefore lead to the modification of hadrons properties, like mass and widths, when they are embedded in the nuclear matter.

Experiments in the light meson sector reported the mass shift and width modification in dense nuclear matter [19]. The high intensity beam up to 15 GeV/c in $\overline{\text{P}}\text{ANDA}$ allows for an extension of in-medium studies towards the heavy-quark

sector, especially for mesons containing open or hidden charm. Given the large contribution of the c quarks in the charmonium mass, the in medium masses of charmonium states are expected to be affected mainly by the gluon condensate. For this reason it is expected a small shift of the in medium mass $\sim 10 \text{ MeV}/c^2$ for the low lying charmonium states. [20].

The D mesons, which are made of a c quark coupled to a light antiquark, represents an unique possibility to study the in medium modifications of systems with a single light quark. Figure 1.9 shows the theoretical predictions for the drop of the D and D^* meson masses in relation to the surrounding nuclear matter density. The D mass dropping lowers the $D\overline{D}$ threshold in the nuclear matter and consequently increases the production cross section of the D and \overline{D} mesons in antiproton nucleus reactions.

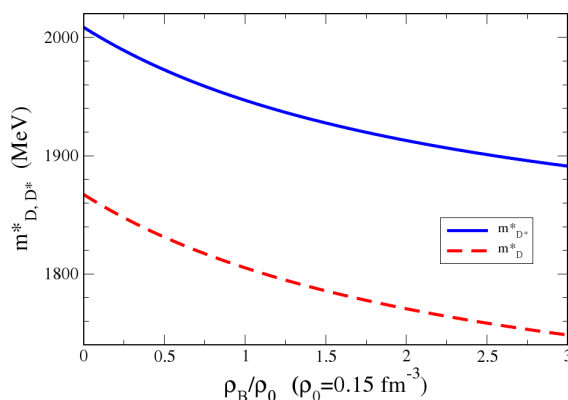


Figure 1.9: D and D^* meson effective masses as a function of nuclear matter density [21].

Another important study for a better understanding of the properties of charmed hadrons in nuclear matter is the measurement of the J/Ψ dissociation in the nuclear matter. This phenomena is due to any interaction of J/Ψ or its precursor state with the nuclear medium which could break its bound state. The available data on the J/Ψ - nucleon cross section is scarce and it is determined by indirect experimental information from the J/Ψ -nucleon interaction in high energy proton-nucleus collisions [22]. Thus the deduced J/Ψ - nucleon dissociation cross section has large uncertainties and its momentum dependence is unknown. In $\overline{\text{P}}\text{ANDA}$ a reliable J/Ψ - nucleus dissociation cross section will be obtained by the comparison of the production yield of J/Ψ in \overline{p} annihilation on protons and different nuclear targets [23]. This is important for the understanding of the charmonium suppression in relativistic heavy ion collisions, which is considered one of the most promising signature of the formation of the quark-gluon plasma.

1.2.3 Hypernuclei

A hyperon is a nucleon where one or more quarks (u, d) are replaced with a strange quark [24]. Hypernuclei are nuclei where one or more nucleons are replaced by hyperons, thus introducing a new flavor, the strangeness. Figure 1.10 shows the 3-dimensional hypernuclear chart with the experimentally found hypernuclei. The $S = 0$ plane contains the ordinary nuclei, the $S = -1$ plane contains the nucleons with Λ or Σ hyperons and the $S = -3$ plane contains the nucleons with $\Lambda\Lambda$ or Ξ hyperons.

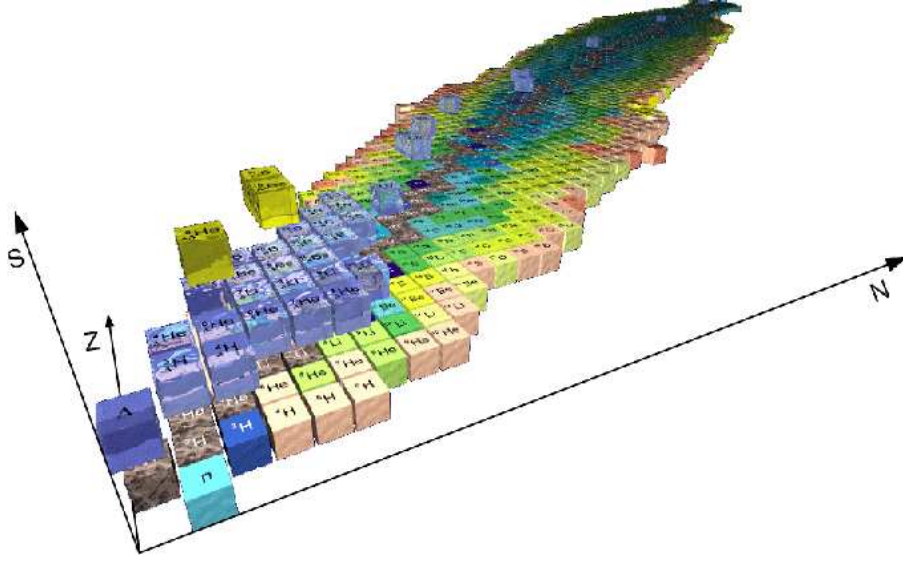


Figure 1.10: 3D chart of the nucleons, arranged according to the number of neutrons (N), number of protons (Z) and strangeness (S).

Since the strangeness quantum number is conserved in strong and electromagnetic interactions, the hyperon ground state could decay only by weak interaction. The lightest hyperon is the Λ^0 (uds) with a mass of 1115.683 ± 0.006 MeV and a mean lifetime of $(2.631 \pm 0.020) \cdot 10^{-10}$ s. Given such hyperon lifetime, the hypernuclei are able to exhibit sharp nuclear energy levels. The access of the hyperon to these nuclear energy levels is not restricted by the Pauli principle. This offers the opportunity for nuclear spectroscopy and the study of the hyperon nucleon interaction, in particular the spin-dependent part of the nuclear potential.

The central part of the $\overline{\text{PANDA}}$ detector can be replaced with an experimental setup for the precision γ ray spectroscopy of single and double hypernuclei. Double and single Λ hypernuclei can be produced from $\overline{p} N$ interactions in a multistage process [25]. The \overline{p} beam with a momentum of 3 GeV/c will interact with a primary

target (^{12}C), producing $\Xi\overline{\Xi}$ pairs at rest in $\overline{p}p \rightarrow \Xi^-\overline{\Xi}^+$ and $\overline{p}n \rightarrow \Xi^-\overline{\Xi}^0$ reactions. The rescattered Ξ^- within the primary target nucleus will be stopped and captured by a secondary target (^9Be , $^{10,11}\text{Be}$ or $^{12,13}\text{C}$). Here it is possible the conversion in a double Λ through the $\Xi^-p \rightarrow \Lambda\Lambda$ reaction. Since it is a multistage process, the spectroscopic information are obtained by the identification of the weak decay products. The γ -ray detection from the disexcitation of the bound hypernuclei within the nuclear potential allows for an unique identification of the double hypernuclei. A γ -rays detection with a resolution of 3.4 keV will be performed with an array of germanium detectors close to the target.

1.2.4 Proton structure

Generalized parton distributions

The binding force between quarks and gluons, which makes possible the formation of hadrons, has to be studied in the non perturbative QCD regime. At the moment there is not a reliable fully quantitative calculations starting from QCD first principles. The nucleon structure is described by phenomenological functions, like form factors, parton densities and distribution amplitudes. In the infinite momentum approximation, the partons are free non-interacting particles, and it is possible to describe the hadrons with the distribution of partons in the longitudinal direction given by the distribution functions. Elastic form factors give information on the charge and magnetization distributions in the transverse plane. The Generalized Parton Distributions (GPDs) [26] unifies and extends these concepts, giving a description of partons with functions of more variables. From the GPDs it is possible to obtain a full three dimensional image of hadrons, since it contains information on the distribution of partons both in the transverse plane and in the longitudinal direction, and the quark and gluon angular momentum contributions to the nucleon spin.

The GPDs has been introduced in the study of hard exclusive processes in lepton scattering experiments. $\overline{\text{P}}\text{ANDA}$ will conduct studies of Hard Exclusive Processes in $\overline{p}p$ annihilation with various final states in a new kinematic region. New insights into the applicability and universality of these novel QCD approaches can be expected. Measurement of the Crossed-Channel Compton Scattering ($\overline{p}p \rightarrow \gamma\gamma$) and Hard exclusive meson production ($\overline{p}p \rightarrow \gamma\pi^0$) are foreseen.

Drell-Yan processes

The Drell-Yan process [27] occurs in high energy hadron-hadron scattering, where a quark and antiquark from the interacting hadrons annihilate creating a virtual

photon or Z boson, which then decays into a pair of oppositely-charged leptons (Fig. 1.11).

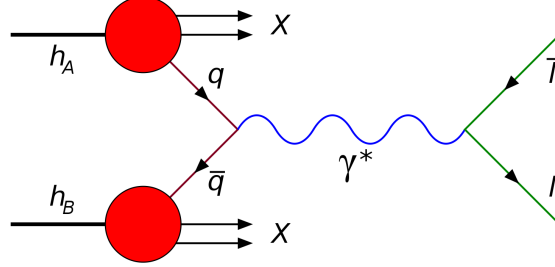


Figure 1.11: Drell-Yan process.

The Drell-Yan process is an ideal tool for investigating the transverse parton distribution functions. In $\overline{\text{P}}\text{ANDA}$ the Drell Yan process will be studied in semi inclusive lepton production for di-muons in scattering of unpolarized antiproton beam over unpolarized proton target $\overline{p}p \rightarrow \gamma^* \rightarrow \mu\mu + X$. From the angular distribution of dileptons it is possible to evaluate the distribution function of a transversely polarized quark inside an unpolarized hadron $h_T^\perp(x, \vec{k}_\perp^2)$.

Time-like form factor of the proton

The electromagnetic form factor of the proton is of utmost importance for the study of hadronic structure and internal dynamics at low energies as well as the higher energies where perturbative QCD applies. The measurement of the electron scattering on protons allows to determine the proton form factors in the region of space like momentum transfer $q^2 < 0$. While $\overline{p}p \rightarrow e^+e^-$ annihilation gives access to the proton electromagnetic form factors in the time like region $q^2 > 4m_p^2c^2$, where m_p is the proton mass (Fig. 1.13).

In the space like region the form factors are real functions of q^2 , and they are the Fourier transforms of the spatial charge (G_E) and the magnetization distribution (G_M). In the time like region the form factors are complex functions, and represent the frequency spectrum of the electromagnetic response of the nucleon. The center of mass differential cross section of the reaction $p\overline{p} \rightarrow e^+e^-$ in one photon approximation is a linear combination of the squared moduli of $|G_E|$ and $|G_M|$.

The $q^2 < 15$ (GeV/c)² region of the proton time like form factors have been measured by E760 and E835 experiments at Fermilab [28]. But due to limited statistics

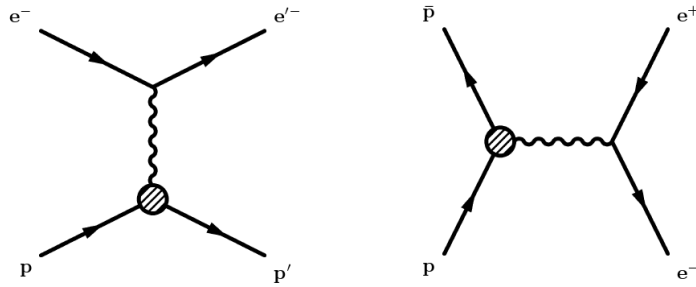


Figure 1.12: Feynman diagrams for electron scattering on proton (left) and its crossed channel $\bar{p}p \rightarrow e^+e^-$ (right).

$|G_M|$ and $|G_E|$ have not been measured separately. Thanks to the improved statistics and wide angular coverage, $\overline{\text{P}}\text{ANDA}$ will measure the G_E and G_M separately with an unprecedented precision up to $14 (\text{GeV}/c)^2$ and the absolute and differential cross section up to $22 (\text{GeV}/c)^2$ [29]. Therefore it is possible to test the transition to the perturbative QCD regime, where an asymptotic behavior is predicted for the proton magnetic form factor. The $\overline{\text{P}}\text{ANDA}$ rich particle identification plays an important role in the rejection of the $\bar{p}p \rightarrow \pi^-\pi^+$ background with a cross section 10^6 times higher.

1.3 Experimental apparatus

1.3.1 Antiproton facility

The $\overline{\text{P}}\text{ANDA}$ experiment will be located at the High Energy Storage Ring (HESR) of the Facility for Antiproton and Ion Research (FAIR). A multistage process is planned at FAIR for the delivering of high quality and high intensity antiproton beams, using key technologies for beam cooling, rapidly cycling superconducting magnets and narrow bunching of beams [30].

The protons accelerated by the LINAC linear accelerator at 70 MeV will be injected in the SIS18 synchrotron ring which is able to accelerate $5 \cdot 10^{12}$ protons per machine cycle, with a repetition rate of 4 Hz. The SIS18, after accelerating the protons at 2 GeV, will send the beam in the main synchrotron SIS100 (1083.6 m circumference), where $4 \cdot 10^{13}$ protons could be accumulated in a single bunch of 25 ns time width, with an energy of 29 GeV. The SIS100 cycle length will be ~ 2 s, then the protons will be directed on the external antiproton production target. The expected antiproton production yield per proton is $\sim 5 \cdot 10^{-6}$, thus from a single

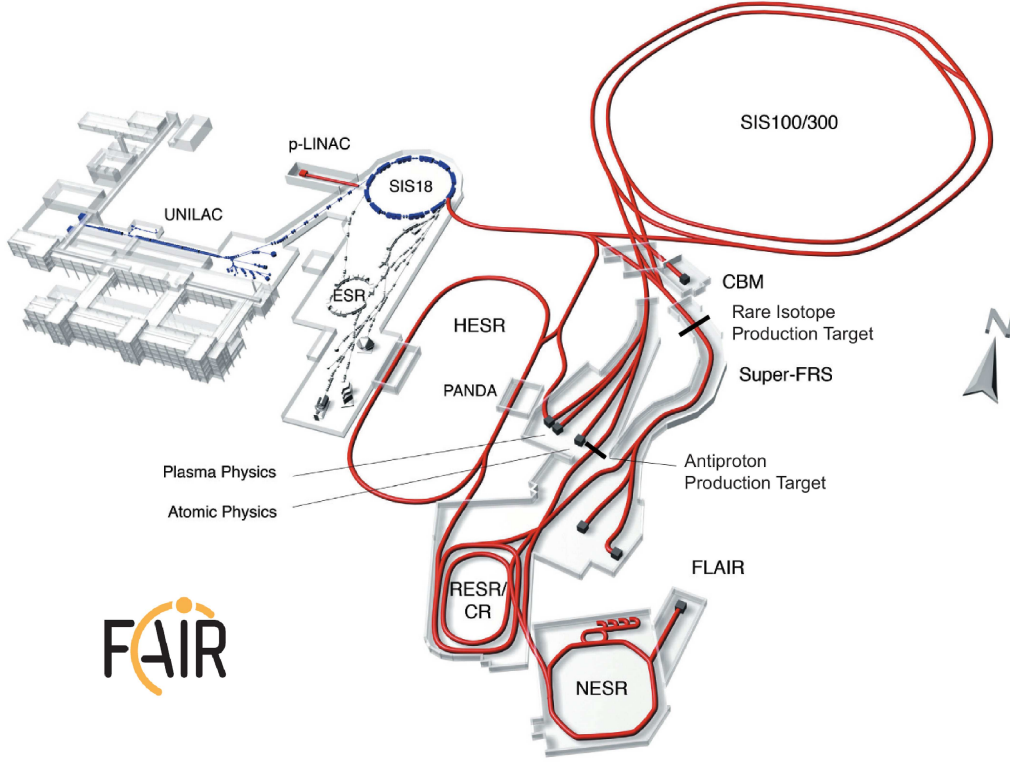


Figure 1.13: Facility for Antiproton and Ion Research (FAIR). The existing facility at GSI is shown in red and the facility under construction in blue.

bunch $\sim 10^8$ antiprotons will be produced. Pulsed magnets will be employed to separate the antiprotons from the other particles produced in the collision. The proton acceleration cycle will be repeated every 10 s, therefore 10^7 antiprotons per second will be produced. The antiproton will be accumulated in the Collector Ring (CR), with a beam momentum of 3 GeV/c and momentum spread of $\delta p/p = 3 \cdot 10^{-3}$ thanks to the fast stochastic cooling. Every 10 s a bunch of $\sim 2 \cdot 10^8$ antiprotons will be delivered to the Accumulator Ring (RESR) able to accommodate up to 10^{11} antiprotons. Finally the antiproton beam will be transferred at the High Energy Storage Ring (HESR) for the $\overline{\text{PANDA}}$ experiment.

The HESR is designed as a race track shaped ring (perimeter of 574 m), with two long straight sections connected by two 180° arc sections (Fig. 1.14). The straight sections will contain Radio Frequency (RF) cavities for acceleration. One section will host the $\overline{\text{PANDA}}$ experiment and the equipment for the insertion of the antiproton beam from the RESR, while the other one will be occupied by the electron cooling system. The incoming antiproton beam from RESR at 3.8 GeV/c

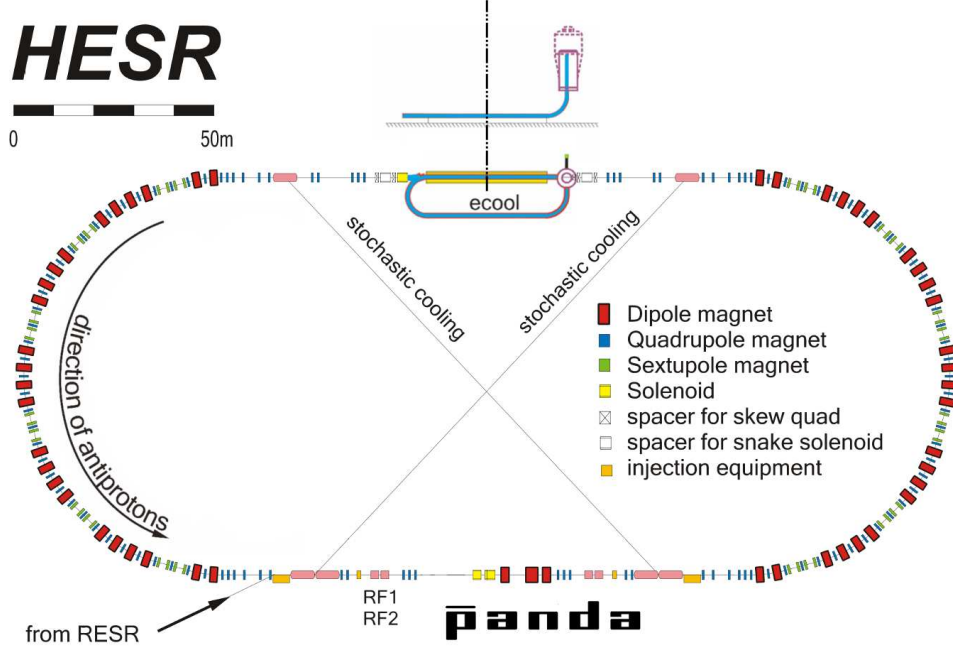


Figure 1.14: Schematic view of the High Energy Storage Ring (HESR).

will have a transverse emittance of 0.25 mm mrad and a relative momentum spread of $3.3 \cdot 10^{-4}$. In the HESR the antiprotons could be accelerated or decelerated in a momentum range between 1.5 GeV/c and 15 GeV/c . Bending magnets with a field between 0.36 T and 3.6 T will be employed. Stochastic cooling systems, placed at the entrance and exit of the straight sections, will allow for an independent longitudinal, horizontal and vertical cooling. The key technology of the HESR is the electron cooling system [31], which is able to increase the longitudinal phase-space density of the circulating antiproton beam by the mixing of a phase-space cooled electron beam with the same average velocity. The resulting friction force between antiprotons and electrons transfers the energy of the chaotic motion of the antiprotons to the electrons. A special vertical tank will accelerate an electron beam up to 1 A current in the energy range of 0.4 MeV to 4.5 MeV . The cooler section length is 22 m , and the longitudinal strength of the solenoidal field of 0.2 T . This allows for a high resolution beam for high precision experiments in a momentum range of 1.5 GeV/c to 8.9 GeV/c . The average luminosity is calculated assuming a hydrogen pellet target with an effective thickness of $4 \cdot 10^{15}$ atoms, and 10^{11} antiprotons stored in the HESR in the High Luminosity or 10^{10} antiprotons in the High Resolution mode. Table 1.5 reports the values for the luminosity and the

antiproton beam parameters in the two different working modalities.

Modality	High luminosity	High resolution
Luminosity	$2 \cdot 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$	$10^{31} \text{ cm}^{-2} \text{ s}^{-1}$
Resolution ($\delta p/p$)	$\sim 10^{-4}$	$\sim 10^{-5}$
Cooling	stochastic cooling	electron cooling
Momentum range	1.5 GeV/c - 15 GeV/c	1.5 GeV/c - 8.9 GeV/c

Table 1.5: HESR working modalities.

1.3.2 Detector

The $\overline{\text{P}}\text{ANDA}$ detector [32] will be located in the HESR and it will provide a full solid angle coverage around the interaction point between the antiproton beam and the fixed target. The detector has to afford a high event rate ($2 \cdot 10^7$ annihilations/s) with continuous readout and efficient on-line event selection. It is designed as a multipurpose and 4π detector since many experimental studies of the $\overline{\text{P}}\text{ANDA}$ program require full exclusive measurements. The $\overline{\text{P}}\text{ANDA}$ apparatus will perform detection and identification of charged particle in a wide momentum range from 100 MeV/c up to 15 GeV/c and γ identification up to 10 GeV with the electromagnetic calorimeters. A momentum resolution of the order of 1% and high tracking resolution of charged particles, is required.

General setup

The $\overline{p}-p$ annihilations will be studied with a hydrogen target (pellet or cluster-jet). Heavier gas target and wire target are under consideration for $\overline{p}-N$ interactions. Despite the boost of the reaction products in the forward direction, a full coverage is crucial for the detection of low energy particles (π , γ , K) which will have an isotropic emission. The proposed detector is subdivided in a target spectrometer which will cover the interaction point at large polar angles and a forward spectrometer which will cover the most forward angles. This configuration allows a full angular coverage and good momentum resolution over a wide range of energies. The target spectrometer will be inside a solenoid magnet, with a field of 2 T, it will detect the charged particles with high transverse momentum tracks. It will contain tracking and particle identification detectors for charged particles and an electromagnetic calorimeter for γ detection and e/π separation. The detectors are arranged in barrel layers covering a polar angle between 22° and 140° , the endcap structure will cover the forward angles down to 5° and 10° in the vertical and horizontal directions, respectively. The forward spectrometer will be behind a dipole magnet with a field integral of 2 Tm for

the momentum analysis of charged particles in the forward angles below 5° and 10° respectively in the vertical and horizontal directions. Different perpendicular detection planes will allow for precise tracking and identification of charged particles with a momentum up to 8 GeV/c and for high quality measurements of neutral particles. A luminosity monitor will be placed behind the target spectrometer covering angles from ~ 0.5 mrad to ~ 5 mrad.

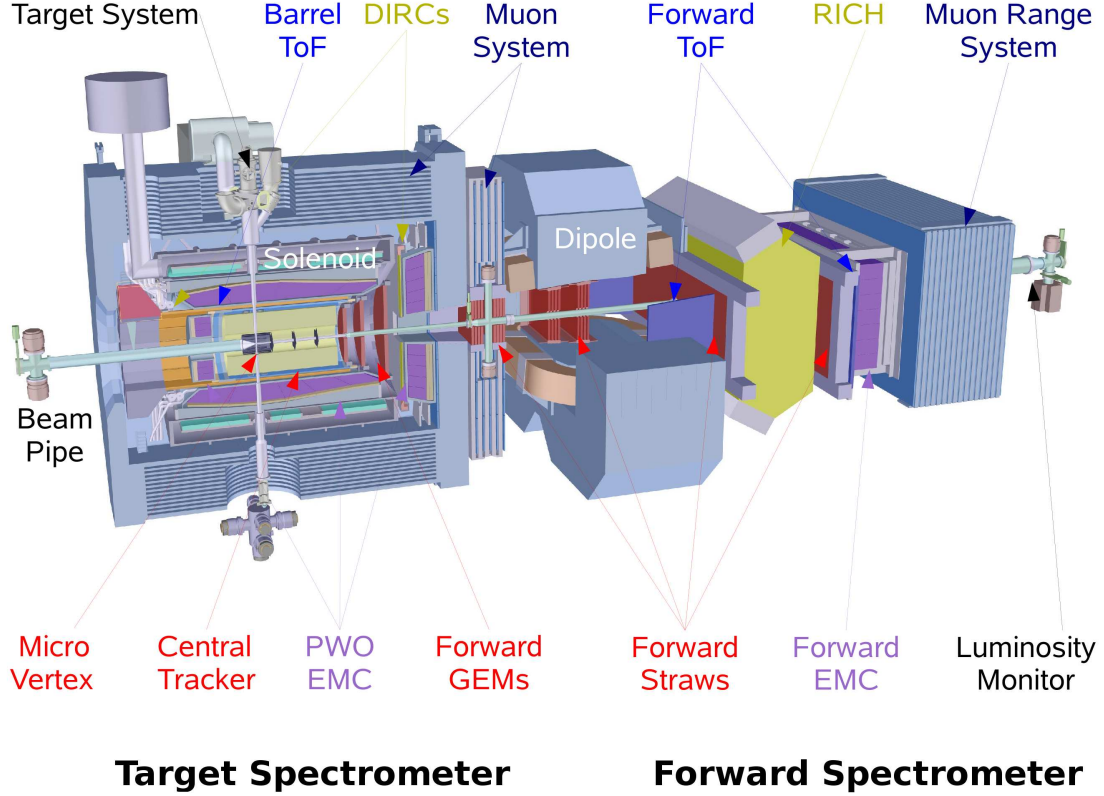


Figure 1.15: Cross section view of the $\overline{\text{P}}\text{ANDA}$ detector model. The interaction point is the crossing between the target system and the beam pipe. The overall length, including the target spectrometer and the forward spectrometer is ~ 15 m, the outer radius of the solenoid magnet is ~ 2.3 m.

Tracking system

The tracking system will provide an accurate determination of the particle momentum, a high spatial resolution of the primary interaction vertex and the detection

of displaced secondary vertices. The central tracker system will be positioned inside the target spectrometer, and the particles momentum can be extracted by the determination of the bending radius due to the solenoid magnet. A brief description of these systems is given in the following.

- **Micro-Vertex Detector (MVD)**

The MVD is the closest detector to the interaction point [33], whose role is the tracking of the charged particle for the vertex reconstruction. In addition, a measurement of the energy loss per unit path-length (dE/dx) will be useful for slow charged particle identification. It is optimized for the detection of secondary vertices from D mesons and hyperon decays and to have maximum acceptance close to the interaction point. The MVD will decrease the transverse momentum measurement uncertainty, from $\delta p/p \approx 2.6\%$ in a scenario without MVD to $\delta p/p \approx 1.4\%$. The MVD is a silicon detector made of radiation hard hybrid pixel detectors and double-side strip detectors. A detailed description of the MVD will be given in Chapter 2.

- **Straw Tube Tracker (STT)**

A straw tube is a type of gaseous ionization detector. It is a metal coated tube, with an applied voltage of some kV between the wall of the tube and the central ground wire along its axis. It is foreseen to employ a tube with a length of 150 cm and a diameter of 1 cm, made of aluminized mylar (Biaxially-oriented polyethylene terephthalate film) and filled with a Ar/CO_2 gas mixture (90/10) at a pressure of ~ 2 atm. This configuration allows a good transverse track resolution of $150\ \mu\text{m}$ with a material budget of only 1.3% radiation length. In addition to that the gas pressure allows for a self supporting structure. When a particle crosses the straw tube, the gas will be ionized and the produced ions and electrons will drift in the electrical field. When the electron is close to the wire ($\sim 50\ \mu\text{m}$), an avalanche multiplication will generate a $\sim 10^5$ times larger charge and the readout of the electrical signal would be possible. The signal arrival time defines the drift path, and the collected charge is proportional to the particle energy loss, giving an important contribution for the global particle identification. Each straw tube will have its own electric field and the detector will be able to afford a high rate, moreover an eventual wire damage will affect only one channel. The $\overline{\text{P}}\text{ANDA}$ STT will consists of 4200 tubes arranged in planar layers, which are mounted in a hexagonal shape around the MVD. It will result in a hollow cylinder, concentric to the beam pipe, with an internal radius of 15 cm and an external radius of 42 cm. An alternative under consideration is the employment of a Time Projection Chamber (TPC) with GEM readout [34].

- **Gas Electron Multiplier (GEM)**

The Gas Electron Multiplier (GEM) is a type of gaseous ionization detector. It is made of an insulating layer, a thin polymer foil, metalized on both sides. The layer is photolithographically perforated by holes of $70\ \mu\text{m}$ diameter with a center to center distance of $150\ \mu\text{m}$. The foil is placed in a gas volume between a cathode and a readout anode, thus creating a strong electrical field in the microscopic holes. A separate electrode creates an electrical field which make possible the drift of electrons produced in ionization towards the amplifying plate. In these holes the avalanche production occurs, and the resulting electrons are ejected from the plate and collected in the readout anode. The GEM is well suited for the forward direction with high rate capability and low material budget thanks to the ultra-thin coating employed. A set of large planar GEM detectors will be used as a first forward tracking detector, within the target spectrometer solenoid magnet, covering the particles emitted at angles below 22° . The present design foresees three detectors at 117 cm, 153 cm and 189 cm from the target, with a forth optional detector at 81 cm.

- **Forward Trackers**

Three pairs of tracking detector layers, positioned in front, within and behind the dipole magnet, will measure the deflection of charged particles in the magnetic field. This system will allow to track particles at the most forward angles with both high and low momenta. Each detector will consist of four double layers of straw tubes, two aligned horizontally and the other two layers with wires inclined by few degrees with respect to the horizontal axis. This configuration makes possible the reconstruction of tracks in each chamber separately, also in case of multitrack events. The expected momentum resolution for protons at $3\ \text{GeV}/c$ is $\delta p/p = 0.2\%$, the main limitation is due to the multiple scattering in the gas and wire material.

Charged particle identification

A particle identification with extreme accuracy over a large range of solid angle and momenta is essential for many aspects of the $\overline{\text{P}}\text{ANDA}$ experimental program. The identification of γ , p , \overline{p} and other quasi-stable charged particles like e^\pm , μ^\pm , π^\pm , K^\pm is required. In addition to the energy loss measurements from tracking system and electromagnetic calorimetry information, the $\overline{\text{P}}\text{ANDA}$ detector will be equipped with dedicated particle identification (PID) systems providing the ability of classifying particle species over the whole kinematic range.

- **Čerenkov detectors**

The Čerenkov detector is based on Čerenkov radiation, an electromagnetic radiation emitted when a charged particle has a velocity (v_p) greater than the

light speed in the medium in which it is traveling c/n , where c is the vacuum speed of light and n the index of refraction of the medium. The electromagnetic radiation is emitted in a cone around the particle motion direction. Measuring the angle of the cone $\theta_c = \arccos(\frac{c}{n v_p})$, and extrapolating the momentum of the particle from the magnetic bending, it is possible to determine the mass of the particle and therefore identify it. Given the strong dependency of the average particle momentum on the polar angle two different Čerenkov detectors will be employed:

- In the target spectrometer relatively slow particles are expected. A barrel DIRC will cover the angular region between 22° and 140° , while the endcap DIRC will cover the remaining angular region down to 5° . The radiator will be made of artificially fused quartz with a relative high index of refraction ($n = 1.47$). The Čerenkov radiation, in the visible and near UV range, will be measured by the Detector of Internally Reflected Čerenkov (DIRC) light [35]. One of the main advantage is the reduction of radiation length since only the thin radiators have to be placed inside the sensible volume, and the readout elements can be placed outside the acceptance. The DIRC will provide π/K separation up to about 4 GeV/c.
- Particles in the most forward angles are expected with an higher momenta. In the forward spectrometer a Ring Imaging Čerenkov Detector (RICH) will be employed, with a concept based on the RICH of the HERMES experiment [36]. It consists of a box filled with the radiator gas at atmospheric pressure, a spherical mirror and the photon detector array. Two different materials will be employed to fill the radiator. The aerogel with a refractive index of $n = 1.0304$, will cover the low energy region below 10 GeV, while the C_4F_{10} gas, with a refractive index of $n = 1.00137$, provides PID at higher momenta. The RICH detector will be able to cover a momentum range of 2 GeV/c - 15 GeV/c and allows for π/K and K/p separation.

- **Time of flight system**

The Time of Flight (TOF) system will generate the stop signal to measure the time that a particle has used to travel a certain distance. In conjunction with the momentum, determined by tracking in the magnetic field, masses and particle identification can be defined. TOF will provide the identification for slow particles, with flying time larger than the time resolution, below the Čerenkov light threshold. In the target spectrometer the flight path is of the order of 1 m, therefore a time resolution smaller than 100 ps is required. A barrel TOF between the STT and the DIRC barrels will provide an angular coverage between 22° and 140° . Assuming a time resolution of $\sigma_t = 100$ ps, it is

possible a π/K separation on a three standard deviation level for a momentum up to 430 MeV/c at 90° and up to 760 MeV/c at a polar angle of 22° . In the forward region a first TOF wall will be placed inside the dipole magnet opening, and a second TOF wall will be placed about 6.9 m from the target. With the expected time resolution of $\sigma_t = 50$ ps, it is possible to achieve π/K and K/p separations on a three standard deviation level for a momentum up to 2.8 GeV/c and 4.7 GeV/c respectively. The TOF barrel part requires 96 strips and the TOF wall part require 66 strips. Each strip consists in a plastic scintillator coupled to a fast phototube on both ends via lightguides, and read out by a fast front-end electronics.

- **Muon detection system**

Muons are important probes for J/Ψ decays, semileptonic D-meson decays and the Drell-Yan process. Since the processes having muons as final state have a low cross section a very good muon detection system is required. The main contribution for the muon identification comes from the muon detection system, additional information are given by calorimetry and TOF measurements. The muon detection will be implemented through the range tracking system, where the absorbing metal layer will be interleaved with detectors layers. This configuration allows to distinguish the energy loss processes of muons and pions and therefore obtain a high separation of primary muons from the background. In the barrel region the iron magnet yoke, employed as absorber, will be segmented with layers of detectors. There will be a first layer of 6 cm of iron followed by 12 layers of detectors spaced by iron layers of 3 cm thickness. In the endcap region the particles are expected with a higher momenta, and for this reason the absorber layer thickness will be increased to 6 cm. In the gap between the endcap of the target spectrometer and the dipole magnet and additional muon filter, with the same mechanical structure of the endcap muon detector, will be introduced. It will increase the absorber depth for the forward angles and it will also give a magnetic screening between the magnetic solenoid of the target spectrometer and the dipole magnet of the forward spectrometer. The most forward angles will be covered by a wall of counters for muon identification, placed at the end of the forward spectrometer at ~ 10 m downstream of the interaction point. Mini Drift Tubes (MDTs) [37] are envisaged for the detection layers.

Calorimetry

The $\overline{\text{P}}\text{ANDA}$ detector will have two electromagnetic calorimeters for the successful detection of photons in the whole solid angle, and a hadron calorimeter for the detection of neutrinos and neutral hadrons in the most forward angles.

- **Barrel Electromagnetic calorimeter**

The electromagnetic calorimeters [38] will provide measurements of photons with accurate energy, position and time with high resolution, for a wide dynamic range of photon energies (~ 10 MeV - ~ 10 GeV). A high and homogeneous efficiency is required for the identification of single photons and the coincident detection of the decay photons from multimeson exit channels. A high granular calorimetry is essential for a precise determination of the opening angle between the decay photons, required for the reconstruction of the invariant mass. Moreover a high response is required in order to afford the high interaction rate. The barrel electromagnetic calorimeter will be positioned behind the DIRC barrel inside the solenoid magnet of the target spectrometer, and it will provide a coverage of the 96% of the full solid angle. When a photon enters in the electromagnetic calorimeter an electromagnetic shower is produced, and it will be detected by the crystals of the calorimeter. The point of impact and the energy are obtained by the reconstruction of the electromagnetic shower. The lead tungstate PbWO_4 has been chosen for the scintillator crystal in order to meet the strong detector requirements. The containment of the shower energy is possible thanks to the short radiation length, a crystal length of 20 cm corresponds with a radiation depth of $22X_0$. The crystal section area will be $2\text{ cm} \times 2\text{ cm}$, thanks to the small Molière radius ($R_M = 59\text{ mm}$) the resolution in the determination of the shower position is increased. The proposed diameter, close to R_M , will allow a position resolution lower than 2 mm, which is $\sim 10\%$ of the crystal diameter. The expected energy resolution σ_E/E for photons and electrons is $1.54\%/\sqrt{E} + 0.3\%$ (E given in GeV). The time resolution is given by the count rate limit, which is dominated by the decay time $\tau = 6.5\text{ ns}$. These crystals allow a π/e^- discrimination of 10^3 for momenta above $0.5\text{ GeV}/c$. The readout of the crystals will be done by large area avalanche photodiodes. With an inner radius of 57 cm the barrel part of the calorimeter requires 11360 crystals. The backward and forward endcaps require 592 and 3600 crystals, respectively. Thus a total of 15552 PbWO_4 crystals will be required.

- **Forward Shashlyk Electromagnetic Calorimeter**

The Forward Electromagnetic Calorimeter will be located at a distance of 7 m downstream of the target, beside the dipole magnet, covering an active area of $\sim 3\text{ m}^2$. In this region there is not a strong requirement on the space resolution and a granularity of $10\text{ cm} \times 10\text{ cm}$ is achievable employing 351 modules. Each module consists of lead and scintillators layers sandwiched together with wavelength shifting (WLS) fiber readout (Shashlyk type) [39]. The length of each module will be 70 cm, corresponding with a radiation depth of $\sim 20X_0$. An energy resolution of $3\%/\sqrt{E}$ and a time resolution of $50\text{ ps}/\sqrt{E}$

are expected (E given in GeV).

- **Forward Hadron Calorimeter**

A hadron calorimeter is foreseen in the forward spectrometer for the measurement of neutral particles. It is placed in a strategical point since for antiproton momenta larger than 5 GeV/c, the 50% of the antineutrons emitted in $p\overline{p}$ interactions are confined in the solid angle of the forward spectrometer. Moreover for an antiproton beam momentum larger than 6 GeV/c in 1/3 of the interactions at least a neutral hadron will cross this region. Energy measurement of neutrons and neutral kaons is foreseen as well. The hadron calorimeter will serve also as an active muon filter, giving energy loss information in addition to the information given by dedicated muon counters behind it. The Mid Rapidity Calorimeter (MIRAC) from WA80 experiment is envisaged for the $\overline{\text{PANDA}}$ detector [40].

Data acquisition and trigger

The $\overline{\text{PANDA}}$ detector has to investigate many different physics topics in parallel, measuring the particles produced from interactions with a rate of $2 \cdot 10^7 \text{ s}^{-1}$. In order to allow a high flexibility in the event selection a continuous readout of all subdetector components has to be realized in parallel. Every subdetector detects the event autonomously and only the physical relevant information is transmitted. The events are marked with a timestamp and buffered for further processing. Thus a precise global time reference, distributed to all subdetectors, is required in order to correlate the different data. The trigger logic will be implemented in FPGAs (Field-programmable Gate Array) enabling sophisticated trigger decisions. High density FPGAs with large number of programmable gates including advanced embedded features will be employed for this purpose. The subdetectors and FPGAs will be connected through high speed serial links (10 Gb/s per link). Moreover the high reconfigurability of the network structure is crucial to reroute traffic for different physics selection topologies. The expected raw data from the subdetectors is of the order of 200 Gb/s, after the realtime selection of interesting events the relevant information for the mass storage will be about 200 MB/s.

Chapter 2

The Micro-Vertex Detector

In this chapter an overview of the Micro Vertex Detector (MVD) is given. Currently, the $\overline{\text{P}}\text{ANDA}$ MVD group [41] is engaged in different research and development activities for an optimized detector design starting from the experimental requirements. Simulation of $\overline{p}p$ and $\overline{p}N$ collisions are performed in order to analyze the high radiation environment and study the tracks distribution of the generated particles for different antiproton beam momenta. Taking into account the simulation results the MVD layout has been designed, maximizing the spatial resolution with a good angular coverage. In parallel, developments of epitaxial silicon sensors and custom Application Specific Integrated Circuit (ASIC) are ongoing in order to digitize the spatial, time and energy loss information. The integration and support infrastructure with a low material budget has been developed and various component have been manufactured and tested. The cooling system technology has been tested as well. Finally simulations with realistic Computer Aided Design (CAD) models taking into account the sensors, electronics, cooling, cabling and support, are performed in order to evaluate the MVD performance and optimize the layout design and the technological solutions.

2.1 MVD specifications

The Micro Vertex Detector (MVD) is a silicon tracking device for charged particles. It is the closest detector to the interaction point, it is enclosed by the central tracker and located inside the solenoid magnet of the target spectrometer with a magnetic field $|\vec{B}| = 2$ T. The MVD is fundamental for precise vertex reconstruction and for the improvement of the central tracking system resolution. Moreover, the MVD is able to perform a measurement of the energy loss per unit path-length (dE/dx) giving an additional input for particle identification.

2.1.1 Vertex reconstruction

The MVD is basically constituted by a set of tracking layers close to the interaction point. It allows for the determination of the primary interaction vertex and secondary vertices of short lived particles and delayed decays. The secondary vertices are important for the study of the weak decay of hadrons with charm or strange quark content (Tab. 2.1.1).

Particle	Lifetime	Decay Length $c\tau$	Decay channels (Branching Ratio)
K_s^0	895.3 ps	2.6842 cm	$\pi^+\pi^-$ ((68.95 \pm 0.14)%)
D^\pm	1.040 ps	311.8 μm	e^+ anything + c.c. ((17.2 \pm 1.9)%) K^- anything + c.c. ((27.5 \pm 2.4)%) K^+ anything + c.c. ((5.5 \pm 1.6)%) \bar{K}^0 anything + K^0 anything ((61 \pm 8)%) K^- anything + c.c. ((27.5 \pm 2.4)%) $\bar{K}^0 \pi^+\pi^+\pi^-$ ((7.1 \pm 1)%)
D^0	410.3 fs	123.0 μm	e^+ anything + c.c. ((6.87 \pm 0.28)%) μ^+ anything + c.c. ((6.5 \pm 0.8)%) K^- anything + c.c. ((53 \pm 4)%) K^+ anything + c.c. ((3.4 \pm 0.4)%) \bar{K}^0 anything + K^0 anything ((53 \pm 4)%) $\bar{K}^0 \pi^+\pi^+\pi^-$ ((7.46 \pm 0.31)%) $K^- \pi^+\pi^-\pi^0$ ((10.9 \pm 1.3)%)
D_s^\pm	490 fs	147.0 μm	e^+ anything + c.c. (\approx 8%) K^- anything + c.c. (\approx 13%) K^+ anything + c.c. (\approx 20%) \bar{K}^0 anything + K^0 anything (\approx 39%)
Λ	26.32 ps	7.69 cm	$p\pi^-$ ((63.9 \pm 0.5)%)
Σ^+	80.18 ps	2.404 cm	$p\pi^0$ ((51.57 \pm 0.30)%) $n\pi^+$ ((48.31 \pm 0.30)%)
Σ^-	147.9 ps	4.434 cm	$n\pi^-$ ((99.848 \pm 0.005)%)
Ξ^-	163.9 ps	4.91 cm	$\Lambda\pi^-$ ((99.887 \pm 0.035)%)
Ω^-	82.1 ps	2.461 cm	ΛK^- ((67.8 \pm 0.7)%) $\Xi^0\pi^-$ ((23.6 \pm 0.7)%) $\Xi^-\pi^0$ ((8.6 \pm 0.4)%)
Λ_c^+	200 fs	59.9 μm	$p\bar{K}^0$ ((2.3 \pm 0.6)%) $pK^-\pi^+$ ((5.0 \pm 1.3)%) $\Lambda\pi^+\pi^+\pi^-$ ((3.3 \pm 1.0)%) $\Sigma^0 + \pi^+\pi^-$ ((3.6 \pm 1.0)%)
Ξ_c^0	112 fs	33.6 μm	$\Xi^-\pi^+$ (unknown)

Table 2.1: Strange and charmed candidates by means of their delayed decay [5]. The abbreviation c.c. indicates the charge coupled channel. For example “ e^+ anything + c.c.” indicates the decay channels that have as a final state an electron or a positron with other particles.

Since the reaction process occurs in flight, the decay length is $L = \beta\gamma c\tau$, where $\beta = v/c$ is the relativistic velocity, $\gamma = (1 - \beta^2)^{-1}$ is the Lorentz factor and τ is the mean decay time in the particle rest frame. The elongation factor is given by $\beta\gamma = \frac{p}{Mc}$, where M is the particle mass and p is the particle momentum.

The tagging of D mesons is important for the investigation of the charmonium states and of the speculated hybrid state above the $D\bar{D}$ threshold. The D meson tagging is achieved through the exclusive detection of their charged decay products: with a reconstruction of two tracks it is possible to find the displaced vertex. Given the small decay lengths, for a clear displaced vertex identification, a spatial resolution $\delta\vec{x} \leq 100\mu\text{m}$ in vertex reconstruction is required. The early identification of D mesons in the MVD allows for an efficient event pattern selection from the data flux of the other detector in the DAQ.

2.1.2 Tracking and momentum resolution

The $\bar{\text{P}}\text{ANDA}$ detector tracking system will track the charged particles in the magnetic field in order to extract the particles momenta. The detection of the tracks hit on the MVD layers, close to the interaction point, allows for the improvement of the overall tracking resolution.

Figure 2.1 shows the results of the simulations of $\bar{p}p$ and $\bar{p}Au$ collisions at low, intermediate and high antiproton beam momenta. The plots show the distribution of tracks as a function of the polar angle and momentum. With a low \bar{p} beam momentum the interaction products have an uniform angular distribution, while in the case of a high \bar{p} beam momentum there is a forward boost of the reaction products. Due to the fixed target setup an enhanced emission of highly energetic particles in forward directions is prominent in particular for light targets. The particles with momenta below 1 GeV/c originating from particle decays are uniformly distributed to nearly all polar angles.

The tracking precision of the low momentum particles (< 1.5 GeV/c) is limited by the resulting lateral deflection due to the multiple Coulomb scattering during the interaction with the detector layers. For example for a proton with a momentum of 1 GeV/c, crossing 800 μm of silicon layers, it is expected an average deflection of 2 mrad, equivalent to 20 μm lateral deflection every 1 cm of flight. Different reactions to be studied at $\bar{\text{P}}\text{ANDA}$ will have in the final state particles with low momentum, even with high \bar{p} beam momentum. In particular for low production cross section channels (exotics, high precision charmonium resonances) the efficient tracking of low momentum particles is fundamental to increase the signal yield. Therefore the material budget of the tracking system has to be reduced in order to reduce multiple Coulomb scattering and energy loss, finding a good compromise between a low radiation length and a sufficient number of tracking layers.

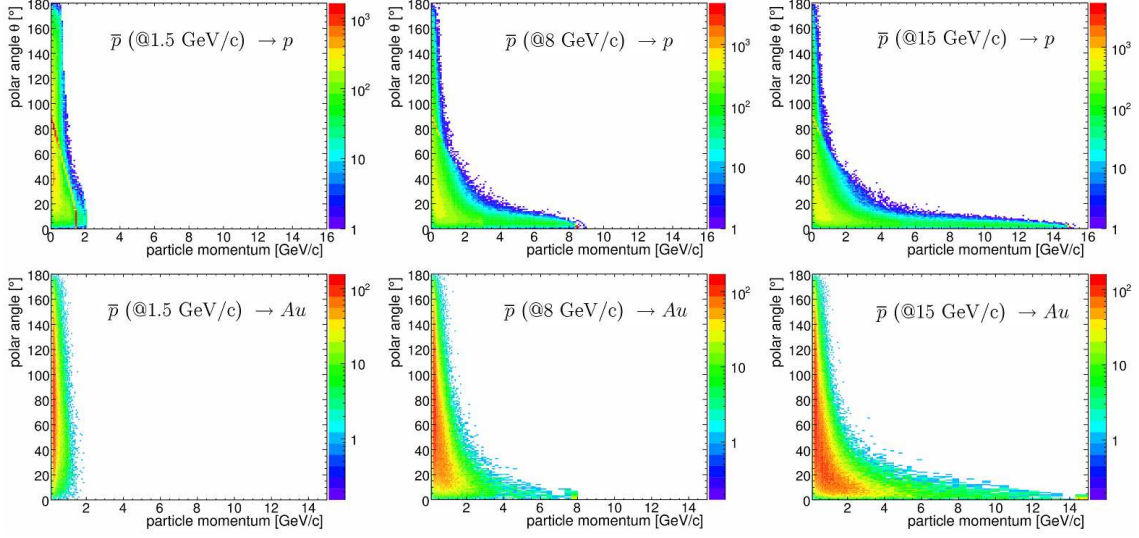


Figure 2.1: Tracks distribution in function of polar angle and momentum [41].

2.1.3 Particle identification

The charged particles that cross the silicon layers deposit a part of their energy through scattering processes with the silicon atomic electrons. The mean value of the energy loss per unit path length is described by the Bethe Bloch equation [5] in the region $10^{-1} < \beta\gamma < 10^3$:

$$-\frac{dE}{dx}\Big|_{mean} = Kz^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \left(\frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} \right) - \beta^2 \right] \quad (2.1)$$

where:

K	$4\pi N_A r_e^2 m_e c^2 = 0.307075 \text{ MeV cm}^2$
z	charge of the traversing particle in units of the electron charge
Z	atomic number of absorption medium (14 for silicon)
A	atomic mass of absorption medium (28 for silicon)
$m_e c^2$	rest energy of the electron (0.511 MeV)
β	velocity of the traversing particle in units of the speed of light
γ	Lorentz factor $(1 - \beta^2)^{-\frac{1}{2}}$
I	mean excitation energy (137 eV for silicon)
T_{max}	maximum kinetic energy transfer in single collision

The fluctuation in energy loss, due to a low number of high energy ionizations, are described by the Landau distribution. Since the Bethe Bloch formula is sufficiently

mass-dependent in the low momentum region, measuring the energy loss it is possible to contribute to the global particle identification procedure (PID). Figure 2.2 shows the simulation results for energy loss in function of the particle momentum for different particle species.

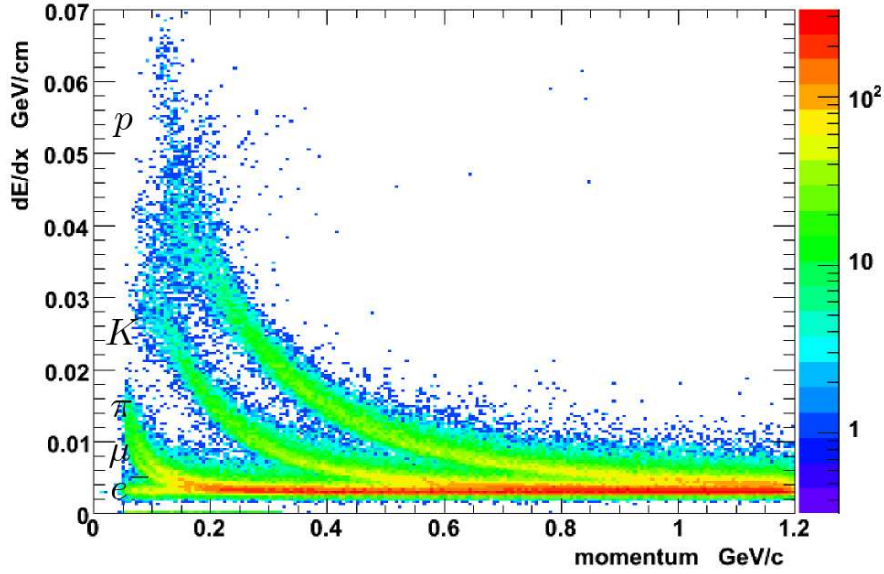


Figure 2.2: Energy loss for p , K , π , μ and e^- [41].

The ability of separating different particle species relies on an accurate energy loss information and a good knowledge of the track inclination with respect to the sensor surfaces. In the low momenta region (≤ 500 MeV/c) below the DIRC threshold, the information for the particle identification comes only from the TOF system, and thus the energy loss information is useful to enhance the PID capability of the overall detector. In general the MVD can contribute to the PID decision of the $\overline{\text{P}}\text{ANDA}$ detector in the momentum range up to ~ 0.6 GeV/c for kaons and up to ~ 1 GeV/c for protons. Signal for e , π and μ are too similar to contribute to the PID [42].

2.1.4 Requirements

From the analysis of the measurements necessary to fulfill the $\overline{\text{P}}\text{ANDA}$ experimental program and the MVD main tasks it is possible to define the MVD basic specifications [33]. Additional inputs come from the simulation information on the radiation environment.

Spatial resolution

A spatial resolution $\delta\vec{x} \leq 100\mu\text{m}$ is required for a clear detection of the displaced vertices. A good spatial resolution along the beam axis (z direction) is essential to recognize the $D\bar{D}$ events as decay products of $c\bar{c}$ resonances. The spatial resolution in the perpendicular plane to the beam axis (r/ϕ directions) is important for a good transverse momentum resolution, especially at low transverse momentum as in the case of slow pions originating from the D^* decay.

Material budget

A large number of radiation length (x/X_0) implies low momentum resolution due to the multiple scattering and a high background in the case of photon conversion. It is critical especially for the low momentum particles, which will be produced abundantly. In addition to that, since the MVD is the innermost detector it does not have to affect the outer detector components. Therefore the MVD material budget has to be kept as low as possible. In order to have a sufficient number of detection layers (~ 4) for the track reconstruction, each layer has to have a number of radiation length $x/X_0 \leq 2\%$.

Time resolution

In the HESR the antiproton beam is stored without any bunch structure. It is foreseen an interaction rate of $2 \cdot 10^7 \text{ s}^{-1}$, thus the mean time between two interactions is 50 ns. In order to associate the MVD hits with the correct interaction, a time resolution of ≤ 10 ns is required. Given the master clock frequency $f_c \approx 155 \text{ MHz}$ the theoretical maximum time resolution is $\sigma_t = (\sqrt{12}f_c)^{-1} \approx 1.9 \text{ ns}$.

Readout speed

The $\bar{\text{P}}\text{ANDA}$ detector will not have a centralized trigger system, therefore the MVD has to send out to the offline electronics all the data which contains information on the hit position, timing and energy loss. Taking into account the MVD particle hit rate of $3 \cdot 10^9$ given in Section 2.2.2 the overall readout speed has to be in the order of $\sim 100 \text{ Gbit/s}$.

Radiation hardness

The close position of the MVD to the interaction point and the high event rate, make radiation hardness a fundamental parameter for the reliability of both sensors and electronics. From particles rates and density simulations the expected fluence

is $\sim 5 \cdot 10^{14} n_{[1 \text{ MeV}_{\text{eq}}]}/\text{cm}^2$ assuming $\bar{p} - p$ annihilations at 15 GeV/c in 10 years of data taking with a duty cycle of 50%.

2.2 MVD design

The MVD design foresees four cylindrical layers (barrels) to cover the angles between 40° and 150° , where low momentum particles ($< 1.5 \text{ GeV}/c$) are expected. While the angular region between 3° and 40° , is covered by six forward disks, where a high flux of particles is expected with an antiproton beam at intermediate and high momenta. Figure 2.3 shows a schematic picture of the MVD layers, the overall length is 460 mm, the internal radius of the innermost layer is 25 mm and radius of the outermost barrel is 150 mm.

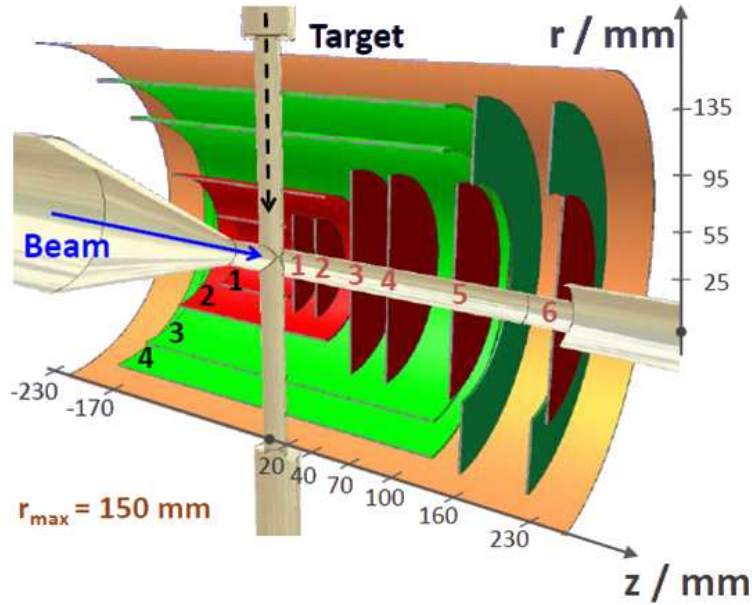


Figure 2.3: MVD layout [41].

Each silicon layer has to provide a two dimensional information about the interaction point between the layer itself and the crossing charged particle. The detection layers in the region close to the interaction point and at the forward angles have to handle a high event rate, and hybrid pixel sensors have to be employed in order to avoid ambiguities and maintain high granularity. The pixel sensors cover the 1st and 2nd barrels and the central part of the forward disks, for an area of 0.11 m^2 , with 11 M readout channels. In the outer region the expected flux is lower, and double

sided strip sensors (DSS) are used in order to reduce the material budget. The DSS sensors will cover the 3rd and 4th barrel and the external region of the 5th and 6th forward disks, for an area of 0.5 m², with 200 k readout channels.

In the early phase of the $\overline{\text{PANDa}}$ R&D monolithic sensors were also considered as a possible alternative due to their reduced material budget and lower cost. However, hybrid pixels with a material budget of 1.12% which is well below the $\overline{\text{PANDa}}$ upper limit, are currently in use in the ALICE experiment. On the other hand, monolithic pixels which fulfill the $\overline{\text{PANDa}}$ specifications in terms of time resolution, radiation hardness and PID capabilities have not yet been demonstrated. Therefore, as of today, the choice of hybrid pixels and strips fully retains its validity.

2.2.1 Implementation

The detector implementation is made taking into account both geometrical and technical considerations. The detector is based on a modular design, each layer is a combination of different supermodules. Each supermodule is mechanically independent and it is composed by modules containing the sensor, the electronic readout, the cooling pipe and the local support. The details of the silicon sensor technology are given in Section 2.3.

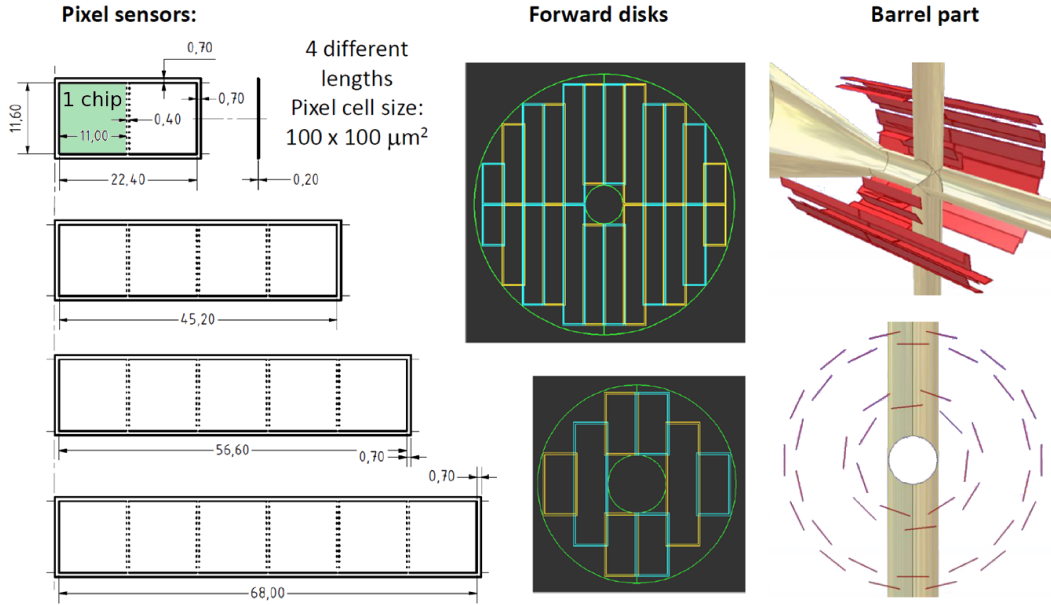


Figure 2.4: MVD pixel modules geometry [41].

The pixel sensor geometry depends on the readout chip size, where the pixel readout cells are arranged in a grid of $\sim 100 \times 100$ cells. A cell size of $100 \mu\text{m} \times 100 \mu\text{m}$

has been chosen in order to comply with the spatial requirements. Two complementary rings of sensors are used to cover the barrel part with a sufficient radial overlap. In the forward disks the sensors are aligned in rows in two complementary planes with a small interspacing along the beam axis. Figure 2.4 shows how different rectangular shaped sensors containing from two to six chips are employed to cover the barrels and the forward disks.

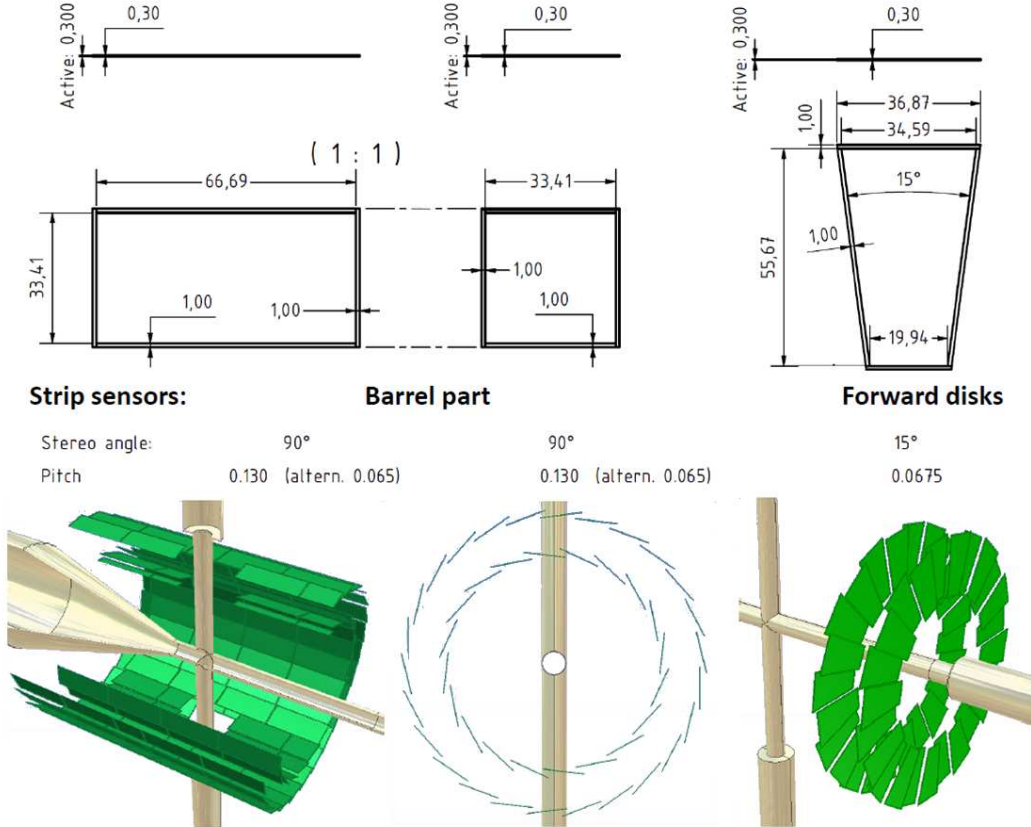


Figure 2.5: MVD strip modules geometry [41].

Since the strip sensor requires a low number of readout channels its geometry is not fixed by the readout chip. For the barrel part two different rectangular shape sensors are employed, while for the peripheral region of the forward disks trapezoidal shape sensors are employed. The rectangular double sided strips have a stereo angle of 90° and a pitch of $130 \mu\text{m}$. The trapezoidal double sided strips have a stereo angle of 15° , in order to place the strips parallel to one sensor edge, and a pitch of $70 \mu\text{m}$ to compensate the worsening of the spatial resolution due to the small stereo angle (Fig. 2.5).

The MVD will operate at atmospheric pressure conditions and at a temperature of $\sim 30^\circ\text{C}$. An active cooling system is envisaged in order to guarantee a stable temperature of the pixel and strip readout electronics. A prototype of the active cooling system has been built and tested (Fig. 2.6). The cooling pipes made of Nickel-Cobalt (2.00 mm external diameter, 1.84 mm internal diameter) are employed with water at 18.5°C as coolant, in an under-pressure mode in order to avoid any damages in case of leakage. The cooling pipes are embedded in the carbon foam of the barrel supermodules and half disk. Resistors are glued on the carbon foam, in order to simulate the readout chips with a thermal dissipation of $\sim 1.5 \text{ W}/\text{cm}^2$. The temperature is measured with an Infra-Red camera and the cooling system keeps the readout chips temperature below 50°C [43].

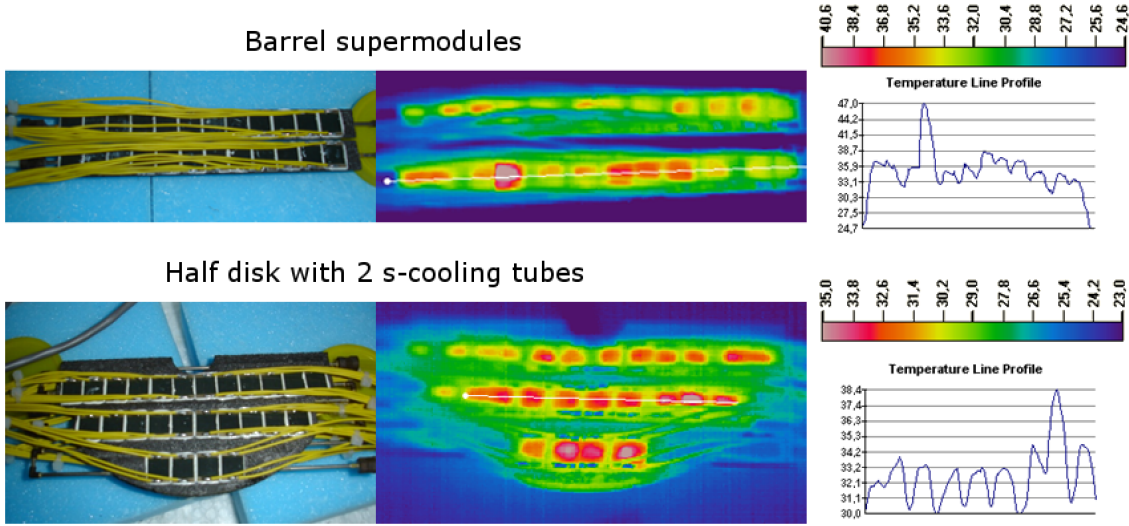


Figure 2.6: Cooling test system for the hybrid pixel detector barrel supermodule and half disk with Infra-Red camera temperature map and temperature line profile [43].

A cylindrical carbon fiber frame holds up all the MVD components [44]. It has a three-point fixation to the supporting structure of the central tracker. The cylindrical frame is subdivided in two half frames, which are mechanically independent. Each half frame supports directly the half strip barrels and the conical structure arranged around the beam pipe. The two pixel barrels are hooked up in a cantilever mode to the conical structure. Three spacers connects the forward pixel disks, the last one is connected through three suspenders at the global frame. The pixel detector module for the forward pixel layers are glued to support half-disks. The strip disks form a mechanical super-module plugged directly to a support ring on the frame. The supporting structures are composed of light weight materials, mainly

carbon and carbon foam, in order to reduce the radiation length. More rigid material are employed only in crucial points in order to strengthen the structure. The routing paths for cooling system pipes, supply cables for sensors and electronics, and signal cables for electronics are carried out in upstream direction. Cables made of aluminum layer deposited on Kapton are envisaged in order to reduce the cable material load. Two cables prototypes with an aluminum thickness of $7\text{ }\mu\text{m}$ and $15\text{ }\mu\text{m}$ and a Kapton thickness of $50\text{ }\mu\text{m}$ and $70\text{ }\mu\text{m}$ respectively, with 1 m of length have been tested without errors for a data transmission rate up to 2 Gb/s [45]. The full details of the MVD mechanical design and the MVD CAD models are given in [46].

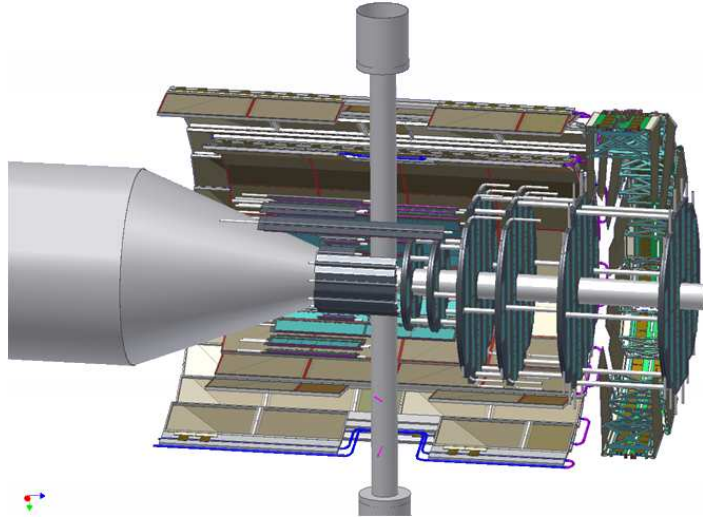


Figure 2.7: MVD layout with the beam and target pipe [41].

2.2.2 MVD simulation results

A detailed CAD model has been developed. The model contains information on the geometry of the MVD components such as electronics, sensors, cooling, support and cabling. In addition the full material list of the MVD components allows for a precise calculation of the radiation length. In the following a list of simulation performed on the PandaRoot framework [47] is reported. These results are important for the validation of the MVD design and for the definition of the readout electronics requirements.

Spatial coverage

The spatial coverage of the MVD depends on the position of the silicon sensors. The MVD spatial coverage simulations are performed with a CAD model which takes into account only the active sensors elements in order to check the efficiency of their arrangement. Charged pions and protons are used as probes. They are generated in a fixed primary vertex point in a momentum range between 150 MeV/c and 1.5 GeV/c in order to study the influence of the particles track bending radius. The tracks are generated with an uniform distribution in the whole solid angle, for each track the number of hits with the active sensors is counted. Figure 2.8 shows the number of hits in function of the initial angles θ (polar) and ϕ (azimuthal).

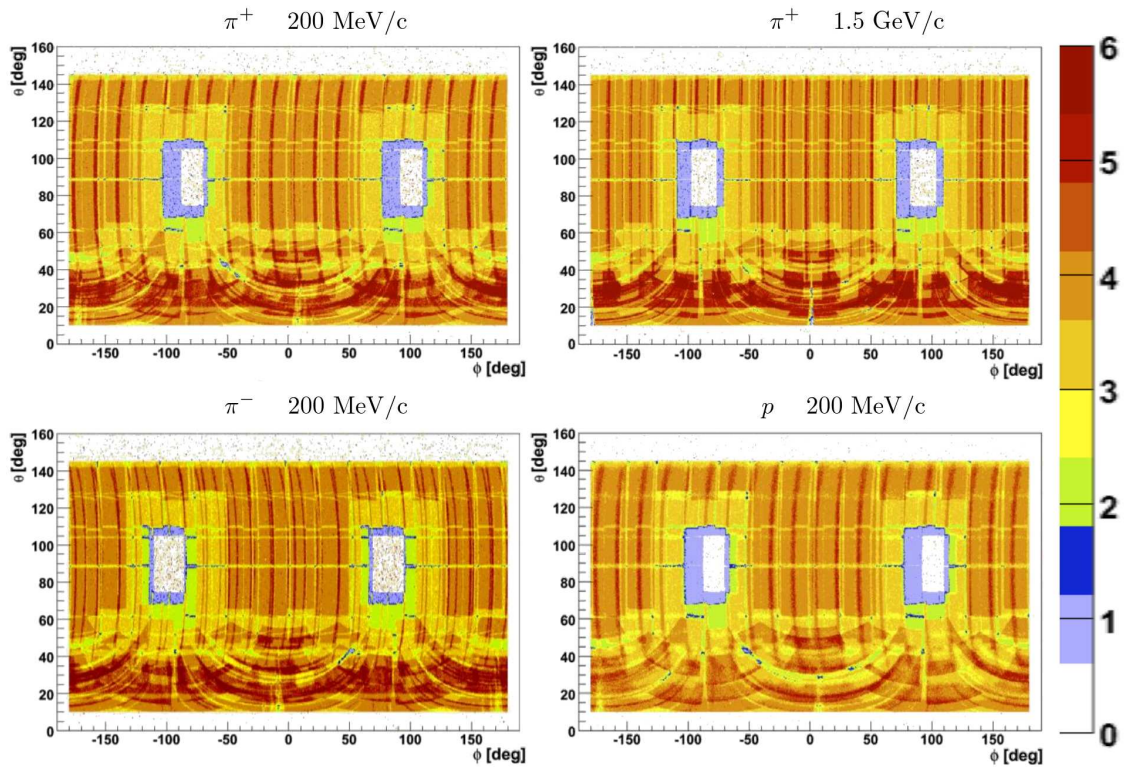


Figure 2.8: MVD spatial coverage [41].

The MVD provides an angular coverage for $3^\circ < \theta < 150^\circ$, the gaps in the diagram at $\theta = 90^\circ$ and $\phi = \pm 90^\circ$ are due to the target pipe crossing. The angles between $\theta = 70^\circ$ and $\theta = 140^\circ$ are covered by all four barrel layers, the number of hits is greater than four in the case of radial overlap of adjacent sensors elements within one barrel layer. In the forward region the strip disks gives a homogeneous coverage

while the pixel disks equipped with double sided rectangular shaped sensors have a circle shaped coverage pattern in the ϕ - θ diagram. At 1.5 GeV/c it is possible to see the projection of the barrel with a periodical pattern in the ϕ direction. At 200 MeV/c the curvature of the particles results in a small deformation of the periodical pattern, which depends on the charge sign and does not affect the MVD overall coverage. The number of hits for slow protons is reduced, since they loss all their energy in the interactions with the first MVD layers. The comparison of the results in the case of π^+ and p at 1.5 GeV/c does not show significant variation due to the mass difference. In this configuration a four hit points coverage is achieved for the 60% of the solid angle region defined by $3^\circ < \theta < 150^\circ$ and $-180^\circ < \phi < 180^\circ$, while considering at least one hit coverage the percentage rises to 96%.

Radiation length

Radiation length simulations are performed in order to map the material budget of the MVD and give a feedback for a further optimization on the detector design. The knowledge of the radiation length X_0 is important for the studies of the electromagnetic interaction of charged particles and photons in the detector material. The energy loss for a charged particle with an initial energy E_0 which travels a distance d in an uniform material with radiation length X_0 is $\Delta E = E_0(1 - e^{-\frac{d}{X_0}})$. From the knowledge of the radiation length it is also possible to calculate the mean free path of high energy photons (> 100 MeV) for e^+e^- pair production $X_{pair} \approx \frac{9}{7}X_0$.

For the simulations a virtual particle which does not interact with material and magnetic field is employed. Therefore this virtual particle is propagated with a straight trajectory from the nominal interaction point over the full solid angles. The radiation length in a certain direction is calculated integrating all the radiation lengths of the materials (from the material definition of the volumes) encountered along the particle path.

Figure 2.9(a) shows the simulation results of the radiation length as a function of the virtual particle propagation angle. A very low material budget in the MVD active region $\theta < 145^\circ$ is achieved. Figure 2.9(b) shows the mapping of the material budget of the MVD components as a function of the polar angle θ . In the MVD active region the average number of the radiation length is $x/X_0 < 10\%$, a $x/X_0 = 14\%$ for angle between $30^\circ < \theta < 50^\circ$ results due to the routing material of the pixel disks. In the forward disks region ($\theta < 22^\circ$) a very low number of radiation length $x/X_0 < 4\%$ is achieved. Analyzing the overall MVD material budget the main contribution comes from cabling ($\sim 38\%$), other contribution are from mechanical support ($\sim 23\%$), silicon sensors ($\sim 20\%$), cooling system ($\sim 14\%$) and readout electronics ($\sim 5\%$). The material budget contribution of the readout electronics is lower than the silicon sensors contribution, because the strip readout chips occupies an area smaller than the strip sensors. Therefore they can be placed independently

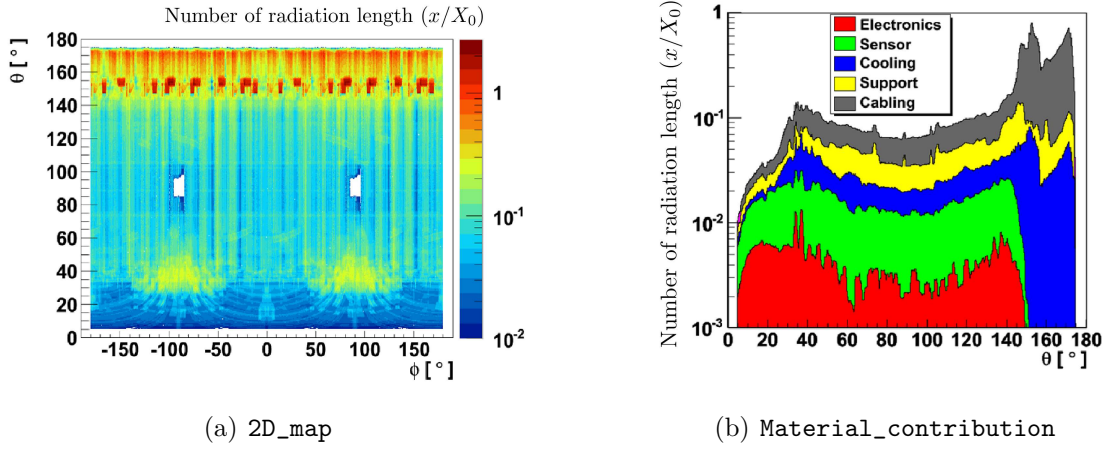


Figure 2.9: (a) Number of Radiation length as a function of the polar and azimuthal angles. (b) Contribution of the different materials to the MVD material budget as a function of the polar angle [46].

with a spatial optimization in order to reduce the overall material budget. This optimization could not be made in the case of hybrid pixel readout chips that are bonded directly on the pixel sensor with an area ratio of 1:1 (see Section 2.3.1).

Hit rate

The estimation of the hit rate that the MVD has to handle is fundamental for the determination of the electronics requirements such as readout speed and maximum tolerable dead time. From the hit rate it is also possible to evaluate the required data link speed and the digital power consumption, which have an influence on the MVD material budget (eg. cabling).

Simulations of $\bar{p}p$ collisions have been performed to study the hit rate as a function of the \bar{p} beam from 1.5 GeV/c to 15 GeV/c in relation of the MVD region [48]. The $\bar{p}Au$ collisions rate is $2 \cdot 10^5 s^{-1}$, and the hit rate of the reaction particles is of one order of magnitude lower than the hit rate in $\bar{p}p$ collisions. The particle hit rate on the silicon sensors in different detector regions reflects the particle track distribution of all outgoing reaction particles.

The highest rate for the strip sensors occurs in the barrel region with a \bar{p} beam at 1.5 GeV/c. Figure 2.10(a) shows the results for all readout channels of the strip sensor located in the foremost part of the third barrel layer (1st strip barrel). The maximum average rate for a strip is $\sim 8 \cdot 10^3$ events per second. The highest rate for the pixel sensors occurs with a \bar{p} beam at 15 GeV/c in the forward region. Figure

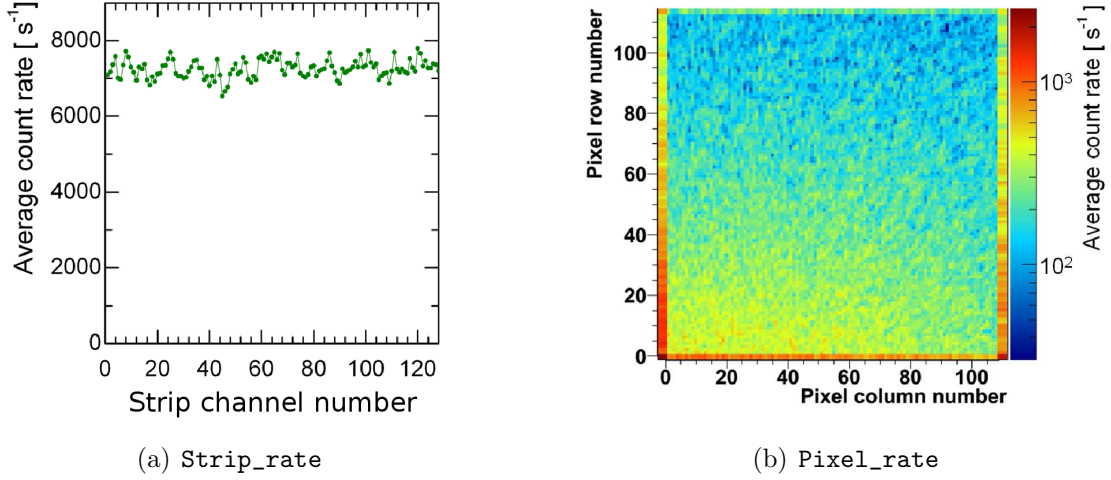


Figure 2.10: (a) Average count rate for all channels of the strip sensor with the highest hit rate. (b) Average count rate for all channels of the pixel readout chip with the highest hit rate [46].

2.10(a) shows the results for the pixel sensor located in the innermost sensor area of the first small disk. At the border of the pixel matrix the count rate is increased because larger pixel are employed, the maximum average hit rate for a pixel is $\sim 10^3$ events per second. The integrated count rate for the MVD is $3.0 \cdot 10^9$ events per second, which result from the sum of $1.8 \cdot 10^9$ events per second in the pixel part and $1.2 \cdot 10^9$ events per second from the strip part.

Resolution

Dedicated simulations have been performed in order to test the MVD spatial resolution and track reconstruction capabilities. A list of the most important results is reported in the following, while the full details are reported in [49].

The contribution of the MVD to the global tracking system has been studied through the momentum reconstruction of π generated at 1 GeV/c in two different detector configurations. The first setup employs the full tracking system (MVD, STT, GEM and forward trackers) while the second setup employs only the outer tracker system (STT, GEM and forward trackers). In the configuration without MVD the resolution is $\sigma(p) = 2.60\%$ and $\sigma(p_t) = 2.90\%$ for the momentum and the transverse momentum, respectively. With the addition of the MVD to the tracking system the resolution is $\sigma(p) = 1.40\%$ and $\sigma(p_t) = 1.42\%$. Therefore the contribution of the MVD to the tracking allows to increase the momentum resolution by a factor of two. Considering the single track reconstruction resolution the MVD

is essential for a resolution along the z direction, while in the xy plane it improves the resolution by about 1 order of magnitude.

For the primary vertex resolution the channel $p\bar{p} \rightarrow \pi^+\pi^-$ has been analyzed with a \bar{p} beam at 15 GeV/c. The two pion production vertex is reconstructed with a resolution $\sigma_{xy} \leq 40\mu m$ in the direction transverse to the beam, and $\sigma_z \leq 70\mu m$ in the longitudinal direction.

The secondary vertices of decaying D meson has been reconstructed in $\bar{p}p \rightarrow D^+D^-$ (at 6.57 GeV/c, 7.50 GeV/c and 8.50 GeV/c). The secondary vertex is reconstructed with a resolution $\sigma_{xy} \leq 35\mu m$ in the direction transverse to the beam, and $\sigma_z \leq 100\mu m$ in the longitudinal direction. Through the analysis of the charged decay products ($D^\pm \rightarrow K^\mp\pi^\pm\pi^\pm$) the exclusive reconstruction of charged D-meson has been performed. The D meson signal has been extracted efficiently from the huge hadronic background, the invariant mass spectrum is reconstructed with a signal to background ratio of 1.4.

2.3 Silicon sensors

Silicon is successfully employed as a material for charged particles tracking detectors in high radiation environment under strong magnetic field, such as at the Large Hadron Collider (LHC) experiments [50]. The sensors are reversed biased p-n junction, fully depleted with a voltage bias in the order of 10^2 V. The energy lost by the crossing charged particle in the sensor volume enables the creation of electron holes pairs. The average energy required for the creation of an electron hole pair is 3.6 eV, thus allowing to achieve a good signal even with a thin silicon layer ($\sim 100\mu m$). The high mobility of both charge carriers results in a very fast collection time (~ 10 ns). The position information is obtained by a segmentation of the electrodes connected to different readout channels realized using microelectronic planar technology. Silicon sensors allows for a compact design with a segmentation density larger than the gaseous detectors of three order of magnitude. In addition they can be produced in big quantities with a very good reproducibility limiting the costs. For the MVD two different silicon sensor are envisaged.

2.3.1 Hybrid pixel sensors

Hybrid pixel sensors [51] are a well established detector technology, and have been employed efficiently for the inner tracking system of LHC detectors [52]. A dedicated research and development activity is ongoing for the realization of custom hybrid pixel sensors for the inner layers of the MVD [53].

Figure 2.11 shows a schematic view of the hybrid pixel sensor and a cross section that shows the hybrid technology under development for the pixel detector of the

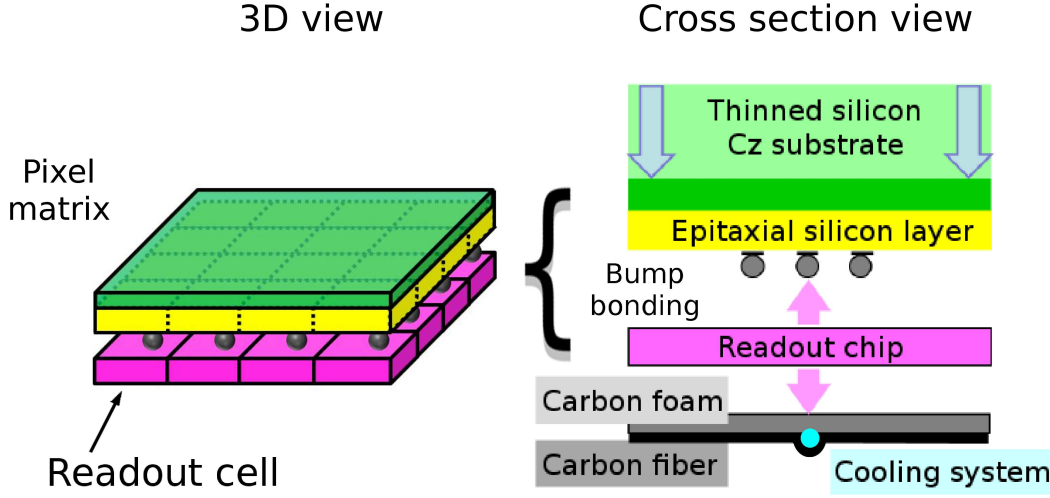


Figure 2.11: Schematic view of the hybrid pixel under development for the pixel detector.

MVD. The epitaxial silicon layer is grown on a silicon Czochralski (Cz) substrate which is almost completely removed. On the surface of the sensor the pixel matrix geometry is defined through the segmentation of the electrodes. Each electrode segment is connected through a tiny conductive bumps to the input pad of the readout cell. The readout cells are arranged in the same matrix structure of the pixel cells, therefore the pixel area is limited by the space required for the readout cell. A custom development is ongoing for the readout ASIC in a CMOS 130 nm technology. The readout chip is glued to the carbon foam, in order to improve the power dissipation, and fixed on the carbon fiber mechanical support. The cooling pipe is embedded in the carbon foam layer.

Three n-epitaxial layers with different thickness ($50\text{ }\mu\text{m}$, $75\text{ }\mu\text{m}$, $100\text{ }\mu\text{m}$) have been deposited on Czochralski substrate thinned to $\sim 50\text{ }\mu\text{m}$ [54]. For the first test the ALICE pixel readout chip [55] has been employed with a pixel size of $50\text{ }\mu\text{m} \times 425\text{ }\mu\text{m}$. The resistivity of the epitaxial layers is between $4\text{ k}\Omega\cdot\text{cm}$ and $5\text{ k}\Omega\cdot\text{cm}$, while the Cz substrate has a n^+ type conductivity (*Sb* dopant) and a resistivity between $0.01\text{ }\Omega\cdot\text{cm}$ and $0.02\text{ }\Omega\cdot\text{cm}$.

Tests with β rays from a ^{90}Sr source have been performed in order to evaluate the signal for a Minimum Ionizing Particle (MIP). Table 2.2 reports the most probable value of the measured Landau for a MIP as a function of the epitaxial layer thickness. The linear trend between the sensor thickness and the ionization charge for a MIP indicates that the charge sharing is not an issue, in fact, even if the pixel width is small, its thickness is of the same order of magnitude.

Epi layer	Thickness [μm]	Resistivity [$\Omega \cdot \text{cm}$]	Ionization charge [e]
Epi-50	49.0 ± 0.5	4060	4070
Epi-75	73 ± 1	4570	5906
Epi-100	98 ± 2	4900	8027
FZ-300	300	-	22500

Table 2.2: Measurement results of the most probable ionization charge for a Minimum Ionizing Particle in epitaxial layer with different thickness. Floating Zone (FZ-300) value given for comparison [54].

Displacement damage test with neutron has been performed at different equivalent fluence values: $5.13 \cdot 10^{13} n_{[1 \text{ MeV}_{\text{eq}}]}/\text{cm}^2$, $1.54 \cdot 10^{14} n_{[1 \text{ MeV}_{\text{eq}}]}/\text{cm}^2$ and $5.13 \cdot 10^{14} n_{[1 \text{ MeV}_{\text{eq}}]}/\text{cm}^2$ corresponding respectively to ~ 1 , ~ 3 , and ~ 10 years of $\overline{\text{PANDA}}$ lifetime with a duty cycle of 50%. After the irradiation the annealing phase at 60° has been observed. The full depletion voltage for all the three epi wafers is $< 6 \text{ V}$ before the irradiation. The type inversion occurs before the annealing phase. The change of the space charge in the depleted region during the annealing phase causes the increase of the full depletion voltage. Measurements with epitaxial sensors with lower resistivity ($\sim 400 \Omega \cdot \text{cm}$) are envisaged. Even if they exhibit a larger full depletion voltage before irradiation they are expected to have type inversion during the annealing phase, thus reducing the increment of the bias voltage. Leakage current measurements for the three epitaxial sensors have been performed. After the irradiation at the maximum fluence the leakage current is below 50 nA/pixel (for a pixel size of $100 \mu\text{m} \times 100 \mu\text{m}$) and it decreases by a factor of 2 after 10 days of annealing. These results represent the worst case estimation of the leakage current, because during the test a fluence expected in 10 year is given in 1000 s, while during the $\overline{\text{PANDA}}$ experiment irradiation phases will be alternated by annealing phases.

2.3.2 Double sided strip sensors

The silicon strip sensors have a one dimensional electrode segmentation, two layer of strip sensor are employed for a two dimensional spatial information. The strips are rectangular shaped, their width (pitch) determines the spatial resolution. The angle between the strips of the two layers is called stereo angle.

The employment of the strip sensors make possible the reduction of the number of readout channels. For example $N_{\text{pixel}} = \frac{A}{w^2}$ pixel readout channels are required to cover a square area A with a spatial resolution w . With $N_{\text{strip}} = 2\sqrt{N_{\text{pixel}}}$ strip readout channels it is possible to cover the same area with the same resolution. The main drawback of the strip sensors is the ghost hit effect depicted in Figure 2.12. When two particles hit the sensor, the first layer gives the coordinates x_1 and x_2 while the second layers gives the coordinates y_1 and y_2 . If the particles arrives

at the same time it is not possible to associate correctly without any assumption the couples of coordinates (x_1, x_2) and (y_1, y_2) . In addition to the hit coordinates (x_1, y_1) and (x_2, y_2) , also the ghost hits (x_1, y_2) and (x_2, y_1) are reconstructed. Double sided strips sensors (DSS) could be efficiently employed in regions with a low hit rate such as the outer layers of the MVD. Thanks to the reduced number of readout channels it is possible to reduce the material budget with respect to the pixel detector.

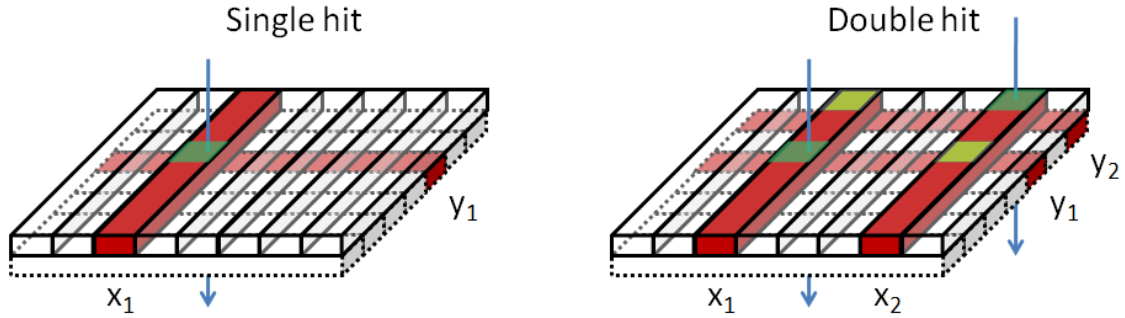


Figure 2.12: Ghost hit during a double hit on a double sided strip sensor.

A test station has been setup at the University of Bonn for the functional characterization of DSS sensors and connected fronted electronics [56]. Its modular design allows for the test of different sensors and electronic readout chips. The functionality of the test station has been verified using the APV25 front end chip [57] and strip sensors with a thickness of $300\ \mu\text{m}$, a side length of $2\ \text{cm}$, a pitch of $50\ \mu\text{m}$ and a stereo angle of 90° (Fig. 2.13). For the final version a sensor thickness of $200\ \mu\text{m}$ is envisaged.

A tracking station has been implemented with four boxes containing DSS detectors in order to study the tracking capabilities and energy loss measurement of charged particles. The FPGA based readout system enable for the real time data processing with hit detection and event building capabilities [58]. The tracking station has been tested in different beam conditions [59], the boxes containing DSS could be moved along the longitudinal direction in a range of $185\ \text{cm}$, and one box could be also rotated. Figure 2.14 shows the energy loss for electrons at $4\ \text{GeV}$ measured at different angles between the sensor plane and the beam direction. It is possible to see that increasing the rotation angle the Landau energy loss peak position increases since the thickness of transversing material is increased.

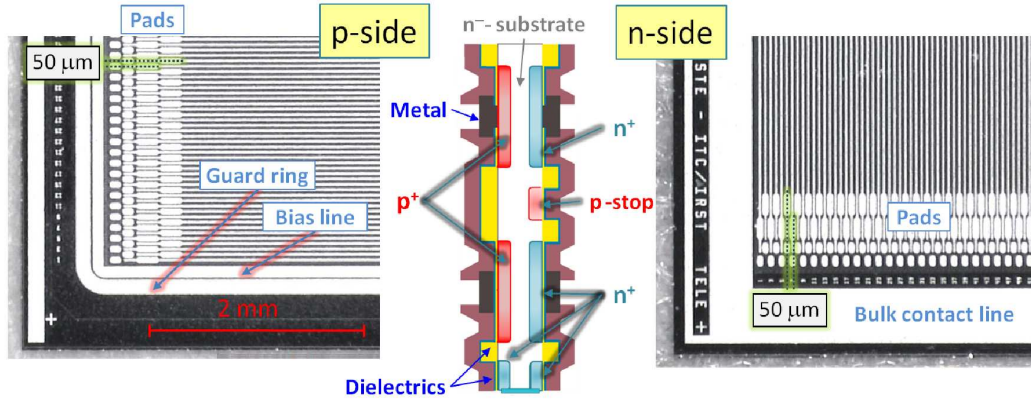


Figure 2.13: Photographs of the metalization on both sides of a DSS test sensor [46].

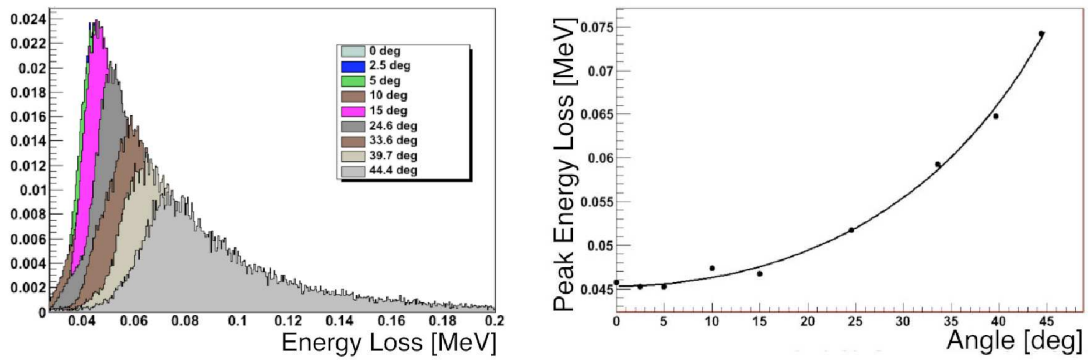


Figure 2.14: Energy loss measurement with the tracking station [59].

Chapter 3

Hybrid Pixel ASIC Architecture

Over the last two decades, pixel detectors have been employed in several scientific fields where two dimensional spatial detection with high resolution of charged ionizing particles and photons is required. Hybrid pixels are employed in the innermost tracking layers of high energy and nuclear physics experiments and have made significant progress in the recent years. Hybrid pixel detectors allows for a separate optimization of sensor and readout electronics. The exponential development of microelectronics has made it a key enabling technology in the development of tracking detectors. The hybrid pixel front end electronics has to be compact and fully optimized to the parameters of the detector, thus it is implemented with application specific integrated circuits (ASICs). Deep submicron CMOS technologies are employed for the design of mixed signal ASICs where low-level analog signals and digital activity coexist in the same monolithic system. The mixed signal approach allows for a more robust system since the information is sent out digitally to the DAQ system. It is possible to design a reliable system with an high integration density able to afford an high data rate, thus limiting the cost of large detection systems. The implementation of analog and digital circuitry on the same chip requires a careful optimization in order to reduce the coupling of spurious switching noise from digital circuits into the sensitive analog building blocks. Last but not least, CMOS technologies allows for the design of radiation hard ASIC. In this chapter the architecture of ToPix, the custom ASIC for the readout of the $\overline{\text{P}}$ ANDA hybrid pixel detector, is described. Key aspects are discussed with a special focus on the Time over Threshold (ToT) technique which is employed for the charge digitization.

3.1 Design aspects

3.1.1 Pixel Readout ASIC Requirements

The pixel readout ASIC has to provide for each hit a simultaneous position, time and energy loss measurement. The specifications for the readout electronics depends on the requirements of the MVD given in section 2.1.4. The fundamental parameters to take into account are the $\overline{\text{PANDA}}$ radiation environment and the close proximity of the MVD to the interaction point.

A pixel size of $100\ \mu\text{m} \times 100\ \mu\text{m}$ has been chosen based on the study of track performance. Since each readout cell has to be bump bonded to the sensor, the readout cell matrix has to respect the same geometry of the pixel sensor matrix. Therefore the readout cell has to fit in an area of $100\ \mu\text{m} \times 100\ \mu\text{m}$. To guarantee the reliability of the system, time and charge digitization has to be performed at the pixel cell level in order to transmit only digital information outside the pixel cell. For a Minimum Ionizing Particle (MIP) in a $100\ \mu\text{m}$ epitaxial sensor an ionization charge of $\sim 1.3\ \text{fC}$ is expected [54]. The measurement of ionization charges up to $50\ \text{fC}$ allows for the identification of protons with a momentum down to $\sim 200\ \text{MeV}/c$. In order to maintain a constant temperature a liquid cooling system is foreseen. Even though a power density of $\sim 1\ \text{W}/\text{cm}^2$ can be tolerated in the worst case, a strong effort will be made to reduce the power consumption of the front-end electronics and hence the material budget. Given the high pixel density ($10^4\ \text{pixels}/\text{cm}^2$), a limit of $15\ \mu\text{W}$ has been put on the analog cell. It is foreseen to employ a p-in-n epitaxial sensor, which should give an adequate radiation hardness with a simple geometry. The possibility of using already well known n-in-n sensor employed in LHC as a backup solution is however considered. Therefore, the front-end is designed to be compliant with sensors of either polarity. A dedicated selection bit allows to program key circuit parameters in order to optimize the performance for each polarity. The noise level is mainly limited by the input transistor thermal noise. An Equivalent Noise Charge of ~ 200 electrons is a good trade off between power consumption and minimum detectable charge. The readout electronics has to work in the $\overline{\text{PANDA}}$ radiation environment, with an accumulated Total Ionizing Dose (TID) of $10\ \text{Mrad}$ in 10 years. Hit rate simulations studies estimate a maximum average rate of $\sim 10^3$ events per second on a single pixel cell. The system will be self-triggered and all the events above a given threshold have to be read out, leading to an high data rate. A time resolution lower than the event rate of $2 \cdot 10^7/\text{s}$ is required. Table 3.1 summarizes the specifications for the pixel readout cell and Table 3.2 summarizes the ASIC specifications.

Pixel Size	$100\ \mu\text{m} \times 100\mu\text{m}$
Noise Level	$200\ e^- \text{ rms}$
Linear dynamic range	Up to 50 fC
Power consumption	$< 20\ \mu\text{W}$
Input polarity	Selectable
Leakage compensation	Up to 50 nA

Table 3.1: Pixel readout cell requirement

Trigger	Self triggering
Active area	$O(1\ \text{cm}^2)$
Data rate	$O(0.8\ \text{Gbit/s})$
TID tolerance	10 Mrad
Neutron fluence tolerance	$5.13 \cdot 10^{14}\ n_{[1\ \text{MeV}_{\text{eq}}]}/\text{cm}^2$
Time resolution	$< 10\ \text{ns}$

Table 3.2: ASIC specifications

3.1.2 Motivation for a custom development

Deep-submicron CMOS processes have been used to implement successfully radiation-tolerant custom integrated circuits for High Energy Physics experiments. The experiments at the Large Hadron Collider (LHC) at CERN employ different front-end chips for the pixel sensors of the inner tracking detectors [51]. Table 3.3 shows a comparison between the LHC experiments readout chip performances and the $\overline{\text{P}}\text{ANDA}$ MVD pixel readout chip requirements.

Experiment	ALICE	ATLAS	CMS	$\overline{\text{P}}\text{ANDA}$ req.
Readout chip	ALICE1LHCB [55]	FEI3 [60]	PSI46 [61]	ToPix
Read-Out	binary	ToT	analog	ToT
Clock frequency	10 MHz	40 MHz	40 MHz	155.52 MHz
Power density	$0.51\ \frac{\text{W}}{\text{cm}^2}$	$0.33\ \frac{\text{W}}{\text{cm}^2}$	$< 0.3\ \frac{\text{W}}{\text{cm}^2}$	$< 0.2\ \frac{\text{W}}{\text{cm}^2}$
Self Triggering	Limited	Limited	Limited	Yes
Pixel Size	$50 \times 425\ \mu\text{m}^2$	$50 \times 400\ \mu\text{m}^2$	$100 \times 150\ \mu\text{m}^2$	$100 \times 100\ \mu\text{m}^2$

Table 3.3: Comparison between pixel readout chips. In 2010 an upgraded version of the ATLAS pixel readout chip has been produced [62].

In the $\overline{\text{P}}\text{ANDA}$ experiment the readout system has to continuously digitize the

detector data (trigger-less) in order to run the experiment at a high rate. The existing chips are optimized for LHC experiments where there are essentially minimum ionizing particles. In $\overline{\text{PANDA}}$ a large number of low-momentum particles are expected. Since they will have lost more energy in the silicon sensor, a higher charge dynamic range is required. In addition, the high track density, low material budget and custom cell size have led to the choice of a custom solution for the front-end chip. A dedicated development offers in addition the possibility of optimizing the chip size in order to cover the sensitive area with a minimal set of different modules (see section 2.2.1).

3.1.3 Technology choice

The development of the CMOS technology follows the industry trends, which are focused on the production of microprocessors and memories. After radiation hardness tests the commercial CMOS processes are employed for the ASIC design for nuclear and high energy physics applications. The technology choice for the ASIC design is guided by the power and area constraints and the necessity for a good radiation hardness. These factors in addition to the requirement for a cutting edge technology even after the several years necessary for the research and development phase leads to the choice of a CMOS 0.13 μm technology for the production of the front-end chip. The readout chips of the LHC experiments have been designed in a CMOS 0.25 μm process. This technology has proved to be radiation tolerant only with radiation hardening layout techniques such as enclosed layout transistors [63] which need about a double area on silicon in comparison with a standard layout transistor. Given the reduced gate oxide thickness, CMOS 0.13 μm technology shows a better radiation tolerance even without hardness by design solutions [64]. The reduction of transistor sizes and the increase of the working frequency enhance the circuit susceptibility to the Single Event Upset effect, therefore a dedicated protection is required for the sensitive digital blocks. In a digital circuit, the power consumption is $P = fC_LV_{\text{supply}}^2$, where f is the bit commutation frequency, C_L the gate capacitance and V_{supply} the voltage supply. In our case, due to the high event rate, the digital logic will have a very low idle time. The power supply of $V = 1.2\text{ V}$ in CMOS 0.13 μm technology allows the reduction of the power dissipation. The minimum gate length of 130 nm allows for a high component density for the digital logic.

Analog design in deep submicron technologies

As previously mentioned CMOS technologies are driven by the need of the digital circuits to increase the performance/cost ratio. Technology scaling is aimed for a fast transition between discrete voltage levels with the reduction of transistor size and power consumption. For the analog circuits [65] transistor parameters

like transconductance and output resistance are of utmost importance. For these reasons analog design in deep submicron technology requires a particular attention. The main points are discussed below. Figure 3.1 shows the unity gain frequency (f_T) and intrinsic gain (g_m/g_{ds}) for a MOS transistor with minimum gate length as a function of the technology node. Going to small feature size the transistor speed increases but the transistor intrinsic gain decreases leading to a speed gain tradeoff.

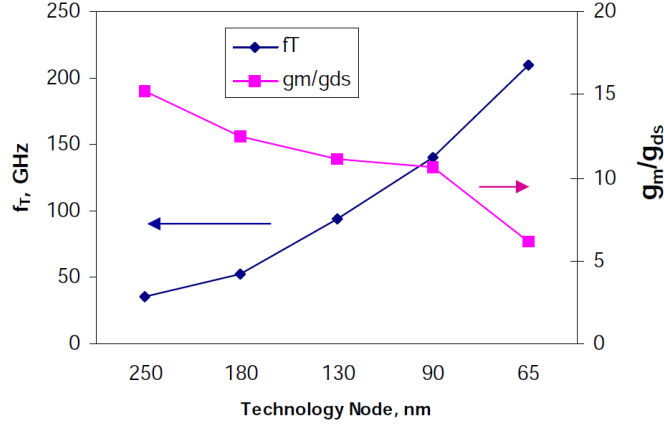


Figure 3.1: Speed and gain for minimum gate length devices dependence on technology node [66].

When transistors operate in strong inversion the source-drain saturation current $I_{ds_{SI}}$ has a quadratic dependence from the gate-source potential V_{gs} :

$$I_{ds_{SI}} = \frac{KP}{2} \frac{W}{nL} (V_{gs} - V_{th})^2 \quad (3.1)$$

where $KP = \mu C_{ox}$ is the transconductance parameter, V_{th} the transistor threshold, W and L are the transistor channel width and length, respectively. The correction factor n depends on the ratio between the gate-channel capacitance C_{gc} and bulk-channel capacitance C_{bc} : $n = \frac{C_{bc}}{C_{gc}} + 1$. When transistors operate in weak inversion the source-drain saturation current $I_{ds_{WI}}$ has an exponential dependence from the gate-source potential V_{gs} :

$$I_{ds_{WI}} = \frac{W}{L} I_{d0} e^{\frac{V_{gs}}{n \frac{k_B T}{q}}} \quad (3.2)$$

where I_{d0} is the current coefficient, k_B is Boltzmann constant and T the absolute temperature.

The transition between weak and strong inversion occurs at the intersection point between $I_{ds_{SI}}$ and $I_{ds_{WI}}$:

$$I_{ds_{WI \rightarrow SI}} = \frac{KP}{2} \frac{W}{nL} \left(2 n \frac{k_B T}{q} \right)^2 \quad (3.3)$$

Therefore a MOS transistor works in strong inversion for an overdrive voltage:

$$V_{gs} - V_{th} \geq 2 n \frac{k_B T}{q} \quad (3.4)$$

In CMOS 0.13 μm technologies $n \approx 1.3$, at a temperature of 300 K the overdrive voltage required to work in strong inversion is ~ 70 mV. It is important to note that the transistor moves from weak inversion to strong inversion with a smooth transition, therefore the above calculated transition point is a very simplified approximation.

The transistor power efficiency can be evaluated by calculating the transconductance ($g_m = \frac{dI_{ds}}{dV_{gs}}$) to the drain-source current (I_{ds}) ratio:

$$\left(\frac{g_m}{I_{ds}} \right)_{SI} = \frac{2}{V_{gs} - V_{th}} \quad (3.5)$$

$$\left(\frac{g_m}{I_{ds}} \right)_{WI} = \frac{1}{n k_B T / q} \quad (3.6)$$

In weak inversion the transistor power efficiency does not depend on the transistor overdrive voltage $V_{gs} - V_{th}$ and it is constant for a fixed temperature. It is possible to verify that in weak inversion the power efficiency is larger than in strong inversion by substituting the condition (3.4) in equation (3.5).

In some circuit blocks like current mirrors, the fundamental parameter is the matching and not the g_m value. The main contribution to the current mirror mismatch comes from the fluctuation of the threshold voltage ΔV_{th} . Using the small signal model the correspondent current variation is:

$$\Delta I_{ds} = g_m \Delta V_{th} \quad (3.7)$$

The calculation of the current mirroring uncertainty $\frac{\Delta I_{ds}}{I_{ds}}$ leads to:

$$\left(\frac{\Delta I_{ds}}{I_{ds}} \right)_{SI} = \frac{2 \Delta V_{th}}{V_{gs} - V_{th}} \quad (3.8)$$

$$\left(\frac{\Delta I_{ds}}{I_{ds}} \right)_{WI} = \frac{\Delta V_{th}}{n k_B T / q} \quad (3.9)$$

Substituting the condition (3.4) in equation (3.8) it is possible to verify that in strong inversion the current mirroring uncertainty is smaller than in weak inversion. Furthermore in strong inversion the mismatch effect can be suppressed by increasing $V_{gs} - V_{th}$. This is the reason why the current mirrors have to work in strong inversion in order to reduce the impact of the threshold dispersion.

In deep submicron technologies to improve the transistor performance the silicon oxide gate thickness is reduced, thus increasing C_{ox} and consequently KP . Therefore

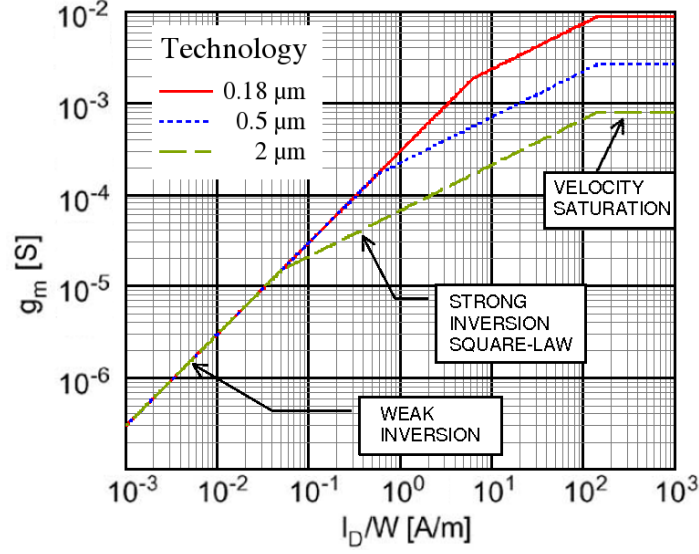


Figure 3.2: Transconductance of NMOS transistor as a function of current density for different CMOS technologies. [67].

the boundary between weak inversion and strong inversion $I_{dsWI \rightarrow SI}$ (see equation (3.3)) moves towards higher currents and a larger L value is required to work in weak inversion for a fixed value of current in comparison with older technologies.

Figure 3.2 shows the relationship between the NMOS transconductance ($g_m = \frac{dI_{ds}}{dV_{gs}}$) as a function of drain current density (I_{ds}/W) for different CMOS technologies. The transconductance is proportional to $(\frac{I_{ds}}{g_m})^\alpha$, where $\alpha = 1$ in weak inversion, $\alpha = \frac{1}{2}$ in strong inversion and $\alpha = 0$ in velocity saturation. Therefore it is possible to recognize the transition point between weak inversion and strong inversion, which occurs at larger current densities for smaller feature size.

The power supply scaling is faster than the scaling of the transistor threshold voltage. This means that the voltage swing on intermediate nodes has to be reduced and only few transistors can be stacked in one branch. Another important parameter to take into account is the transistor threshold voltage matching which plays an important role in multichannel ASICs. The standard deviation of the MOS threshold dispersion is proportional to the inverse of the square root of the transistor area [68]:

$$\sigma_{V_{th}} = \frac{A_{VT}}{\sqrt{WL}} \quad (3.10)$$

where A_{VT} is a technology dependent constant and is roughly proportional to the oxide thickness, which scales with the technology feature size.

Figure 3.3 shows that for the minimum transistor length $\sigma_{V_{th}}$ increases, therefore

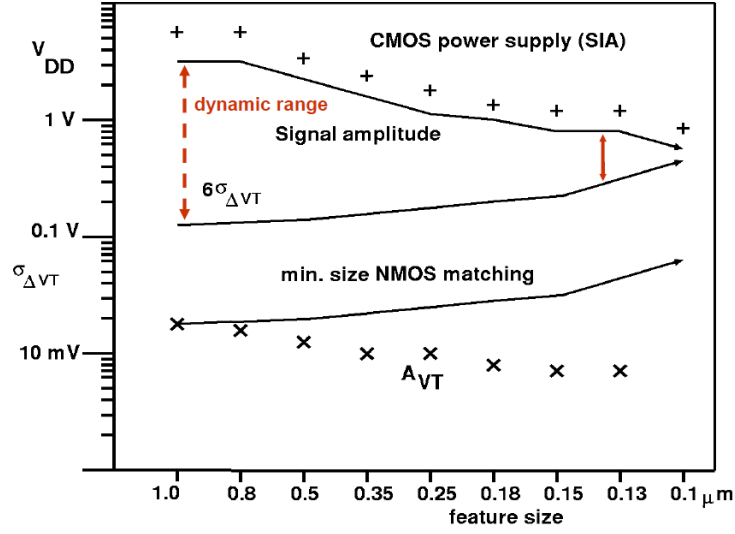


Figure 3.3: Evolution of power supply voltage and the measured NMOS threshold matching factor A_{VT} through various process generations. The available signal swing (upper solid line) is derived by taking 90% from the nominal power supply and subtracting a threshold voltage and $4k_B T/q$ gate overdrive [68].

in order to preserve the relative matching $\sigma_{V_{th}}/V_{supply}$ larger transistors have to be employed. To overcome the signal swing reduction new approaches have to be adopted in the analog signal processing, like, for example the Time over Threshold (ToT) described in section 3.3.

The analog layout geometry in deep submicron technologies has a strong impact on the circuit performance [69]. With the reduction of the feature size more strict rules have to be observed in order to guarantee the system reliability. Symmetry is an important factor for the transistor matching, process gradients and device location with respect of the other blocks have to be taken in account as well. For these reasons a careful floorplanning is required. Given the small feature size, the parasitic components could have a high relative value in comparison with the designed parameters. Therefore an accurate transistor sizing and evaluation of the interconnections is required, and an exhaustive study of the extracted circuit is fundamental to verify the circuit performance. In mixed signal designs the substrate noise due to the fast switching of the digital circuitry can affect the sensitive analog block. The CMOS 0.13 μm processes offer the triple well as a standard option which is fundamental for the isolation of NMOS transistors bulk from the global chip substrate, thus reducing the noise pick up. The presence of an increased number of interconnection metal layers (~ 8) allows for a better management of the wire parasitic coupling.

3.2 ToPix architecture

The ToPix floorplan foresees a matrix of 116×110 pixel readout cells with a size of $100\ \mu\text{m} \times 100\ \mu\text{m}$, thus covering a $1.276\ \text{cm}^2$ active area. Each pixel readout cell embeds the analog and digital electronics for the time and charge digitization. The pixels are arranged in 110 columns, composed of 116 pixel cells sharing the same buses and control lines. Each column is controlled by a peripheral logic which can read and write the configuration and read the event data stored in the pixel registers. The master clock frequency is 155.52 MHz. The choice of this particular frequency stems from the reuse in the $\overline{\text{P}}\text{ANDA}$ clock distribution system of building blocks derived by the present trigger system of the COMPASS experiment at CERN. Finally the data are multiplexed on two 311.04 Mbit/s serializers by a data transmission logic. The columns are readout with a scheme similar to the one implemented in the FEI3 chip of ATLAS [60] [70].

3.2.1 Pixel readout cell

The pixel readout cell is a mixed signal block, the analog readout chain interfaces to the sensor and the digital part implements the pixel control logic and the data registers. The pixel readout architecture is based on the Time over Threshold (ToT) technique [71] which makes a low power charge digitization possible. This approach has been selected due to its well-known capability of providing linear measurements also when the main amplifier is saturated [72], and it will be described in detail in section 3.3.

Analog readout chain

The input stage is a Charge Sensitive Amplifier (CSA) which receives the current signal from the pixel sensor. The CSA integrates the current signal collecting the charge on its feedback capacitor. The value of the injected charge is measured through the time spent to discharge the feedback capacitor with a constant current source. The leakage current compensation implemented through simple Alternate Current (AC) coupling between the sensor and the read-out input node would require a filtering capacitance of $\sim 100\ \text{pF}$, which is not possible to implement due to the strict space limitations. For this reason a baseline restorer is required to compensate the Direct Current (DC) sensor leakage current. Two feed-back networks are used for providing the constant discharge current and to control the baseline, making it insensitive to the sensor leakage. This approach allows an independent optimization of the two stages. One of the interesting features of this readout cell is the ability to compensate a leakage current up to 50 nA. The baseline restorer consist in a low pass differential amplifier which sense the difference between the CSA output voltage and

the baseline reference voltage. The differential amplifier output controls a current source that injects the leakage compensation current into the input node. Since the output signals can have a long duration ($\sim 10 \mu\text{s}$), the leakage compensation feedback has to be low bandwidth ($\sim 10 \text{ Hz}$) in order to avoid cutting these signals. The comparator has as input the output signal of the CSA and a preset threshold voltage. When a current pulse is presented at the CSA input C_f is being charged and the CSA output goes over the threshold. When the CSA is completely discharged the signal goes below the threshold to the baseline value. The threshold value has to be fixed not too close to the baseline in order to avoid picking up the noise, and not too far from the baseline in order to be able to detect small values of charge. A coarse value of the threshold common for all the pixels is fixed, and a fine tuning is possible on a pixel by pixel basis by a local 5 bit DAC. The width of the pulse generated by the comparator, the Time over Threshold (ToT), is given by the ratio of the charge injected by the pixel detector to the discharging current value (Equation (3.19)). This linear relationship is valid even if the CSA is saturated, provided that I_{dis} is constant during the discharging phase.

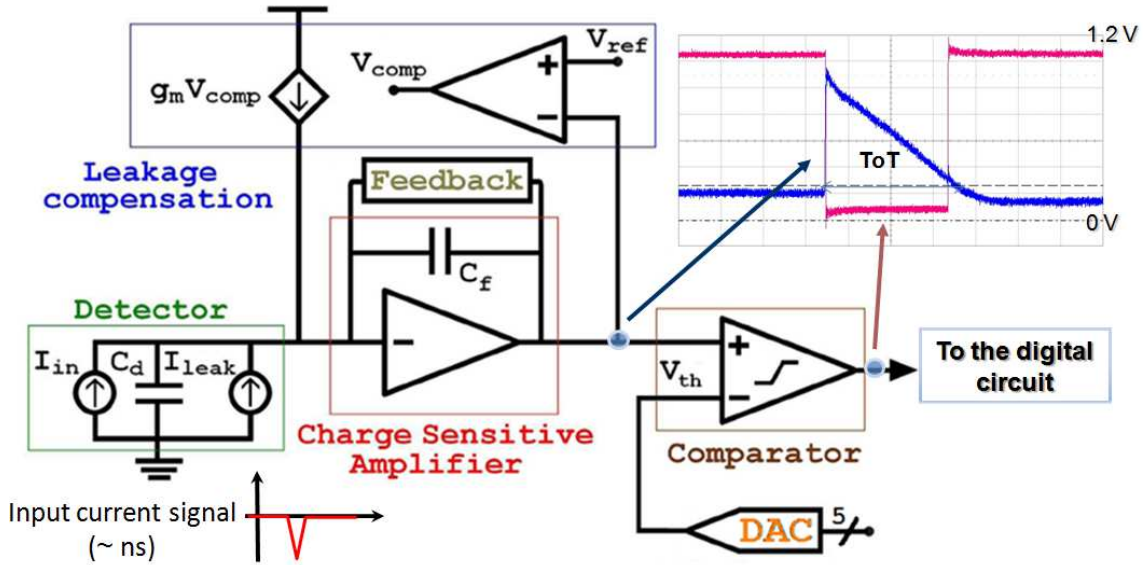


Figure 3.4: Analog ReadOut Channel

Figure 3.4 shows the building blocks of the analog readout channel. The detector is modeled with a variable current generator (I_{in}) which generates the current due to the sensor charge collection, a constant current source (I_{leak}) for the leakage current and the detector capacitance ($C_d \approx 200 \text{ fF}$). The transistor level implementation of the analog blocks will be described in chapter 5.

Pixel control logic

To perform the ToT digitization a global 12 bits timestamp is distributed in parallel to every pixel readout cell. The control logic receives as input the comparator signal (*pixel_in*) from the analog readout. When *pixel_in* switches from logical state 0 to 1 and from 1 to 0 the corresponding timestamp value is stored in the 12 bit leading-edge register and 12 bit trailing-edge register, respectively. Then the busy flag is activated to indicate that the data is ready to be readout. The value in the leading-edge register gives the particle hit timing and the difference between the two registers gives the ToT information. The control logic also manages the busy logic and the readout commands. An additional 8 bit register is employed for the configurations on a pixel by pixel basis. It stores 5 bits for the comparator threshold DAC, 1 bit to enable the comparator output on the chip output pad, 1 bit to enable the internal test charge injection and 1 bit to mask the comparator output in case of a noisy pixel. These registers are implemented with Triple Modular Redundancy (TMR) in order to be Single Event Upset (SEU) tolerant. The configuration register, which is fundamental for the proper setting of some parameters in the readout circuit, has a feedback for the automatic error correction. The trailing edge and leading edge registers stores the data only for a limited time (up to $\sim 10 \mu s$), thus they implements only the TMR error detection.

The *busy_out* signal is generated with an OR between the busy flag and *busy_in* which is in turn the *busy_out* of the previous cell. In this way an OR chain is propagated along the column, therefore a column busy signal is generate when at least one cell is busy. While *read_cmd* = 1 the read mode is enabled for the cell with the highest priority which has both leading edge and trailing edge data, that is with *busy_in* = 0 and *busy_out* = 1. When the read mode is enabled the hard wired pixel address (*addr_out*) is sent over the 7 bit address bus (*addr_out*), and the *read_le* and *read_te* signals transfer respectively the leading edge register and trailing edge register on the 12 bit data bus (*data_out*). The *freeze* = 1 signal prevent the pixel to enter in read mode in order to avoid that high priority pixels are always in read mode thus denying to low priority cells the possibility to be read out. However even if *freeze* = 1 the cell can be read if it has already stored the leading edge and it is waiting for the trailing edge.

When *config_mode* signal is asserted, all pixels are set in busy mode. The pixel with the highest priority loads its address in the address bus. In this case the *read_te* and *read_le* commands are employed respectively to read and write the configuration register. When *config_mode* is released, the cell reset its busy and the following pixel can be configured. In each configuration cycle the pixels are accessed in sequence from the cell with the highest priority to the lowest one.

All the operations of the pixel control logic are based on 7 states: 1 - leading edge detected, 2 - leading edge and trailing edge detected, 3 - waiting to be the readout,

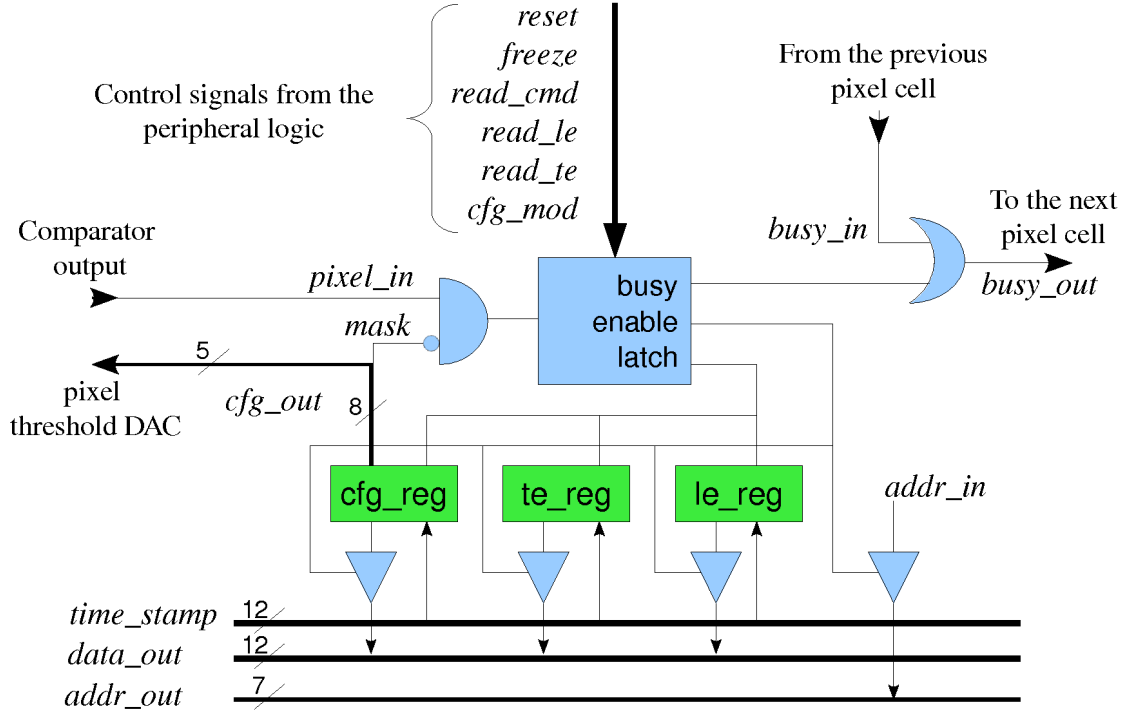


Figure 3.5: Pixel control logic

4 - waiting for configuration, 5 - writing data on the buffer, 6 - reading/writing configuration register, 7 - waiting after configuration. The states are stored on 2 D flip-flops and 5 latches.

3.2.2 Peripheral logic

The pixel matrix is under the pixel sensor active area. A peripheral logic, placed outside the active area, execute the pixel matrix readout and the off-chip data transmission. The pixel cells are arranged in columns of 116 elements. The functional readout unit is the double column. Two adjacent columns shares the timestamp, address and data buses.

The double column signals are controlled by the Column Readout Control Unit (CRCU). The CRCU generates for each column the *freeze*, *read_cmd*, *read_le* and *read_te* signals. The *reset*, *cfg_mode* and 12 bits *time_stamp* are shared among the two columns. All the signal are differential and transmitted along the column by dedicated drivers (ColDriver). The CRCU receives from the double column the 7 bits *addr_out* and the 12 bits *data_out*. These signals are on differential buses and

Signal name	Direction	Type	Description
<i>reset</i>	input	differential	Reset all D flip-flops and latches
<i>pixel_in</i>	input	single ended	Comparator signal from the analogue part. The two edges of this signal activates the load signal of the leading and trailing edge registers, respectively.
<i>freeze</i>	input	differential	Prevents pixels from asserting its own internal busy unless it is already asserted.
<i>read_cmd</i>	input	differential	Set the pixels in read mode.
<i>read_le</i>	input	differential	In read mode activate the leading edge register output enable. In config mode activate the configuration register output enable.
<i>read_te</i>	input	differential	In read mode activate the trailing edge register output enable. In config mode activate the configuration register load.
<i>cfg_mode</i>	input	differential	Set the pixels in config mode.
<i>busy_in</i>	input	single ended	Busy in from the higher priority pixels.
<i>busy_out</i>	output	single ended	Busy out to the lower priority pixels.
<i>time_stamp</i>	input	differential	12 bits time stamp bus.
<i>addr_in</i>	input	single ended	7 bits internal pixel address (hard-wired).
<i>addr_out</i>	tri-state out	differential	7 bits address bus.
<i>data_out</i>	tri-state out	differential	12 bits data bus.
<i>cfg_out</i>	output	single ended	8 bits configuration bus (internal).

Table 3.4: Pixel cell control unit [73].

are readout by two separate sense amplifiers banks. The address sense amplifiers bank is controlled by *precharge_A*, *en_A* and *latch_A*. The data sense amplifiers bank is controlled by *precharge_D*, *en_D* and *latch_D*. In addition, the CRCU receives from each column the single ended *busy* signal.

Each event stored in the pixel cell register requires 32 bits: 1 bit to identify the column of the double column, 7 bits for pixel address, 12 bits for leading edge and 12 bits for trailing edge. The 32 bits data is Hamming encoded in a 37 bit word and it is stored on the Double Column Buffer (DCB) containing a 32 level deep FIFO

(First In First Out). The data is decoded at the buffer output. The Hamming encoding allows to detect up to two simultaneous bit errors, and correct single-bit errors. The CRCU generates the readout commands when *busy* = 1 and the DCB have space for the command allocation.

Figure 3.6 shows the 8 phases of the column readout sequence:

0. In idle state all signals are low except the two precharge signals which are active. The readout can be started when freeze is released and a busy is active (ie. at least one cell is ready to be readout).
1. The readout phase starts when *read_cmd* and *read_le* signals are set to 1, thus the address of the highest priority pixel is sent on the *addr_out* bus and the leading edge data is sent on the *data_out* bus. The two precharge signals are set to 0.
2. In order to allow the storage of the bus values on the sense amplifiers *en_A* and *en_B* are set to 1.
3. The output of the sense amplifiers is stored in a temporary register, by setting *latch_A* and *latch_D* to 1.
4. The leading edge phase is terminated by setting *read_le*, *en_D* and *D_latch* signals to zero. The *precharge_D* signal is set to one. Since the readout time is much smaller compared with the average time between two events, this phase lasts 2 clock cycles in order to give enough time for the sense amplifier stabilization.
5. The pixel trailing edge data is sent to the data bus by setting *read_te* to 1 and *precharge_D* to 0.
6. The bus value with the trailing edge data is stored in the sense amplifiers by setting *en_D* to 1.
7. The output of the sense amplifier data bank is stored in the temporary register by setting *latch_D* to 1.
8. The read phase is terminated by setting *read_cmd* to 0 and the two precharge signals to 1. The temporary register is written in the DCB.

The 12 bits *time_stamp* bus is driven by the timestamp counter. A timestamp counter cycle period is:

$$T_{ts} = \frac{2^{12}}{f_{clock}} = \frac{4096}{155.52 \text{ MHz}} = 26.34 \mu\text{s} \quad (3.11)$$

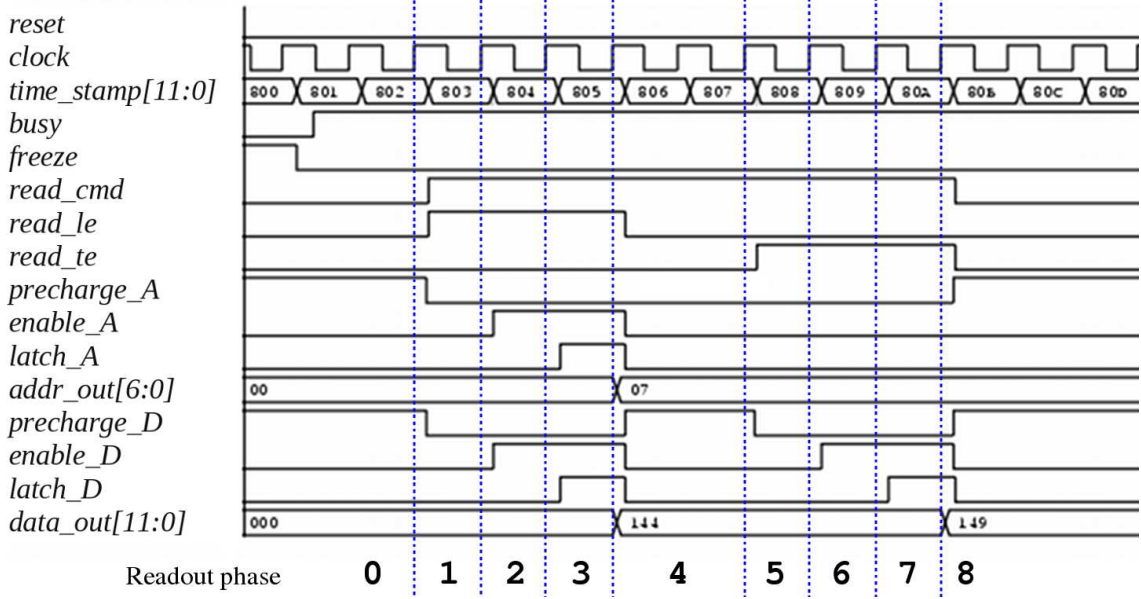


Figure 3.6: CRCU readout cycle

If during a counter cycle there are no events it is not possible to associate the events with the correct counter cycle. To sort out the data from different count cycles two solutions are under consideration. One possibility is a dummy event generation at each end of counter cycle, another possibility is to encapsule the event data with cycle identification code.

In configuration mode a similar cycle is performed with *cfg_mode* = 1 to read and write the pixel configuration registers. The data to be written on the pixel configuration registers are driven on the 12 bits *time_stamp* bus, the pixel configuration registers data is read on the 12 bits *data_out* bus.

The pixel matrix is composed of 55 double columns. The output of the selected DCB is connected to a 32 bits shift register. When valid data are present on the serial output (*data_valid* = 1) the transmission is started automatically unless *data_wait* is set to 1. The data is transmitted via two 310.5 Mbit/s serial links. The working frequency is doubled by considering both clock edges. The chip configuration is made via three serial link signals which controls the 17 bits Configuration Shift Register (CSR): *serial_in* is the CSR input, *serial_out* is the CSR output and *serial_en* is the CSR enable. The CSR contains 12 bits of data bits for the Chip Control Unit (CCU) operation code.

Two internal registers are interfaced to the CSR: the Configuration Input Register (CIR) and the Configuration Output Register (COR). When the *serial_en* goes to 1, the COR is transferred to the CSR and the CSR content is serially downloaded

via the *serial_out* output. In parallel the data on the *serial_in* input is serially loaded into the CSR. When *serial_en* returns to 0, the CSR content is transferred to the CIR and read by the Configuration Control Unit (CCU). The CCU embeds the chip readout logic and chip configuration control logic. A schematic representation of the ToPix architecture is given in Figure 3.8.

Figure 3.7 shows the data output protocol. Each data frame starts with a frame header and ends with a frame trailer, the output word is of 40 bits. The 2 bits header indicates if the word is a frame trailer, a frame header or a hit event data. The frame header has 12 bits for the chip address, 8 bits for the Frame Counter (FC) which indicates the timestamp counter cycle and 6 bits for the Error Correction Code (ECC). Each event has 14 bits for the pixel address to identify the pixel among the 12769 pixels in the chip, 12 bits for the leading edge time and 12 bits for the trailing edge time. The frame trailer has 16 bits for the number of events, 16 bits for the CRC (Cyclic Redundancy Check) and 6 bits for the ECC.

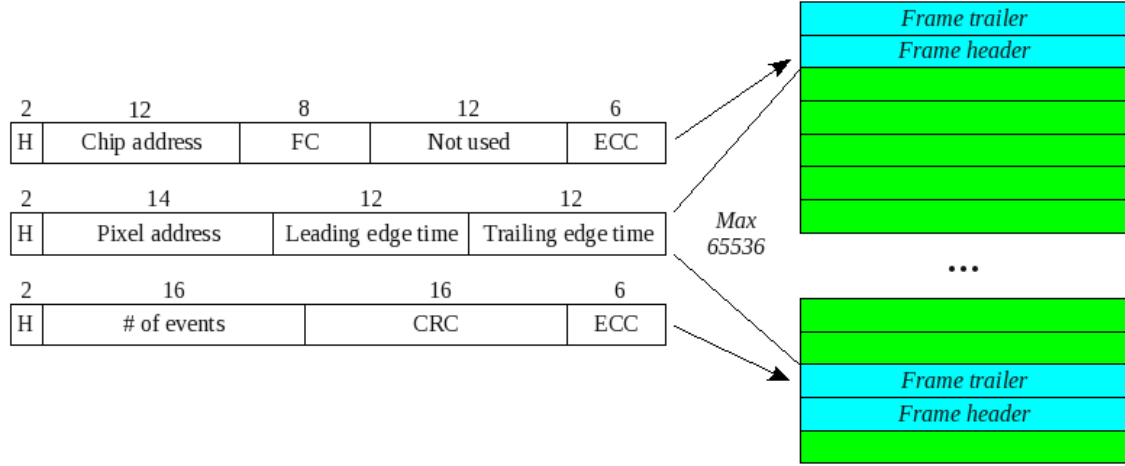


Figure 3.7: Output data format

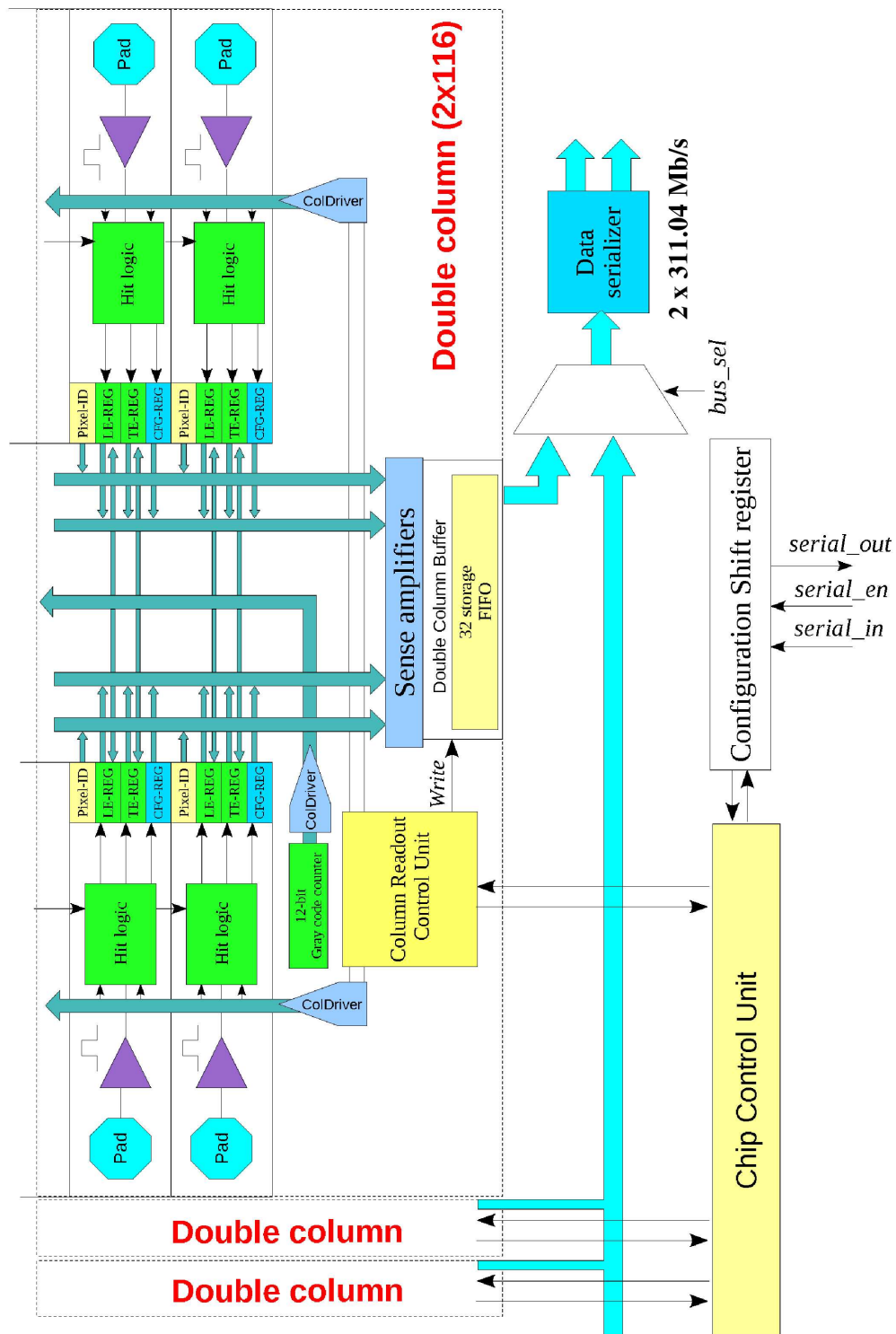


Figure 3.8: ToPix architecture

3.2.3 System level aspects

An accurate design of the data transmission systems is fundamental for the ASIC reliability. In single ended transmission systems the current return path through the ground is shared with multiple circuits, leading to mutual interference. To solve this problem differential transmission systems are employed. They have separate current return paths, in addition the electromagnetic coupling between the two wires reduces the emission of electromagnetic radiation and consequently the interference with the surrounding circuitry. Since both transmission lines are in the same environment they are affected by the same disturbances, which affects the common mode voltage but not the differential signal.

On-chip data transmission

The column input and output signals are transmitted with a frequency of 155.52 MHz along the column over a distance of $100\text{ }\mu\text{m} \times 116 = 11.6\text{ mm}$. The columns exhibits a line resistance of $681\text{ }\Omega$ and a parasitic capacitance of 3 pF , considering the input loads in each pixel.

The column input signals are sent by differential drivers with pre-emphasis (ColDriver) over the timestamp and control buses, and read by differential receivers placed in the pixel cell. Figure 3.9(a) shows the schematic of the data transmission system with the parasitic component of the transmission line. Figure 3.9(b) shows the simulation results of the ColDriver output and receiver input during the transmission of 3 bits. The ColDriver transmit a differential signal with a common mode voltage $V_0 = 0.6\text{ V}$, and a differential voltage of $\Delta V = 0.6\text{ V}$. The receiver input signal has the same common mode voltage, but the differential voltage is attenuated to $\Delta V = 0.2\text{ V}$. Anyway the differential receiver input voltage swing is 0.8 V , therefore the signal can be correctly reconstructed. The timestamp value is Gray-encoded in order to reduce the switching activity and to avoid synchronization problems in case of a load signal when the bus is changing its value.

The column output signals are generated in the pixel cell and are sent to the DCB over the data and address buses. The space and power limitations in the pixel cell does not allow the implementation of a driver bank in each pixel. Therefore the signals are read by a sense amplifier, placed in the peripheral area, which is able to discriminate small and fast voltage variations.

Off-chip data transmission

The ASIC digital input and output signals uses the Scalable Low-Voltage Signaling (SLVS) differential standard. The SLVS is a differential current-steering electrical protocol, with a common mode voltage of 200 mV and a voltage swing of 200 mV on a $100\text{ }\Omega$ load. Therefore it is compatible with the power supply of 1.2 V , the

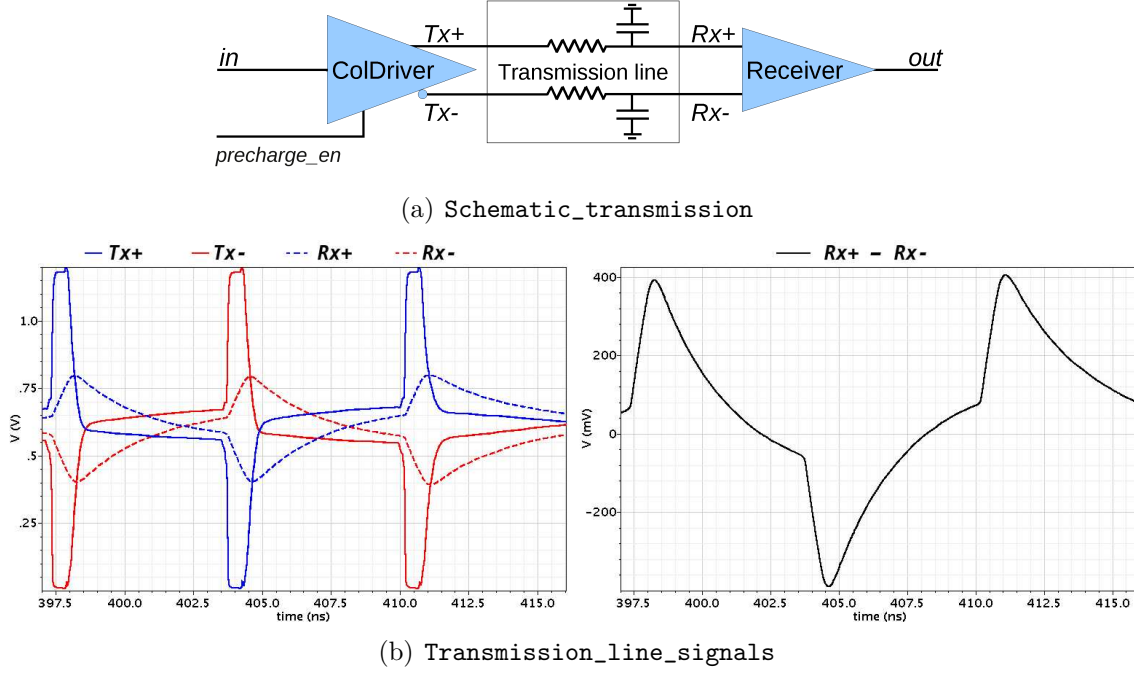


Figure 3.9: Transmission of the “101” bit sequence through the pixel column. Differential signals at the comparator output and receiver input(left). Input voltage swing at the receiver input (right).

output current is 2 mA and the power consumption at the load is 0.4 mW. The SLVS transmitter and receiver described in [74] are radiation hard and suitable for transmission up to 320 Mbit/s within a distance of a few meters.

3.3 Time over Threshold

The Charge Sensitive Amplifier (CSA) consists in an inverting voltage amplifier with feedback capacitance C_f for the charge integration. In the standard configuration a feedback resistance R_f is employed for the discharging of C_f . For a delta current pulse $I_{in}(t) = \delta(t)Q_{in}$ the response of the CSA with resistive feedback is:

$$v_{out}(t) = -\frac{Q_{in}}{C_f} \left(1 - e^{-\frac{t}{R_f \cdot C_f}} \right) \quad (3.12)$$

In circuits implemented in deep submicron technologies the power supply is limited to ~ 1.5 V in order to prevent the gate oxide breakdown. Typical values of feedback capacitance used in amplifiers for pixel detectors are in the order of ~ 10 fF. Supposing to have a rail to rail architecture to maximize the output swing in a

standard CSA configuration, a linear dynamic range ($Q_{in,range} = V_{out,swing} \cdot C_f$) in the order of 15 fC results. Therefore to increase the linear dynamic range a high value of feedback capacitor is needed. Moreover the strict area and power requirements does not allow to integrate in the pixel cell a fast ADC required for the output sampling.

The Time over Threshold technique (ToT) permits to measure the value of the injected charge, measuring the time taken for the discharging with a constant current (I_{dis}). The ToT stage is made of a CSA and a constant current feedback generator which is activated when the output is over a certain threshold. The integrator stage output is given by:

$$v_{out}(t) = -A_v \cdot v_{in}(t) = -\frac{A_v}{C_{in}} \int_0^t I_{in}(t') dt' \quad (3.13)$$

where $A_v > 0$ is the amplifier voltage gain, I_{in} is the current at the input node, and $C_{in} = C_d + C_M$ is the equivalent input capacitance given by the detector capacitance C_d and the additional capacitance due to the Miller effect C_M . The effective Miller capacitance is the feedback capacitance C_f multiplied by the factor $(1 + A_v)$. By explicating $C_{in} = C_d + C_f(1 + A_v)$ in equation (3.13) it becomes:

$$v_{out}(t) = \frac{-A_v}{C_d + C_f(1 + A_v)} \int_0^t I_{in}(t') dt' \quad (3.14)$$

The input current $I_{in}(t) = I_s(t) - I_{dis}(t)$ is given by the difference between the sensor signal current $I_s(t)$ and the discharging current $I_{dis}(t)$. Since the charge collection time is in the order of 10 ns, at least two order of magnitude lower than the typical discharging time, it is possible to assume the injected charge as a delta pulse $I_s(t) = \delta(t)Q_{in}$. The discharging current is a constant current injected at the input node while the signal is over a certain threshold. Theoretically in a noiseless case it is possible to set the threshold at $v_{out} = 0$, therefore it is generated in the time interval $0 < t < ToT$ where ToT is the discharging time. Substituting $I_{in}(t) = \delta(t)Q_{in} - I_{dis}$ in equation (3.14) yields:

$$v_{out}(t) = \frac{-A_v}{C_d + C_f(1 + A_v)} (Q_{in} - I_{dis} t) \quad (3.15)$$

At the time instant $t = ToT$ by definition the signal reaches the threshold $v_{out} = 0$, therefore:

$$v_{out}(ToT) = \frac{-A_v}{C_d + C_f(1 + A_v)} (Q_{in} - I_{dis} ToT) = 0 \quad (3.16)$$

When $v_{out} \approx 0$ applying the small signal approximation, with the ideal amplifier gains is $A_v = \infty$, gives:

$$\lim_{A_v \rightarrow \infty} \frac{-A_v}{C_d + C_f(1 + A_v)} = -\frac{1}{C_f} \quad (3.17)$$

substituting in (3.18) results:

$$v_{out}(ToT) = -\frac{1}{C_f}(Q_{in} - I_{dis} ToT) = 0 \quad (3.18)$$

and the linear relationship between the injected charge and the ToT is thus obtained:

$$ToT = \frac{Q_{in}}{I_{dis}} \quad (3.19)$$

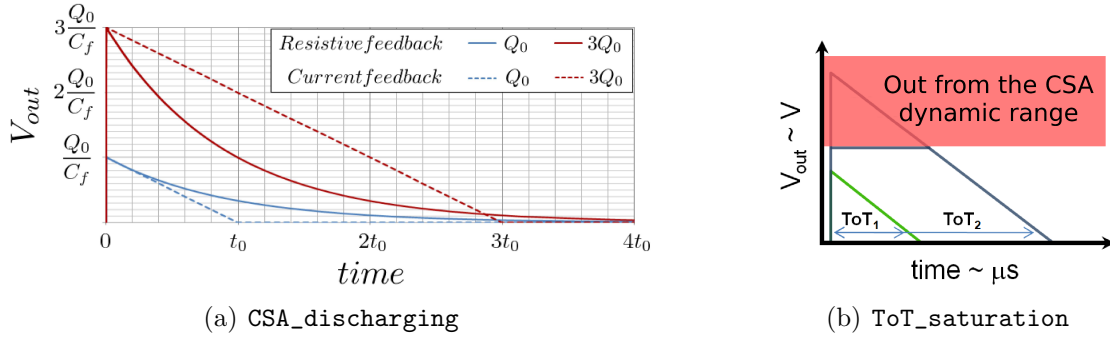


Figure 3.10: a) CSA discharged with resistance and constant current generator. b) Output ToT signals.

The ToT does not depend on the feedback capacitance C_f and neither on the detector capacitance C_d . The small signal approximation is required only for the output close to the threshold $v_{out} \approx 0$. Therefore, under the assumption of a constant discharging current I_{dis} , the ToT relationship is valid even when the preamplifier is saturated, thus allowing a high dynamic range of the charge measurement. Figure 3.10(a) shows the output of the CSA with a resistive feedback (standard CSA configuration) and with a constant current feedback (ToT stage), for $Q_{in} = Q_0$ and $Q_{in} = 3Q_0$. The absolute value of the output is taken in consideration for simplicity. In both cases the peak value is equal to Q_{in}/C_f . In case of constant current discharging also the signal width is linearly proportional to the charge (Q_{in}/I_{dis}). Figure 3.10(b) shows the output of the ToT stage for a signal that has a voltage swing under the saturation limit and a signal that saturates the CSA. Since the discharging current value is constant, in both cases the discharging is linear with the same slope and therefore a linear relationship between ToT and input charge is maintained. These considerations are valid under the assumption of ideal components, such as ideal voltage amplifier for the charge amplification and ideal constant current generator for the discharging of C_f . For example a real amplifier introduces a non zero rising time and a real current generator has a non infinite output resistance which could in some case lead to the generation of a non constant current. These and other issues will be addressed in chapter 5.

Pile up

The signal processing time is equal to ToT. If an additional input signal is present during the processing time a pile-up occurs. Therefore to study the ToT system efficiency it is important to estimate the pile-up probability. From the average event rate r , assuming that the time at which the different events occurs is statistically uncorrelated, the expected number of events n in the observation time Δt can be described with the Poisson distribution:

$$P(n) = \frac{(r \Delta t)^n e^{-r \Delta t}}{n!} \quad (3.20)$$

The assumption to have statistically uncorrelated events is a good approximation for a rough comparison of the average event rate and the readout processing time. For a precise study of the event arrival time an accurate simulation of the MVD event detection with a realistic beam is required. Setting $\Delta t = ToT$ and $n = 0$ it is possible to calculate the probability to have no signals during the processing time. Hence from equation (3.20) with a rate of 10^3 events per second, which is the maximum expected rate for a pixel, the probability to have pile up during the processing of a long ToT signal of $10 \mu s$ is:

$$1 - P(0) = 1 - e^{-r \Delta t} \approx 10^{-2} \quad (3.21)$$

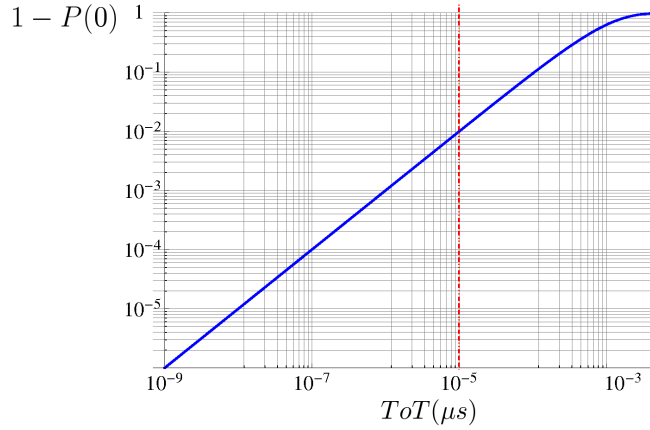


Figure 3.11: Pile up probability as a function of the ToT. The Red line indicates the maximum the ToT signal width for a input charge of 50 fC with the present architecture.

Therefore $\sim 1\%$ of signals with a ToT of $10 \mu s$ are affected by pile up. Figure 3.11 shows the pile up probability as a function of ToT. Considering that a long

ToT signal occurs for large ionizing particles which are a small fraction of the total particles, one can conclude that the pile up has a small impact on the readout reliability.

3.3.1 Saturation and cross talk

CSA operating ranges

For a CSA with feedback capacitance C_f and input capacitance C_d , applying the Miller theorem the equivalent input capacitance is $C_{in} = C_d + C_f(1 + A_v)$, where A_v is the voltage gain of the core amplifier in negative feedback configuration. The input voltage can be written as a function of the total stored charge $Q_{in}(t)$:

$$v_{in}(t) = \frac{Q_{in}(t)}{C_{in}} = \frac{Q_{in}(t)}{C_d + (1 + A_v)C_f} \quad (3.22)$$

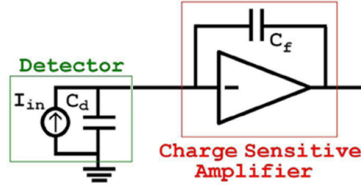


Figure 3.12: CSA

When the core amplifier is in the linear region, it can be considered as an ideal voltage amplifier with $A_v = \infty$, and the input node is a virtual ground:

$$\lim_{A_v \rightarrow \infty} v_{in}(t) = \lim_{A_v \rightarrow \infty} \frac{Q_{in}(t)}{C_d + (1 + A_v)C_f} = 0 \quad (3.23)$$

Now calculating the charge on the detector capacitance Q_d and the charge on the feedback capacitance Q_f when $A_v \rightarrow \infty$ it is possible to verify that in the linear region the charge is stored on the feedback capacitance:

$$\lim_{A_v \rightarrow \infty} Q_d(t) = \lim_{A_v \rightarrow \infty} C_d v_{in}(t) = \lim_{A_v \rightarrow \infty} C_d \frac{Q_{in}(t)}{C_d + (1 + A_v)C_f} = 0 \quad (3.24)$$

$$\lim_{A_v \rightarrow \infty} Q_f(t) = \lim_{A_v \rightarrow \infty} (1 + A_v)C_f v_{in}(t) = \lim_{A_v \rightarrow \infty} (1 + A_v)C_f \frac{Q_{in}(t)}{C_d + (1 + A_v)C_f} = Q_{in}(t) \quad (3.25)$$

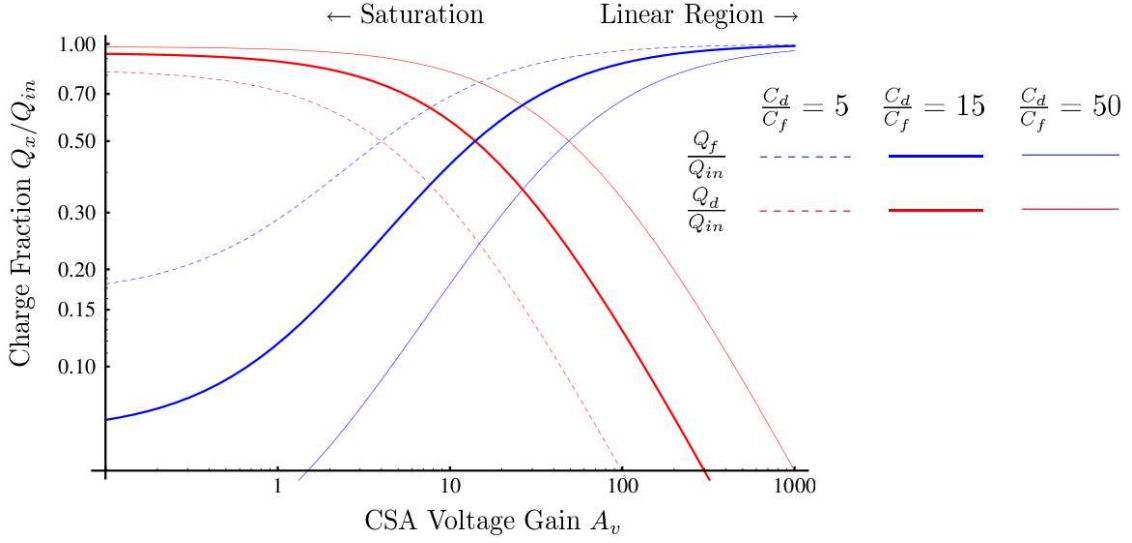


Figure 3.13: Charge Sharing

When the CSA goes out from the linear region and saturates A_v drops. Thus the input node can not be considered anymore as a virtual ground and the charge is shared between C_d and C_f . For $A_v = \frac{C_d}{C_f} - 1$ the charge is equally shared between the two capacitors.

Figure 3.13 shows the fraction of the total charge stored on each capacitor, Q_d/Q_{in} and Q_f/Q_{in} , as a function of the amplifier voltage gain A_v for three different $\frac{C_d}{C_f}$ ratios. The input node voltage can be calculated as:

$$v_{in}(t) = \frac{Q_d(t)}{C_d} \quad (3.26)$$

3.3.2 Cross talk

The pixel detector capacitance C_d has two contributions:

- the backside capacitance C_b towards the backplane, which depends on the pixel area and the thickness of the depletion zone.
- the interpixel capacitance C_c towards the adjacent pixels, which depends on the lateral dimensions and on the distance between the readout electrodes.

Figure 3.14 shows three pixel readout channels. The second channel receives from the sensor a charge signal i_{in2} on its input node. When the CSA is in linear region

Modality	Non Saturated	Saturated
Charge collection	on C_f	C_d and C_f
CSA voltage gain A_v	∞	drops
CSA charge gain	$1/C_f$	drops v_{sat}/Q_{inj}
$v_{out}(t)$	$-\frac{Q_{inj}-I_{dist}t}{C_f}$	v_{sat}
$v_{in}(t)$	0	$\frac{Q_{inj}-I_{dist}t}{C_d+(A_v+1)C_f}$

Table 3.5: CSA working modalities.

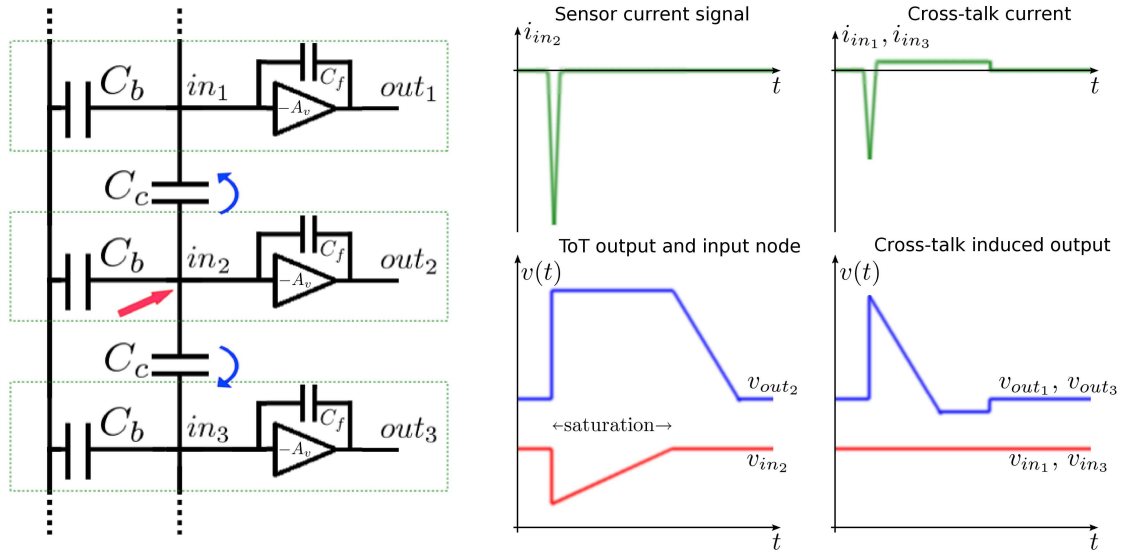


Figure 3.14: Cross Talk

the input is a virtual ground, and as calculated in the previous section it is collected on the feedback capacitance. When the CSA is saturated the variation of the input node voltage $v_{in2}(t)$ due to the charge collection on the detector capacitance injects a current signal through the coupling capacitances C_c to in_1 and in_3 . The injected current in the neighbor channels is:

$$i_{in1}(t) = i_{in3}(t) = \frac{dv_{in2}(t)}{dt} C_c$$

The voltage signal $v_{in2}(t)$ has a triangular shape. The steep leading edge injects a fast current of the same sensor signal polarity, while the slow trailing edge injects

a constant current of the opposite polarity, the total injected charge is 0. Due to crosstalk, the analog frontend which is in principle working for a predetermined sensor polarity has in practice to tolerate signals of both polarity.

3.3.3 Digitization resolution

The digitization resolution depends on the clock frequency f_c that supplies the timestamp. All the events (eg. leading edge crossing) that occurs within a clock cycle with period $T = \frac{1}{f_c}$ are digitized with the same timestamp value. The difference between the event time and the associated timestamp value is the quantization error ϵ . Since the event time and the clock signal are statistically uncorrelated the random events can be considered with a uniform distribution in function of the time. Therefore the digitization error probability density function is $p(0 < \epsilon < T) = T^{-1}$.

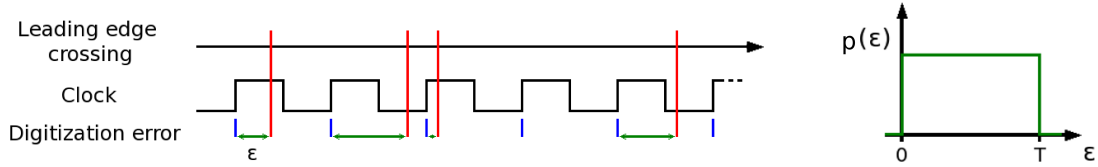


Figure 3.15: Digitization error ϵ and its probability density function $p(\epsilon)$.

The mean value of the event distribution in the given time interval is:

$$\mu_\epsilon = \int_0^T p(\epsilon) \epsilon d\epsilon = \frac{T}{2} \quad (3.27)$$

and therefore the resolution σ_t is:

$$\sigma_\epsilon = \sqrt{\int_0^T p(\epsilon) (\epsilon - \mu_\epsilon)^2 d\epsilon} = \frac{T}{\sqrt{12}} = (\sqrt{12}f_c)^{-1} \quad (3.28)$$

If discharging current value is much more accurate than the ToT measurement:

$$\left(\frac{\sigma_{I_{dis}}}{I_{dis}}\right)^2 \ll \left(\frac{\sigma_{ToT}}{ToT}\right)^2 \quad (3.29)$$

the resolution on the charge digitization depends on the ToT resolution:

$$\sigma_Q = \sqrt{\left(\frac{\sigma_{ToT}}{ToT}\right)^2 + \left(\frac{\sigma_{I_{dis}}}{I_{dis}}\right)^2} Q = \frac{\sigma_{ToT}}{ToT} Q = \sigma_{ToT} I_{dis} \quad (3.30)$$

The ToT is calculated by subtracting the timestamp value for the leading edge t_{LE} and trailing edge t_{TE} . Therefore the ToT digitization error is $\epsilon_{ToT} = \epsilon_2 - \epsilon_1$, where ϵ_1 is the t_{LE} digitization error and ϵ_2 is the t_{TE} digitization error. Figure 3.16 shows the ToT digitization error as a function of ϵ_1 and ϵ_2 , and the probability density function of the quantization error on ToT considering the t_{LE} and t_{TE} statistically uncorrelated:

$$p(-T < \epsilon_{ToT} < T) = \frac{T - |\epsilon_{ToT}|}{T^2} \quad (3.31)$$

The ToT resolution is:

$$\sigma_{ToT} = \sqrt{\int_0^T p(\epsilon_{ToT}) (\epsilon_{ToT} - \mu_{\epsilon_{ToT}})^2 d\epsilon_{ToT}} = \frac{T}{\sqrt{6}} = (\sqrt{6}f_c)^{-1} \quad (3.32)$$

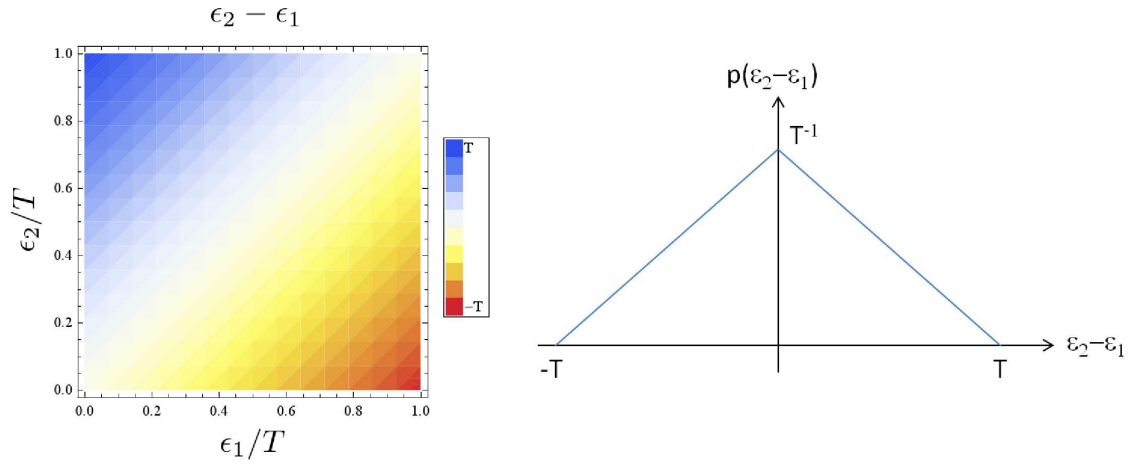


Figure 3.16: ToT digitization error $\epsilon_2 - \epsilon_1$ and probability density function.

The resolution on the charge digitization is:

$$\sigma_Q = I_{dis} \sigma_{ToT} = \frac{I_{dis}}{\sqrt{6}f_c} \quad (3.33)$$

Working with a clock frequency $f_c = 155.52$ MHz from Equation (3.28) the time digitization resolution is:

$$\sigma_t = (\sqrt{12}f_c)^{-1} = 1.856 \text{ ns} \quad (3.34)$$

Choosing a typical discharging current $I_{dis} = 5$ nA, from Equation (3.33) the charge digitization resolution is:

$$\sigma_Q = \frac{I_{dis}}{\sqrt{6}f_c} = 13.17 \text{ aC} = 83 \text{ e}^- \quad (3.35)$$

3.3.4 Noise

The noise performance of a CSA is expressed as the Equivalent Noise Charge (ENC), defined by the ratio of the output voltage root mean square (rms) noise to the signal amplitude for a charge of 1 electron. The ENC can be calculated as the product of the output rms noise V_{noise} and the feedback capacitance C_f :

$$ENC = \frac{V_{noise}}{\frac{v_{out}}{Q_{in}}} = V_{noise} \cdot C_f \quad (3.36)$$

The comparator noise rate is given by the combined probability function for Gaussian amplitude and time distribution [75].

$$f_n = f_{n_0} \cdot e^{-\frac{V_{th}^2}{2V_{noise}^2}} \quad (3.37)$$

where f_{n_0} is the noise rate at zero threshold which depends on the CSA transfer function, V_{th} is the threshold voltage, and V_{noise} is the CSA output voltage noise. The minimum detectable charge is fixed by the threshold voltage:

$$Q_{min} = C_f \cdot V_{th} \quad (3.38)$$

Therefore the signal to noise ratio for the minimum detectable charge Q_{min}/ENC is the parameter that has to be maximized in order to reduce the noise occupancy. For example in case of $Q_{min}/ENC = 6$, the noise rate is reduced by a factor:

$$f_n/f_{n_0} = e^{-\frac{36}{2} \frac{ENC^2}{ENC^2}} = 1.5 \cdot 10^{-8}$$

The ToT technique allows to perform the charge measurement through two timing measurement. For each timing measurement the voltage noise is translated in jitter (Fig. 3.17), which is proportional to the noise to slope ratio:

$$\sigma_t = \frac{\sigma_{v_{out}}}{\left. \frac{dv_{out}}{dt} \right|_{V_{th}}} \quad (3.39)$$

assuming that the two timing measurements are uncorrelated the noise in the ToT measurement is:

$$\sigma_{ToT} = \sqrt{\sigma_{t_{LE}}^2 + \sigma_{t_{TE}}^2} = \sigma_{v_{out}} \sqrt{\left(\left. \frac{dv_{out}}{dt} \right|_{V_{th,LE}} \right)^{-2} + \left(\left. \frac{dv_{out}}{dt} \right|_{V_{th,TE}} \right)^{-2}} \quad (3.40)$$

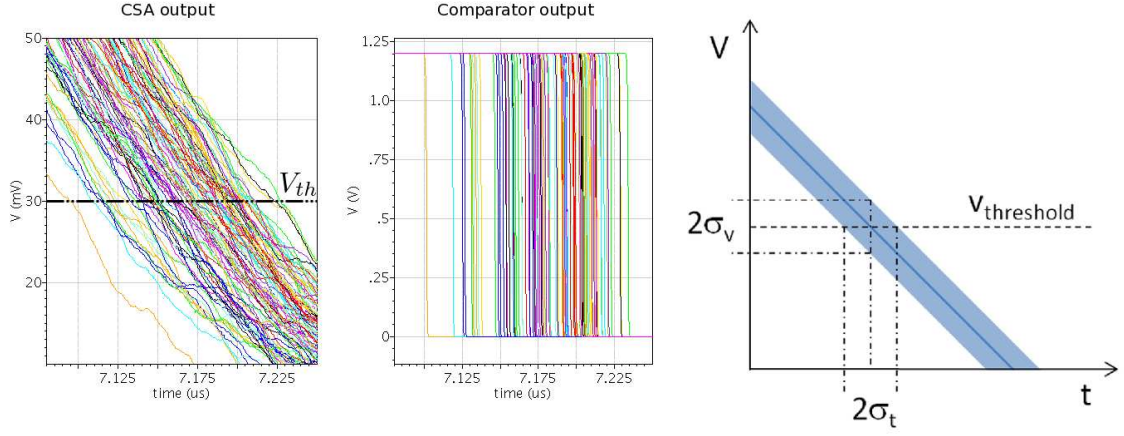


Figure 3.17: Jitter on falling edge threshold crossing.

ToT signal shape

Since the noise that affects the ToT measurement is inversely proportional to the signal slope, considerations on the output signal shape are required for the ToT system noise analysis.

The CSA has a fixed peaking time t_p , therefore the intersection between the output signal and the threshold depends on the signal amplitude (Fig. 3.18). The

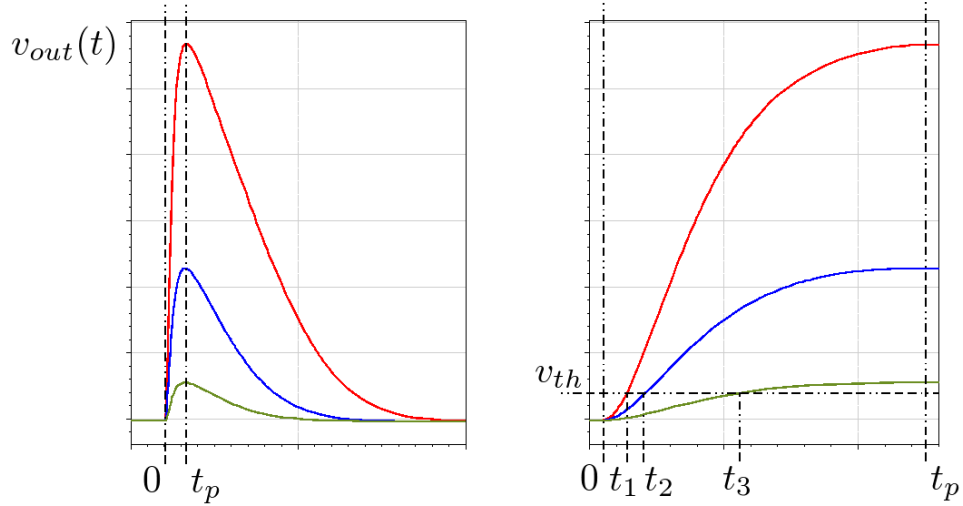


Figure 3.18: Time walk

time walk is the difference between the crossing points and it is a systematic effect which depends on the signal amplitude, hence on the ToT value. The time walk can be corrected by a calibration curve, thus the uncertainty on the rising edge timing is due to the noise. The shape of the rising edge is determined by multiple time constants, however it can be approximated with a linear fit in the threshold crossing region:

$$\left. \frac{dv_{out}}{dt} \right|_{V_{th,LE}} = \frac{V_{th}}{\Delta t_{crossing}} \quad (3.41)$$

where $\Delta t_{crossing}$ is the time difference between the charge signal arrival time and threshold crossing time. The trailing edge slope can be calculated under the assumption of a linear response:

$$\left. \frac{dv_{out}}{dt} \right|_{V_{th,TE}} = \frac{I_{dis}}{C_f} \quad (3.42)$$

where I_{dis} is the constant discharging current.

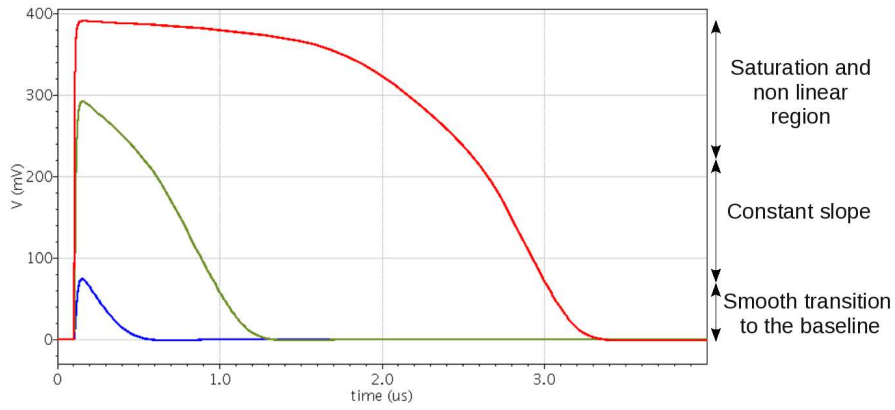


Figure 3.19: ToT shape

Figure 3.19 shows the shape for three different ToT signals. On the basis of the output voltage it is possible to recognize the saturation and non linear region where the CSA gain drops, the constant slope region where the CSA works in linear region and the smooth transition to the baseline. This transition behavior is due to the fact that the feedback circuit that provides the discharging current is not an ideal switch. It is implemented through a differential pair that requires a certain voltage (~ 40 mV) to be completely activated. For small signals the differential pair acts as a resistive feedback. In this case the signal shape is given by a transfer function which takes into account the RC filtering due to the feedback capacitance and the equivalent feedback resistance.

On the one hand the approximation done in equation (3.42) is not valid in the transition region between the baseline and the linear region, on the other if the comparator threshold is set in the constant slope region the smallest signal can not be detected. For a precise study of the leading and trailing edge slope a set of simulations have been performed with the present architecture. Table 3.6 shows the simulation results, for two different charge values Q_{in} with two different comparator threshold values V_{th} . It is possible to see that the ToT noise is dominated by the trailing edge jitter $\sigma_{TE}/\sigma_{ToT} \approx 1$. Both threshold values are in the smooth transition region. For comparison the trailing edge slope in the constant slope region is $\left. \frac{dv_{out}}{dt} \right|_{V_{th,TE}} = 0.38 \text{ V}/\mu\text{s}$. The jitter with the threshold in the constant slope region is $\sigma_{ToT_{min}}$, therefore the ratio $\frac{\sigma_{ToT}}{\sigma_{ToT_{min}}}$ is the noise multiplying factor due to the fact that the threshold is in the smooth transition region.

Q_{in}	V_{th} [mV]	$\left. \frac{dv_{out}}{dt} \right _{V_{th,LE}}$ [V/ μ s]	$\left. \frac{dv_{out}}{dt} \right _{V_{th,TE}}$ [V/ μ s]	$\frac{\sigma_{TE}}{\sigma_{ToT}}$	$\frac{\sigma_{ToT}}{\sigma_{ToT_{min}}}$
0.5 fC	15	1.45	0.13	0.9958	2.9
2.0 fC	15	5.71	0.17	0.9995	2.2
0.5 fC	30	0.83	0.17	0.9800	2.2
2.0 fC	30	6.87	0.28	0.9991	1.4

Table 3.6: Leading edge and trailing edge slope and contribution to noise

A method to reduce the ToT jitter is the employment of a double threshold system, one for the leading edge and one for the trailing edge. The first threshold can be set with the same value of the actual comparator threshold in order to detect small charges, the second can be set in the constant slope region reducing the noise thanks to the large slope value. This architecture does not implement a double threshold system which would require a larger silicon area. For ToPix purposes the critical parameter is Q_{min}/ENC , and an effort has been made in order to reduce the ENC, thus decreasing also the absolute value of the jitter. In the actual system the relative jitter increment is of a factor 2-3 for small charge values close to the minimum detectable charge, and of a factor below 1.4 for large charges. Since such small charge values are due to MIPs, the charge information is not used for PID purposes, therefore a jitter reduction is not strictly required.

Jitter and measuring time relationship

The noise performance [76] of the ToT stage can be studied with the equivalent circuit where the ToT stage is assumed noiseless and the system noise is modeled with an equivalent input noise voltage and current generators. The equivalent voltage source generates a random sequence of δ pulses (series noise). In this calculation

only the white series noise is take into account, since at high frequencies the $1/f$ component is negligible. The equivalent current source generates a random sequence of current δ pulses (parallel noise) which results in a voltage step due to the integration on the sensor capacitance.

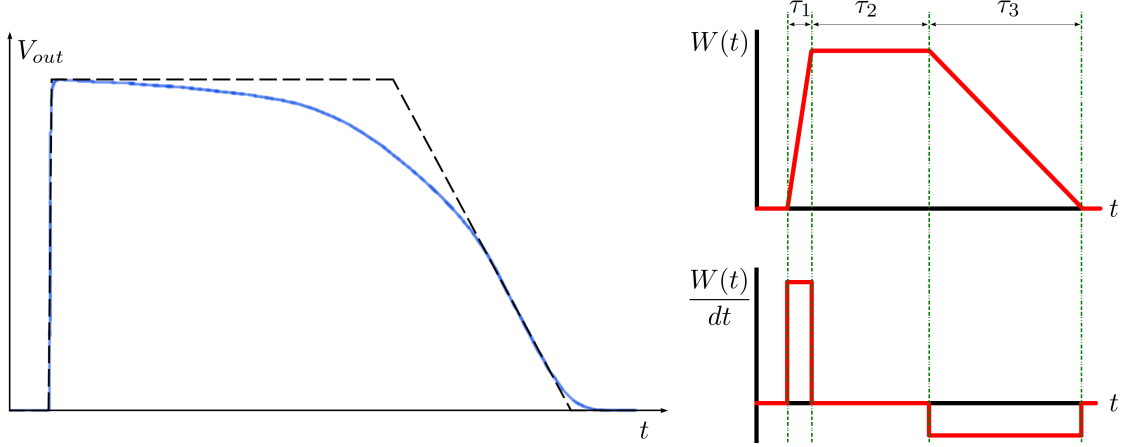


Figure 3.20: Trapezoidal weighting function.

Measurements have shown that the jitter increases with the ToT length. A set of simulations has been performed in order to study this effect related to the measuring time window. Equation 3.40 takes into account in the jitter calculation only the projection of the voltage output noise in the leading edge and trailing edge crossing point. This equation is valid in a small signal approximation and it does not take into account the effects introduced by the fact that the ToT signal saturates.

A time domain approach has been chosen for the noise calculation [77], using a trapezoidal weighting function $W(t)$ for the approximation of the saturated ToT signal as shown in Figure 3.20. Therefore it is possible to calculate the ENC component due to the white parallel noise and white series noise [78] [72]:

$$ENC_{pw}^2 = \frac{1}{2} i_n^2 \int_{-\infty}^{\infty} [W(t)]^2 dt = a_p \left(\tau_2 + \frac{\tau_1 + \tau_3}{3} \right) \quad (3.43)$$

$$ENC_{sw}^2 = \frac{1}{2} C e_n^2 \int_{-\infty}^{\infty} \left[\frac{W(t)}{dt} \right]^2 dt = a_s \left(\frac{1}{\tau_1} + \frac{1}{\tau_3} \right) \quad (3.44)$$

where i_n and e_n are the noise spectral densities of the parallel and series sources, C is the input capacitance, $W(t)$ is the weighting function, a_p and a_s are two proportionality coefficients, τ_1 is the rising time, τ_2 is the flat top time due to the

saturation and τ_3 is the falling time. Since the parallel and series noise are statistically uncorrelated, the ENC is the sum in quadrature of ENC_{pw} and ENC_{sw} :

$$ENC = \sqrt{ENC_{pw}^2 + ENC_{sw}^2} = \sqrt{a_p \left(\tau_2 + \frac{\tau_1 + \tau_3}{3} \right) + a_s \left(\frac{1}{\tau_1} + \frac{1}{\tau_3} \right)} \quad (3.45)$$

An intuitive approach can explain the time dependence of the results. The ENC_{pw} depends on the random current δ pulses which can inject a positive or negative unit charge q_u . These pulses are integrated over the measuring time, supposing to have N random events, the additional charge rms value injected by the current noise source is $q_u \sqrt{N}$. This non zero charge rms value increases the time jitter. Since the number of events N is proportional to the measuring time the charge rms value will be $ENC_{pw} \propto \sqrt{time}$. The ENC_{sw} depends on the random voltage δ pulses which can be considered as a difference between a two voltage step pulses, with the second step delayed of an infinitesimal interval dt . For this reason the ENC_{sw} depends on the derivative of the weighting function $W(t)$, thus on its slope which is proportional to the inverse of the rising and falling time. When the preamplifier has a zero output slope (i.e. saturated) the contribution of the series noise does not introduce any time shift.

A set of simulations has been performed with a leakage current $I_{leak} = 50nA$. A such large value has been chosen in order to increase the parallel noise contribution of the leakage compensation circuit. Since the threshold is fixed in the smooth transition region, the slope value of the ToT output signal has been normalized to I_{dis}/C_f , in order to neglect the jitter variation due to the shape distortion. The trapezoidal filter shape depends on the ToT. From the simulation data the rising time is constant $\tau_1 = 10$ ns and also the falling time for a saturating signal is constant $\tau_2 = 1050$ ns. Hence the flat top time is $\tau_2 = ToT - \tau_1 - \tau_3$. It is possible to extend the case also for non saturating signal where $\tau_2 = 0$ and $\tau_3 = ToT - \tau_1$. Consequently in equation (3.45) the ENC can be expressed as a function of the ToT . Figure 3.21 shows the fit results with $a_s = (4.1 \pm 1.1) \cdot 10^6 [C^2 \cdot s]$ and $a_p = (6.4 \pm 0.6) \cdot 10^2 [C^2/s]$. The first point for $ToT = 200$ ns was not taken into account in the interpolation because it is not possible to be approximated with a triangular signal but rather by the inverse Laplace Transform of the ToT stage transfer function for small signals. Therefore in this case the noise can be calculated in the frequency domain taking in to account the AC transfer function. The value $ENC_{AC} = 379.7$ calculated with the AC simulation is within 1σ dispersion of the $ENC_{tn} = 378.8 \pm 3.7$ calculated from the jitter of the transient noise simulation. The increment of the noise of large signal with the \sqrt{ToT} is not an issue since the signal to noise ratio $\propto ToT/\sqrt{ToT}$ increases with \sqrt{ToT} .

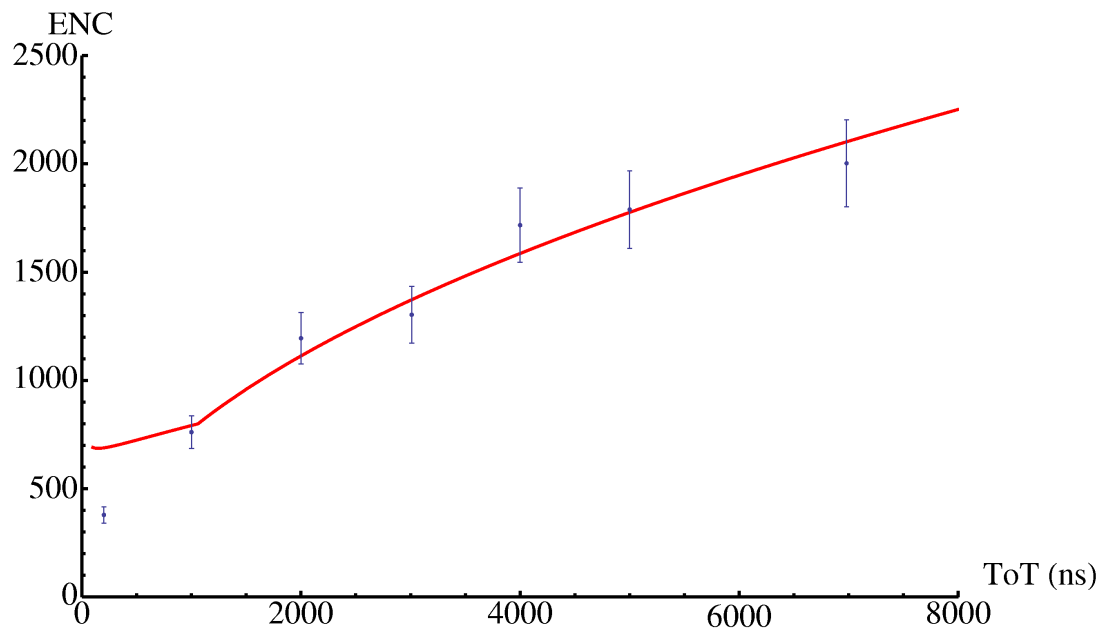


Figure 3.21: Interpolation of the ENC obtained from simulation as a function of ToT.

Chapter 4

Test results from first prototypes

Large scale mixed signals ASICs are complex systems and a prototyping phase is required for test and optimization purposes. In high energy physic experiments where a relatively small number of chips is produced the cost of the system can be dominated by Non Recurrent Engineering (NRE) costs. In particular the cost of the masks necessary for the ASIC fabrication is increasing significantly when going to more scaled feature size. The cost of a set of masks for a CMOS 0.13 μm process easily exceeds 300.000 euro. Furthermore, in an integrated circuit even small mistakes may force to a re-fabrication of the ASIC, which implies the production of a new set of masks. To minimize this risk, in this project a three step approach suitable for multichannel ASICs has been chosen. The first step has been the design of two prototypes intended to explore mostly the pixel architecture. The experimental characterization of these circuits has provided very usefull guidelines for the design of the final pixel cell, that will be discussed in chapter 5. The second step, which is the present phase of the project consists in the design of a multichannel ASIC, incorporating all the functional building blocks including the full digital part of the chip. This prototype will allow also the bump bonding to a sensor to test the architecture and most of the system level aspects. In these two preliminary steps only relatively small chips are needed. These prototypes are fabricated in Multi Project Wafer (MPC) runs, where masks and wafers cost are shared between different users. Finally the full scale ASIC will be fabricated with a dedicated engineering run.

ToPix_1, fabricated in 2006, is the first prototype aimed to identify the critical points in the analog readout. The second prototype, ToPix_2 fabricated in 2008, implements a complete readout cell with analog and digital circuitry. The cells are arranged in columns with a simplified version of the peripheral logic. These two prototypes are designed to work with a clock frequency of 50 MHz which was the first value selected for the master clock frequency of the $\overline{\text{P}}$ ANDA experiment. Given the reduced ASIC size bump bonding to a sensor was not feasible. In this chapter the results of the two prototypes design in the first step are presented and discussed.

4.1 ToPix_1

The first prototype [79] chip contains 32 readout cells, each one is equipped with a preamplifier and a discriminator. The preamplifier consist of a CSA with a feedback capacitance of 10 fF, a constant current feedback and a baseline restorer. The amplifier size is $37\ \mu\text{m} \times 51\ \mu\text{m}$ and the discriminator size is $12.8\ \mu\text{m} \times 48\ \mu\text{m}$. Figure 4.2 shows the ToPix_1 architecture. The ASIC size is $2\ \text{mm} \times 1\ \text{mm}$. The cells are arranged in 8 groups of 4 cells. Each group has 4 calibration input lines, 4 analog output lines and 4 digital output lines. Each input calibration line is in common for one of the cell in each of the 8 groups. In each cell, a calibration capacitor of 30 fC shunts the calibration line to the input node. Therefore, sending a voltage step on the calibration line a delta shaped current pulse is injected at the input node. The output lines are multiplexed in order to be shared between the cells belonging to different groups. In order to drive the capacitive load of output pads and measurement probes, which can be up to 10 pF, the analog signals are driven by a source follower and the digital signals are driven by a buffer. Six cells belonging to two different groups have direct connection to a dedicated input pad. This configuration allows for the observation of the cross-channel effects.

4.1.1 Front-end simplified scheme

Figure 4.1 shows a simplified schematic view of ToPix_1 readout, which is designed to work with a n-type sensor (negative current pulses). The CSA core amplifier has three feedback components:

- The feedback capacitance C_f fixes the charge gain ($1/C_f$). On the one hand a high value of C_f decreases the CSA charge gain, on the other hand a low value of C_f decreases the CSA loop stability. In this prototype a nominal value of the feedback capacitance of 10 fF has been chosen as the optimal compromise between gain and loop stability.
- The baseline restorer is implemented with a g_m/C low pass filter stage which compute the difference between the baseline reference voltage and the CSA output. The resulting low frequency voltage signal controls the gate of a PMOS (M4) which generates the leakage compensation current at the input node.
- The discharging current generator is based on a differential pair. The CSA output is presented at M2 input, the baseline reference voltage is presented at the M1 input. When $V_{out} = V_{ref}$ the current generated by M3 is equally shared in the two branches. When a negative current signal is present at the CSA input, V_{out} increases thus switching off M2. Consequently M3 current flows in

the input node through M1 and C_f is discharged. A good constant discharge is achieved only when v_{out} is sufficiently large to fully steer the current from one branch to the other of the differential pair. Since M1 and M2 work in weak inversion this voltage is about 40 mV.

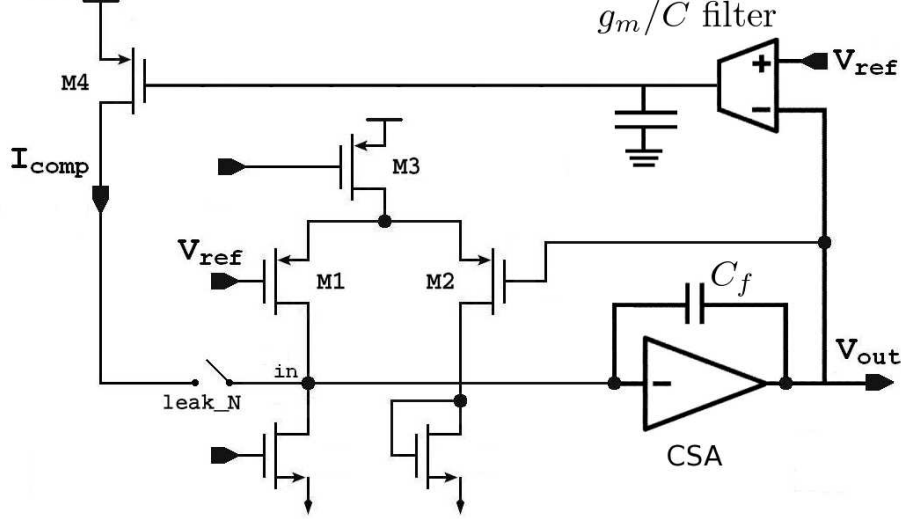


Figure 4.1: Simplified scheme of ToPix_1 front-end.

4.1.2 Test results

Figure 4.3 shows the preamplifier output. The electrical parameter test results are summarized in Table 4.1. A large channel-to-channel variation of the ToT and of the baseline value has been measured. A such large baseline variation is due to the leakage compensation stage where a $10\ \mu\text{m} \times 10\ \mu\text{m}$ zero-vt transistor has been employed as capacitance. This component has a non negligible gate leakage current which was overlooked in the design phase. This extra current alters the correct operation of the filter. The measured noise is referred in the case without input capacitance load ($C_d = 0$) and zero leakage current.

Radiation damages tests

ToPix_1 was tested both for ionizing damage and displacement damage:

- Ionizing damage occurs when high energy photons or charged particles produces electron - hole pairs in insulation layers. The electrons have a sufficient

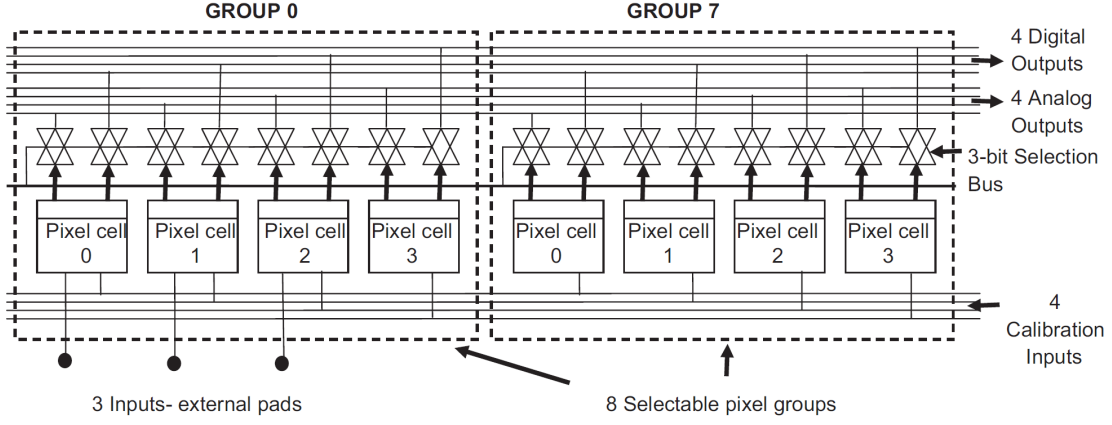


Figure 4.2: ToPix_1 architecture [79].

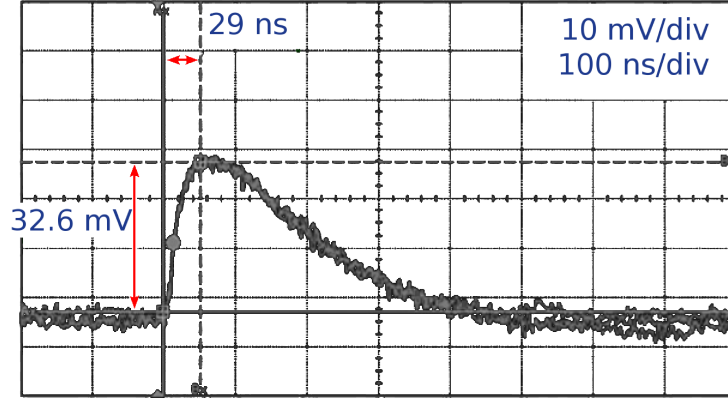


Figure 4.3: ToPix_1 - Cell output for an input charge of 0.5 fC [79].

Analog gain	60 mV/fC
Linear input range	100 fC
$V_{noise,rms} (C_d = 0)$	1 mV
ENC ($C_d = 0$)	104 electrons
Power consumption	12 μ W/cell
ToT dispersion (rms)	20%
Baseline dispersion (rms)	13 mV

Table 4.1: ToPix_1 electrical functionality test results [79].

mobility to move toward the positive electrode while the holes due to their low mobility have a high probability to be trapped in the oxide volume or in the oxide interface. If this phenomena occurs in the MOS gate, the additional fixed charge due to the hole trapping changes the electrical field thus shifting the transistor threshold voltage. In the CMOS 130 nm technology chosen for our ASIC design the gate oxide layer is 2 nm. In a such thin layer the trapping probability is reduced thus decreasing the threshold voltage shift. In [80] a voltage shift of few mV has been measured for a TID of 10 Mrad in a CMOS 130 nm process. These values are ~ 5 times lower than the values measured in a 180 nm process. The holes trapping in the Shallow Trench Isolation (STI) modifies the electric field at the edge of the transistor, thus opening a lateral parasitic conductive channel between source and drain in NMOS transistors. In deep submicron technologies the STI oxide does not scale down as the gate oxide and the hole trapping in the STI oxide is not negligible. The parasitic channel leakage current becomes the dominant current when the transistor is switched off [81]. The lateral parasitic channel can be modeled as a lateral transistor and it has been shown that it increases the $1/f$ noise for shorter channel transistor at low current density [82]. TID effects on CMOS 130 nm technologies performance are discussed in [80]. The ionization effects depends on the cumulative ionizing radiation, and it is measured by the Total Ionizing Dose (TID) which depends on the absorbed energy through ionization per unit mass of material (in this case SiO_2). However also the dose rate is important, as at low dose rates the combined annealing effect becomes important.

- Displacement damages occurs when an incident particle displaces the silicon atom from the lattice site thus altering the electrical characteristic of the crystal. It is a cumulative long term damage, which depends on the energy (> 25 eV) and momentum transferred to the lattice atoms, therefore it has to be referred to the incident type of particle. Usually the information is normalized to the damage of 1 MeV neutron fluence over 1 cm^2 . The displacement damage introduces defects in the crystal which can create new energy states. If the state is close to the energy band edges it increases the charge trapping probability. The creation of mid-gap states facilitates the electron transition between the valence band and the conduction band: in depletion regions the probability of an electron to be promoted to the conduction band increases thus increasing the current flow, while in non depleted regions the recombination is facilitated hence reducing the current flow. Displacement damage can also change the donor and acceptor density profile in silicon.

Enclosed layout transistor prevents the radiation induced leakage current in NMOS transistors [63]. The source diffusion is enclosed by the gate, thus avoiding the formation of any parasitic channel between the source and the drain (Fig. 4.4).

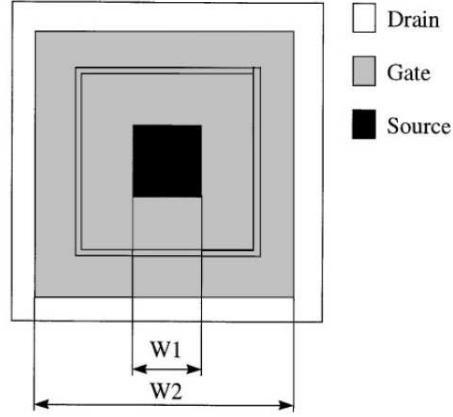


Figure 4.4: Square shaped enclosed layout transistor geometry [63]. It is equivalent for a linear transistor with $\frac{W}{L} = 8/\ln\left(\frac{W_2}{W_1}\right)$.

Since enclosed layout introduces area penalty and limitations in the transistor form factor, in ToPix_1 only linear transistors are employed in order to test the TID tolerance capability. Two TID measurements at different dose rate have been performed with X-rays. The high dose rate measurements were performed using the X-ray source of the Microelectronics Laboratory at CERN in order to obtain a final dose of the same order of magnitude expected in the $\overline{\text{PANDA}}$ lifetime in less than 1 day.

One chip was irradiated with a dose rate of 400 rad/s with three measurement points for a TID of 3.5 Mrad, 5.6 Mrad and 19.5 Mrad. Then measurements were performed during the annealing phase: 4 days $25^\circ\text{C} \pm 2.5^\circ\text{C}$ and 7 days at $100^\circ\text{C} \pm 2.5^\circ\text{C}$. Other three chip were irradiated with a dose rate of 100 rad/s and measurement were performed for a TID in the 0.179 Mrad - 6.2 Mrad range followed by measurement during annealing. The low dose rate measurements were performed using the X-ray source of the University of Piemonte Orientale and Alessandria. The dose rate of 1.1 rad/s, even if it is 1 order of magnitude larger than $\overline{\text{PANDA}}$, allows to observe the combined effect of annealing during the irradiation. A TID of 3 Mrad was obtained in 3 weeks without any annealing measurement after irradiation. The TID measurement results are summarized in Table 4.2. For the high dose rate measurements only the measurement of the chip with the higher variation are reported. The ToT gain depends on the discharging current of 5 nA, which is sensible to the radiation induced leakage currents. Hence the measured gain variation is satisfactory. The comparator threshold variation can be compensated using static DACs, that were not present on this prototype. The radiation tolerance of

the prototype circuit was found to be satisfactory, despite the exclusive use of linear transistor geometry.

X-ray facility	CERN	Unipmn - AL
TID	19.5 Mrad	3 Mrad
Rate	400 rad/s	1.1 rad/s
Irradiation time	<1 day	5 weeks
Annealing	>7 days	0
Radiation induced leakage	<15%	< 8%
Analog gain variation	<3%	<1.5%
ToT gain variation	<18%	<14%
Baseline and comparator threshold dispersion	<11%	<6.7%
Noise	<18%	<14%

Table 4.2: TID test results. The percentage are referred to the difference between the measurement before irradiation and the maximum value measured during or after irradiation [79].

Displacement damage test with neutrons were performed at Laboratori Nazionali di Legnaro (LNL), Padova. Two chips were irradiated with a neutron flux of $1.7 n_{[1 \text{ MeV}_{\text{eq}}]}/\text{cm}^2$ and $3.6 n_{[1 \text{ MeV}_{\text{eq}}]}/\text{cm}^2$ respectively. In this way it is reproduced a displacement damage of the same order of magnitude expected in the $\overline{\text{PANDA}}$ lifetime. Functionality test were performed before and after the exposition of the chips to the neutron flux, and two cells per chip were characterized. The sensible parameters like leakage current, baseline voltage, comparator threshold, ToT gain and analog gain were measured and their variation has no significant change ($< 1\%$). The noise variation was within $< 2\%$.

The results from the first prototype shows that the radiation hardness is sufficient for the $\overline{\text{PANDA}}$ environment even without hardness-by-design transistors. For a final choice it is important to take into consideration also the studies from the second prototype since it includes more digital circuitry, and therefore the possibility of evaluating Single Event Effects (SEE).

4.2 ToPix_2

In ToPix_2 [83] each cell in an area of $100 \mu\text{m} \times 100 \mu\text{m}$ embeds the analog readout chain for the charge digitization, the pixel control logic and the data registers (section 3.2.1). In this version a 5 bit DAC allows a fine tuning of the comparator threshold on a pixel by pixel basis. For test purposes each pixel can be individually connected to the calibration signal which makes the injection of a current pulse possible. The front-end design has been updated to work with sensors of either polarity.

ToPix_1 was designed with a CSA feedback capacitance of 10 fF. Since the baseline restorer performance was not satisfactory in ToPix_2 a more conservative design has been chosen with a feedback capacitance of 24 fF thus reducing the analog gain to 41.7 mV/fC. This allows to improve the CSA feedback stability and improve the baseline restorer filter. ToPix_2 allows to compensate leakage of p-type and n-type sensors.

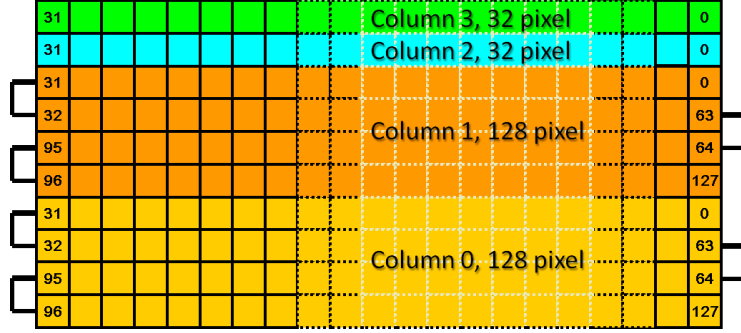


Figure 4.5: Pixel cells arrangement in ToPix_2.

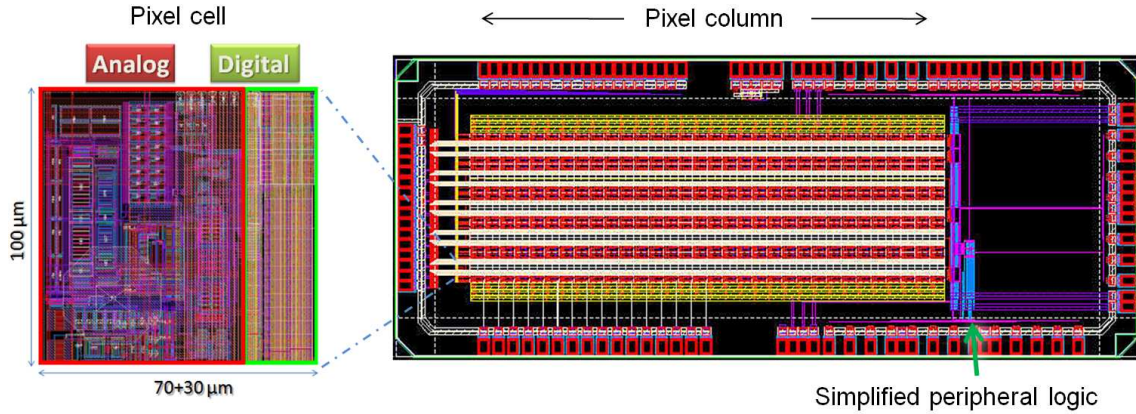


Figure 4.6: ToPix_2 layout with the detail of the readout cell.

ToPix_2 has 320 pixel readout cells arranged in four columns, two short columns with 32 pixels and two folded column with 128 pixels. It is present a simplified version of the peripheral logic described in section 3.2.2. In the final version of ToPix the length of each column will be 11.6 mm. In this prototype folded columns are employed (Fig. 4.5) to estimate the effect of the column length on the data transmission. In this way it is possible to implement a long column in a limited

polarity signal as in the case of a n-type sensor in the RC filter. The compensation current is injected at the input node through a current mirror (*leak_P* activated).

4.2.2 Test system setup

ToPix_2 was directly bonded on a custom made Printed Circuit Board (PCB) as shown in Figure 4.8. It has been tested with two different test setups. The first was developed at INFN Torino and the latter developed at Jülich.

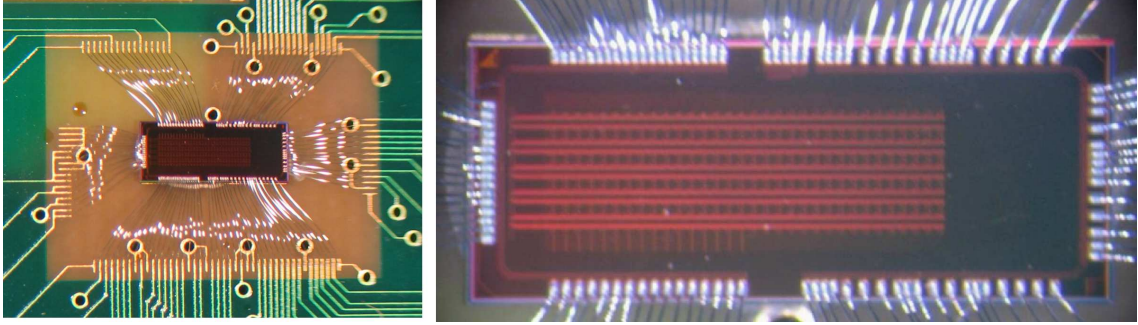


Figure 4.8: Photo of ToPix_2 ($5mm \times 2mm$) wirebonded on PCB.

INFN Torino setup

In the INFN Torino setup the ToPix_2 testboard is connected to a Virtex II Field Programmable Gate Array (FPGA) which implements the configuration protocol. The system is controlled by a custom LabView software executed on a PC equipped with the NI-PCI-7831R board. A General Purpose Interface Bus (GPIB) connects the PC to the Tek AFG 3242 pulse generator. Figure 4.9 shows a block scheme of this setup system.

FZ Jülich setup

The second setup system is developed at the institute for nuclear physics (IKP) of Forschungszentrum Jülich. In this setup the communication between the ToPix_2 testboard and the digital readout board is implemented by an adapter board for voltage translation from 1.2 V to 3.3 V. The core of the digital board is a Xilinx Virtex 4 VLX60 FPGA and a SIS 1100 optical card is employed for the connection with the PC running a custom readout software written in C++. Figure 4.10 shows a picture of this setup system.

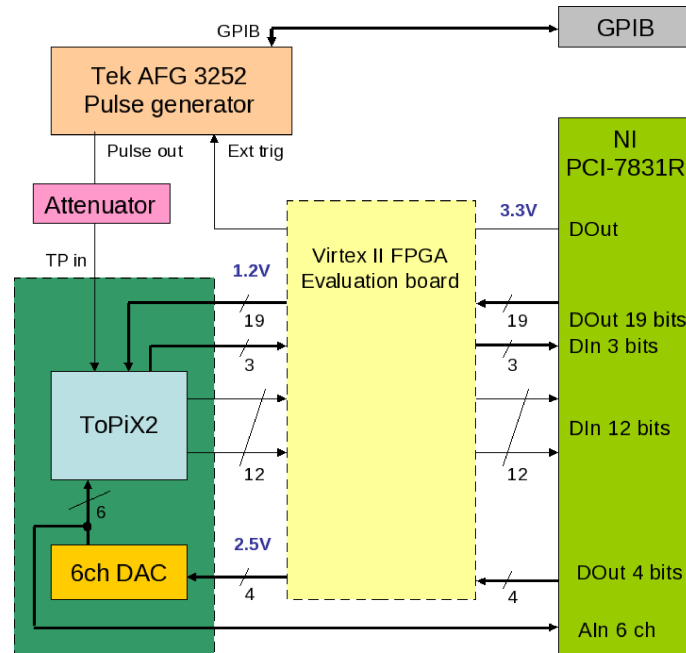


Figure 4.9: Torino setup scheme.

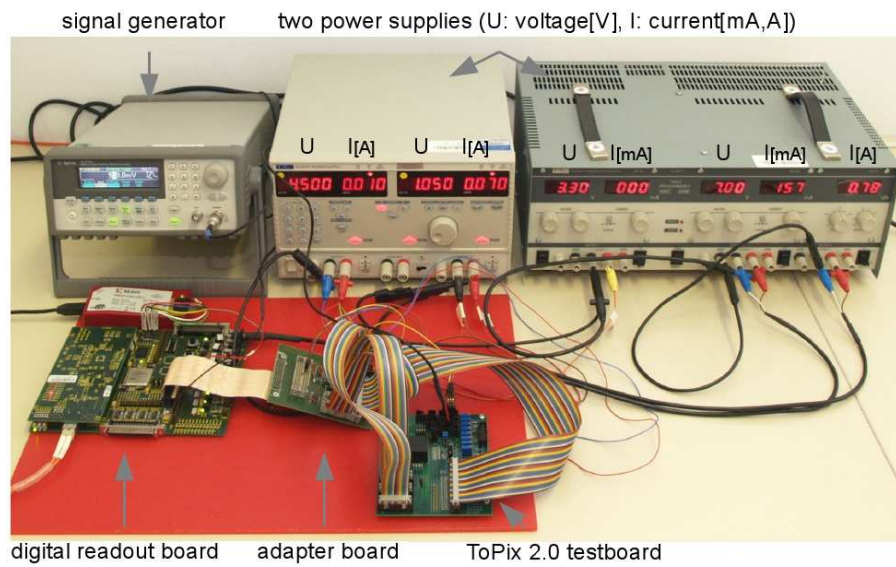


Figure 4.10: FZ Jülich test setup.

4.2.3 Test results

Signal reconstruction

In ToPix_2 the CSA output is not accessible on the ASIC pad, and only ToT information is available. For test purposes, the shape of the CSA output signal can be reconstructed performing a series of measurement with a fixed value of injected charge varying the threshold as shown in Figure 4.11. The signal peak can be interpolated finding the intersection between the linear fit on the leading edge and trailing edge data. Figure 4.12 shows the ToT scan result for different values of input charge.

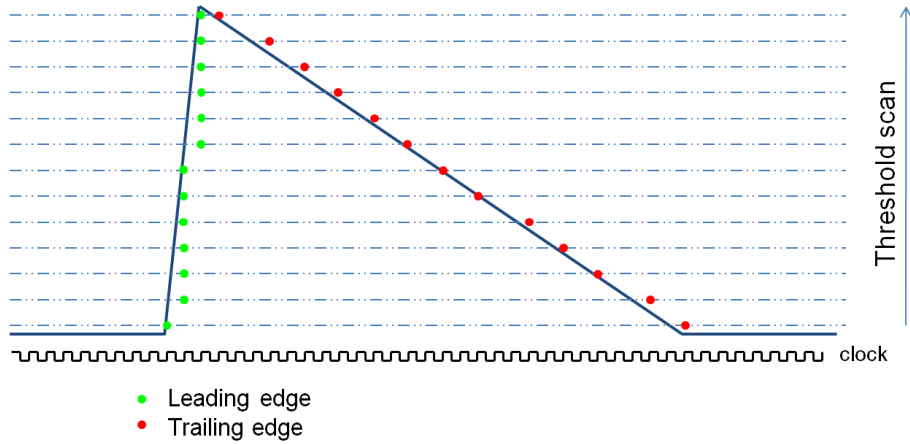


Figure 4.11: Threshold scan representation.

The standard method for the noise measurement foresees a threshold scan close to the peak of a small signal. In ToPix_2, due to a bug in the calibration line, it is not possible to send a simultaneous test pulse to every pixel. Therefore for a fast noise measurement a threshold scan in the baseline region without any signal has been performed. It has been measured that this approach gives the same noise value of the standard approach. For each threshold value a set of measurements are performed by observing the system for a fixed small time window. $R(V_{th})$ is defined as the ratio between the number of times that the noise crosses the threshold and the total number of observation. The measured points are fitted with an S-curve (Error function), the mean is the baseline value $V_{baseline}$ and σ_v is the noise:

$$R(V_{th}) = \frac{1}{2} \left(1 + \operatorname{erf} \left[\frac{V_{th} - V_{baseline}}{\sqrt{2\sigma_v^2}} \right] \right) \quad (4.1)$$

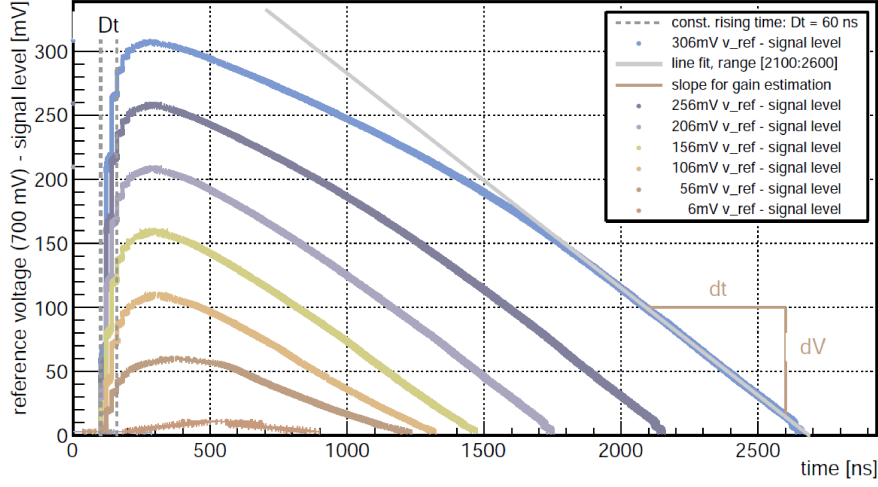


Figure 4.12: Reconstructed signal shape with threshold scan for different input charge values [85]. The two small signals are dominated by the calibration signal noise.

where $erf[x]$ is the error function:

$$erf[x] = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt \quad (4.2)$$

Dynamic range and linearity

ToPix_2 has been tested for either input polarity. Figure 4.13 shows the response of two different pixels cells compared with the simulation, in a input charge range between 1 fC and 100 fC for positive charges (p-type sensor). A linear fit has been performed on the experimental values, and the difference between the measured value and the fit is reported. The maximum dispersion from the linear fit is ± 1 fC. Linearity measurements on different cells have been performed to verify the charge measurement dynamic range, with a nominal discharging current of 5 nA. The obtained results are compatible with the following linear fit predicted by simulations for a p-type sensor signal:

$$ToT_p = \frac{Q_{inj}}{5.3 \text{ nA}} + 300 \text{ ns} \quad (4.3)$$

The measurements are in good agreement with the simulation results, and the Dynamic Range (DR) is:

$$DR = \log_2 \left(\frac{Q_{max}}{ENC} \right) = \log_2 \left(\frac{100 \text{ fC}}{0.026 \text{ fC}} \right) = 11.9 \text{ bit} \quad (4.4)$$

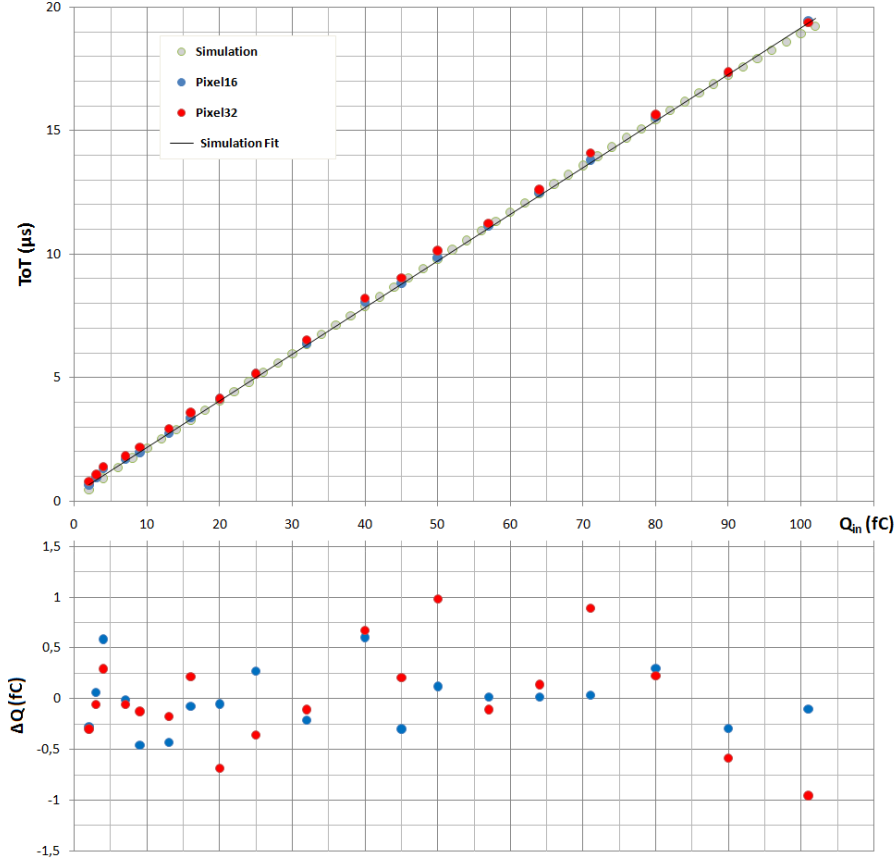


Figure 4.13: Linearity measurements for a p-type sensor compared with the simulation

The large ToT signals have a small low frequency component that is compensated by the baseline holder, leading in a compression of the ToT. For charge values close to 100 fC, the compression of ToT with a leakage current of 10 nA is $\approx 2\%$, and with a leakage current of 50 nA is $\sim 4\%$.

Detailed linearity measurements performed at FZ Jülich show a non linear charge - ToT relationship for output signals with $\text{ToT} \lesssim 1.2\mu\text{s}$. It can be roughly translated in a charge region $\lesssim 4$ fC. This non linearity is due to the fact that the shape of the response for low charge values is not perfectly triangular. This can be explained considering that for small output signals the differential stage (figure 4.7) does not work as a constant current generator but rather as a feedback resistance. The linearity in the small charge region can be improved by increasing the analog gain, since in this way it is possible to reduce the minimum charge required to fully steer the current in the differential pair.

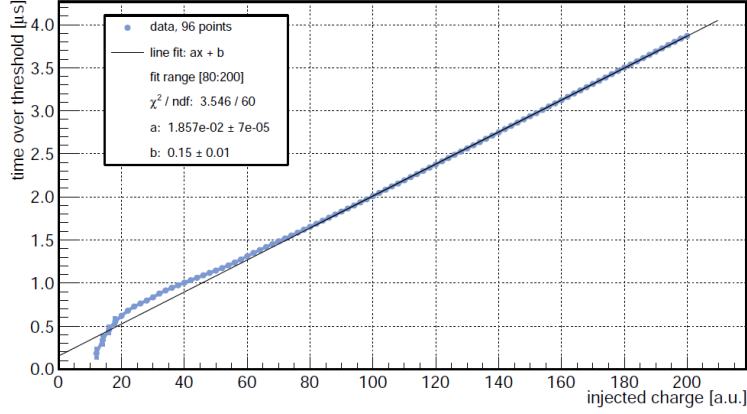


Figure 4.14: Non linearity for $\text{ToT} \lesssim 1.2\mu\text{s}$ [85]. Comparator threshold at 25 mV. Charge in arbitrary unit.

ToT dispersion

The channel to channel rms ToT dispersion is $\frac{\sigma_{\text{ToT}}}{\text{ToT}} \approx 10\%$. The discharging feedback current has minor implication on the uniformity between the different channels (Figure 4.15). This result shows that the current source that biases the feedback stage does not give the major contribution in the ToT dispersion. The other blocks that contribute to the ToT dispersion are the differential pair of the feedback stage and the differential pair of the leakage compensation. Montecarlo simulations have been performed to understand how to improve the ToT uniformity. The critical block is the leakage compensation stage, where the mismatch effects on its input transistors creates an offset that unbalance the feedback circuit changing the effective discharging current value.

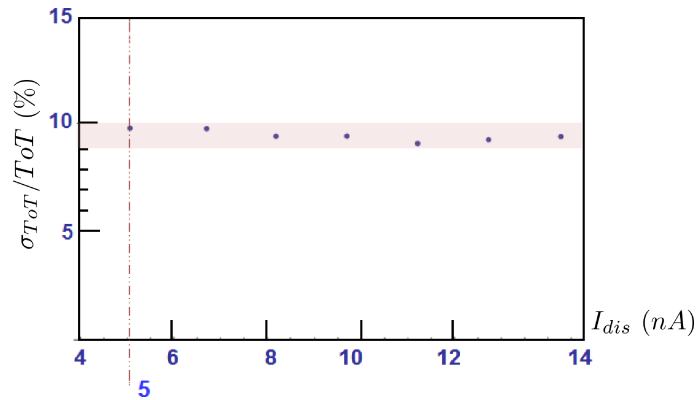


Figure 4.15: ToT dispersion

Threshold dispersion

The local 5 bit DAC in each pixel for the threshold dispersion mitigation has been tested. Figure 4.16 shows the dispersion of the threshold values before the correction and after the correction. With a fine tuning it is possible to reduce the peak to peak value of the dispersion from ~ 30 mV to ~ 2 mV.

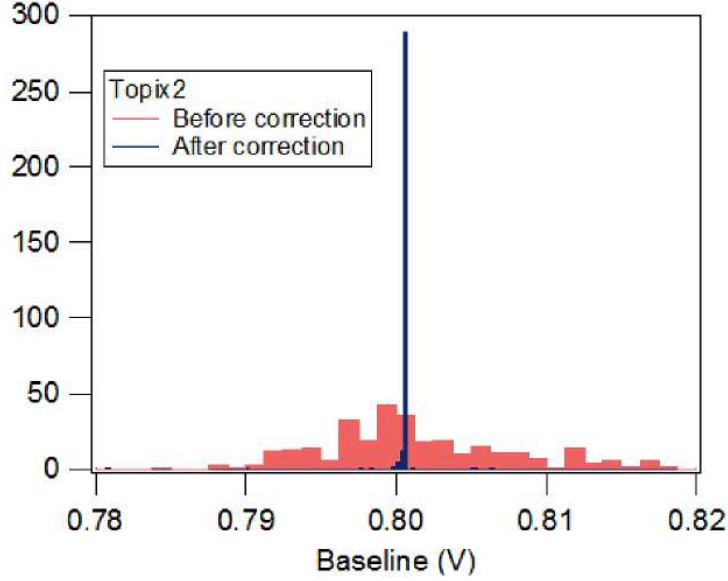


Figure 4.16: Threshold dispersion

Spectra with an epi-sensor

ToPix_2 has been tested with an epitaxial sensor (thickness: $50\text{ }\mu\text{m}$, size: $125\text{ }\mu\text{m} \times 325\text{ }\mu\text{m}$) connected by wire bonding to the external pad of the chip. Figure 4.17 shows the spectra obtained using a ^{214}Am source (60 keV γ photons). In this case the signal to noise ratio is limited by parasitics capacitance due the external connections: bonding pad, wire bonding and protection diodes.

Calibration

ToPix_2 has been successfully calibrated with ^{214}Am source (60 keV γ photons). Figure 4.18 shows the result of the calibration performed with the 60 keV γ emitted by Americium source on a standard floating zone p-type sensor ($300\text{ }\mu\text{m}$ thick, size: $50\text{ }\mu\text{m} \times 425\text{ }\mu\text{m}$). The peak amplitude has been reconstructed multiplying the ToT by the tail slope of the ToT signal. The input charge depends on the number of

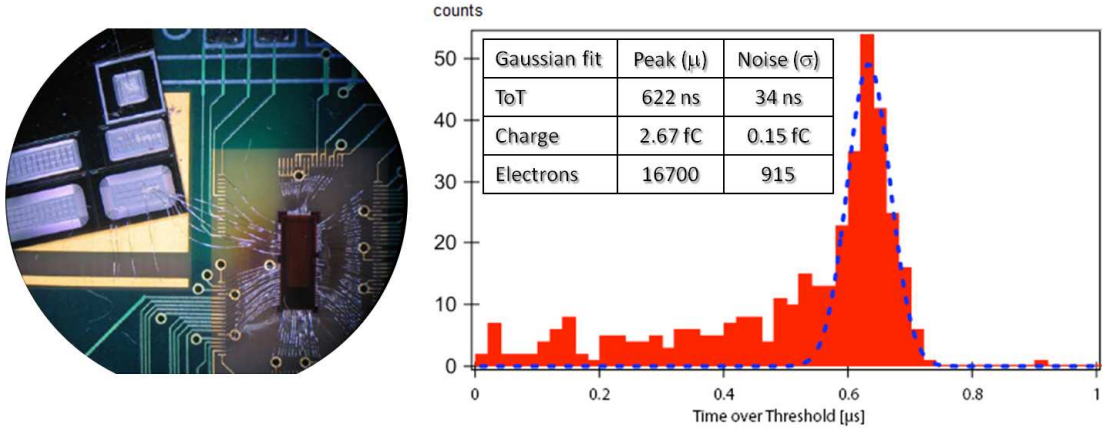


Figure 4.17: Epitaxial sensor measurement with a ^{214}Am source.

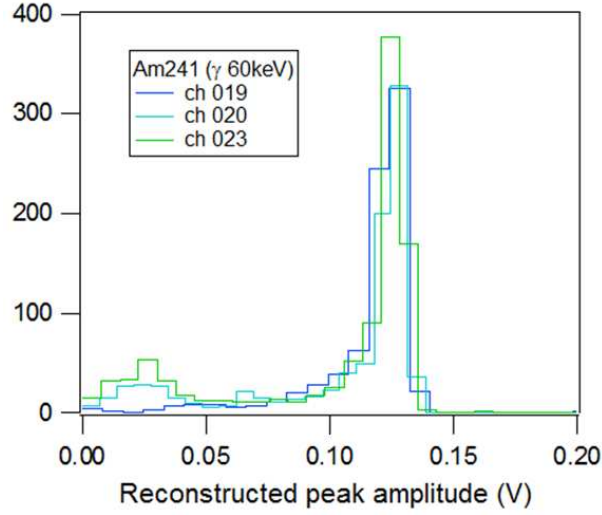


Figure 4.18: Calibration with 60 keV γ from Americium source.

electron/hole (e/h) pairs which is given by the ratio between the γ photon energy and the e/h creation energy:

$$N_{e/h} = \frac{E_\gamma}{E_{e/h}} = \frac{60 \text{ keV}}{3.6 \text{ keV}} = 1.67 \cdot 10^4 \rightarrow Q_{in} = 2.67 \text{ fC} \quad (4.5)$$

The response of the three channels are close to the expected value:

$$V_{peak} = \frac{Q_{in}}{C_f} = \frac{2.67 \text{ fC}}{24 \text{ fF}} = 0.111 \text{ V} \quad (4.6)$$

Baseline shift for an opposite polarity signal

Figure 4.19 shows the response of a pixel readout cell in p-type configuration, for a square pulse over the calibration capacitance. The rising edge of the pulse injects a positive current in the readout cell and the ToT stage response is proportional to the injected charge value. The plot shows the linear time over threshold range and the overshoot as expected from circuit simulations. The falling edge of the pulse injects a negative current pulse in the readout cell. This leads to the shift of the baseline thus increasing the restoring time ($\sim 150 \mu\text{s}$). This effect is due to the fact that the PMOS which implements the equivalent resistor in the leakage compensation RC filter (Fig. 4.7) works properly only when the signal at the output of the differential pair that drives the RC filter is moving downward from its steady point. In case of a signal moving upward the source and drain of the PMOS are exchanged and its equivalent resistance drops.

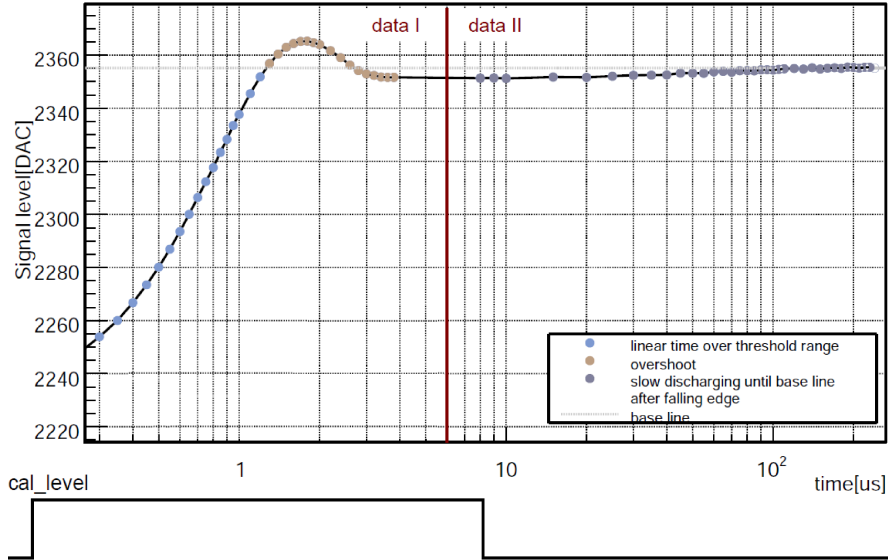


Figure 4.19: Baseline shift due to negative current pulse in a readout cell in p-type configuration [85]. Data I: signal after charge injection; Data II: Signal after falling edge the signal generator, bottom: square pulse over the calibration line. Time in logarithmic scale, 1 DAC = 0.3 mV.

In principle the polarity selector guarantees the proper swing of the signals in this point. However using the calibration line implies always the injection also of a signal with the opposite polarity for which the circuit has been programmed. Therefore the filter is used in a non appropriate condition which leads to the long settling times. The tolerance for current pulses of opposite signals (i.e. negative current for a p-type sensor) is required not only for test purposes, in order to send a fast square pulse sequence on the calibration line, but also in case of a cross talk current signal

coming from neighbor pixels (see section 3.3.2). When the CSA of a neighbor pixel saturates, a triangular shaped voltage pulse is present on the interpixel capacitance which is coupled to the input node of the pixel under observation. The rising edge of the triangular pulse injects a current pulse of the same polarity of the one of sensor, while the falling edge injects a current signal of opposite polarity. The resulting baseline shift will increase the system dead time. Since a large number of particles that can saturate the CSA is expected, the correct management of current signals of opposite polarity it is of utmost importance for the ToT system reliability. The details of the solution implemented to suppress the baseline shift in ToPix_3 are given in section 5.2.2.

Ionizing damage test

Total Ionizing Dose test was performed on four chip using the X-ray irradiation facility at CERN with a dose rate of 407 rad/s for a TID of 35 Mrad [83]. After irradiation an annealing phase at 100°C has been followed. During the irradiation an average baseline dispersion below 3% has been observed, a such low value is comparable with the dispersion due to the process variation. Concerning the noise during irradiation a maximum increase of 20% has been measured, corresponding to ~ 30 ENC. The annealing phase has a beneficial effect both on the baseline value which is partially recovered and on the noise which returns close to the value before irradiation. Measurement on the average and rms values of the tail slope have been performed during irradiation. The tail slope depends on the ratio between the discharging current and the CSA feedback capacitance. In ToPix_2 the CSA feedback capacitance is 24 fF, and the nominal discharging current is 5 nA, hence the tail slope is 0.21 mV/ns. After irradiation the tail slope increases by a factor of ~ 2 . This means that in addition to the nominal discharging current of 5 there is a radiation induced leakage current approximately of the same value. The rms value of the tail slope distribution of the different channels before the irradiation is 0.01 mV/ns, at 10 Mrad it increases by a factor of ~ 2 , at 35 Mrad it increases by a factor of ~ 6 . The baseline and noise variation are satisfactory whereas the tail slope results requires the correct key of interpretation in order to be validated. The test is performed with a dose rate of 3 order of magnitude larger than the $\overline{\text{P}}\text{ANDA}$ dose rate, with a final TID 3 times larger than the value expected in the experiment lifetime. Ionizing radiation damage test on ToPix_1 shown that at low dose rate the damage effect is limited thanks to the annealing beneficial effect. Hence the obtained results are beyond any worst estimation. However the linear relationship between ToT and Q_{in} is maintained and it is possible to make a local calibration with the internal test charge injection circuit.

4.2.4 Single event upset test

The charge generated by a ionizing particles in the sensitive volume can be large enough to significantly alter for a short time the voltage on an internal node of a latch memory, consequently flipping the value of the stored bit. This effect is known as Single Event Upset (SEU) and it is a non destructive single event effect. However if a bit of the pixel configuration register flips following a SEU, the correct functionality of the circuit may be compromised. The SEU depends on two parameters, the sensitive volume and the minimum energy required for an upset. Deep-submicron CMOS technologies are more sensitive to SEU [86].

The ToPix_2 configuration register is based on the Dual Inter-locked Storage Cell (DICE) [87], SEU hardened architecture for latches, where the capability to resist particle hits is based on the cross coupled inverter latch structure. Figure 4.20 shows the layout and the schematic view of a DICE cell. All the PMOS transistors are implemented in the same n-well in order to increase the SEU tolerance. When the write command is active $D1$ and $D2$ are set to the bit value, $\overline{D1}$ and $\overline{D2}$ are set with to the bit negation value. When the read command is active $D1$ and $\overline{D1}$ are sent as output. The reset RN is active low.

The employment of DICE cell has been chosen for the reduced size ($5\ \mu\text{m} \times 6\ \mu\text{m}$) which allow to contain the area occupancy of the memories. The DICE cell size is $5\ \mu\text{m} \times 6\ \mu\text{m}$. Using the ion beams at the SIRAD [88] facility of the INFN-LNL laboratory a radiation damage characterization has been performed to test the SEU sensitivity of the DICE memories.

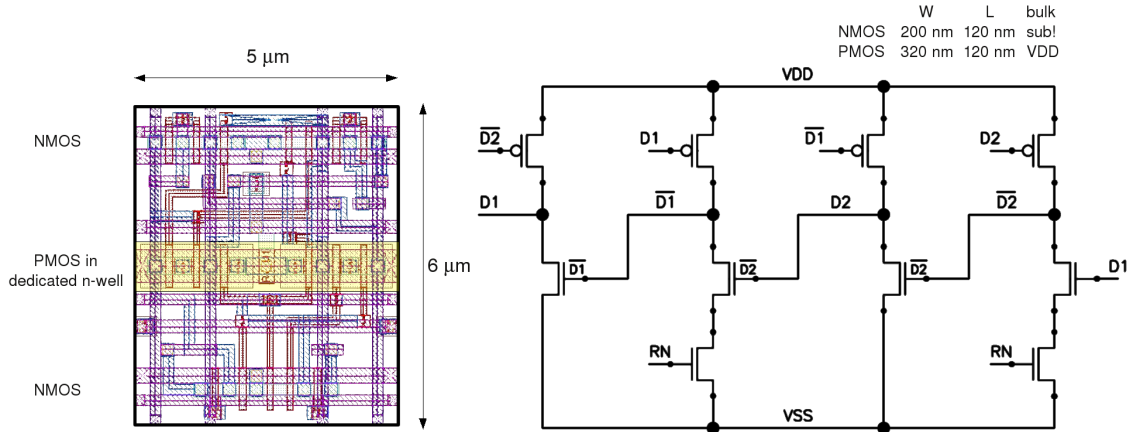


Figure 4.20: Layout and schematic view of the DICE cell.

Experimental setup

The ToPix_2 PCB was fixed on a sample holder movable with a step motor and was placed inside the irradiation chamber held at vacuum (pressure of $8 \cdot 10^{-6}$ mbar) to take advantage of the full beam energy. The PCB was connected to the acquisition board placed outside the irradiation chamber with cables of few meters. The clock frequency was reduced at 10 MHz, in order to work with the large capacitive load given by these long cables. A PC running LabView equipped with the NI-PCI-7831R board generates patterns and works as a triggered memory. A Virtex II FPGA implements the configuration protocol. To analyze the SEU sensitivity for different values of Linear Energy Transferred (LET), tests with different ion beams of different energies were performed at the SIRAD facility. To achieve a different LET without changing the ion beam, the mobile support structure was rotated of 30° .

To test the DICE memory sensitivity to SEU, the 12 bit configuration registers embedded in all the 320 pixel cells, were taken into account. All the registers are readable but only the configuration register is writable externally. A LabView software performed the SEU online analysis. The 12 bits of all the configuration registers were written with a test pattern made of alternatively 0 and 1, after 2 seconds the register was read and each difference was counted as a SEU, finally the original 12 bit sequence was written again.

Test results

The Single Event Upset cross section, the probability to have an upset, is

$$\sigma_{SEU} = \frac{N_{errors}}{\Phi N_{bit}} \quad (4.7)$$

where N_{errors} are the number of SEUs, Φ is the total incident particle fluence and N_{bit} is the total number of bits. The experimental points are fitted with the Weibull function [89], which gives the SEU cross section as a function of the deposited ionization energy E_{dep} (a sensitive volume of $1 \mu m^3$ is assumed):

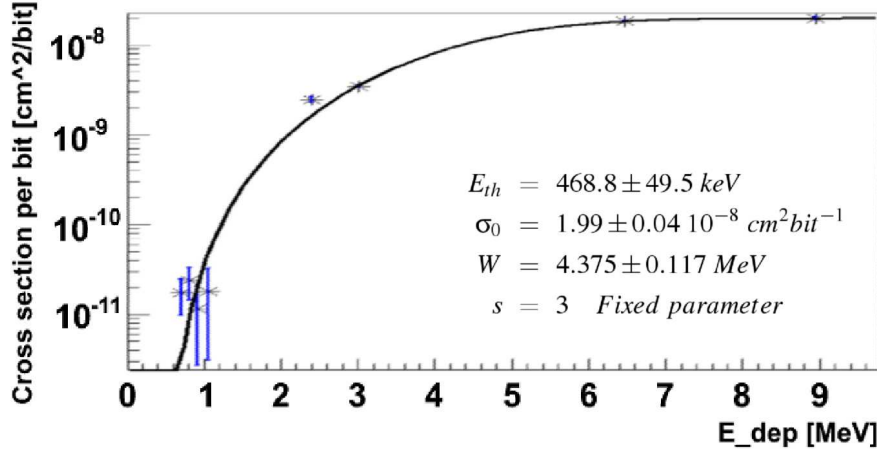
$$\sigma = \sigma_0 \left[1 - e^{-\left(\frac{E_{dep} - E_{th}}{W}\right)^s} \right] \quad (4.8)$$

where W and s are shape parameters, σ_0 is the saturated SEU and E_{th} is the deposited energy threshold for a SEU. For each configuration in Table 4.3 more runs were performed to calculate an average value for σ_{SEU} , and estimate the error using the standard deviation.

In order to compare this result with the SEU capability of a standard memory without any protection two 12 bits register of the peripheral logic were also tested.

Ion	Beam Angle	E_{dep} [MeV]	σ_{SEU} [cm^2/bit]	$\delta\sigma_{SEU}$
^{16}O	0°	0.70	$6.646 \cdot 10^{-8}$	$2.866 \cdot 10^{-8}$
^{16}O	30°	0.81	$9.178 \cdot 10^{-8}$	$3.621 \cdot 10^{-8}$
^{19}F	0°	0.91	$4.480 \cdot 10^{-8}$	$3.451 \cdot 10^{-8}$
^{19}F	30°	1.07	$6.851 \cdot 10^{-8}$	$5.675 \cdot 10^{-7}$
^{28}Si	30°	2.40	$9.435 \cdot 10^{-6}$	$6.182 \cdot 10^{-7}$
^{35}Cl	0°	3.01	$1.326 \cdot 10^{-5}$	$3.257 \cdot 10^{-7}$
^{58}Ni	0°	6.47	$7.071 \cdot 10^{-5}$	$9.794 \cdot 10^{-6}$
^{79}Br	0°	8.96	$7.611 \cdot 10^{-5}$	$3.430 \cdot 10^{-7}$

Table 4.3: SEU cross sections of ToPix_2, for the different ions.


 Figure 4.21: Weibull fit to the experimental ion data of ToPix_2 configuration register. A sensitive volume of $1 \mu m^3$ is assumed.

The 12 bits shift register was tested with a cycle similar for the configuration register. The 12 bits counter was tested with a periodic cross check with a synchronized counter implemented on FPGA. Table 4.4 shows the SEU cross section for registers based on DICE and standard architectures. In the memories without SEU protection the energy threshold is $E_{th} \approx 0$, and the saturation cross section σ_0 is ~ 1.3 times larger.

The SEU rate can be calculated by knowing the MVD particles rate [91] and the probability for a certain particle to deposit a certain energy in the sensitive volume. Hadrons with an energy larger than 20 MeV are considered to induce the same SEU given by protons [92], while the leptons contribution is negligible. A SEU cross section of $8.78 \cdot 10^{-16} cm^2/bit$ has been calculated for the configuration

Device	Architecture	E_{th} [MeV]	σ_0 [cm ² bit ⁻¹]	W [MeV]
Configuration register	DICE	0.47	$1.99 \cdot 10^{-8}$	4.38
Shift register	Standard	$1.58 \cdot 10^{-15}$	$2.6 \cdot 10^{-8}$	1.03
Counter	Standard	$7.31 \cdot 10^{-14}$	$2.6 \cdot 10^{-8}$	1.46

Table 4.4: SEU cross sections. [90]

register. In comparison the SEU cross section is 34 times larger for the shift register and 54 time larger for the counter. Supposing to use the DICE architecture in the final version of ToPix, taking into account all the 12760 pixel configuration registers (12 bits), a rate of 3 SEU/hour per chip is expected. Considering all the 824 pixel readout chips of the MVD pixel detector it is possible to estimate a rate of 2472 SEU/hours. [90]. To reduce the number of errors, the Single Event Upset tolerance has to be increased. For this reason for the ToPix architecture a Triple Modular Redundancy (TMR) with majority voting memory cell has been chosen.

4.2.5 Results summary

The measurements discussed in this section are summarized in Table 4.5.

ToT gain	$152 \text{ ns/fC} \pm 6 \text{ ns/fC}$
Input charge range	from 1 fC to 100 fC
Equivalent Noise Charge	$163 e^- \text{ rms}$
Threshold dispersion	$\sim 2 \text{ mV}$ (5 bits DAC tuning)
Time resolution	5.8 ns (50 MHz clock)
Power consumption	$< 20 \mu\text{W/cell}$
Radiation dose	35 Mrad X-ray
Baseline variation	$\sim +3\%$
Noise variation	$\sim +20\%$
ToT gain variation	factor 2

Table 4.5: ToPix_2 performance before and after irradiation.

These results have guided the design of ToPix_3 discussed in chapter 5. The measured noise of 163 ENC meets the requirements. The channel to channel threshold dispersion is mitigated by the 5 bit DAC with a maximum variation of ~ 2 mV. The TID test shows that a satisfactory radiation hardness is achieved for the PANDA environment with the employment of standard layout transistors. A good linearity is achieved for large charges up to 100 fC, with a maximum deviation from the linear fit < 1 fC. The linearity has to be increased for charges $\lesssim 4$ fC. The

strict unipolarity of the baseline restorer is an issue in case of cross talk. The DICE architecture is not enough SEU tolerant for the $\overline{\text{PANDA}}$ environment. Therefore the pixel registers have been redesigned in ToPix_3 with an architecture based on TRM in order to increase SEU tolerance. This has determined an increase of the digital area which now occupies 50% of the pixel cell. Therefore the layout of the analog part was completely revised as well.

Chapter 5

ToPix_3 analog readout

The experience gained with the two prototypes discussed in chapter 4 has provided the guidelines to develop the final version of the front-end electronics. While the overall architecture remained unchanged, all the building blocks were re-implemented from scratch. The complete redesign was motivated by three facts. First, key performances of the analogue part, such as the gain of the front-end stage, the capability of the baseline restorer to handle simultaneously pulses of either polarity and the precision of the current feed-back had to be improved. Second, the area of the analogue parts had to be reduced by 35% to accommodate the increased digital part. Third, a different flavor of the process, which optimizes the routing of the power supplies, was chosen for the implementation of the final chip. The design and the optimization of the final front-end was the topic of the last part of this PhD work. In February 2011 the ToPix_3 prototype, incorporating all aforementioned improvements was submitted to the foundry for fabrication. This chapter describes in detail the design of the new analogue blocks. The transistor level implementation is presented along with the results of extensive computer simulations.

5.1 Front end analysis

One of the primary goals of ToPix is to minimize the power consumption. Therefore, in the front-end a “shaper-less” architecture has been chosen, in which the output of a single stage Charge Sensitive Amplifier (CSA) drives directly the discriminator. A preliminary noise study of the CSA can be performed assuming a front end model [51] which simplifies the ToT stage transfer function calculation for small signals (Fig. 5.2). The input capacitance C_{in} takes into account the detector capacitance and the other capacitances between the input transistor gate and ground. The core amplifier model foresees a single transistor stage with transconductance g_m , output resistance R_0 and output capacitance C_0 . The ideal unity gain

buffer avoid any loading effect that would reduce the CSA open loop gain. The feedback capacitance C_f is connected directly to the preamplifier output to avoid extra phase shifts introduced by the buffer. The feedback capacitance is discharged by the resistive feedback R_f .

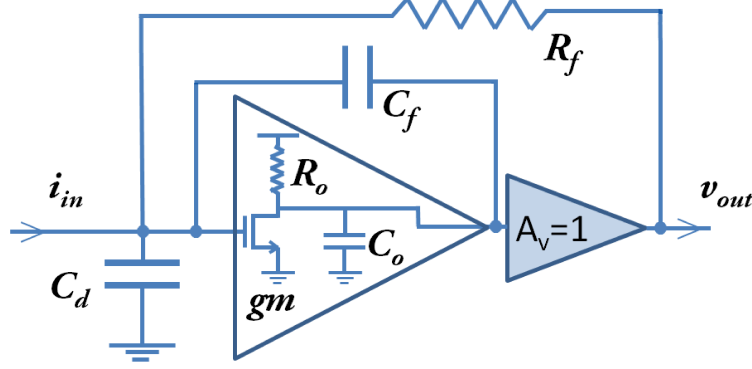


Figure 5.1: Simplified front-end for small signal transfer function calculation.

Under the assumption of $C_{in} \gg C_f$ and core amplifier open loop gain $A_v \gg 1$, the transfer function can be expressed as:

$$H(s) = \frac{v_{out}}{i_{in}} \approx \frac{R_f}{(1 + \frac{s}{\omega_1}) \cdot (1 + \frac{s}{\omega_2})} \quad (5.1)$$

where the two poles are:

$$\omega_1 \approx \frac{1}{R_f C_f} = \frac{1}{\tau_f} \quad (5.2)$$

$$\omega_2 \approx \frac{g_m C_f}{C_o C_{in}} = \frac{1}{\tau_r} \quad (5.3)$$

The response for a negative delta current pulse $I_{in}(t) = -Q_{in} \delta(t)$ is given by the inverse Laplace transform of 5.1:

$$v_{out}(t) = Q_{in} R_f \frac{e^{-t/\tau_f} - e^{-t/\tau_r}}{\tau_f - \tau_r} = \frac{Q_{in}}{C_f} \frac{e^{-t/\tau_f} - e^{-t/\tau_r}}{1 - \tau_r/\tau_f} \quad (5.4)$$

and the output signal peaking time, which is independent from the input charge, is given by:

$$\left. \frac{dv_{out}(t)}{dt} \right|_{t=t_p} = 0 \implies t_p = \frac{\tau_r \ln[\tau_f/\tau_r]}{1 - \tau_r/\tau_f} \quad (5.5)$$

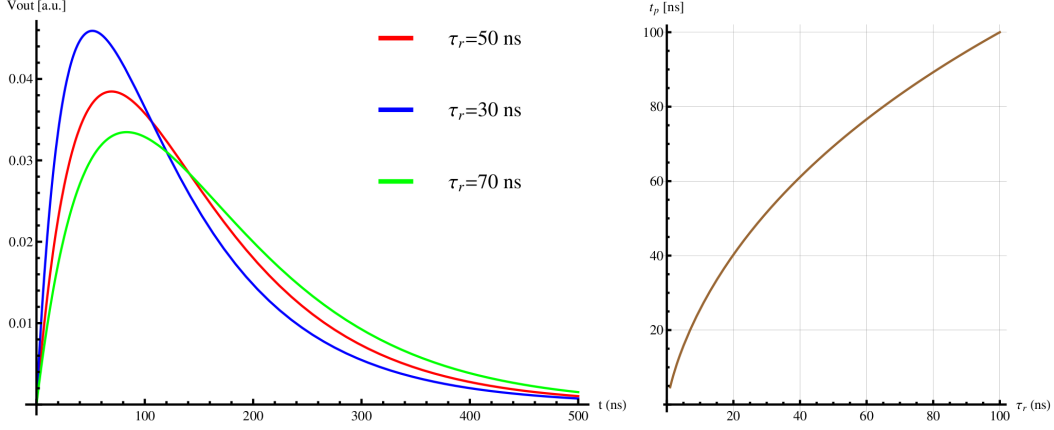


Figure 5.2: Output signal calculated from equation (5.4) for different τ_r with $\tau_f = 100$ ns (left). Peaking time t_p as a function of τ_r (right).

Figure 5.2 shows the output signal shape for three different τ_r values and the peaking time t_p as a function of τ_r . In both cases the falling time is fixed $\tau_f = 90$ ns. For small τ_r values the contribution of τ_f is not negligible.

From equation 5.2 it is possible to evaluate the falling time t_r . The feedback resistance R_f represents the small-signal equivalent resistance of the feed-back network. This, as described elsewhere in this thesis, is implemented with a differential pair with PMOS input transistors. Since these transistors are typically biased with a current of 5 nA, they operate in weak inversion. Therefore the equivalent resistance is given by:

$$R_f = g_m^{-1} = \left(\frac{I}{n k_B T / q} \right)^{-1} = 6.6 \text{ M}\Omega \quad (5.6)$$

where k_B is the Boltzmann constant, T the absolute temperature and q the electron charge. The correction factor n depends on the ratio between the gate-channel capacitance C_{gc} and bulk-channel capacitance C_{bc} , in our case $n = \frac{C_{bc}}{C_{gc}} + 1 \sim 1.3$. Using a feedback capacitance $C_f = 12$ fF the fall time is

$$\tau_f = R_f C_f \approx 80 \text{ ns} \quad (5.7)$$

Equation 5.2 shows that the rise time depends on the detector capacitance C_{in} (which is assumed to be 200 fF) and the input parasitic capacitance (estimated to be 200 fF), the preamplifier load capacitance C_0 which is ~ 50 fF and the transconductance of the input transistor, g_m . Therefore to reduce the rise time a larger g_m is required and, consequently, a larger power consumption. As discussed in chapter 3, for ToT measurements we are not interested in the peak of the signal but rather on a precise

timing measurement of the leading and trailing edges. Furthermore, the accuracy of the leading edge determines the precision of the time stamp that tags the event. The time jitter depends on the ratio between the rms output noise and the slope of the signal, so for a constant peaking time, it decreases for larger signals. In this design, it has been chosen to have a time jitter equal to the quantization noise for signals of 1 fC in the worst noise condition, i.e. for a total input referred noise of 200 electrons rms. Such value of noise is expected at the end of the lifetime of the detector, when the sensor leakage current will increase significantly due to the radiation damage. This choice guarantees jitters well below the quantization error (so the latter will dominate the accuracy of the timestamp) for most of the signals of interest, while allowing for low power consumption. The rise time t_r has therefore to be optimized so that the slope of the signal is always sufficient to reduce the jitter to a value lower than the quantization error given by the 155 MHz clock, i.e.:

$$jitter_{le} < \sigma_t = (f_c \sqrt{12})^{-1} = 1.8 \text{ ns} \quad (5.8)$$

The system noise requirement is 200 ENC translates into an output rms voltage of:

$$v_{out,noise} = \frac{ENC}{C_f} = 2.7 \text{ mV} \quad (5.9)$$

Therefore the slope required to satisfy the condition expressed in equation (5.8) is:

$$\frac{dV}{dt} \geq \frac{v_{out,noise}}{\sigma_t} = 1.5 \text{ V}/\mu\text{s} \quad (5.10)$$

Supposing to have an output signal with an amplitude of 75 mV and fixing the comparator threshold at 1/3 of the peak value (25 mV from the baseline), it is possible to calculate the rise time by evaluating dv_{out}/dt at the threshold crossing point. Therefore one can evaluate the time at which the leading edge crosses the comparator threshold as: $v_{out}(t_{le}) = v_{th}$, and the slope at the crossing point:

$$\left. \frac{dv_{out}(t)}{dt} \right|_{t=t_{le}} \geq \frac{v_{out,noise}}{\sigma_t} \quad (5.11)$$

This equation has been solved with a numerical method and it is verified for $\tau_r \lesssim 40$ ns. Once the rise time has been fixed, it is possible to calculate the required input transistor transconductance from equation (5.3)

$$g_m = \frac{C_o C_{in}}{C_f \tau_f} = \frac{50 \text{ fF } 400 \text{ fF}}{12 \text{ fF } 50 \text{ ns}} = 20 \text{ } \mu\text{S}. \quad (5.12)$$

The input transistor should work in weak inversion, where the g_m/I_{ds} ratio is maximized.

$$g_m = \frac{dI_{ds}}{dV_{ds}} = \frac{I_{ds}}{nk_B T/q} \quad (5.13)$$

where I_{ds} is the drain source current, V_{ds} is the drain source current. Knowing g_m , from equation (5.13) it is possible to calculate the lower limit for the bias current of the input transistor:

$$I_{ds} = g_m(nk_B T/q) = 1.3 \mu\text{A} \quad (5.14)$$

The two poles model can be oversimplified especially for very low power circuits where the contribution of higher order time constants may not be negligible.

5.1.1 Minimum noise estimation

It is well known that in an optimized front-end the noise should be dominated by the input transistor. The input referred thermal noise spectral density for a MOS transistor operating in the subthreshold region is:

$$e_{n_{th}}^2 = 4 k_B T \gamma \frac{1}{gm} = \frac{2k_B T}{g_m}$$

where the inversion coefficient γ has been assumed to be $\frac{1}{2}$ in weak inversion. It is possible to translate the voltage noise into a current noise dividing the input referred voltage noise by the input impedance:

$$i_n^2 \approx e_n^2 |(s C_{in})|^2$$

The ENC can hence be defined through the transfer function $H(s)$:

$$ENC_{th} = \frac{C_f}{q} \left(\int_0^\infty |s H(s)|^2 i_n^2 df \right)^{\frac{1}{2}} = \sqrt{\frac{1}{2} k_B T \frac{C_{in} C_f}{C_o q^2}} \quad (5.15)$$

Assuming $C_f = 12$ fF $C_o = 50$ fF and $C_{in} = 400$ fF, the thermal noise contribution turns out to be $\sim 88 e^-$. It is worth nothing that in this simplified model the transconductance of the input transistor, gm , does not appear in the ENC expression because it defines both the shaping time and the noise contribution. Therefore the decrease in noise for higher transconductance is canceled-out by the corresponding increase of the bandwidth. This is only an approximation, since, in practice, the transfer function will contain higher order poles that will contribute to the shaping. Introduced by the other elements in the feed-back loop (output buffer, current feed-back generator) these poles do not depend on the transconductance of the input device, so an increase in the input bias current would bring some noise advantage.

The 1/f noise spectral density is given by:

$$e_{n_{1/f}}^2 = \frac{K_f}{C_{ox} W L} \frac{1}{f}$$

where K_f is a constant dependent on technology and device, C_{ox} is the gate capacitance per unit area, W and L are the effective transistor size.

$$ENC_{1/f} = \frac{C_f}{q} \left(\frac{K_f}{C_{ox}WL} C_{in^2} \int_0^\infty |H(s)|^2 \frac{1}{f} df \right)^{\frac{1}{2}} = \frac{C_d}{q} \sqrt{\frac{K_f}{C_{ox}WL}} \sqrt{\ln \left(\frac{\tau_f}{\tau_r} \right)} \quad (5.16)$$

For the 0.13 μm process used to implement the circuit, $K_f = 30 \cdot 10^{-25}$ J, $C_{ox} = 15$ fF/ μm^2 . The size of the input transistor has been chosen to be $W = 20$ μm and $L = 500$ nm. The choice of the transistor length (which is about four times the minimum allowed by the process) is dictated by the need of having a reasonable output impedance. The width is then selected in order to allow operation in weak inversion (where the gm to current ratio is the highest) in a reasonable range of bias currents around the selected point discussed above. The transistor should not be oversized, since in weak inversion the capacitance matching rule does not apply, and increasing the transistor size beyond necessity just brings in more parasitic capacitance. With these numbers, the flicker noise is calculated to be ~ 17 e^- and does not represent a severe concern.

The noise contribution of the feedback resistance R_f has to be calculated taking into account the current noise of the transistors that provides the discharging current. As one can see in Figure 5.14, two transistors are connected to the input node. The PMOS M1 of the differential pair and the NMOS M4 that sinks the PMOS bias current. At the equilibrium both are biased with 5 nA, so their total noise contribution is given by:

$$2i_{nw}^2 = 4k_B T g_m = \frac{4qI_{ds}}{n} \quad (5.17)$$

where the relationship between g_m and I_{ds} in weak inversion has been employed.

The white parallel ENC component is:

$$ENC_{pw} = \frac{C_f}{q} \left(\int_0^\infty |H(s)|^2 2i_{nw}^2 df \right)^{\frac{1}{2}} = \sqrt{\frac{I_{ds}}{n q}} R_f C_f \quad (5.18)$$

Solving the calculations, one finds 45 electrons rms.

The overall ENC is the sum in quadrature of the components calculated above.

$$ENC = \sqrt{ENC_{th}^2 + ENC_{1/f}^2 + ENC_{pw}^2} \approx 100 e^- \quad (5.19)$$

The value found for the noise has to be taken as a lower limit, since in the calculation only the main contributors are considered, which implies a simplified expression of the transfer function. The value estimated for the parasitic capacitances are an educated guess and the equations used in the hand calculations do not embed the

full complexity of deep submicron transistors. While the above considerations represent useful guidelines in the starting phase of the design, the final noise performance can only be assessed with simulations on the final layout, which combine complete transistors models with a more accurate estimation of the parasitic capacitances of the circuit. However even after a detailed design optimization several uncertainties remain. The precise contribution of the sensor capacitance and of the interconnect and the exact evolution of the sensor performance due to the radiation damage are a typical example. Therefore, the circuit should allow adequate flexibility in the adjustment of the bias point, in such a way that optimal performance can be attained for different experimental situations.

5.2 Building blocks design

5.2.1 Charge sensitive amplifier

The input stage is a gain enhanced cascode amplifier with capacitive feedback C_f . A feedback capacitance of 12 fF, which is half of the one employed in ToPix_2, has been chosen as the best compromise between the need of maximizing the gain for low signals and the one of having an adequate phase margin in the feed-back loop. The output stage is a source follower which is employed as a voltage buffer to drive the output capacitive load. The schematic view of this stage is shown in Figure 5.3.

Direct cascode

Figure 5.4a shows the full transistor implementation of the direct cascode stage, while in 5.4b the loads have been replaced with ideal components. The input signal is presented on the gate of M1 while M2 is the cascode transistor biased with an external voltage V_{casN} . Transistors M3 and M4 implement a cascode current mirror with current I_1 and equivalent resistance R_1 . The transconductance of transistor M1 is enhanced by the direct injection of I_2 from the cascode current mirror M5 and M6 with equivalent resistance R_2 . In this way it is possible to reduce the current load on transistors M3 M4, thereby increasing the output resistance. Table 5.1 shows the transistors parameter with $I_1 = 1.5 \mu\text{A}$ and $I_2 = 2.5 \mu\text{A}$. The total current in M1 is $4 \mu\text{A}$, and the input DC level voltage is fixed by this current and the size of the input transistor at $\sim 200 \text{ mV}$. The bias current selected for M1 is greater than the minimum value estimated in the first cut calculation ($1.3 \mu\text{A}$). This choice is motivated by the fact that the output source follower introduces a pole at relatively low frequency that contributes to the signal shaping. Therefore increasing the bias current in M1 allows to improve the noise figure since in this way only the bandwidth of the cascode is increased while the source follower still provides some extra filtering.

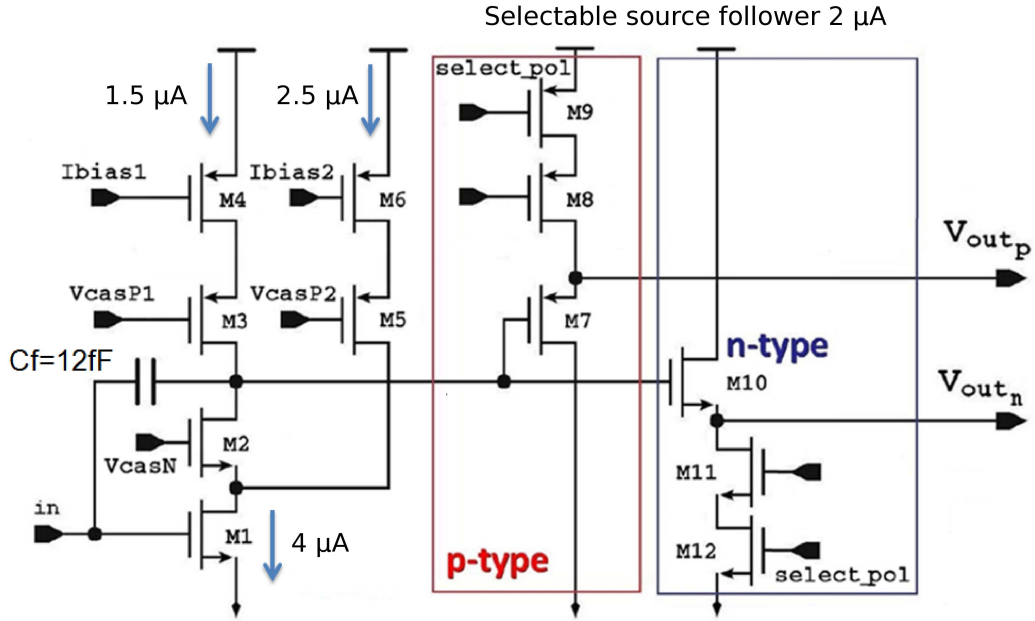


Figure 5.3: Charge Sensitive Amplifier schematic

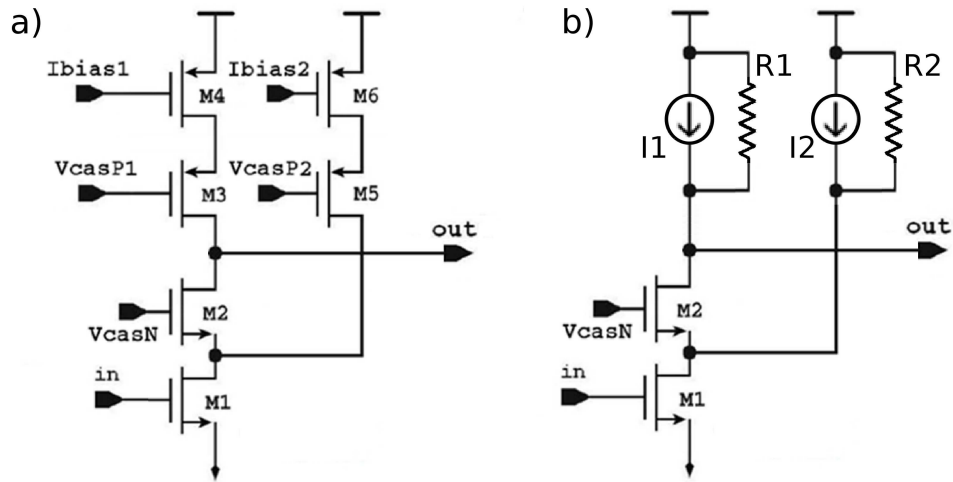


Figure 5.4: a) Direct cascode schematic and model. b) Simplified model.

From the small signal model it is possible to calculate the transfer function of the input stage. The calculations can be performed with the small signal model in a similar way as for the standard cascode amplifier. The resistances $R1$ and $R2$ of

MOS	W [μm]	L [μm]	gm [μS]	gm_b [μS]	ro [$M\Omega$]
M1	20	0.5	121.3	-	0.26
M2	5	0.5	43.9	7.39	0.69
M3	10	1	30.9	4.34	2.09
M4	6	2	23.4	-	2.96
M5	10	1	46.8	6.31	1.54
M6	6	4	24.1	-	2.33

Table 5.1: Input stage transistor parameters.

the cascoded current sources can be calculated as:

$$R1 = ro3 + ro4 + (gm3 + gmb3) ro3 ro4 \approx 224 M\Omega \quad (5.20)$$

$$R2 = ro5 + ro6 + (gm5 + gmb5) ro5 ro6 \approx 195 M\Omega \quad (5.21)$$

The equivalent resistance of the cascode input stage formed by M1 and M2 is given by:

$$R3 = (ro1 // R2) + ro2 + (gm2 + gmb2) (ro1 // R2) ro2 \approx 685 k\Omega \quad (5.22)$$

where the loading effect introduced by the current source delivering I2 has been included in the calculation. The DC gain of the amplifier is defined by the following expression:

$$A_{v0} = -\frac{R1 gm1 (ro1 // R2) (1 + (gm2 + gmb2) ro2)}{R1 + (ro1 // R2) + ro2 + (gm2 + gmb2) (ro1 // R2) ro2} \approx -1087 \quad (5.23)$$

The parallel combination of R1 and R3 defines the overall output resistance of the cascode stage. The dominant pole of the system is at the output node and its frequency can be determined as:

$$f_0 = \frac{1}{2\pi C_0 (R1 // R3)} \approx 500 kHz$$

where C_0 is the output capacitance

$$C_0 \approx C_{dg2} + C_{dg1} \approx 30 fF. \quad (5.24)$$

Figure 5.5 shows the Bode plot of the cascode stage.

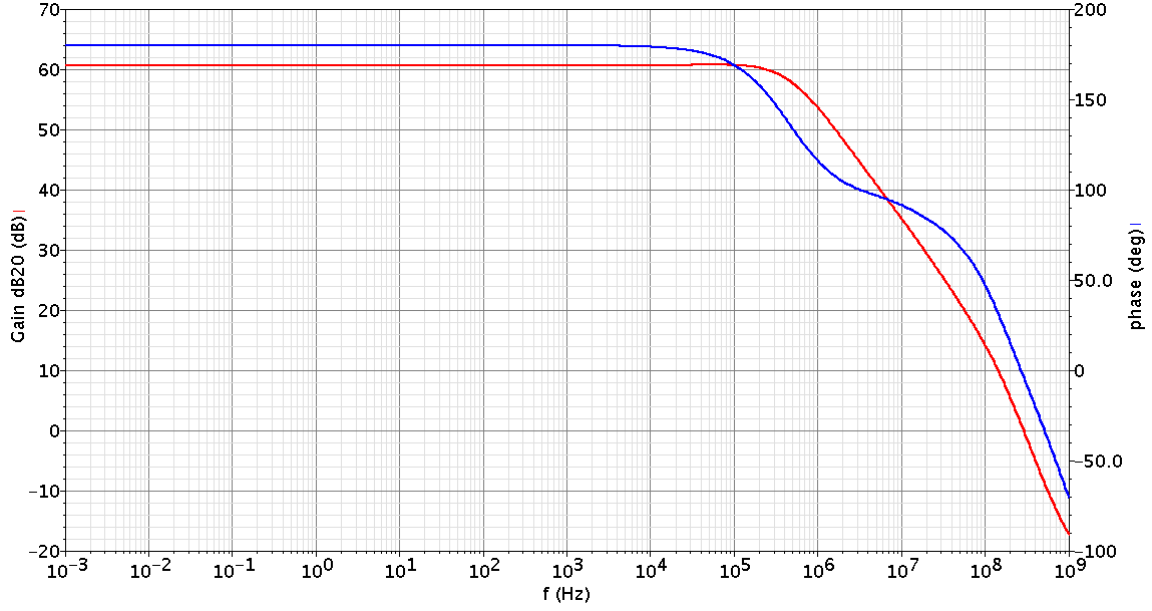


Figure 5.5: Cascode stage Bode plot.

Consideration on noise

The input equivalent noise can be computed as:

$$v_n^2 = \sum_{i=1}^6 \frac{A_{vi}}{A_{v0}} v_{ni}^2$$

where A_{v0} is the cascode stage gain found in 5.23 and A_{vi} indicate the voltage output gain of a voltage signal presented at the input of transistor M_i , hence $A_{v1} = A_{v0}$. v_{ni} is the noise of transistor M_i referred back to its input. The main noise contribution is the thermal noise, which has a spectral density:

$$e_{n_{th}}^2 = 4 k_B T \gamma \frac{1}{gm}$$

where the inversion coefficient γ can be assumed $\frac{1}{2}$ in weak inversion and $\frac{2}{3}$ in strong inversion.

The voltage gain of transistors M2, M3 and M5 is negligible. The contribution of transistor M4 and M6 have been calculated with the small signal model:

$$\frac{A_{v4}}{A_{v0}} = \frac{R0 \ gm4 \ ro4(1 + (gm3 + gmb3) \ ro3)}{R0 + ro4 + ro3 + (gm3 + gmb3) \ ro4 \ ro3} \frac{1}{A_{v0}} \approx \frac{1}{5} \quad (5.25)$$

$$\frac{A_{v6}}{A_{v0}} = \frac{R_x \, gm6 \, ro6 \, (1 + (gm5 + gmb5) \, ro5)}{R_x + ro6 + ro5 + (gm5 + gmb5) \, ro6 \, ro5 \, ro1 \, gm1} \frac{1}{gm1} \approx \frac{1}{5} \quad (5.26)$$

where R_x is the load seen by the current generator I2:

$$R_x = \frac{ro1 \, (R1 + ro2)}{R1 + (1 + (gm2 + gmb)) \, ro1 \, ro2} \quad (5.27)$$

Therefore:

$$v_n^2 \approx v_{n1}^2 + \frac{1}{25}v_{n4}^2 + \frac{1}{25}v_{n6}^2 \approx v_{n1}^2$$

It is required that current mirrors work in strong inversion for better matching and lower noise. In strong inversion the transconductance is given by:

$$gm = \sqrt{2 \, \mu \, C_{ox} \, \frac{W}{L} \, I_d} \quad (5.28)$$

where μ is the charge carrier mobility, C_{ox} the gate oxide per unit area and I_d the drain current. In the chosen technology PMOS transistors have a mobility ~ 6 times lower than their NMOS counterparts. Therefore, especially with low bias current, it is easier to drive them in strong inversion even with moderate channel lengths. The aspect ratios chosen for M4 and M6 (6/4 and 6/2 respectively) guarantees compact area and good matching performance while making their contribution to the overall system noise negligible. These values allow also to increase in the bias current by at least a factor 2 without compromising the operating points of the amplifier.

The chip will be produced in a p-substrate process, therefore the standard NMOS transistors are fabricated directly on the chip substrate. The process offers also the possibility of implementing the NMOS devices in dedicated wells (triple well option) as sketched in Figure 5.6. In this case a deep n-well is fabricated in which the p-well hosting the NMOS transistors is put. This solution allows a good shielding of the transistor from the common chip substrate at the expense of an increased area. In a mixed mode design it is very important to protect the sensitives nodes from the potential interference of the digital switching circuitry. The triple well solution has hence been used for the input transistor M1 and its cascode device M2.

Source follower

The CSA output stage is a source follower, which is employed as a voltage buffer to drive the loading capacitances at the input of the feedback stages and of the comparator. Since the source follower has an asymmetric rise and fall times and the polarity of the injected charge determines the direction of the leading edge, a NMOS source follower is needed for n-type sensors and a PMOS one for p-type sensors,

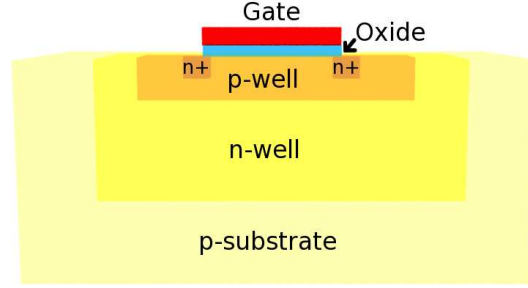


Figure 5.6: Triple well graphical representation (not in scale).

hence maximizing the output swing. The selection between the two is done via the `select_pol` status bit. In p-type configuration `select_pol` is low, M9 is switched on and M12 is switched off. In n-type configuration `select_pol` is high, M12 is switched on and M9 is switched off. This stage is biased with a nominal current of $2\ \mu\text{A}$. The output DC voltage is regulated by the baseline holder. The value of the baseline voltage V_{ref} must be set according to the sensor type. Typical values are 300 mV for n-type sensors and 700 mV for p-type ones. The buffers have the source and bulk short circuited in order to suppress the bulk effect that would decrease their voltage gain. For this reason transistor M11 in Figure 5.3 is implemented as a triple well device in order to decouple its bulk from the global substrate and to allow the source-bulk connection.

5.2.2 Baseline holder

As a first step the solution presented in [93] has been considered for the leakage compensation. Shown in Figure 5.7, this architecture provides also the discharging current generation. A similar circuit has been designed in the current technology with a filtering capacitance of 10 pF in order to evaluate by simulations its leakage compensation capabilities. This filtering capacitance requires an area of $\sim 500\ \mu\text{m}^2$ and it is close to the maximum value that could be implemented in the pixel cell. In case of a leakage current of 10 nA the resulting compression of the ToT signal is 13%. Increasing the leakage current to 50 nA, the compression increases to 38%. The baseline shift is $\sim 6.1\ \text{mV}$. On the basis of these results, a different approach employing a dual feedback loop has been preferred for the ToPix architecture.

The baseline holder is a specific feedback network that controls the DC output of the preamplifier, making it insensitive to the sensor leakage current. The output of the CSA is sensed by a differential pair and compared to the preset reference voltage. The resulting error signal is used to drive a PMOS, which acts as a voltage controlled current source and injects the compensation current into the input node.

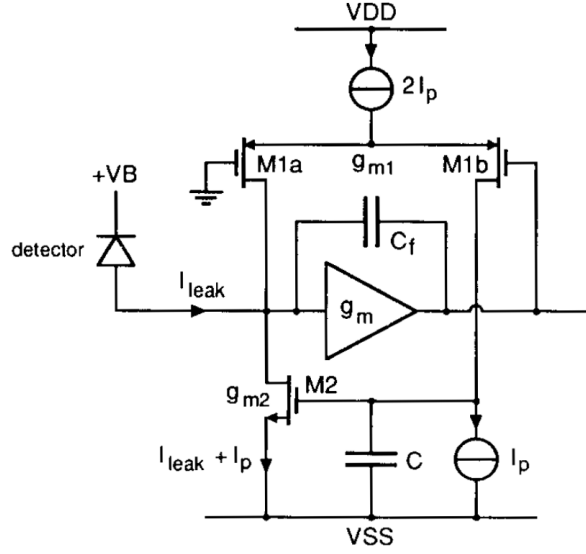


Figure 5.7: CSA with a feedback circuitry which automatically compensates for the detector leakage current proposed in [93].

Before being presented to the current source the error signal is filtered by a compact RC stage. This circuit principle was already explored in ToPix_2 but, as described in chapter 4, the test results have shown a non fully satisfactory performance. For this reason this stage has been completely redesigned. Figure 5.8 shows the schematic of the new baseline holder and Table 5.2 report the transistors size. The input differential pair is a telescopic cascode that senses and amplifies the difference between the reference voltage and the CSA output. A nominal bias current of 150 nA is mirrored by the cascode current mirror M9-M10.

The telescopic cascode load has to be designed in order to reduce the voltage drop thus making room for a larger output voltage swing. For this reason in strong inversion the low voltage cascode load (Fig. 5.9(b)) is normally used. The gates of transistors M7 and M8 are connected to the drain of M5. The gate of transistors M5 and M6 are biased with a dedicated line. The resulting voltage drop is:

$$V_{drop} = V_{gs7} = V_{ds7} + V_{ds5} \quad (5.29)$$

A minimum value of V_{gs} is hence required to guarantee an adequate headroom to the circuit. This may become problematic in weak inversion where the V_{gs} is below the threshold voltage. In this design, given the low bias current, the transistors work in weak inversion and the V_{gs} is ~ 150 mV, while the minimum $V_{ds,sat}$ is ~ 50 mV. Therefore if the topology of Figure 5.9(b) is used a headroom of only 50 mV would

result. The voltage drop in a standard cascode load (fig. 5.9(a)) is:

$$V_{drop} = V_{gs7} + V_{gs5} \quad (5.30)$$

However given the low values of V_{gs} in weak inversion the use of this topology becomes again convenient. In addition this configuration has the advantage that it does not require an extra bias line.

Transistor M11 limits the voltage swing at the differential stage output, thereby reducing potential kick back effects towards the preamplifier. A couple of CMOS switches is used to present the correct signals to the gate of M1 and M2. In p-type configuration the CSA output signal is negative and it is presented on the gate of M1, while the reference voltage is presented to the gate of M2. Vice versa, in n-type configuration the CSA output signal is positive and it is presented to the gate of M2, while the reference voltage is presented to the gate of M1. Since the gate of M1 is the non-inverting input and the gate of M2 is the inverting one, in both cases the voltage at the output of the differential pair moves downwards from its DC operating point. This is not true if a parasitic signal with a polarity opposite to the one expected from the sensor and for which the chip is programmed is presented to the CSA input. The problem originating from this fact will be addressed later in the discussion of the RC filter.

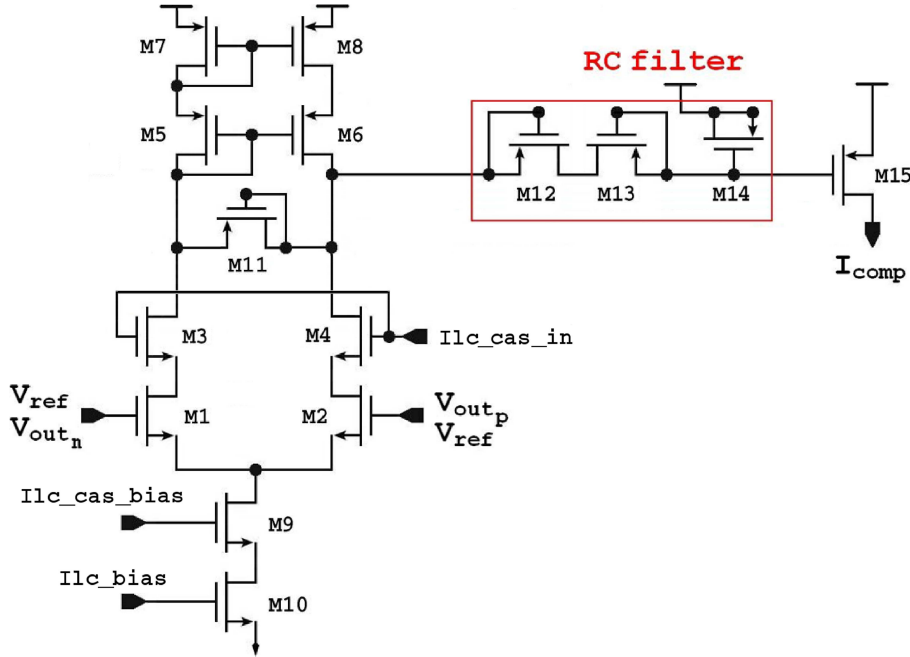


Figure 5.8: Simplified scheme of the baseline holder.

	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14
W [μm]	2×5	2×5	5	5	5	5	5	5	5	5	0.25	0.5	0.5	2×1
L [μm]	1	1	0.5	0.5	0.5	0.5	1	1	0.5	1	1	1	10	12

Table 5.2: Baseline holder transistors size.

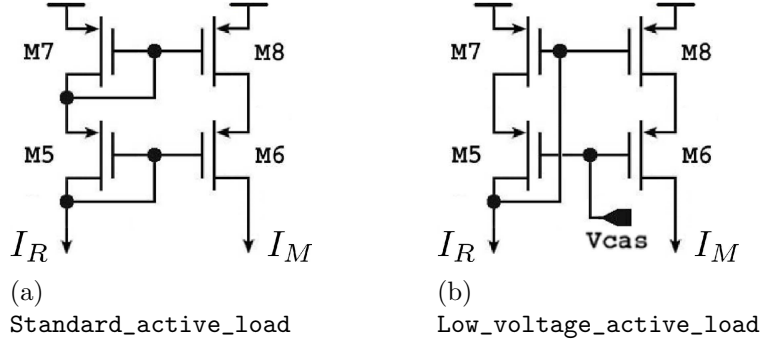


Figure 5.9: Telescopic cascode active load topologies.

The Time over Threshold can be very long, reaching 10 μs for a 50 fC input. Therefore, a very low cutoff frequency is necessary in order to prevent these long signals from being clipped by the leakage compensation circuit, otherwise a nonlinearity will be introduced. This is not desirable since the resulting compression curve might depend on the leakage current value. For an adequate circuit performance the cutoff frequency f_{bhl} defined by equation (5.31) should be as low as 10 Hz.

$$f_{bhl} = \frac{1}{2 \pi R_{bhf} C_{bhf}} \quad (5.31)$$

Assuming a value of the filtering capacitance of 1 pF a resistance in excess of 10 G Ω is needed. Such a large equivalent resistance is implemented with two PMOS devices with gate and source short circuited [84]. These devices exhibit a high equivalent resistance in the order of $10^{10} \Omega$ when $V_{ds} < 0$. When $V_{ds} > 0$ the role of the drain and of the source is exchanged; the device becomes a normally diode connected transistor and its equivalent resistance drops. In ToPix_2 the equivalent resistance was implemented with only M13. As discussed in section 4.2.3, the output signal of the differential pair is negative only when the CSA receives an input current pulse of the same polarity expected for the sensor signal. However for test purposes or for cross talk management the filter has to handle either polarity. When an opposite polarity signal is presented the differential pair output rises, consequently M13 source and drain are exchanged thus lowering its equivalent resistance. It has been experimentally verified that this leads to very long settling times. Therefore in ToPix_3 an additional PMOS (M12) has been implemented. When the output of

the differential pair has a positive swing M12 exhibits a large equivalent resistance, allowing proper filtering of the ToT signal. For normal signals when the voltage swing is negative, M12 behaves as a diode connected transistor and its impedance becomes negligible with respect to one of M13.

Figure 5.10 shows the response of the ToT stage to a cross talk signal with and without transistor M12. The input signal is a triangular shaped voltage pulse with a peak of 200 mV, a rise time of 5 ns and a fall time of 5 μ s. A cross coupling capacitance of 50 fF has been assumed. The rising edge injects a current of the same polarity of the sensor, therefore the injected charge is correctly processed. The falling edge injects a constant current of opposite polarity, hence the CSA output goes below the baseline. In the configuration with M12 the cutoff frequency remains unaltered and the discharging takes place through the constant current discharging feedback circuit. In the configuration without M12, the baseline restorer cutoff frequency rises and the signal is compensated. At $t = 5 \mu$ s, the cross talk current signal ends. In the configuration with M12, the feedback filter remains unaltered and it holds correctly the baseline. In the configuration without M12 the filter cutoff frequency drops and the baseline is restored only after $\sim 200 \mu$ s with a series of oscillations.

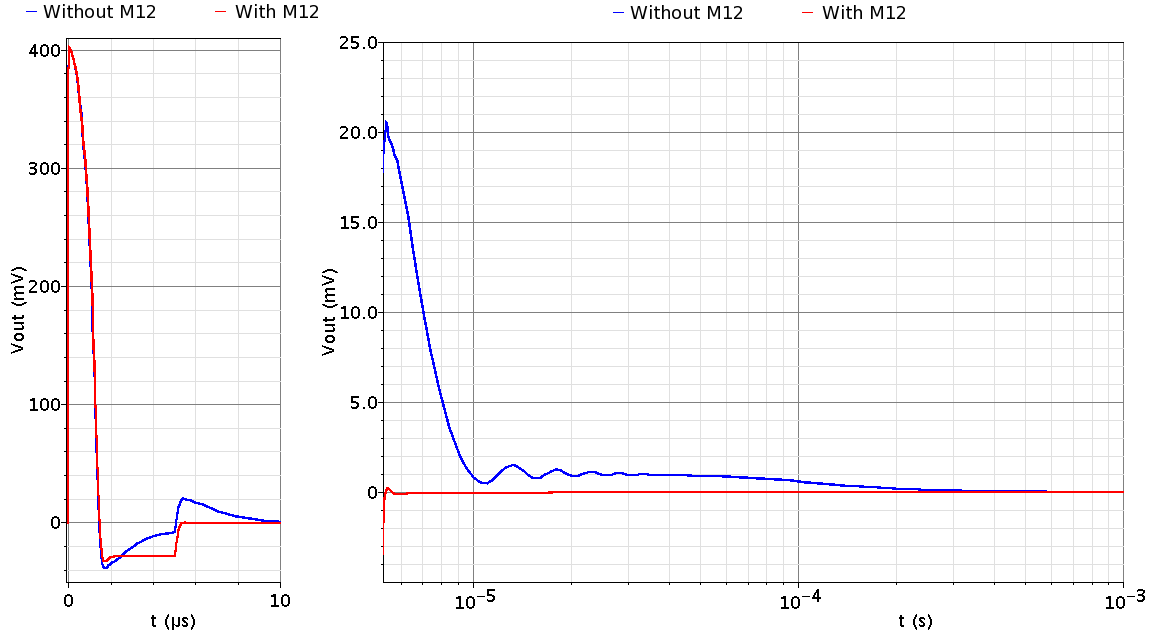


Figure 5.10: Response for a cross talk signal with and without transistor M12.

M12 and M13 have to be optimized carefully in order to provide an equivalent

resistance which lies in an acceptable range ($\sim 500\text{ M}\Omega - 10\text{ G}\Omega$) for all the possible working conditions. Thanks to the high value of the equivalent resistance, a capacitance in the order of $\sim 5\text{ pF}$ is sufficient to achieve a filter cut off frequency in the order of 10 Hz . The filtering capacitor is implemented through MOS devices exploiting the gate oxide (M14), and it occupies an area of $172\text{ }\mu\text{m}^2$.

Figure 5.11 shows the bandwidth reduction due to the RC filter. The bandwidth of the differential pair is 200 kHz , thanks to the RC filtering it is possible to limit the action of the filtering stage for frequencies below 10 Hz thus preserving the ToT signals.

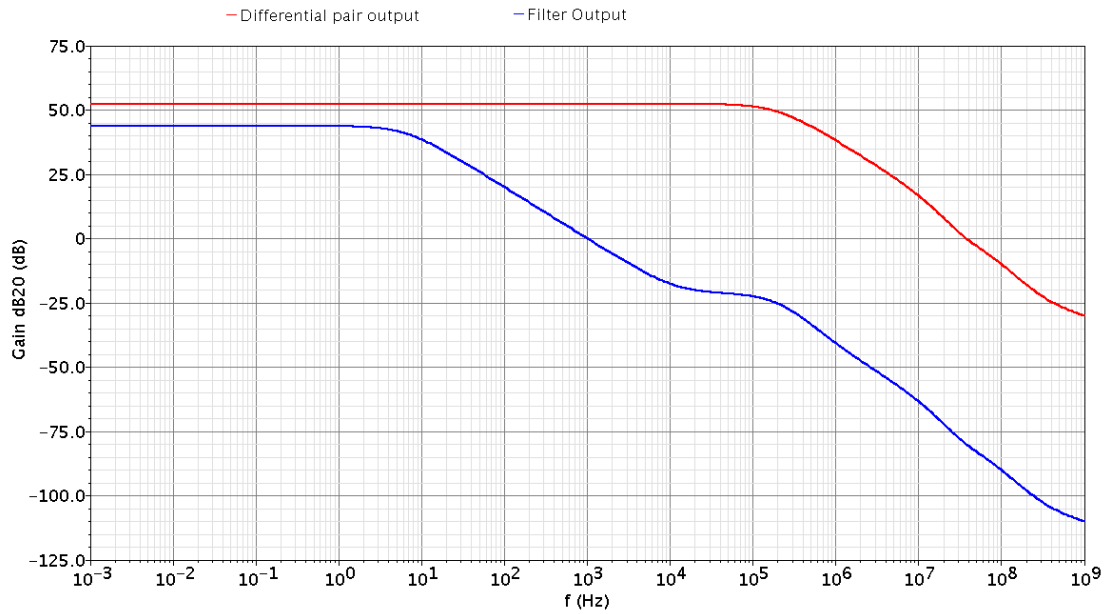


Figure 5.11: Magnitude plot of an AC signal presented on differential pair input. Output of the differential pair before the RC filter, and after the RC filtering.

Temperature variations, which affect the threshold voltage, may significantly alter the equivalent resistance. Therefore extensive temperature simulations have been performed in order to verify the temperature dependence of the filter cut off frequency f_{bhl} . Even if a precise value of the resistor is not important, too small values can lead to signal non linearity and frequency instability. Too large resistors, on the other hand, would compromise the accuracy of the compensation, pushing the circuit towards an open-loop condition. The results of simulations performed in a $10^\circ\text{C} - 90^\circ\text{C}$ temperature range are show in Table 5.3. The threshold of M12 and M13 decreases with temperature, thus reducing the equivalent filter resistance

and consequently increasing the cutoff frequency f_{bhl} . The f_{bhl} increment from $T = 10^\circ C$ to $T = 90^\circ C$, is of one order of magnitude and does not represent an issue.

T [$^\circ C$]	f_{bhl} [Hz]	V_{th} [mV]
10	8	254
30	19	238
50	39	223
70	73	207
90	124	124

Table 5.3: RC filter cut off frequency and M13 threshold voltage at different temperatures.

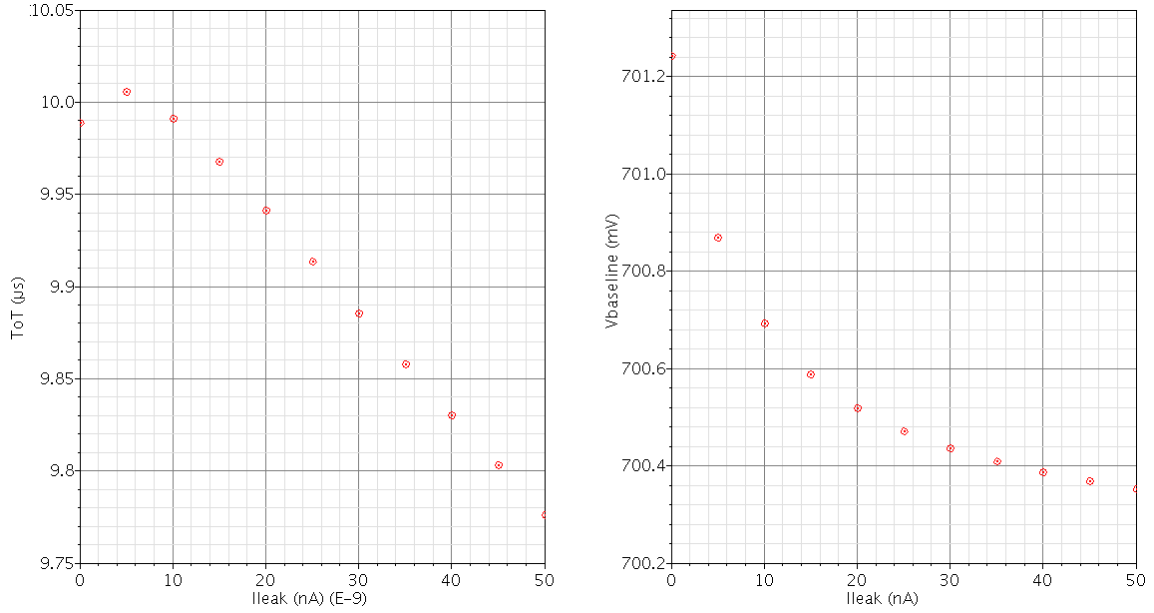


Figure 5.12: Simulation of the ToT compression for an input charge of 50 fC and baseline shift due to the leakage.

To quantify the performance of the leakage compensation system two parameters have been studied varying the leakage current (I_{leak}). The first one is the compression of the ToT signal, the latter is the baseline shift (Figure 5.12). As a test charge 50 fC has been chosen, which is the largest charge expected to be measured. For $I_{leak} \leq 10$ nA the ToT variation is negligible ($< 0.1\%$), for larger leakage current values there is a quite linear compression of ~ 5.5 ns/nA. For a leakage current of 50 nA the compression is of the order of 2%. The baseline shifting is below 1 mV and

it is negligible also for large leakage current values. These performances are fully adequate for the application.

5.2.3 Constant feedback current generator

The constant current feedback generator is a network that provides the CSA discharging current [70]. Figure 5.13 shows its working principle. The discharge current is provided by a differential pair, connected at the input node, biased with a nominal current $2 I_{fb}$. A second current generator forces the I_{fb} current from the input node to the ground. The three cases of interest are:

- When the feedback capacitance C_f is not charged, the differential pair is perfectly balanced. Therefore a current I_{fb} flows to the ground in each branch.
- In p-type configuration when C_f is charged M1 is switched off and a current of $2 I_{fb}$ flows through M2. The second current generator injects a negative current at the input node equal to I_{fb} . Therefore the net current available to discharge the capacitance is I_{fb} .
- In n-type configuration when C_f is charged M1 is switched on and the $2 I_{fb}$ current flows in the first branch. In this case half bias current flows in the input node and half flows to the ground.

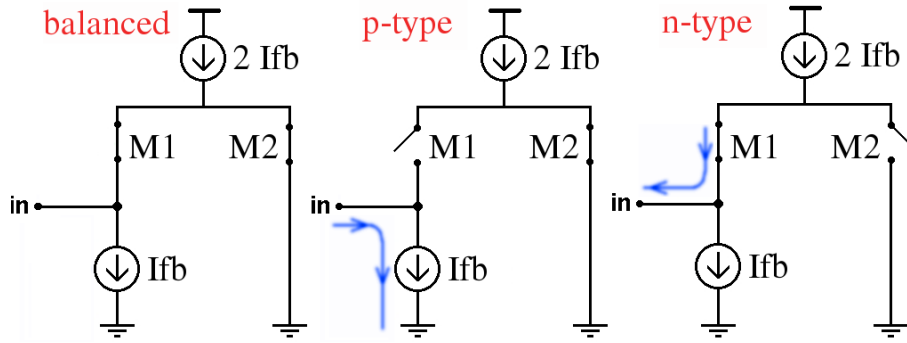


Figure 5.13: Working principle of the Constant Feedback Current Generator. The blue line shows the path of the discharging current.

Figure 5.14 shows the schematic view of this stage. The CSA output signal is presented to the gate of M2, while M1 receives the baseline reference voltage. With a p-type sensor, V_{out} will have a negative polarity, steering all the current from M1 to M2. In this case the current in M3 is used to recharge the feed-back capacitor. With n-type sensors, V_{out} will be positive, steering the current from M2 to M1.

M1 will have an excess current that will discharge the feedback capacitor. At the equilibrium this stage provides an equivalent small signal feed-back resistance of $6.7 \text{ M}\Omega$ with $I_{fb} = 5 \text{ nA}$ (see equation (5.6)).

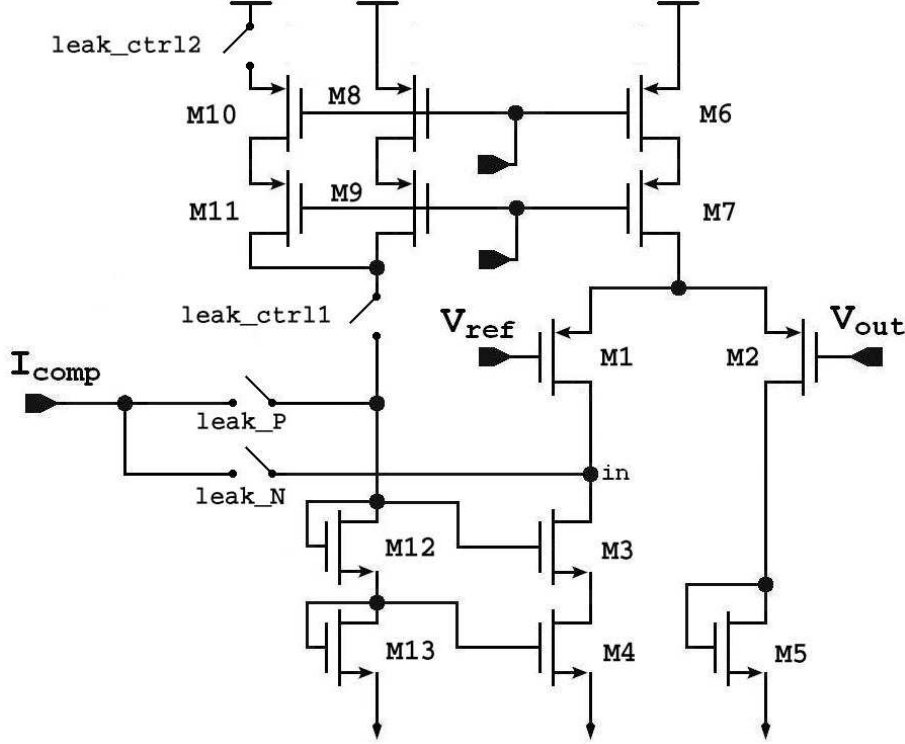


Figure 5.14: Schematic of the constant feedback current generator.

	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13
W [μm]	5×1	5×1	2	4	1.5	2×0.3	2	0.3	2	0.3	2	2	4
L [μm]	0.5	0.5	5	1	5	5	0.5	5	0.5	2	0.5	1	5

Table 5.4: Current feedback generator transistors size.

Table 5.4 reports the transistors size. A good matching of M1 and M2 is essential to reduce the baseline dispersion among different channels. In fact if M2 and M1 are not equal the current that flows in M1 and M2 is different. Hence the baseline holder gives an additional current (positive or negative) to balance the differential pair thus shifting the baseline. For this reason they have been designed with a large multiplicity. The final size of the M1 and M2 have been chosen after detailed simulations in order to evaluate the propagation delay due to the input capacitive load and increase the loop stability. Transistors M6 and M7 implements a cascode

current source that generates the 2 I_{fb} bias current. Transistor M5 is the load of the second branch. Transistors M3 and M4 acts as current source (I_{fb}) mirroring the current in M12 and M13.

This stage provides also the injection of the leakage compensation current at the input node. Using four switches it is possible to change the topology of the circuit in order to choose the polarity of the current to be compensated:

- p-type sensor leakage current flows from the sensor to the input node, therefore the compensation system has to create an equal current flow from the input to the ground. Both `leak_ctrl1` and `leak_ctrl2` are switched off, while `leak_P` has to be switched on. When no leakage current is present the compensation current I_{comp} is equal to I_{fb} . In this way the differential pair is perfectly balanced. When a leakage current is present and additional current equal to the leakage flows through M13 ($I_{comp} = I_{leak} + I_{fb}$) and it is mirrored in M4.
- n-type sensor leakage current flows from the input node to the sensor, therefore the compensation system generates an equal current flow from Vdd to the input node. In this case the compensation current is directly injected at the input node. In standard configuration both `leak_ctrl1` and `leak_ctrl2` are switched on, as well as `leak_N`. Since the width of M8 and M10 is the half of M6, in this branch flows a current equal to 2 I_{fb} which biases M4. Therefore when no leakage current is present I_{comp} injects a current equal to I_{dis} for the proper bias of the differential pair at equilibrium. When leakage current is present $I_{comp} = I_{leak} + I_{fb}$. For test purposes the leakage compensation circuit can be excluded from the feedback. In this case both `leak_N` and `leak_ctrl2` must be switched off.

ToT linear range limitation

As calculated in chapter 3, when the CSA saturates the input node rises (p-type case) or drops (n-type case). In both cases when the transistors connected at the input node are pushed out from the saturation region, the discharging current increases leading in a compression of the ToT signal. This phenomena depends on the input capacitance and the input DC voltage. Since the input DC voltage is at ~ 200 mV, assuming a detector capacitance of 200 fF, for a n-type sensor the compression occurs from $Q_{in} \approx 90$ fC. For a p-type sensor a much larger current (~ 200 fC) could be collected on the input capacitance while ensuring the proper bias of the constant current feedback.

5.2.4 Comparator

The comparator has a folded cascode input stage, and two CMOS inverters in cascade as driver in order to have a fast transition between the two logic states. Since the comparator performance in ToPix_2 was satisfactory, the transistor level implementation has not been changed. However the layout has been redesigned in order to fit in the available cell area. The large input transistors M1 and M2, with $W/L = 25 \mu\text{m}/0.5 \mu\text{m}$, have been designed in a common centroid layout splitting each transistor in 16 parts. The circuit is biased by $I_{\text{bias_d}}$, with a nominal value of 500 nA, the overall current dissipated by the comparator is 10 times larger. Figure 5.15 shows the transistor level implementation. The comparator gives a high level output when $V_{\text{in}2} > V_{\text{in}1}$. Therefore in n-type configuration, where the CSA output is positive, in1 is connected to the comparator reference voltage and the CSA output to in2. In p-type configuration where the CSA output is negative the signals are exchanged using CMOS switches.

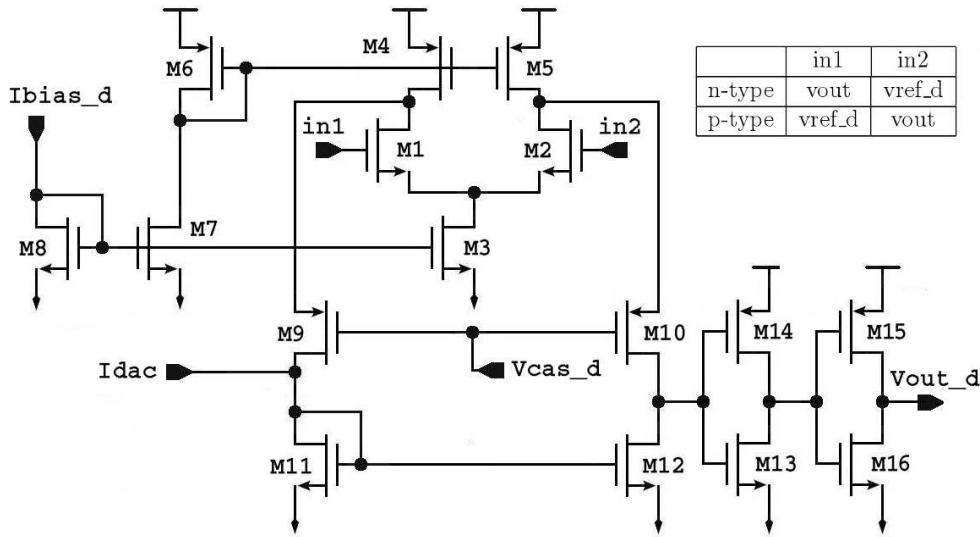


Figure 5.15: Comparator schematic.

DAC current source

Since $V_{\text{ref_d}}$ is common to all pixels, in order to mitigate the threshold dispersion a local five bit DAC is added in each pixel, to allow a fine tuning of the threshold on a pixel by pixel basis. The DAC can sink or source current to a low impedance node, the drain of M9 and M11 in Figure 5.15. The I_{dac} value is regulated by a 5

bit DAC, the first bit (select_range) determines the current polarity and 4 bits are employed to set the current value:

$$I_{dac} = I_{bit} (-1)^{select_range} \sum_{i=0}^3 B_i 2^i \quad (5.32)$$

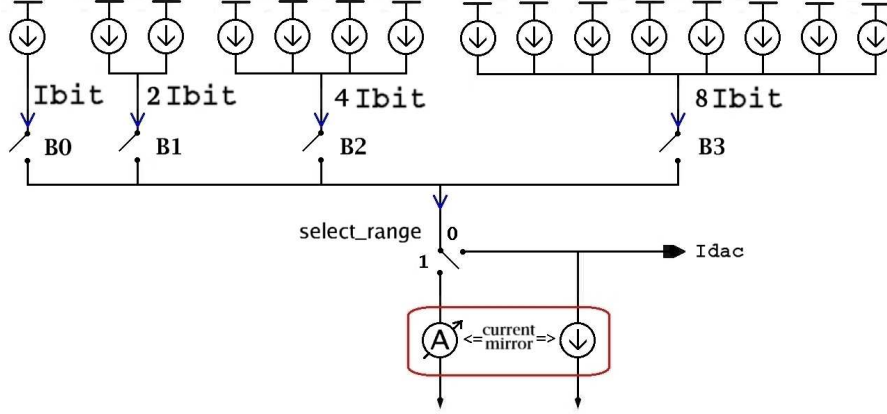


Figure 5.16: Simplified model of the 5 bit DAC.

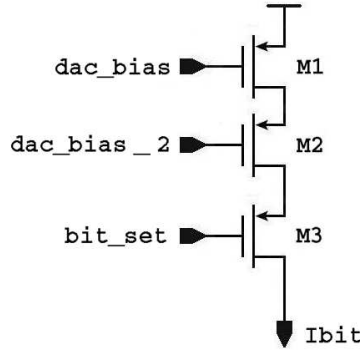


Figure 5.17: Comparator with 5 bit DAC

A simplified scheme of the DAC is shown in Figure 5.16. The DAC is made of 16 I_{bit} current generators regulated by switches. If $select_range = 1$, the current is mirrored in order to sink the current from the comparator. For simplicity the switches are represented in common for each group of I_{bit} current generators. Each of the bit B_0 , B_1 , B_2 , B_3 controls a switch (M_3 in Fig. 5.17) that activates the

relative current generator. Figure 5.17 shows the schematic of the Ibit current generator. Transistors M1 and M2 implements a cascoded current mirror, while M3 on the basis of the bit_set can turn on the Ibit current generator. The cell bias can be changed thus varying the DAC full scale range.

5.2.5 Clipping circuit

A clipping circuit has been designed in order to protect the front-end when a large charge is presented at the input node, thus avoiding long dead times. The front-end requires to measure charges up to 50 fC, so larger charges have to be discharged with an extra current. The clipping circuit exploits the fact that the input node rises (p-type case) when the CSA saturates. Connecting the input node at the gate and drain of a low power NMOS and its source at ground, it is possible to clip the voltage signals larger than the threshold voltage of the transistor ($V_{th} \approx 600$ mV). Post layout simulations in the corner cases have been performed to characterize the device. Figure 5.18 shows the $Q_{in} - ToT$ relationship when the clipping circuit is activated, the circuit has a linear response up to 50 fC then the ToT saturates at $\sim 16.5 \mu s$. The clipping circuit can be enabled or disabled by a dedicated configuration bit.

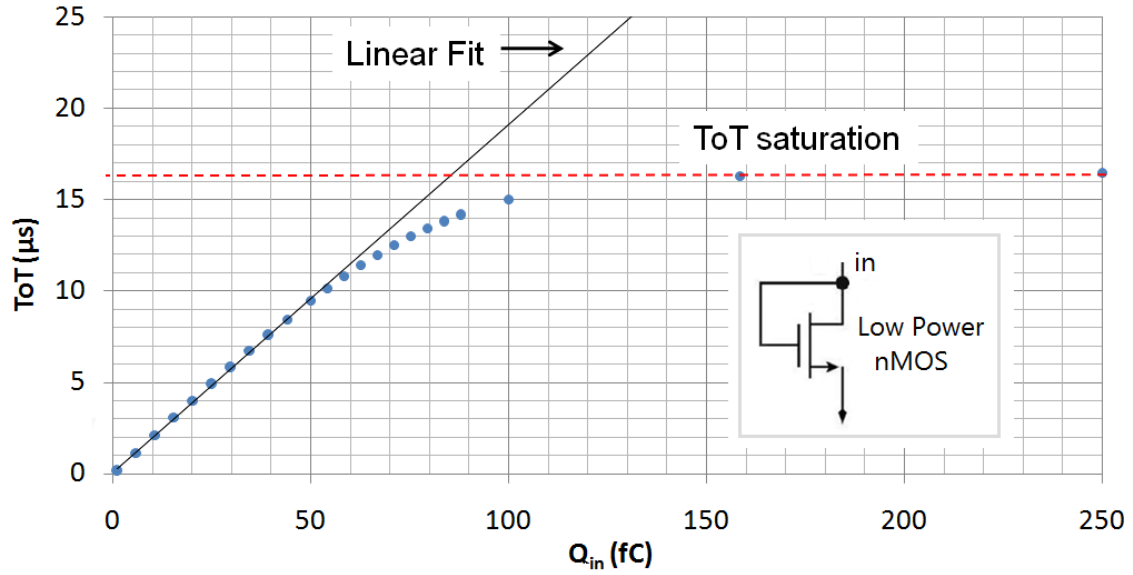


Figure 5.18: ToT saturation with clipping circuit

5.2.6 Calibration circuit

The calibration circuit allows to inject a current pulse (I_{inj}) into the preamplifier to test the circuit response. The calibration circuit in ToPix_2 has a bug that does not allow to inject the calibration signal simultaneously in more than one pixel. Moreover it was difficult to estimate precisely the value of the injected charge. For this reason a new calibration circuit has been designed.

Figure 5.19 shows the schematic of the calibration circuit. The TestP signal is a CMOS differential signal common to all the pixels. The positive line is TestPH and the negative one is TestPL. TestP_EN is a status bit of the pixel configuration register, and activates the injection subcircuit. Table 5.5 shows the status of the two CMOS switches on the basis of the test control signals. When TestP_EN = 0 Switch1 is always off and Switch2 is always on, hence $V_c = 0$ V. With TestP_EN=1 and TestP low (TestPH=0, TestPL=1) only Switch2 is on, hence $V_c = 0$ V. Commuting TestP high (TestPH=1, TestPL=0) only Switch1 is on, hence $V_c = cal_level$. In order to avoid ambiguities, when TestP_EN = 1 and TestPH = TestPL both switches are turned off. A delay is implemented with a CMOS switch always turned on in order to compensate the inverter delay. Therefore when TestP_EN = 1, with a positive TestP step it is possible to inject a positive pulse current into the input node, and with a negative step a negative pulse current is injected. The absolute value of the injected charge is:

$$Q_{cal} = \int_{t_0}^{t_1} i(t) dt = C_{cal} \int_0^{cal_level} dV_c = C_{cal} \cdot cal_level \quad (5.33)$$

The nominal value of the capacitance is $C_{cal} = 36$ fF, due to process and mismatch variations a spread within 10% is expected, thus limiting to this level the accuracy of the injection charge. The maximum voltage level for cal_level is 1.2 V, therefore the maximum value of the charge that can be injected with this system is 43.2 fC.

TestP_EN	TestPL	TestPH	Switch1	Switch2
0	0	0	Off	On
0	0	1	Off	On
0	1	0	Off	On
0	1	1	Off	On
1	0	0	Off	Off
1	0	1	On	Off
1	1	0	Off	On
1	1	1	Off	Off

Table 5.5: State of the CMOS switches. Logic level 0 is at 0 V, logic level 1 is at 1.2 V.

If one wants to send a double current pulse of the same polarity it is possible to

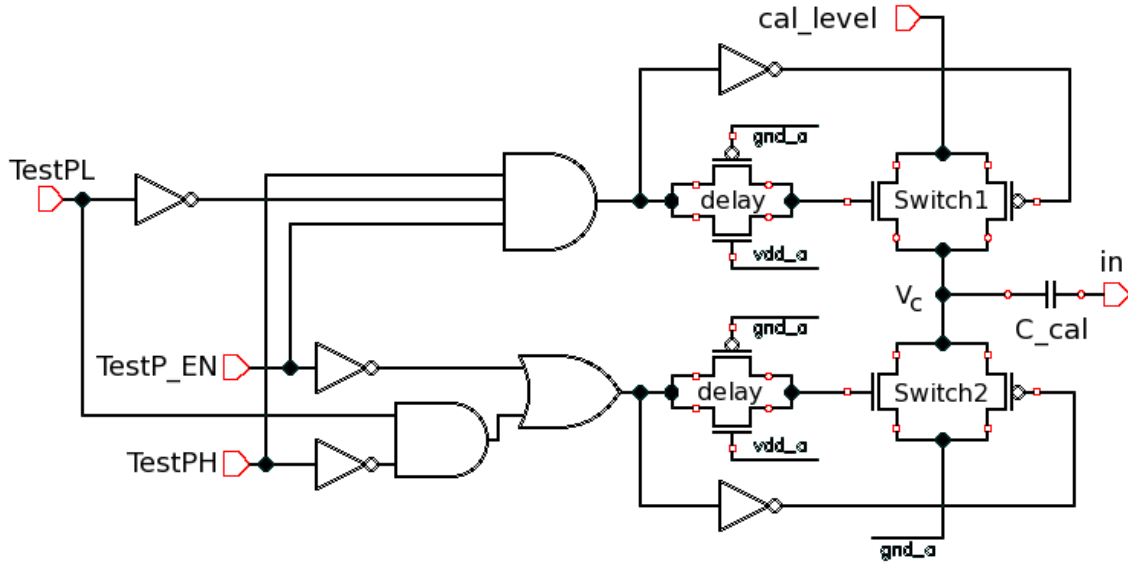


Figure 5.19: Calibration circuit schematic.

present a double step voltage on the calibration capacitance by setting TestP_EN = 1, TestPL = 0, TestPH=1, and sending the double step signal on cal_level.

5.2.7 Analog cell layout

The Analog Cell Layout is implemented in an area of $50\ \mu\text{m} \times 100\ \mu\text{m}$. The floorplan has been optimized in order to place the comparator between the most sensible analog blocks (preamplifier, constant current feedback and baseline holder) and the digital cell. In Figure 5.20 the different components are labeled as following:

- 1 Calibration circuit;
- 2 Charge Sensitive Amplifier;
- 3 Constant Current Feedback;
- 4 Baseline Holder;
- 5 5 bit DAC for the threshold correction;
- 6 Comparator;
- 7 Large charge cut-off circuit;
- 8 Bump bonding pad with octagonal shape.

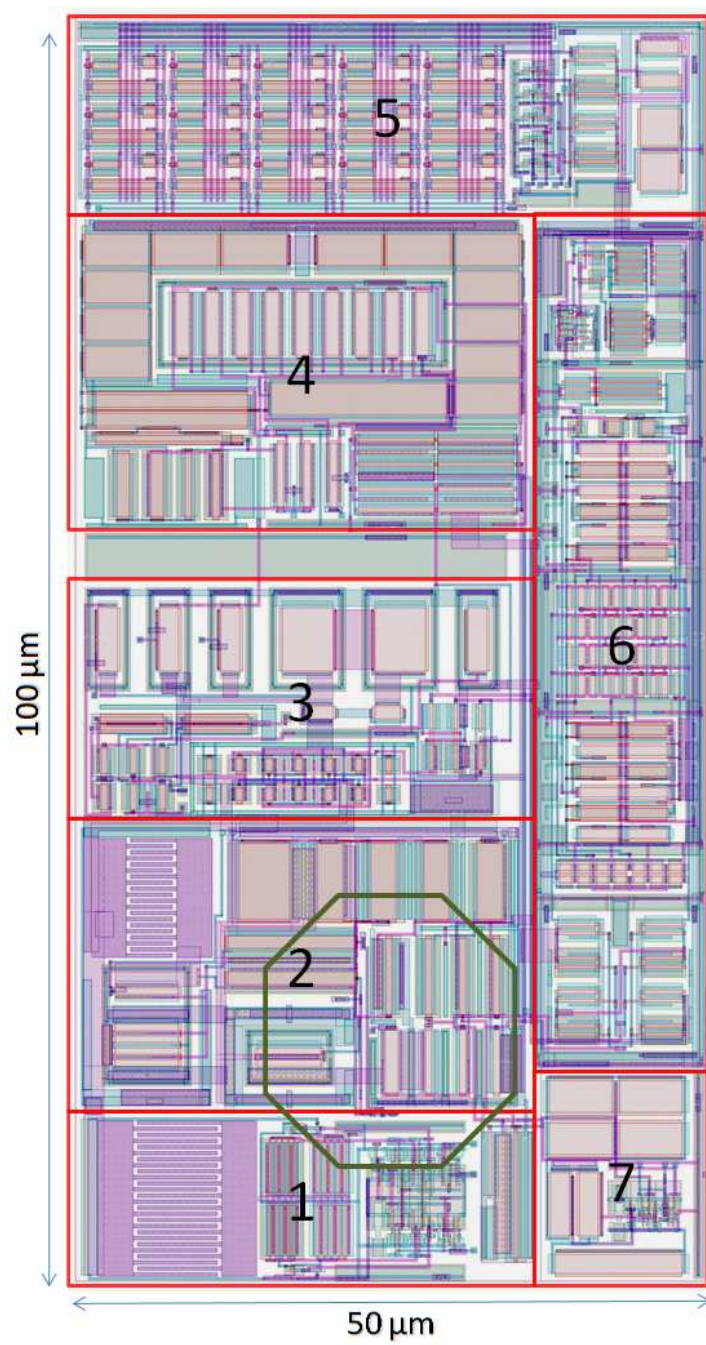


Figure 5.20: Analog Cell Layout

The bias lines are propagated vertically, low levels metal are employed for the bias line and high levels metal for the power supply lines. In order to avoid the propagation of spurious signals through the power supply, 7 separate lines have been employed. The input cascode stage of the CSA has a dedicated ground (gnd_pre). The triple well transistors of the input stage have vdd_pre as shield. The leakage compensation stage bias is given by vdd_ilc. The comparator has a dedicated supply line (vdd_d) and a dedicated ground (gnd_d). All the other analog blocks are supplied by vdd_a and gnd_a.

5.3 Post-layout simulations

Extensive post-layout simulations have been performed in order to validate the circuit performances. It is important to evaluate the contribution of the parasitic components which are non negligible given the small feature size of this technology. The reliability of the circuit has been tested with a parametric simulation with a sweep on the process corners. Other parametric simulations have been performed for different temperatures in the 0°C - 100°C range and leakage currents from 0 nA to 50 nA. A selection of the simulation results is reported in the following.

Comparison with the two-poles model

To verify the validity of the two poles approximation discussed in section 5.1 a fit (in equation (5.34)) has been made on simulated data of the complete ToT stage. This fit is performed only for comparison purposes since it does not represent a fully accurate model. The real transfer function of the system depends on a large number of poles and zeros.

$$v_{out}(t) = \frac{Q_{in}}{C_f} \frac{e^{-t/\tau_f} - e^{-t/\tau_r}}{1 - \tau_r/\tau_f} \quad (5.34)$$

The peak value has been normalized to 1 and the simulation data has been fitted with the function in equation 5.4. Figure 5.21 shows the fit result, the parameters of the fit are:

- $\tau_r = 43.5 \pm 0.5$ ns
- $\tau_f = 94.4 \pm 0.8$ ns

The fit results are in reasonable agreement with the parameters calculated with the simplified model, where $\tau_r \approx 50$ ns and $\tau_f \approx 80$ ns. The deviation of the simulation data from the fit ϵ is normalized to the peak value V_p . The maximum deviation is ~ 0.15 , and the falling edge ($t < t_p$) is approximated with a maximum deviation of ± 0.05 . The residue function (V_p/ϵ) shows the time dependence of the signal

components that are neglected in the two poles model. The peaking time of the fit function is moved forward of ~ 10 ns.

In the two poles model the value of the τ_r is greater than the one that would be expected from the simple formula defined in equation (5.3). This can be explained with the fact that in this model the output buffer is supposed to have zero output impedance. This is not the case in reality. For power reasons the source follower implementing the buffer is biased with a low current (typically $2 \mu\text{A}$), hence its output impedance is not negligible and introduces a further pole. If this it is taken into account the resulting value of gm_1 is $80 \mu\text{S}$, which is in fairly good agreement with the experimental one.

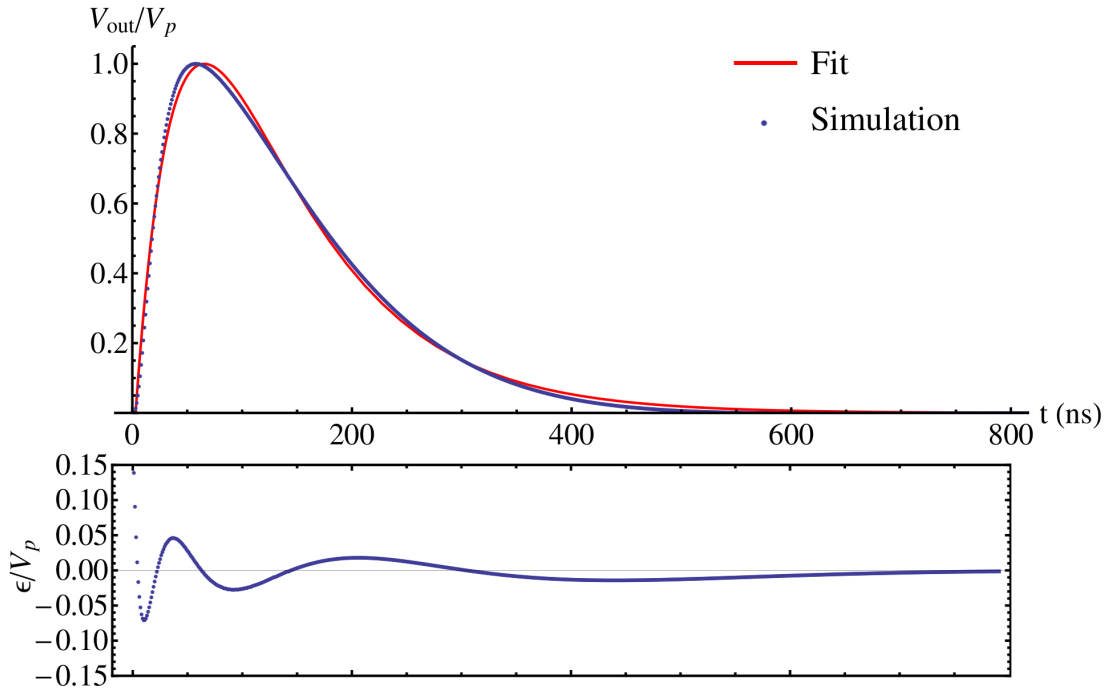


Figure 5.21: Comparison of the signal with two poles transfer function and the simulation output.

Process corners

The foundry provides a model that describes the process variation of the chip fabrication. The simulation software allows to change the physical properties of the silicon by relating directly to the effects on the working performance of a particular device. The process corner is expressed in units of standard deviation. The

parameter c_c for positive values increases the capacitances value, c_n increases the current and speed for NMOS devices, c_p increases the current and speed for PMOS devices. The characterization of the circuit at the different corner processes is important to evaluate the chip to chip variation and permits to optimize the design for a higher yield. Intensive simulations have been performed varying the corner parameters from -3σ to 3σ , thus taking into account the process variations with a confidence level of 99.73%.

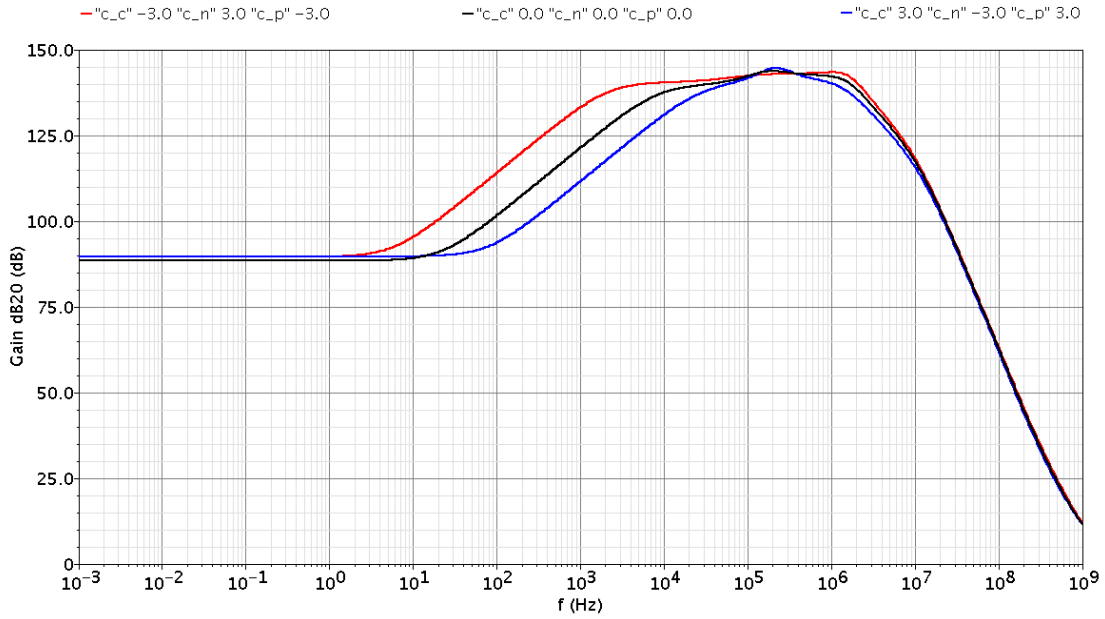


Figure 5.22: AC magnitude plot of v_{out}/i_{in} for standard process and the two worst process corners.

The baseline shift due to the process variation is below 0.5 mV. A such low value is negligible. In order to estimate the variation of the analog gain simulation on the capacitance corner have been performed. A value of 76.4 ± 5.1 mV/fC with 1σ confidence level results. Figure 5.22 shows the AC magnitude plot of v_{out}/i_{in} for the standard process and the two worst cases. The ToT stage behaves as a bandpass filter. At small frequencies the DC gain is reduced at ~ 90 dB by the baseline holder in order to compensate the leakage current. The pole $f_{bhl} = 18$ Hz of the RC filter in the feedback loop introduces a zero in the transfer function. The gain is between 40 kHz and 1.4 MHz is ~ 140 dB. At higher frequencies the gain drops due to the pole introduced by the CSA ($1/\tau_r$) and the current feedback network ($1/\tau_f$). The two worst process cases have been taken into account. When $c_p = -3$, the PMOS transistor threshold voltage is higher than the standard process case, thus transistors

M12 and M13 of the loop filter exhibits a larger equivalent resistance, lowering f_{bhl} . Vice versa when $c_p = 3$ f_{bhl} increases. In the $c_n = 3$ corner the transconductance of the CSA input NMOS transistors is increased, therefore the CSA bandwidth increases to 2.3 MHz. Vice versa $c_n = -3$ the bandwidth decreases to 1.9 MHz.

Noise

A set of 100 transient noise simulations have been performed injecting a test charge of 1 fC in p-type sensor configuration, with zero leakage current. Figure 5.23 shows the output of the CSA with the signal superimposed. The output voltage rms noise is $V_{noise,rms} = 1.90$ mV, with a signal to noise ratio of 45. The Equivalent Noise Charge is $155 e^-$. The main contribution comes from the input transistor of the CSA (M1 in Figure 5.3) which generates the 29.9% of the total noise. The second noise contributor is the transistor M4 of the current feedback circuit (Fig. 5.14) whose white current noise flows directly in the input node. Its output noise contribution is 0.83 mV which is the 16.5% of the overall. The noise rate at zero threshold is $f_{n0} \approx 16$ MHz. Using equation (3.37) the resulting noise rate with a threshold $V_{th} = 6 V_{noise,rms}$ is ~ 0.25 Hz.

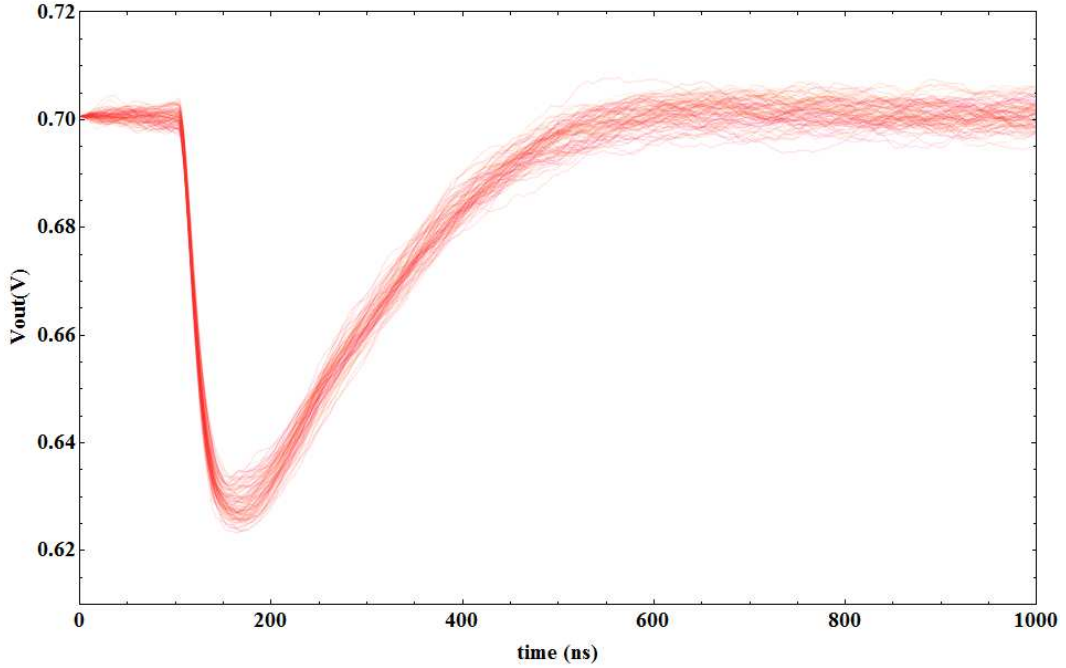


Figure 5.23: Transient Noise Simulation of the pixel readout cell.

Ileak nA	M1 CSA		M4 IFB		M6 IFB		M13 IFB		$V_{out,rms}$ mV	ENC e^-
	mV	%	mV	%	mV	%	mV	%		
0	1.04	29.9	0.83	19.1	0.56	8.8	0.3	3.0	1.90	155
10	1.04	16.5	1.63	40.9	0.57	5.0	0.8	10.5	2.56	209

Table 5.6: Noise contribution.

With a leakage current of 10 nA, the ENC increases to $209 e^-$. This is due to the fact that the leakage compensation current flows through transistor M4. This results in an increment of its transconductance thus increasing the white current noise spectral density. In fact the equivalent output noise of the CSA input transistor remains unchanged (1.04 mV), while the noise contribution of M4 increases by a factor of 2 and contributes to the 40.9% of the total noise. The output noise spectral density with a leakage current of 10 nA is shown in Figure 5.24.

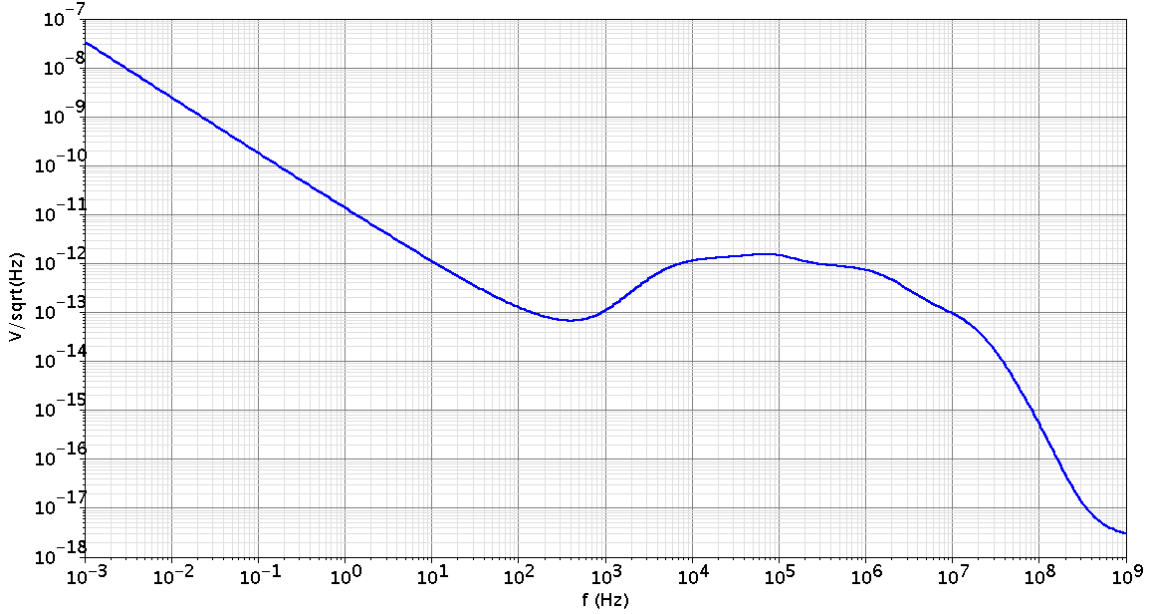


Figure 5.24: Output noise spectral density with a leakage current of 10 nA.

Power supply gain

Two simulations have been performed in order to evaluate the power supply gain with no additional filtering capacitances. In the first simulation an AC voltage signal has been presented on the power supply. The resulting output frequency

spectrum is shown in Figure 5.25. For frequencies below 200 Hz the power supply gain is -63.5 dB. A positive gain is reached around 1 MHz. The dependency of the discharging current on the power supply has been evaluated as well. It is important because a power supply ripple can alter the discharging current thus increasing the digitization uncertainty. If the power supply ripple frequency is larger than the ToT signal frequency, it can introduce a random ToT variation. If the power supply ripple frequency is lower than the ToT signal frequency, it can introduce a ToT variation that depends on the time relationship between the signal and the ripple. From equation (3.30) it is possible to define the condition when the current uncertainty has the same contribution of the ToT digitization resolution:

$$\left(\frac{\sigma_{I_{dis}}}{I_{dis}}\right)^2 = \left(\frac{\sigma_{ToT}}{ToT}\right)^2 \quad (5.35)$$

The maximum ToT signal which is expected to be measured is of 10 μ s, which corresponds to an input charge of 50 fC. The ToT resolution is $\sigma_{ToT} = \sqrt{2}\sigma_t = 2.62$ ns. Therefore with a nominal current I_{dis} the condition (5.35) is verified for a discharging current with a rms spread of $\sigma_{I_{dis}} = 1.3$ pA. The discharging current gain referred to the power supply is 86.6 pA/V. Hence the condition (5.35) is verified for a power supply rms ripple of 15 mV.

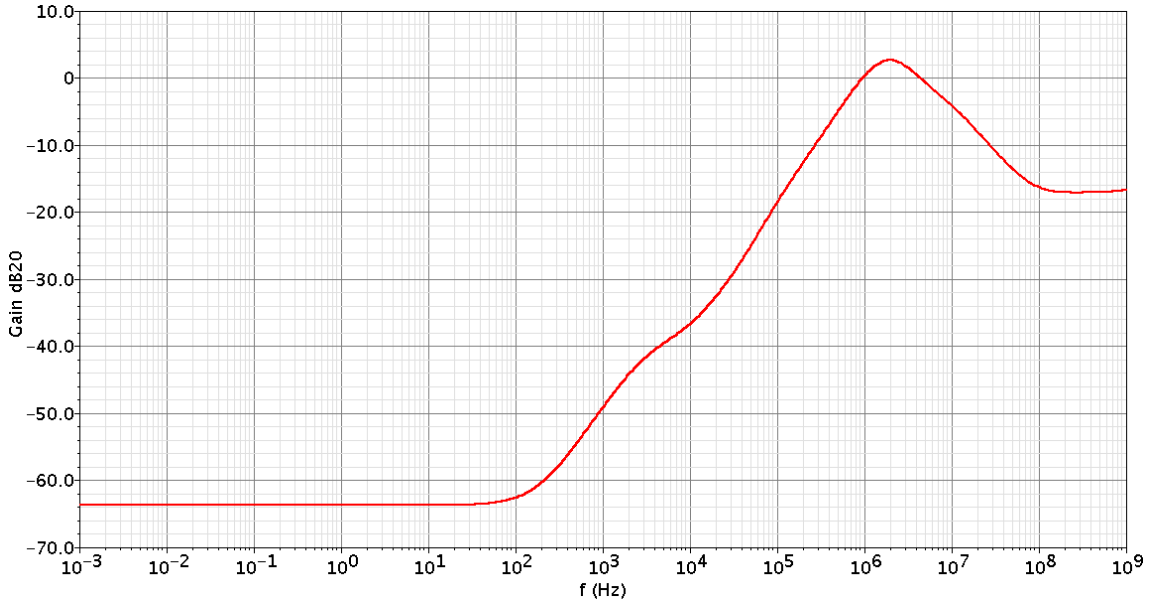


Figure 5.25: Power supply AC gain.

In the second simulation a voltage pulse with an amplitude of 50 mV, rising time of 1 ns, width of 500 ns and falling time of 1 ns has been presented on the power

supply. The resulting output signal has an amplitude of 17.2 mV and the baseline is correctly restored.

Linearity

Linearity simulations have been performed with two different comparator threshold values: 15 mV and 30 mV above the baseline voltage. The ToT - Q_{in} relationship has been fitted with a linear fit:

$$ToT = a Q_{in} + b \quad (5.36)$$

where a is the inverse of the discharging current and b is the fit offset.

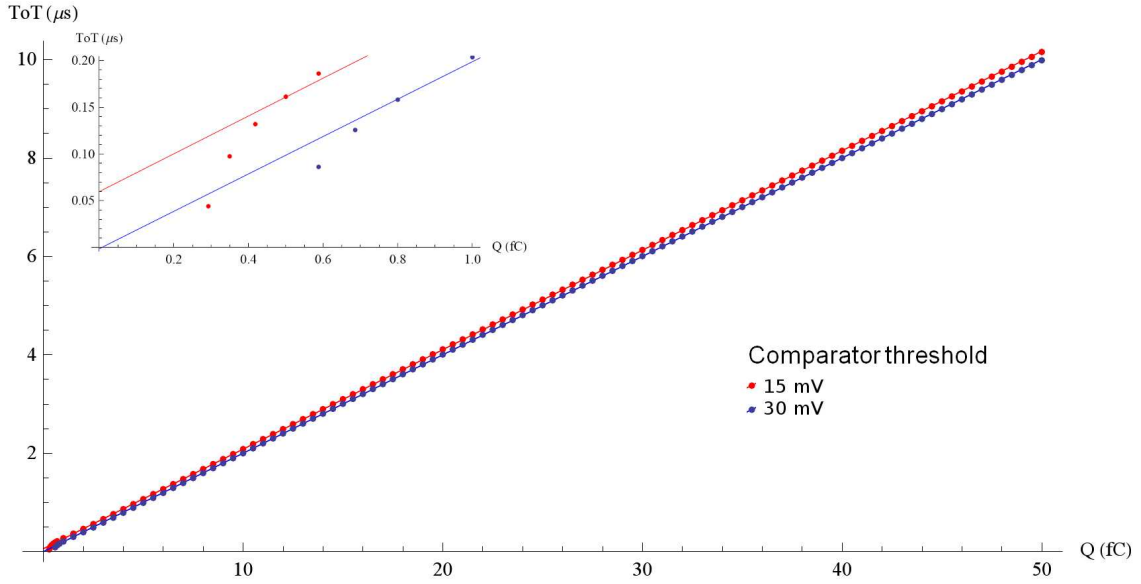


Figure 5.26: Linearity simulations.

With the threshold at 30 mV the fit parameters are: $a = (200.022 \pm 0.046)$ ns/fC and $b = (-1.365 \pm 1.34)$ ns. The fit residuals rms has been computed in order to characterize the goodness of the linear approximation for input charges larger than 1 fC. In this case the rms value of the differences between the simulation data and the linear fit is 6.2 ns, which equivalent to $\sim 187 e^-$. The minimum charge that triggers the comparator commutation is ~ 0.6 fC. The fit parameters of the linearity measurement with the threshold at 15 mV are: $a = (202.179 \pm 0.065)$ ns/fC and $b = (59.734 \pm 1.86)$ ns. In this case it is possible to detect charges down to ~ 0.3 fC. The rms value of the fit residuals for $Q_{in} > 1$ fC is 5.9 ns. In both cases the fit slope is close to 200 ns/fC, which is the inverse of the nominal discharging

current of 5 nA. Figure 5.26 shows the linearity simulation results and the two linear fits.

Mismatch

The channel to channel variation of the ToT gain and baseline voltage has been estimated through a Monte Carlo mismatch simulation with 300 runs. The results are shown in Figure 5.27. A test charge of 5 fC has been employed. The baseline peak to peak variation is ~ 12 mV, and it can be compensated by the comparator threshold DAC. The relative ToT channel to channel rms variation is $\sigma_{ToT}/ToT \approx 7\%$. The ToT variation is due to the mismatch between the input transistors of the current feedback circuit (M1 and M2 in Figure 5.14). Hence, with the nominal discharging current $I_{fb} = 5$ nA, the channel to channel rms I_{fb} spread is 350 pA.

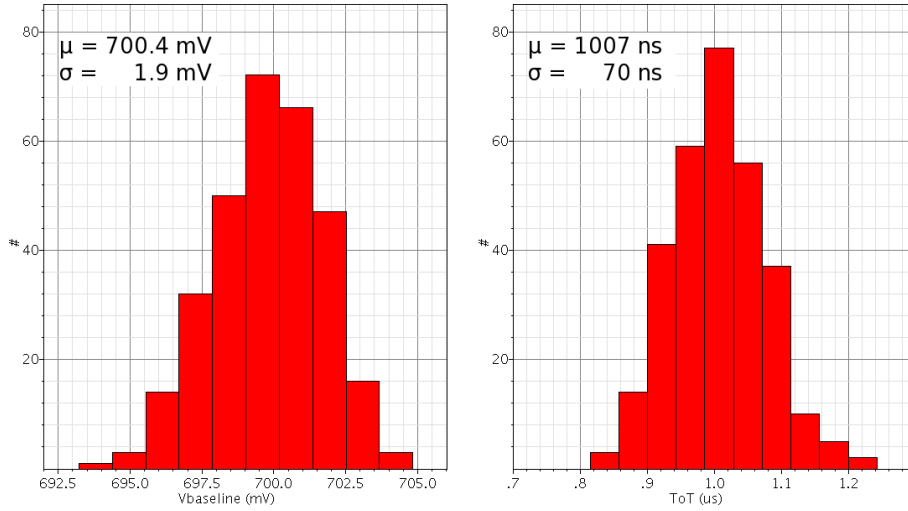


Figure 5.27: Monte Carlo mismatch simulation.

Full pixel cell simulation

A set of transient simulations has been performed on the complete pixel cell including the digital logic. In order to reduce the cross talk between the analog and digital part, the source and substrate of the NMOS transistors in the digital part have been splitted. Figure 5.28 shows the interference of the digital circuit activity on the analog output signal. The time between the pulses is equal to the clock period (~ 6.4 ns). The average peak of the disturbance is below 0.5 V, which is ~ 4 times smaller than the electronic noise, hence it is fully tolerable. A ToT linearity

simulation has been successfully performed reconstructing the ToT value from the difference of the values stored in the leading edge and trailing edge registers.

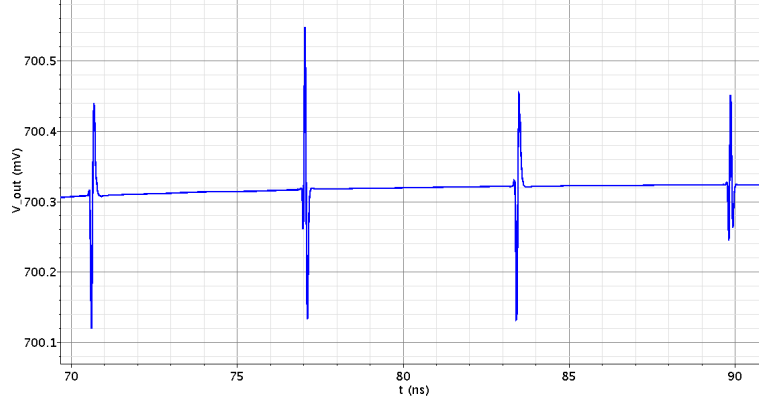


Figure 5.28: Post layout simulation, interference of the digital circuit activity on the analog output signal.

Simulation summary

A summary of the front end analog performances is reported in Table 5.7. The simulation results meet the requirements. The front end is able to manage pulses of either polarities without additional dead time. The calibration circuit bug has been corrected, thus allowing the simultaneous charge injection in different cells.

Analog Gain		76.4 ± 5.1 mV/fC
ToT gain	$v_{th} = 30$ mV	(200.022 ± 0.046) ns/fC
	$v_{th} = 15$ mV	(202.179 ± 0.065) ns/fC
ToT fit residuals rms ($Q_{in} = 1fC - 50fC$)		6 ns
Channel to channel ToT spread		7%
Channel to channel baseline spread		1.9 mV
Minimum charge	$v_{th} = 15$ mV	0.3 fC
	$v_{th} = 30$ mV	0.6 fC
Equivalent noise charge	I _{leak} =0 nA	155 e^-
	I _{leak} =10 nA	209 e^-
ToT compression	I _{leak} =0 nA	< 0.01%
	I _{leak} =50 nA	< 2%
Power consumption		15 μ W
Front end area		100 μ m \times 50 μ m

Table 5.7: Summary of the simulation results.

5.4 ASIC layout

ToPix_3 has been submitted to the foundry for fabrication in February 2011. It is designed in a CMOS 0.13 μm technology with a power supply of 1.2 V. The ASIC size is 4.5 mm \times 4 mm and the layout is shown in Figure 5.29. The chip contains 640 pixels, arranged in four 128-cells columns and four 32-cells columns (bottom part of the ASIC layout). As in ToPix_2 the columns are folded in order to test the signal transmission over long lines. The basic readout unit is the double column which is in its final form, as well the column readout logic and signal buffering system (top right part of the layout). The chip data transmission and configuration logic is still in a prototype version. The 26 analog pads are listed in Table 5.8. They are located in the chip top left side. The remaining pads are employed by the digital section, for a total number of 61 pads.

Pin name	Type	Description
vdd_pre	Shield	Input triple well bias
gnd_pre	Ground	Preamplifier ground
vdd_ilc	Power	Offset compensation circuit power
vdd_a	Power	Analogue power
VcasP1	Ibias	Preamplifier cascode load bias (pMOS, vdd_a)
VcasP2	Ibias	Preamplifier direct cascode bias (pMOS, vdd_a)
Isf	Ibias	Source follower bias (pMOS, nMOS)
Ilc_cas_bias	Ibias	Loop filter bias (nMOS, gnd_a)
Ilc_cas_in	Vbias	Loop filter cascode bias (nMOS, gnd_a)
Ifb_bias	Ibias	Feedback stage bias ($\times 10$) (pMOS, vdd_a)
Ifb_cas	Vbias	Feedback stage cascode bias (pMOS, vdd_a)
Vref	Vbias	Analogue baseline reference voltage
gnd_a	Ground	Analogue ground
vdd_d	Power	Digital power (analogue section)
dac_bias_2	Ibias	DAC bias (pMOS, vdd_d)
Ibias_d	Ibias	Comparator bias ($\times 10$) (nMOS, gnd_d)
Vref_d	Vbias	Comparator reference voltage (nMOS, gnd_d)
Vcas_d	Vbias	Comparator cascode bias (pMOS, vdd_d)
cal_level	Vref	Calibration voltage for test pulse (CREF = 36 fF)
gnd_d	Ground	Digital ground, analog section

Table 5.8: ToPix_3 analog pad list.

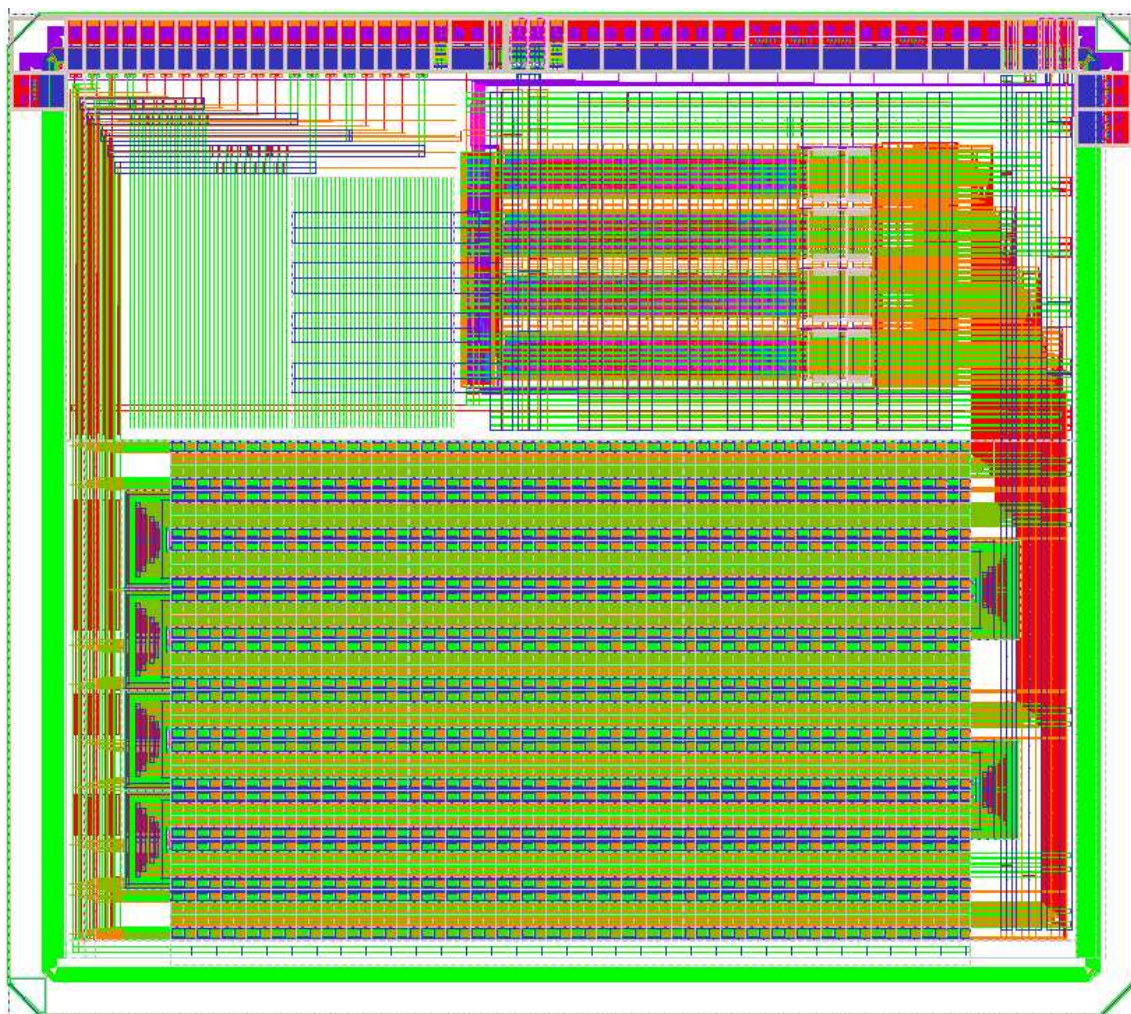


Figure 5.29: ToPix_3 layout.

Summary

This work has been carried out in the context of the research and development activity for the design of the $\overline{\text{P}}\text{ANDA}$ (antiProton ANnihilation at DArmstadt) Micro Vertex Detector (MVD). $\overline{\text{P}}\text{ANDA}$ is an experiment planned at the future international Facility for Antiproton and Ion Research (FAIR) in Darmstadt, Germany. The general purpose $\overline{\text{P}}\text{ANDA}$ detector will study antiproton-proton and antiproton-nucleus reactions in a fixed target setup with an antiproton beam of unprecedented luminosity ($2 \times 10^{32} \frac{1}{\text{cm}^2 \text{s}}$) and momentum resolution ($\delta p/p \sim 10^{-5}$). Its physics program includes the spectroscopy of charmonium states and investigation of open-charm production, the search of gluballs and hybrids, the study of the behavior of hadrons in nuclear matter, and precise γ ray spectroscopy of hypernuclei.

The MVD is located in the innermost part of the experimental apparatus. It has to provide a precise tracking of all charged particles and perform a measurement of the energy loss per unit path-length (dE/dx) giving an additional input for particle identification. Hybrid pixels sensors equips the detection layers in the region close to the interaction point where a high event rate is expected. A dedicated research and development activity is ongoing for the realization of custom hybrid pixel sensors with epitaxial sensors ($100 \mu\text{m}$ thickness). A detailed CAD model has been employed to perform simulations to evaluate the MVD spatial coverage, radiation length, hit rate and spatial resolution. The results are used to define the readout electronics requirements.

The pixel readout ASIC has to provide for every hit a simultaneous position, time and energy loss measurement. In order to guarantee the reliability of the system, only digital information can be transmitted outside the pixel cell. A pixel size of $100 \mu\text{m} \times 100 \mu\text{m}$ has been chosen in order to combine good spatial resolution with an adequate space for the implementation of the readout electronics and digital logic in each cell. A maximum hit rate of $\sim 10^3 \text{ s}^{-1}$ over a single cell has been estimated. For a Minimum Ionizing Particle (MIP) in a $100 \mu\text{m}$ epitaxial sensor an ionization charge of $\sim 1 \text{ fC}$ is expected. A large number of low-momentum particles are foreseen. Since they will lose more energy in the sensor, for particle identification purposes the measurement of ionization charges up to 50 fC is required. A low power consumption allows to reduce the material budget (e.g. cooling and power

supply). Given the high pixel density (10^4 cm^{-2}), a limit of $15 \mu\text{W}$ has been put on the power consumption of the analog cell. The noise level is mainly limited by the input transistor thermal noise and an Equivalent Noise Charge of ~ 200 electrons is a good trade off between power consumption and minimum detectable charge. A sensor leakage current compensation up to 50 nA is required. A time resolution $< 10 \text{ ns}$ allows to tag correctly the events from a collision rate of $2 \cdot 10^7 \text{ s}^{-1}$. Given the close position of the MVD to the interaction point and the high event rate, the radiation hardness is a fundamental parameter for the system reliability. The required tolerance is of 10 Mrad for a Total Ionizing Dose (TID) and for a non ionizing particles fluence of $5.13 \cdot 10^{14} \text{ n}_{[1 \text{ MeV}_{\text{eq}}]}/\text{cm}^2$. These values are calculated for 10 years of data taking with a 50% duty cycle.

In the PANDA experiment the readout system has to continuously digitize the detector data (trigger-less) in order to run the experiment at a high rate. In addition, the high track density, low material budget and custom cell size have led to the choice of a custom solution for the front-end chip, named ToPix. A CMOS $0.13 \mu\text{m}$ technology has been chosen for the ASIC production. The pixel readout architecture is based on the Time over Threshold technique which makes a low power charge digitization possible. This approach has been selected due to its well-known capability of providing linear measurements also when the main amplifier is saturated. This is particularly important since the circuit has to work with a power supply of 1.2 V . The feed-back capacitor of a charge sensitive amplifier is discharged by a constant current source. When the leading and trailing edges of the CSA output signal cross a preset threshold, the corresponding timestamp value is stored by the pixel control logic in the leading-edge and trailing-edge registers. The value in the leading-edge register gives the particle hit timing and the difference between the two registers gives the ToT information which is proportional to the input charge. The ToPix floorplan foresees a matrix of 116×110 pixel readout cells with a size of $100 \mu\text{m} \times 100 \mu\text{m}$, thus covering a 1.276 cm^2 active area. The basic functional block is the double column which in the final version will be made of 116×2 pixels. These pixels shares the same buses and control lines. Each double column is controlled by a peripheral logic which can read and write the configuration and read the event data stored in the pixel registers. The master clock frequency which supplies the timestamp is at 155.52 MHz . Finally the data are multiplexed on two 311.04 Mbit/s serializers by a data transmission logic.

A three step approach has been chosen for the ASIC fabrication in order to reduce the risks and contain the costs. In the first step two reduced scale prototypes have been designed in order to explore mostly the pixel architecture. They were fabricated in Multi Project Wafer (MPW) runs and tested both for electrical functionality and radiation hardness. ToPix_1, fabricated in 2006, is the first prototype aimed at identifying the critical points in the analog readout. ToPix_2, fabricated in 2008, implements a complete readout cell with analog and digital circuitry. The

cells are arranged in columns with a simplified version of the peripheral logic. Radiation damage tests have shown that this technology has an adequate total dose radiation tolerance even without the employment of the hardness by design transistors. ToPix_2 has been tested also for Single Event Upset (SEU) tolerance of the pixel registers. The DICE (Dual Inter-locked Storage Cell) architecture has been rejected, opting for an architecture based on Triple Modular Redundancy in order to increase the SEU tolerance. The ToPix_2 test results show a good agreement with the specifications. However some issues have been highlighted. The channel to channel variation of the ToT is too high and the precision of the current feed-back had to be improved. The analog gain was not sufficient to guarantee a good linearity for small charge values (~ 4 fC). The baseline restorer cannot handle simultaneously input pulses of either polarity.

The results of these two prototypes provided the starting point for the design of the final pixel cell version which was the focus of the second part of this PhD work. While the overall architecture remained unchanged, all the building blocks were re-implemented from scratch. An additional challenge in the design is introduced by the fact that the analog parts had to be reduced by 35% ($50 \mu\text{m} \times 100 \mu\text{m}$) in order to make room for TMR registers in the digital cell. In this design the analog gain has been increased with a nominal feedback capacitance of 12 fF, which is the half of the one in ToPix_2. In order to guarantee the loop stability the number and size of the transistors in the feedback path have been carefully optimized to reduce the signal propagation delays. The mismatch effects have been minimized achieving a ToT channel-to-channel variation $\frac{\sigma_{ToT}}{ToT}$ of 7%. The rms spread of the baseline is 1.9 mV. The effect of this spread can be easily compensated by tuning the comparator threshold with the 5 bit DAC as in ToPix_2. A more compact baseline holder has been designed. It is able to manage either signal polarity without introducing additional dead time. The calibration circuit bug present in ToPix_2 has been corrected, thus allowing the simultaneous charge injection in different cell. Since for particle identification purposes only the ionization charges up to 50 fC are significant, a cutoff circuit for larger signals has been introduced. A maximum time duration for the ToT signal has been fixed thus reducing the dead time for larger signals. The cutoff circuit can however be disabled if one wants to fully exploit the maximum possible dynamic range. Extensive post layout simulations have been performed in order to validate the circuit performance. It is important to evaluate the contribution of the parasitic components which are non negligible given the small feature size of this technology. The reliability of the circuit has been tested with a parametric simulation with a sweep on the process corners. Other parametric simulations have been performed for different temperatures in the $0^\circ\text{C} - 100^\circ\text{C}$ range and leakage currents from 0 nA to 50 nA. An analog gain of 76.4 ± 5.1 mV/fC results taking into account the process variations. An excellent linearity is achieved in the 1 fC - 50 fC input charge range, with a rms spread from the linear fit of 6 ns. For

lower values the relationship is not linear, however with a comparator threshold voltage above 15 mV from the baseline a minimum charge of 0.3 fC can be detected. This correspond to $\sim \frac{1}{4}$ of a MIP in 100 μm silicon. The Equivalent Noise Charge (ENC) is $155 e^-$ in case of zero leakage. It rises to a value of $209 e^-$ with a leakage of 10 nA. The baseline holder can accommodate a dark current up to 50 nA with a maximum ToT compression of 2%. The power consumption of the analog cell is below 15 μW .

The simulation results are promising and meets the specifications. In February 2011 the Topix_3 prototype with the final version of the pixel cell has been submitted to the foundry for fabrication. Each cell has a pad for bump bonding to sensor. Test with the hybrid sensors will be performed in 2012. Finally the full scale ASIC is expected to be fabricated with a dedicated engineering run in 2013.

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