Integrated Front End Electronics for Cellular Signal Recording Systems Based on Diamond Microelectrode Arrays

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Abstract

This thesis presents a study of an Analog Front End for cellular electrical signal recording systems based on diamond microelectrodes.

The diamond is the most recent material considered for microelectrode implementation. Its surface becomes conductive through the hydrogenation process. It is biocompatible and optically transparent and its noise level is lower than the conventional metal microelectrodes. For this reason it is important to minimize the noise introduced by the electronics employed in the signal processing.

The advent of the microelectrode array (MEA) makes it possible to have hundreds of recording channels. To avoid signal attenuation and minimize noise the preamplifier has to be close to the recording electrodes and if it occupies a small area the number of the channels could be increased.

To comply with noise and space requirements we choose to design an integrate circuit in CMOS AMS $0.35\mu m$ technology.

Particular attention has been focused on the design of a low noise low power preamplifier which has to work under few kilohertz range, cutting the DC component generated at the electrode - electrolyte interface.

A complete processing channel for neural signal recording has been simulated. A total gain of ≈ 2500, with a high pass cutoff frequency of $\approx 0.4Hz$ and a low pass cutoff frequency tunable in the range of $\approx 2kHz - 6kHz$ is achieved. An input referred noise voltage of $2.34\mu V$ is obtained.

A brief summary of the thesis contents is reported in the following:

1. **Introduction**

   Contains a short description of neurons electrical activity and cultured cell recording methods. It introduces the use of MEA as biosensors and gives attention to the diamond as new material for microelectrodes.

2. **Front End Architectures for Neural signal Recording**

   Define the basic specifications of the Front End Architecture and describes some interesting solutions which have been proposed in scientific literature.

3. **Low Noise Low Power Preamplifier**

   Presents a short overview of the simulation environment and discuss the Preamplifier design, reporting the results of the simulations.

4. **Filter stage**

   Describes the design of the filter stage and reports the results of the simulations.

5. **Complete Front End simulations**

   Contains a brief introduction to the Output Buffer and presents the results of the complete AFE simulations.

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Chapter 1

Introduction

The characterization of electrical signal in animal cells is important because it helps scientists to understand how nerves work, and how the brain controls muscle and other physical functions.

Moreover it is possible to implement a cell based Biosensor, a device which employs cultured biological cells as transducer to monitor changes in physiological activity due to environmental threat. Possible applications are pharmaceutical screening, biochemical agents monitoring, drug detection.

The electrical activity of cells consist in a variation of the transmembrane potential, called Action Potential. This potential is due to the alteration of ionic concentrations in cell's cytoplasm and external medium.

This chapter starts with a short description of neurons electrical activity, then it focuses on cultured cell recording methods, analyzing the microelectrode array and modeling the cell-electrode interface.

It is also given a short introduction to the diamond as material for microelectrodes.

1.1 Neuron's electrical activity

1.1.1 Neurons

Neurons are electrically excitable cells in the nervous system that process and transmit information. In vertebrate animals, neurons are the core components of the brain, spinal cord and peripheral nerves.
Neurons are highly specialized for the processing and transmission of cellular signals. Given the diversity of functions performed by neurons in different parts of the nervous system, there is, as expected, a wide variety in the shape, size, and electrochemical properties of neurons.

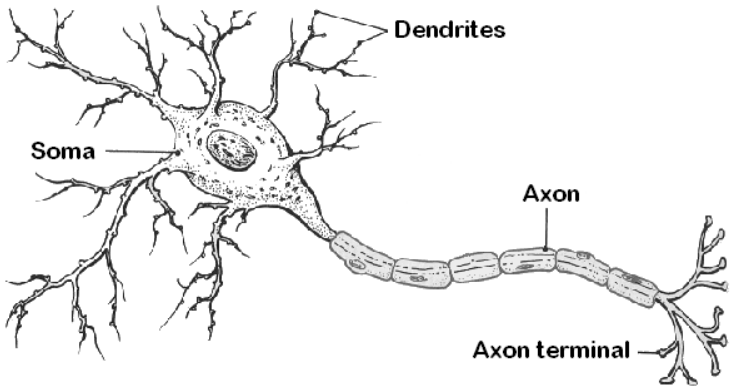

Figure 1.1: A typical neuron

Figure 1.1 shows the neuron's main structural components, which are listed below:

- The cell body, called soma, that contains the nucleus of the cell, and therefore is where most protein synthesis occurs. The nucleus ranges from $4\mu m$ to $25\mu m$ in diameter.
- The dendrites, branching fibers extending from the cell body. These fibers increase the surface area available for receiving incoming information.
- The axon, considerably thicker and longer than the dendrites of a neuron. It

carries information away from the soma to the synaptic sites of other neurons (dendrites and somas), muscles, or glands.

- The axon terminal, a specialized structure at the end of the axon that is used to release neurotransmitter chemicals and communicate with target neurons.

Neurons receive electrical input on the cell body and dendritic tree, and transmit output via the axon.

1.1.2 Cellular Membrane

The cellular membrane is a semipermeable lipid bilayer that covers all parts of the cell and separates fluid inside the cell from fluid outside the cell.
Membranes are constructed by molecules with long hydrophobic fatty chains and a charged hydrophilic head. This molecules arrange themselves into bilayers, by positioning their charged head towards the surrounding water, and their hydrophobic chains towards the inside of the bilayer, defining a non-polar region between two polar ones.
This forms a continuous lipid bilayer (see Figure 1.2), approximately $7nm$ thick, that contains the cellular components .

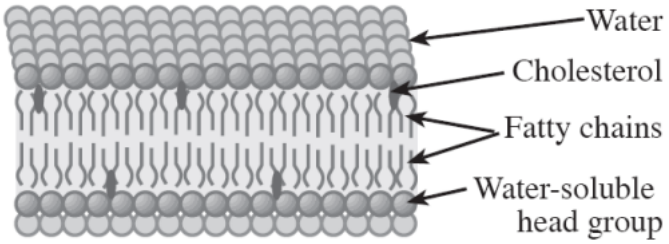

Figure 1.2: Cell membrane [1]

The arrangement of hydrophilic and hydrophobic heads of the lipid bilayer prevents hydrophilic solutes from passively diffusing across the band of hydrophobic tail groups, allowing the cell to control the movement of these substances via transmembrane protein complexes such as pores and gates.

While gases, small uncharged molecules, and water are able to diffuse directly through the membrane, ions and charged and uncharged molecules requires the presence of transmembrane protein.

There are protein that pumps ions across the membrane against their electrochemical gradient, at rate of $10^3 ions/s$. These pumps maintain a low concentration of calcium and sodium inside the cell, and transport Na^+ and K^+ to establish the resting membrane potential.

There are proteins that forms a channel across the membrane in which specific types of ions can move along their electrochemical gradients. These channels can be either always-open, or gated, with the state being determinate by the transmembrane potential. This channel proteins allow $10^8 ions/s$ to pass through the membrane.

Electrical Model of cellular membrane

The electrical model [2] is based upon the equivalent circuit for a patch of cell membrane.

The ionic channels are symbolized through a variable conductance $(g_{Na}, g_K, g_{Ca}, g_{Cl})$ that depends on the state of channel proteins, the voltage generators take account of the ionic potentials at equilibrium $(V_{Na}, V_K, V_{Ca}, V_{Cl})$. The membrane capacitance is expressed by C_m and V_m is the transmembrane potential. The current generator I_{stim} has been added to describe any currents which are externally applied during the course of an experiment.

In Figure 1.3 the electrical model of the cell membrane is shown.

The net current which flows into the cell through these channels has the effect of charging the membrane capacitance, giving the interior of the cell a membrane potential V_m relative to the exterior.

$$C_m \frac{dV_m}{dt} = I_{stim} - [g_{Na}(V_m - V_{Na}) + g_K(V_m - V_K) + g_{Ca}(V_m - V_{Ca}) + g_{Cl}(V_m - V_{Cl})] \quad (1.1)$$

In Hodgkin and Huxley channel conductance control theory are involved two control particles. The first moves out of an inhibitory site when the transmembrane potential reaches a threshold allowing ions to flow though the channel. A second inhibitory particle moves slowly to occupy the inhibitory site and stop the ion flow.

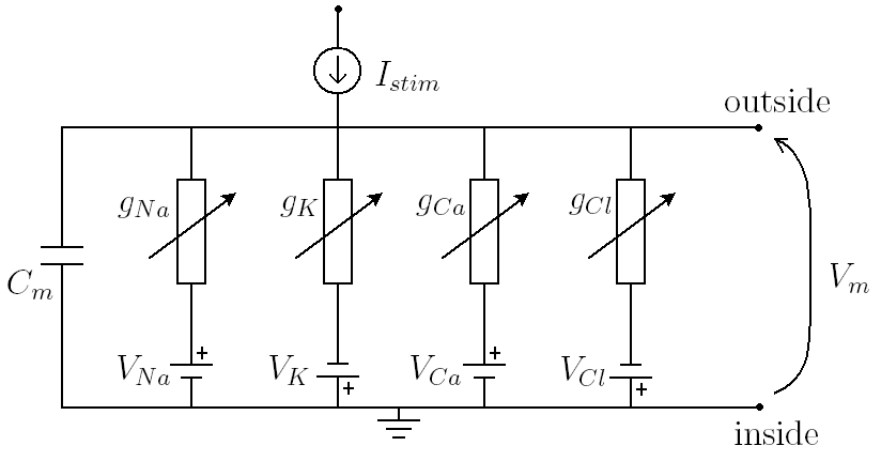

Figure 1.3: Electrical model of cell membrane

These are represented by two variables each governed by a first order differential equation. The sodium and potassium conductance are then expressed:

$$g_{Na}(V_m, t) = g_{Na,max} m^3 h \tag{1.2}$$

$$g_K(V_m, t) = g_{K,max} n^4 \tag{1.3}$$

where m and n are activation coefficient, h is inactivation coefficient. Both activation and inactivation variables are governed by the differential equations:

$$\frac{dx(V_m)}{dt} = \frac{x_\infty(V_m) - x(V_m)}{\tau_x(V_m)} \tag{1.4}$$

$$x(t) = x_\infty(V_m) - (x_\infty(V_m) - x_\infty(0))e^{\frac{-t}{\tau_x}} \tag{1.5}$$

where x stand for the m,n,h coefficients.

The maximum values for the ionic channel conductance [3] are reported below:

$$g_{Na} = 15.0 mS/cm^2$$

$$g_K = 3.2 mS/cm^2$$

$$g_{Ca} = 0.079 mS/cm^2$$

$$g_{Cl} = 0.26 mS/cm^2$$

Figure 1.4 shows the dependence of the time constants (τ_x) and activation parameters (h, n, m) from the membrane potential (V_m).

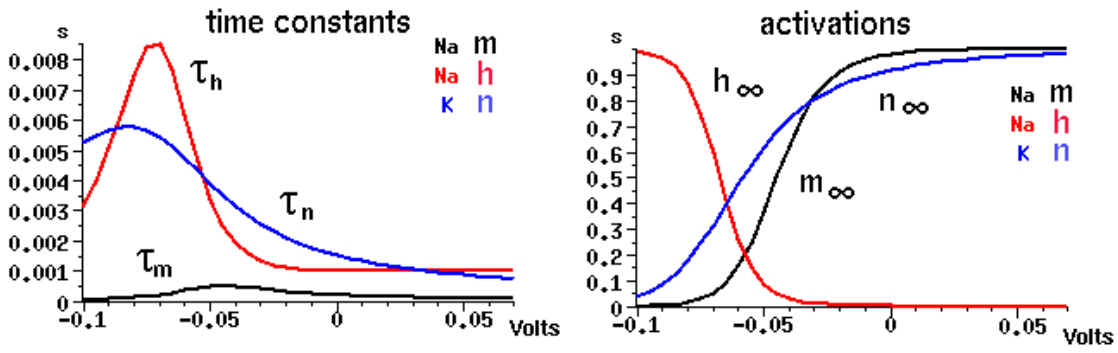

Figure 1.4: Ion channels activation

1.1.3 Resting Potential

The neuron's electrical activity is due to the presence of an electrochemical gradient across the neuron's membrane [3].

There are relatively more sodium ions outside the neuron and more potassium ions inside that neuron. Even if the concentrations of the different ions attempt to balance the difference of potential between the internal and the external side of the membrane, the ions cannot pass because the cell membrane allows only some ions to pass through channels (ion channels).

Ion	$[Ion]_{out}$	$[Ion]_{in}$	$\frac{[Ion]_{out}}{[Ion]_{in}}$	Equilibrium potential @ $37°C$
Na^+	$145mM$	$12mM$	12	$+67mV$
K^+	$4mM$	$155mM$	26×10^{-3}	$-98mV$
Ca^{++}	$1.5mM$	$0.1\mu M$	15×10^3	$+129mV$
Cl^-	$123mM$	$4.2mM$	29	$-90mV$

Table 1.1: Free ionic concentration [1]

At rest, potassium ions (K^+) can cross through the membrane easily, but chloride ions (Cl^-) and sodium ions (Na^+) have a more difficult time crossing. The negatively charged protein molecules (A^-) inside the neuron cannot cross the membrane. In addition to these selective ion channels, there is a pump that uses energy to move $3Na^+$ out of the neuron for every $2K^+$ it puts in.

At resting potential the sodium - potassium pumps move approximately the same

electrical charge inside and outside the cell.

Potassium channels are also present allowing free flow of only potassium ions.

The higher concentration of potassium inside the cell drives potassium ions to the outside. After a small number of potassium ions leave the cell, the outside of the cell becomes positively charged compared to the inside, developing an electrical field. This electrical field balances the force on the ions from the concentration gradient and is known as the resting potential.

The Nerst equation gives the equilibrium potential as function of the ionic concentration ($[S]$) ratio and the valence (z_s):

$$E_s = E_1 - E_2 = \frac{RT}{z_s F} ln(\frac{[S]_1}{[S]_2}) \tag{1.6}$$

where R is the gas constant ($8.415 \frac{J}{Kmol}$) and F is the Faraday's constant ($9.648 \times 10^4 \frac{C}{mol}$). To calculate the transmembrane potential, it is necessary to modify the Nerst equation, weighting the ionic concentration in proportion of open channels through the membrane:

$$E_s = \frac{RT}{F} ln(\frac{[P]_k[K]_{out} + [P]_{Na}[Na]_{out} + [P]_{Cl}[Cl]_{in} - \frac{I_{pump}}{F}}{[P]_k[K]_{in} + [P]_{Na}[Na]_{in} + [P]_{Cl}[Cl]_{out}}) \tag{1.7}$$

where P is the permeability constant, I_{pump} is the current flow through the sodium - potassium pumps.

The major contribution to the resting membrane potential is due to K^+. The difference between the intracellular and extracellular potential, is the resting potential value, and is typically $-70mV$.

1.1.4 Action Potential

If the transmembrane potential reaches about $-50mV$, voltage gated sodium channels will open for a short period.

Upon activation, sodium channels open in the membrane allowing ions to flow rapidly down their electro-chemical gradient toward a new steady state. This new state (depolarization) is reached when the intracellular potential reaches $+50mV$.

This is an activated state, which does not last long because the ion channels quickly

change their configuration again and the cell membrane returns to the previous state pumping positively charged ions outside the cell (repolarization).

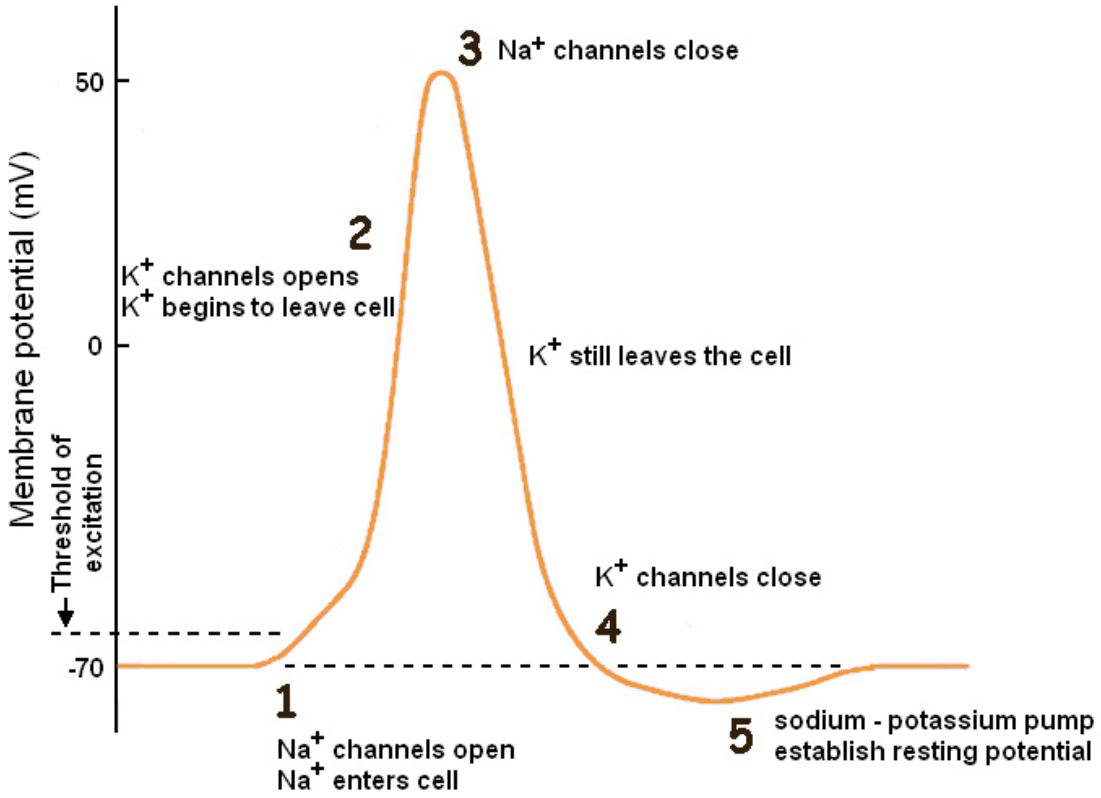

Figure 1.5: Action Potential

The process can be summarized as following:

1. The first step of the action potential is the opening of Na^+ channels allowing a flood of sodium ions into the cell. This causes the membrane potential to become positive.

2. At some positive membrane potential the K^+ channels open allowing the potassium ions to flow out of the cell. This state of depolarization is reached when the intracellular potential reaches $+50mV$.

3. Next the Na^+ channels close. This stops inflow of positive charge. But since the K^+ channels are still open it allows the outflow of positive charge so that the membrane potential decreases.

4. When the membrane potential begins reaching its resting state the K^+ channels close.

5. The sodium - potassium pump starts, transporting sodium out of the cell, and potassium into the cell so that it is ready for the next action potential.

The entire membrane does not depolarize at once. Rather, depolarization starts in one area and spreads by diffusion to contiguous regions. The entire process of depolarization and repolarization takes between $0.5ms$ and $1.5ms$.

1.2 Cultured Cell Recording Methods

The neural recording may be performed on a complete live animal (in vivo) or in extracted tissue (in vitro).
Use of cultured cell outside of the body simplifies the recording of electrical activity, giving the chance to stimulate the cells electrically or chemically and determine how it reacts. For this reason, finding best ways to record from cultured cells electrical activity become very important.

1.2.1 Patch clamping

The first method that was introduced is the patch-clamping. It consists of patching the tip of an electrolyte-filled pipette to the membrane of a cell, clamping it to a preset voltage, and measuring the resulting current. This is an invasive method and allows the study of individual ion channels in cells, using a glass pipette, with an open tip diameter of about $1\mu m$.

The patch clamping measures directly the transmembrane potential by an intracellular recording of action potential. The method permits for a signal with an amplitude of $100mV$ to be recorded, but it has a mechanically fragile connection which makes long term recordings difficult. In some cases it involves also a localized rupture of the cell membrane compromising the intracellular ionic composition.

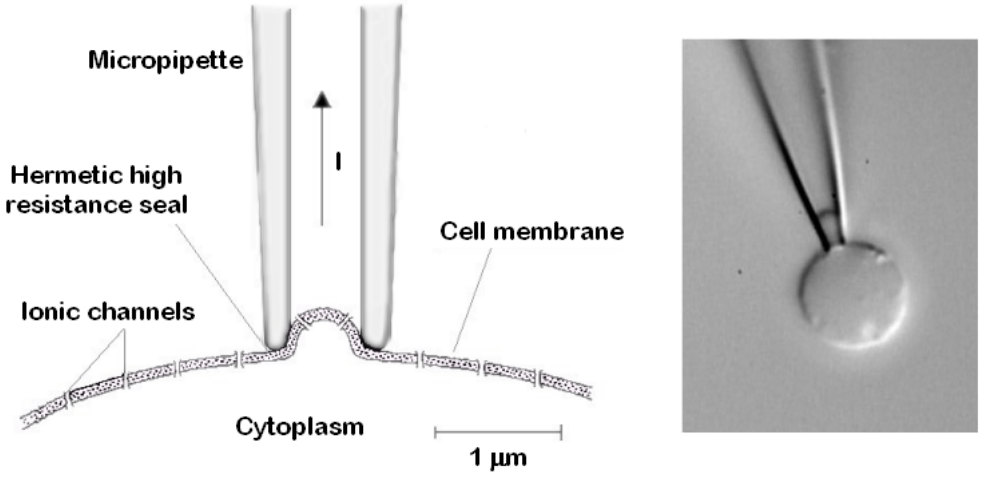

Figure 1.6: Patch clamping

1.2.2 Microelectrode

The disadvantages inherent in invasive techniques lead to the development of non-invasive solutions.

When in a cell, the transmembrane potential varies, the ion concentration in the surrounding extracellular medium changes. This cause a time-varying difference in potential between a recording electrode, in close proximity of the cell, and a distant neutral reference electrode. In this way the electrical activity of neurons can be recorded, in a non invasive way, without disturbing any cell membrane.

The diameter of these electrodes is on the order of $10\mu m$, and the signal is on the order of $100\mu V$.

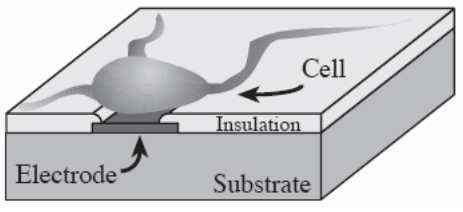

Figure 1.7: Scheme of a cultured cell over an electrode

This method even if do not permit to measure directly the action potential

has some advantages over standard intracellular recording which are related to the possibility of monitoring and stimulating the electrochemical activities of several cells independently and simultaneously for a long time.

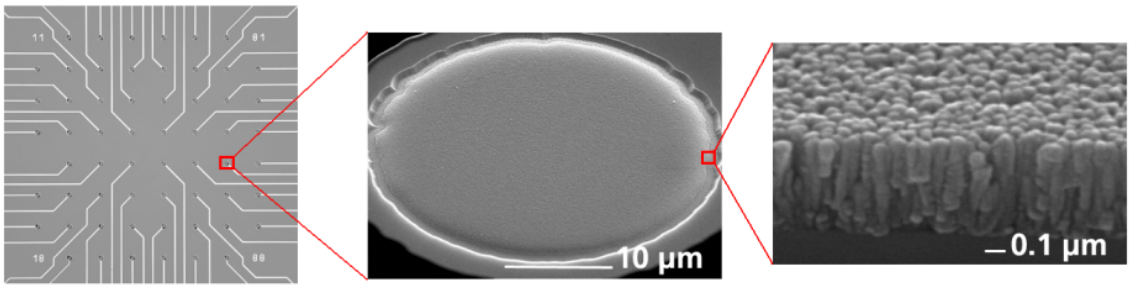

Figure 1.8: Titanium nitride MEA [4]

A microelectrode array (MEA) is an arrangement of several electrodes (typically 60 outdistanced of some hundreds micrometers) allowing extracellular recording and stimulation of several sites in parallel. Planar microelectrodes are non-invasive, can accommodate large numbers of cells, and are simple to implement.

The biological sample can be positioned directly on the recording area, the MEA serves as a culture and perfusion chamber. Electrical activity can be detected at distances of up to $100\mu m$ from a neuron in an acute brain slice. Typically, signal sources are within a radius of $30\mu m$ around the electrode center. Small electrode and interelectrode distance results in a higher spatial resolution.

The impedance of a flat, round titanium nitride electrode ranges between 20 and $400k\Omega$, and decreases increasing the diameter.

The smaller an electrode, the higher is the noise: the average noise level of $30\mu m$ microelectrode is less than $10\mu V$ and for $15\mu m$ microelectrode is less than $15\mu V$.

1.2.3 Diamond microelectrode

Diamond is the most recent material considered for microelectrode implementation and it is still in testing phase.

Although the diamond has a bandgap of $5.5eV$ and it is considered an electrical insulator, it has been discovered that if its surface is hydrogenated it become conductive.

Trough the hydrogenation process the dangling bonds at the surface of diamond are saturated by monovalent hydrogen atoms (see Figure 1.9). In this process there are particular defects that act as acceptors which creates a hole accumulation layer at the diamond surface.

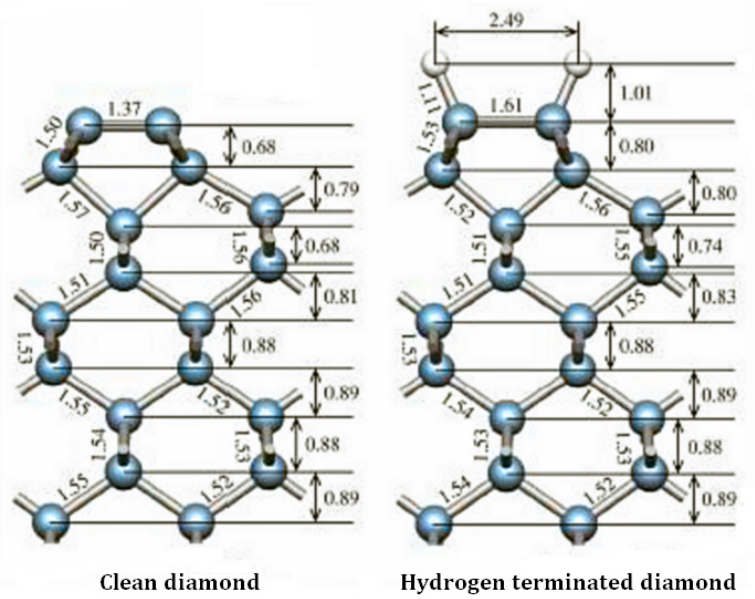

Figure 1.9: Atomic geometries for the clean and hydrogenated (001) diamond surfaces

Furthermore when the diamond surface is exposed to the atmosphere, a thin water layer spontaneously forms over it. This water layer acts as a surface acceptor for diamond exchanging electrons with the diamond hydrogen terminated surface. In this way diamond surface becomes conductive, with an areal density of p-type carriers $\rho_{surface} \approx 10^{13} cm^{-2}$, and a superficial sheet resistance of $\approx 10^4 \Omega/\square$ at room temperature.

The diamond presents some interesting properties which make it superior to conventional electrode materials.
First of all the diamond is biocompatible, it has an inert surface that assure a long term stability with weak adsorption of polar molecules.

The diamond has a transmittance greater than 50% in the visible wavelength region upon $500nm$, so it can be considered optically transparent. When a cell is positioned over a diamond electrode it could be seen through the microscope, on the contrary a classical metallic microelectrode is not transparent and covers the area upon him hiding the cell. This permits to position correctly the cell over the microelectrode. Besides also the optical signals of cells by using fluorescent dyes could be recorded. The characteristics of the diamond surface, in particular the resistivity, could be modulated with oxygen or hydrogen termination.

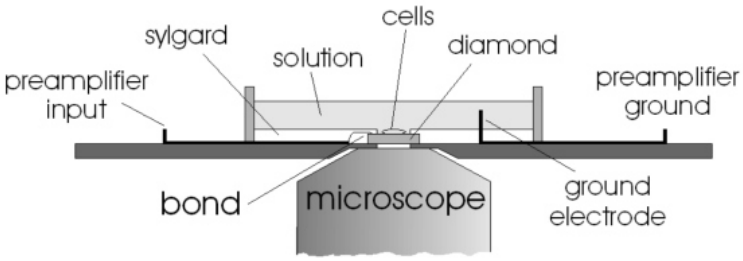

Figure 1.10: Diamond macroelectrode testing setup

For the testing measurement a diamond macroelectrode with a recording area of $3mm^2$ was used.

The borders of the macroelectrode are fixed to a high resistivity printed circuit board. A microscope is positioned under the macroelectrode and through it is possible to see the cells placed over the macroelectrode and immersed in the electrolyte medium.

A sylgard passivation layer is used to insulate the electrolyte form the conductors, interconnects and bondwires. The preamplifier input signal comes from a gold wire of $20\mu m$ diameter pasted to the diamond with a silver paste. The ground electrode is connected to a silver chloride reference electrode immersed in the culture media. From this experimental setup it is possible to measure the noise level of the diamond electrode. A noise level lower than the metallic electrodes ($\leq 5\mu V$) is expected. To amplify the signal without increase the noise floor, the signal that comes form the diamond electrode has to amplified by a low noise preamplifier. Its requirements are analyzed in detail in the next Chapter.

1.3 MEA as Biosensor

An extracellular recording system (Figure 1.11)is composed by the following components:

- Signal source (cells / tissue)
- Cell / sensor interface
- Microelectrode arrays (MEA)
- Analog Front End (AFE)
- Recording hardware and software

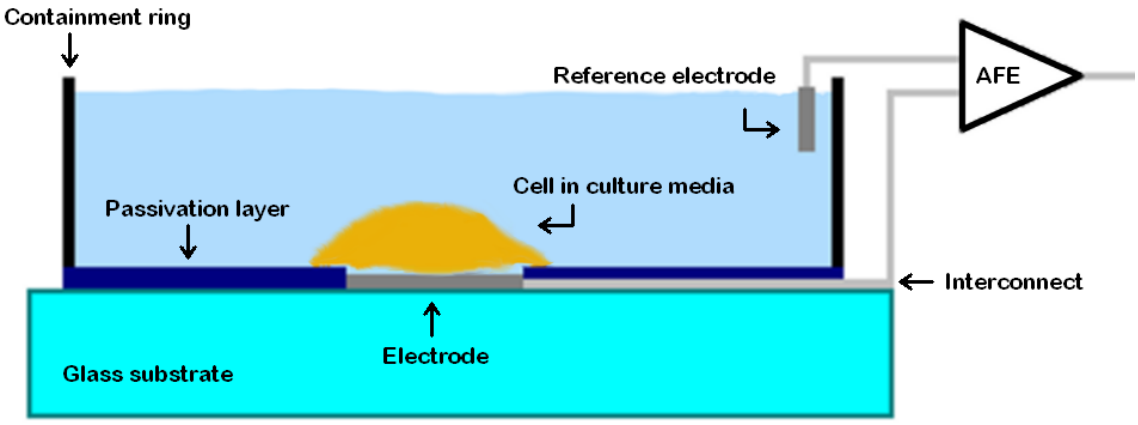

Figure 1.11: Sensor

Planar microelectrode arrays for cultured cell studies consist of a substrate of glass, plastic or silicon (which allows inclusion of active circuitry in close proximity to the cells) over which a conductor (gold, platinum, indium-tin-oxide, iridium, etc.) is deposited and patterned.

A passivation layer is deposited over the conducting electrodes and interconnects and then removed in regions over the electrodes to define the recording sites.

Each electrode site is generally connected to the input of a high input impedance, low noise amplifier to allow amplification of the relatively small extracellular signals. Cells are cultured directly on this surface and contact the exposed conductor at the

deinsulated recording sites.

Depending on the size of the electrodes and the cells, recordings of electrical activity or impedance can be from a single cell or populations of cells.

Extracellular signals are 10^3 times smaller than transmembrane potentials, the amplitude and wave shape of the transduced signal depend on many factors, including the diameter of the neuron, the proximity of the electrode to the neuron, the angle between the electrode surface and the neuron, and even the particular portion of the neuron to which the electrode is closest.

There are small regions of close adhesion where the distance between cell membrane and substrate is below $15nm$. Other regions of the membrane are more loosely coupled and the separation distance reaches $100nm$.

Due to the low-pass filtering properties of the extracellular space, extracellular signal amplitudes decrease with increasing distance of the signal source to the electrode, neurons located beyond $140nm$ from the electrode become indistinguishable from noise.

Therefore, a high spatial resolution of the electrode array and a close interface between electrode and cell membrane is very important for a high signal-to-noise ratio.

The transmembrane current and the extracellular potential are approximately equal to the first derivative of the transmembrane potential, the reason for this will be explained in next section.

1.3.1 Sensor electrical model

To understand the relationship between the action potential and the signal measured with the electrode is important to create a schematic circuit of the cell - electrode junction.

The first step is to consider the resistive model of a cell positioned over an electrode (Figure 1.12), which takes account of:

$Z_{electrode}$, the electrode impedance.

R_{seal} , the resistance between the electrode and the bulk electrolyte due to the thin layer of medium between the cell and the passivation layer.

C_{m1} **and** R_{ch1} , the membrane capacitance and ion channel resistance over the electrode.

C_{m2} **and** R_{ch2} , the membrane capacitance and ion channel resistance of the top and sides of the cell.

R_{soln} , the solution resistance.

Z_{co} , the reference electrode impedance.

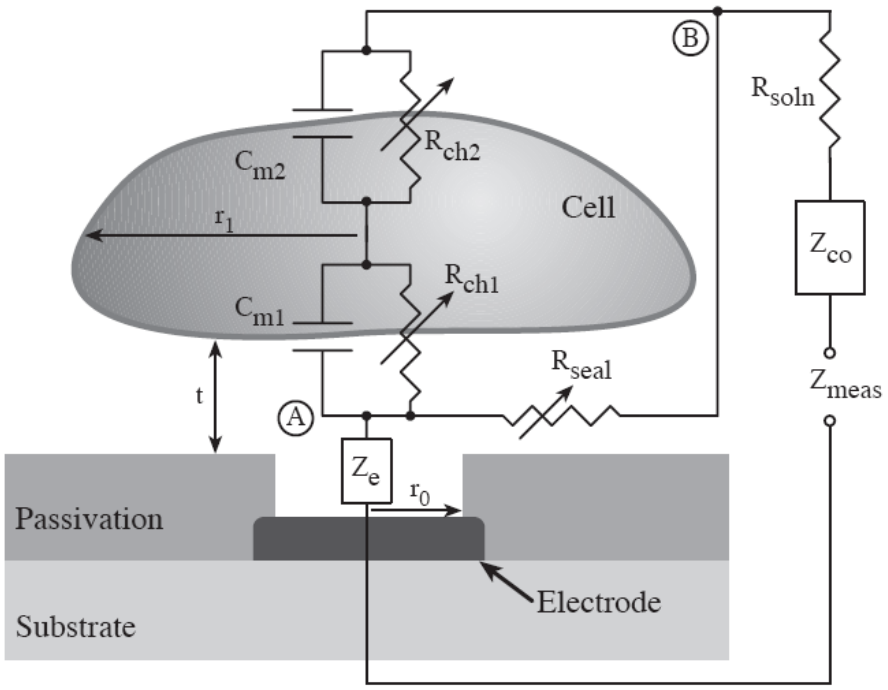

Figure 1.12: Full resistive model of a cell positioned over an electrode [1].

Note that in reality R_{seal} is distributed with the capacitance and conductance of the membrane in the region over the passivation layer. The resistance R_{seal} must be of the same order or larger than the membrane impedance if changes in membrane properties are to be observed.

From the resistive model, could be made a simplified electrical model, which considerers only the cell base and microelectrode interaction (Figure 1.13).

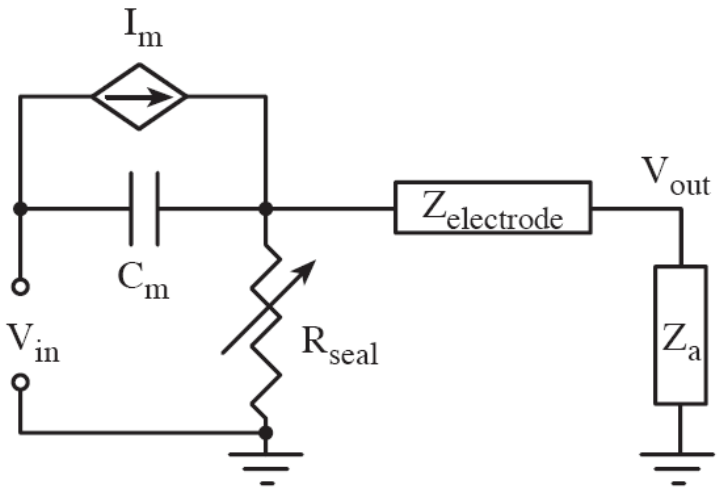

Figure 1.13: Electrical model of a cell positioned over a microelectrode [1].

V_{in} is the transmembrane voltage, measurable directly only with an intracellular recording.

C_m is the basal membrane capacitance.

I_m is the basal ionic current, that flows through the ionic channels.

R_{seal} is the resistance between the electrode and the bulk electrolyte due to the thin layer of medium between the cell and the passivation layer.

$Z_{electrode}$ is the electrode impedance.

Z_a is the input impedance of the amplifier.

Microelectrode - electrolyte interface

A description of the interface between the electrode and electrolyte is necessary to understand how the electrode transfers the signal to the amplifier and to create the model of the electrode impedance ($Z_{electrode}$).
When a metallic electrode is immersed in a electrolyte medium, both of them are electroneutral, but chemical reactions immediately start, in which electrons are transferred between the metal and electrolyte, forming an electric field at the interface. This induced electric field inhibits the reduction reaction ($A^+ + e^- \rightarrow A$)

while favoring the oxidation reaction ($A \rightarrow e^- + A^+$), until an equilibrium condition is reached and the net currents due to electron transfer is zero.

The induced electric field orient the electrolyte's water dipoles in a layer at the

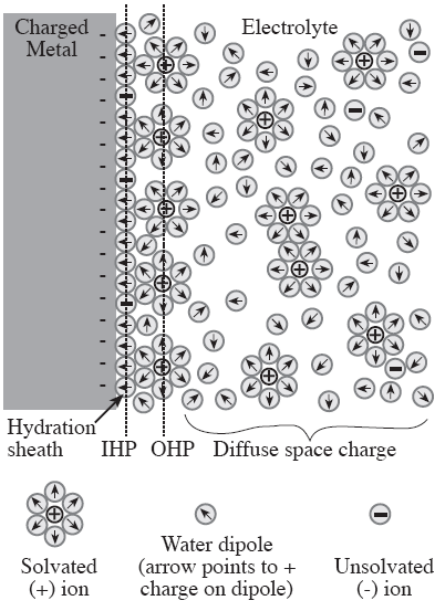

Figure 1.14: Microelectrode - electrolyte interface

metal surface. There is also a specific adsorption of ions at the electrode surface interspread with the orientated water dipoles. The locus of centers of these ions is called inner Helmholtz plane (IHP).

Just beyond the water dipoles there are solvated ions (result of the electron transfer with the metal). The outer Helmholtz plane (OHP) is the locus of the electrical centres of solvated ions in their position of closest approach.

This complex system can be modeled using passive circuit elements as in Figure 1.15. The double layer is modeled with the interfacial capacitance (C_I). There is equal current flow in both directions which results in zero net current.

If a DC potential is applied across the interface, there will be a current flow across the plate, so there must be a resistive path in the model. If the potential difference is relatively small, the current flow will be linearly related to the voltage. The equivalent resistance is called charge transfer resistance (R_t). In series is added a resistor and capacitor in parallel (R_w and C_w), to model using Warburg's theory,

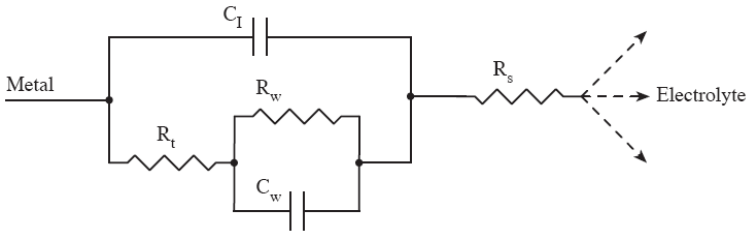

Figure 1.15: Circuit model for the metal-electrolyte interface ($Z_{electrode}$).

the impedance effects caused by diffusion.

Spreading resistance, R_s, is modeled for the current that spreads outward from the electrode to the solution it is in. There are several methods proposed to calculate this resistance. In general, the calculation depends on the shape and conductivity of the electrolyte.

In table 1.2 the electrode model parameters values for different electrode size are reported.

Area	C_I	R_t	$C_w 1/\sqrt{Hz}$	$R_w\sqrt{Hz}$	R_s
$480\mu m^2$	$326pF$	$6.8M\Omega$	$7.0\mu F$	$22.9k\Omega$	$14.6k\Omega$
$240\mu m^2$	$163pF$	$13.5M\Omega$	$3.5\mu F$	$45.8k\Omega$	$20.6k\Omega$
$120\mu m^2$	$82pF$	$27.1M\Omega$	$1.7\mu F$	$91.7k\Omega$	$29.1k\Omega$
$60\mu m^2$	$41pF$	$54.2M\Omega$	$869nF$	$183k\Omega$	$41.2k\Omega$
$30\mu m^2$	$20pF$	$108M\Omega$	$435nF$	$367k\Omega$	$58.2k\Omega$
$150\mu m^2$	$15pF$	$217M\Omega$	$217nF$	$733k\Omega$	$82.4k\Omega$

Table 1.2: Electrode model parameters for different electrode sizes on the electrode array. All electrodes are circular and bare platinum [1].

1.3.2 Signal Transduction

The action potential propagates along the transversal direction of the membrane as a traveling wave.

For a traveling wave the total current is proportional to the second derivative of the transmembrane potential (V_m):

$$I_{total} = K\frac{d^2V_m}{dt^2} \tag{1.8}$$

where K is the propagation constant which depends on the resistance and shape of the propagation mean. This current will flow through the seal resistance, generating a potential at the electrode equal to the product $I_{total} \cdot R_{seal}$, which is transduced by the microelectrode.

The amplitude and the shape of the transduced signal depend on the coupling between the cell and the microelectrode, which is modeled with the resistance R_{seal}. A high value of R_{seal} indicates a tight seal condition, a low value of R_{seal} indicates a weak coupling.

In the bandwidth of interest the electrode is mostly capacitive, combined with the input resistance of amplifier (Z_a) it formes a high pass filter, which result in an additional derivative for the frequencies below the pole.

The seal resistance between the cell and the electrode, the parasitic current paths between the electrode and amplifier can alter the shape of the recorded action potential. Theoretically the signal transduced by the microelectrode could change from a close approximation of the intracellular action potential to its third temporal derivative.

Figure 1.16 shows the results of three simulation with three different R_{seal}.

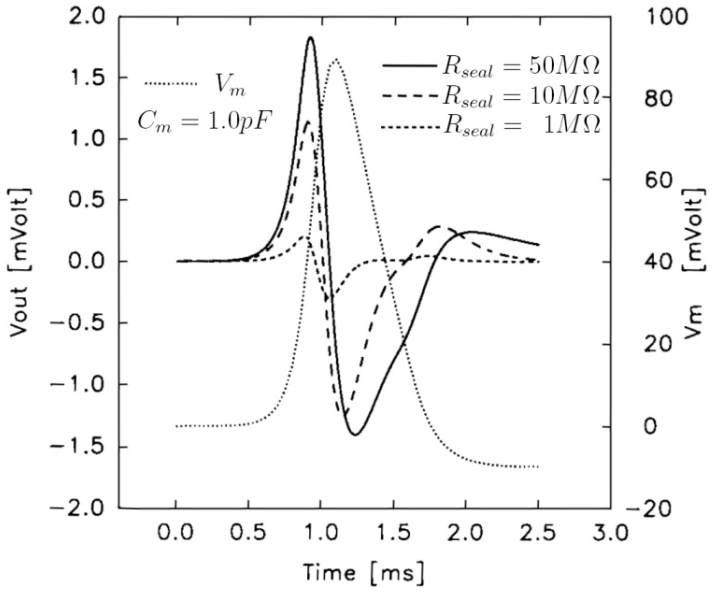

Figure 1.16: Results of microelectrode recording simulation with 1, 10, 50 $M\Omega$ [5].

The signal obtained by $1M\Omega$ is similar to the second time-derivative of the action potential. The signal obtained by $10M\Omega$ is slower than that obtained by $1M\Omega$ and its shape becomes less similar to the second time-derivative and more similar to the first time derivative of the action potential. The similarity to the first time derivative of the action potential becomes evident when using $R_{seal} = 50M\Omega$.
Figure 1.17 shows the results of the simulation in a strong adhesion condition ($R_{seal} = 1G\Omega$), which is impossible to obtain with a microelectrode, because all its surface must stay at $10nm$ from the cell. The simulated signal is very similar to the action potential.

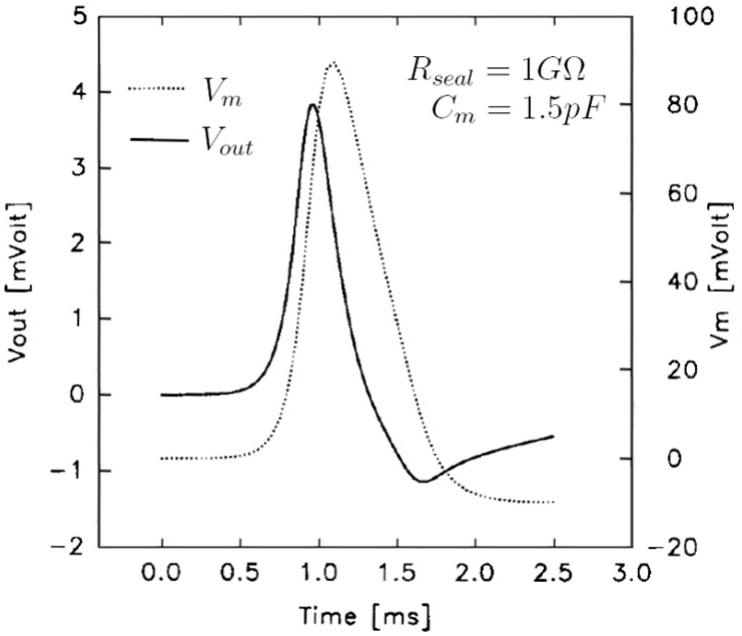

Figure 1.17: Result of microelectrode recording simulation in a strong adhesion condition, $R_{seal} = 1G\Omega$ [5].

Chapter 2

Front End Architectures for Neural signal Recording

The Analog Front End (AFE) interfaces the sensor to the analysis/reading instrumentation.
The typical AFE contains the following building blocks:

Preamplifier input stage which receives the signal from the microelectrode.

Bandpass Filter amplifies and filters the signal.

Output buffer connect the precedent stages to the recording hardware.

Many implementations of AFE for neural signal interfaces have been proposed, but some of them have implementation problems regarding large components values which are not integrable, high power dissipation, use of non standard CMOS processes, or requirement of high precision matching.
This chapter describes some interesting solutions which have been proposed in scientific literature.

2.1 Basic Specifications

The AFE requirements, are imposed by the characteristics of the signal coming form microelectrode:

- Amplitude: $150\mu V$
- Frequency: $10Hz - 3KHz$
- Biological Noise: $10\mu Vrms$
- DC component: $\pm 50mV$

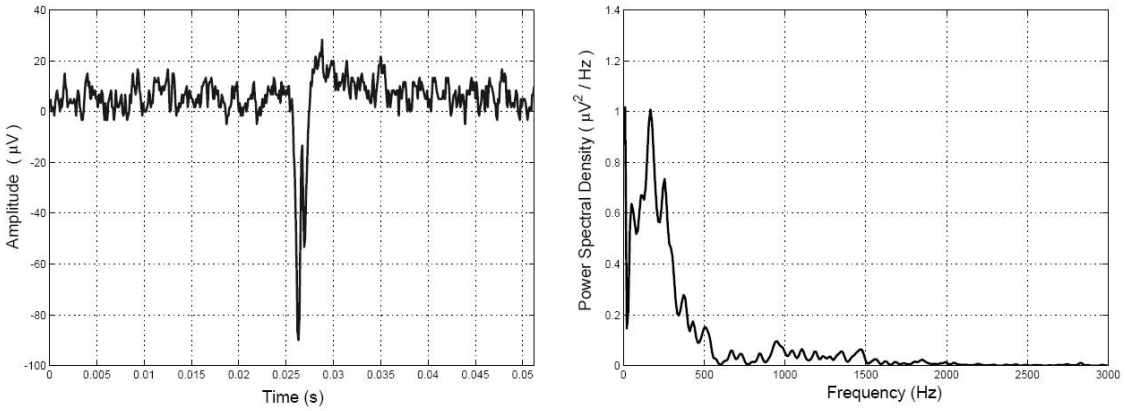

Figure 2.1: Time and frequency domain analysis of neuron electro-physiological activity [6].

First of all, the preamplifier has to cut the DC component, with a typical band between $f_L \approx 10Hz$ and $f_H \approx 10kHz$.
The differential input must have a high input resistance, so that the voltage drop on the the microelectrode ($R_{elecotrde} \leq 400K\Omega$) should be negligible.
The most critical factor is the noise, which must be very low. The preamplifier should have also high gain in order to minimize the noise contribution of the following stages. A low power consumption is desirable, in order to reduce the heating, and a small silicon area permits to have many recording channels on the same chip.

2.2 NEURO32 chip Architecture

NEURO32 chip [7] is a 32-channel integrated circuit for recording neuronal signals in neurophysiological experiments using microelectrode arrays.

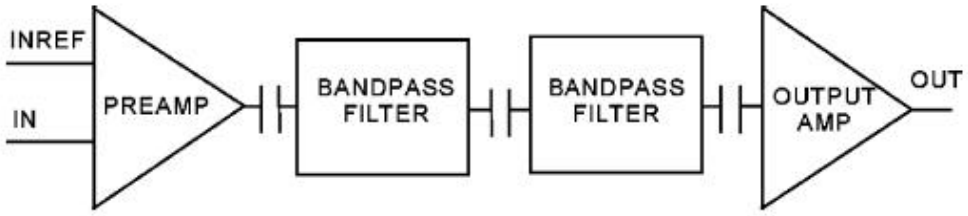

Figure 2.2: Block diagram of a single analog channel of NEURO32 chip.

Each of the 32 channels (Figure 2.2) has a low-noise preamplifier and bandpass filters, and an output analog multiplexer. All stages are separated by AC-coupled buffer circuits.

2.2.1 Preamplifier

The preamplifier must have tolerance for large DC input voltage offsets that are generated at the electrode-electrolyte interface.

To optimize the full circuit noise performance, the gain of the input stage should be sufficiently high such that the noise contributions from the following stages are negligible. Therefore it is very important to have a low noise in this stage.

The preamplifier (Figure 2.3) has an input differential stage, which gain is controllable with the current IPRE in the range $20 - 100V/V$. The second stage is formed by a source follower and a common source amplifier with source degeneration, with a total gain of $5V/V$. Between this stages there is an AC-coupling capacitor with an DC bias circuit.

In low frequency region the noise of MOS transistors is dominated by flicker noise. In the process used the ratio of flicker noise coefficients of NMOS and PMOS transistor is $\frac{K_{fn}}{K_{fp}} \approx 60$, so it is better to use a PMOS transistor in the input stage.

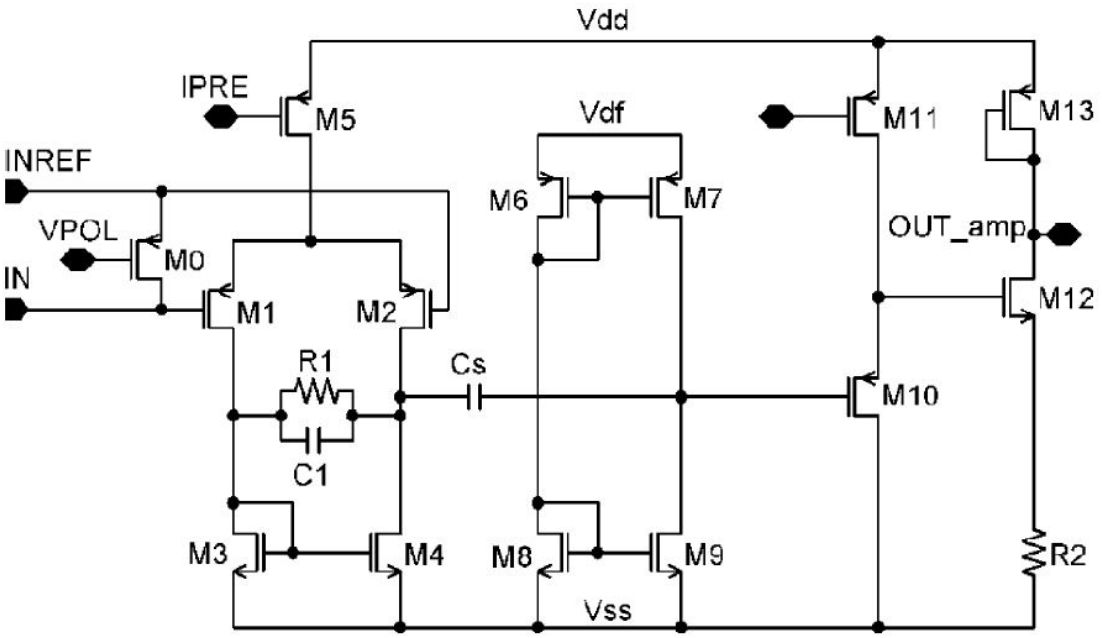

Figure 2.3: Schematic diagram of the NEURO32 chip preamplifier.

The flicker noise spectral density is minimized when:

$$\frac{L_1}{L_3} = \sqrt{\frac{K_{fp}\mu_p}{K_{fn}\mu_n}} \tag{2.1}$$

where μ_p and μ_n is the hole and electron mobility respectively.

Even if the thermal noise is not dominating, it has to be minimized by using input transistors with large W/L ratio and large drain current.

The source follower noise performance is not critical, because the input stage has an high gain and the input referred noise due to it is negligible. The principal requirement for the source follower is a wide linear output range.

Increasing the bias current of the input differential pair the gain increases and the noise decreases, but an high gain reduces the tolerance to the input offset. The measured parameters of the preamplifier are summarized in Table 2.1.

Figure 2.4 shows the measured noise spectrum at the output of the preamplifier for three different values of the bias currents. From $500Hz$ to $2kHz$ the white noise and flicker noise have the same contribution, for values under this range the flicker noise dominates, for values upon this range the white noise dominates.

The input impedance of amplifier must be much higher than the electrode impedance,

$I_{bias}(\mu A)$	$Gain(V/V)$	$V_{noise,in}(\mu Vrms)$	Tolerance to the input offset (mV)
150	522	1.22	(-7, +9)
100	450	1.32	(-8, +14)
79	414	1.35	(-8, +17)
63	350	1.53	(10, +22)
43	294	1.61	(12, +26)
34	247	1.77	(-14, +35)
24	196	2.13	(-18, +47)
16	138	2.73	(-24, +62)
11	100	3.36	(-34, +60)

Table 2.1: Gain, noise and tolerance to the input offsets as a function of the bias current in the input stage

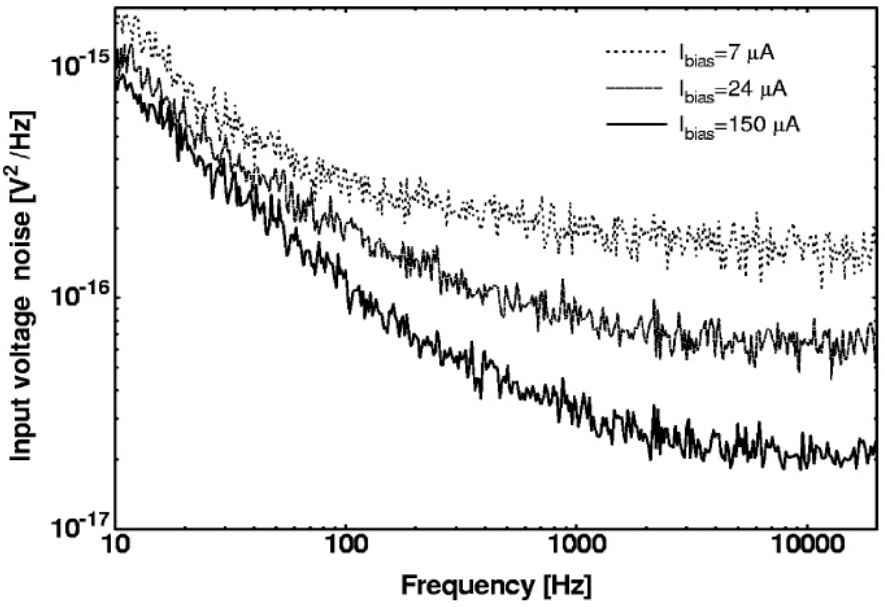

Figure 2.4: Input referred noise spectrum of NEURO32 chip preamplifier, with different bias current [7].

which depends on the experimental set-up and can vary from $10k\Omega$ to $10M\Omega$. On the other hand, the input impedance should not be too high, to reduce the effects of any parasitic currents flowing to the electrode.
In order to control the input impedance of the preamplifier, there is a voltage controlled resistor, between the two inputs of the preamplifier, which is realized using a long PMOS transistor controlled by the external reference voltage VPOL.

2.2.2 Bandpass filter

This design of this stage is driven by the silicon area and the power consumption constraints.
The filter stage input is connected at the preamplifier output through AC coupling circuit.
A novel scheme for band pass filter is proposed in this paper, in order to set the lower cut-off frequency at approximately $20Hz$, using low value capacitors, in the range of a few picofarad.
The band pass filter is obtained as combination of two RC low pass filters, and a differential amplifier (Figure 2.5).

The transistors M25 e M26 work as resistance of the RC filters, the capacitor C_{hf} is used to set the higher cutoff frequency (p_2) and C_{lf} to set the lower cut off frequency (p_1). The dominant pole, which determines the lower cutoff frequency of the filter, is pushed down by the Miller effect. The capacitance C_{lf} is multiplied by the gain of the differential amplifier ($\approx 400V/V$):

$$p_1 = \frac{1}{[g_{m29}/(g_{ds29} + g_{ds31})]C_{lf}R_{lf}}. \tag{2.2}$$

Whit the external currents (IFILTR, ILF, IHF) the gain, the low and the high cutoff frequencies can be separately controlled (see Figure 2.6).

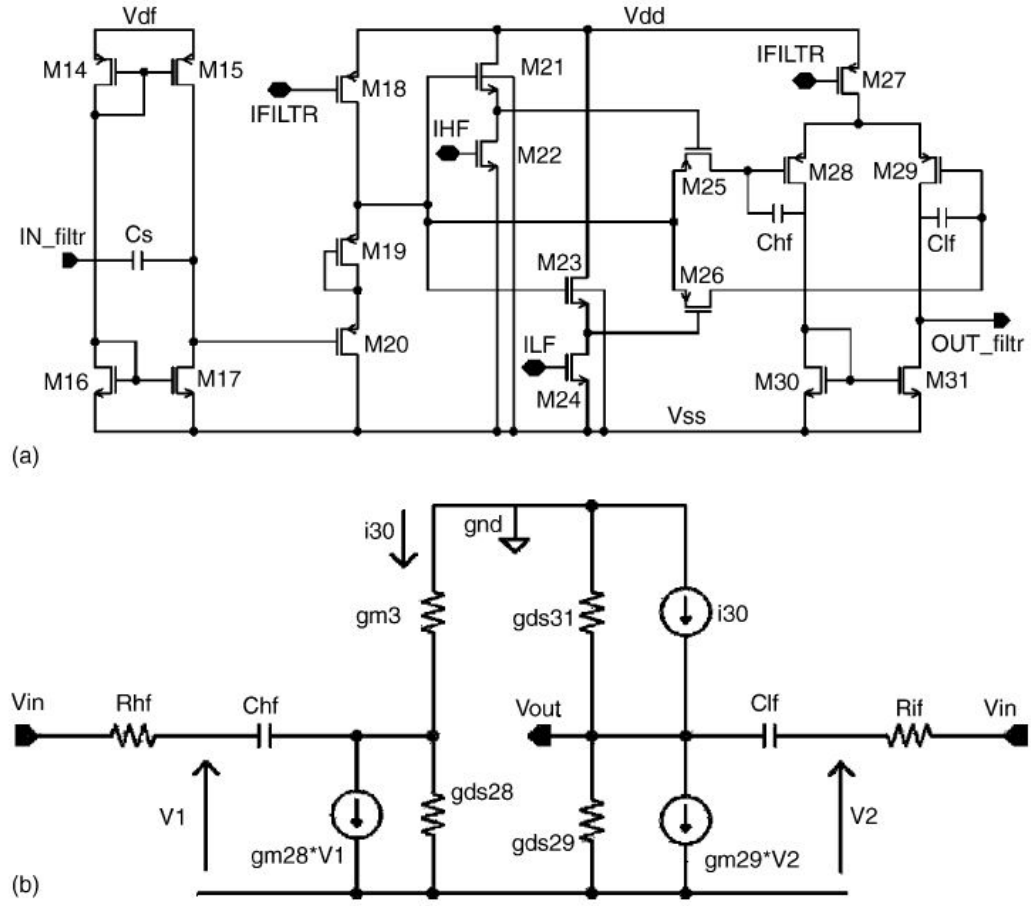

Figure 2.5: Schematic diagram of the NEURO32 chip filter stage (a), and equivalent circuit model (b).

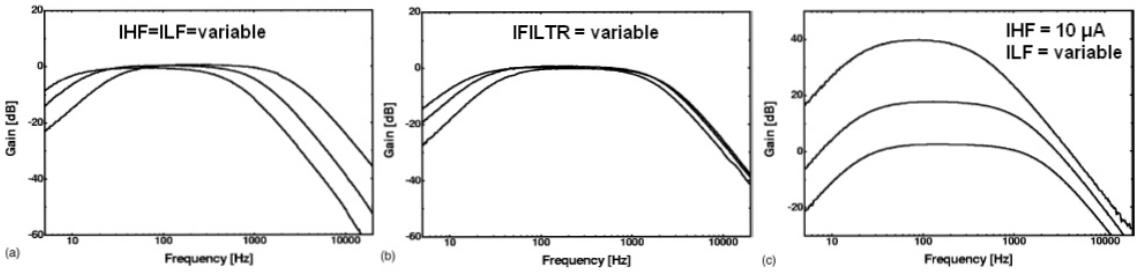

Figure 2.6: Measured frequency responses of two cascaded filter stages for three different mode of passband control for Neuro32 chip.

2.2.3 Output amplifier

The role of the output amplifier is to suppress the difference of the DC output offset between the different channels.

The output amplifier input is AC-coupled with the filter stage output.

The first stage is formed by two source followers, connected to the differential

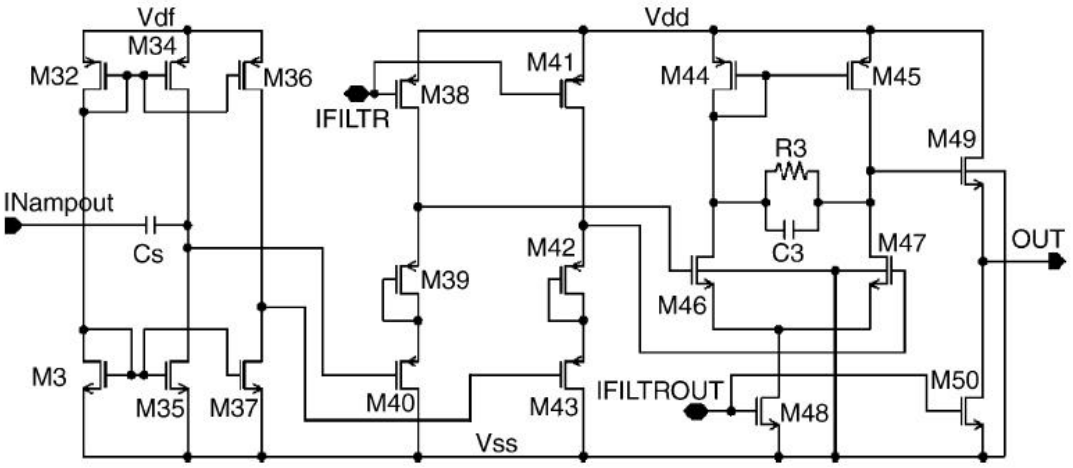

Figure 2.7: Schematic diagram of the NEURO32 chip output amplifier.

stage. At the output the signal is large and the most important requirement of this amplifier is the linearity. In this design the gain is $2V/V$ and the output linear range is $\pm 1V$. The DC output is $0V$ with a rms variation of DC output offset of $5mV$.

2.2.4 Results

The chip was fabricated in a $0.7\mu m$ CMOS process, in Table 2.2 the principal parameter of the chip are reported.

Figure 2.8 shows the measured distribution of gain and equivalent input noise on all channels of the NEURO32 chip. The noise of $3\mu V$ is the minimum obtainable value when the inputs are shorted to the ground, instead when the input is connected to the electrode, there is also the noise due to input transistor $M0$ (see Figure 2.3).

Parameter	Measured value
Nominal bandwidth	$30 - 2000Hz$
Total equivalent input noise	$3\mu Vrms$
Input signal linear range	$960\mu Vp - p$
Tolerance to the input offset	$(-10mV, +20mV)$
Gain	$1000V/V$
Input signal common mode range	$\pm 300mV$
Power dissipation per channel	$1.7mW$
Power supplies	$+2.5V, -2.5V$
Single channel area	$100\mu m \times 3500\mu m$
Total chip area	$4.0mm \times 4.3mm$
Control range of the lower cut-off frequency	$10 - 130Hz$
Control range of the higher cut-off frequency	$400 - 2800Hz$
Control range of the gain	$100 - 10000V/V$

Table 2.2: Summary of basic parameters and test results of the NEURO32 chip [7].

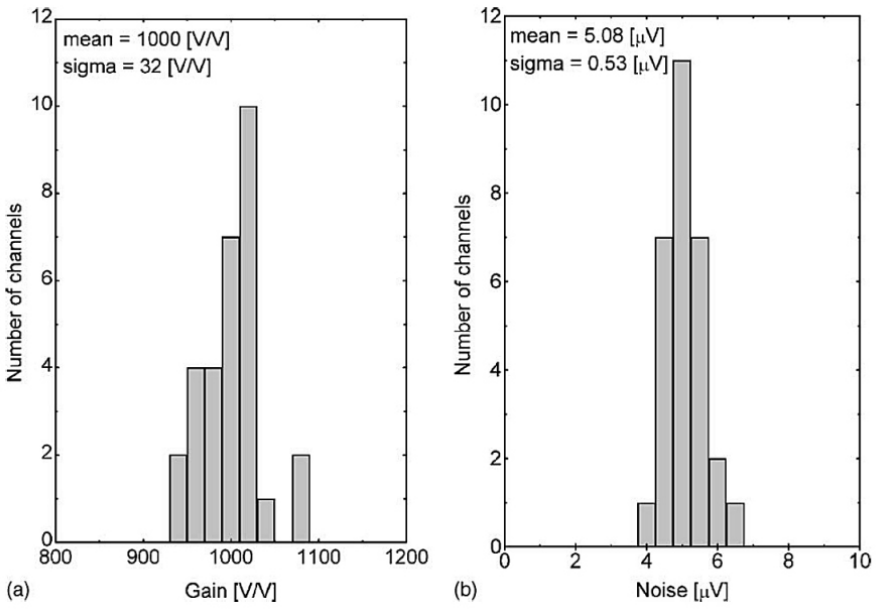

Figure 2.8: Distributions of (a) gain, and (b) equivalent input noise in 32 channels of one NEURO32 chip [7].

2.3 Harrison Preamplifier Architecture

The architecture proposed by Harrison [8] introduces a new technique to implement in an integrated circuit a high value resistance using MOS-bipolar pseudoresistor elements.

The design of the preamplifier (Figure 2.9) consists in a bandpass filter, realized through a resistive-capacitive feedback loop. The preamplifier transfer function is:

$$A_{vM}(s) = \frac{A_{v0}^{OTA}(sC_1R)}{(A_{v0}^{OTA}+1)(sC_2R+1)+sC_1R} \tag{2.3}$$

where A_{v0}^{OTA} is the OTA open loop gain.

The values of R and C_2 define the low frequency cutoff $f_L = \frac{1}{2\pi RC_2}$.

To set $f_L \approx 10Hz$, the product RC_2 must be $\approx 10^{-2}$. If we use a $50pF$ *poly1-poly2* capacitor the required resistor value would be in order of $10^9\Omega$ which can not be integrated as a standard linear resistor. On the other hand a $50pF$ capacitor in $0.35\mu m$ CMOS process typically occupies already an area of $0.06mm^2$. Therefore further increasing the size of the capacitor would quickly lead to a excessive use of silicon area.

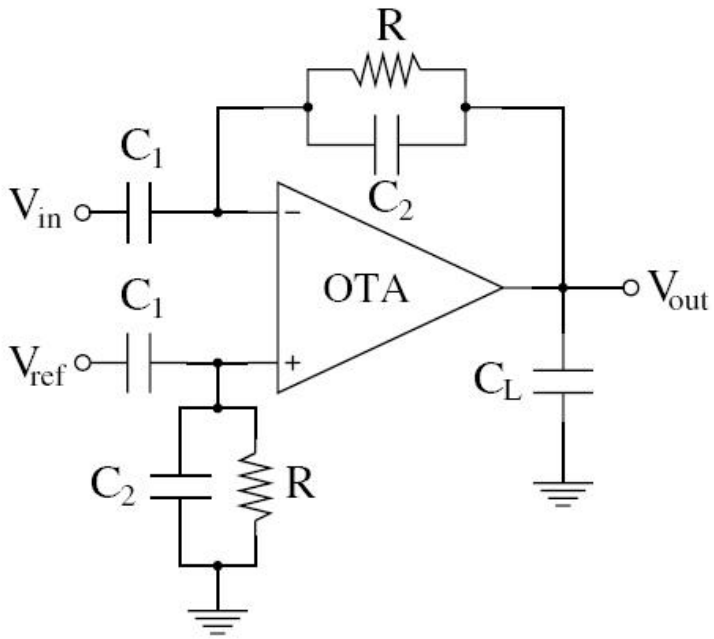

Figure 2.9: Schematic diagram of Harrison bandpass filter with RC feedback.

2.3.1 MOS-bipolar pseudoresistor

Connecting a PMOS transistor as in Figure 2.10, it is possible to obtain a device that works as resistance, in a definite condition of polarization.

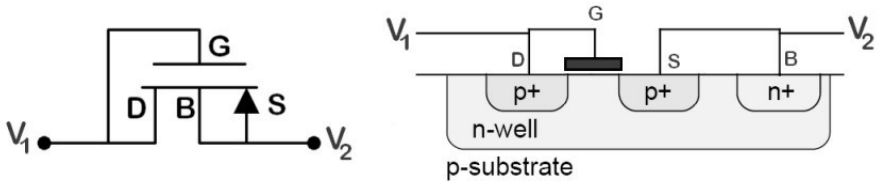

Figure 2.10: I-V relationship and incremental resistance of MOS-bipolar pseudoresistance.

The PMOS transistor is used in a configuration in which the Drain and Gate are shorted, and the Bulk is connected to the Source.Depending on the polarization the transistor can work as:

diode connected MOS when $V_1 < V_2$, the current for subthreshold MOS transistors is proportional to $I \propto e^{\frac{\kappa V}{V_T}}$.

diode connected BJT when $V_1 > V_2$, the p+/n emitter-base junction is forward biased, the collector is shorted with base, and the current is proportional to $I \propto e^{\frac{V}{V_T}}$.

In the formulas appears the thermal voltage, $V_T = \frac{k_b T}{q}$ where q is the electron charge ($1.6 \times 10^{-19} C$), k_b is the Boltzmann's constant ($1.38 \times 10^{-23} \frac{m^2 kg}{s^2 K}$), and T is the absolute temperature. At room temperature ($T = 300K$), $V_T = 26mV$.

The experimental I-V relationship in the region close to $0V$ is constant with a value of few pA. For $\mid \Delta V \mid < 0.2V$ the measured incremental resistance is $r_{inc} = \frac{dV}{dI} > 10^{11}\Omega$.

Putting two MOS-bipolar devices in series it is possible to reduce the distortion for large output signals.

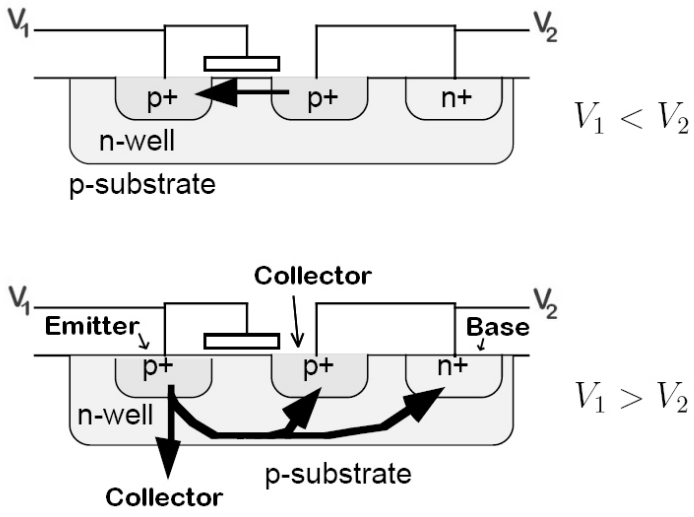

Figure 2.11: Scheme of MOS-bipolar pseudoresistance.

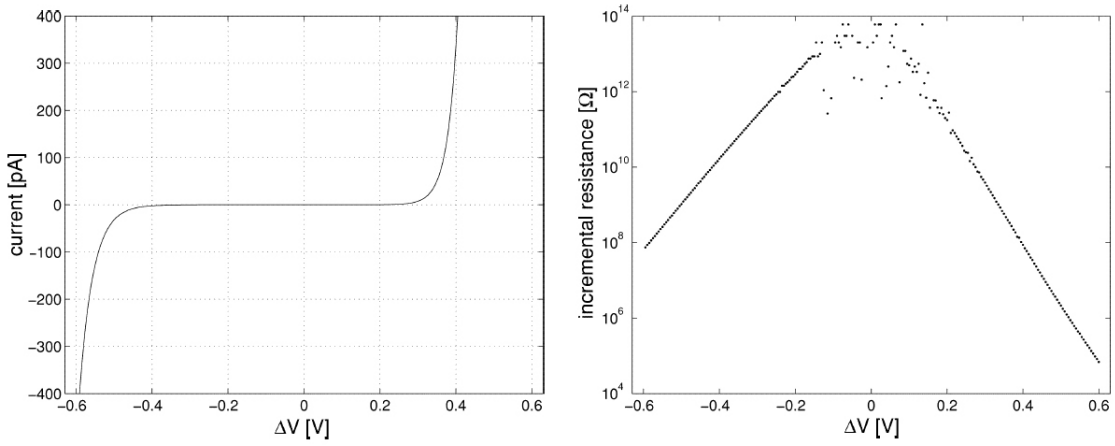

Figure 2.12: I-V relationship and MOS-bipolar pseudoresistance [8].

2.3.2 OTA design

The choose of the OTA (Operational Transconductance Amplifier) to use in the preamplifier architecture is driven by low noise, high gain and low power requirements.

The ideal gain of the preamplifier is:

$$A_{vM}^{ideal} = \lim_{A_{v0}^{OTA}\to\infty} A_{vM} = \lim_{A_{v0}^{OTA}\to\infty} \frac{A_{v0}^{OTA}(sC_1R)}{(A_{v0}^{OTA}+1)(sC_2R+1)+sC_1R} = \frac{C_1}{C_2} \tag{2.4}$$

when the OTA open loop gain is infinite (A_{v0}^{OTA}). In the real case A_{vM} differs from the ideal value A_{vM}^{ideal}, because the OTA open loop gain has a finite value. The error on the total gain is:

$$err(A_{vM}) = \frac{A_{vM}^{ideal} - A_{vM}}{A_{vM}^{ideal}} \tag{2.5}$$

We can rewrite Equation 2.4 as:

$$A_{vM} = \frac{A_{v0}^{OTA}(sC_1R)}{SR(A_{v0}^{OTA}sC_2 + C_1 + C_2) + 1} \approx \frac{A_{v0}^{OTA}C_1}{(A_{v0}^{OTA}+1)C_2 + C_1} \tag{2.6}$$

This approximation is possible because in the bandwidth of interest $SR(A_{v0}^{OTA}sC_2 + C_1 + C_2) \gg 1$, thanks to the high value of R ($\approx 10^{12}\Omega$).

Using the definition 2.5 is possible to calculate the error in this case:

$$err(A_{vM}) \approx \frac{\frac{A_{v0}^{OTA}C_1}{(A_{v0}^{OTA}+1)C_2+C_1} - \frac{C_1}{C_2}}{\frac{C_1}{C_2}} = \frac{A_{v0}^{OTA}C_2}{(A_{v0}^{OTA}+1)C_2 + C_1} - 1 \tag{2.7}$$

Let us consider $A_{v0}^{OTA} = 10^3$, with $C_1 = 10pF$ and $C_2 = 100fF$,

$$err(A_{vM}) \approx \frac{A_{v0}^{OTA}C_2}{A_{v0}^{OTA}C_2 + C_1} - 1 = \frac{10^3 \cdot 100fF}{10^3 \cdot 100fF + 10pF} - 1 = -0.091 \tag{2.8}$$

In table 2.3 are reported the calculated errors for different values of A_{v0}^{OTA}.

Another factor that influences the error on A_{vM} is the precision of the ratio C_1/C_2. The mismatching between the two capacitors can be reduced in order to obtain an error of 1% on the preamplifier gain.

The OTA open loop gain A_{v0}^{OTA} must be set in order to have a difference between the ideal an the real gain (see Table 2.3) at least comparable with the error due to the capacitors mismatch. This condition can be satisfied using an OTA with $A_{v0}^{OTA} = 10^4$, which can be obtained by most CMOS OTA architectures.

$A_{v0}^{OTA}[V/V]$	$A_{vM_{error}}[\%]$
10^2	-50
10^3	-9.1
10^4	-0.99
10^5	-0.10

Table 2.3: Influence of A_{v0}^{OTA} on the A_{vM} precision.

The intrinsic biological noise is around $10\mu Vrms$. Therefore to avoid increasing the noise floor the preamplifier rms noise must be at least a factor two smaller.
On the basis of these valuations, in the choice of OTA architecture the noise is the most critical parameter since a gain of 10^4 is easily achieved.
In order to determine the best solution in terms of noise, an analysis on four different OTA architectures with differential input and single-ended output is performed:

- Symmetrical OTA with cascoded output stage
- Miller OTA
- Telescopic CMOS OTA
- Folded cascode OTA

For each proposed OTA topology, a short description with circuit scheme and input equivalent noise (V_{irn}^2) is reported.

Symmetrical OTA with cascoded output stage

This configuration is made with a basic differential pair with PMOS input transistors (M1, M2).

In M10 flows the biasing current mirrored by M9. This current sets the bias of the differential pair. The transistors M3 and M4 mirror the current which flows from the input transistors in M5 and M6 respectively. Finally there is a PMOS current mirror formed by M7, M8.

The cascoded output increments the output resistance increasing the gain and creating a high frequency pole.

Equation 2.9 reports the input referred noise as function of the noise of the transistors. The transistors M1 - M2, M3 - M4, M5 - M6, M7 - M8, are considered matched in pairs.

$$V_{irn}^2 \approx 2V_{n1}^2 + \frac{1}{g_{m1}^2 r_{o,I}^2}(2V_{n3}^2 + 2V_{n6}^2 + 2V_{n8}^2 + \frac{V_{nN}^2}{g_{m6}^2 r_{dN}^2} + \frac{V_{nP}^2}{g_{m8}^2 r_{dP}^2}) \tag{2.9}$$

with $r_{o,I}^2 \approx 1/g_{m4}^2, r_{dN}^2 \approx 1/g_{dN}^2, r_{dP}^2 \approx 1/g_{dP}^2$

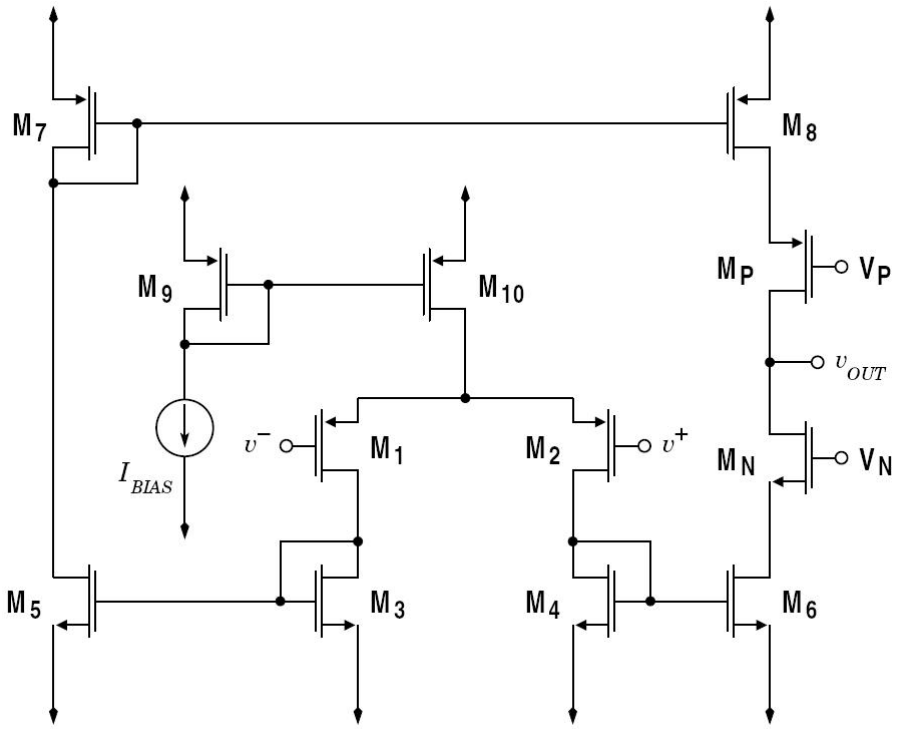

Figure 2.13: Symmetrical OTA with cascode output stage.

Miller OTA

The Miller OTA is a two stage amplifier. The first stage is a basic differential pair implemented with PMOS transistors (M1 and M2), which has a single-ended current source as active load implemented with NMOS transistors (M3 and M4). This stage is biased with the current mirror formed with PMOS transistors M7 and M8, whose reference current source is I_{bias}.
The second stage is a basic common source amplifier with an NMOS transistor (M5) acting as amplifier and a PMOS transistor (M6) acting as a current source load.
The OTA is usually compensated with a capacitor which feedback the output signal at the gate of M5 transistor. Equation 2.10 reports the input referred noise as function of the noise of the transistors. Transistors M1 - M2, M3 - M4, are considered matched in pairs.

$$V_{irn}^2 \approx 2V_{n1}^2 + 2\frac{g_{m3}^2}{g_{m1}^2}V_{n3}^2 + \frac{1}{g_{m1}^2 r^2 o, I}(V_{n5}^2 + \frac{g_{m6}^2}{g_{m5}^2}V_{n6}^2) \tag{2.10}$$

with $r_{o,I}^2 \approx 1/g_{m4}^2$

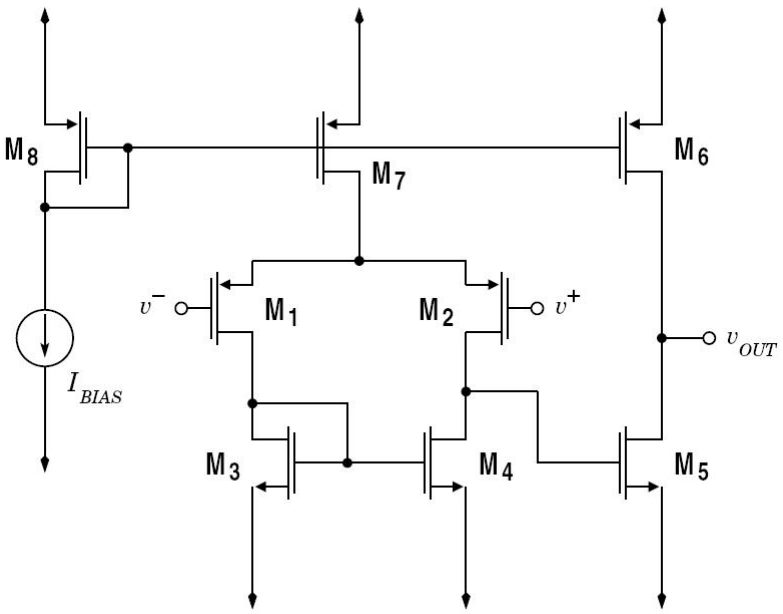

Figure 2.14: Miller OTA.

Telescopic CMOS OTA

This configuration is a single stage cascoded OTA, it presents a differential stage with a high gain.

Cascoding the output, the output resistance can be increased of 2 order, increasing the gain which is proportional to it.

The current mirror load (M5 - M6, M7 - M8) is known as "wide swing cascode", it improves the dynamic range better than a basic cascode.

One of the disadvantages is the reduction of the input common mode range, because of the extra voltage drops required by the cascode transistors.

There is only one dominant pole, due to the high resistance at the output stage.

Equation 2.11 reports the input referred noise as function of the noise of the transistors. Transistors M1 - M2, M5 - M6 are considered matched in pairs, the other transistors noise contribution are negligible.

$$V_{irn}^2 \approx 2V_{n1}^2 + 2\frac{g_{m6}^2}{g_{m1}^2}V_{n6}^2 \tag{2.11}$$

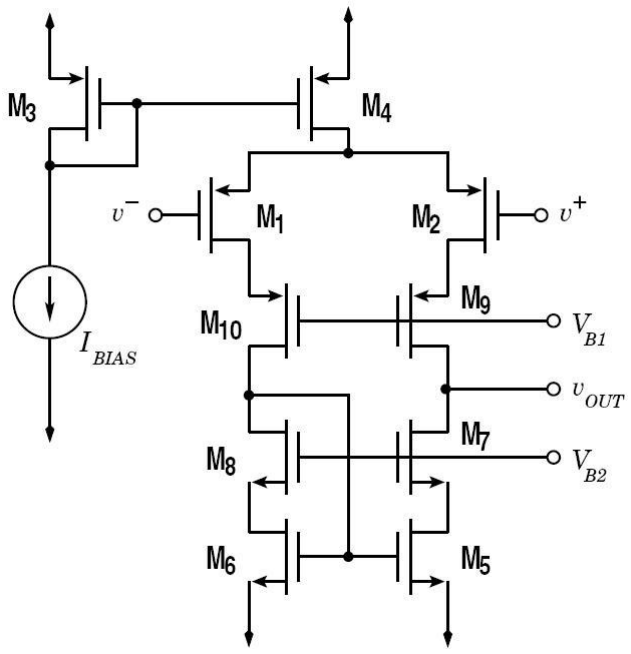

Figure 2.15: Telescopic cacode OTA.

Folded cascode OTA

The Folded cascode OTA is a two stage amplifier which has an improved common mode range and power supply rejection. The folded cascode OTA has an input differential transcoductrance stage (M1, M2) with a current stage (mirror connected M6, M7), and a cascoded output. There are two bias currents, one to bias the differential stage, one for the current stage, and two bias voltages to bias the gates of cascode transistors.

This particular implementation of the input stage improves the input common mode range. The output cascode increases the output resistance and the gain of the second stage.

Equation 2.12 reports the input referred noise as function of the noise of the transistors. Transistors M1 - M2, M6 - M7, M12 - M13, are considered matched in pairs, the other transistors noise contribution are negligible.

$$V_{irn}^2 \approx 2V_{n1}^2 + 2\frac{g_{m6}^2}{g_{m1}^2}V_{n6}^2 + 2\frac{g_{m12}^2}{g_{m1}^2}V_{n12}^2 \tag{2.12}$$

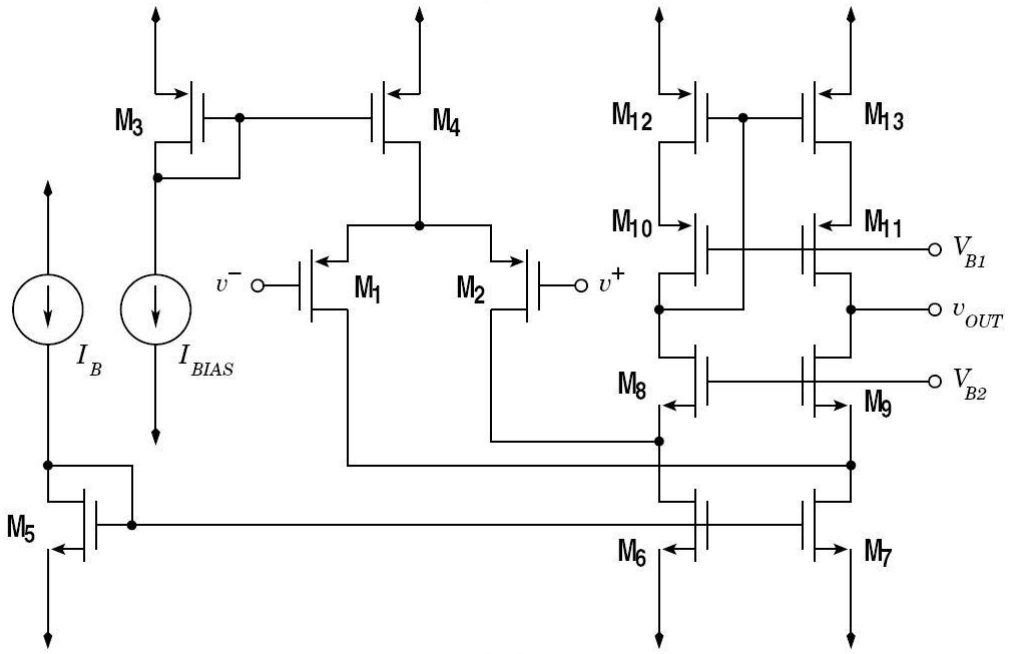

Figure 2.16: Folded cascode OTA.

2.3.3 Performance

The best topology is the symmetrical OTA, since its noise is dominated by the differantial pair which has a high gain. With a high gain of the differential pair ($A_{v_I} = g_{m1}^2 r_{o,I}^2$) Equation 2.9 becomes:

$$V_{irn}^2 \approx 2V_{n1}^2 \tag{2.13}$$

It is possible to remove the two output stage cascode devices, saving space, with a tollerable gain loss.

In Table 2.4 the performance of two different designs are reported. For Harrison design these are measured values; for the Bottino-Valle case only simulated values are available.

	Harrison	Bottino-Valle
Technology	AMI ABN $1.5\mu m$	AMS $0.35\mu m$
Supply voltage	$\pm 2.5V$	$\pm 1.65V$
Supply current	$16\mu A$	$10\mu A$
Gain	$39.5dB$	$40dB$
f_L	$25mHz$	$400mHz$
f_H	$7.2kHz$	$11kHz$
V_{irn}	$2.1\mu V$	$3.35nV$
Power dissipation	$80\mu W$	$24\mu W$

Table 2.4: Performance summary of Harrison [8] and Bottino-Valle [9] implementations.

Figure 2.17 reports the measured transfer function of Harrison preamplifier, and the measured input-referred voltage noise spectrum. The flicker noise corner is at $100Hz$ and the thermal noise level is $21nV/\sqrt{Hz}$. The total input referred noise ($V_{irn} = 2.1\mu V$) is obtained through an integration from $0.5Hz$ to $50kHz$.

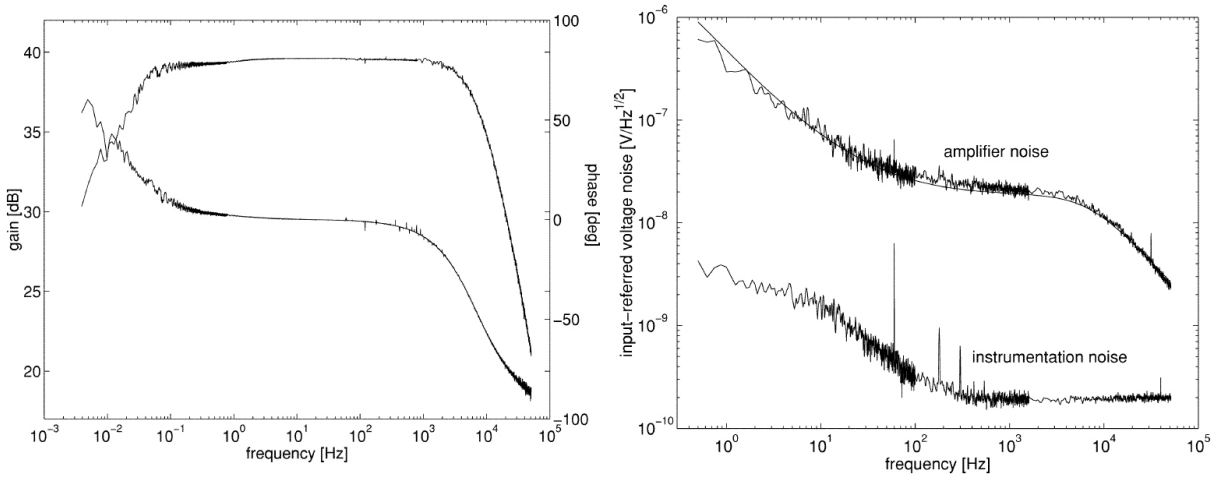

Figure 2.17: Measured transfer function and input referred voltage noise spectrum for Harrison preamplifier (AMI ABN 1.5μm) [9].

2.4 Chopper technique to reduce flicker noise

The architecture proposed by Uranga [10] exploits the chopper technique to reduce the amplifier noise.

In the chopper amplifier the input signal is first modulated in amplitude with a carrier signal at a frequency f_c and then passed through the preamplifier and a band pass filter centered at f_c. Finally the signal is demodulated and filtered with a low pass filter.

The input noise is due mainly to the flicker noise, with the modulation process this

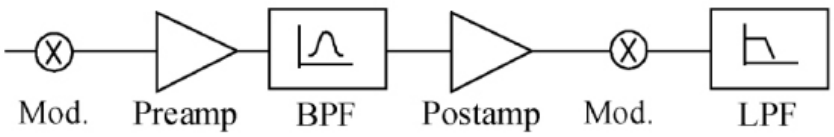

Figure 2.18: Analog processing chain of the chopper amplifier.

noise is converted in white spectrum noise, improving the signal to noise ratio.

2.4.1 Modulator an Demodulator

The modulator is composed by 4 NMOS as shown in Figure 2.19. The transistors

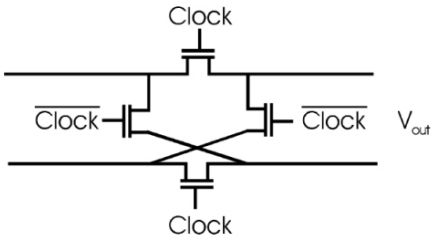

Figure 2.19: Scheme of modulator.

work as switches and each gate is connected to a clock signal.

The modulator and the demodulator are driven from the same clock because between these two stages there is not phase shifting in the signal.

The time constants of spikes due to the charge injections must be smaller than the copper period: $\tau = R_{on}C_{in} \ll T_c = \frac{1}{f_c} = 40\mu s$, where R_{on} is the channel resistance when the NMOS is switched on, and C_{in} is the amplifier input capacitance.

The spikes frequency will be higher than the chopper frequency, so is possible to eliminate the spikes with a bandpass filter.

2.4.2 Preamplifier

The preamplifier is composed by 2 stages:

1. transconductance input stage (M1, M2), in fully differential configuration.

2. transimpedance output stage (M3, M4), in folded cascode configuration.

The preamplifier gain is proportional to the g_{m1}/g_{m2} ratio, where g_{m1} is the channel transconductance of the first stage and g_{m2} is the channel transconductance of the second stage.

The thermal noise is inversely proportional to g_{m1}, which must be maximized. At the same time to obtain a high gain is necessary to maximize the g_{m1}/g_{m2} ratio, minimizing g_{m2}. In the first stage, sizing opportunely M1 and M2 ($W/L = 900/6, I_D =$

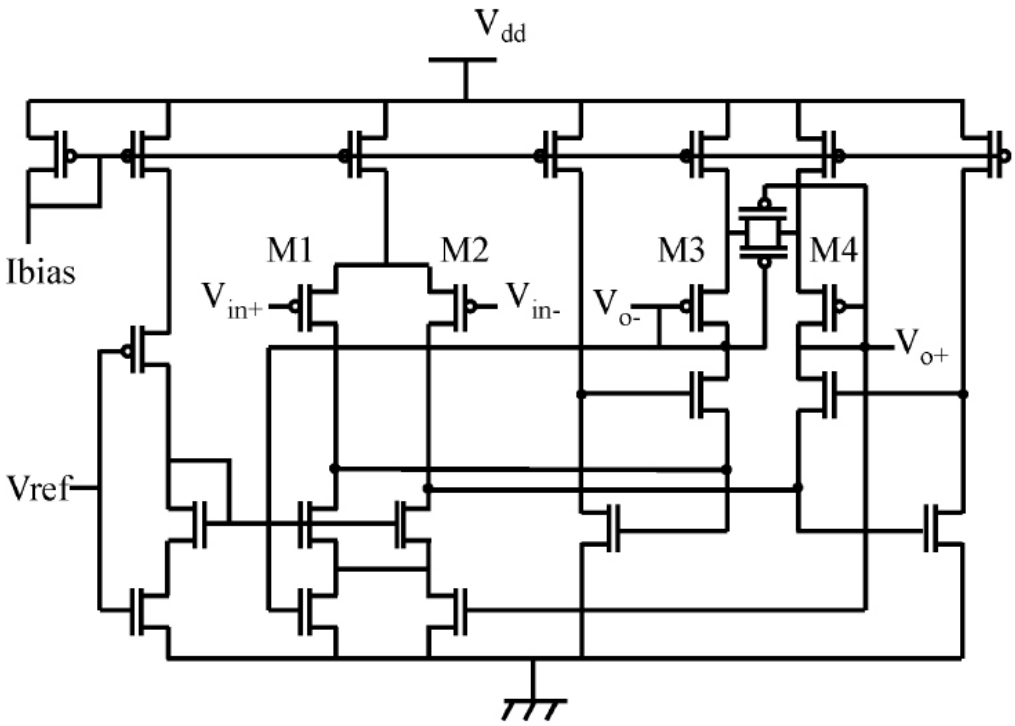

Figure 2.20: Scheme of the preamplifier.

$60\mu A$) the channel conductance value becomes $g_{m1} = 1.082\frac{mA}{V}$. In the second stage through two voltage controlled degenerate resistors it is possible to obtain a very low value for the channel transconductance ($g_{m2} = 20.8\frac{\mu A}{V}$) for M3 and M4 MOS transistor.

2.4.3 Bandpass and Low Pass Filters

After the preamplifier there is the band pass filter. The passing band is centered on the chopper frequency ($f_c = 25KHz$), with a bandwidth of $10kHz$, in this way is possible to eliminate the spikes produced by the modulator's switches. The low pass filter is the last stage of the chain and gets in input the signal from the demodulator. The cut-off frequency is set at $4kHz$ and the DC gain is $28dB$. Both the band pass and low pass filters are designed with the g_m/C technique.

2.4.4 Performance

The chip is implemented in a standard $0.7\mu m$ CMOS technology (one poly, two metals, self aligned twin-well CMOS)

Figure 2.21 reports the full chopper amplifier frequency response. The DC gain is $74dB$. In order to eliminate the DC component it is possible to implement an external high pass filter ($R = 1\mu F$, $C = 1.5k\Omega$) that rejects the signals below $100Hz$ improving the signal to noise ratio. In Figure 2.22 is shown the measured input-

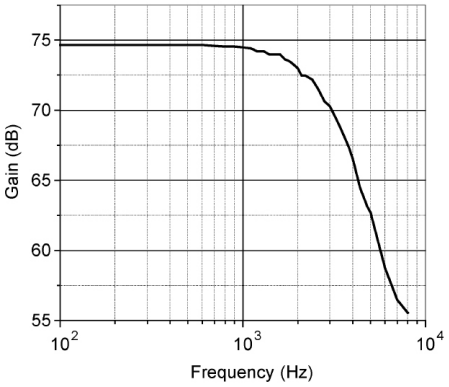

Figure 2.21: Measured chopper amplifier frequency response [10].

referred voltage noise spectrum. The average value is $6.6nV/\sqrt{Hz}$, and the total integrated noise in the $3kHz$ bandwidth is $453nV$.

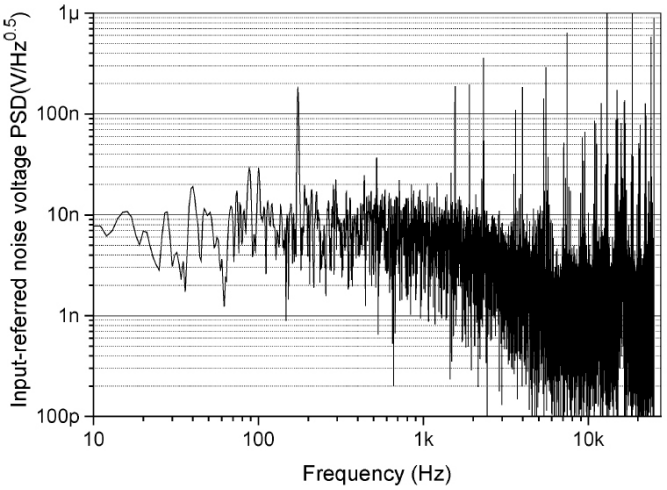

Figure 2.22: Measured chopper amplifier noise spectrum [10].

2.5 Perelman-Ginosar Architecture

The architecture proposed by Perelman-Ginosar [11] has two particular characteristics:

1. separation of the signal into a low-frequency local field potential (LFP) and high-frequency spike data (SPK), with two different analog processing chains;
2. digitally controllable Variable Gain Amplifier (VGA) with selectable offset, gain, and cut-off frequency.

The chip is implemented in AMS $0.35\mu m$ CMOS technology, with 12 recording channels.
Local Field Potential (LFP) occupies the frequencies below 100Hz. This potential is a result of the sum of electrical activity of cells within approximately $50\mu m - 350\mu m$ from the tip of the electrode and it carries important information about neural tissue activity.

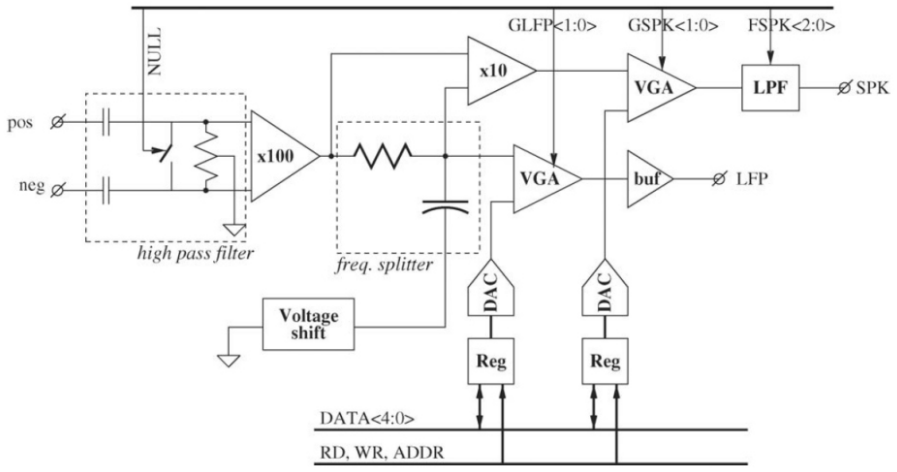

Figure 2.23: A single channel block diagram.

In Figure 2.23 it is shown a single channel diagram block. The input signal passes through an high pass filter which cuts the DC component of the signal. The corner frequency f_H should be of several hertz in order to pass the LFP part of the signal intact.

The resistors used in the high pass filter ($8M\Omega$) are integrated on chip, the capacitors are too big to be integrated and are external.
Because of the high time constants if a strong signal saturate the recording channel, it may take long time to settle back. In order to avoid this problem a digitally controlled switch is used to shorts circuits the resistance, nulling the filter output.
The frequency splitter introduces a thermal noise in the signal due to the resistance, $V_{n,rms} = \sqrt{4k_bTRf_0} = 28\mu V$ (considering a band $f_0 = 10kHz$, and $R = 5M\Omega$). An amplifier has been added before the frequency splitter to reduce the input referred noise: with a gain of $40dB$ the input referred noise due to the resistance becomes $0.28\mu V$.
The splitting frequency is set around $200Hz$, by a first order RC filter with a resistance of $5M\Omega$ (high resistive poly) and a capacitance of $150pF$ (gate oxide capacitor).
The frequency splitter act as:

- low pass filter: if the signal is taken across the capacitor, the signal passes to the spike (SPK) processing chain.
- high pass filter: if the signal is taken across the resistance, the signal passes to the Local Field Potential (LFP) processing chain.

The low frequency LPF signal is amplified by a variable gain amplifier (VGA) and then buffered, with a maximum gain of $60dB$.
The high frequency SPK signal pass through two gain stages. The first stage has a an amplification of $20dB$. The second stage has variable gain and the total maximum gain is $80dB$. Finally the signal is filtered with a second order Bessel Low pass filter.
In Figure 2.24 the chip architecture is shown. The controller selects through a multiplexer the cannel output which has to be compared with the reference potential, and receives the result of the comparison. Then the controller stores digitally the compensation value in the register of the channel which has to be calibrated. This value is converted in analog signal and passed to the negative input of VGA.

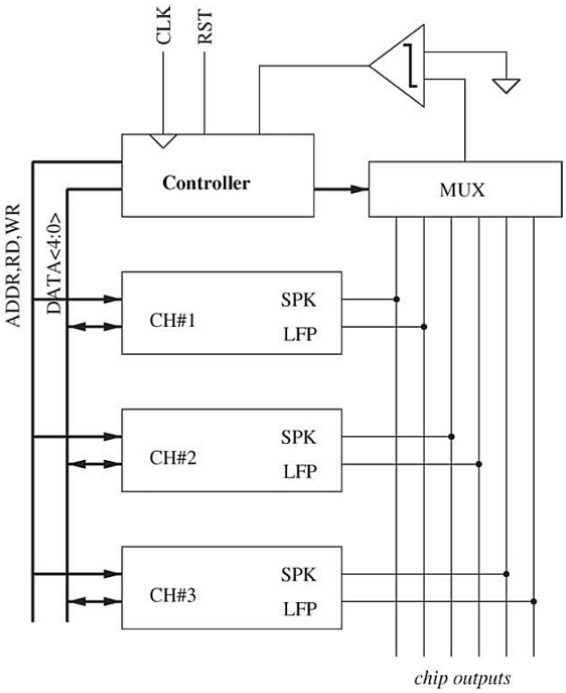

Figure 2.24: Chip architecture.

Measurement result

In Table 2.5 are reported the results of the test performed on the chip fabricated using AMS $0.35\mu m$ quad-metal, double poly CMOS process with 3.3 V power supply.

SPK gain	$77dB$
LFP gain	$58dB$
SPK noise (RMS)	$3.1\mu V$
LFP noise (RMS, above 1 Hz)	$5\mu V$
Output offset (highest gain)	$< 50mV$
Channel power	$3.3mW$
Output LPF cutoff	$8 - 13kHz$
Band splitter frequency	$330Hz$

Table 2.5: Electrical test results summary [11].

Figure 2.25 shows the frequency response and input referred noise spectrum for SPK and LPF processing chains. Figure 2.26 presents an in vivo recording segment with a close up on a large spike.

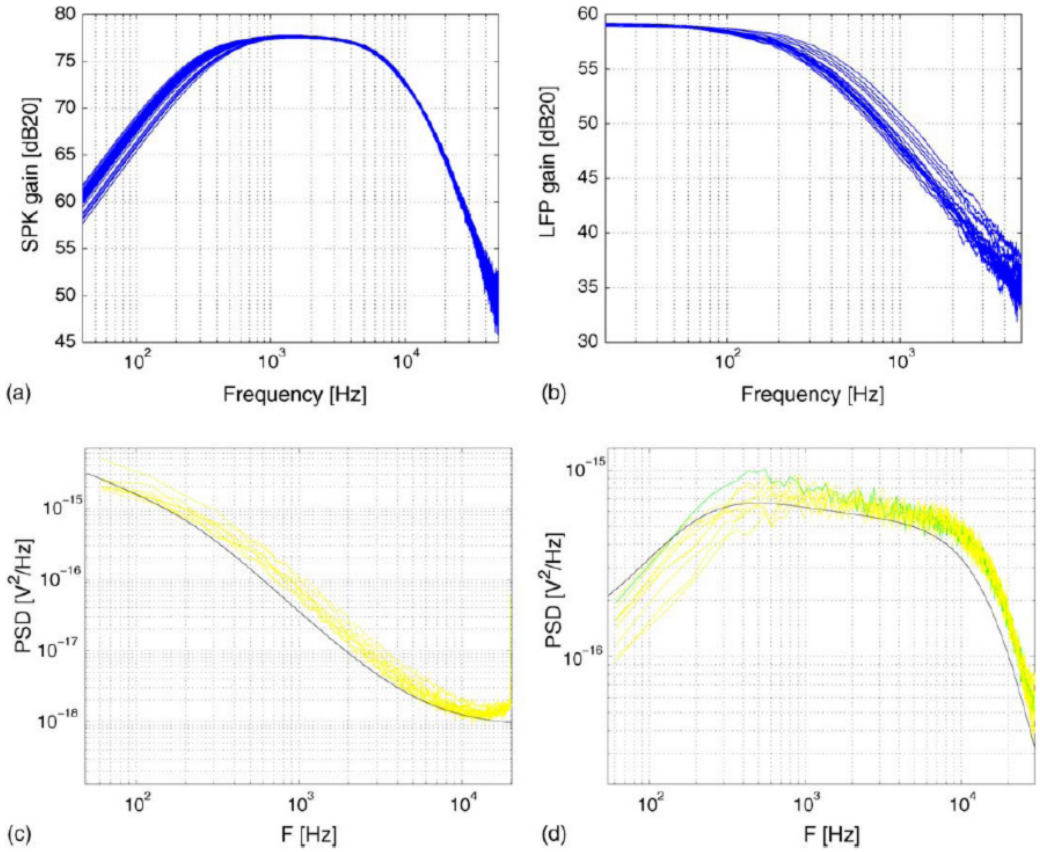

Figure 2.25: (a) and (b) SPK and LFP frequency response, (c) and (d) SPK and LFP input referred noise spectrum [11].

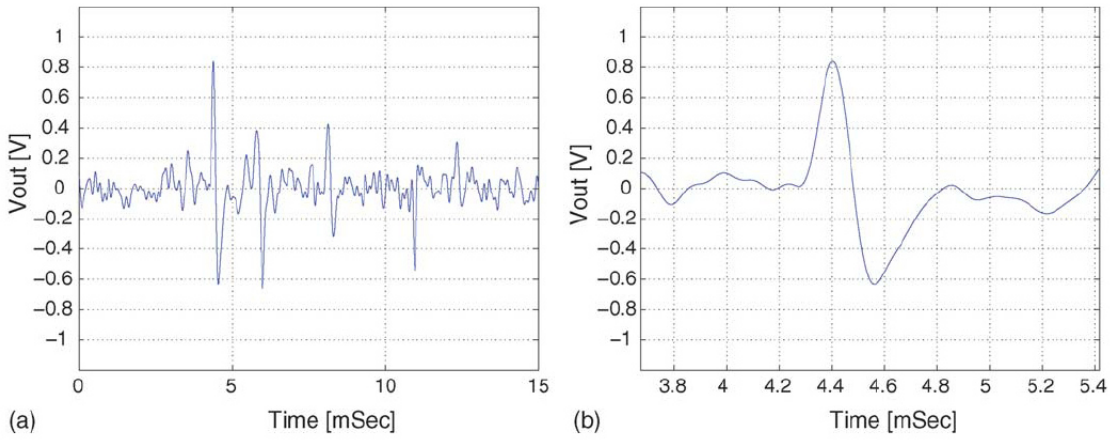

Figure 2.26: In vivo measurement: (a) signal segment; (b) close up on a large spike [11].

2.6 Choice of the architecture for the diamond sensors

A comparison between the different architectures introduced in this Chapter is useful to choose the best solution for our application. In Table 2.6 the basic parameters of the architectures are summarized.

Referenece	NEURO32	Harrison $^{\diamond}$	Uranga	Perelman
Technology	$1.5\mu m$	$1.5\mu m$	$0.7\mu m$	$0.35\mu m$
Supply voltage	$5V$	$5V$	$3.3V$	$3.3V$
Area occupation	$0.35mm^2$ $^{\triangle}$	$0.16mm^2$	$0.3mm^2$ $^{\triangle}$	-
Power consumption	$1700\mu W$ $^{\triangle}$	$80\mu W$	$965\mu W$	$3300\mu W$
IN-referred noise	$3\mu V_{rms}$	$2.1\mu V_{rms}$	$453nV_{rms}$	$3.1\mu V_{rms}$

$^{\triangle}$ indicates the value is relative to the recording channel and not only to the preamplifier.

$^{\diamond}$ For Harrison architecture the simulated values are reported.

Table 2.6: Performance summary of four recent interface implementations for neuropotential recording.

Perelman architecture, although interesting for the signal separation and for the automatic DC offset calibration, was not chosen because of application issues regarding large component values and high power dissipation.
Uranga architecture has the lowest noise but it exploits the chopper technique, which is not a standard and widely tested method in neural amplifiers.
Neuro32 chip has a low noise level, a high output swing, it permits to tune externally the upper and the lower corner frequency. However this system employs in several points amplifiers with relatively low open-loop gain and it uses a fairly complex approach to implement the AC coupling between subsequent stages. For our application we have preferred to use a preamplifier based on the Harrison scheme followed by a DC coupled g_m/C filter.
In fact, as it will be discussed in more detail in Chapter 3 the Harrison approach allows to implement a high pass filter with very low cut off frequency in a small silicon area.
The DC coupling between the filters allows a more compact design.

Figure 2.27 shows a block scheme of our chain.

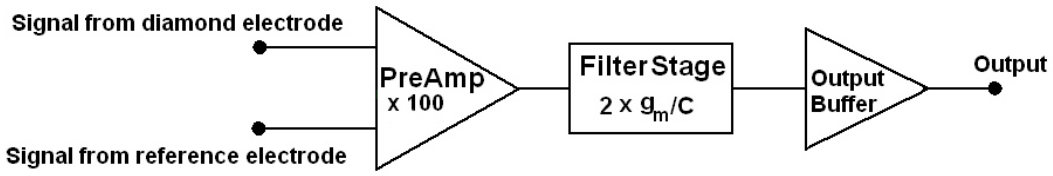

Figure 2.27: Analog processing chain.

Each channel contains a preamplifier with a gain of 100, two cascaded g_m/C filtering cells, and an output buffer.
To design our circuit we use $AMS0.35\mu m$ technology, with a supply voltage selectable among $3.3V$ and $0V$ or $1.65V$ and $-1.65V$.

Chapter 3

Low Noise Low Power Preamplifier

The preamplifier is the first component of AFE. Its design is the most critical one, because it receives the signal directly from the microlectrode and has strong constraints on noise, power consumption and size.
In this chapter the Preamplifier design is discussed, and the results of the simulations of the schematic circuit are reported. A short overview of the simulation environment used is given at the beginning of the Chapter.

3.1 Introduction to the simulator enviroment

In this work Cadence is used as graphical tool for circuit design and Analog artist to run simulations with AMSC035 libraries. There are three kinds of possible simulations:

- DC (Direct Current) simulation analyzes the static operating points (DC voltages and currents) of a circuit. For the MOS transistors it gives the values for the small signal model parameters.
- In the AC (Alternate Current) simulation the simulator uses a linearized model for the nonlinear components, and it gives the response in the frequency domain of the circuit. The results are valid only for small signals around the DC

operating points.

- The transient simulation gives the response of the circuit in the time domain.

All simulations start calculating an estimation of the DC operating points using the DC equivalent model of the circuit (see diagram in Figure 3.1). In the AC simulation the DC node voltages are essential to know the operating point of non linear circuit elements. In the transient simulation the DC operating point are used as an initial estimate to solve the time dependent equations.

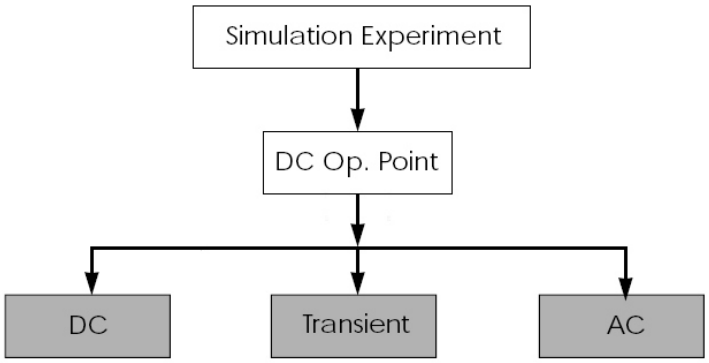

Figure 3.1: Diagram of possible simulations.

3.1.1 Process fluctuation

For the design of robust circuits, one aspect is the accurate modeling of the process variation and its inclusion within silicon foundry simulation libraries. There exist two standard approaches for analyzing process variation: worst case method and Monte Carlo method.

Worst case method

The foundries give different simulations models for designing integrated circuits which take in to account of the process fluctuations the electrical parameters.
The simulations are usually effectuated with the "Typical Mean (TM)" model, which

uses the model of the standard process, but in some cases due to production tolerances the physical model of the electrical components has to be changed. There are two extreme cases:

- Worst Power (WP), there is a worsening of the dissipated power and a reduction of the delays in the signal propagation. In the MOS transistors the mobility of the charge carriers increases and the threshold voltage decreases.
- Worst Speed (WS), the delay in the signal propagation increases but it is compensated by low power dissipation. In the MOS transistors the mobility of the charge carriers decreases and the threshold voltage increases.

In the worst cases the circuit component parameters are varied simultaneously as reported in Table 3.2. A corner analysis is a set of simulations in which the circuit is simulated over multiple corners of the process (TM, WP, WS), power supply, and temperature. These analysis permit to study, with only a few simulations run, the process dependent variation of the performance of the designed circuit.

In Figure 3.2 the graph represent typical statical fluctuation of the the threshold voltage for NMOS (V_{ton}) and PMOS (V_{top}) transistors.

Monte carlo - Process

The process fluctuations can be represented to the simulator also as statistical distributions, which can be used in the Monte Carlo simulation.
In the Monte Carlo simulation the circuit is simulated several times by randomizing new values for each parameter. The values for each parameters are taken from a statistical distribution conforming to the process specification.
In this way it is possible to obtain a more reliable simulation which takes in to account of many cases and not only the worst ones. For example it is possible to know how is frequent a typical process, and how many times a worst case occurs. On the other hand this simulations take much more time that the corner analysis.

Parameter	Worst Power	Worst Speed
v_{th0}	min	max
x_w	max	min
x_l	min	max
t_{ox}	min	max
μ_0	max	min
n_{sub}	min	max
n_{ch}	min	max
r_{sh}	min	max

Table 3.1: Variation of basic MOS parameters in the WP and WS cases.

- v_{th0} is the threshold voltage for long and wide transistor;
- x_l is the effective channel length for a small channel transistor;
- x_w is the effective channel width for a narrow channel transistor;
- t_{ox} is the gate oxide thickness;
- μ_0 is the effective mobility;
- n_{sub} is the substrate doping;
- n_{ch} is the channel doping;
- r_{sh} is the n-diffusion and p-diffusion sheet resistance;

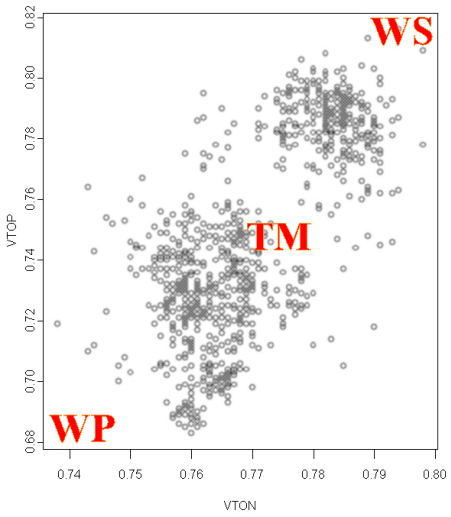

Figure 3.2: Typical values of the threshold voltage for NMOS (V_{ton}) and PMOS (V_{top}) transistors

Monte carlo - Mismatch

With the Monte Carlo analysis it is also possible to simulate the mismatch between the circuit components.

The analysis of the process fluctuations (Corner and Monte Carlo Process Only analysis) does not account for the variation of the transistor electrical parameters within the same die. Therefore for a fabricated die, all transistors will have the same model.

But in reality, because of the random fluctuation which occur during the chip fabrication phase, the dimensions and other important properties of transistors and passive components are not reproduced with absolute precision, so there could be some variation from the designed values.

As defined in [13] mismatch is the process that causes time-independent random variations in physical quantities of identically designed devices. This variations are modelized by a statistical function.

The variance of the electrical parameter P between two identical transistors sized W/L with mutual distance D, can be written in a general form as:

$$\sigma^2_{\Delta P} = \frac{A^2_P}{WL} + S^2_P D^2 \tag{3.1}$$

where A_P is the area proportionality constant for parameter P and S_P describes the variation of parameter P with the spacing.

In figure 3.3 a scheme of possible simulation for process fluctuations and mismatch analysis is shown.

Figure 3.3: Scheme of possible simulation for process fluctuation and mismatch analysis

3.2 Preamplifier design

The preamplifier employs the architecture proposed by Harrison (see Paragraph 2.3). The circuit is based on a operational amplifier with high open loop gain and a negative feedback network formed by poly-to-poly capacitors.

3.2.1 Preamplifier specifications

From the general review of Chapter2 it is possible to set the followings requirements for the preamplifier:

- Differential input and single ended output.
- Passing band between $10Hz$ and $10kHz$, eliminating the large DC component due to the electrode-electrolyte interface.
- High gain ($\geq 40dB$).
- High input resistance ($\gg 400k\Omega$), so that the microelectrode resistance is negligible.
- High common mode rejection ratio (CMRR $\geq 60dB$).
- Low noise ($\approx 1\mu W$).
- Low power dissipation ($\approx mW$) in order to avoid the heating of the cells.
- Small silicon area ($0.10mm^2$).

Harrison architecture using bipolar-MOS achieves a very small high pass cut off frequency occupying a small silicon area on the chip. It also has a very low noise level, and a low power dissipation, with great chance of improvement because it is possible to redesign separately the OTA. This architecture is the best choice for our purpose.

3.2.2 OTA Design

The architecture chosen for the OTA is the symmetrical OTA (see Paragraph 2.3.2). Initially simulations were performed using the symmetrical OTA with and without cascoded output. The noise level was the same. Since the gain was already adequate without the output cascode devices we decided to remove them in order to have more compact design.

In Figure 3.4 the schematic diagram of the symmetrical OTA is shown.

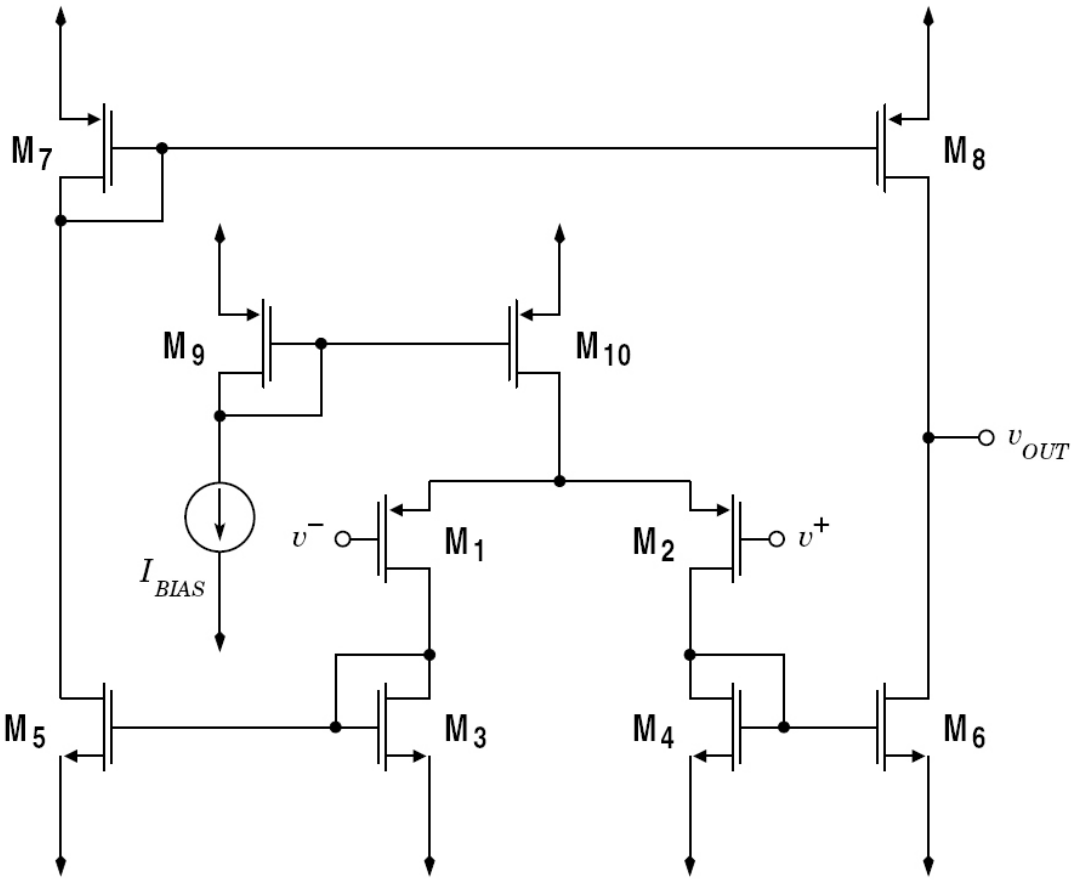

Figure 3.4: Schematic diagram of the symmetrical OTA.

Setting $I_{bias} = 6\mu A$ and sizing equally M9 and M10, in M1 and M2 flows $3\mu A$, and this current is mirrored in M5 by M3 and in M6 by M4.

The total current is $I_{tot} = 18\mu A$, the power consumption of the OTA is:

$$P_{ota} = V_{supply} \cdot I_{tot} = 3.3V \times 18\mu A = 59.4\mu W \tag{3.2}$$

The MOS transistors has to be sized in order to reduce the noise.
At low frequencies the main noise component is the flicker noise (known also as 1/f noise). For a MOS transistor the flicker noise expression is:

$$V_n^2 = \frac{K_f}{WLC_{ox}}\frac{1}{f} \tag{3.3}$$

To reduce the flicker noise it is therefore necessary to maximize the transistors gate area (WL). In the process used the PMOS flicker noise coefficient (K_{fp}) is 60 times lower than the NMOS flicker noise coefficient K_{fn}. For this reason PMOS are used as input transistors.
Although the thermal noise gives a minor contribution, it cannot be neglected. For a MOS transistor the thermal noise expression is:

$$V_n^2 = 4k_bT\frac{2}{3}g_m r_o^2 \tag{3.4}$$

For the symmetrical OTA the total input referred noise is given by the following formula:

$$V_{irn}^2 = 2V_{n1}^2 + \frac{2V_{n3}^2 + 2V_{n6}^2 + 2V_{n8}^2}{g_{m1}^2 r_{0,I}^2} \tag{3.5}$$

where the transistors M1 - M2, M3 - M4, M5 - M6 and M7 - M8 are matched in pairs. The contribution due to the thermal noise is:

$$V_{irn,thermal}^2 = [\frac{16k_bT}{3g_{m1}}(1 + 2\frac{g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}})]\Delta f \tag{3.6}$$

In order to reduce the thermal noise, the followings condition have to be satisfied: $g_{m1} \gg g_{m3}$ and $g_{m1} \gg g_{m7}$.
To minimize the flicker noise, the M1 and M2 transistors are set with an high $(W/L)_{1,2}$ ratio.
The thermal noise depends on $\frac{g_{m_{3,7}}}{g_{m1}}$, once g_{m1} is fixed with $(W/L)_1$, is necessary to reduce the value of $g_{m_{3,7}}$. To minimize g_{m3} and g_{m7}, different simulations were performed with different values for the channel length of the M3, M4, M5, M6, M7, M8 transistors (L_x). For example with $L_x = 6\mu m$, was obtained $g_{m3} = 15\mu S$.

Finally was choose $L_x = 20\mu m$ in which case $g_{m3} = 8.21\mu S$. After some simulations we set the W/L ratios reported in Table 3.2.

MOS	W/L
M1	$1000\mu m/2\mu m$
M2	$1000\mu m/2\mu m$
M3	$2\mu m/20\mu m$
M4	$2\mu m/20\mu m$
M5	$2\mu m/20\mu m$
M6	$2\mu m/20\mu m$
M7	$6\mu m/20\mu m$
M8	$6\mu m/20\mu m$
M9	$20\mu m/20\mu m$
M10	$20\mu m/20\mu m$
I_{Bias}	$16\mu A$

Table 3.2: MOS dimension.

The OTA open loop gain is given by the product of the OTA transconductance (g_m^{OTA}) with the output resistance (R_{out}):

$$g_m^{OTA} = \frac{g_{m1}}{g_{m3}} g_{m6} = \frac{78.76\mu S}{8.21\mu S} 8.23\mu S = 78.95\mu S \tag{3.7}$$

$$R_{out} = \frac{1}{g_{ds6} + g_{ds8}} = \frac{1}{12.02nS + 7.67nS} = 50.8M\Omega \tag{3.8}$$

$$A_v^{OTA} = g_m^{OTA} \cdot R_{out} = 78.95\mu S \cdot 50.8M\Omega = 4010 \tag{3.9}$$

According to Equation 2.3.2 this value leads to a close loop gain of $97.6V/V$ which is 2.4% smaller than the ideal one achievable with an infinite gain OP-AMP.

	$M1$	$M2$	$M3$	$M4$	$M5$	$M6$	$M7$	$M8$	$M9$	$M10$
c_{bb}	$1.794p$	$1.794p$	$35.72f$	$35.71f$	$35.7f$	$35.7f$	$159.7f$	$159.6f$	$541.6f$	$541.8f$
c_{bd}	$-8.21za$	$-8.214a$	$-44.55a$	$-44.55a$	$-6.355a$	$-12.12a$	$-46.02a$	$-18.66a$	$-132a$	$-567.1a$
c_{bg}	$-1.645p$	$-1.645p$	$-25.01f$	$-25.01f$	$-25.05f$	$-25.05f$	$-32.21f$	$-32.24f$	$-102.4f$	$-101.9f$
c_{bs}	$-149.7f$	$-149.8f$	$-10.66f$	$-10.65f$	$-10.64f$	$-10.64f$	$-127.4f$	$-127.4f$	$-439.1f$	$-439.4f$
c_{db}	$-11.77a$	$-11.81a$	$-45.12a$	$-45.08a$	$-10.34a$	$-16.69a$	$-147.3a$	$-70.9a$	$-506.8a$	$-1.696f$
c_{dd}	$143.3f$	$143.4f$	$593.5a$	$593.4a$	$344.1a$	$391.1a$	$1.491f$	$1.075f$	$4.82f$	$9.095f$
c_{dg}	$-143.4f$	$-143.5f$	$-622.7a$	$-622.6a$	$-361.1a$	$-413.6a$	$-1.701f$	$-1.201f$	$-5.655f$	$-10.9f$
c_{ds}	$74.66a$	$74.93a$	$74.34a$	$74.23a$	$27.35a$	$39.2a$	$357.8a$	$197.4a$	$1.341f$	$3.499f$
c_{gb}	$-1.763p$	$-1.762p$	$-1.836f$	$-1.831f$	$-1.846f$	$-1.839f$	$-63.46f$	$-63.49f$	$-219f$	$-218.4f$
c_{gd}	$-143.3f$	$-143.4f$	$-493.8a$	$-493.8a$	$-329.9a$	$-364a$	$-1.304f$	$-999.4a$	$-4.28f$	$-6.774f$
c_{gg}	$2.161p$	$2.162p$	$136.6f$	$136.6f$	$136.5f$	$136.5f$	$386.2f$	$385.8f$	$1.292p$	$1.295p$
c_{gs}	$-255.5f$	$-255.9f$	$-134.3f$	$-134.3f$	$-134.3f$	$-134.3f$	$-321.4f$	$-321.3f$	$-1.069p$	$-1.07p$
c_{jd}	$815.2f$	$815.3f$	$1.868f$	$1.867f$	$1.69f$	$1.752f$	$6.044f$	$5.671f$	$20f$	$21.76f$
c_{js}	$1.068p$	$1.068p$	$2.518f$	$2.518f$	$2.518f$	$2.518f$	$9.388f$	$9.388f$	$30.02f$	$30.02f$
c_{sb}	$-31.95f$	$-32.03f$	$-33.83f$	$-33.83f$	$-33.85f$	$-33.84f$	$-96.06f$	$-96.08f$	$-322.1f$	$-321.7f$
c_{sd}	$-3.769a$	$-3.779a$	$-55.11a$	$-55.1a$	$-7.86a$	$-14.99a$	$-140.2a$	$-56.84a$	$-408.1a$	$-1.754f$
c_{sg}	$-373.2f$	$-373.6f$	$-111f$	$-111f$	$-111.1f$	$-111.1f$	$-352.2f$	$-352.4f$	$-1.184p$	$-1.182p$
c_{ss}	$405.1f$	$405.7f$	$144.9f$	$144.9f$	$144.9f$	$144.9f$	$448.4f$	$448.5f$	$1.506p$	$1.506p$
g_{ds}	$61.03n$	$61.18n$	$14.83n$	$14.85n$	$11.5n$	$12.02n$	$9.693n$	$7.67n$	$20.11n$	$36.05n$
g_m	$78.76u$	$78.91u$	$8.211u$	$8.219u$	$8.232u$	$8.233u$	$8.859u$	$8.869u$	$23.35u$	$23.31u$
$g_{m_{bs}}$	$13.63u$	$13.66u$	$2.157u$	$2.159u$	$2.164u$	$2.164u$	$2.305u$	$2.308u$	$6.117u$	$6.105u$
i_{bulk}	$110f$	$110f$	$-12.25a$	$-12.25a$	$-12.25a$	$-12.25a$	$330.4a$	$330.4a$	$1.101f$	$1.101f$
i_d	$-2.993u$	$-2.999u$	$2.993u$	$2.999u$	$3.002u$	$3.005u$	$-3.002u$	$-3.005u$	$-6u$	$-5.992u$
i_{ds}	$-2.993u$	$-2.999u$	$2.993u$	$2.999u$	$3.002u$	$3.005u$	$-3.002u$	$-3.005u$	$-6u$	$-5.992u$
i_s	$2.993u$	$2.999u$	$-2.993u$	$-2.999u$	$-3.002u$	$-3.005u$	$3.002u$	$3.005u$	$6u$	$5.992u$
pwr	$3.735u$	$3.741u$	$3.581u$	$3.59u$	$5.874u$	$4.958u$	$4.034u$	$4.958u$	$7.082u$	$5.126u$
r_{on}	$417.1K$	$415.9K$	$399.8K$	$399.2K$	$651.7K$	$549.1K$	$447.5K$	$549.1K$	$196.7K$	$142.8K$
v_{bs}	$855.5m$	$855.5m$	0	0	0	0	0	0	0	0
v_{db}	-2.104	-2.103	1.196	1.197	1.956	1.65	-1.344	-1.65	-1.18	$-855.5m$
v_{ds}	-1.248	-1.247	1.196	1.197	1.956	1.65	-1.344	-1.65	-1.18	$-855.5m$
$v_{ds_{sat}}$	$-50.62m$	$-50.63m$	$475.9m$	$476.4m$	$475.9m$	$476.4m$	$-586.5m$	$-586.5m$	$-452.6m$	$-452.6m$
v_{gb}	-1.65	-1.65	1.196	1.197	1.196	1.197	-1.344	-1.344	-1.18	-1.18
v_{gd}	$453.6m$	$452.8m$	0	0	$-760m$	$-452.9m$	0	$306.3m$	0	$-324.8m$
v_{gs}	$-794.5m$	$-794.5m$	1.196	1.197	1.196	1.197	-1.344	-1.344	-1.18	-1.18
v_{th}	$-899.3m$	$-899.3m$	$498.7m$	$498.7m$	$498.7m$	$498.7m$	$-709.2m$	$-709.2m$	$-700.9m$	$-700.9m$

Table 3.3: Basic MOS parameters, for OTA.

Table 3.3 reports the MOS model parameters given by the DC simulation, for the transistors which constitute the OTA: the parasitic capacitance (c_{xy}), the transconductance (g_m), the body effect transconductance (g_{mb}), the current which flows through the different terminals (i_x), the channel resistance (r_{on}), the difference of potential between the different terminals (v_{xy}), the threshold voltage (v_{th}) and the saturation voltage ($v_{ds_{sat}}$).

The MOS is a 4 terminal device: "d" stand for drain; "s" stand for source; "g" stand for gate; "b" stand for bulk.

In the model is considered the junction between source/drain and external lines ("j").

OTA Stability

The next step is to study the OTA stability through the Open Loop transfer function. To test the OTA Open Loop behavior the positive and negative inputs must be properly biased (V_{DC}^{in+} and V_{DC}^{in-}).

The value of V_{DC}^{in+} is chosen in order that it stays in the input common mode range, the value of V_{DC}^{in-} is chosen at the same level of the DC output level ($V_{DC_{CloseLoop}}^{out}$) when the OTA is in Buffer configuration (see Figure 3.5).

In the simulation the difference $V_{DC}^{in+} - V_{DC}^{in+}$ is $79\mu V$.

In figure 3.11 the Bode plot of the OTA in Open Loop configuration is reported.

The Open Loop gain is $72dB$ ($A_v^{OTA} = 3980V/V$), which differs of 0.7% from the

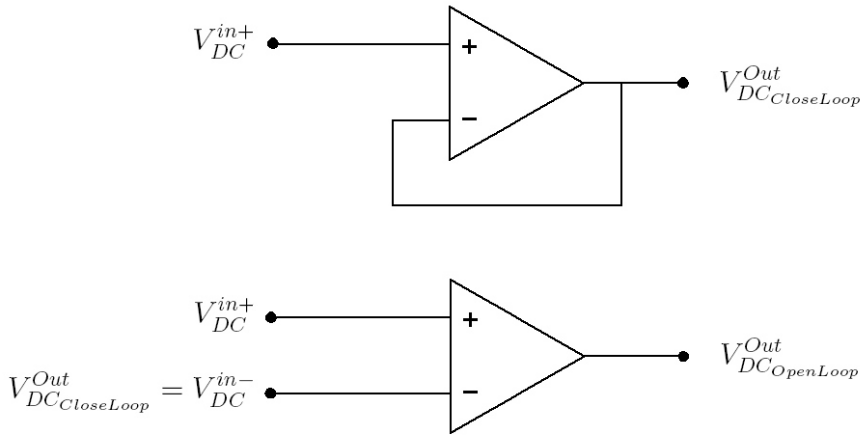

Figure 3.5: OTA Bode diagram.

value calculated with the Equation 3.7.

The low pass cut off frequency is at $f_L^{OTA} = 310Hz$, and the gain-bandwidth product is $1.231 \times 10^6 Hz$.

At $0dB$ the phase is of $-140deg$, so the Phase Margin is $PM = 40$. The low phase margin is not a problem because the OTA will be used with an high value of the gain.

In figure 3.6 the Bode plot for the OTA Open Loop gain and phase is shown.

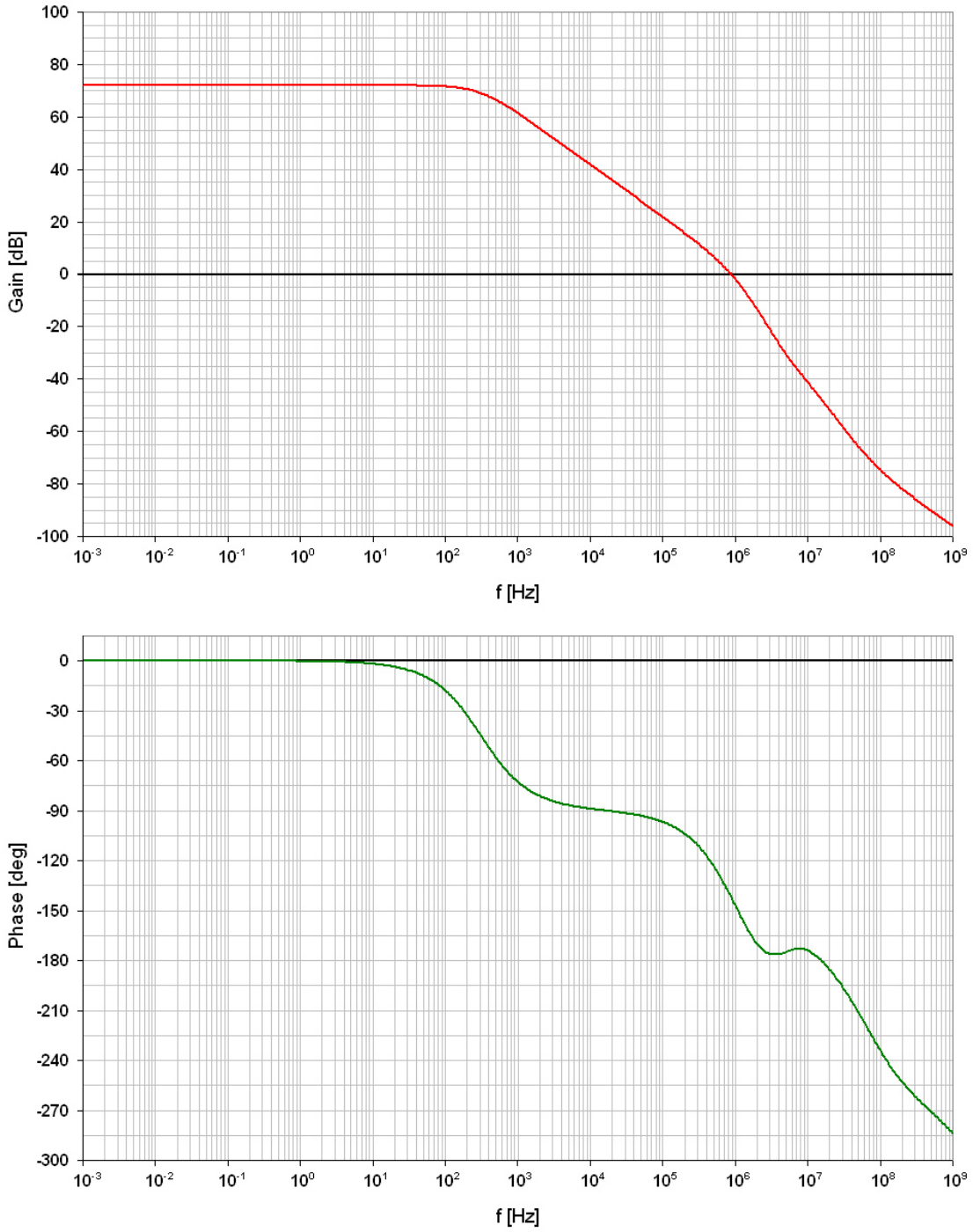

Figure 3.6: OTA Bode diagram.

3.2.3 MOS-bipolar pseudoresistor characterization

To achieve an incremental resistance of $\frac{dV}{dI} \approx 10^{12}\Omega$ in the design we used diode connected MOS transistors in series as explained in Paragraph 2.3.1.
In Figure 3.7 the device is shown. Each MOS is sized with a ratio $W/L = 2\mu m/2\mu m$.

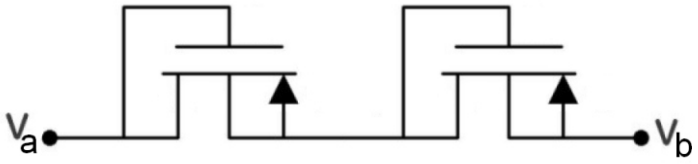

Figure 3.7: Mos-bipolar device

In Figure 3.8 the Current to Voltage relationship of the device is shown.

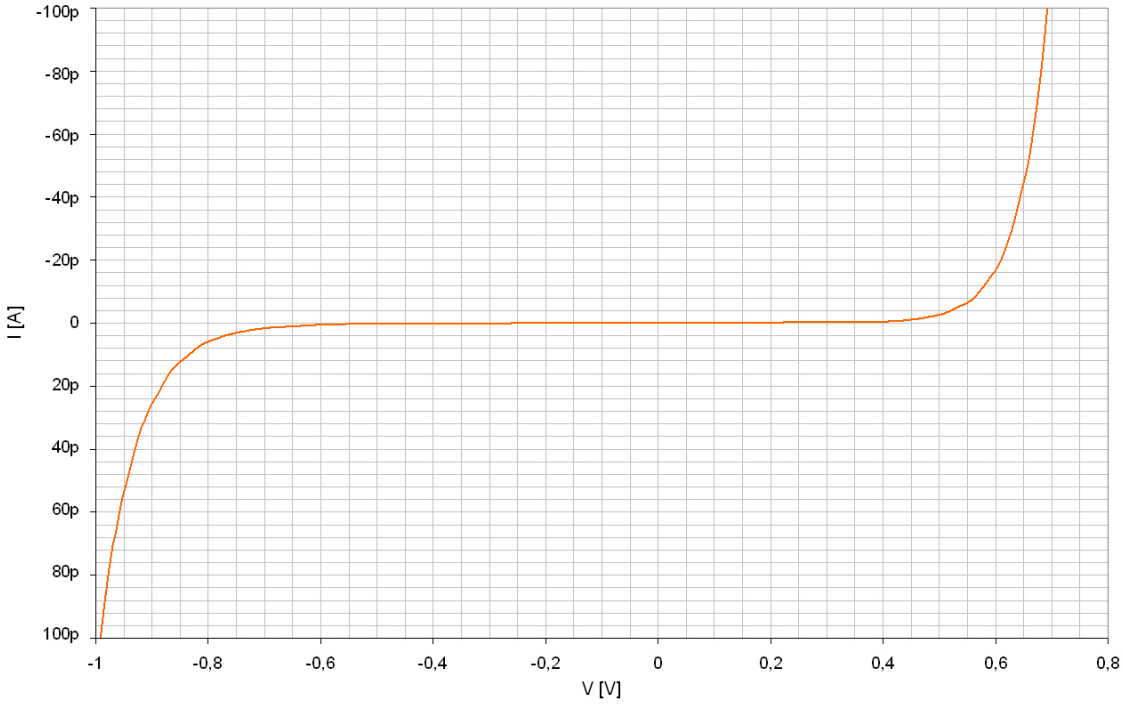

Figure 3.8: Mos-bipolar device Current to Voltage relationship

The inverse of the derivative of the Current to Voltage relationship gives the value of the incremental resistance as a function of the potential difference at the

terminals of the device: $r_{inc}(V) = (\frac{dI(V)}{dV})^{-1}$.

The device formed by $M_c - M_d$ (see Figure 3.10) has a potential difference at the terminals of $0V$. The device formed by $M_a - M_b$ connects the negative input to the output. The difference of potential at its terminals depends on the amplitude of the signal, and ranges between $-10mV$ and $5mV$. The incremental resistance value could change, considering also the worst cases, in the interval between $1.52 \times 10^{12}\ \Omega$ and $1.99 \times 10^{12}\ \Omega$.

The oscillation of the incremental resistance is not a problem because it is related only to the high pass cut off frequency.

Figure 3.9 shows the simulation of incremental resistance with worst case analysis.

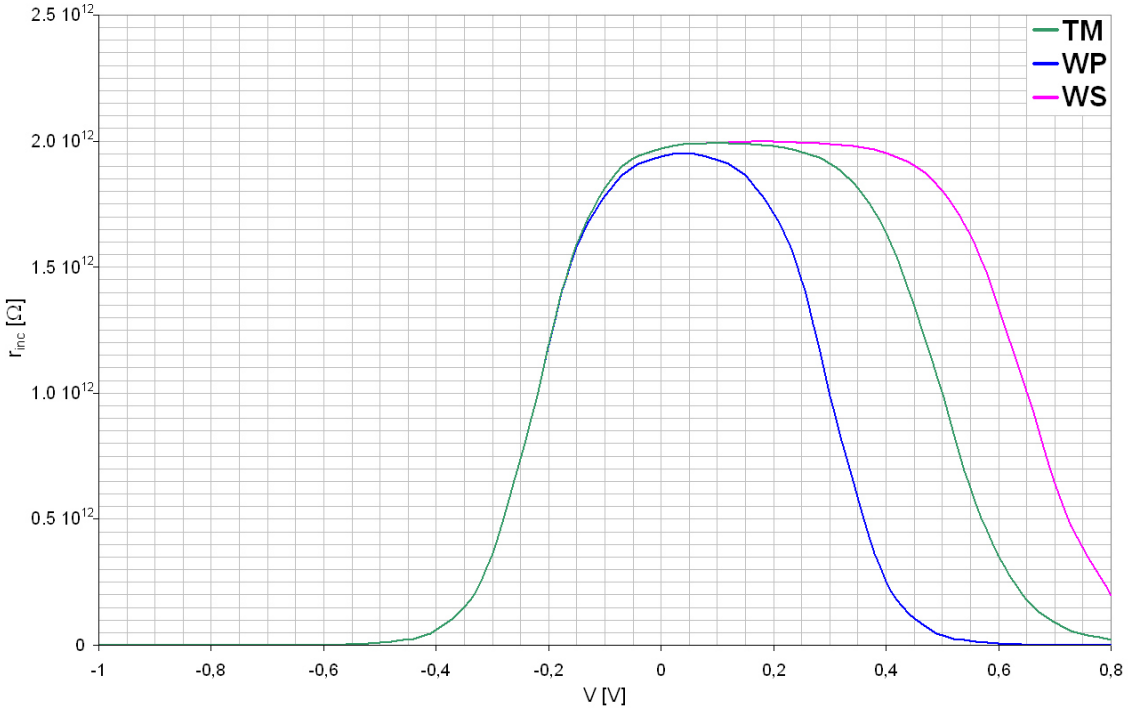

Figure 3.9: Mos-bipolar device incremental resistance

3.2.4 Design of the Full Amplifier

Figure 3.10 shows the schematic diagram of the full preamplifier.

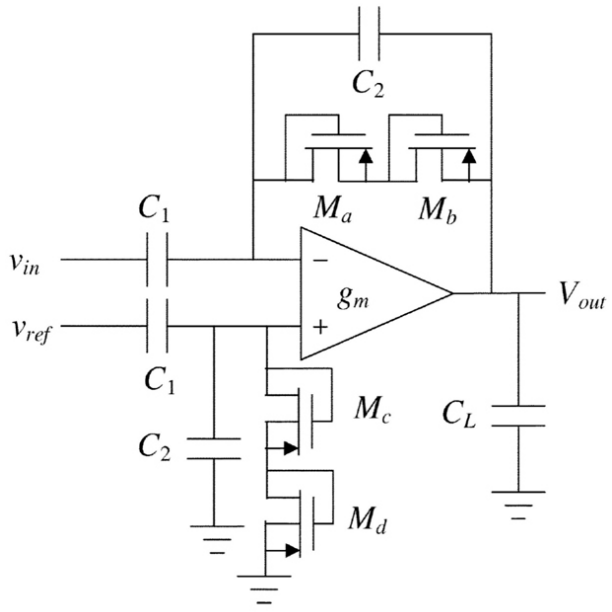

Figure 3.10: Schematic diagram of the preamplifier.

For the values of the capacitance are chosen the following values: $C_1 = 20pF$, $C_2 = 200fF$, $C_L = 10pF$. In the typical process case the incremental resistance it is $r_{inc} \approx 1.97 \times 10^{12}\Omega$. With an infinite gain OTA the following value for the gain and band would be achieved:

$$A_v \approx C_1/C_2 = \frac{20pF}{200fF} = 100 \tag{3.10}$$

$$f_H \approx \frac{1}{2\pi\ r_{inc}\ C_2} = \frac{1}{2\pi\ 1.97\ 10^{12}\ \Omega\ 200fF} = 398mHz \tag{3.11}$$

$$f_L \approx \frac{g_m^{OTA}}{2\pi\ A_v\ C_L} = \frac{78.95\mu S}{2\pi\ 100\ 10pF} = 12.5kHz \tag{3.12}$$

In figure 3.11 the Bode diagram of the Preamplifier is shown.

Using the actual OTA a Close Loop gain of $84.33V/V$ $(39.52dB)$ is achieved, and the passing band is between $f_H = 380mHz$ and $f_L = 10.5kHz$.

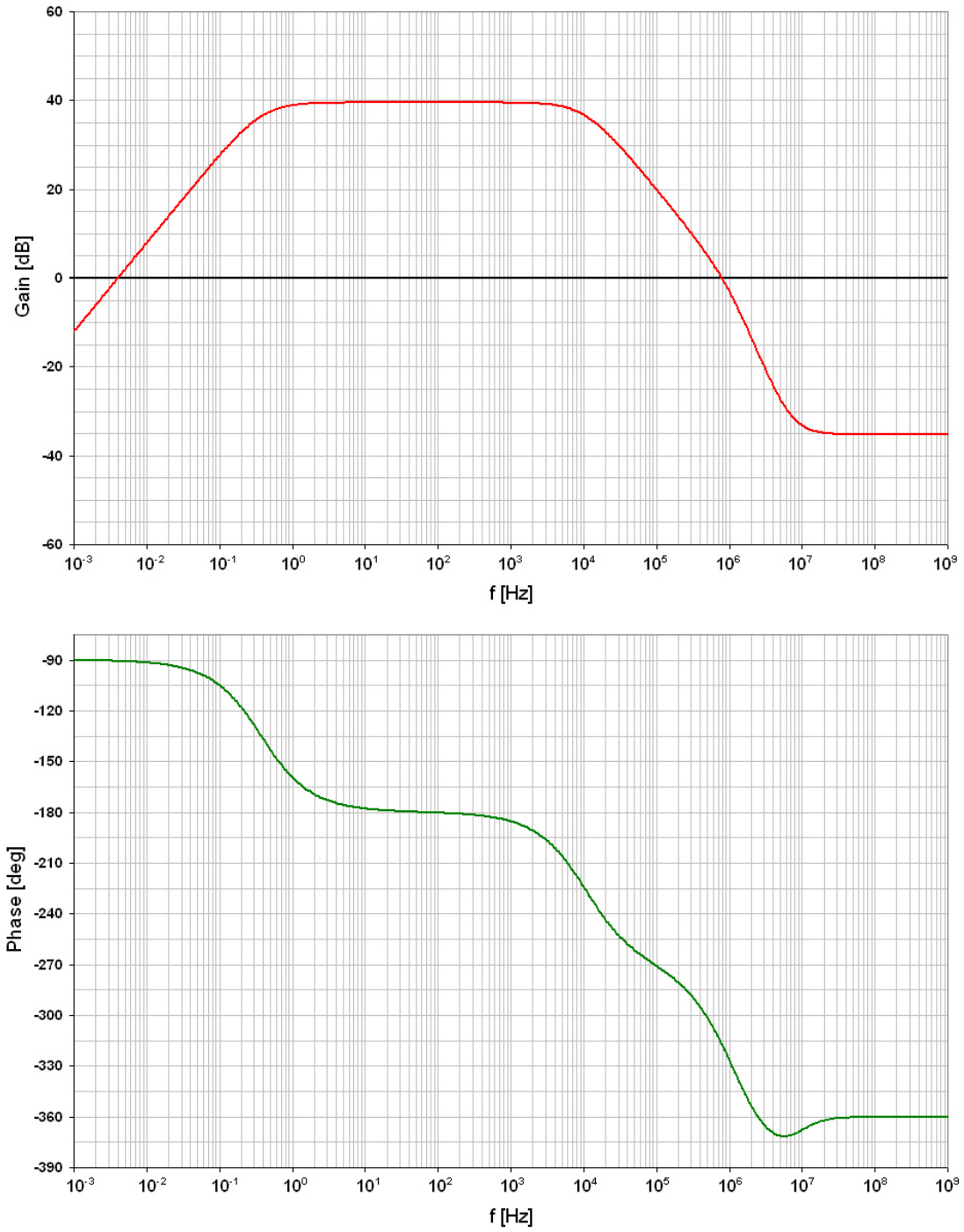

Figure 3.11: Preamplifier Bode diagram.

3.3 Preamplifier Analysis

Now the design at the schematic level of the preamplifier is ready, and it is possible to proceed with extensive simulations, to study the response of the preamplifier in a wide range of working condition, such as different values Temperatures, different Power Supplies, etc...

3.3.1 Temperature dependent analysis

Due to the power dissipation the circuit heats up. The temperature of the circuit has effect on the concentration of the electric carriers and their mobility. This may influence the gain and the DC output offset of the preamplifier.

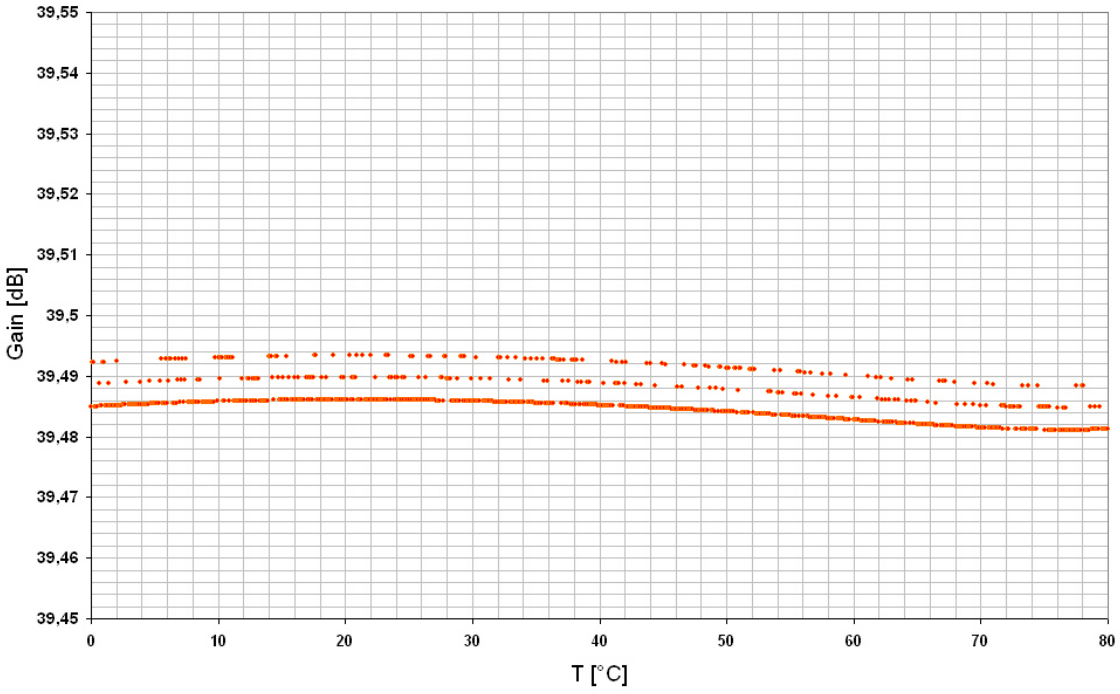

Figure 3.12: Preamplifier gain in function of the temperature, for a signal of $1kHz$.

The simulation is performed over different values of temperature from $0°C$ to $80°C$ with a step of $0.01°C$, to calculate the gain of the preamplifier when receives as input signal a sinusoidal wave at $1kHz$ (see Figure 3.12).
In this range of temperature the gain varies from a minimum value of $39.481dB$ to a

maximum value of $39.493dB$, therefore the maximum fluctuation of the gain value is $0.012dB$ and it is negligible.

A DC simulation is done to study the effect of the temperature on the DC output level (V_{DC}^{Out}), in Figure 3.13 the result is shown.

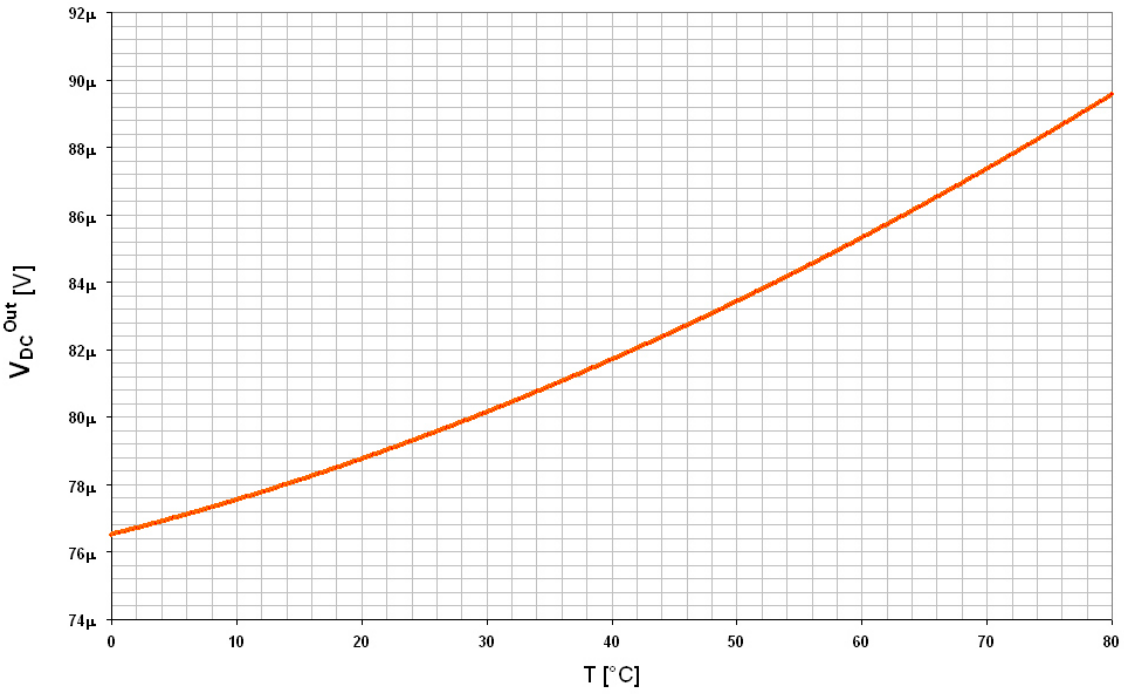

Figure 3.13: Preamplifier V_{DC}^{Out}, for a signal of $1KHz$.

The difference between (V_{DC}^{Out}) and the reference DC level increases when the temperature rises.

At $0°C$ the difference is $76.5\mu V$ and at $80°C$ the difference is $89.5\mu V$. If the temperature of the circuit increases of $10°C$ there is a change of $\approx 2\mu V$ on the output offset, which does not influence the preamplifier performance.

3.3.2 Supply voltage dependent analysis

To study the effect of the supply voltage on the preamplifier performance it is possible to simulate the AC frequency response of the circuit over different supply voltages

value.

A DC simulation is also done to evaluate the variation of the DC output level (ΔV_{DC}^{out}) with different supply voltages from the DC output level with $V_{supply} = 3.3V$.

In Table 3.4 the results are shown.

V_{supply}	f_H	f_L	ΔV_{DC}^{out}
$2.0V$	$390mHz$	$6.9Hz$	$63.7\mu V$
$2.1V$	$390mHz$	$125.9Hz$	$50.9\mu V$
$2.2V$	$390mHz$	$1.1kHz$	$56.8\mu V$
$2.3V$	$390mHz$	$3.1kHz$	$64.6\mu V$
$2.4V$	$390mHz$	$5.3kHz$	$62.2\mu V$
$2.5V$	$390mHz$	$7.3kHz$	$49.5\mu V$
$2.6V$	$390mHz$	$8.7kHz$	$29.3\mu V$
$2.7V$	$390mHz$	$10.0kHz$	$4.1\mu V$
$2.8V$	$390mHz$	$10.5kHz$	$-24.1\mu V$
$2.9V$	$390mHz$	$10.8kHz$	$-53.3\mu V$
$3.0V$	$390mHz$	$11.0kHz$	$-77.3\mu V$
$3.1V$	$390mHz$	$11.0kHz$	$-50.4\mu V$
$3.2V$	$390mHz$	$11.0kHz$	$-24.7\mu V$
$3.3V$	$390mHz$	$11.0kHz$	$0\mu V$
$3.4V$	$390mHz$	$11.0kHz$	$23.9\mu V$
$3.5V$	$390mHz$	$11.0kHz$	$47.1\mu V$
$3.6V$	$390mHz$	$11.0kHz$	$69.6\mu V$

Table 3.4: High pass cutoff frequency (f_H) and low pass cutoff frequency (f_L) in function of the supply voltage (V_{supply}).

The high pass cut off frequency is independent from the supply voltage. The low pass cut off frequency become stable for $V_{supply} = 2.7$. If $V_{supply} > 3.3V$ the power dissipation increases.

It is possible to conclude that if $2.7V < V_{supply} < 3.3V$ the preamplifier design aims are satisfied.

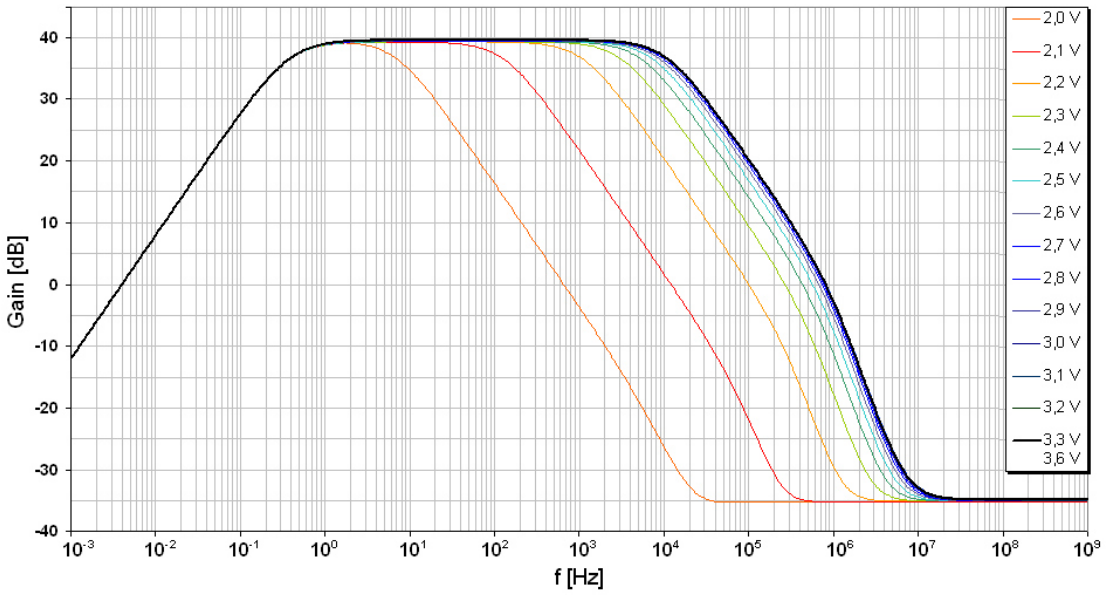

Figure 3.14: Preamplifier gain in function of the supply voltage.

3.3.3 Power Supply Rejection Ratio

Any signal or noise on the supply lines may change the bias conditions of the circuit and affects the output, degrading the noise performances.
The Power Supply Rejection Ratio (PSRR) is the ratio of the power supply voltage change (dV_s) over the output voltage change (dV_o), and it is expressed in dB:

$$PSRR = 20log(\frac{dV_o}{dV_s}) \tag{3.13}$$

In Figure 3.15 the plot of the PSRR is shown.

The PSRR assumes negative values, therefore the signals on the power supply lines are suppressed.
In the band of interest the PSRR is $-7dB$, this is not a very low value, but it has to compared with the gain of the preamplifier which is $40dB$.

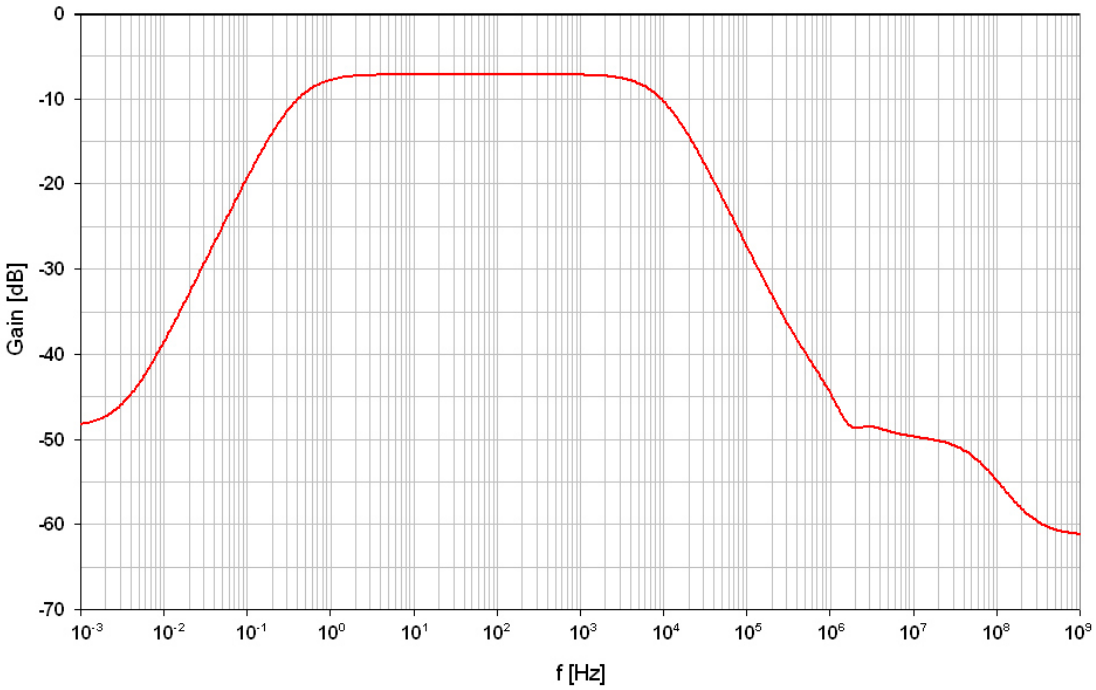

Figure 3.15: Preamplifier - PSRR.

3.3.4 Power ON

When the power supply is switched on, the supply lines do not reach immediately the working values, so also the output takes a few time to reach the correct DC level.

In the design of the preamplifier the MOS-bipolar device feedbacks the signal from the output to the negative input of the OTA, its incremental resistance depends on the DC voltage level of this two nodes. If the output is not stable also the incremental resistance does not hold a constant value, and this may cause a permanent oscillation in the output of the preamplifier.

Replacing the power generator with a time variable generator which creates a step, from the negative supply value to the positive supply value, with rising time of $10ns$ or $10\mu s$ is possible to simulate the switching on of the power supply, and study the response of the circuit.

The figure 3.16 shows the response of the circuit for a switching time of $10ns$.

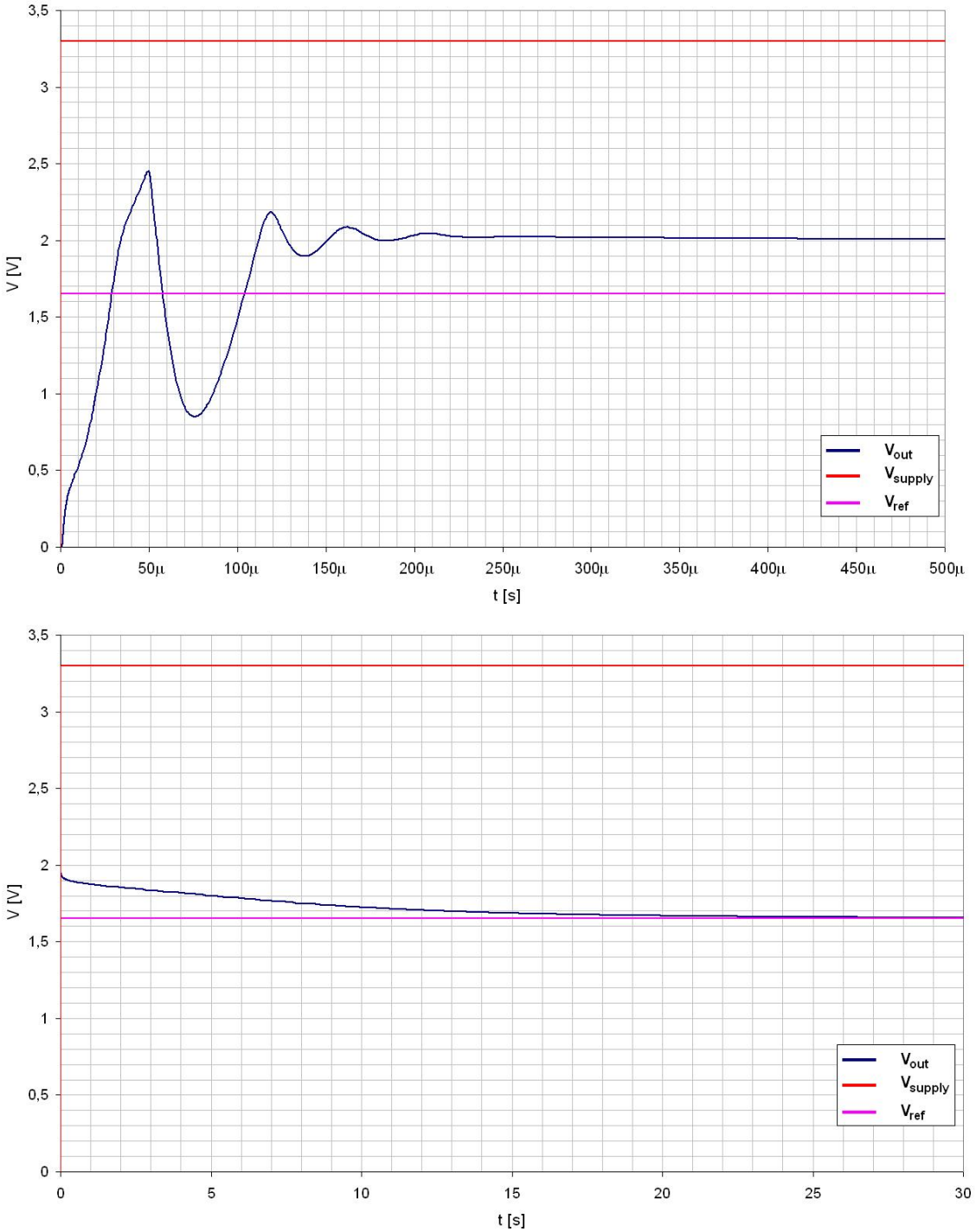

Figure 3.16: Preamplifier - Power ON

After an initial oscillation in the first $300\mu s$, the DC output level become stable and decreases until it reaches the reference value in $\approx 25s$. A similar result is obtained whit a rising time of $10\mu s$. This means that every time the power supply is switched on the preamplifier work correctly after this initial "DC output calibration" time.

3.3.5 Corner Analysis

The corner analysis of the preamplifier is performed to understand how the response of the circuit changes with the spread of the production process.
Figure 3.17 shows the transfer function of the preamplifier in the typical mean case and in the two worst cases.

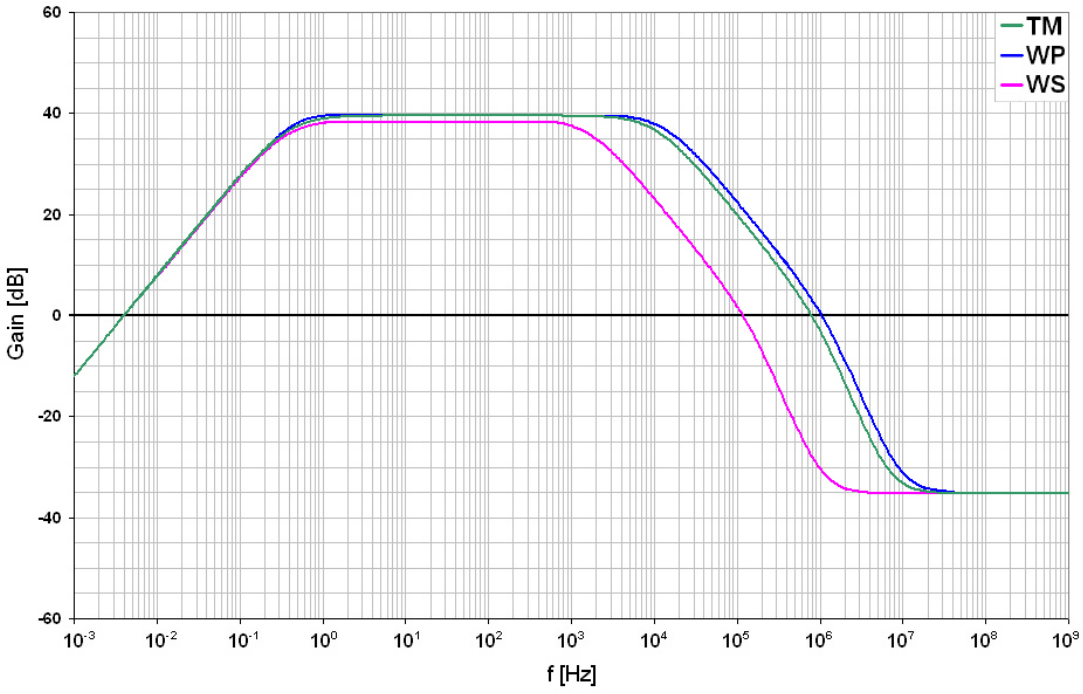

Figure 3.17: Preamplifier Corner analysis - Gain

As a input signal in the transient analysis a square wave is chosen. Its amplitude is at the same value of a typical neural signal amplitude ($150\mu V$), its pulse time is at the same order of a typical neural signal duration ($1ms$), and its rising

and falling time are both of $1ns$. In this way the square wave with steep edges has components of all frequencies and is a good signal to test the frequency response of our preamplifier.

In Figure 3.18 the response of the preamplifier to the input square wave with steep edges is shown.

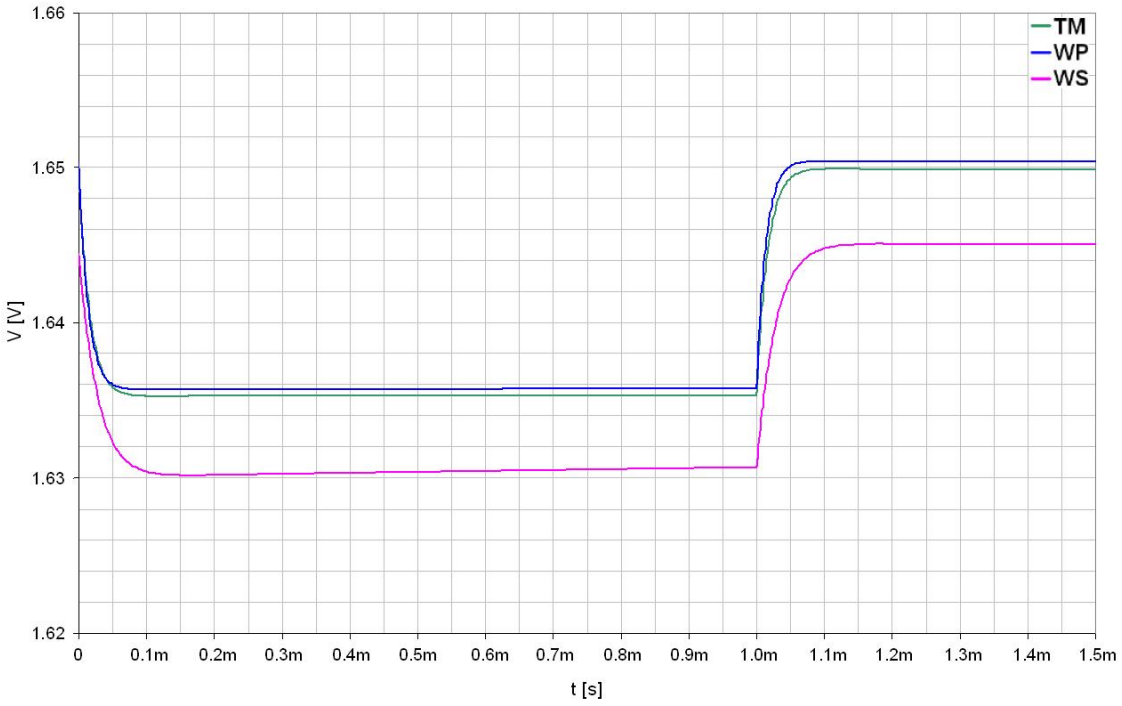

Figure 3.18: Preamplifier Corner analysis - Transient

In table 3.5 the difference from the DC output level in the TM case (ΔV_{DC}^{out}) for the two worst cases is reported.

Case	ΔV_{DC}^{out}
WP	$356\mu V$
WS	$-5.005mV$

Table 3.5: Preamplifier DC output level in worst cases.

3.3.6 Noise Performance

The last simulation on the schematic of the preamplifier is done to study the noise performance.

Figure 3.19 shows the output noise spectrum, which is calculated taking into account the contribution of all the transistors.

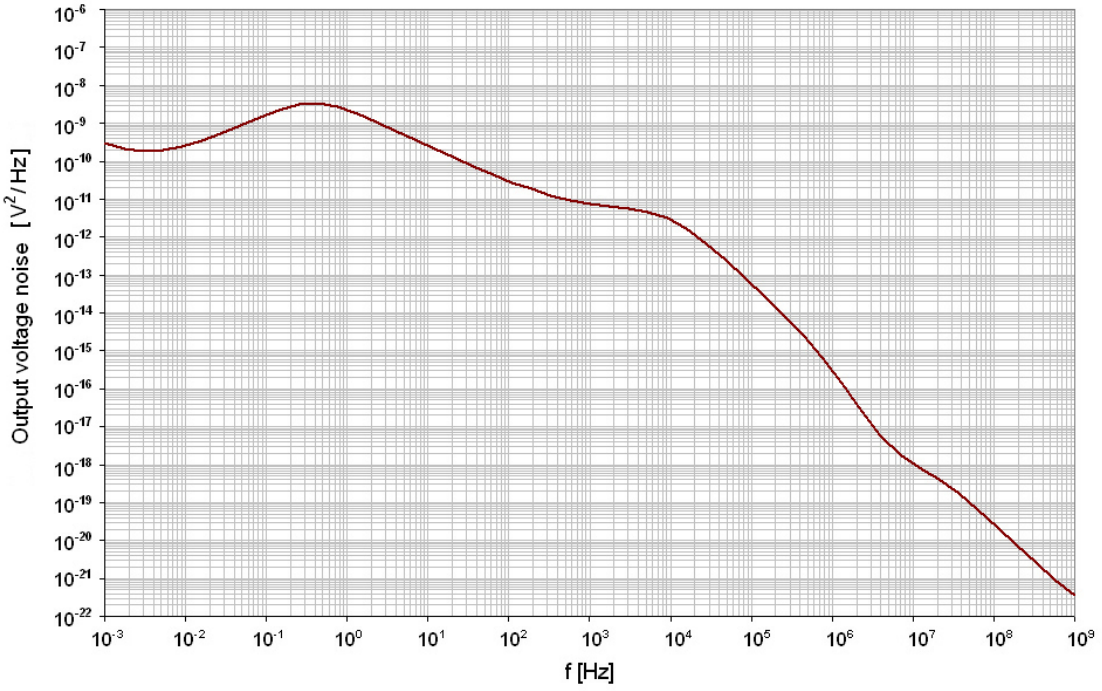

Figure 3.19: Preamplifier input referred noise spectrum

Table 3.6 shows the output noise contribution of the OTA transistors. In the NMOS transistors the flicker noise dominates because it has a flicker noise coefficient greater than the PMOS, in which the thermal noise dominates.

The total input referred noise is defined as:

$$V_{irn} = \frac{1}{A_v}\sqrt{\int_{f_1}^{f_2} V_n^2(f)df} \tag{3.14}$$

where $V_n^2(f)$ is the output noise spectrum, f_1 - f_2 represents the noise bandwidth, and A_v is the preamplifier gain.

Using Equation 3.14, integrating in a bandwidth of $16kHz$, $V_{irn} = 2.8\mu V$ is obtained.

Device	Type of Noise	Noise Contribution	% Of Total
M1	thermal	$11.45 \times 10{-}9V^2$	20.21
M2	thermal	$11.43 \times 10{-}9V^2$	20.18
M6	flicker	$6.27 \times 10{-}9V^2$	11.07
M5	flicker	$6.25 \times 10{-}9V^2$	11.03
M4	flicker	$5.47 \times 10{-}9V^2$	9.66
M3	flicker	$5.45 \times 10{-}9V^2$	9.62
M8	thermal	$1.58 \times 10{-}9V^2$	2.79
M7	thermal	$1.58 \times 10{-}9V^2$	2.78
M6	thermal	$1.49 \times 10{-}9V^2$	2.59
M5	thermal	$1.46 \times 10{-}9V^2$	2.59

Table 3.6: Preamplifier Integrated Noise Summary (in V^2) Sorted By Noise Contributors.

This value of V_{irn} is in the average of the noise values of the preamplifier architectures analyzed in Chapter 2, but in this design the noise bandwidth is greater than the other architecture. For example in the Harrison architecture the noise Bandwidth is $7.5kHz$. So reducing the bandwidth it is possible to reduce the noise bandwidth and consequently the input referred voltage noise.

Chapter 4

Filter stage

The filter stage follows the preamplifier and it amplifies again the signal in the bandwidth of interest. It also increases the slope of the transfer function after the cutoff frequency in order to have a more neat cut of the signal components with a frequency greater than desired one.
This chapter describes the design of the filter stage and reports the results of the simulations.

4.1 Filter Stage Design

4.1.1 Filter specifications

The filter stage receives as input the signal from the preamplifier. The signal coming from the microelectrode has an excepted peak-to-peak value $V_{pp_{in,preamp}} = 150\mu V$. The gain of the preamplifier is $A_{v,preamplifier} \approx 100$, so it is possible to calculate the peak-to-peak value of the signal at the input of the filter stage:

$$V_{pp_{in,filter}} = A_{v,preamplifier} \cdot V_{pp_{in,preamp}} \approx 100V/V \cdot 150\mu V = 15mV \tag{4.1}$$

This stage must be designed in order to amplify without distortions all signals with a peak-to-peak value less than $15mV$. To comply with this requirement the output of the filter stage must have a large output swing.
The filter stage should exhibit a low pass behavior with a cut off frequency of the order of $\approx 10kHz$. It is also desirable to have the possibility to tune externally this

cut off frequency.

We choose to design the filter stage using two cascaded single pole OP-AMP filters in non inverting configuration. For the implementation of the OP-AMP filter we choose to use the g_m/C technique.

4.1.2 OP-AMP Filter Design

The OP-AMP has a differential input and a single ended output and it is constituted by two stages with Miller compensation.

In Figure 4.1 the OP-AMP scheme is shown.

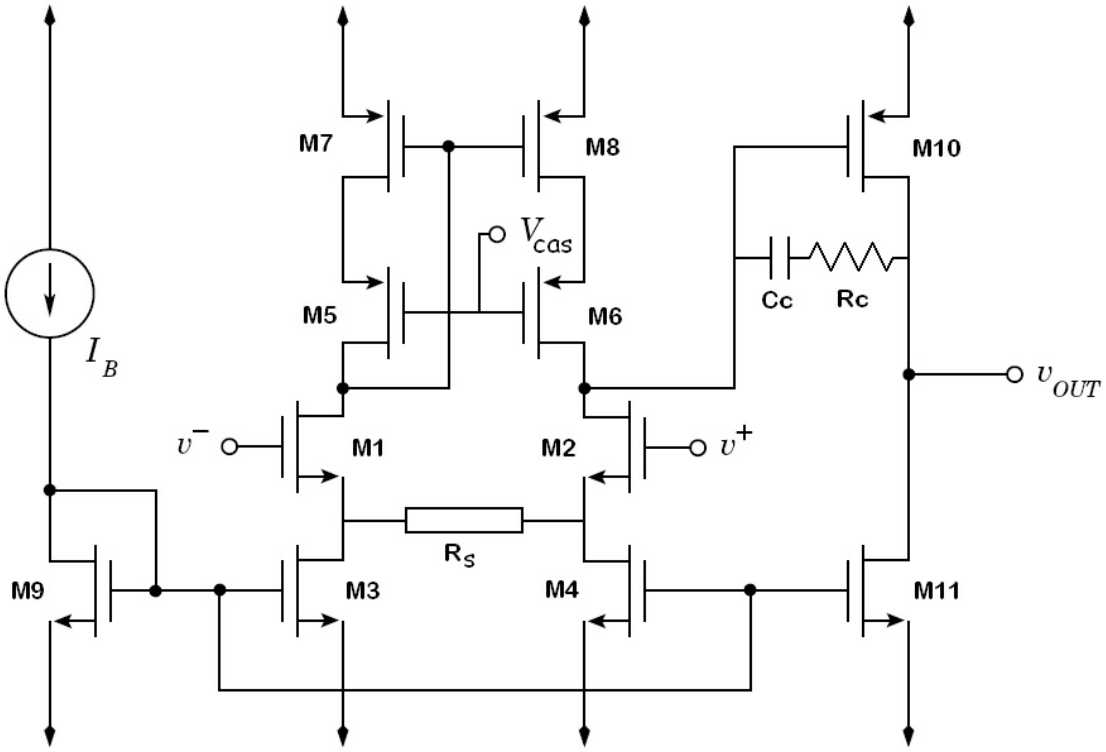

Figure 4.1: Filter OP-AMP scheme.

First stage

The first stage is composed by a differential pair with NMOS input transistors (M1, M2), a cascoded current mirror load (M5, M6, M7, M8) and current source transistors (M3, M4) which mirror the current I_{bias}. The input transistors have a

MOS	W/L	# of Gates
M1	100/4	2
M2	100/4	2
M3	40/20	4
M4	40/20	4
M5	20/0.5	1
M6	20/0.5	1
M7	20/15	4
M8	20/15	4
M9	40/20	4
M10	20/15	4
M11	40/20	4

I_{Bias}	$5\mu A$
Cc	$5pF$
Rc	$40k\Omega$

Table 4.1: MOS dimension.

source degeneration resistance (R_s).
The use of "wide swing cascode" increases the output resistance, reducing also the systematic mismatch between the currents that flow in the differential branches.
The gates of M6, M7 transistors are biased with V_{cas}. In order to bias the cascode transistors in the saturation region, V_{cas} has to satisfy the following conditions:

$$\begin{aligned} V_{dd} - V_{ds8_{sat}} &> V_{cas} + V_{gs6} \\ V_{cas} + V_{gs6} - V_{ds6_{sat}} &> V_{out1}^{DC} + S_{swing} \\ \Rightarrow V_{out1}^{DC} + S_{swing} - V_{gs6} + V_{ds6_{sat}} < V_{cas} &< V_{dd} - V_{ds8_{sat}} - V_{gs6} \end{aligned} \tag{4.2}$$

where V_{out1}^{DC} and S_{swing} are the DC voltage level and the signal swing at the output of the first stage.
After some simulation $V_{cas} = 2.0V$ is chosen.

The source degeneration resistance (R_s) is made by 4 NMOS transistor connected in series as shown in Figure 4.2. All transistors gate are biased with $V_{bias\ gate}$, and their bulk are connected to the negative supply. The simulation are done connecting $V_{bias\ gate}$ to the positive supply. The value of the source degeneration resistance is

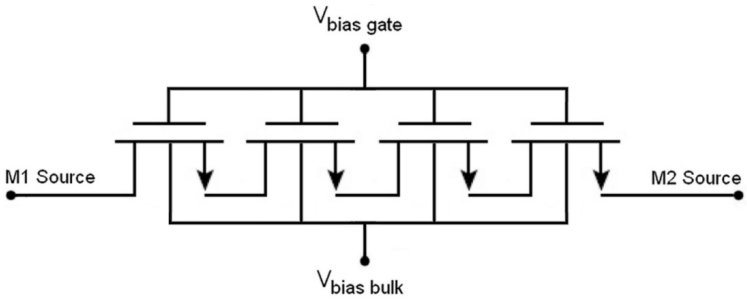

Figure 4.2: Source degeneration resistance scheme.

given by the sum of the inverse channel conductance of each transistor

$$\sum_{transistor\ M_i} \frac{1}{g_{ds_i}}$$

$$R_s = \frac{4}{g_{ds}} = \frac{4}{4.385\mu S} = 912.2k\Omega \tag{4.3}$$

The load resistance is given by the cascode equivalent resistance:

$$R_d = (g_{m6} + g_{mb6})r_{o8}r_{o6} + r_{o8} + r_{o6} = 523.17M\Omega \tag{4.4}$$

From the DC simulation of the first stage the following values are obtained:

$$\begin{aligned} g_{m8} &= 24.61\mu S \\ g_{mb8} &= 6.841\ \mu S \\ g_{m6} &= 89.71\mu S \\ g_{mb6} &= 21.97\mu S \\ r_{o8} &= \frac{1}{146.3nS} = 6.83527M\Omega \\ r_{o6} &= \frac{1}{1.455\mu S} = 687.285k\Omega \\ g_{m2} &= 108.3\mu S \\ g_{mb2} &= 24.08\mu S \end{aligned}$$

Now is possible to calculate the first stage gain:

$$A_{v_1} = \frac{g_{m2}r_{o2}R_d}{R_d + \frac{R_s}{2} + r_{o2} + (g_{m2} + g_{mb2})\frac{R_s}{2}r_{o2}} = 498.106 \tag{4.5}$$

Second stage

The second stage is a simple PMOS (M10) common source with NMOS based active load (M11). This stage gain is given by:

$$\begin{aligned} A_{v_2} &= g_{m10}(r_{o_{10}}//r_{o_{11}}) = g_{m10}\frac{1}{g_{ds10}+g_{ds11}} \\ &= 24.83\mu S\frac{1}{14.91nS+35.34nS} = 494.328 \end{aligned} \tag{4.6}$$

In figure 4.3 the Bode plot of the full OP-AMP without compensation is shown. The open loop gain is $106.87dB$ with a low pass cut off frequency of $260Hz$. At $0dB$ the phase is $-130deg$, so the phase margin is $50deg$.

Miller Compensation

With a phase margin value of 50 the OP-AMP is not adequately if it is used in low gain configuration as we need. The Phase margin is increased with Miller Compensation using the capacitance C_c. The compensation resistance (R_c) regulates the transfer function zero:

$$z_1 = -\frac{1}{R_cC_c - C_c/g_{m10}} \tag{4.7}$$

To avoid stability issues, the zero z_1 must pushed to ∞

$$R_c = 1/g_{m10} \Longleftrightarrow z_1 = \infty \tag{4.8}$$

Trough the compensation capacitance ($C_c = 5pF$) is possible to set the unity gain frequency:

$$G_{meq} = \frac{g_{m2}}{1+(g_{m2}+g_{mb2})\frac{R_s}{2}} = 1.76\mu S \tag{4.9}$$

$$f_{UG} = \frac{G_{meq}}{2\pi C_c} = 56.2kHz \tag{4.10}$$

In figure 4.4 the Bode plot of the OP-AMP with compensation is shown. The open loop gain is $106.87dB$ with a low pass cut off frequency of $245mHz$. At $0dB$ the phase is $-90deg$, so the phase margin is now $90deg$.
The unity gain frequency ($0dB$) is at $54.9kHz$, close to the value calculated in Equation 4.9.

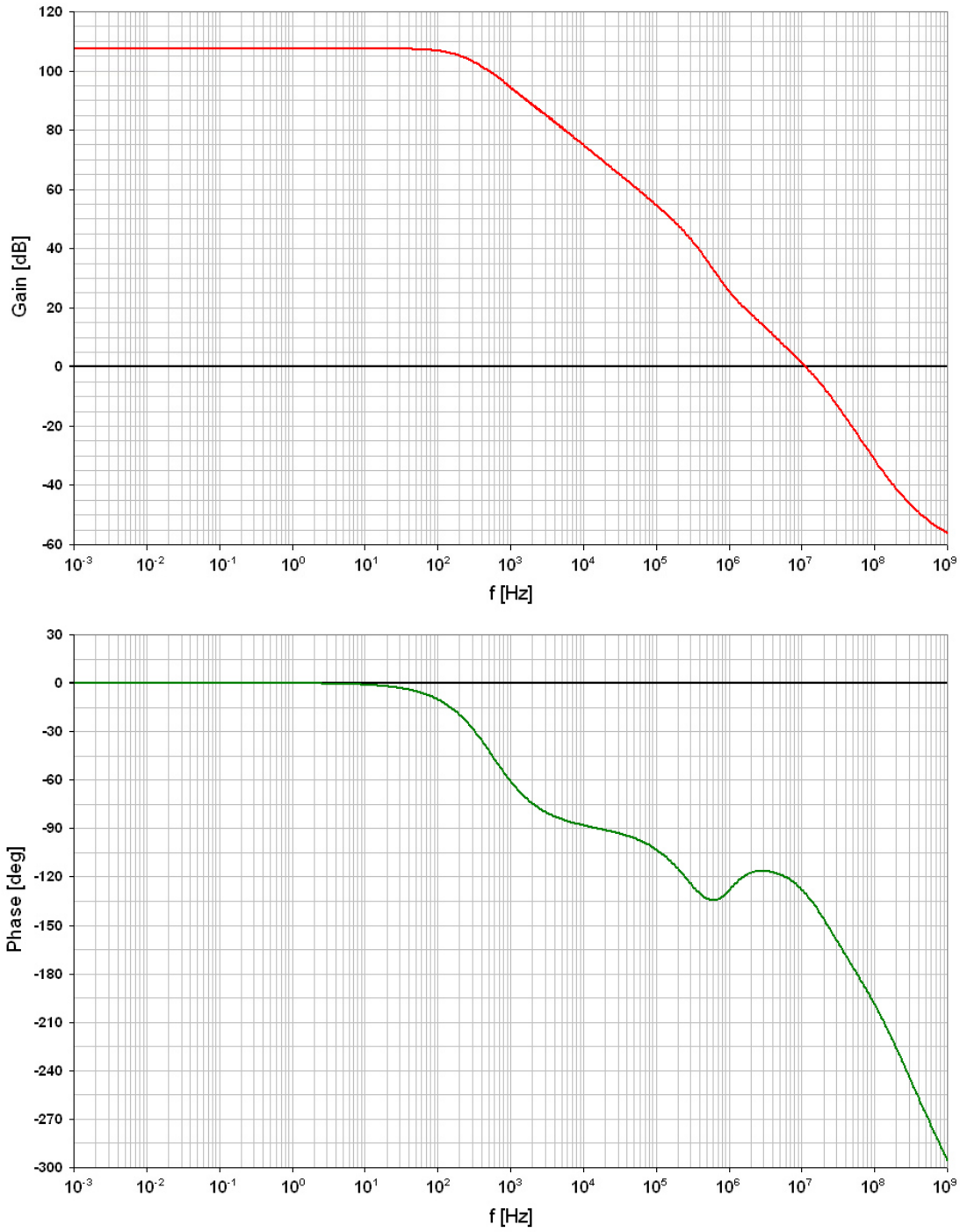

Figure 4.3: Filter OP-AMP open loop Bode diagram without compensation.

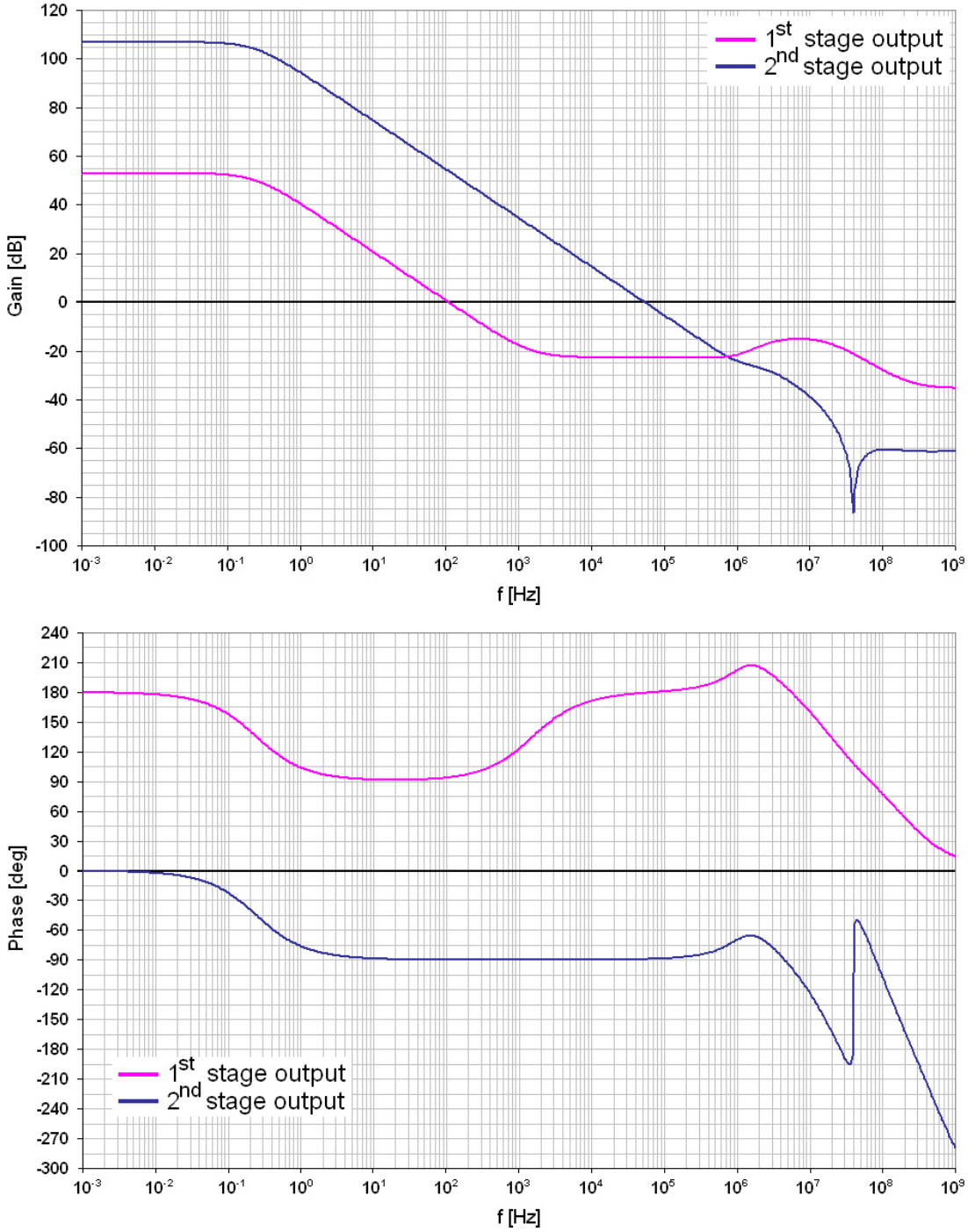

Figure 4.4: Filter OP-AMP open loop Bode diagram with compensation.

4.1.3 Two filters in cascade

The OP-AMP is ready to be used in non inverting condition. Each OP-AMP close loop gain is:

$$A_v^{close\ loop} = \frac{A_v^{OL}}{1 + A_v^{OL}\frac{R_1}{R_1+R_2}} \tag{4.11}$$

$$\lim_{A_v^{OL}\to\infty} A_v^{close\ loop} = 1 + \frac{R_2}{R_1} \tag{4.12}$$

In order to achieve a gain of 5 per filter, R_2 must be four times greater than R_2. In our design we choose: $R_1 = 100k\Omega$ and $R_2 = 400k\Omega$.
Putting the two filters in cascade as in Figure 4.5 is possible to achieve a total in band gain of 25.

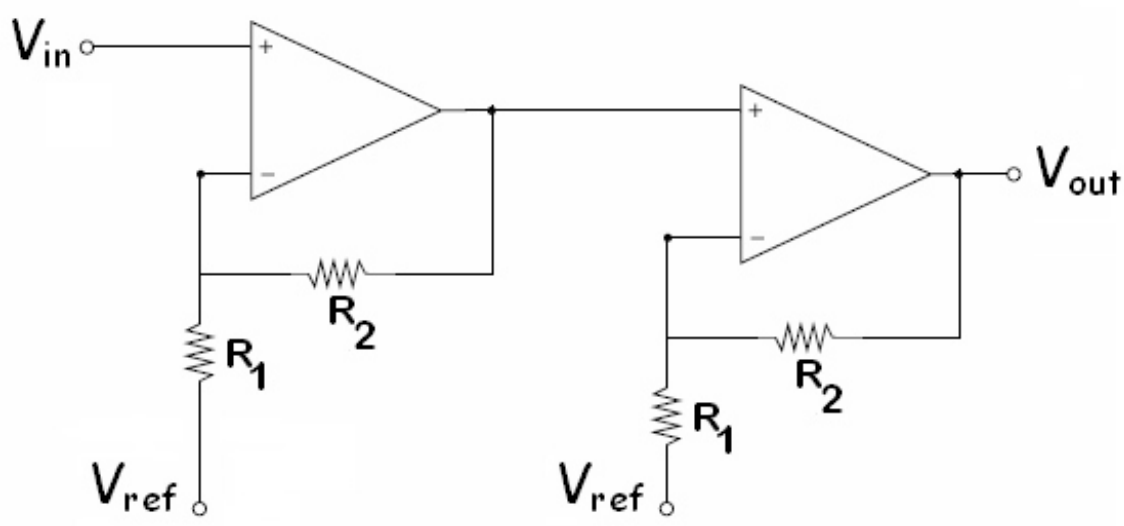

Figure 4.5: Filter stage scheme.

In figure 4.6 the Filter Stage Bode diagram is shown. The filter stage Gain is $27.94dB$, and its low pass cutoff frequency is $6.5kHz$

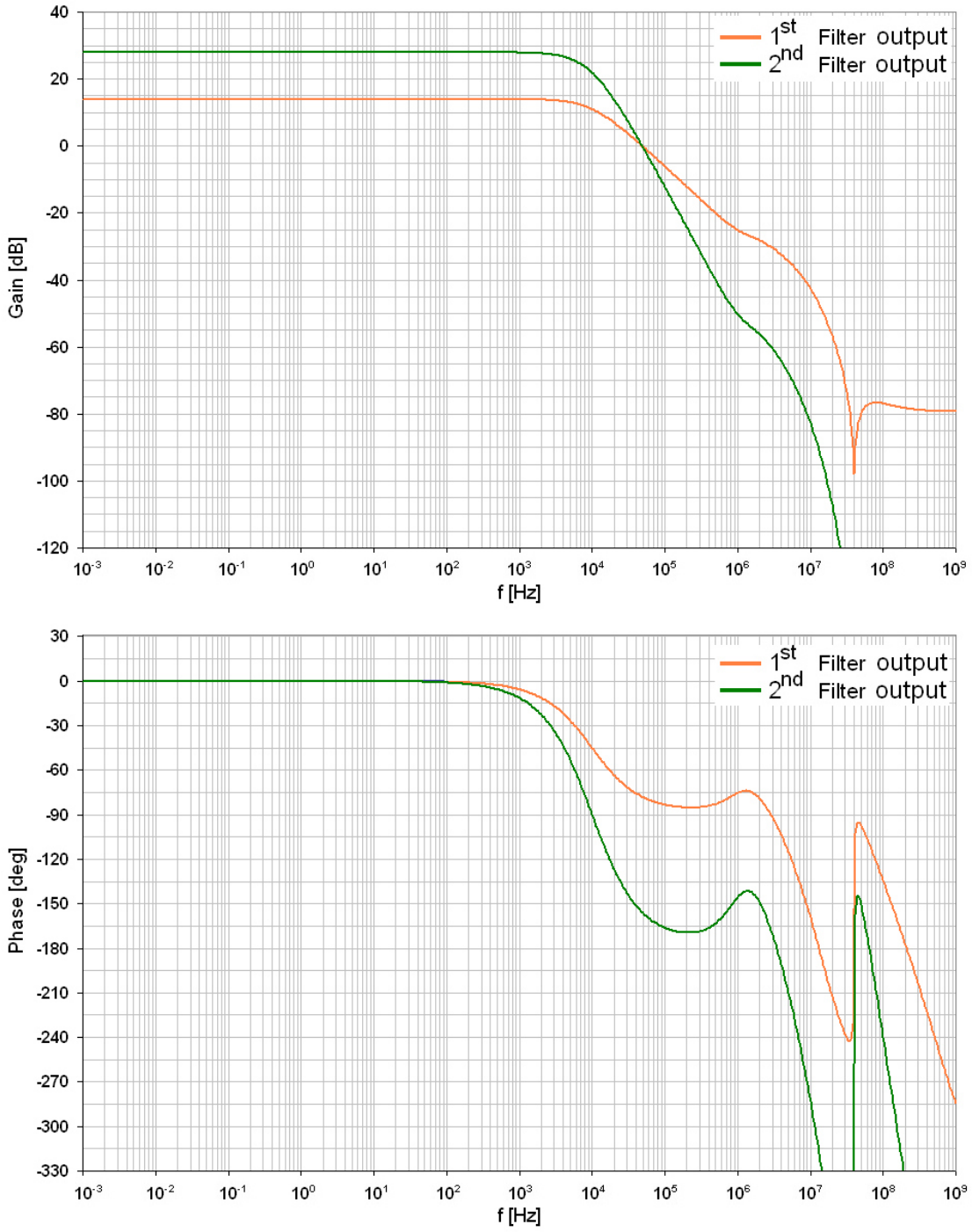

Figure 4.6: Filter stage Bode diagram.

Output Offset

The circuit to work correctly has to balance the current in the branches of the differential pair creating an output offset:

$$G_{meq} = \frac{\partial I_{branch}}{\partial V_{out_1}} \Rightarrow \Delta I_{branch} = \Delta V_{out_1} G_{meq} \tag{4.13}$$

The mismatch between circuit components affects the circuit DC working point and the current values in the branches. For example a mismatch between mirror transistors changes the mirrored current values in the different branches of the circuit, a mismatch of the input transistors broke the symmetry of the differential pair and a mismatch in the feedback resistors change the OP-AMP closed loop gain.
In a multichannel recording system there may be a difference between the different channel DC output level because of the transistors mismatch.
If the DC output level is too distant from the reference value, the output linear range decreases.
To reduce the channel-to-channel difference the mismatch had to be reduced.
According to Equation 3.1 increasing the transistors area it is possible to reduce the mismatch. The followings solutions were used during the OP-AMP design:

- Increase L of PMOS loads in order to increase the cascode resistance and consequently increase the gain of the first stage. With a high gain value the effects of the mismatch are compensated with little variation of the output DC level.

- Increase L of NMOS current sources, to reduce the mismatch effect in the mirrored current in the two branches of the differential pair.

- Increase L input NMOS transistors, in order to reduce the mismatch on g_m value.

- Split the transistors gate, so in the chip fabrication process the size of transistors are reproduced with more precision.

Increasing again the G_{meq} value it is possible to reduce further on the output offset. But to hold steady the unity gain frequency, the compensation capacitance

C_c has to be increased. A high value of C_c requires a large silicon area.

To comply with the space requirement we choose to use a $5pF$ capacitance and use an offset compensation system.

In figure 4.7 a scheme of a possible offset compensation system is shown. The DC voltages V_{offset} represent the offset of the circuit in Buffer configuration, $V_{compensation}$ is a DC reference voltage, it could vary the DC output level of the Filter Stage changing the DC level of the negative input of the first OP-AMP.

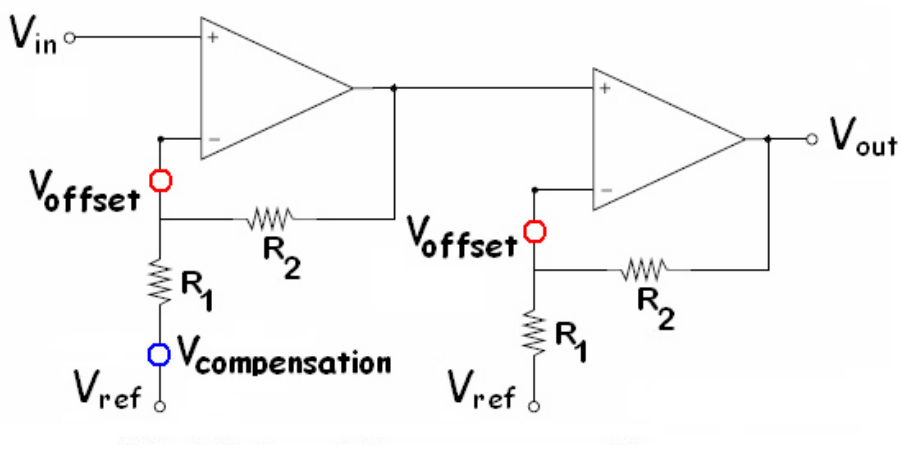

Figure 4.7: Filter stage offset Compensation

4.1.4 Bandwidth tuning

Once the circuit is fabricated there could be the need to change the filter stage cut off frequency to serve different applications. It is possible to change the cut off frequency, by changing the degeneration resistance. The degeneration resistance is made by four NMOS transistors connected in series (see Figure 4.2), varying the $V_{bias-gate}$ is possible to change the channel conductance g_{ds} of the transistors. Table shows the value of the cut off frequency for different settings of $V_{bias\ gate}$.

In Figure 4.8 the result of the transient simulation is shown. It is possible to see how changes the waveform changing the cut off frequency.

$V_{gate\ bias}$	g_{ds}	V_{DC}^{out}	f_L
$2.0V$	$1.137\mu S$	$49.7\mu V$	$1.7kHz$
$2.1V$	$1.440\mu S$	$41.5\mu V$	$2.1kHz$
$2.2V$	$1.735\mu S$	$36.2\mu V$	$2.6kHz$
$2.3V$	$2.022\mu S$	$32.4\mu V$	$3.0kHz$
$2.4V$	$2.299\mu S$	$29.6\mu V$	$3.4kHz$
$2.5V$	$2.568\mu S$	$27.5\mu V$	$3.8kHz$
$2.6V$	$2.828\mu S$	$25.8\mu V$	$4.2kHz$
$2.7V$	$3.078\mu S$	$24.4\mu V$	$4.5kHz$
$2.8V$	$3.319\mu S$	$23.3\mu V$	$4.9kHz$
$2.9V$	$3.551\mu S$	$22.3\mu V$	$5.2kHz$
$3.0V$	$3.773\mu S$	$21.5\mu V$	$5.5kHz$
$3.1V$	$3.986\mu S$	$20.9\mu V$	$5.9kHz$
$3.2V$	$4.190\mu S$	$20.3\mu V$	$6.2kHz$
$3.3V$	$4.385\mu S$	$19.8\mu V$	$6.5kHz$

Table 4.2: Filter Stage Low Pass cutoff frequency f_L, channel conductance of R_s transistor, DC output level V_{DC}^{out} in function of $V_{gate\ bias}$.

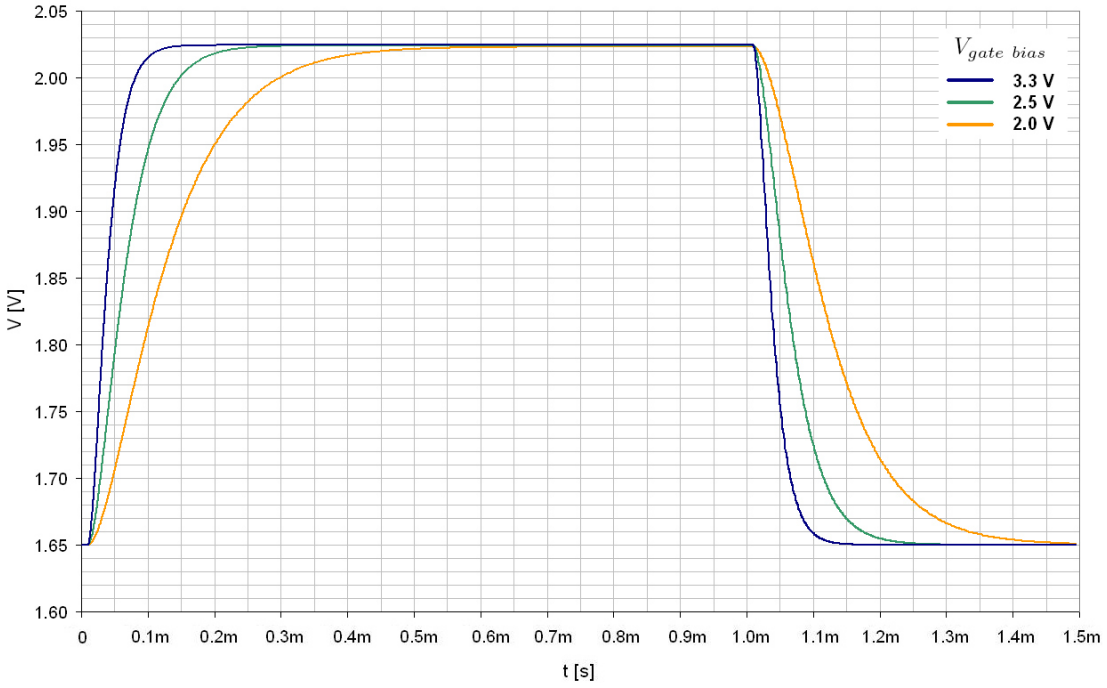

Figure 4.8: Filter Stage transient simulation with different cut off frequency

4.2 Filter stage Analysis

Now the design at the schematic level of the Filter stage is complete, and it is possible to simulate its response to a wide range of working conditions.

4.2.1 Monte Carlo Simulation

Due to the mismatch of the circuit components the response of this stage could change. The parameters that we analyze are the DC output level and the gain.
Through Monte Carlo simulations it is possible to study the effects of the mismatch on the circuit performance: in each run random values for the circuit element parameters are generated according to the statistical fluctuations.
In the simulations it is possible to include also the statistical model due to process variations.
Figure 4.9 shows the results of the process and mismatch AC and DC simulations after the first OP-AMP filter and at the output of the filter stage.
At the first filter output the DC level is at $1.65093V$ with a standard deviation of $10.175mV$. This value correspond to a V_{offset} of $\approx 2mV$ in the unity gain case.
Trough the AC simulation is possible to give an estimation of the gain of the filter stage taking into account the process variation and mismatch:

$$A_{v_{filter\ stage}} = 24.885 \pm 0.113$$

4.2.2 Output Linearity

The AC simulation results are valid only for small signals around the DC operating points.
If the signal is too large the response of the circuit becomes non-linear, the gain value depends on the inputs signal amplitude, and the signal is distorted.
To specify the input linear range, transient simulations with signals of different amplitude are done. The input signal is a square wave with steep edges (rising and falling times of $1ns$), and a pulse width of $1ms$.

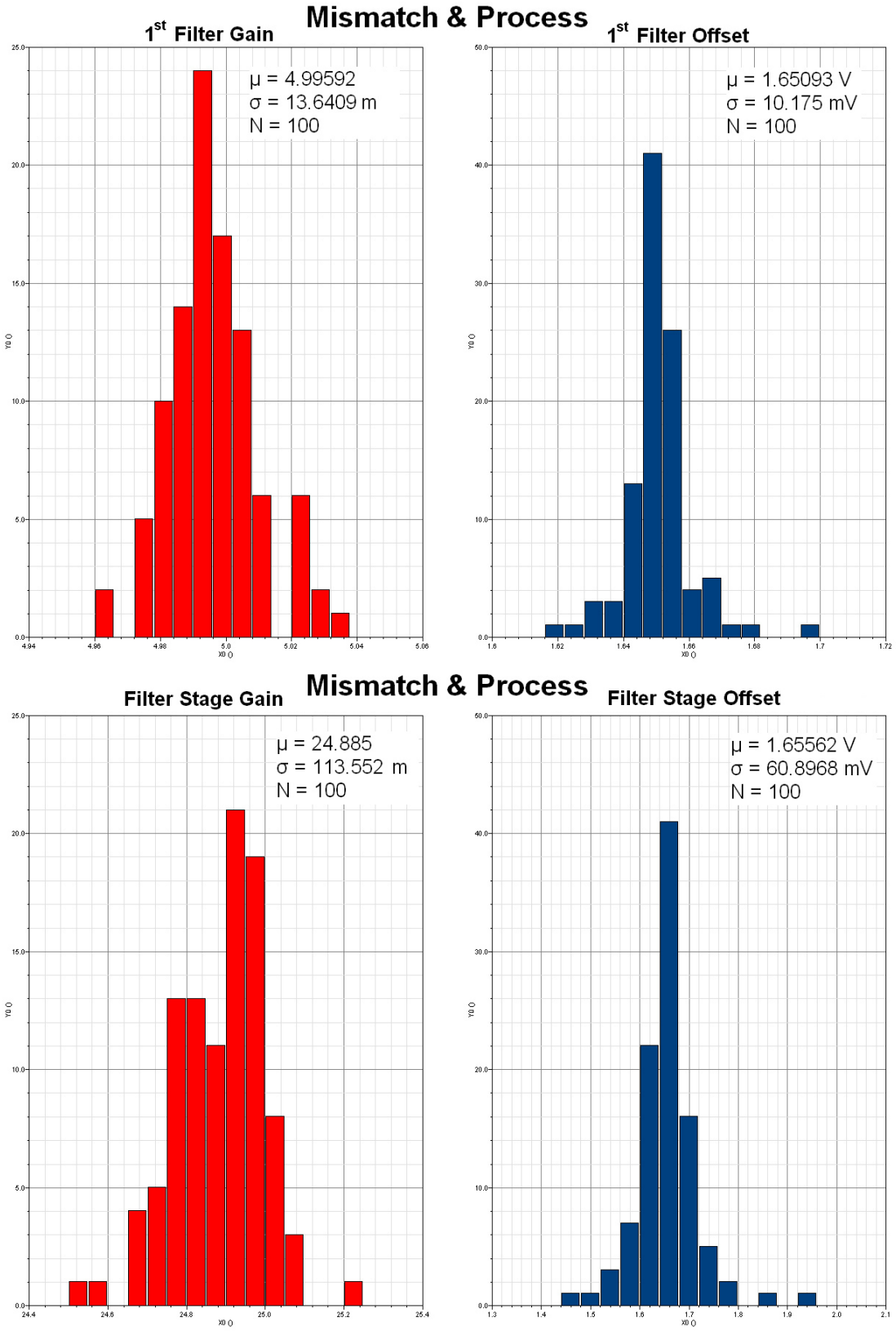

Figure 4.9: Filter stage mismatch

Square waves with amplitude from $-80mV$ to $+80mV$ with an interval of $10mV$ are used in these simulations. The gain is calculated as ratio of output signal amplitude and input square wave amplitude.

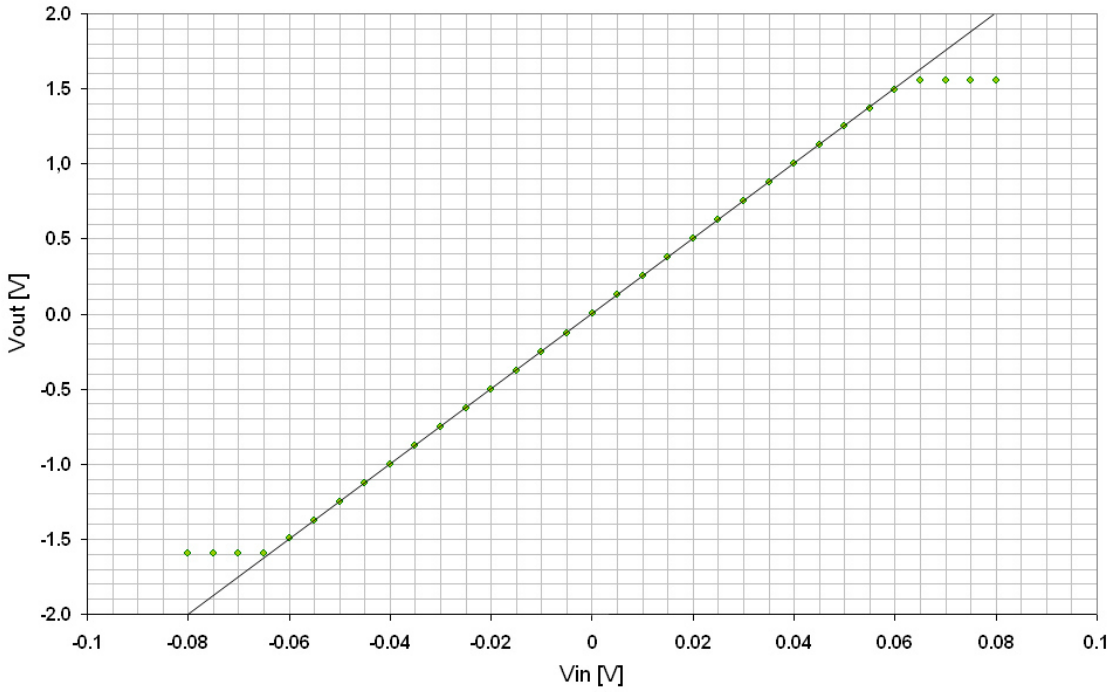

Figure 4.10: Filter stage output linearity

$$V_{out} = A_v \cdot V_{in} + \epsilon \tag{4.14}$$

Fitting the graph in Figure 4.10 with Equation 4.14 in the range $-50mV$ - $+50mV$ the following parameters are obtained:

$$A_v = 24.9547 \pm 2 \times 10^{-4}$$

$$\epsilon = (28.6 \pm 6.4)\mu V$$

With the χ^2 test is obtained $\chi^2 = 11.98$ with 20 degrees of freedom, for this value the fit is acceptable with a 90% of confidence level.
So it is possible to assert that for a signal in the range between $-50mV$ and $+50mV$ the circuit has a linear response.

4.2.3 PSSR, Temperature and Corner Analysis

A simulation is done to calculate the Power Supply Rejection Ratio, and its result is shown in Figure 4.11.

The PSSR assumes positive values from $2kHz$ to $100kHz$, but it remains below $10dB$. This should not influence negatively the circuit performance because the main interference signals on power supply lines are usually around $50Hz$.

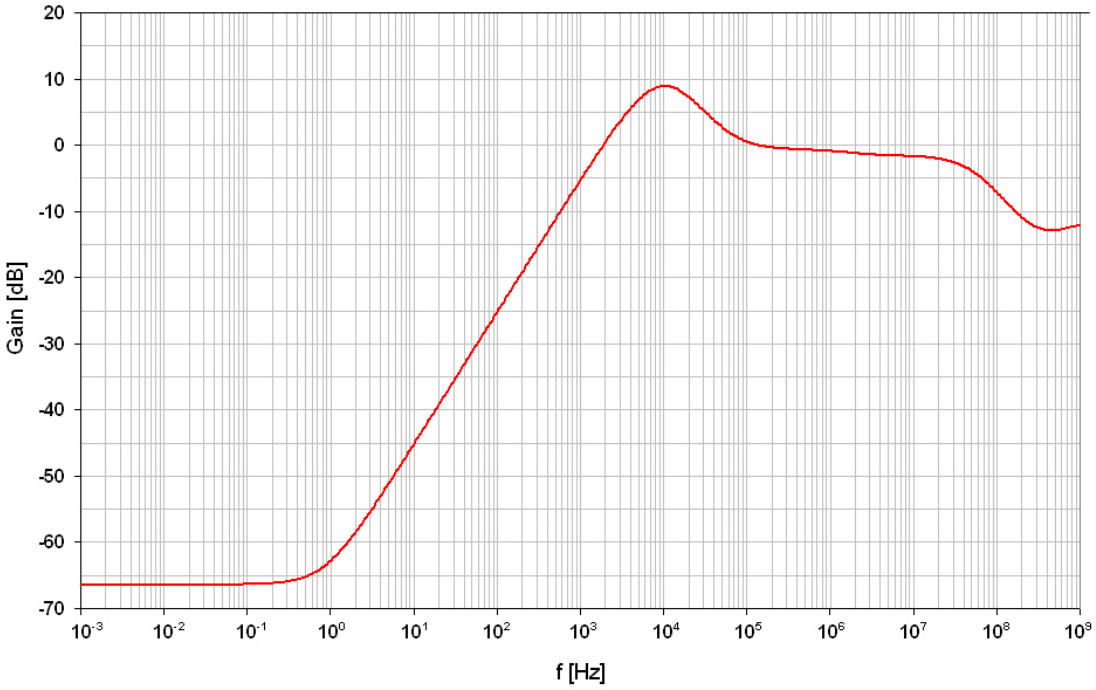

Figure 4.11: Filter stage PSRR

Temperature analysis is done with AC and DC simulation varying the circuit temperature from $0°C$ to $80°C$ with steps of $0.1°C$.

Figure 4.12 shows the dependence of the filter stage gain from the temperature. The gain is $27.9456dB$ at $0°C$ and it decreases reaching the value of 27.9400 at $80°C$. This variation represent $6 \times 10^{-3}\%$ of the gain, so it is negligible.

Figure 4.13 shows the influence of the temperature on the difference between the DC output level and reference voltage value. When the temperature rises the DC output level decreases, from $24.4\mu V$ at $0°C$ to $14.0\mu V$ at $80°C$. This variation does not influence the output linearity of the filter stage.

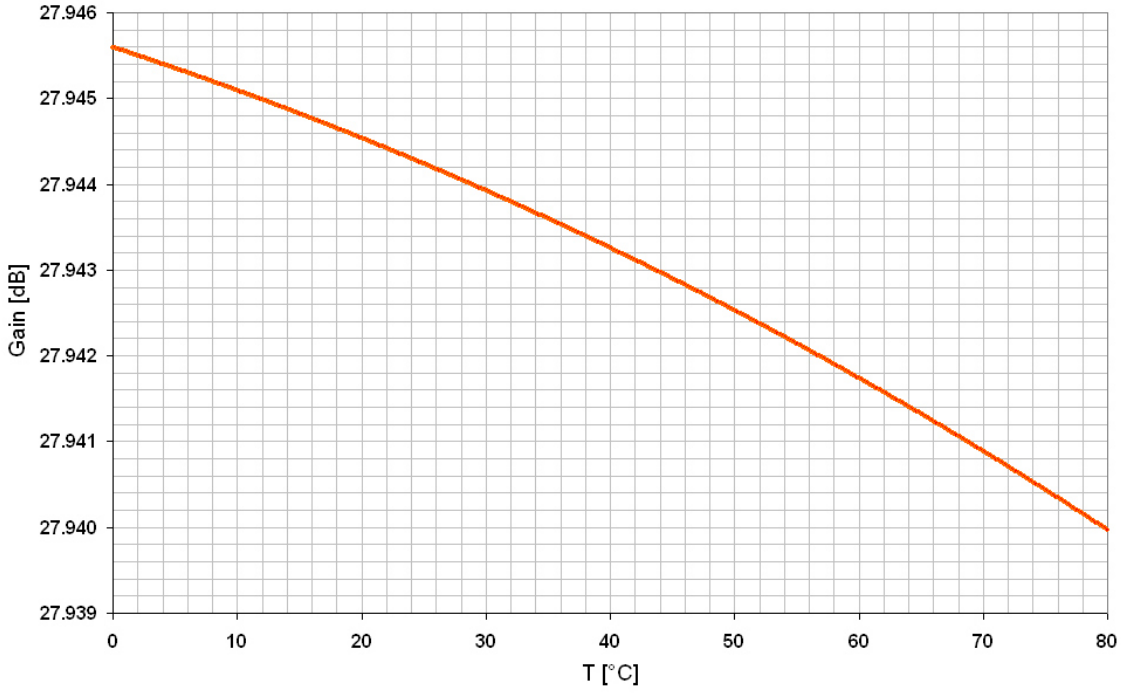

Figure 4.12: Filter Stage Gain in function of the temperature.

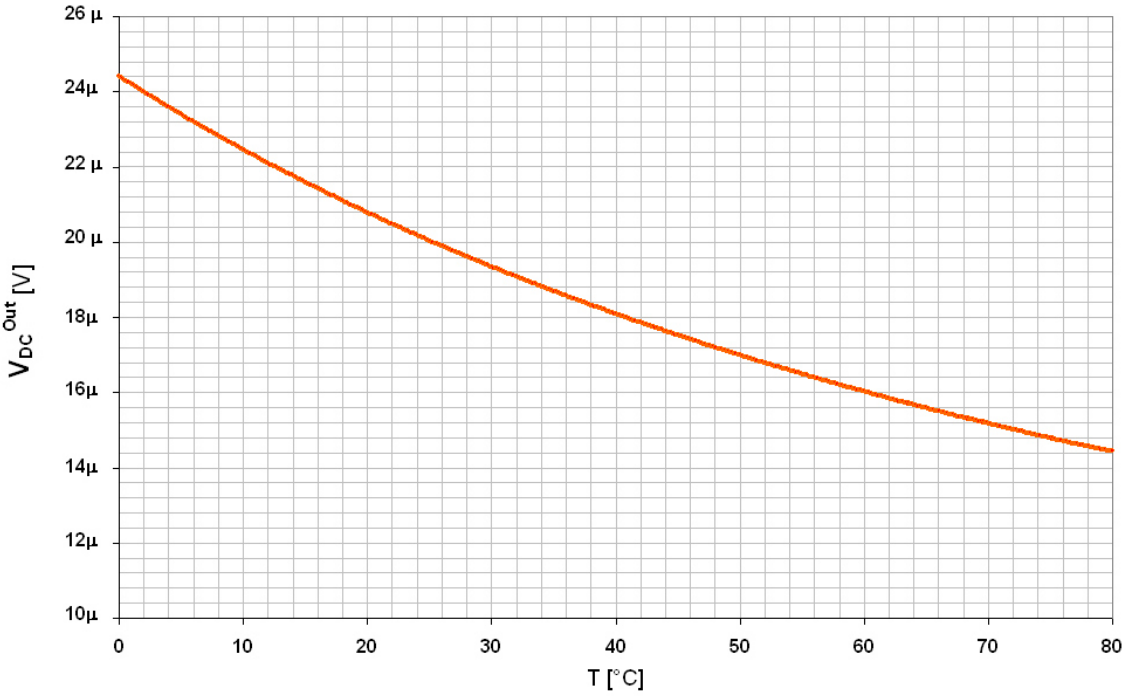

Figure 4.13: Filter Stage DC output level in function of the temperature

A Corner analysis is done to study the response of the circuit in the worst cases. Figure 4.14 shows the AC response of the filter stage in the corner cases. The cutoff frequency in the WS case is lower than the WP case. In Table 4.3 the results are summarized.

Case	Gain	f_L
TM	$27.943dB$	$6.5kHz$
WP	$27.947dB$	$8.7kHz$
WS	$27.902dB$	$4.6kHz$

Table 4.3: Filter gain and cutoff frequency in worst cases.

In the transient simulation, a square wave with steep edges is used as input signal, its amplitude is $15mV$, its rising and falling time are $1ns$ and its width is $1ms$. According to the AC results, in the WP case the output signal has more high frequency components than the WS case (see Figure 4.15).

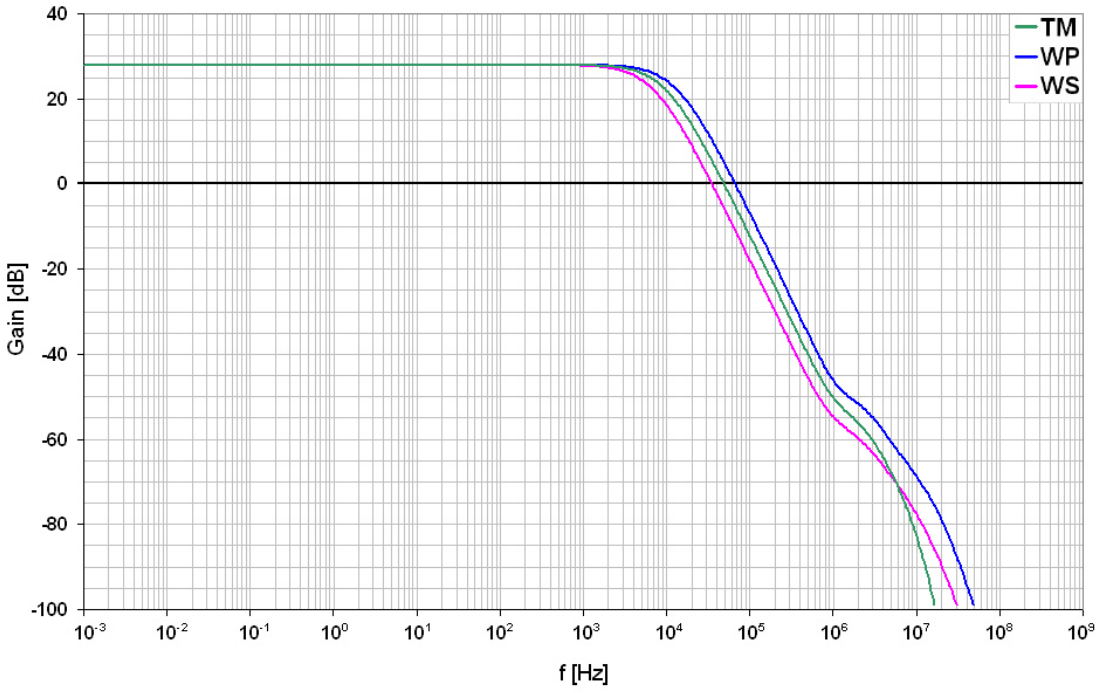

Figure 4.14: Filter stage corner AC

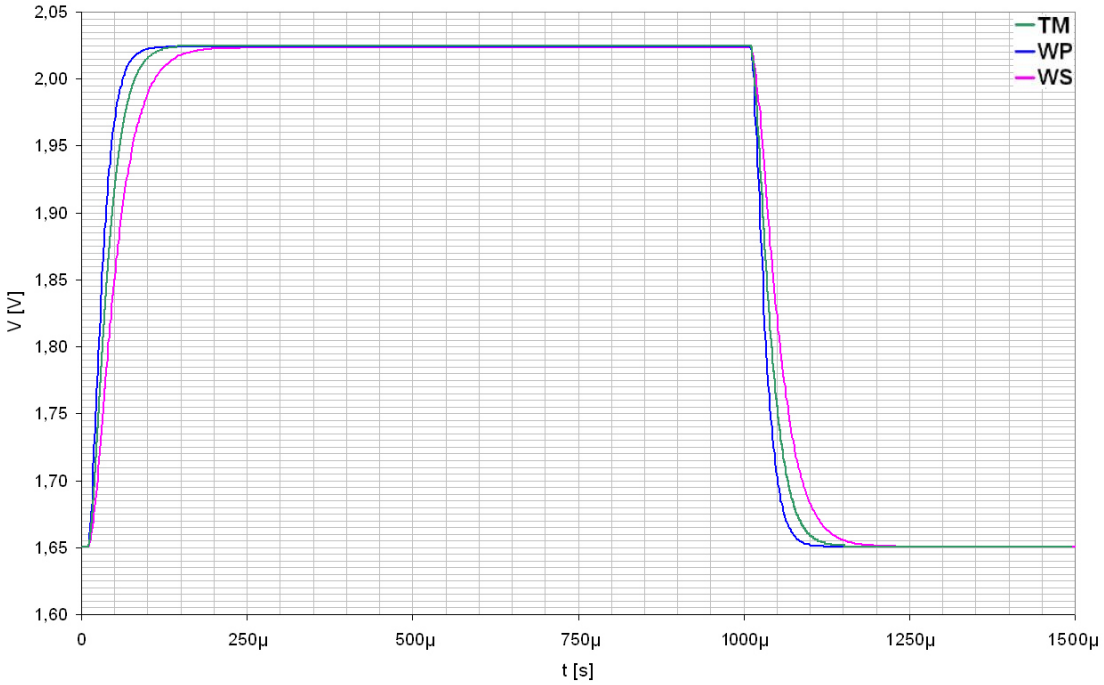

Figure 4.15: Filter stage corner transient

Noise

The last simulation on the Filter stage is done to study the noise performance. Table 4.4 shows the output noise contribution of the filter stage transistors. As expected the main contribution is due to the first OP-AMP filter (F1), because its noise is amplified to the output by the second OP-AMP filter (F2).

In Figure 4.16 the output noise spectrum is shown.

The value of the total Input Referred Voltage Noise is $V_{irn} = 3.8\mu V$. This value is referred to the filter stage input, so it is negligible compared to the noise introduced by the preamplifier.

Device	Type of Noise	Noise Contribution	% Of Total
F1/M4	thermal	$8.52 \times 10^{-7} V^2$	20.66
F1/M3	thermal	$8.52 \times 10^{-7} V^2$	20.65
F1/M4	flicker	$5.26 \times 10^{-7} V^2$	12.75
F1/M3	flicker	$5.26 \times 10^{-7} V^2$	12.75
F1/M8	thermal	$4.28 \times 10^{-7} V^2$	10.37
F1/M7	thermal	$4.27 \times 10^{-7} V^2$	10.37
F1/M8	flicker	$1.17 \times 10^{-7} V^2$	2.85
F1/M7	flicker	$1.17 \times 10^{-7} V^2$	2.85
F2/M4	thermal	$4.17 \times 10^{-8} V^2$	1.01
F2/M3	thermal	$4.17 \times 10^{-8} V^2$	1.01

Table 4.4: Filter Stage Integrated Noise Summary (in V^2) Sorted By Noise Contributors.

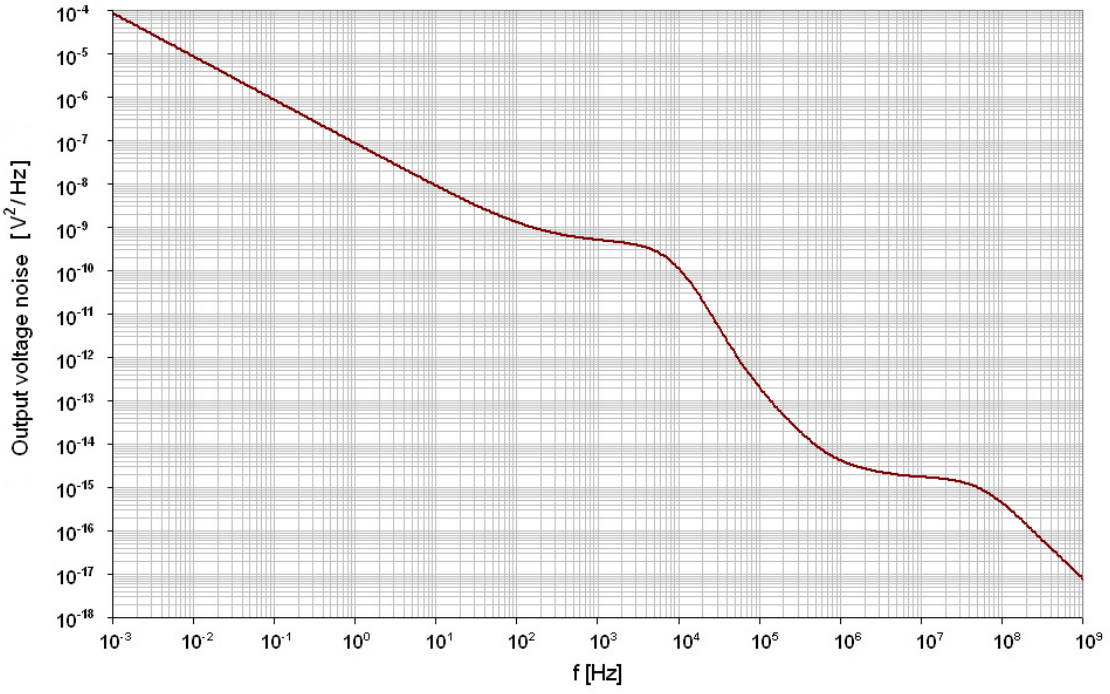

Figure 4.16: Filter stage noise

Chapter 5

Complete Front End simulations

This chapter describes the simulations of the full AFE.
The chain has been completed with a unity gain output buffer whose purpose is to interface the AFE to the recording hardware.
After a brief introduction to the Output Buffer the results of the complete AFE simulations are presented.

5.1 Output Buffer

5.1.1 Output Buffer requirements

With the first two blocks of the AFE a total gain of ≈ 2500 is achieved. This value is adequate for our purpose, so as output of the analog processing chain all we needs is a unity gain buffer.
The signal coming from the preamplifier has an excepted peak-to-peak value $V_{pp_{in,filter}} = 15mV$. The gain of the filter stage is $A_{v,preamplifier} \approx 25$, so it is possible to calculate the peak-to-peak value of the signal at the input of the buffer:

$$V_{pp_{in,buffer}} = A_{v,filter} \cdot V_{pp_{in,filter}} \approx 25V/V \cdot 15\mu V = 375mV \tag{5.1}$$

So the Buffer linear output range must be at least $375mV$.
Another requirement is that the Buffer cut off frequency must be higher than $10kHz$.

5.1.2 Output Buffer design

For the implementation of the Output Buffer a standard configuration in class AB with two stage and Miller compensation is chosen.
In Figure 5.1 the schematic of the output OP-AMP is shown.

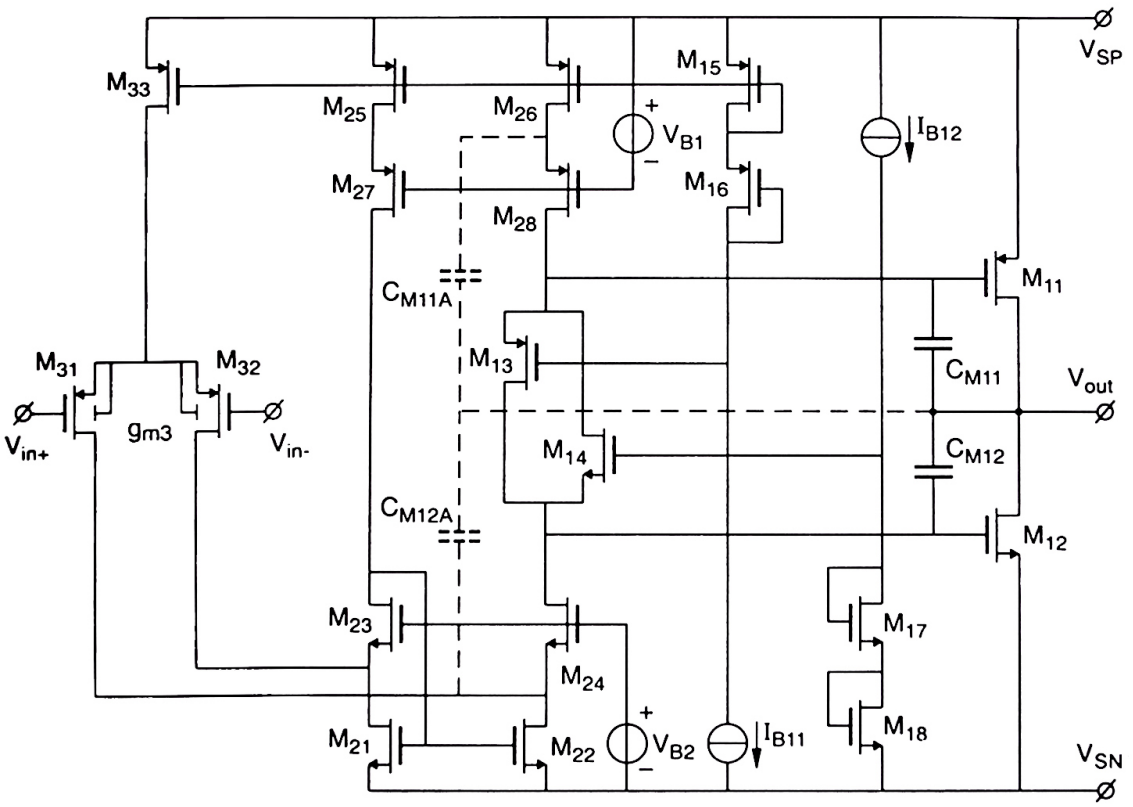

Figure 5.1: Output OP-AMP.

The output buffer is connected to the oscilloscope with a load resistance of 50Ω and a load capacitance of $20pF$.
If a supply voltage between $0V$ and $3.3V$ is used, the DC output level is $\approx 1.65V$. This means that a current of $33mA$ will flow in the load resistance. To avoid this large current flow at the output there are two solutions:

- Put a high load resistance $1M\Omega$, in order to have a current flow of few μV
- Use a dual power supply with $\pm 1.65V$, in order to have a DC output level $\approx 0V$.

In Figure 5.2 the output buffer block is shown.

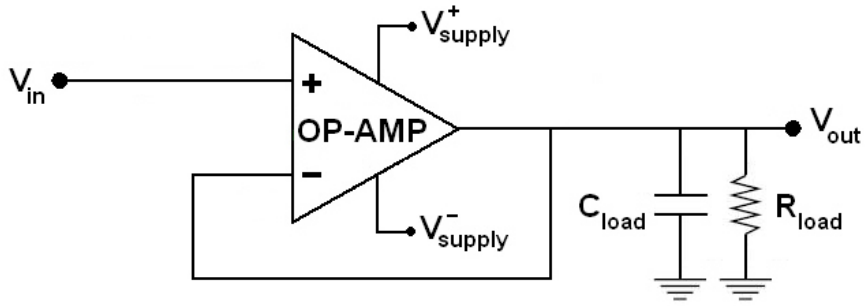

Figure 5.2: Output Buffer scheme.

Figure 5.3 shows the open loop Bode plot of the output OP-AMP and Figure 5.4 shows the Bode plot of the output buffer. The performance of the buffer in the two conditions described are summarized in Table 5.1.

Setting			Open Loop			Buffer configuration		
V^+_{supply}	V^-_{supply}	R_{load}	Gain	f_L	PM	Gain	Gain $\frac{V}{V}$	f_L
$3.3V$	$0V$	$1M\Omega$	$114.42dB$	$6.5Hz$	$60deg$	$-1.09mdB$	0.9998	$8MHz$
$1.65V$	$-1.65V$	50Ω	$38.58dB$	$1.5kHz$	$90deg$	$-158.94mdB$	0.9818	$400kHz$

Table 5.1: Performance of the Buffer in the two possible conditions.

A transient simulation is done with a square wave with steep edges, to test the stability of the buffer in the two different conditions. The results are shown in Figure 5.5 and Figure 5.6. The response in the two cases is the same.

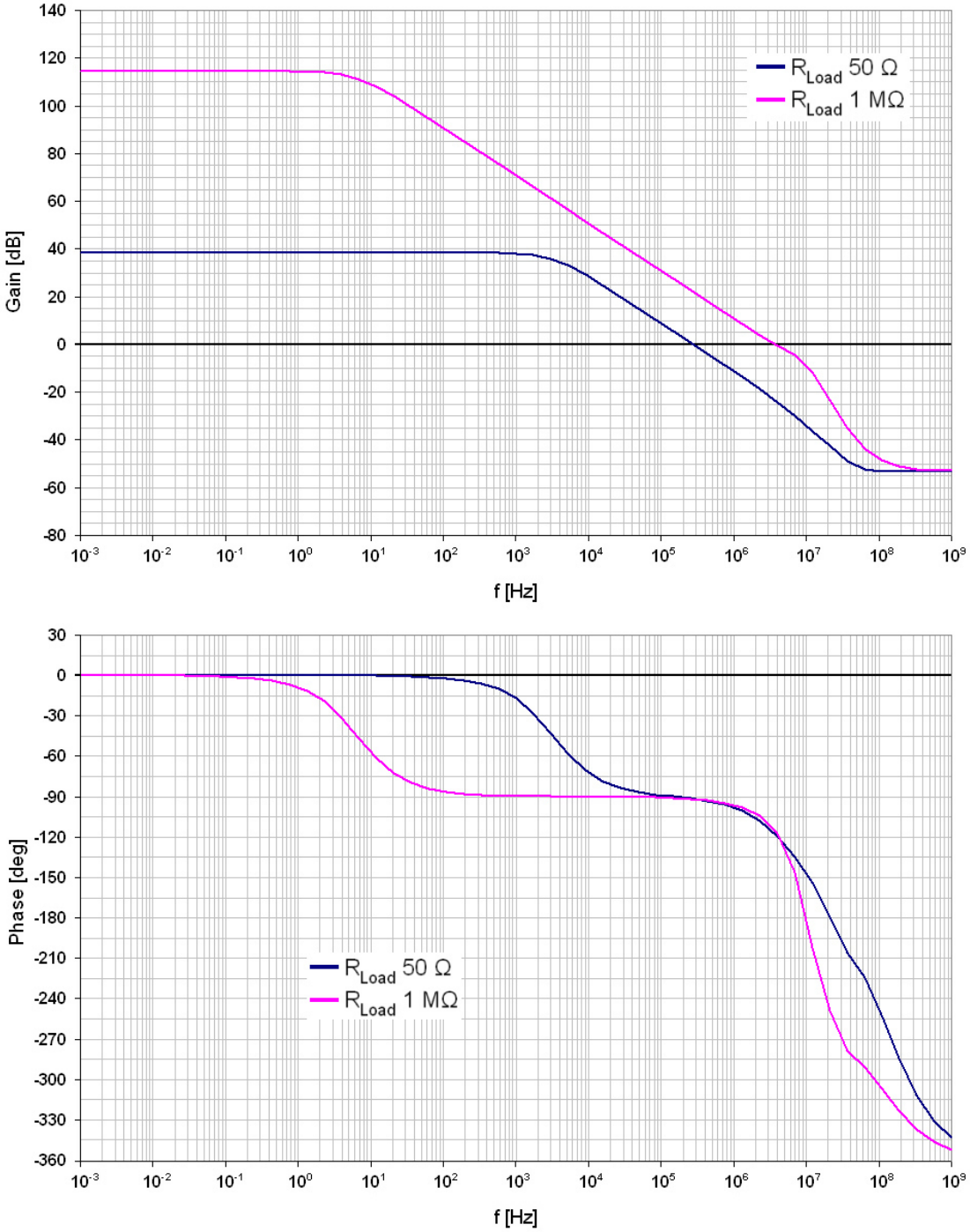

Figure 5.3: Output OTA open loop Bode plot.

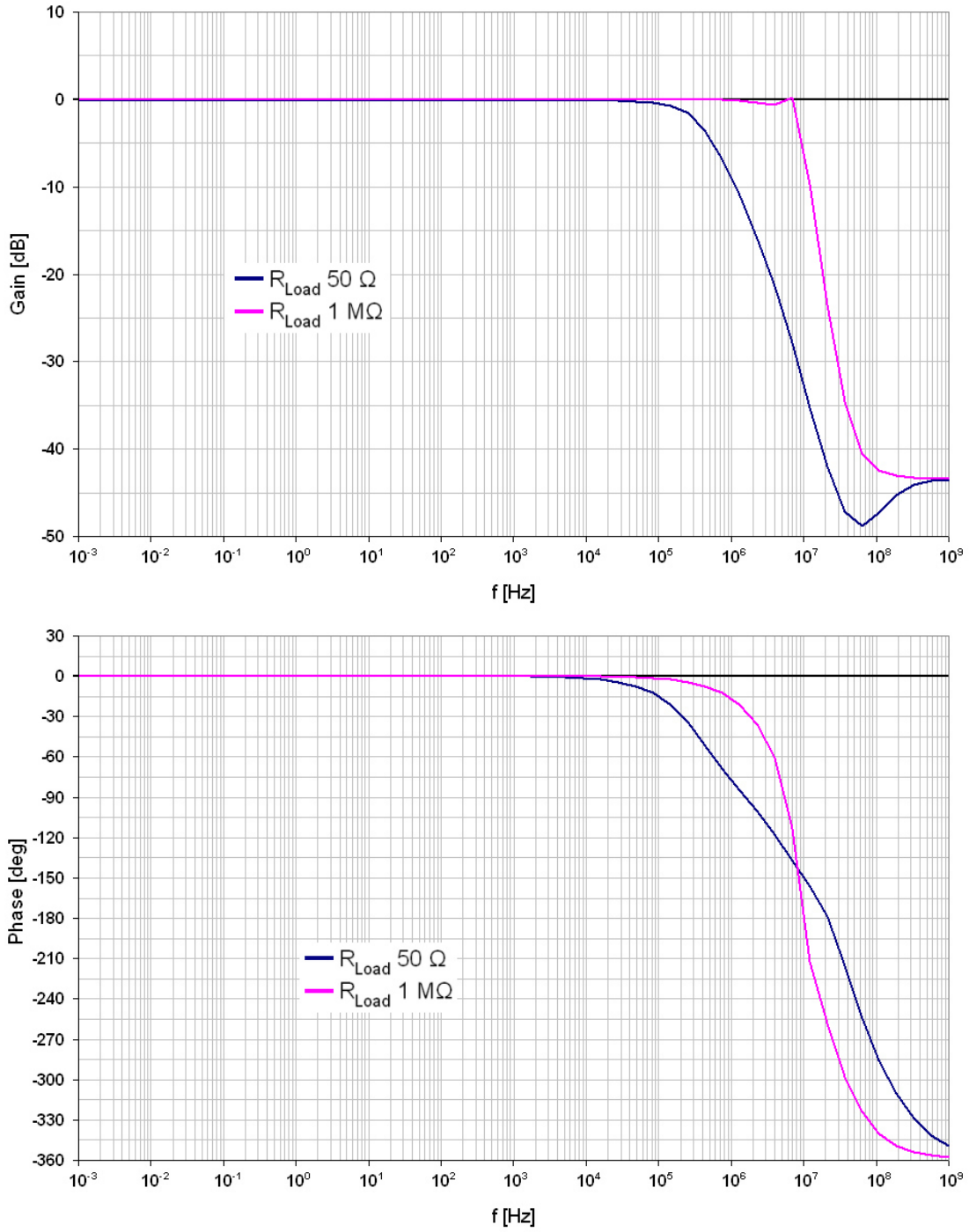

Figure 5.4: Output Buffer Bode plot.

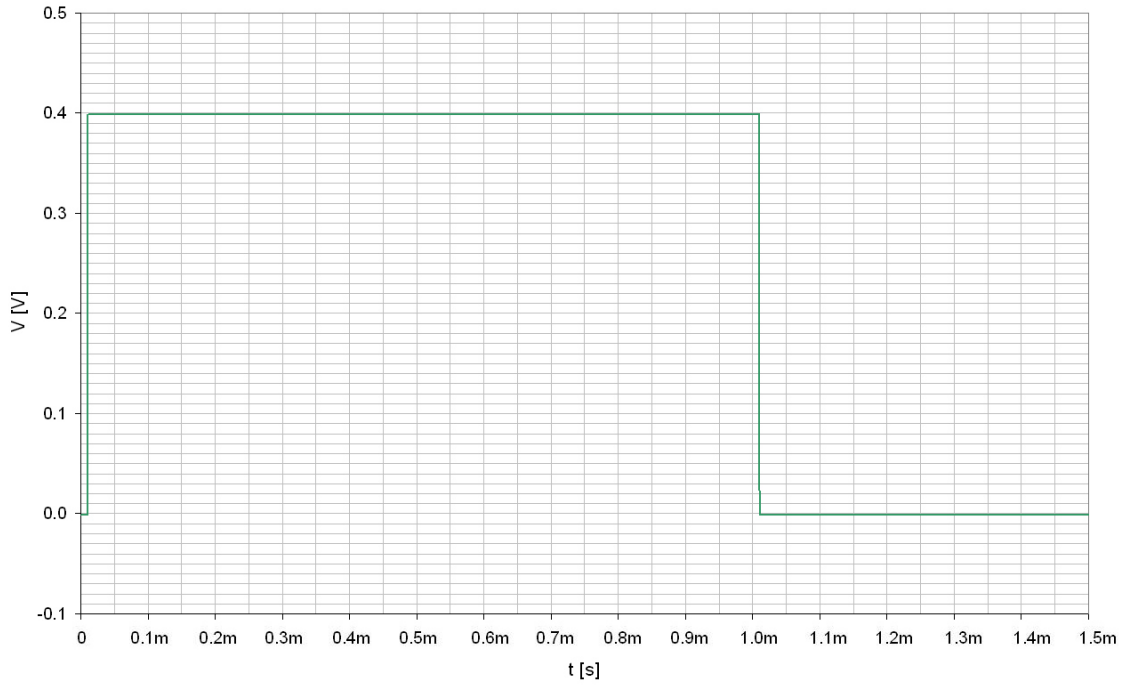

Figure 5.5: Output Buffer transient simulation with 50Ω load.

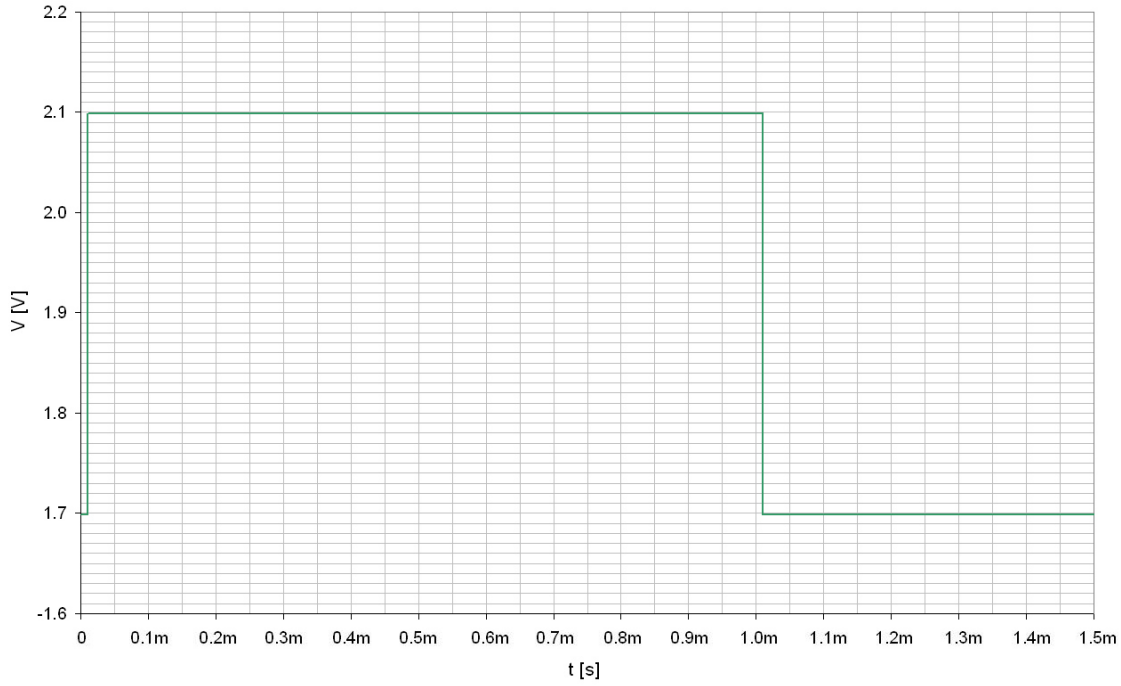

Figure 5.6: Output Buffer transient simulation with $1M\Omega$ load.

5.2 AFE simulations

The design of the Analog Front End at the schematic level is complete. Now it is possible to proceed with the simulations on the complete chain. The simulations are done using dual power supply with $\pm 1.65V$.
In Figure 5.7 the AFE scheme is shown.

Transfer Function

We want to compare our circuit with the commercial chips transfer function. This comparison is an important test, because the commercial chips are widely tested and their transfer function is optimized to filter and amplify properly the neural signals. Table 5.2 shows the results of the corner AC and DC simulation.
In the worst cases there is a notable change of the low pass cut off frequency, these variation could be compensated with by tuning the cut off frequency of the filter stage.

	TM	WS	WP
A_v^{AFE}	$67.39dB$	$67.28dB$	$67.39dB$
f_H^{AFE}	$380mHz$	$380mHz$	$390mHz$
f_L^{AFE}	$5.2kHz$	$4.6kHz$	$7.6kHz$
V_{DC}^{out}	$1.9mV$	$11.1mV$	$2.6mV$

Table 5.2: AFE AC and DC simulations.

The gain of AFE is stable in the different corner cases around the value of $67.3dB$. In the bandwidth of interest the phase is $-180deg$, so it inverts the signal.
The transfer function calculated through the simulation is comparable with the AC response of the commercial system, which have a bandpass from few Hz to $\approx 3kHz$.
In Figure 5.9 the results of the transient analysis in the worst cases are shown.

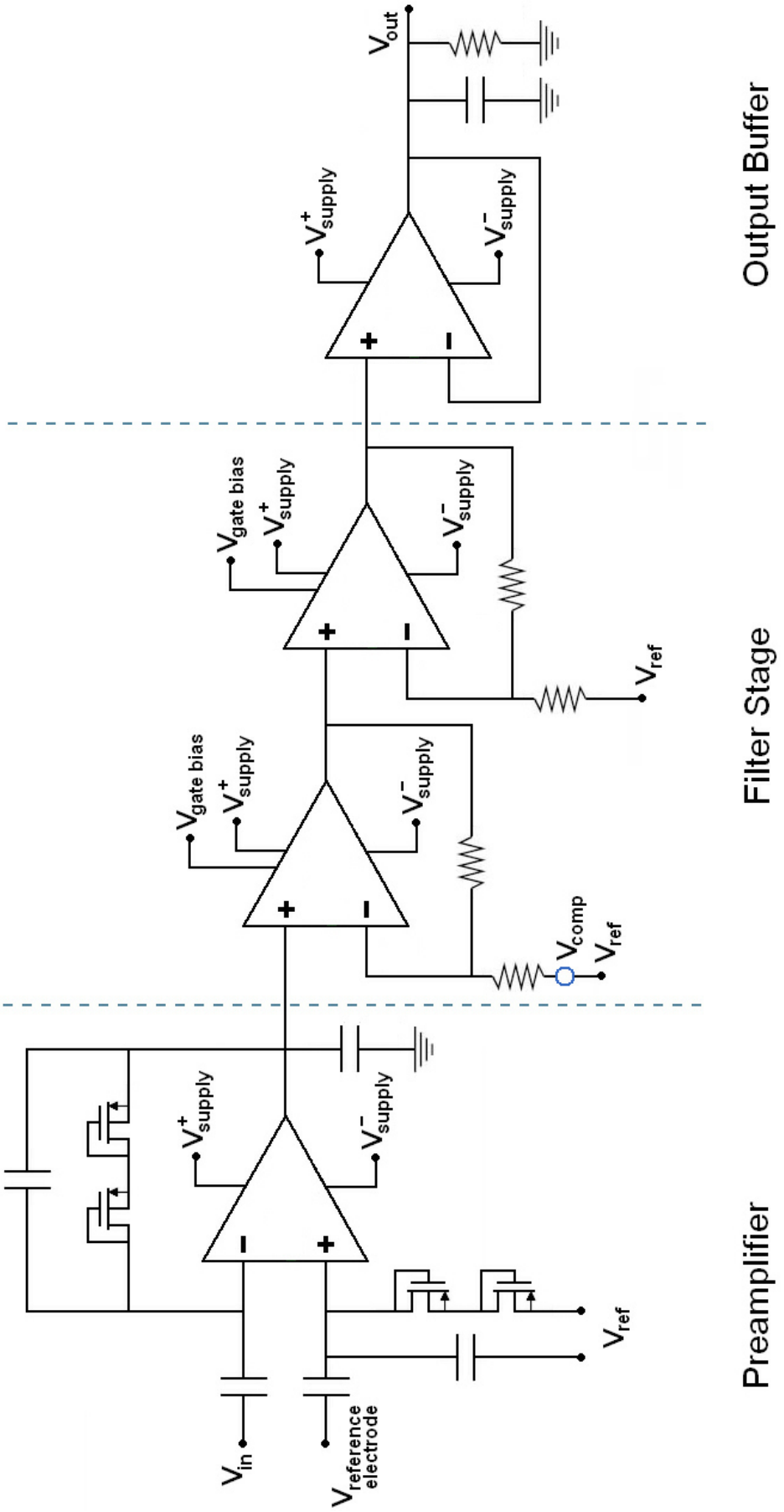

Figure 5.7: AFE scheme.

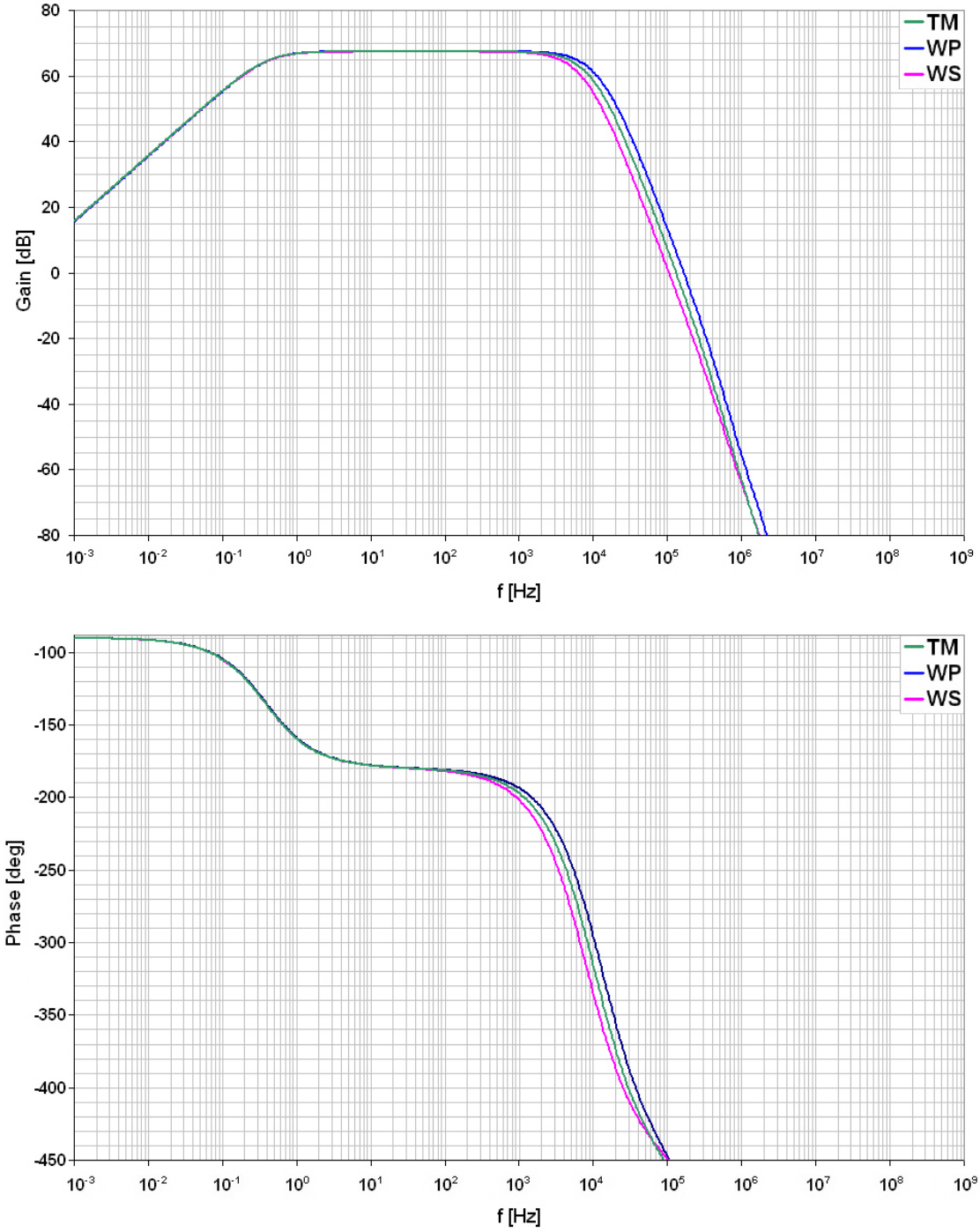

Figure 5.8: AFE open loop Bode.

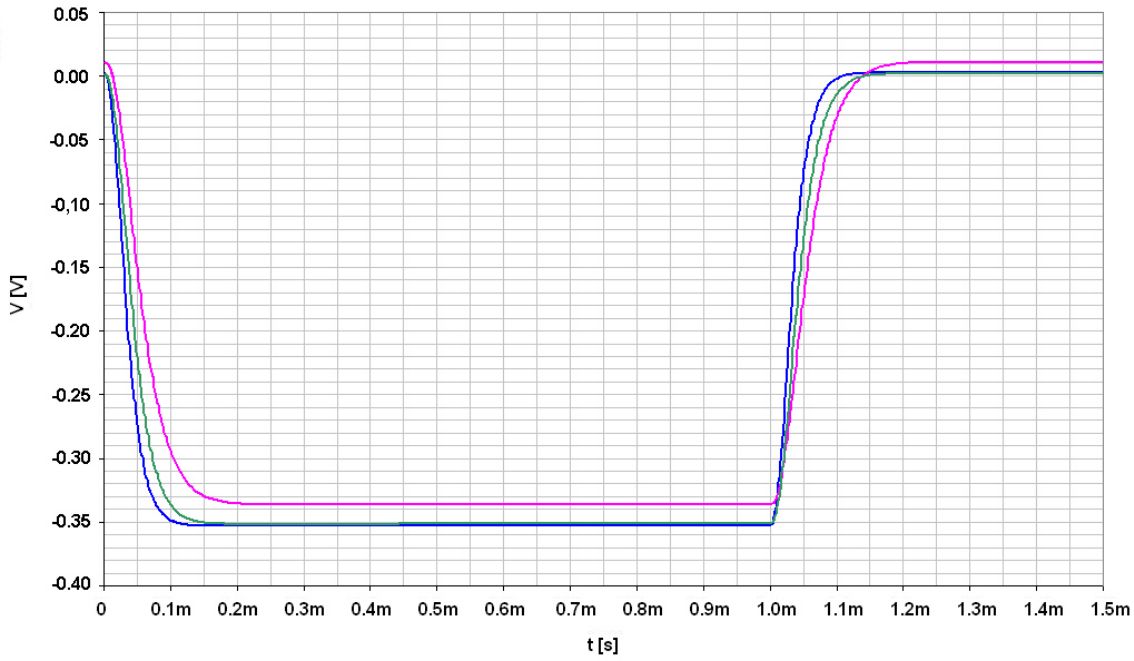

Figure 5.9: AFE worst case transient simulations.

Output Linearity

Transient simulations with signals of different amplitude are done to calculate the AFE linear response range.

As test signal a square wave with steep edges is used, its amplitude varies from $-500\mu V$ to $500\mu V$. The output voltage can be described by the following equation:

$$V_{out} = A_v \cdot V_{in} + \epsilon \tag{5.2}$$

Fitting the graph in Figure 5.10 with Equation 5.2 in the range $-350\mu V$ - $+400\mu V$ the following parameters are obtained:

$$A_v = 2359.51 \pm 0.35$$

$$\epsilon = (-245.02 \pm 29.94)\mu V$$

With the χ^2 test is obtained $\chi^2 = 0.75$ with 15 degrees of freedom, for this value the fit is acceptable with a 99.5% of confidence level.

So it is possible to assert that for a signal in the range between $-350\mu V$ and $+400\mu V$

the circuit has a linear response. Therefore a typical neural signal which has a peak-to-peak value of $\approx 150\mu V$ could be amplified without distortions.

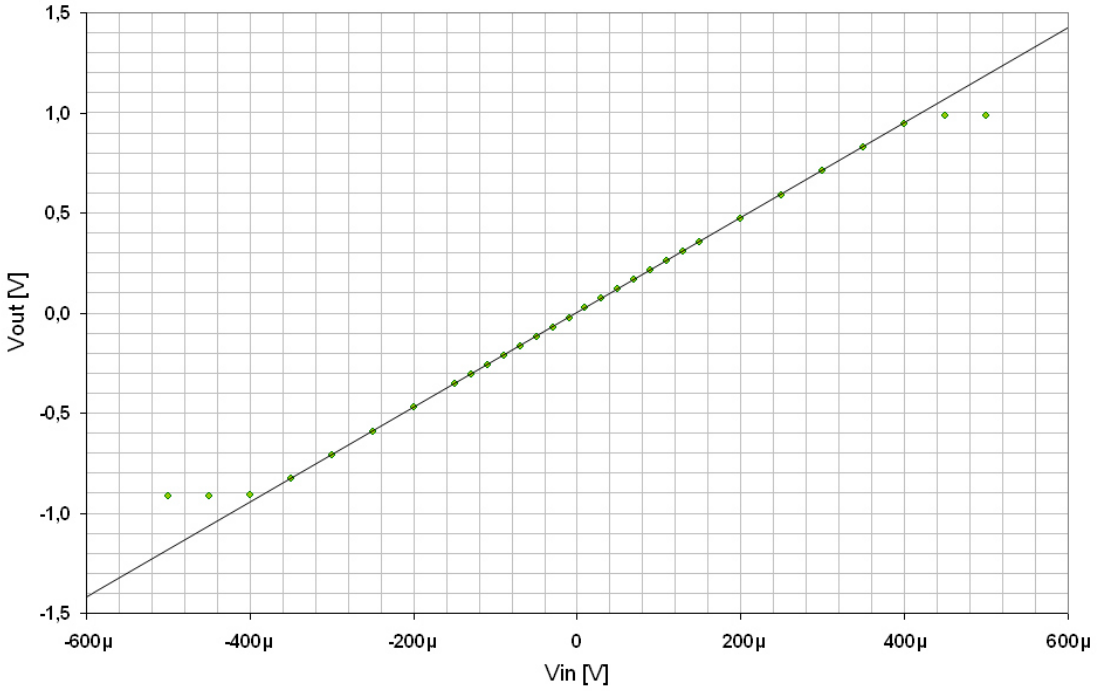

Figure 5.10: AFE Linearity.

Monte Carlo Analysis

To simulate the circuit response variation due to the mismatch and process variation effects a Monte Carlo analysis is done.

In Figure 5.11 the results of the Monte Carlo simulations are shown.

The output offset has a mean value of $-43\mu V$ and a gaussian distribution with a $\sigma = 18mV$. This means that an output DC level in the range $-54mV$ - $+54mV$ must be expected from each channel.

The gain of the AFE taking into account the process variation and mismatch is $A_v^{AFE} = 2355.4 \pm 10.6$ $(67.44 \pm 0.4dB)$.

The error of the gain value is the standard variation of the results obtained with Monte Carlo simulation. In the corner analysis are considered only the worst case

and it gives a pessimistic evaluation.

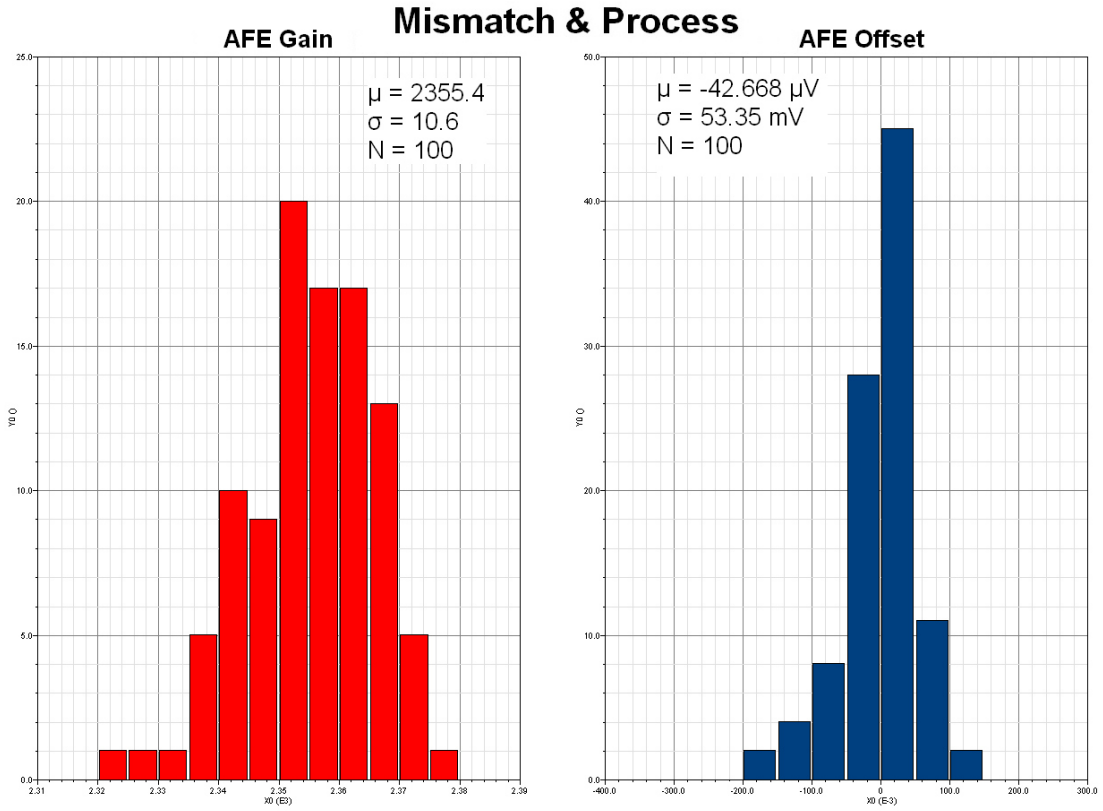

Figure 5.11: AFE Mismatch and process variation.

Temperature dependent analysis

A temperature dependent AC and DC analysis is done to study the response of the circuit at different working temperature. In Figure 5.12 the results are shown.
The variation of the DC output offset is $\approx 10mV$, and it is 10 time lower than the offset variation due to the process variation and mismatch.
The influence of the temperature on the circuit gain is $\approx 0.1dB$ and it is negligible compared to the total gain value.

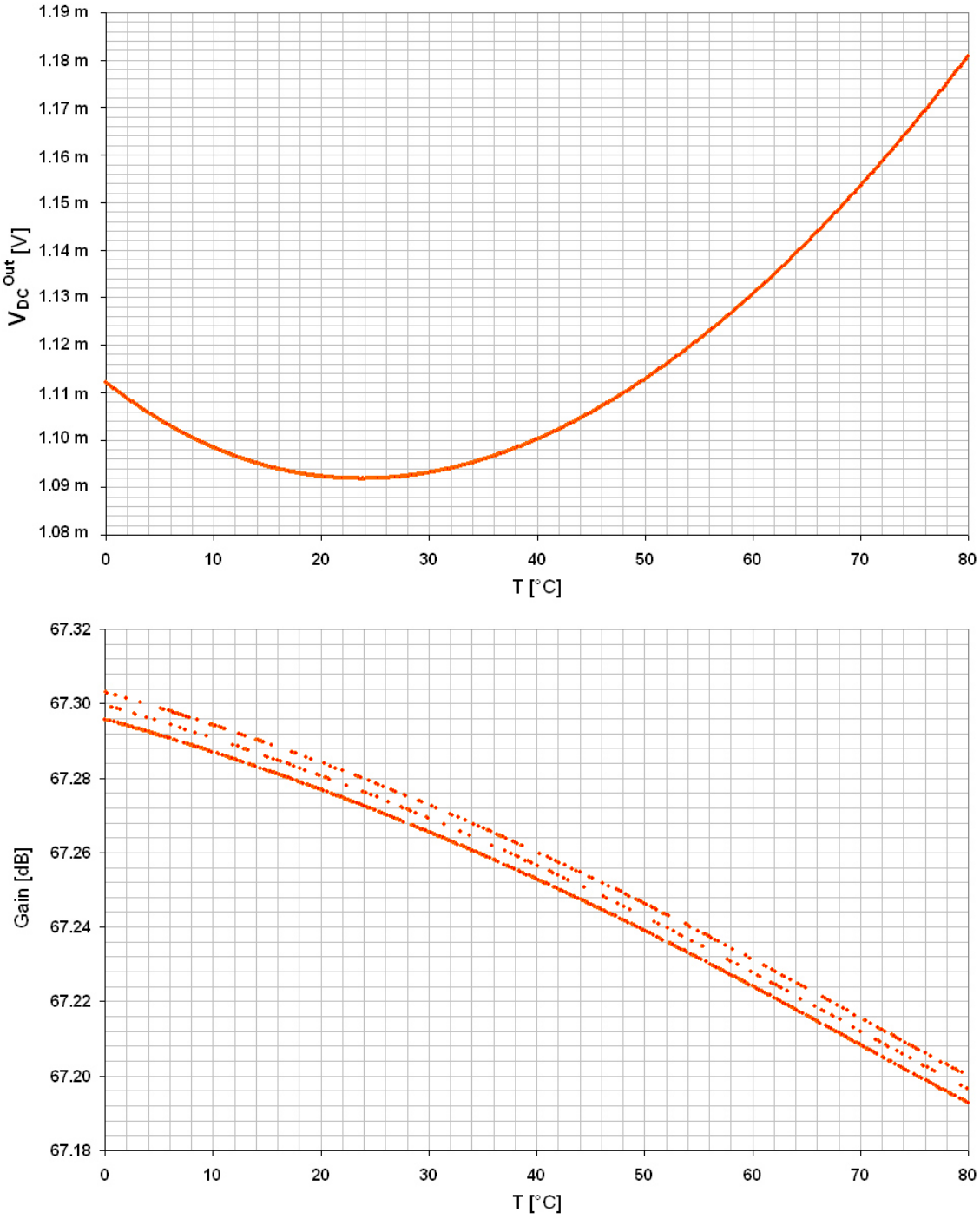

Figure 5.12: Output Buffer temperature dependent analysis.

Noise Analysis

The noise is the most critical factor, because it could alter the recorded signal. So it has to be as low as possible.
To evaluate the noise performance of the circuit a noise analysis is done.
Table 5.3 shows the output noise contribution of the circuit components. The main contributors are the preamplifier input transistors as expected.

Device	Type of Noise	Noise Contribution	% Of Total
Preamp/M1	thermal	$5.86 \times 10^{-6} V^2$	17.13
Preamp/M2	thermal	$5.85 \times 10^{-6} V^2$	17.09
Preamp/M6	flicker	$3.57 \times 10^{-6} V^2$	10.44
Preamp/M5	flicker	$3.56 \times 10^{-6} V^2$	10.40
Preamp/M4	flicker	$3.12 \times 10^{-6} V^2$	9.11
Preamp/M3	flicker	$3.11 \times 10^{-6} V^2$	9.08
Preamp/M8	thermal	$8.09 \times 10^{-7} V^2$	2.36
Preamp/M7	thermal	$8.06 \times 10^{-7} V^2$	2.36
Preamp/M6	thermal	$7.52 \times 10^{-7} V^2$	2.20
Preamp/M5	thermal	$7.50 \times 10^{-7} V^2$	2.19

Table 5.3: Analog Front End Integrated Noise Summary (in V^2) Sorted By Noise Contributors.

Figure 5.13 show the AFE output noise spectrum.
The value of total input referred voltage noise of our AFE design is $V_{irn} = 2.34\mu V$, so the noise requirements are met.

Amplification of a Neural signal

The final test on our AFE design is a transient simulation with in input a typical neural signal. In Figure 5.14 a typical action Potential signal is shown.
The cell - electrode coupling is modelized in a simple way through a RC high pass filter ($R_{seal} \approx 500\Omega$, $C_{membrane} \approx 1pF$). In Figure 5.15 the signal at the electrode is shown. Figure 5.16 shows the signal at the output of the analog processing chain.

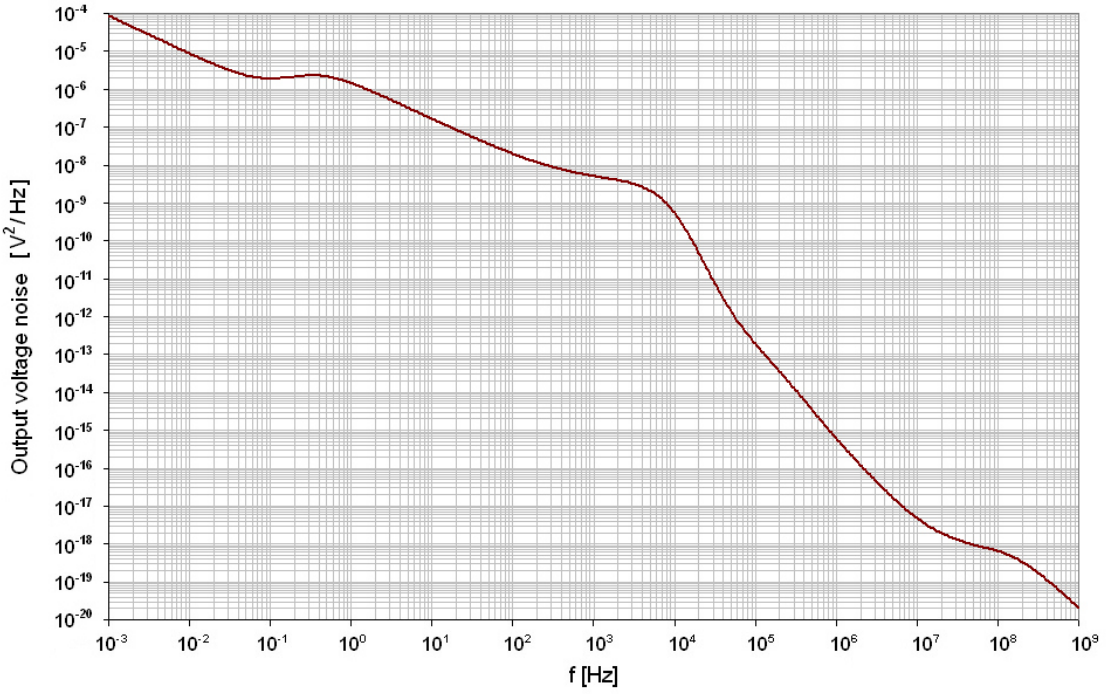

Figure 5.13: AFE output noise spectrum.

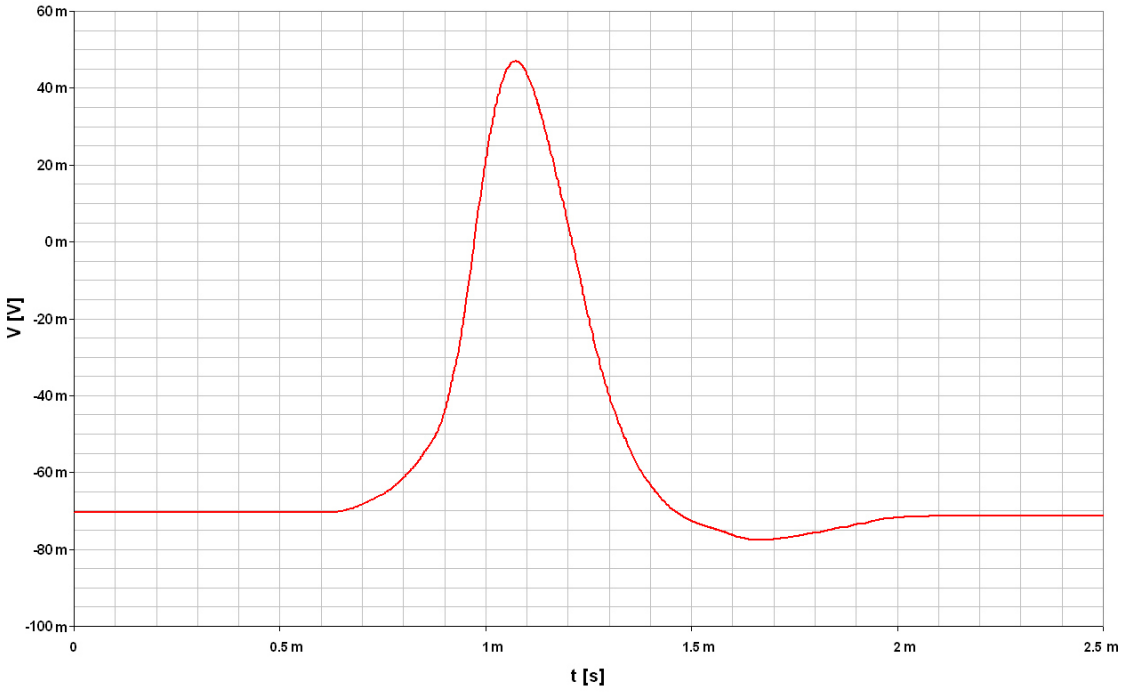

Figure 5.14: A typical Action Potential signal.

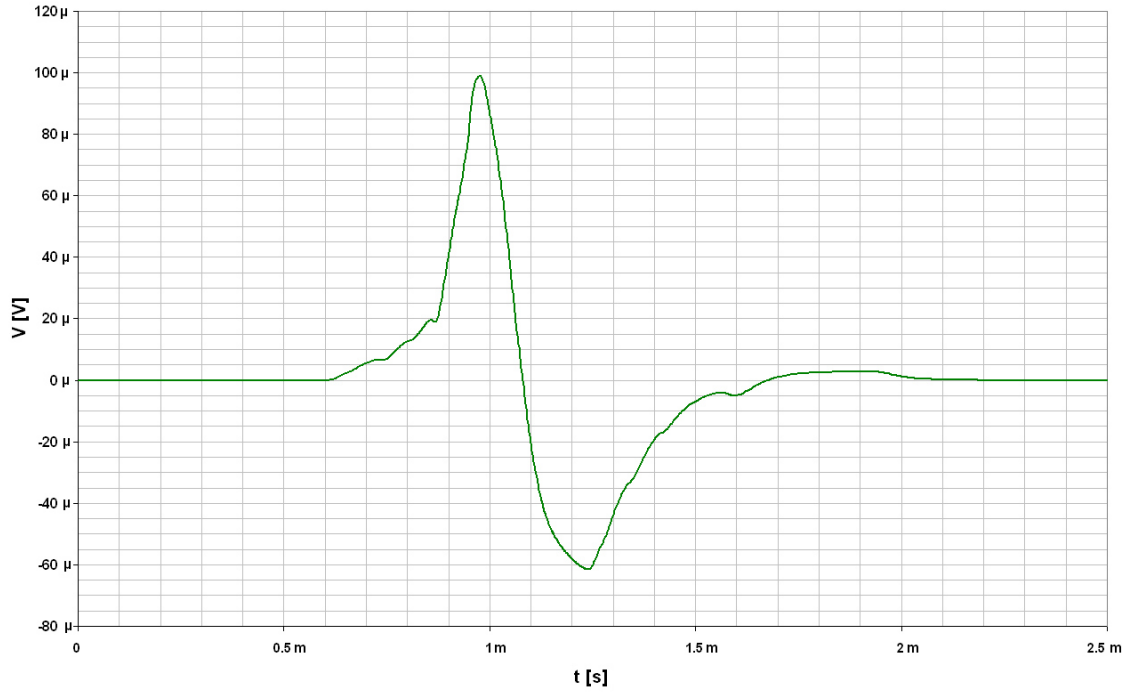

Figure 5.15: AFE input signal.

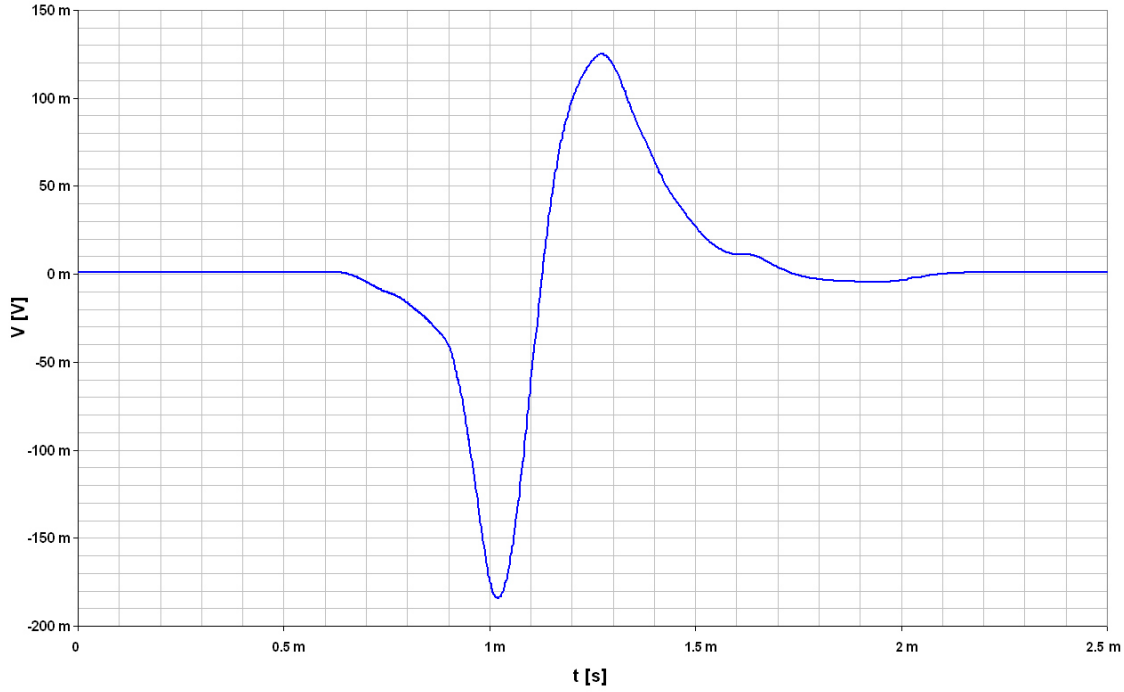

Figure 5.16: AFE output signal.

Conclusions and future work

The aim of this work was to do a feasibility study of an Analog Front End for neural signal read by diamond microelectrode.
The diamond is a new electrode material. Its surface becomes conductive through the hydrogenation process, and it has many interesting properties; the most important are regulable surface conductivity, biocompatibility and optical transparency.
The noise level of the diamond microelectrodes is lower than the metal ones, so it becomes important to minimize the noise introduced by the electronic amplification instrumentation.
Actual commercial recording systems are made of discrete components, to reduce the dimension of the circuit and comply with the noise requirement we choose to design an integrate circuit in CMOS AMS $0.35\mu m$ technology.
A complete processing channel for neural signal recording has been simulated. It is composed by three stages:

- Preamplifier, with differential input and single ended output. It has a gain of 100 with pass band behavior between $380mHz$ and $10kHz$. To achieve this very low cut off frequency with integrated component a mos-bipolar pseudoresistance is exploited($\approx 10^{12}\Omega$).
  Particular attention is given in the design of the OTA to minimize the noise and the power consumption ($59.4\mu W$).

- Filter Stage, composed by two OP-AMP filter designed with gm/C technique. It has a gain of 25 with a low pass cut off frequency tunable in the range $1.7kHz$ and $6.5kHz$. Since the offset is a critical factor in this stage it has been provided of an offset compensation system.

- Output Buffer, in a standard configuration in class AB with two stage and Miller compensation.

The supply voltage is selectable among $3.3V$ and $0V$ or $1.65V$ and $-1.65V$, in the first case the output load resistance can be 50Ω, in the second case of $1M\Omega$.
The complete circuit has a bandpass between $380mHz$ and $5.2kHz$ with a gain of ≈ 2500. The total input referred noise is $V_{irn} = 2.34\mu V$. The low pass cut off frequency could be reduced tuning the filter stage. In this way it is also possible to reduce further on the noise.
This design could be improved by making the gain of the AFE programmable. For example the gain of the preamplifier can be controlled changing the feedback capacitance, through a set of switches.
The next step of the work is to design the circuit layout and to fabricate a test chip.

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