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Integrated Front-End Electronics for High Precision Timing Measurements with Radiation Detectors

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Introduction

The need for the precise measurement of the energy and time associated to the passage through matter of a quantum of radiation is of primary importance in a number of scientific fields and motivates the development of very specific and highly performing detector systems. Nowadays, silicon technologies, such as hybrid pixel systems, represent a mature tool for the implementation of medium and large scale radiation detectors. The pressing research goals, together with the constant improvement in silicon detector performance, calls for the development of custom readout front-ends with more and more ambitious specifications. Consequently, modern CMOS technologies found a rich soil for the development of dedicated integrated systems with optimized custom functions. The implementation of systems for energy and time measurements require complementary optimization of the front-end electronics.

Nowadays, the vast majority of developed front-ends for silicon detectors focuses on energy measurement. This work describes the design, realization and test of integrated front-end electronics for precise timing with silicon pixel sensors. The study was part of the R&D activity for the Gigatracker (GTK), the beam spectrometer of the NA62 experiment.

Key timing issues and techniques are presented in Chapter 1. The purpose is to present the various factors affecting the resolution of a time measuring system and to provide the analysis of some of the most relevant techniques used to cope with them.

The experimental approach and the GTK specifications are described in Chapter 2. The GTK is formed by three stations of hybrid silicon sensors coupled to custom front-end ASICs. The input charge is distributed as a Landau centered at 2.4 fC, corresponding to a Minimum-Ionizing-Particle (MIP) in a 200 μm thick silicon detector. The sensor is biased at 500 V to ensure a collection time of the order of 3 ns. For a good efficiency the system must be able to detect signals from 1 fC to 10 fC with a time resolution better than 200 ps RMS. The pixel area is 300 μm x 300 μm and the allowed power consumption is 2 mW/channel. Since a significant part of the total power will be reserved to the digital logic, the power available for the analog front-end is of the order of 1 mW/channel. Moreover for this application it is important to convert the signals to fully differential as early as possible to reject the digital noise.

The implementation of a multichannel low power front-end with such an accurate timing capability is a challenging target in the present scientific panorama, where detectors tend to increase the number of channels in order to improve the granu-

larity. The implementation of the required performance in a circuit with an area and power consumption not yet reported in literature is the object of this work. Two complementary architectures have been developed at this scope in a 0.13 μm CMOS technology with a power supply of 1.2 V. The two solutions are presented and described in details, and the advantages and the drawbacks of each are pointed out in Chapter 3.

The attention in this work is on the novel pixel front-end design based on the Constant Fraction Discrimination (CFD) technique that meets the time resolution requirement of the experiment. It allows to directly compensate for timing errors due to signal amplitude variations, minimizing the overall calibration effort. The development of two prototypes of this architecture, together with their test results, are widely discussed in Chapter 4.

The experience acquired in the first phase of the work has shown that statistical pulse shape variations in the sensor contribute significantly to the timing accuracy of the system. This has led to a new design optimized to minimize the effect of signal shape variations on the measurement. The new circuit is presented in Chapter 5.

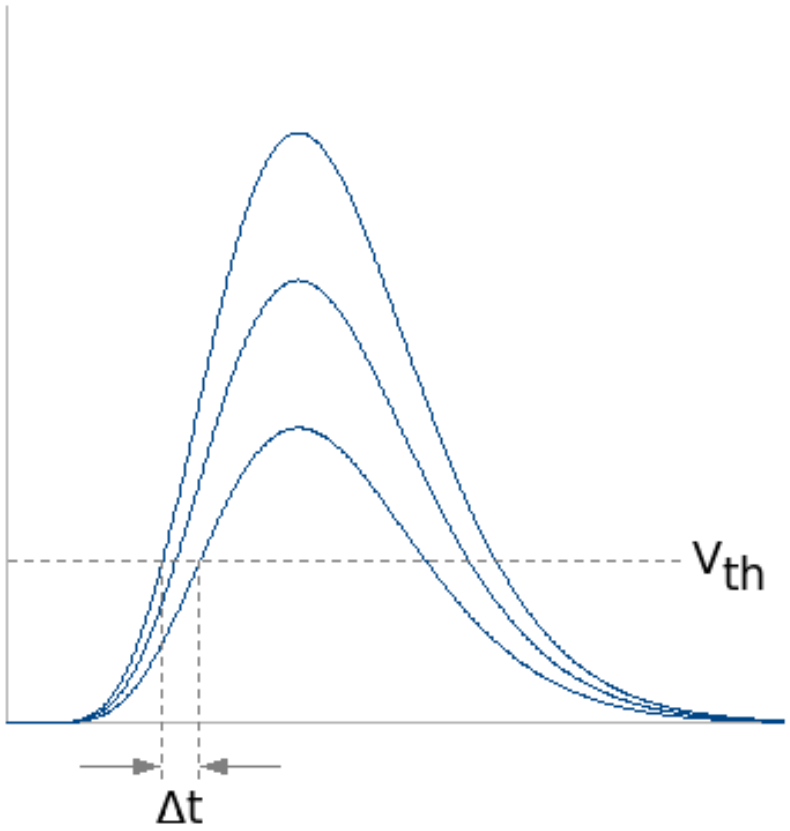
Chapter 1

Precise extraction of timing information from nuclear radiation pulses

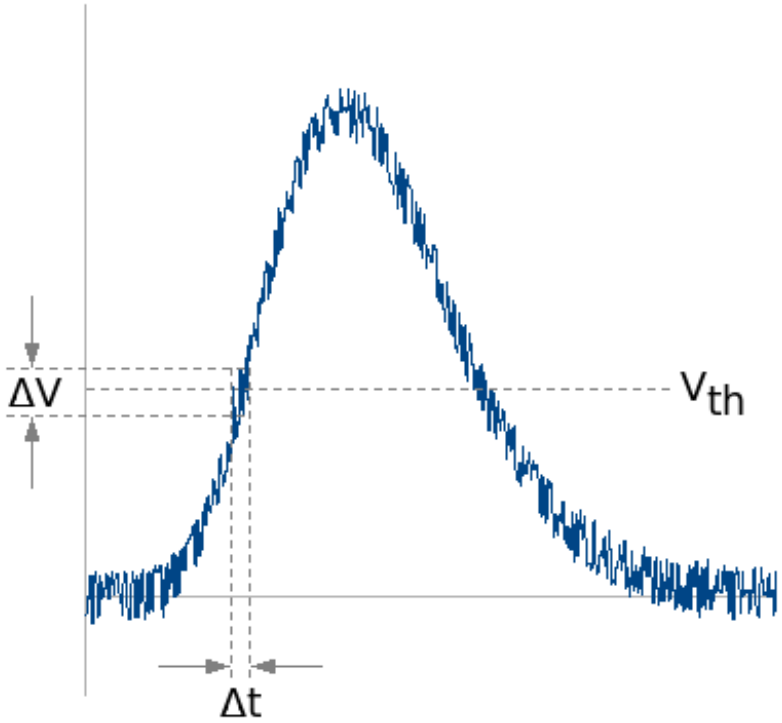
A nuclear radiation system consists of a set of detectors which sense the occurrence of a nuclear event coming from atomic or subatomic particles, gamma rays or X rays. In detector systems the energy of the incident radiation, or a part of it, is absorbed both through atom excitation or charge generation in the sensitive medium. In scintillators, for examples, the passage of the radiation excites the atoms which re-emit the absorbed energy in the form of light. The emitted light is then collected by a photomultiplier tube (PMT) and converted into electrons. In semiconductor detectors the electron-hole pairs are generated in an electric field by the incident radiation. A current pulse is produced as the charge is collected at the electrodes. In both cases the signal is proportional to the energy absorbed in the detector. In some application it is sufficient to detect the presence of a hit. Therefore the front-end electronics can be relatively simple. In other circumstances it is required to extract the information about the energy deposited in the sensor and/or to time tag the event with a resolution as low as 100 ps [1] [2]. This leads to a much more sophisticated readout electronics. This chapter reviews the optimization guidelines which are commonly applied for precise energy and time measurements, with a particular focus on the latter topic.

1.1 Principles of time pick-off

The measurement of the time of occurrence of an event is a key point in many applications [3] [4]. Ideally, a time pick-off circuit should generate a logic output pulse precisely related in time to the beginning of the signal and independent on its shape and amplitude. However, each time measurement is characterized by an error which defines the resolution of the system, i.e. its capability of resolving two different events [5]. The important sources of error which can occur are time walk, drift and jitter (see Fig. 1.1). The time walk is the displacement of the output pulse, relative to the effective occurrence of the event, due to amplitude variations of the input signal. The drift is the long term timing error induced by component aging



(A)



(B)

Figure 1.1: (A) Signal amplitude variations generating time walk and (B) jitter induced by noise

and temperature variations in the detecting system. Finally, the jitter is the timing uncertainty induced both by the electronic noise or by the statistical fluctuations of the signal from the detector.

In scintillator systems possible causes of timing error are the variations of the generation rate of photons in the scintillator and of their transit time through it, the fluctuations of the transit time of the photoelectrons in the PMT and the variations of the PMT gain. The first three sources affect the time of occurrence of the PMT signal and to some extent their shape, while the first and the last change the amplitude of the output signal.

In semiconductors the pulse shape is mainly dependent on the distribution of the charge generated by the detected radiation, on variations in charge collection time and in electron and hole mobilities due for example to non linearities in the electric field or to crystal defects or impurities. These important sources of error apply to the following principal types of time pick-off techniques [6].

1.1.1 Leading edge timing

Using a leading edge discriminator, where the input signal crossing a fixed threshold level generates the output pulse, is the simplest way of implementing a time measurement. However, the measured output time depends both on the amplitude and on the rise time of the input signal, making this option useful only in those applications involving a very narrow range of signal amplitudes and rise times. In Fig. 1.2 signals A and B with the same rise time and different amplitudes occur simultaneously, but cross the threshold at different times thereby generating time walk of the output logic pulse from the discriminator. Similarly, signals B and C, having the same amplitude but different rise times, introduce a walk error. The error is most pronounced for signals with longer rise times that only slightly exceed the threshold level.

Moreover, the leading edge discriminator introduces another contribution to the time walk called charge sensitivity. An additional quantity of charge is required to actually trigger the discriminator when the signal crosses the threshold. This phenomenon is illustrated in Fig. 1.2. The shaded area k represents the additional amount of charge required by the discriminator to switch. The times t_{10}, t_{20} and t_{30} at which the output signals actually occur differs from the times t_1, t_2 and t_3 at which the input signals cross the threshold of a variable quantity. To understand this point let's assume that the transfer function A(s) of the discriminator has a first order low pass behavior and that the circuit is driven by $V_{in}(s)$ being an ideal step with zero rise time. In the following equations v_{min} is the minimum input voltage that the discriminator can amplify, B is the ratio between the actual input signal and the minimum one and V_{OH} and V_{OL} are the voltages corresponding to a logic

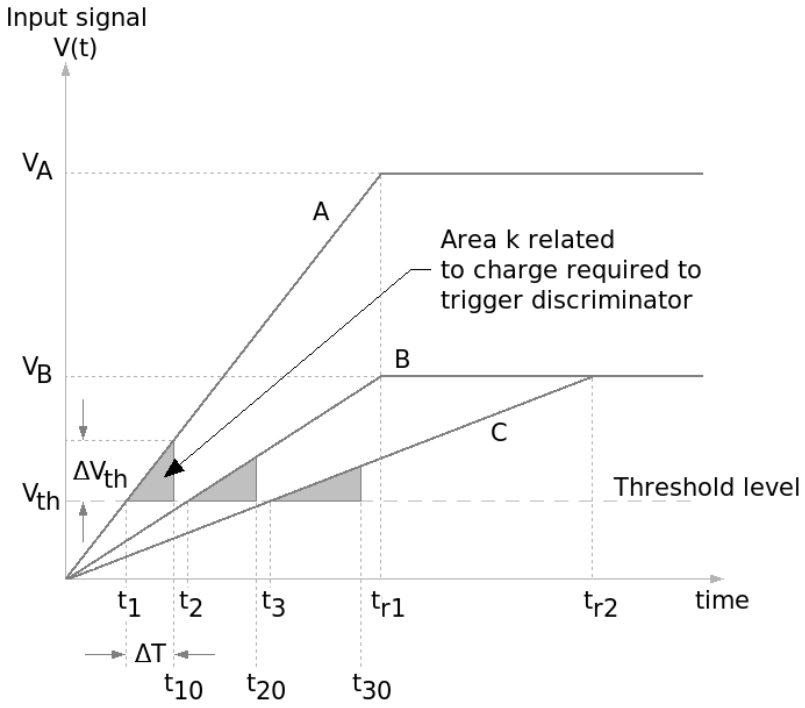


Figure 1.2: Time walk in leading edge discriminator due to amplitude and rise time variations and to charge sensitivity

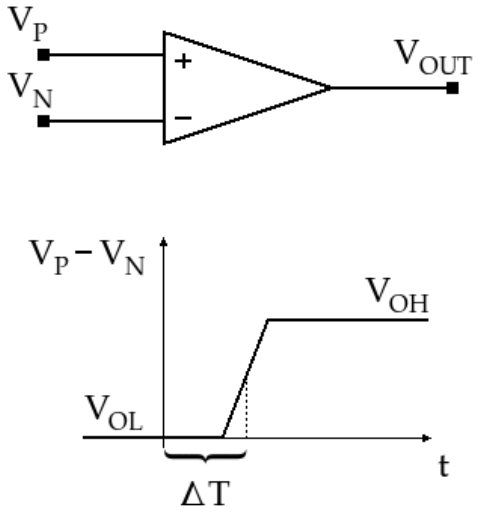


Figure 1.3: Leading edge discriminator output is affected by a propagation delay equal to the time needed by the output to reach the 50% of the signal, measured with respect to the threshold crossing time

one and to a logic zero valid signals respectively.

$$A(s) = \frac{A_0}{1 + s\tau_P} \tag{1.1}$$

$$V_{in}(s) = \frac{v}{s} \tag{1.2}$$

$$= \frac{Bv_{min}}{s} \tag{1.3}$$

$$v_{min} = \frac{V_{OH} - V_{OL}}{A_0} \tag{1.4}$$

In this case the delay ΔT taken by the output signal to reach half of the maximum output amplitude can be calculated from equation 1.5

$$\frac{V_{OH} - V_{OL}}{2} = \mathcal{L}^{-1}[A(s)V_{in}(s)]|_{\Delta T} \tag{1.5}$$

$$\frac{v_{min}A_0}{2} = Bv_{min}A_0(1 - e^{-\frac{\Delta T}{\tau_P}}) \tag{1.6}$$

$$\Delta T = \tau_P \ln(\frac{2B}{2B - 1}) \tag{1.7}$$

The delay introduced by charge sensitivity is shorter for higher signals, the result for $\tau_P = 100$ ns is plotted in Fig. 1.4. This value of τ_P is representative of the time constants that can be found in standard integrated discriminators.

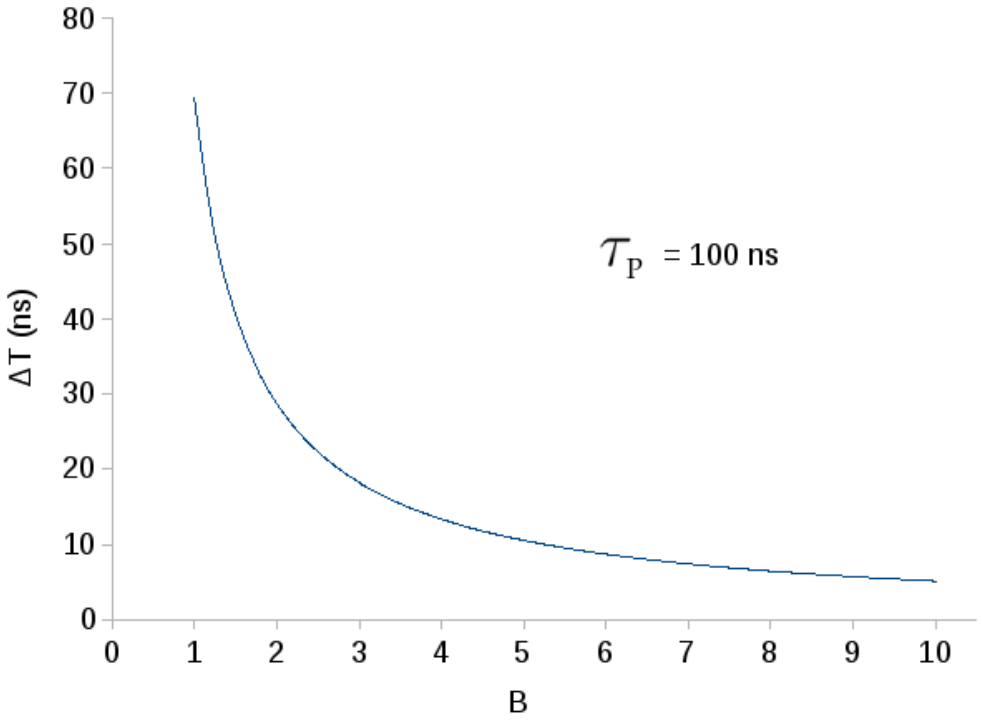


Figure 1.4: Propagation delay versus the ratio between the actual and the minimum detectable signal for $\tau_P = 100$ ns

For what concerns the jitter, the presence of noise will cause the signal to cross the threshold sooner or later with respect to the ideal case. Assuming a gaussian

probability density of noise amplitude with zero mean and a standard deviation σ_V, the time uncertainty σ_T in threshold crossing time for the leading edge discriminator is given with reasonable accuracy by [7]:

$$\sigma_T = \frac{\sigma_V}{\frac{dV(t)}{dt}|_{t=T}} \tag{1.8}$$

Considering a linear input signal V(t):

$$V(t) = \frac{At}{t_r} \tag{1.9}$$

where t_r is the peaking time, the jitter can be expressed as [8]:

$$\sigma_T = \frac{\sigma_V t_r}{A} \tag{1.10}$$

1.1.2 Constant fraction discrimination

The constant fraction method allows to implement accurate time measurement regardless of the pulse height, thus compensating for time walk. The idea is to create a variable threshold that tracks the signal always at a certain fraction of its maximum amplitude [9]. A functional representation of a Constant Fraction Discriminator (CFD) is shown in Fig. 1.5 [1]. It works by comparing a delayed copy

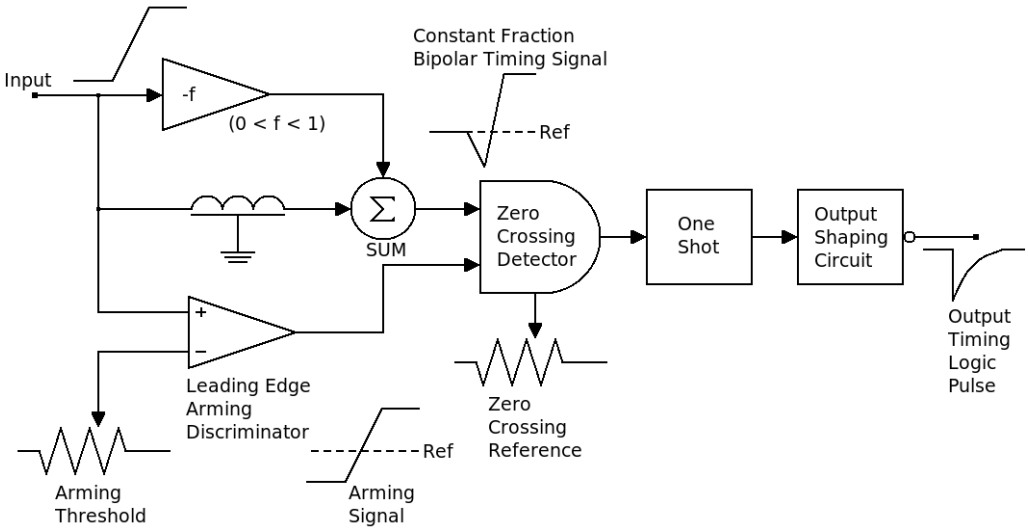


Figure 1.5: Functional representation of a CFD

of the signal with an attenuated and inverted one. The result is a bipolar signal whose zero crossing is detected and used to produce the logic output signal. A leading edge discriminator is used to gate the zero crossing one in order to prevent it from triggering on noise. A one-shot multivibrator is used to prevent multiple output signals from being generated in response to a single input pulse.

Altough difficult to implement, the CFD can provide excellent timing performance over a wide dynamic range of input signals. With this technique, time walk

due to rise time and amplitude variations is corrected and jitter can be minimized by properly choosing the delay t_d and the fraction f [10].

Let's start the analysis of the CFD by considering the elementary case of a linear signal with the leading edge given by equation 1.9. The output of the CFD is given by:

$$V_{CFD} = V(t - t_d) - fV(t) \tag{1.11}$$

If the zero crossing time T_{zc} occurs before the attenuated signal has reached its maximum amplitude A, it can be calculated as:

$$V(T_{zc} - t_d) = fV(T_{zc}) \tag{1.12}$$

$$\frac{A(T_{zc} - t_d)}{t_r} = \frac{fAT_{zc}}{t_r} \tag{1.13}$$

$$T_{zc} = \frac{t_d}{1 - f} \tag{1.14}$$

Ideally this condition eliminates the amplitude and rise time dependence of the zero crossing time, as illustrated in Fig. 1.6, since it depends only on the parameters of the CFD itself.

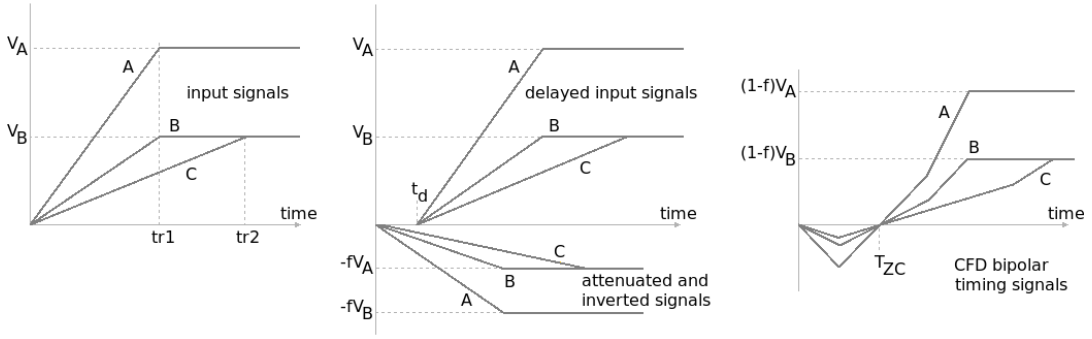


Figure 1.6: Signal formation in a CFD

The resulting bipolar waveform has an underdrive which should be high enough to be separated from noise. Lower values of delay and fraction lead to a smaller underdrive, thus the CFD parameters should be chosen appropriately considering the noise affecting the signal.

For a non linear input signal the rise time independence does not hold anymore. To illustrate this aspect let's consider the case in which the CFD algorithm is applied to the signal delivered by a CR-RC shaper. The pulse response of such a circuit is given by equation 1.15, where τ represents the peaking time and A a gain factor.

$$V(t) = Ate^{-\frac{t}{\tau}} \tag{1.15}$$

The zero crossing time is found comparing the delayed copy of the signal with the attenuated one (equation 1.16) and is given in equation 1.17.

$$A(T_{zc} - t_d)e^{-\frac{T_{zc} - t_d}{\tau}} = fAT_{zc}e^{-\frac{T_{zc}}{\tau}} \tag{1.16}$$

$$T_{zc} = \frac{t_d}{1 - fe^{-\frac{t_d}{\tau}}} \tag{1.17}$$

By inspecting equation 1.17 it can be noticed that the denominator now contains a dependence on the peaking time. In a CR-RC shaper the peaking time can be considered constant only when the collection time in the detector is much shorter than the peaking time. If this is not the case rise time variations in the detector signal will result in variations of the peaking time, introducing a jitter in the timing measurement. The sensitivity to peaking time variation can be minimized by using small values of the fraction f and/or small values of the delay time t_d. In fact if t_d is much less than τ equation 1.17 reduces to equation 1.14. However, as discussed above, the minimum fraction and delay are limited by the minimum underdrive amplitude required to trigger.

For what concerns the jitter, it is defined as:

$$\sigma_{Tzc} = \frac{\sigma_{V_{CFD}}}{\frac{dV_{CFD}(t)}{dt}|_{t=Tzc}} \tag{1.18}$$

where $\sigma_{V_{CFD}}$ is the standard deviation of the noise on the bipolar signal V_{CFD}, which is supposed to be linear in the region of the zero crossing time T_{zc}. The jitter can be related also to the noise affecting the input signal which is fed to the CFD, as reported in equation 1.19. In this expression it is assumed that the noise $v_n^2(t)$ on the input signal is a random process following a Gaussian distribution of amplitudes with zero mean value and standard deviation σ_V. $\Phi(t_d)$ is the autocorrelation function of the input noise. Furthermore the CFD is considered ideal, thus having infinite bandwidth and zero noise.

$$\sigma_{V_{CFD}} = \sigma_V \sqrt{1 + f^2 - \frac{2f\Phi(t_d)}{v_n^2(t)}} \tag{1.19}$$

For the uncorrelated noise case, which is the simplest and most frequent one [11], equation 1.19 is reduced to:

$$\sigma_{V_{CFD}} = \sigma_V \sqrt{1 + f^2} \tag{1.20}$$

Considering a linear input signal (see equation 1.9), the slope of the bipolar signal at zero crossing is obtained by deriving equation 1.11:

$$\frac{dV_{CFD}(t)}{dt}|_{t=Tzc} = \frac{(1\text{-}f)A}{t_r} \tag{1.21}$$

Combining equation 1.21 with equations 1.18 and 1.20, yields to the following expression for the jitter induced by noise for linear input signals:

$$\sigma_{Tzc} = \frac{\sigma_V t_r \sqrt{1 + f^2}}{A(1\text{-}f)} \tag{1.22}$$

A comparison between equations 1.10 and 1.22 indicates that in identical noise conditions and for the same input signal, the jitter on the zero crossing of the bipolar signal is always higher than the jitter experienced by the leading edge discriminator. Moreover, the slope of the CFD signal (equation 1.21) is slower than the one of the input signal (equation 1.9), making the leading edge discriminator more robust to

the charge sensitivity effect. However in most practical applications an increase in jitter is a tolerable side effect if compared to the benefits deriving from the reduced sensitivity of the CFD to amplitude and rise time variations.

Other limitations to the CFD performance come from the non linearities introduced in the signal processing chain which unavoidably occurs when the circuit is implemented on silicon. This aspect will be dealt with in more detail in the following.

1.1.3 Amplitude correction

Another technique to correct for time walk induced by deterministic signal amplitude variations is to record in parallel to the time measurement the information about the amplitude of the signal [9]. Knowing the correspondence between the signal amplitude and the time walk error, allows to correct off-line the measured leading edge time. However all uncertainties in the amplitude measurement or in the time-walk-to-amplitude calibration curve affect the timing precision.

1.1.3.1 Waveform digitization

In principle, the maximum information for off-line correction is provided when the full signal waveform is digitized. This solution offers the best opportunities for precise timing, but involves a complex circuitry that can be afforded only in those applications where the area and the power consumption are not the major constraint. This technique is treated in detail in [12]. Digitization implies approximation, as a continuous signal distribution is transformed into a discrete set of values. To reduce the additional errors introduced by digitization, the discrete digital steps must correspond to a sufficiently small analog increment [7]. The minimum sampling time is determined by the minimum delay obtainable with the technology used. Nowdays, very precise timing can be achieved, thus extracting the maximum information about the signal. However during the acquisition of a signal the system cannot accept a subsequent event. This fact results in a high dead time, which is the sum of the times needed to acquire the signal, to convert it in a digital form and to readout the memory. The last contribution depends on the speed of data transmission and on buffer access. To reach resolutions of the order of tens of picoseconds, a sampling frequencies of about 50 GS/s and an analog bandwidth of the order of the GHz are required. Such a sampling frequency limits the maximum event rate which can be treated without introducing deleterious artifacts.

1.1.3.2 Time over threshold

In many applications, where full waveform digitization can not be afforded due to the complex circuitry and the power consumption required, other methods should be used to extract the amplitude information. A typical solution is the employment of the Time over Threshold (ToT) technique, based on the fact that the time spent by a signal above a given threshold depends in general on the signal amplitude. The practical implementation of ToT involves the use of a simple leading edge discriminator which track both the leading and the trailing edges of the input signals. Considering the triangular signal shown in Fig. 1.7, the times at which the signal

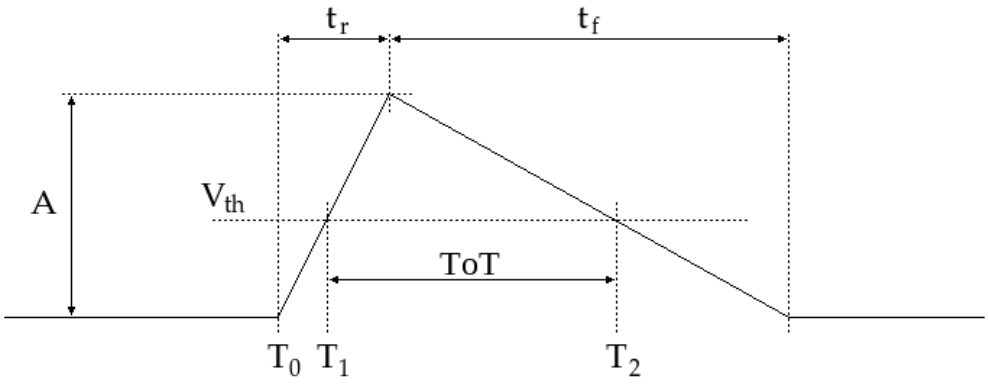


Figure 1.7: Triangular signal with a rise time t_r and a fall time t_f

crosses the threshold are defined as:

$$T_1 = \frac{V_{th} t_r}{A} \tag{1.23}$$

$$T_2 = t_r + t_f - \frac{V_{th} t_f}{A} \tag{1.24}$$

The corrected value is equal to:

$$T_0 = T_{1,meas} - \frac{V_{th} t_r}{A} \tag{1.25}$$

where $T_{1,meas}$ is the time measured by the leading edge discriminator. A in equation 1.25 is a function of TOT and can be calculated from equations 1.23 and 1.24.

$$ToT = T_2 - T_1 \tag{1.26}$$

$$= (t_r + t_f)(1 - \frac{V_{th}}{A}) \tag{1.27}$$

$$\frac{1}{A} = \frac{1}{V_{th}}(1 - \frac{ToT}{t_r + t_f}) \tag{1.28}$$

Putting equation 1.28 in equation 1.25, the resulting corrected time is:

$$T_0 = T_{1,meas} + t_r(1 - \frac{ToT}{t_r + t_f}) \tag{1.29}$$

Thus the time walk is given by:

$$\text{time walk} = t_r(\frac{ToT}{t_r + t_f} - 1) \tag{1.30}$$

and depends linearly on the ToT. This dependency is further complicated for non triangular input signals and due to non-linearity effects such as the charge sensitivity. Thus, typically the ToT technique implies a complex calibration.

The jitter σ_{T0} on the final value can be calculated as follows:

$$\sigma_{T1} = \frac{\sigma_V t_r}{A} \tag{1.31}$$

$$\sigma_{T2} = \frac{\sigma_V t_f}{A} \tag{1.32}$$

$$\sigma_{ToT} = \sqrt{\sigma_{T1}^2 + \sigma_{T2}^2} \tag{1.33}$$

$$\sigma_{T0} = \sqrt{\sigma_{T1}^2 + (\frac{t_r}{t_r + t_f})^2 \sigma_{TOT}^2} \tag{1.34}$$

$$= \frac{\sigma_V t_r}{A} \sqrt{1 + \frac{t_r^2 + t_f^2}{(t_r + t_f)^2}} \tag{1.35}$$

where σ_{T1} and σ_{T2} are respectively the jitter on the leading and trailing edges of the input signal due to noise σ_V. As expected, equation 1.35 shows that the error due to noise is higher than the jitter in the simple leading edge discriminator.

Due to the fact that the corrected time is a function of the measured time and of the ToT, the jitter on the final time is a function of the jitter on both the leading and the trailing edges. Since typically the signals are asymmetrical, the jitter on the trailing edge is higher than the jitter on the leading edge and the final ToT is dominated by the error made tracking the trailing edge.

On the other hand, the ToT approach has the advantage of being very simple to implement and ideally allows to compensate completely for the time walk error. However its functionality does not hold anymore if the curve ToT versus time walk changes. Thus, depending on the application, the system needs to be periodically calibrated to face variations in the input signal characteristics related for example to the detector aging. Moreover statistical changes in the rise and/or fall times of the input signal, thus in its shape, will affect the timing precision.

1.1.4 Crossover timing

One method to eliminate the dependency of the measured time from the amplitude of the input pulses is to derive the filtered signals to produce a bipolar waveform. For signals with the same rise time, the peak amplitude is reached always at the same instant, independently on the amplitude. Thus the derivative of the signals produces a bipolar signal which crosses the zero always at the same time, as illustrated in Fig. 1.8. The time walk due to the amplitude variations is reduced to the charge sensitivity of the zero crossing discriminator, however the zero crossing time is still a function of the input pulse shape.

Fig. 1.9 illustrates the implementation of a bipolar shaper with either RC-shaped or double delay line shaped pulses [1], where the second provide better time resolution. The resulting output signal is given for the two cases relatively by:

$$V_{RC}(t) = \frac{dV_{sh}(t)}{dt} \tag{1.36}$$

$$V_{DD}(t) = V_{sh}(t - t_d) - V_{sh}(t) \tag{1.37}$$

The RC-shaper implements the derivation of the signal and the zero crossing happens in coincidence of the peak amplitude of the input signal. The double delay line can

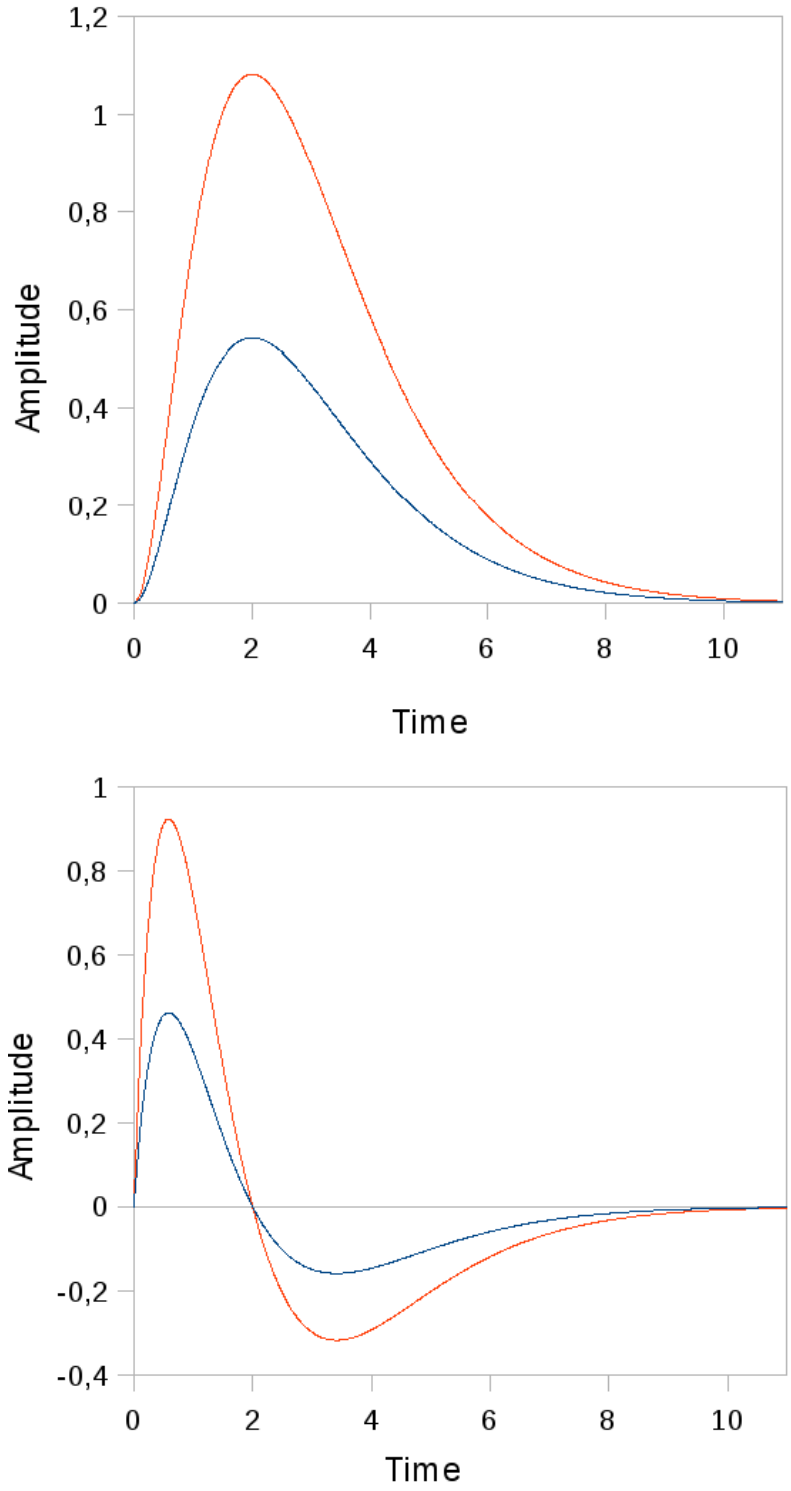


Figure 1.8: Principle of the crossover technique

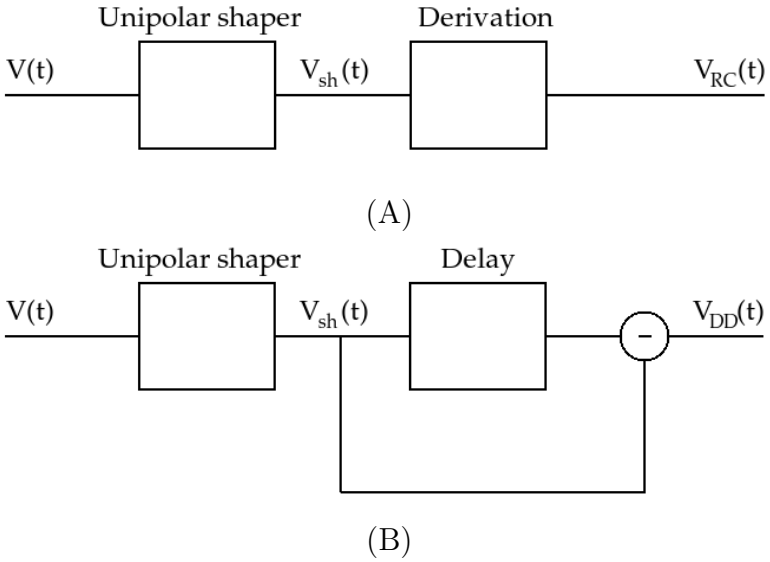


Figure 1.9: Block diagram of the two mostly used alternative to implement a bipolar filter starting from an unipolar shaper: (A) the RC shaper and (B) the double delay line

be treated as a particular case of a CFD with unitary fraction where the value of the delay is chosen in order that the zero crossing occurs at the peaking amplitude.

After having discussed the different techniques to minimize the amplitude sensitivity of the timing measurement let's focus now on the minimization of the effects of noise.

1.2 Optimum filtering for energy measurements

Timing and energy measurements require different optimization of the signal processing chain. To allow a better understanding of the tradeoffs that need to be addressed in the design phase both optimization strategies are now described. Let's start discussing the optimization for energy measurements [13] which is the one usually followed in the design of front-end electronics for standard silicon detector applications.

In a linear detector the signal charge is proportional to the energy deposited by the quantum of radiation. Thus the object of the measurement becomes the charge Q released by the radiation in the detector. The Equivalent Noise Charge (ENC) represents the error on the Q measurement and is defined as the amount of input charge necessary to have a Signal-to-Noise-Ratio (SNR) equal to the unity. To minimize the ENC a filter at the output of the preamplifier can be used [14] [15].

The signal and the noise at the output of the filter are given by:

$$\begin{aligned} v_o(t) &= Qs(t)*h(t) && (1.38)\\ &= Q\int_{-\infty}^{\infty} H(j\omega)S(\omega)e^{j\omega t}df && (1.39)\\ \sigma_n^2 &= \int_{-\infty}^{\infty} N(\omega)|H(j\omega)|^2 df && (1.40) \end{aligned}$$

where $Qs(t)$ is the signal to measure at the output of the amplifier, $N(\omega)$ is the noise spectral density introduced by the preamplifier itself and $H(s) = \mathcal{L}[h(t)]$ is the transfer function of the filter. Thus the SNR at the output of the filter at the instant t_m of the measurement results in:

$$SNR^2 = Q^2\frac{(\int_{-\infty}^{\infty} H(j\omega)S(\omega)e^{j\omega t_m}df)^2}{\int_{-\infty}^{\infty} N(\omega)|H(j\omega)|^2 df} \quad (1.41)$$

Let's consider the Schwartz inequality:

$$|\int_{-\infty}^{\infty} u_1(\omega)u_2(\omega)d\omega|^2 \leq \int_{-\infty}^{\infty} |u_1(\omega)|^2 d\omega \int_{-\infty}^{\infty} |u_2(\omega)|^2 d\omega \quad (1.42)$$

which becomes an equality for $u_1(\omega) = k' u_2^*(\omega)$, with k' an arbitrary constant. Applying equation 1.42 to equation 1.41 the result is:

$$\begin{aligned} u_1(\omega) &= H(j\omega)N^{\frac{1}{2}}(\omega) && (1.43)\\ u_2(\omega) &= \frac{S(\omega)e^{j\omega t_m}}{N^{\frac{1}{2}}(\omega)} && (1.44)\\ Q^2\frac{(\int_{-\infty}^{\infty} H(j\omega)S(j\omega)e^{j\omega t_m}df)^2}{\int_{-\infty}^{\infty} N(\omega)|H(j\omega)|^2 df} &\leq Q^2\frac{\int_{-\infty}^{\infty} N(\omega)|H(j\omega)|^2 df \int_{-\infty}^{\infty} \frac{|S(\omega)|^2}{N(\omega)}df}{\int_{-\infty}^{\infty} N(\omega)|H(j\omega)|^2 df} && (1.45) \end{aligned}$$

which leads to:

$$SNR^2 \leq Q^2 \int_{-\infty}^{\infty} \frac{|S(\omega)|^2}{N(\omega)}df \quad (1.46)$$

Equation 1.46 represents the upper limit to the SNR which is independent from the filter transfer function $H(s)$. The maximum SNR is obtained for:

$$H(j\omega) = k'\frac{S^*(\omega)}{N(\omega)}e^{-j\omega t_m} \quad (1.47)$$

In the case of white noise $N(\omega) = W^2$, equation 1.47 becomes:

$$H(j\omega) = \frac{k'}{W^2}S^*(\omega)e^{-j\omega t_m} \quad (1.48)$$

from which it can be calculated the transfer function of the optimum filter in the time domain:

$$\begin{aligned} h(t) &= \frac{k'}{W^2}s(t_m - t) && (1.49)\\ &= Ks(t_m - t) && (1.50) \end{aligned}$$

where K is an arbitrary constant. Thus the optimum filter output to an input delta signal is the reflected image of the input signal itself. Moreover, it is clear that s(t) must be known to implement the optimum filter.

The maximum SNR in presence of white noise is obtained if all the energy of the input signal is used, i.e. the best time to perform the measurement is at the end of the signal from the preamplifier:

$$\mathrm{SNR}^2_{\mathrm{max}} = \frac{\mathrm{Q}^2}{\mathrm{W}^2}\int_{-\infty}^{\infty}|\mathrm{S}(\omega)|^2\mathrm{df} \tag{1.51}$$

$$= \frac{\mathrm{Q}^2}{\mathrm{W}^2}\int_{-\infty}^{\infty}\mathrm{s}^2(\mathrm{t})\mathrm{dt} \tag{1.52}$$

Fig. 1.10 shows the familiar model of a radiation detector, where the input signal is $\mathrm{I_{in}} = \mathrm{Q}\delta(\mathrm{t})$ and C represents the overall capacitance at the input of the preamplifier, including the detector one [16] [17]. For simplicity, the preamplifier is assumed with infinite input impedance and bandwidth. Moreover the contribution of 1/f noise is not considered. The signal and the noise at the output of the preamplifier

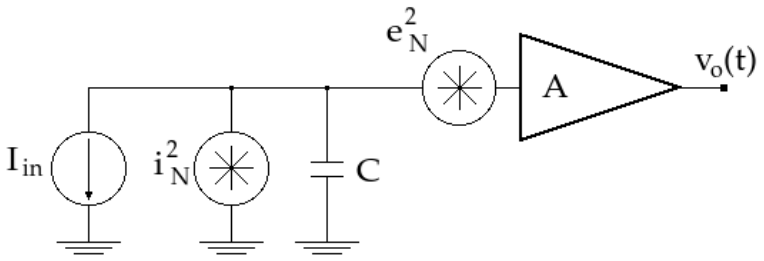


Figure 1.10: Block diagram of the detector and the preamplifier with noise sources

are:

$$\mathrm{V_o(s)} = \frac{\mathrm{QA}}{\mathrm{sC}} \tag{1.53}$$

$$\mathrm{N}(\omega) = \mathrm{A}^2(\mathrm{e}_\mathrm{n}^2 + \frac{\mathrm{i}_\mathrm{n}^2}{\omega^2\mathrm{C}^2}) \tag{1.54}$$

In this case the noise is not white, thus the signal is first processed with a whitening filter. Given the constant noise density W^2 at the output of the whitening filter, the transfer function $\mathrm{H_W(s)}$ should satisfy the following equations:

$$\mathrm{W}^2 = \mathrm{N}(\omega)|\mathrm{H_W}(\mathrm{j}\omega)|^2 \tag{1.55}$$

$$|\mathrm{H_W}(\mathrm{j}\omega)|^2 = \mathrm{H_W}(\mathrm{j}\omega)\mathrm{H_W^*}(\mathrm{j}\omega) \tag{1.56}$$

$$= \frac{\mathrm{W}^2}{\mathrm{N}(\omega)} \tag{1.57}$$

$$= \frac{\mathrm{W}^2\omega^2\mathrm{C}^2}{\mathrm{A}^2(\mathrm{i}_\mathrm{n}^2 + \mathrm{e}_\mathrm{n}^2\omega^2\mathrm{C}^2)} \tag{1.58}$$

$$\tag{1.59}$$

Thus the transfer function of the whitening filter is:

$$H_W(j\omega) = \frac{j\omega CW}{A(i_n + j\omega Ce_n)} \quad (1.60)$$

$$= \frac{W}{Ae_n}\frac{j\omega C\frac{e_n}{i_n}}{1 + j\omega C\frac{e_n}{i_n}} \quad (1.61)$$

$$= G\frac{j\omega\tau_c}{1 + j\omega\tau_c} \quad (1.62)$$

Considering equation 1.62 the whitening filter is formed by an ideal amplifier with gain $G = \frac{W}{Ae_n}$ followed by a CR differentiator with time constant $\tau_c = C\frac{e_n}{i_n}$ equal to the noise time constant. Referring to equation 1.54, $\omega_c = 1/\tau_c$ is the frequency at which the contributions of the parallel and series noises at the output of the preamplifier are equal, as shown in Fig. 1.11 [18]. It should be noted that the high pass filter after the integrator has the further function of avoiding the pile-up of events, as it will be discussed in the following section.

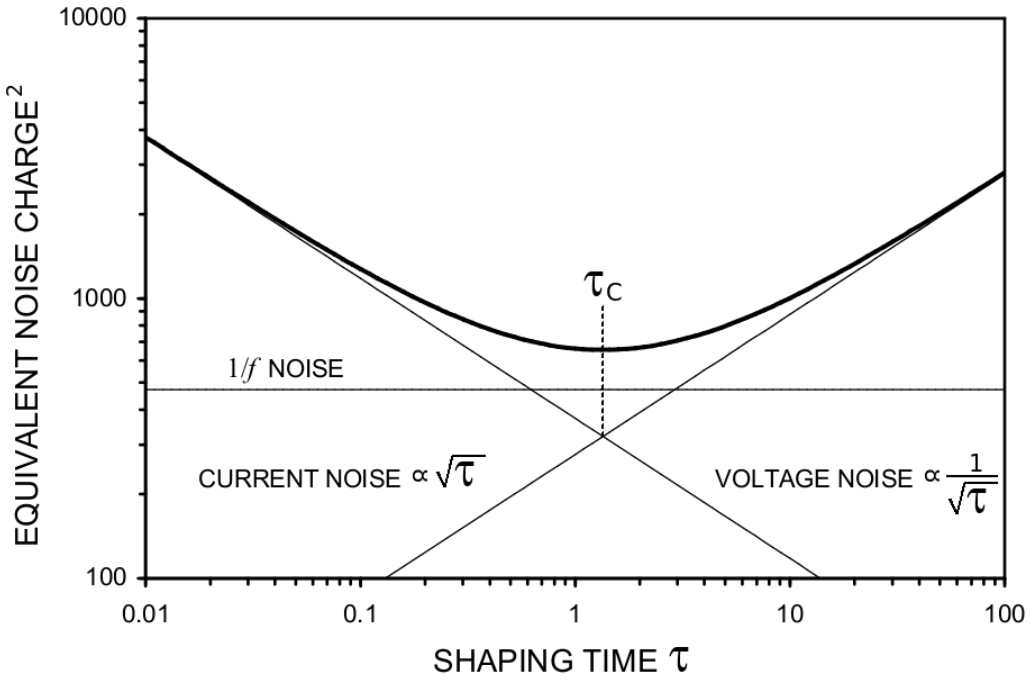


Figure 1.11: The dependence of the preamplifier noise contribution on the amplifier shaping time constant

Now, at the output of the whitening filter, the noise is white with a probability density W^2, but the signal which passed through the same filter has become:

$$V_W(s) = \mathcal{L}[v_W(t)] \quad (1.63)$$

$$= V_o(s)H_W(s) \quad (1.64)$$

$$= \frac{QW}{Ce_n}\frac{1}{s + \frac{1}{\tau_c}} \quad (1.65)$$

$$v_W(t) = \frac{QW}{Ce_n}e^{-\frac{t}{\tau_c}}\theta(t) \quad (1.66)$$

where $\theta(t)$ is the Heaviside step function. The optimum filter transfer function is obtained from equation 1.50:

$$h(t) = Ke^{\frac{t-t_m}{\tau_c}}\theta(t_m - t) \tag{1.67}$$

Considering that the maximum SNR is obtained if the measurement is performed at the end of the signal, t_m is infinite.

The output of the complete chain, formed by the amplifier, the whitening filter and the optimum shaper, is the convolution of equations 1.66 and 1.67:

$$\begin{aligned} v_{opt,E}(t) &= \int_0^\infty v_w(x)h(t\text{-}x)dx & (1.68)\\ &= \frac{KQW}{Ce_n}\int_0^\infty e^{-\frac{x}{\tau_c}}\theta(x)e^{\frac{t-t_m-x}{\tau_c}}\theta(x-t+t_m)dx & (1.69)\\ &= \frac{KQWt_c}{2Ce_n}[e^{-\frac{t-t_m}{\tau_c}}\theta(t-t_m) + e^{\frac{t-t_m}{\tau_c}}\theta(t_m-t)] & (1.70)\end{aligned}$$

The result is the indefinite cusp shown in Fig. 1.12 which reaches its maximum value at the time $t = t_m$:

$$\begin{aligned} v_{opt,E,max} &= \frac{KQW}{Ce_n}\int_0^\infty e^{-\frac{2x}{\tau_c}}dx & (1.71)\\ &= \frac{KQW\tau_c}{2Ce_n} & (1.72)\end{aligned}$$

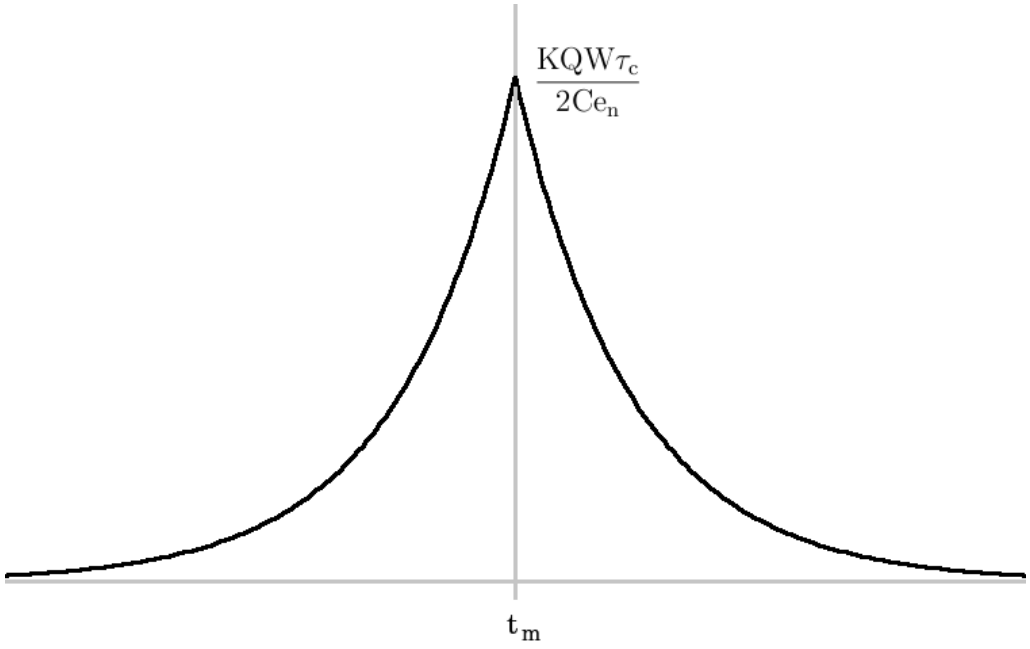


Figure 1.12: Output of the full chain composed by the amplifier, whitening filter and shaper for optimum energy measurement

The noise at the output of the optimum filter is given by:

$$\sigma_n = \sqrt{\int_{-\infty}^{\infty} W^2 |H(j\omega)|^2 df} \quad (1.73)$$

$$= W\sqrt{\int_{-\infty}^{\infty} h(t)^2 dt} \quad (1.74)$$

$$= W\sqrt{\int_{-\infty}^{t_m} K^2 e^{\frac{2(t-t_m)}{\tau_c}} dt} \quad (1.75)$$

$$= KW\sqrt{\frac{\tau_c}{2}} \quad (1.76)$$

The resulting SNR for the optimum filter is:

$$SNR_{opt} = \frac{v_{opt,E,max}}{\sigma_n} \quad (1.77)$$

$$= \frac{Q}{Ce_n}\sqrt{\frac{\tau_c}{2}} \quad (1.78)$$

$$= \frac{Q}{\sqrt{2Ce_n i_n}} \quad (1.79)$$

Thus the ENC is given by:

$$ENC_{opt} = \sqrt{2Ce_n i_n} \quad (1.80)$$

As already discussed, the assumption that all the information from the input signal is used implies that the insant of measurement t_m is delayed of an infinite time with respect to the event occurrence time. Moreover it is possible to use the apparatus to perform only one measurement since the output of the filter has an infinite duration. In fact, in case of multiple events, the peaks of the cusp following the first one would overlap to the tails of the previous cusps, resulting in an error in the amplitude measurement. This effect, called pile-up, can be prevented by adding a bound on the duration of the shaper output signal using only a part of the input information. The transfer function of a sub-optimum shaper with a finite output of duration t_l becomes:

$$h_l(t) = h(t)\theta(t - t_m + t_l) \quad (1.81)$$

The output of the filter, shown in Fig. 1.13, is given by the convolution of the transfer function $h_{textrml}(t)$ with the signal:

$$v_{sub\text{-}opt,E}(t) = \int_0^{t_l} v_w(x) h_l(t-x) dx \quad (1.82)$$

$$= \frac{KQW\tau_c}{2Ce_n}[(e^{\frac{t-t_m}{\tau_c}} - e^{-\frac{t-t_m+2t_l}{\tau_c}})\theta(t_m - t)\theta(t - t_m + t_l)$$
$$+(e^{-\frac{t-t_m}{\tau_c}} - e^{\frac{t-t_m-2t_l}{\tau_c}})\theta(t - t_m)\theta(t_m - t_l - t)] \quad (1.83)$$

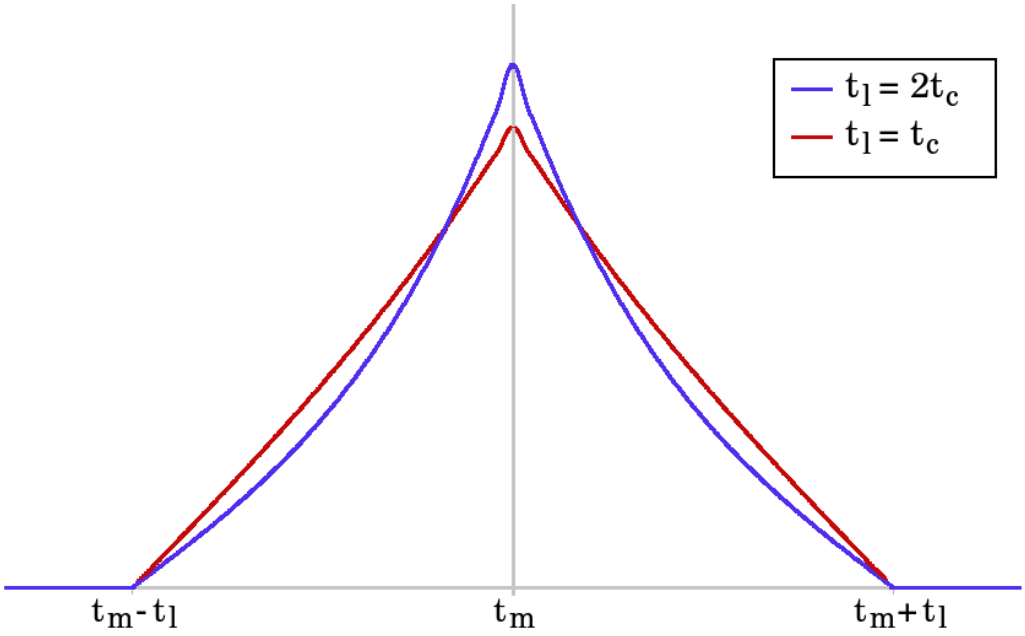


Figure 1.13: Output of the sub-optimum filter with finite duration t_l

The SNR of the sub-optimum filter can be calculated as:

$$\mathrm{SNR} = \frac{v_{\text{sub-opt,E}}(t_m)}{\sqrt{W^2 \int_{-\infty}^{\infty} h_l(t)^2 dt}} \tag{1.84}$$

$$= \mathrm{SNR}_{\text{opt}} \sqrt{1 - e^{-\frac{2t_l}{\tau_c}}} \tag{1.85}$$

Depending on the event rate, the value of t_l can be tuned in order to reduce the probability of pile-up to the desired value. If t_l and τ_c are of the same order of magnitude, the SNR does not worsen significantly with respect to the ideal case. For example, if the limit time t_l is equal to time constant τ_c, the SNR is worsened only by 7% with respect to $\mathrm{SNR}_{\text{opt}}$, while for $t_l = 2\tau_c$ the SNR is only 1% less than in the optimal case.

1.3 Optimum filtering for timing

The optimum timing for a signal Qs(t) in presence of noise is obtained with the filter that minimizes the jitter σ_t [19] [20]. From the definition of jitter (see equation 1.8), it is the same as searching the filter z(t) that maximizes the Slope-to-Noise-Ratio (SLNR) at the instant t_m of the measurement. The problem is similar to the one treated in the previous section, with the difference that the signal now is $Q\frac{ds(t)}{dt}$. Thus the conclusions are the same with the difference that the filter optimized for timing requires a further derivation with respect to the energy optimum shaper:

$$\mathrm{SLNR}^2_{\text{max}} = Q^2 \int_{-\infty}^{\infty} \frac{\frac{ds(t)}{dt}^2}{\sigma_n^2} dt \tag{1.86}$$

$$= Q^2 \int_{-\infty}^{\infty} \frac{|j\omega S(\omega)|^2}{N(\omega)} df \tag{1.87}$$

As in the previous case the $SLNR_{max}$ is independent from the filter.

In case of white noise, the result becomes:

$$SLNR^2_{max} = \frac{Q^2}{W^2}\int_{-\infty}^{\infty}|j\omega S(\omega)|^2 df \quad (1.88)$$

$$= \frac{Q^2}{W^2}\int_{-\infty}^{\infty}\frac{ds(t)}{dt}^2 dt \quad (1.89)$$

$$z(t) = K\frac{ds(t_m - t)}{dt} \quad (1.90)$$

$$= \frac{dh(t)}{dt} \quad (1.91)$$

For radiation detectors the whitening filter is used and its output is given by equation 1.66. Assuming the same conditions examined in the case of optimum filtering for energy measurement, the optimum filter for timing is obtained deriving equation 1.67:

$$z(t) = K[\frac{e^{\frac{t-t_m}{\tau_c}}}{\tau_c}\theta(t_m - t) - e^{\frac{t-t_m}{\tau_c}}\delta(t - t_m)] \quad (1.92)$$

Thus the optimum timing filter output is given by the convolution of equations 1.66 with 1.92:

$$v_{opt,t}(t) = v_W(t) * z(t) \quad (1.93)$$

$$= \frac{KQW}{2Ce_n}[e^{\frac{t}{\tau_c}}\theta(t_m - t) - e^{-\frac{t}{\tau_c}}\theta(t - t_m)] \quad (1.94)$$

The result is the derivative of the indefinite cusp shown in Fig. 1.14.

The SLNR at the output of the optimum filter is given by:

$$SLNR = \frac{Q^2}{W^2}\int_{-\infty}^{\infty}|j\omega S(j\omega)|^2 df \quad (1.95)$$

$$= \frac{Q^2}{2\pi W^2\tau_c}\int_{-\infty}^{\infty}|\frac{j\omega\tau_c}{1 + j\omega\tau_c}|^2 d(\omega\tau_c) \quad (1.96)$$

$$= \frac{Q^2}{2\pi W^2\tau_c}\int_{-\infty}^{\infty}\frac{\omega^2\tau_c^2}{1 + \omega^2\tau_c^2}d(\omega\tau_c) \quad (1.97)$$

$$= \frac{Q^2}{2\pi W^2\tau_c}(\omega\tau_c - \arctan\omega\tau_c)|_{-\infty}^{\infty} \quad (1.98)$$

$$= \infty \quad (1.99)$$

Equation 1.98 shows that, in case of optimum filtering, the timing is perfect.

Similarly to the optimum energy shaper, the optimum filter for timing is not feasible since it requires an infinite time for the measurement and is affected by the pile-up problem. The requirement of a finite time for the measurement and of a finite event rate leads to sub-optimum solutions. The results are analogous to the ones obtained in the previous section.

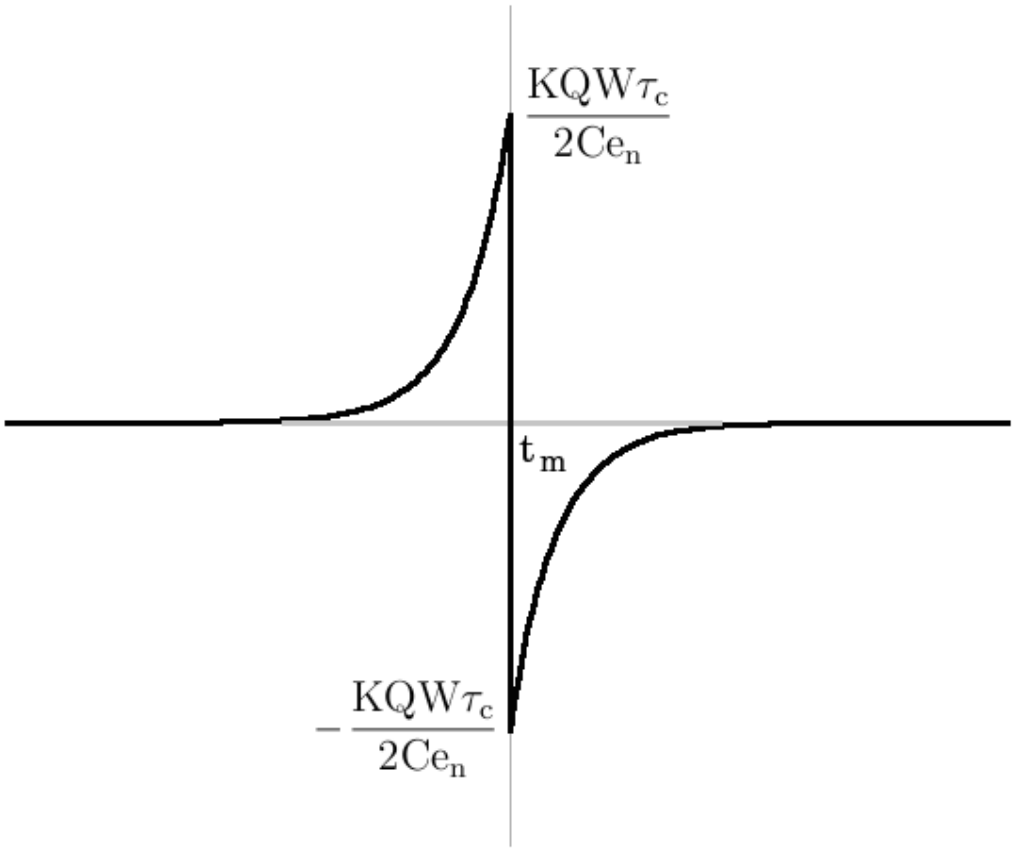


Figure 1.14: Output of the full chain composed by amplifier, whitening filter and shaper for optimum timing

1.4 Accurate timing with semiconductor detectors

In this section the basic items which determine the accuracy in measurements with semiconductor detector are discussed [21] [22]. Fig. 1.15 illustrates the essential parts of any signal processing system for semiconductor detector signals. The event

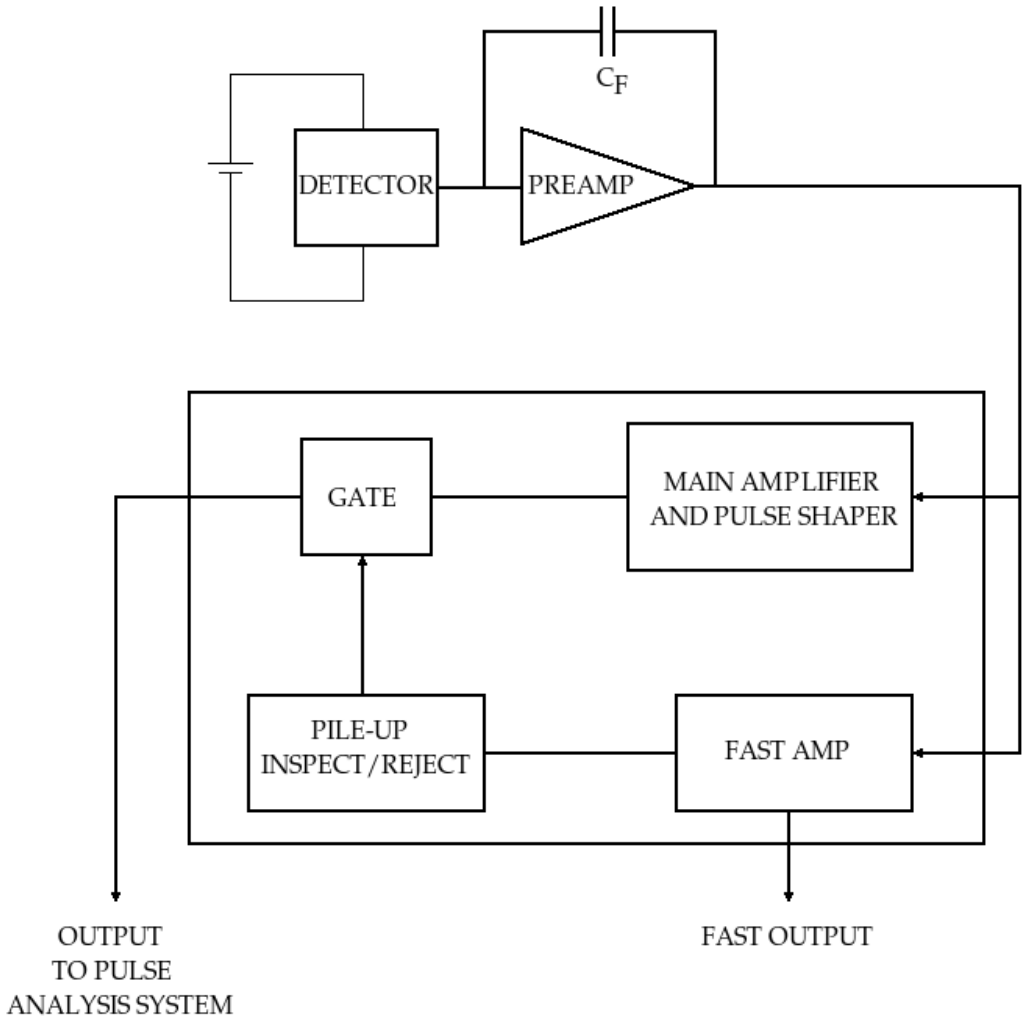


Figure 1.15: Basic block diagram of a spectroscopy system

is detected by a reversed bias sensor which produces current pulses at the input of a Charge Sensitive Amplifier (CSA). The charge induces a step waveform at the output of the preamplifier. In some cases a resistor is used in parallel to the feedback capacitor to restore the baseline at the output of the stage. In other cases the charge on the feedback capacitor is cancelled with a pulse reset method. The following stage is the main amplifier which performs the signal shaping. Many factors may influence the design of the shaper [23].

The rejection of signal pile-up is performed with a parallel fast amplifier where signals are differentiated to produce very short pulses. When pairs of pulses are too

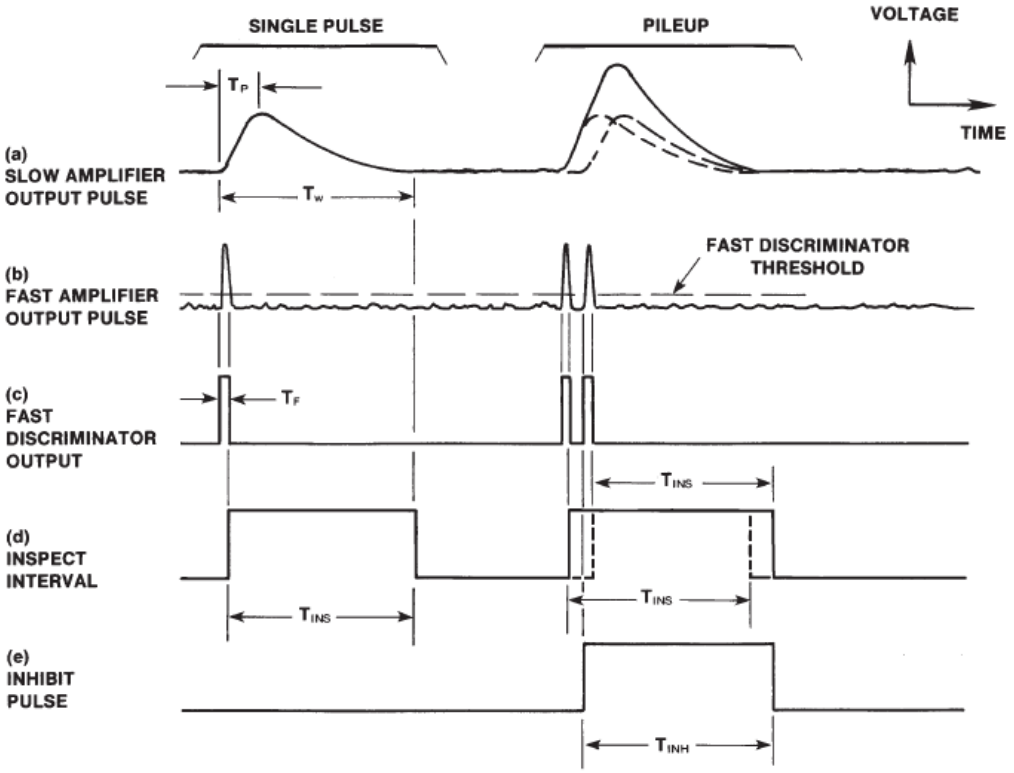


Figure 1.16: Basic waveform in the pile-up rejector

close together, signals from the slow amplifier are rejected (see Fig. 1.16).

1.4.1 Signal characteristics in semiconductor detectors

The charge produced by the radiation in the detector is proportional to the absorbed energy:

$$Q = \frac{Eq}{\epsilon} \tag{1.100}$$

where Q is the charge produced, E is the absorbed energy, q is the charge of the electron and ϵ is the average energy required to produce an electron-hole pair. The coefficient ϵ represents the conversion efficiency of the detector and depends on the material and, to a minor degree, on the temperature (see Table 1.1 from [22]).

Material		ϵ
Si	@25° C	3.61 eV
	@77 K	3.81 eV
Ge	@77 K	2.96 eV
Compounds (e.g. Hg_2I, CdTe)		> 4 eV

Table 1.1: Values of ϵ for different materials and at different temperatures

The fact that the energy released in the sensor produces both ionization and vibrations in the crystal lattice in random way means that the signal output charge, which is due only to the ionization, is intrinsically subject to random fluctuations. If the ionizing collisions were very rare with respect to the phonon ones, the variation in the number N of electron-hole pairs would obey to the Poisson statistics, leading to:

$$\sigma_{\mathrm{E}} = \epsilon\sqrt{\mathrm{N}} = \sqrt{\mathrm{E}\epsilon} \tag{1.101}$$

where it has been used the relation $\mathrm{N} = \frac{Q}{q}$. In practice the assumption about the rarity of ionizing collision is not valid. This produces a reduction in the energy fluctuation of a factor $\sqrt{\mathrm{F}}$:

$$\sigma_{\mathrm{E}} = \sqrt{\mathrm{FE}\epsilon} \tag{1.102}$$

where F is the Fano factor. F is always lower than the unity and approximates 0.12 for silicon and germanium. The intrinsic resolution as a function of energy in percentage is summarized in Table 1.2 for Si and Ge detectors.

E (eV)	$\frac{\sigma_{\mathrm{E}}}{\mathrm{E}}$ for Si (%)	$\frac{\sigma_{\mathrm{E}}}{\mathrm{E}}$ for Ge (%)
10^3	2.138	1.885
$2 \cdot 10^3$	1.512	1.333
$5 \cdot 10^3$	0.956	0.843
$10 \cdot 10^3$	0.676	0.596
$20 \cdot 10^3$	0.478	0.421
$50 \cdot 10^3$	0.302	0.267
$100 \cdot 10^3$	0.214	0.188
$200 \cdot 10^3$	0.151	0.133
$500 \cdot 10^3$	0.096	0.084
10^6	0.068	0.060
$2 \cdot 10^6$	0.048	0.042
$5 \cdot 10^6$	0.030	0.027
$10 \cdot 10^6$	0.021	0.019
$20 \cdot 10^6$	0.015	0.013
$50 \cdot 10^6$	0.010	0.008
$100 \cdot 10^6$	0.007	0.006
$200 \cdot 10^6$	0.005	0.004
$500 \cdot 10^6$	0.003	0.003

Table 1.2: Intrinsic detector resolution for Si and Ge detectors at 77 K for different energies

The time taken to collect the electrons and holes at the electrodes of the detector may influence the choice of signal shaping method. To simplify the discussion, the sensor crystal is assumed to be extremely pure, with no acceptors or donors. Thus the bias applied throughout the material would produce a constant electric field. Moreover, the electric field is assumed uniform along all the detector. In Fig. 1.17 it is shown a planar geometry detector where a single electron-hole pair is produced at a distance x from the p^+ contact. Due to the electric field, the electron drifts

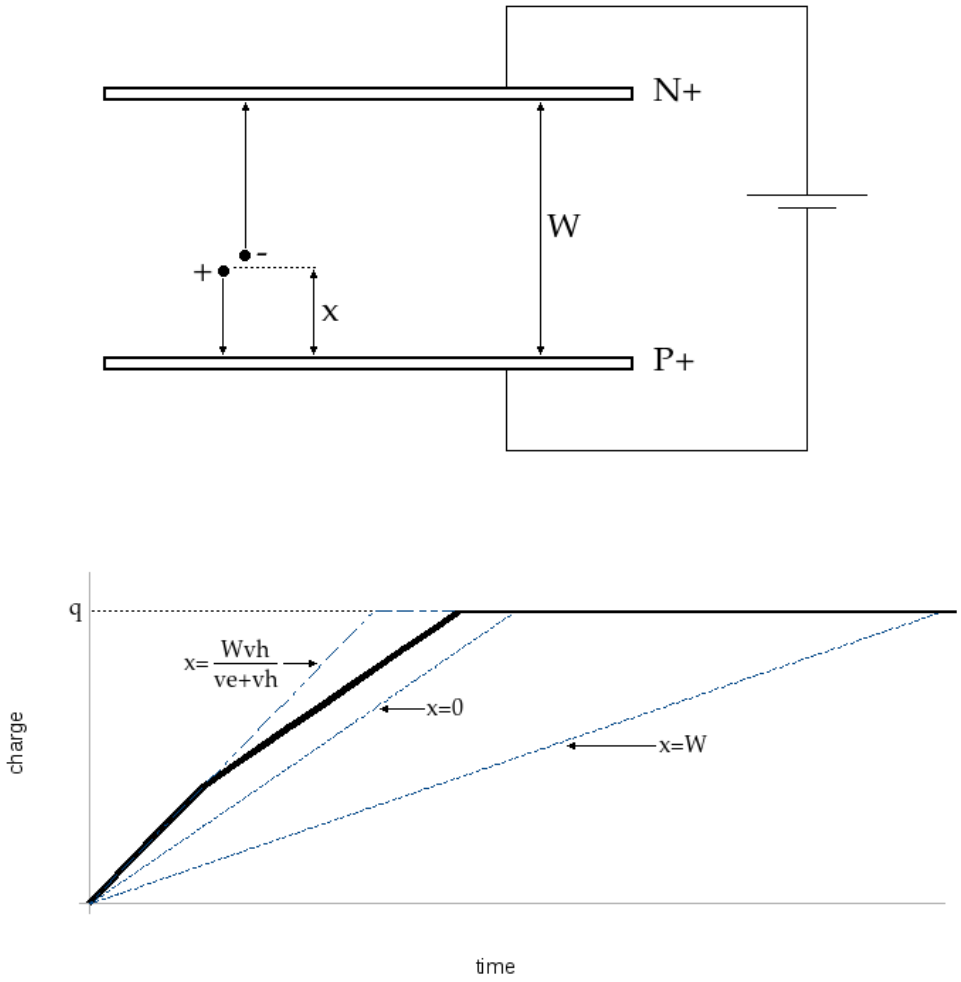


Figure 1.17: Pulse shape generation in a planar detector

toward the positively biased n^+ contact, while the hole drifts to the opposite one. The output current signal persists until the carriers are moving. The charge collected as a function of time is given by the solid line in Fig. 1.17, where v_e and v_h are respectively the drift velocities of electrons and holes. The dotted lines show the signal a x = 0, due exclusively to the electrons and at x = W, induced by holes only. The fastest signal is obtained when the collection times of electron and holes are equals (dashed line).

The signal observed for a radiation event is given by the integral of the signals

from the single electron-hole pairs produced. The statistical distribution of the depths of pair production causes the signal shape to change from one event to the other. This effect is known as charge straggling [24] [25]. Moreover, if the assumption of a uniform electric field is released, the radiation interacting on the border of the detector will be subject to a non-uniform electric field, leading to the dependence of signal shape on the position inside the detector (border effect). Furthermore, a reverse biased semiconductor exhibits a leakage current whose fluctuations produce noise [26]. A basic source of the leakage are the electron-holes pairs generated by termally induced lattice vibrations in presence of trapping levels. Particularly those levels in the middle of the band gap favor the transition of electrons from the valence to the conduction band. Thus the leakage current I_L of semiconductors often obey to the relationship:

$$I_L \propto e^{-\frac{E_g}{2kT}} \tag{1.103}$$

where E_g is the band gap of the material, k is the Boltzmann constant and T is temperature. For many high resolution applications, cooling could be required. Moreover, hard radiation exposition increases the number of traps in the crystal leading to higher leakage.

1.4.2 The preamplifier

Fig. 1.18 shows the two methods commonly used to couple detectors to the preamplifier input. The DC coupling is used for high resolution applications primarily because it minimizes the stray capacitance at the input of the amplifier improving the SNR. Moreover the output of the preamplifier can be monitored to measure the leakage current. In reset systems the reset rate combined with the value of C_F provides an absolute measurement of the leakage current. In R_FC_F feedback systems the change in the DC level at the output of the preamplifier with respect to the detector bias gives the information about the leakage current.

In the AC connection one side of the detector is conveniently grounded. However the detector load constitutes a source of noise and the stray capacitor worsen the SNR. Furthermore the differentiator formed by the coupling capacitor, by the detector load and by the preamplifier input may cause the degradation of the resolution at high counting rates. The AC connection is commonly employed with room temperature detectors used in charge particle spectroscopy, where these factors may contribute less to resolution than various detector and beam resolution factors.

The equivalent input circuit of a detector preamplifier system with an input capacitance C and a shunt resistance R is shown in Fig. 1.19. The noise generated by R is represented as a voltage generator $v^2 = 4kTR\Delta f$, leading to :

$$V_{out}^2 = 4kTR\Delta f \frac{R}{1 + 4\pi^2 f^2 C^2 R^2} \tag{1.104}$$

where Δf is the small frequency interval centered on f. The total noise at the system output is given by the integral of the previous equation over the bandwidth of the shaper amplifier. The maximum noise is reached for $R = \frac{1}{2\pi fC}$. The noise tends to zero for very small and very large values of R. In the first case the signal at the

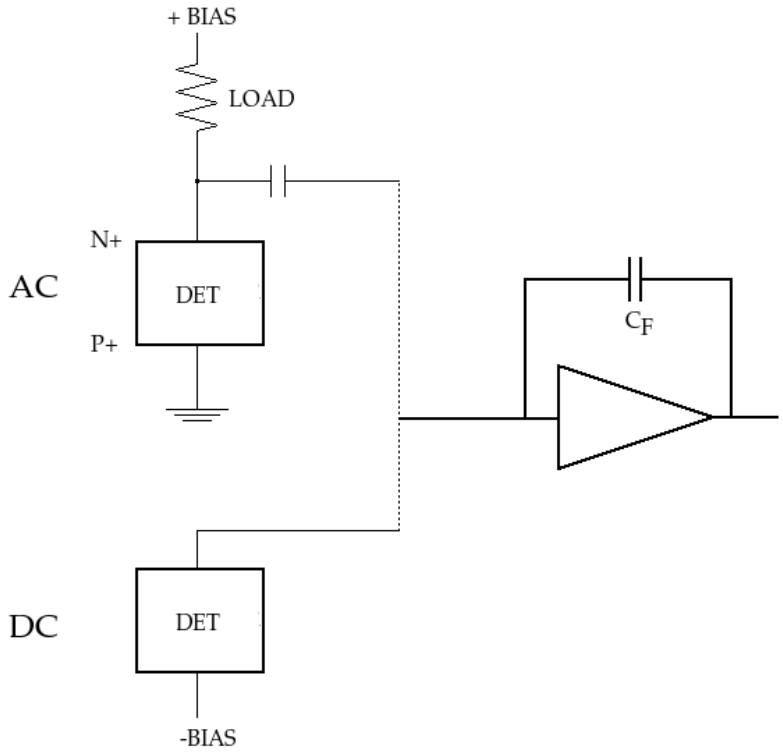


Figure 1.18: Coupling of the detector with the preamplifier

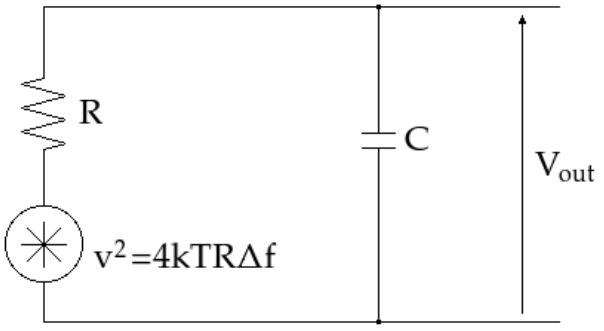


Figure 1.19: Equivalent input circuit of a detector preamplifier circuit

input is virtually shorted out, thus it is clear that highest possible values of shunt impedance are essential in high resolution systems.

As already discussed, many systems use a high value resistor in parallel to C_F in order to discharge it and to restore the preamplifier baseline. The result is an exponential decay of the signals at the output of the preamplifier with a quite long decay constant $R_F C_F$. The further differentiation required in the shaping amplifier results in a long term undershoot with consequent degradation effects at high counting rates, as shown in Fig. 1.20. For this reason usually a pole-zero cancellation

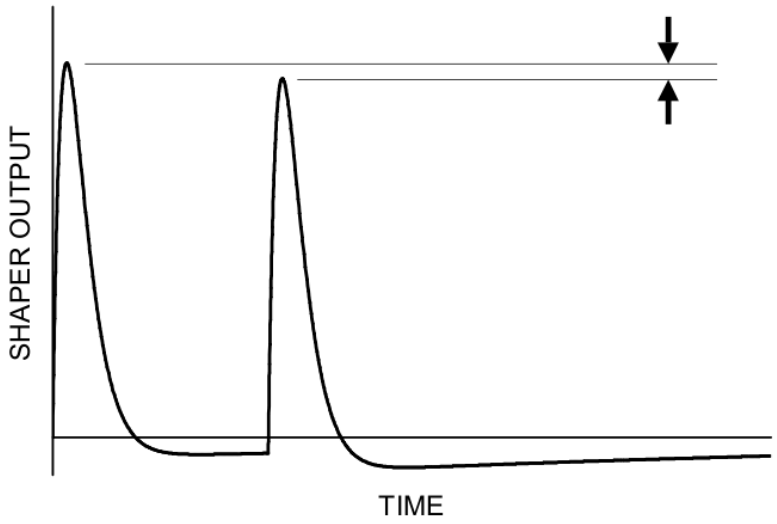


Figure 1.20: Loss of resolution at high counting rates due to baseline variations

circuit is included in most amplifiers. The compensation, illustrated in Fig. 1.21, is achieved by shunting the main differentiator capacitor in the shaping amplifier by a resistor R_Z [27] [28]. The circuit transfer function is given by:

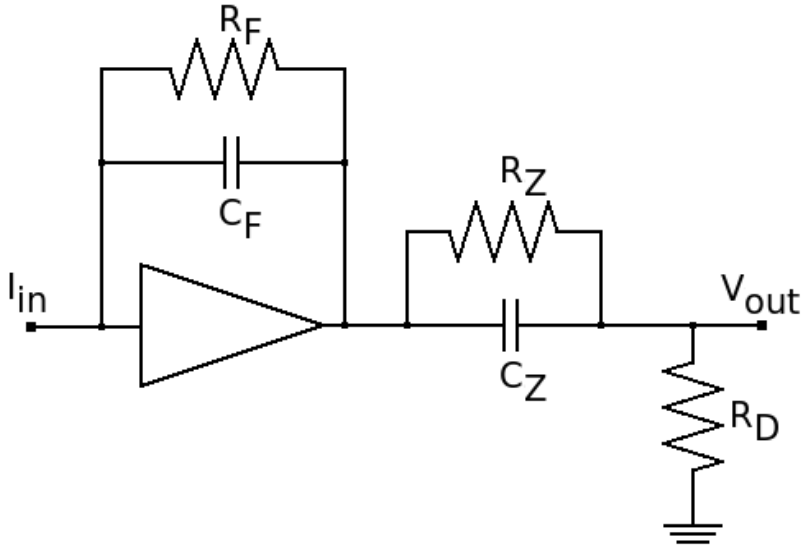


Figure 1.21: Pole-zero cancellation circuit

$$V_{out} = I_{in} \frac{R_D R_F}{R_D + R_Z} \frac{1 + s\tau_Z}{(1 + s\tau_F)(1 + sk\tau_Z)} \tag{1.105}$$

where $\tau_Z = R_Z C_Z$, $\tau_F = R_F C_F$ and $k = \frac{R_D}{R_F + R_D}$. The pole-zero cancellation is obtained when $R_Z = \frac{R_F C_F}{C_Z}$.

There are other disadvantages related to the use of the shunt resistor R_F. First of all it acts as a noise source. As already discussed the noise is reduced by using high value resistors, which, on the other hand, do not behave as pure resistors at high frequencies. Therefore the pole-zero compensation is never perfect and the resolution can be seriously degraded at high counting rates. Moreover the stray capacitance associated with R_F degrades the SNR. For these reasons the pulse reset method is commonly used in high resolution, high rate systems.

1.4.3 The pulse shaper

The choice of the shaping filter for different applications is dictated by the noise performance of the filter itself [29]. A shaper with a fast peaking time minimizes the parallel noise, while a slow shaper is affected by lower series noise [30].

For energy measurements the optimum peaking time is the one that minimizes the total noise (the shaping time at which the series and the parallel noise are equal, see Fig. 1.11). The choice depends on the event rate. If the maximum acceptable dead time is lower than the optimal peaking time, there is a trade-off between noise performance and efficiency. In this case the maximum peaking time which can be afforded depending on the event rate should be chosen.

For time measurements fast systems are preferred. This is due in principle to the fact that the reduction of the bandwith (BW) of the amplifier leads to a reduction of a factor $\sqrt{BW}$ of the noise, but also the slope decreases of a factor BW. Thus, referring to equation 1.10, the jitter is increased of a factor $\sqrt{BW}$. On the other hand, using a shaping filter with a peaking time higher than the collection time introduces more noise without improving the slope of the signal. The shaper velocity is limited by the sensor collection time. Thus the optimal peaking time for timing is given by the charge collection time in the sensor [31]. This difference in optimization is at the base of the architecture choice. In systems which perform both time and energy measurements, two shaper are used in parallel at the output of the preamplifier, a faster one for timing and a slower filter for the energy measurement.

Typically, in shaping filters, a differentiation network followed by at least one integration network limits the amplifier bandwidth. Fig. 1.22 illustrates the block diagram of a basic CR-RC shaper, where the gain stage A allows to set the overall gain of the chain and to insulate the differentiator and the integrator time constants, and the buffer B drives the following stages with the appropriate impedance. The detector is represented as a current source with a capacitor C_D in parallel. Increasing the number of integrators leads to generic transfer function for a CR-RC^n shaping filter:

$$\frac{V_o(s)}{I_{in}(s)} = \frac{1}{C_F} \frac{\tau_P}{(1 + s\tau_P)^{1+n}} \tag{1.106}$$

where it is assumed A = 1. Higher order filters have more symmetrical shaped pulses with a faster return to baseline (see Fig. 1.23) [32]. Fig. 1.24 includes the

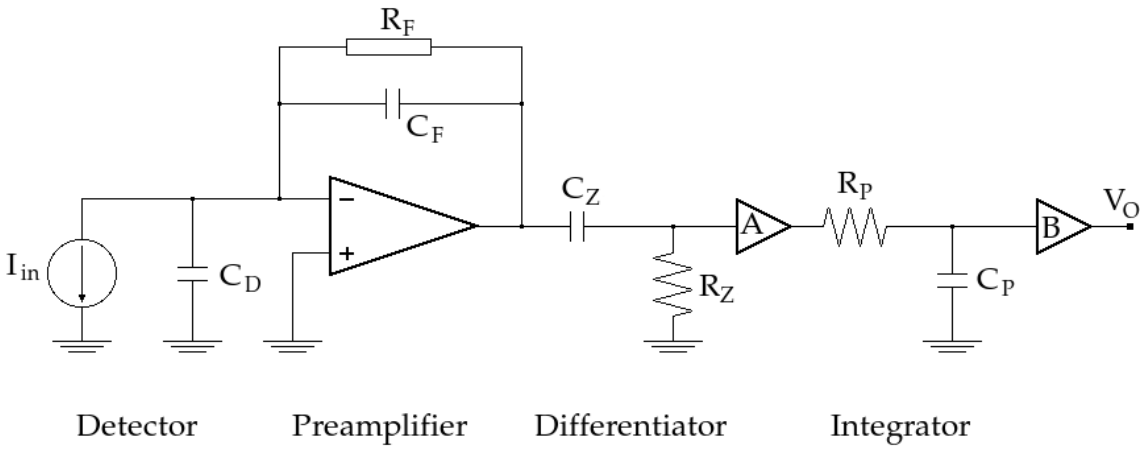


Figure 1.22: Basic CR-RC shaper

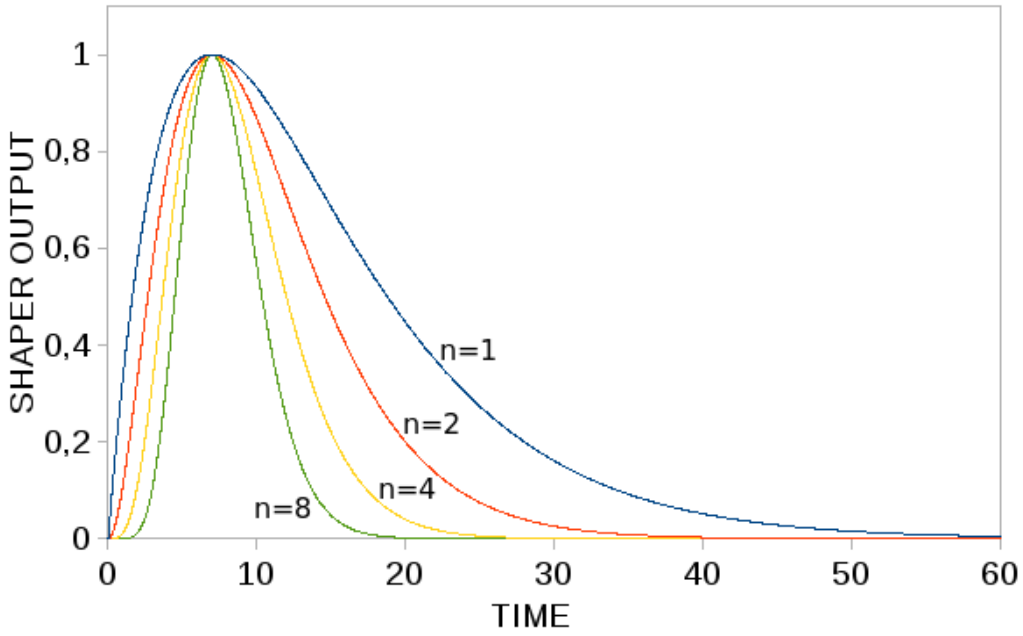


Figure 1.23: Output of CR-RC^n filters with the time constants adjusted to preserve the peaking time

series and parallel noise sources which represent the noise of the detector and of the preamplifier. The equivalent noise current at the input of the preamplifier is:

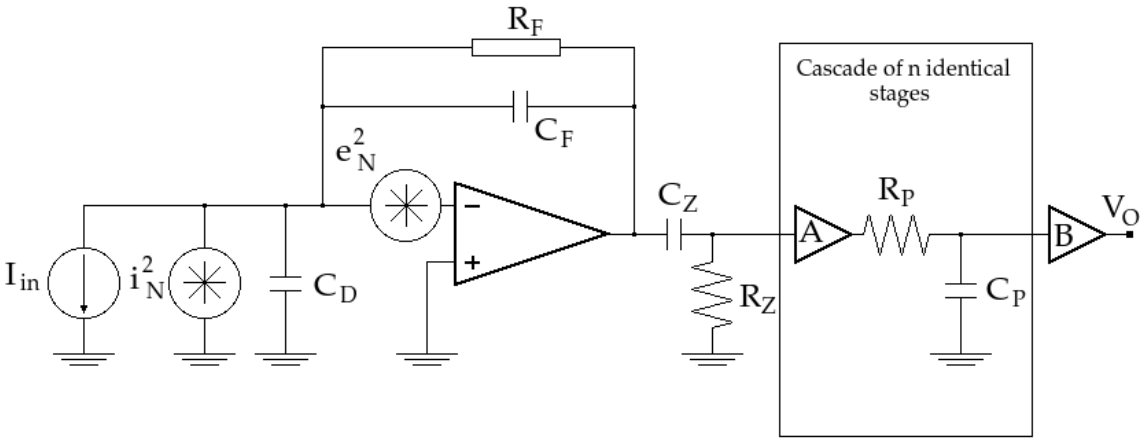


Figure 1.24: Block diagram of a CR-RC^n shaper with noise sources

$$i^2_{neq} = e^2_n \omega^2 C^2_{IN} + i^2_n \tag{1.107}$$

where C_{IN} is the total capacitance at the preamplifier input, including also C^2_D, and the voltage noise is due to the white noise and to the 1/f contribution:

$$e^2_n = e^2_{nw} + \frac{2\pi A_f}{\omega} \tag{1.108}$$

Assuming an infinite R_F, the transfer function of the CR-RC^n and the total transfer function are respectively given by:

$$H(s) = \frac{s\tau}{1+s\tau}\frac{A^n}{(1+s\tau)^n} \tag{1.109}$$

$$T(s) = \frac{1}{sC_F}H(s) \tag{1.110}$$

Finally, the output voltage equivalent noise can be calculated as:

$$v_{no} = \frac{1}{2\pi}\int_0^\infty i^2_{neq}|T(j\omega)|^2 d\omega \tag{1.111}$$

Combining equations 1.107 and 1.111, the equivalent output noise can be written as follows:

$$v_{no} = e^2_{nw} C^2_{IN} A_1^{'} + 2\pi A_f C^2_{IN} A_2^{'} + i^2_n A_3^{'} \tag{1.112}$$

where the three contributors are respectively the white series noise, the 1/f series noise and the white parallel noise. $A_1^{'}$, $A_2^{'}$ and $A_3^{'}$ are given by:

$$A_1^{'} = \frac{1}{2\pi}\int_0^\infty \omega^2 |T(j\omega)|^2 d\omega \tag{1.113}$$

$$A_2^{'} = \frac{1}{2\pi}\int_0^\infty \omega |T(j\omega)|^2 d\omega \tag{1.114}$$

$$A_3^{'} = \frac{1}{2\pi}\int_0^\infty |T(j\omega)|^2 d\omega \tag{1.115}$$

Introducing the characteristic shaping time τ_s, which can be arbitrarily set equal to the peaking time for unipolar pulses or to the zero crossing time for bipolar signals, and the adimensional variable $x = \omega\tau_s$, the equivalent output noise becomes:

$$v_{no} = \frac{e_{nw}^2 C_{IN}^2}{\tau_s} A_1 + 2\pi A_f C_{IN}^2 A_2 + i_n^2 \tau_s A_3 \quad (1.116)$$

$$A_1 = \frac{1}{2\pi} \int_0^\infty x^2 \frac{|T(x)|^2}{\tau_s} dx \quad (1.117)$$

$$A_2 = \frac{1}{2\pi} \int_0^\infty x \frac{|T(x)|^2}{\tau_s} dx \quad (1.118)$$

$$A_3 = \frac{1}{2\pi} \int_0^\infty \frac{|T(x)|^2}{\tau_s} dx \quad (1.119)$$

This parameterization allows to characterize the shaper in terms of adimensional noise coefficients, called form factors, whose effect is scalable by the characteristic shaping time. Equation 1.117 to 1.119 apply to any shaper. In Table 1.3 the form factors for a set of filters have been calculated [33].

Filter	A_1	A_2	A_3
CR-RC	0.92	0.59	0.92
CR-RC^2	0.82	0.54	0.66
CR-RC^7	0.94	0.51	0.46
CC-2	0.93	0.59	0.88
CC-3	0.85	0.54	0.61
CC-7	1.04	0.51	0.40
CR^2-RC	1.03	0.75	1.01

Table 1.3: Form factors for different filter shaper

1.4.4 Monolithic CFD implementation

As the number of identical readout channels is continuously increasing, the requirements of low power consumption, low noise and small size of readout electronics become more severe. To readout such a large number of channels, the printed circuits and hybrid electronics are clearly inadequate and monolithic integration is the only possible approach to the design of a readout system. CMOS technologies have been chosen for integration due to the high integration density, to the low power consumption feature and to their capability of combining both digital and analog circuits on the same chip. While other timing techniques described in this chapter are easily feasible in integrated circuits, the main problem for monolithic CFDs is the implementation of a delay line as ideal as possible. Furthermore the practical implementation of CFDs suitable for multichannel ICs entails several issues. The

area of the circuit and the power consumption have to be minimized and the impact of process spreads must be taken into account. Furthermore the arming circuitry must be designed to prevent the generation of full swing logic levels at the outputs of the zero crossing detector. Moreover detector signals are subject to statistical fluctuations that affect not only the amplitude but also the signal shape.

Constant fraction shaping methods in integrated circuits, like simple RC low pass filter, distributed RC delay line [34] [35] or lumped element technique [36], have been investigated in [37]. Neither of these methods can match the ideal delay line implementation. The one that comes closest to it is the distributed RC delay line. Fig. 1.25 shown three CFD schemes implementing a distributed RC delay line in all of them. The fraction is generated with a voltage divider. The output of the three configurations are compared in Fig. 1.26. The solution A implies a large area occupation and power consumption due to the presence of fast buffers and introduces the issue of offset compensation to maintain the DC voltages along the filter. The same circuit implemented without buffers, as shown in solution B, simplifies all problems linked to area, power consumption and offset compensation and its output does not differ significantly from the first case (see Fig. 1.26). The cross coupling configuration of Fig. 1.25 C shows a more compact solution [66]. The coupling between the delay and the fraction results in a two-time lower signal, which should be amplified again, and in a slower slope and thus in a higher jitter (see Table 1.4). Nevertheless between all investigated solutions the cross coupling is the more

	Slope (mV/ns)
Scheme A	64.4
Scheme B	47
Scheme C	18.4

Table 1.4: Jitter of the three configurations

effective for those application where it is important to have fully differential signals as early as possible and where the size and the power consumption are the primary constraints.

The solution C has been studied in detail [38]. In this configuration, the current flowing in the output resistor is equal to the current in the feedback one, leading to:

$$\frac{V_{out}(s) - V_{d,n}(s)}{R} = -\frac{V_{in}(s) - V_{d,n}(s)}{FR} \tag{1.120}$$

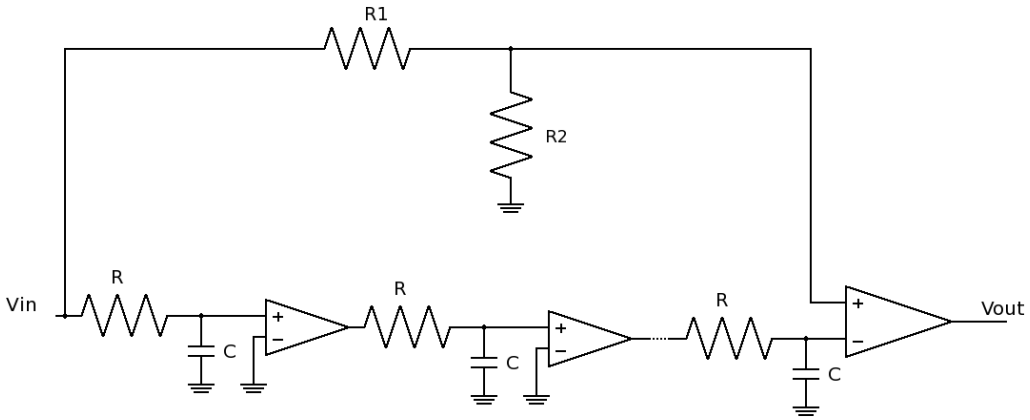
$$V_{out}(s) = V_{d,n}(s)\frac{F}{1+F} - V_{in}(s)\frac{1}{1+F} \tag{1.121}$$

The voltage V_d for a first order filter is given by:

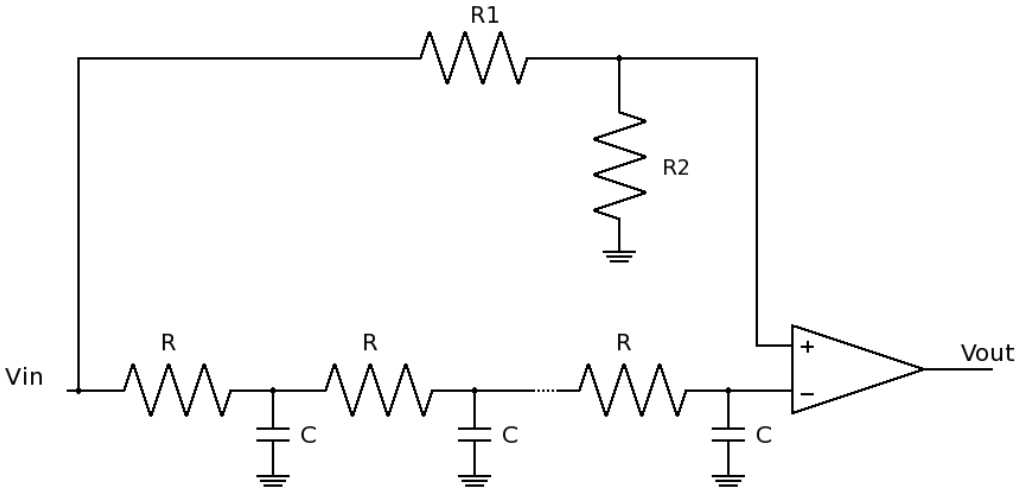
$$V_{d,1}(s) = V_{in}(s)\frac{F}{sRC + 2 + F(sRC+1)} \tag{1.122}$$

For a higher order filter V_d can be calculated using the recursive equation:

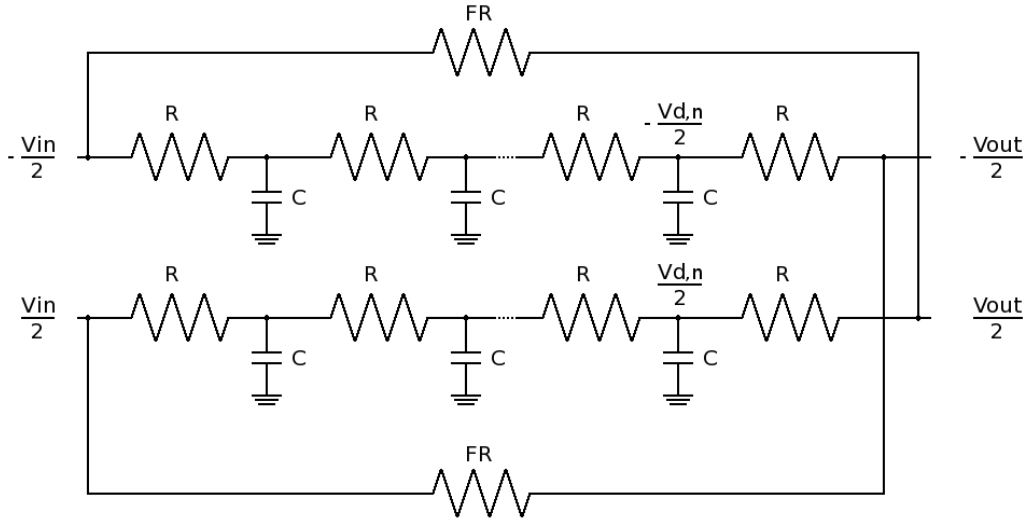
$$V_{d,n}(s) = V_{in}(s)\frac{A_n(s)}{B_n(s) + FC_n(s)} \tag{1.123}$$



(A)



(B)



(C)

Figure 1.25: (A) Implementation of the CFD using a distributed RC delay line with (B) and without fast buffers. (C) Cross coupling CFD topology

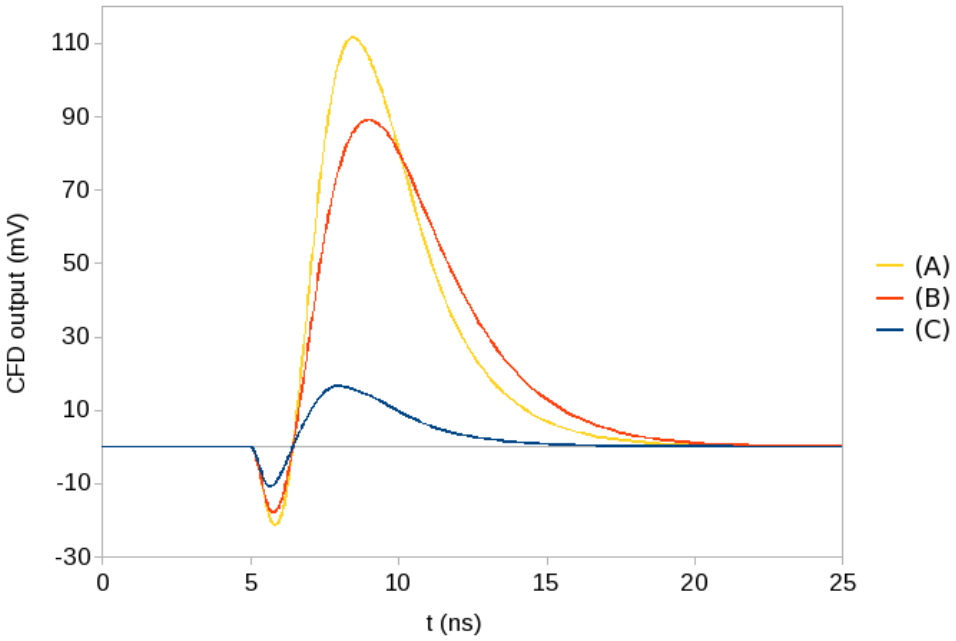


Figure 1.26: Output of the three considered CFD architectures shown in Fig. 1.25

where the coefficients A_n, B_n and C_n are calculated as follows:

$$A_n(s) = (F+1) - B_{n-1}(s) \quad (1.124)$$

$$B_n(s) = B_{n-1}(s)(sRC+1) + C_{n-1}(s) \quad (1.125)$$

$$C_n(s) = sRCB_{n-1}(s) + C_{n-1}(s) \quad (1.126)$$

Equations 1.121 to 1.126 represent the transfer function of a cross coupling CFD filter of arbitrary order.

An interesting item is the filter order choice. The same delay can be implemented using more RC filters with lower time constants in cascade. A simulation of the described CFD topology (Fig. 1.25 C) with different RC filter orders is plotted in Fig. 1.27 and shows that, once the fraction is fixed, a higher order filter has a higher slope [40]. The value of the RC time constant for different filter orders has been calculated in such a way that the zero crossing occurs always at the same time. In order to fix the fraction at 25% in the different cases it is necessary to change the value of the feedback resistor, since the fraction and the delay are coupled in this topology. The values used in simulations are listed in Table 1.5, where F is the ratio between the feedback and the output resistors shown in Fig. 1.25. Thus it is suitable to use higher order RC lines to reduce the jitter and consequently to improve the timing precision. The same conclusion can be achieved considering that ideally, the higher is the order of the filter, the more its behavior tends to the ideal delay line. Moreover lower order filters, which are implemented with higher time constants, slow down the input signal more with respect to the ideal case. However, the choice of the filter order will depend mainly on the available area.

Furthermore, since the CFD is composed by resistors and capacitors, the variations of the filter time constant with the process is a significant source of error

Filter order	RC time constant (ps)	feedback F
3^{rd}	75.9	4.45
4^{th}	66.8	6
5^{th}	60.2	7.93
6^{th}	50.8	9.92

Table 1.5: Value of the RC time constants used in simulation for different filter orders. The values have been calculated in order to have the same delay in all situations

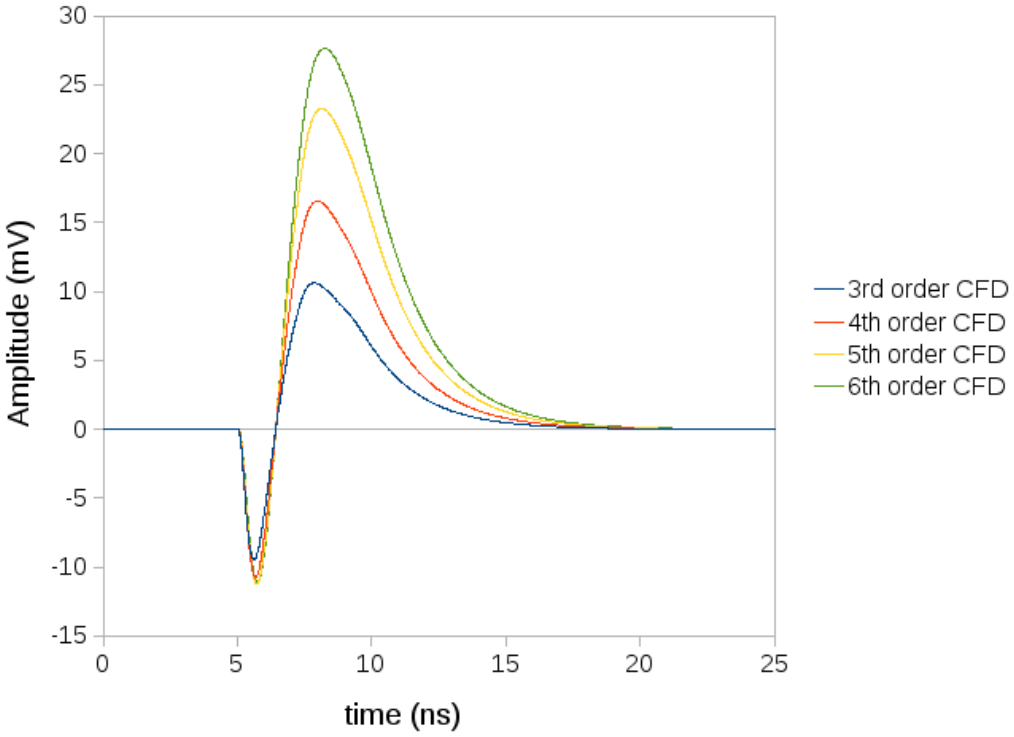
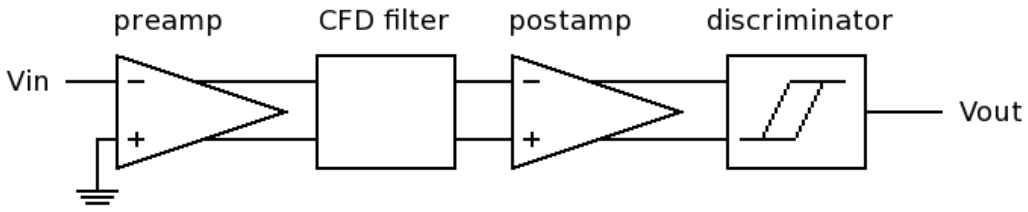


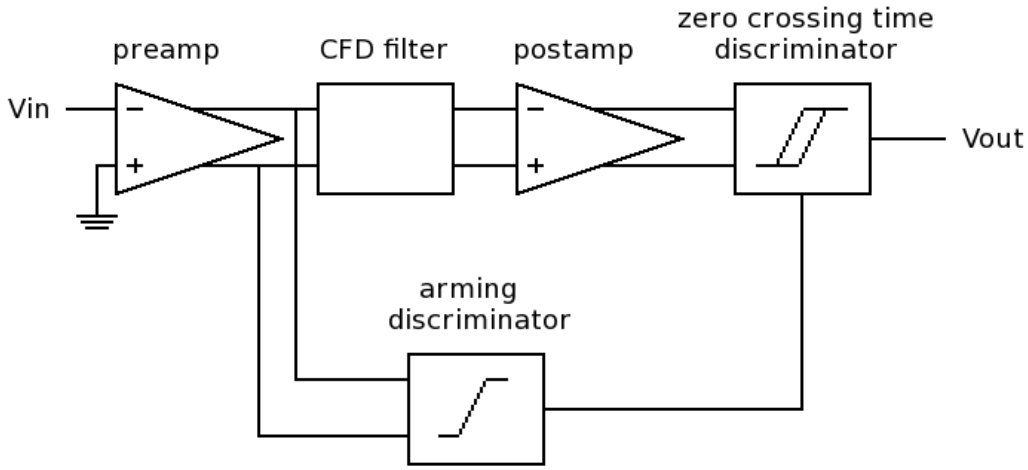
Figure 1.27: Simulation result of the cross coupling CFD with different filter orders and a fixed fraction of the 25%

that must be taken properly into account. In semiconductor manufacturing, the process spread refers to the variation of fabrication parameters obtained in applying an integrated circuit design to a semiconductor wafer. Due to parameters variations, a circuit etched on semiconductor devices may run slower or faster than specified. Process corners represent the extremes of these parameter variations. If the circuit works correctly in any of these process corners, the design has an adequate margin [39]. To ensure that the zero crossing time remains always in the optimized region, the delay and the fraction should be made programmable. The value of the programmable capacitors can be calculated, for example, in order to have the same RC time constant in all the corners of the process. The calculation becomes more complicated because of parasitic (see Appendix B). It should be noted that due to the presence of parasitic in resistors and capacitors and in the swithces used to program the filter, the behavior of high order filters deviates from the ideal delay line. Moreover lower order filters are more easily programmable.

For what concerns the zero crossing detection, in the standard topology the output of a leading edge discriminator is put in AND with the output of the zero crossing detector to avoid the propagation of spurious signals to the following logic. For integrated CFDs, the arming circuitry must be designed to prevent the generation of full swing logic levels in any point of the chain. In fact, even if the gating with the leading edge prevents these pulses from reaching the rest of the logic, the noise injected on chip by thousand of discriminators switching on noise might not be tolerable. When time walk minimization is the primary concern a delay of the order of the peaking time can be used. The higher is the delay, the bigger is the underdrive of the bipolar signal which can be used to trigger. The trigger disables the threshold of the discriminator itself allowing the zero crossing detection (Fig. 1.28 A). With this technique, the threshold is disabled only in presence of the signal, preventing the discriminator from firing on noise. However, as it has been described in the previous section, detector signals are subject to statistical fluctuations that affect not only the amplitude, but also the signal shape. To minimize the sensitivity of the CFD to the shape variations of the input signal a delay shorter than the peaking time must be used [40]. This implies the reduction of the amplitude of the underdrive. In this case an independent arming discriminator is necessary to gate the zero crossing one (Fig. 1.28 B).



(A)



(B)

Figure 1.28: (A) For CFDs with a delay of the order of the signal peaking time a discriminator with hysteresis can be used. (B) To minimize the effects of signal shape variantions a shorter delay must be used leading to the necessity of having an independent arming discriminator

Chapter 2

The NA62 experiment

The aim of the NA62 experiment is to collect about 80 events of the rare decay $K^+ \to \pi^+\nu\overline{\nu}$ with a signal to background ratio (S/B) of 1:10 in two years of data taking [41].

Thanks to its very clean theoretical character [42], [43], the study of this channel offers a unique opportunity for testing the Standard Model (SM) and for deepening the knowledge of the Cabibbo-Kobayashi-Maskawa (CKM) matrix. Furthermore it is extremely sensitive to possible new degrees of freedom beyond the SM.

At the present time the SM prediction [44], [45] for the branching ratio of the decay of interest is:

$$\mathrm{BR}(K^+ \to \pi^+\nu\overline{\nu}) = (8.5 \pm 0.7)\mathrm{x}10^{-11} \tag{2.1}$$

So far the most precise results, performed with kaon decays at rest and based on seven events [46], have been obtained by the E784 and E949 collaborations at Brookhaven National Laboratory (BNL) [47], [48]:

$$\mathrm{BR}(K^+ \to \pi^+\nu\overline{\nu}) = (1.73^{+1.15}_{-1.05})\mathrm{x}10^{-10} \tag{2.2}$$

2.1 Experimental approach

The experiment will exploit the Super-Proton-Synchrotron (SPS) accelerator at CERN [49], [50], already used for the NA48 experiment, and will be located in the North Area High Intensity Facility (NAHIF). The charged kaon beam is obtained by the collision of the 400 GeV/c primary proton beam from SPS on a beryllium target. Since the cross section to make kaons increases as a function of proton energy is is convenient to use a high energy proton beam. Moreover the higher kaon energy leads to easier photon detection and as a consequence simplifies the suppression of the background originating from $K^+ \to \pi^+\pi^0$. On the other hand, using a high energy beam the pions and the protons cannot be efficiently separated from the kaons. This means that the upstream detectors must sustain a particle flux which is 17 times larger than the useful kaon one. For these reasons and for other considerations about the distance and the length of the decay region and the signal acceptance a kaon momentum of 75 GeV/c has been chosen as central value.

Due to the impossibility to detect the two neutrinos in the final state, different techniques have to be combined to achieve the required background rejection.

Decay mode	Branching ratio	Background rejection
$K^+ \to \mu^+\nu$ ($K_{\mu 2}$)	63%	μ PID, two-body kinematics
$K^+ \to \pi^+\pi^0$	21%	Photon veto, two-body kinematics
$K^+ \to \pi^+\pi^+\pi^-$	6%	Charged particle veto, kinematics
$K^+ \to \pi^+\pi^0\pi^0$	2%	Photon veto, kinematics
$K^+ \to \pi^0\mu^+\nu$ ($K_{\mu 3}$)	3%	Photon veto, μ PID
$K^+ \to \pi^0 e^+\nu$ (K_{e3})	5%	Photon veto, E/p

Table 2.1: Some of the most probable K^+ decay modes and rejection criteria

Basically the experimental apparatus consists of two spectrometers, one for the incoming particles and one for the decay products in the forward direction. An interesting signal would be a final state containing a single π^+. To match this track with the K^+ one, timing, spatial and angular informations are needed. Moreover, other k^+ decay modes can fake the signal if some particles escape detection or are mistakenly identified as pions. Therefore accurate kinematics reconstruction, precise particle timing, efficiency of the vetoes and excellent particle identifications are required to apply the rejection criteria. Particular attention must be payed to the two body decays $K^+ \to \pi^+\pi^0$ and $K^+ \to \mu^+\nu$, which branching ratio is ten orders of magnitude higher than the expected signal. Background coming from three and four body decays must be taken into account too. Table 2.1 shows the most frequent K^+ decay modes together with the techniques intended to reject them. Referring to Fig. 2.1, the only measurable quantities in the experiment are the momentum of both the incoming K^+ and the outgoing π^+ (relatively P_K and P_π) and the angle between them ($\theta_{\pi K}$). Under the hypothesis that the final state is a positive pion

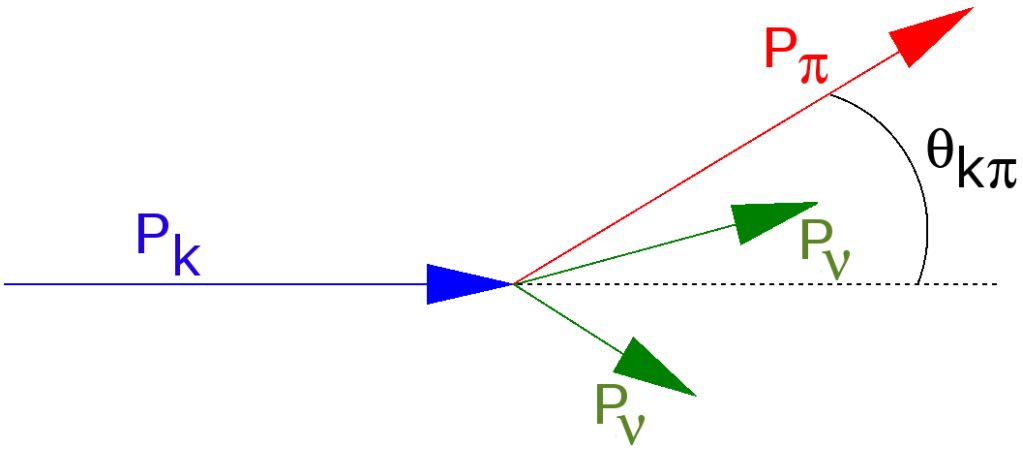


Figure 2.1: Kinematics of $K^+ \to \pi^+\nu\overline{\nu}$

and considering that the angle $\theta_{\pi K}$ is small (see Fig. 2.2), the squared missing mass

variable can be defined as:

$$m^2_{miss} \simeq m^2_K(1 - \frac{|P_K|}{|P_\pi|}) + m^2_\pi(1 - \frac{|P_\pi|}{|P_K|}) - |P_K||P_\pi|\theta^2_{\pi K} \quad (2.3)$$

As shown in Fig. 2.3, two acceptance regions can be defined to be kinematically

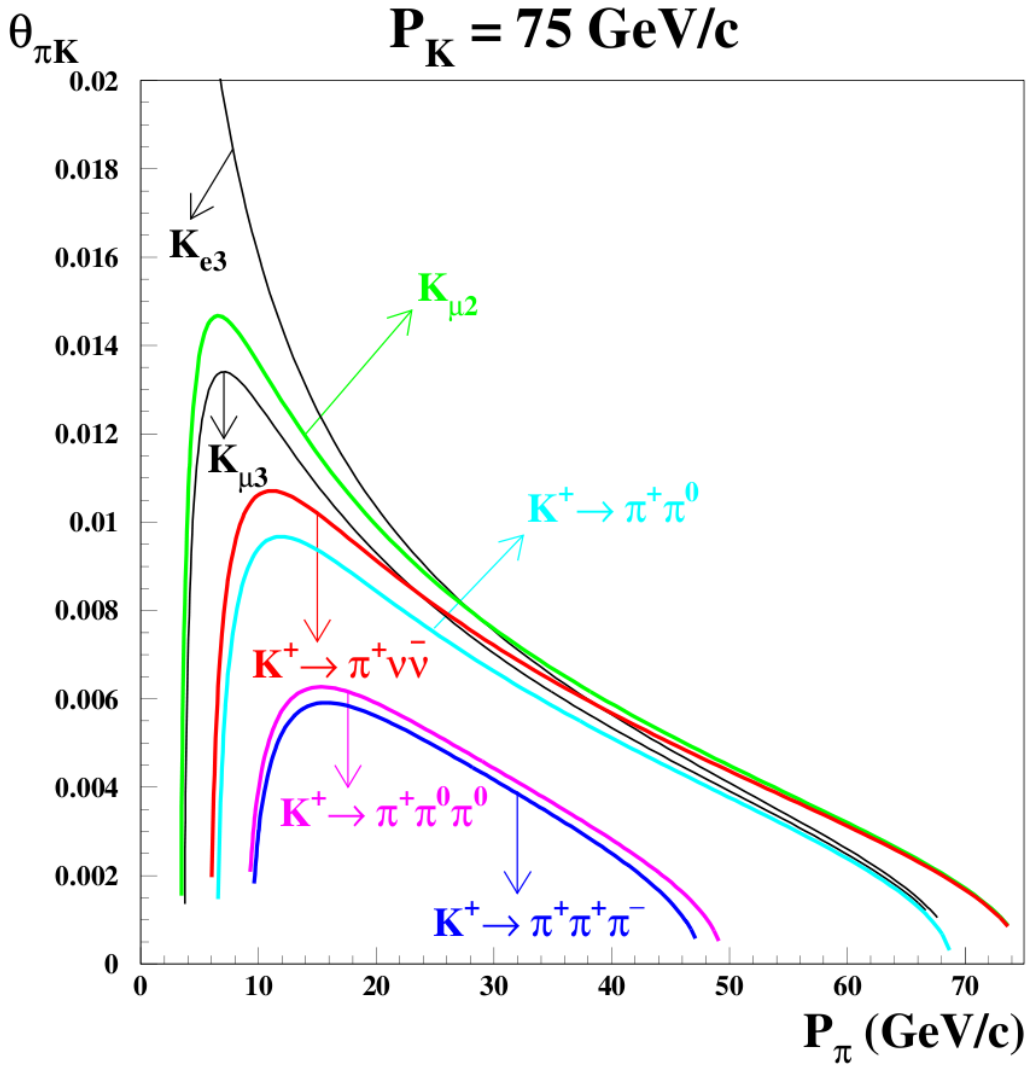


Figure 2.2: Angle-momentum relation for K^+ decays

free from most of the frequent kaon decays for $P_K = 75$ GeV/c. In particular the line of the two pion decay lies in the signal region and the three pion decay imposes a lower bound:

- Region I: $0 < m^2_{miss} < m^2_{\pi 0} - (\Delta m)^2$
- Region II: $m^2_{\pi 0} + (\Delta m)^2 < m^2_{miss} < \min[m^2_{miss}(\pi^+\pi^-\pi^0) - (\Delta m)^2]$

where Δm depends on the missing mass resolution. With a resolution on the kaon momentum at the level of 0.3%, a resolution on the pion momentum better than

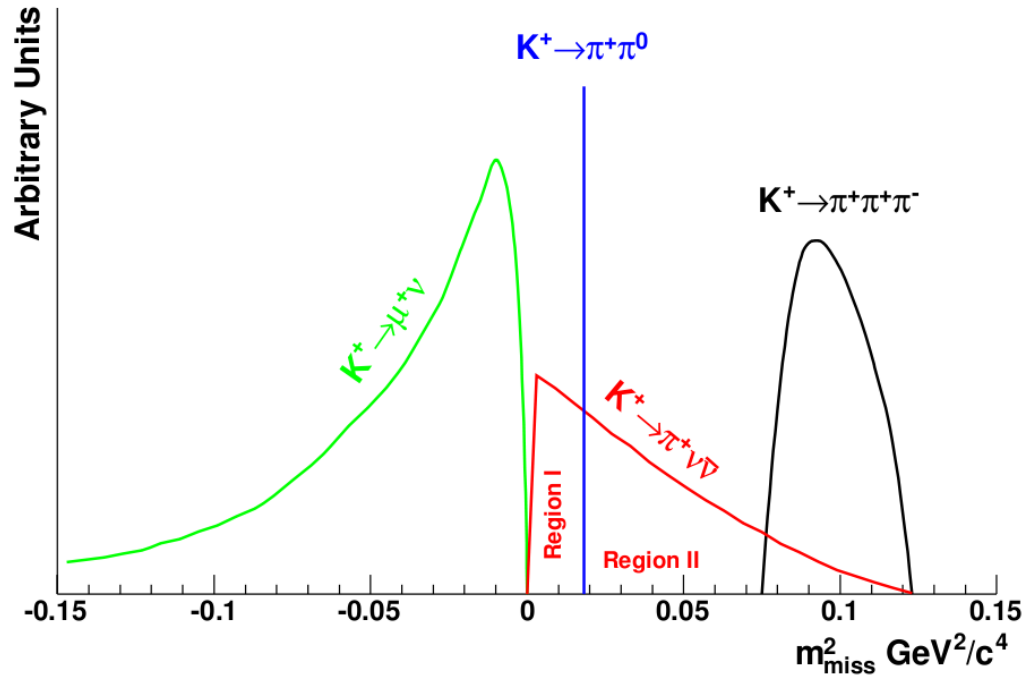


Figure 2.3: Squared missing mass distribution for signal and background events under the hypothesis that the final state is a π^+

1% at 30 GeV/c and a resolution of $\theta_{\pi K}$ of 50-60 μrad, the squared missing mass resolution can be fixed at $(\Delta m)^2 \simeq 8\text{x}10^{-3}\text{GeV}^2/c^4$. The above specifications define the required performance of the upstream and downstream detectors.

2.1.1 Detector layout

The detector elements are described in this section together with their function. The overall beam and detector layout, shown in Fig. 2.4, is inspired by the experience gained in the previous kaon decay experiment NA48 [51] performed at CERN SPS.

The use of a 75 GeV/c secondary beam fixes the distance of the decay region to $\sim$ 100 m and the decay fiducial region to $\sim$ 65 m. The kaon decay products can be recorded by a series of detectors surrounding the beam starting from the begin of the fiducial region.

- The **CEDAR** provides the K^+ identification with respect to protons and pions composing the incoming beam by employing a differential Cerenkov counter.
- The Gigatracker (**GTK**) is composed by three stations of silicon pixel detectors measuring the time, direction and momentum of the beam particles before entering the decay region.
- The **STRAW** detects the direction and momentum of the secondary charged particles originated in the decay region. Chambers of straw tubes are suitable as tracking detectors thanks to their capability to operate in vacuum.

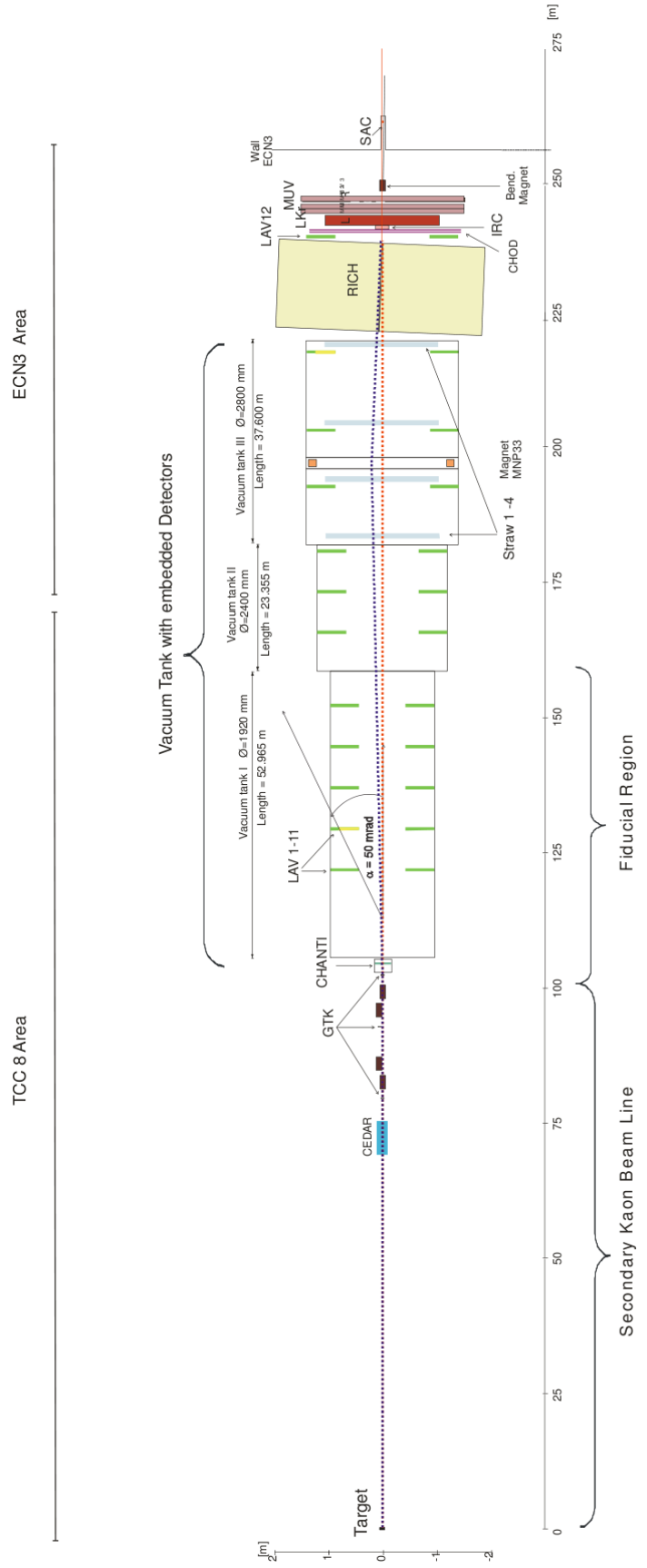


Figure 2.4: NA62 experimental setup

- The **RICH** (Ring Imaging Cerenkov counter) detector performs the separation of pions and muons in the momentum interval between 15 GeV/c and 35 GeV/c.

- A system of photon veto detectors provides hermetic coverage from zero out to large angles ($\sim$ 50 mrad) from the decay region. It is composed by a high performance Liquid Krypton electromagnetic calorimeter (**LKr**) acting in the angular interval between 1 mrad and 15 mrad, by an Intermediate Ring and Small Angle Calorimeters (**IRC** and **SAC**), coverig respectively the area around and in the beam, and by a series of 12 Large Angle Veto detectors (**LAV**) surrounding the vacuum tank and providing the full coverage for angles as large as 50 mrad.

- The MUon Veto detector (**MUV**) provides redundancy with respect to the RICH in the detection of muons. It is composed by a hadron calorimeter followed by additional iron and a transversally segmented hodoscope. It also serves the purpose of deflecting the charged beam away from the SAC photon detector placed in the end of the hall.

- The CHarge ANTI detector (**CHANTI**) consists of scintillators providing additional rejection of the accidental background coming from the hadronic interactions of the beam particles in the last GTK station.

- The material of the RICH may complicate the detection of photons because of conversions or of photo nuclear interactions. To mitigate this inefficiency, Charged HODoscope (**CHOD**) is placed downstream of the RICH.

- All these detectors are operated and interconnected with high performance trigger and data acquisition (**TDAQ**) system.

2.1.2 Tracking stations

As already discussed in this section, the squared missing mass is the most discriminating variable to distinguish the signal from the background and, assuming that the decay particle is a π^+, it allows to reject more than 90% of K^+ decays. The whole NA62 experiment will succeed only if the K^+ and π^+ momenta and angles will be measured with great accuracy. This implies the minimization of the amount of material crossed by the particles. As a consequence the tracking system requires low mass and high precision detectors to measure the momentum of the incoming kaons and of the decay products.

The kaon spectrometer, namely the GTK, is composed by three stations of hybrid silicon pixel detectors matching the beam dimensions and placed in vacuum. It has to sustain the full beam intensity (about 750 MHz) and to provide a time resolution better than 150ps RMS in order to avoid the wrong association of a kaon with the decay particle reconstructed in the downstream detectors. Four dipole magnets provide an achromatic spectrometer for particles of any momentum. The GTK provides a 0.2% RMS momentum resolution and an angular resolution of $\sim 15\mu$rad.

The downstream magnetic spectrometer for positive pion momentum measurement consists of a single dipole magnet with four straw chambers operating directly in vacuum tank to reduce the multiple scattering of the outgoing pions.

2.1.3 Timing requirements

The timing performance of the experiment is set by the need to match the kaon and pion tracks. The fraction of the wrong association can be kept below 1% if a 150 ps time resolution on the beam particles and a 100 ps time resolution on the π^+ tracks are guaranteed. Precise timing for the positive kaons and for the pions is provided respectively by the GTK and by the RICH counter. Due to the high particle rate and to the limited material budget, the timing information on the kaon track with the required resolution is technologically challenging. The NA62 collaboration has performed a full R&D study [52] to demonstrate that excellent timing performance can be achieved using micro pixel silicon trackers.

2.1.4 Veto system

The required background rejection cannot be achieved with the kinematic information alone. This fact involves the necessity of an efficient veto on muons and photons.

Detecting the photons coming from the π^0 decay leads to the suppression of the background due to $K^+ \to \pi^+\pi^0$ channel. The NA62 design insists on the very high detection efficiency of high energy photons in the angular region from zero to 50 mrad from the K^+ decay vertex with respect to the beam line. In fact, in order to consistently detect photons at higher angles it would be necessary to install photon detectors along the entire length of the vacuum tank. Moreover these high angles photons are characterized by low energies which would make their detection difficult. For the same reason the π^+ momentum will be required to be less than 35 GeV/c during the analysis. In this way, the minimum momentum available for the π^0 is 40 GeV/c and such an high energy deposit can hardly be missed by the calorimeters. The LAV, LKr, IRC and SAC calorimeters will perform the photon vetoing on different angles.

Furthermore a muon veto system is mandatory as well to cope with the K^+ decays containing a muon in the final state. The muon veto system (MUV) consists of two iron scintillator hadronic calorimeters (MUV1 and MUV2) separated by an iron wall from a plane of fast scintillators (MUV3). Further muon rejection is provided by the RICH.

Finally the beam hadronic interactions in the last station of the GTK may cause the emission of a leading π^+ which enters the pion acceptance while the associated multiplicity of soft particles can escape from the detector. The CHANTI detector, placed just downstream of the GTK, provides a veto for charged particles to reject this accidental background.

2.1.5 Particle identification

The identification of kaons is a key point for the NA62 experiment, since the 93% of the beam is composed by pions and protons which can interact with the residual gas in the vacuum tank and mimic the signal. The CEDAR detector, placed upstream of the GTK, flags the arrival of a K^+ with the appropriate momentum and with a time resolution of about 100 ps. The precise timing of the CEDAR relaxes the requirements for the residual gas pressure in the decay region to $\sim 10^{-6}$ mbar. The RICH detector, placed after the last straw chamber and equipped with 2000 phototubes, provide an additional 10^2 factor of suppression of background originating from the $K^+ \to \mu^+\nu$ decays. It also distinguishes the positrons from the positive pions, allowing the suppression of events with positrons in the final state, such as $K^+ \to \pi^0 e^+\nu$, or channels with a $\pi^0 \to \gamma e^+ e^-$ decay. The RICH is filled with Ne at atmospheric pressure. The pion Cerenkov threshold of the Ne is ~ 13 GeV/c, therefore a minimum π^+ momentum of 15 GeV/c is required to ensure full efficiency. Finally, the RICH provides a redundant measurement on the π^+ momentum. In addition the LKr detector provides powerful particle identification not only for muons, but also for positrons and electrons.

2.2 The GTK detector

2.2.1 Detector requirements and architecture

The GTK is one of the key elements for the NA62 experiment. It has to provide precise measurements of momentum, time and angle of the incoming 75 GeV/c kaons. The GTK is composed by three stations of hybrid silicon pixel detectors mounted around four achromat magnets as shown in Fig. 2.5. In each station (see

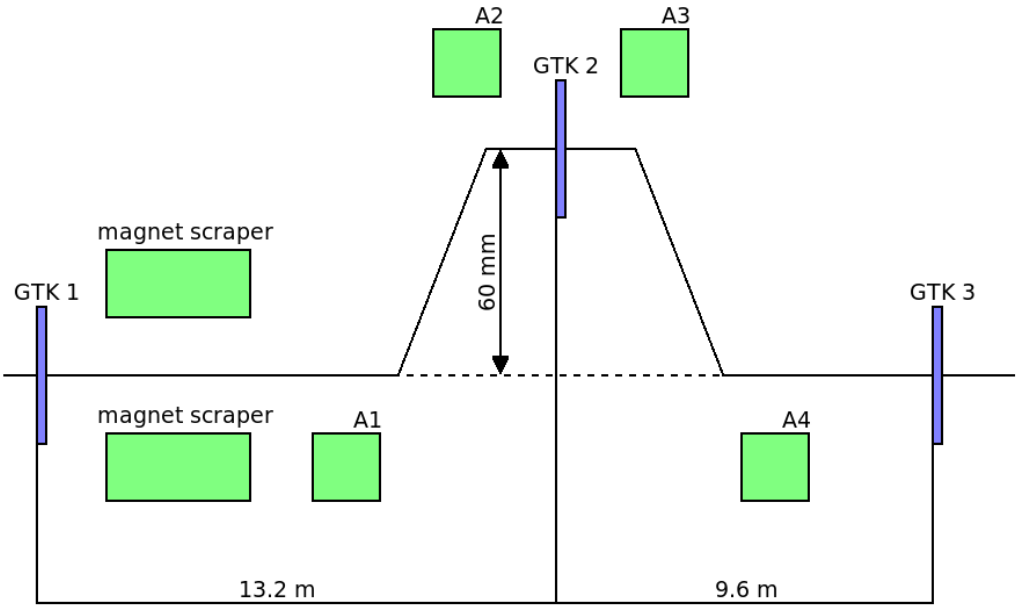


Figure 2.5: Schematic layout of the Gigatracker

Fig. 2.6) the expected beam area of 60 mm x 27 mm is completely covered by one single, fully active silicon sensor bump-bonded to 2 x 5 read-out chips. The read-

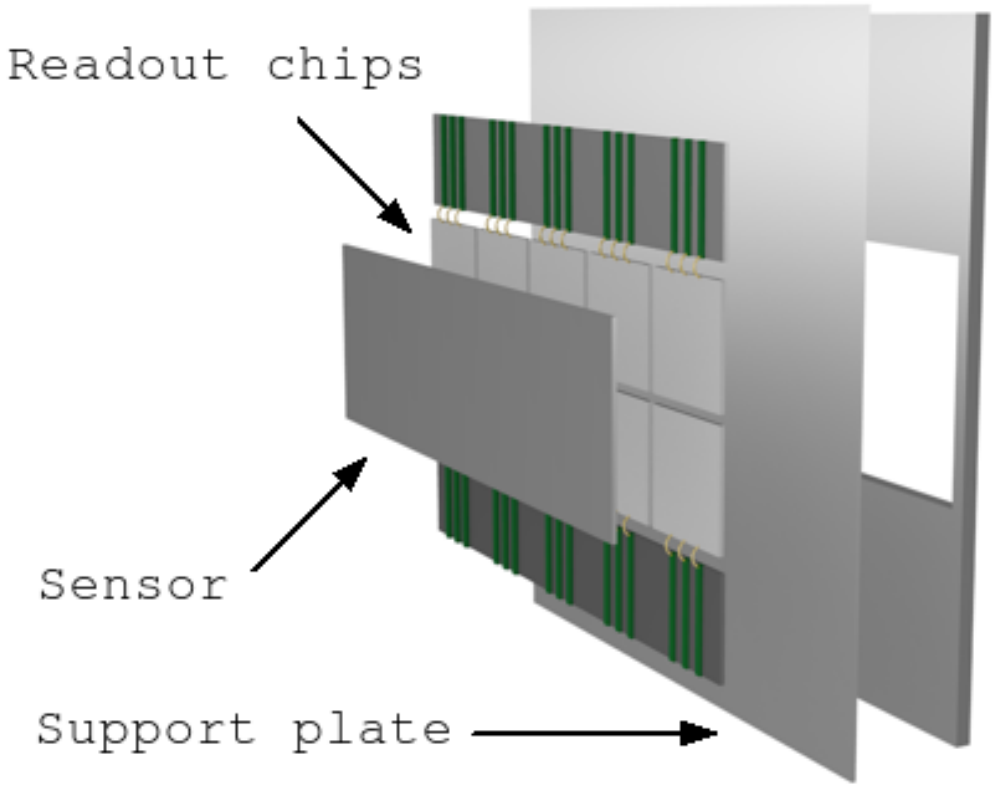


Figure 2.6: GTK single station scheme. The ten ASIC chips bump bonded to the sensor are supported by a carbon plate outside the beam area

out is accomplished with ten ASIC chips, each containing 1800 pixel having an area of 300 μm x 300 μm and organized in a matrix of 45 x 40 elements. In order to cover the total active area, the ASICs are accessible only from the top and from the bottom of the assembly as shown in Fig. 2.7.

The detector is placed along the beam line just before the decay fiducial region. It is exposed to a very high and non uniform beam rate of 0.75 GHz in total, hence the name Gigatracker, with a peak of 130 MHz/cm^2 around the center. For this reason the GTK will be replaced every 50 days of data taking. Moreover, to reduce the leakage in the silicon sensor, the GTK must be cooled at 5° C or below. This requirement limits the power dissipation by the ASIC chip to be lower than 2 W/cm^2.

The informations given by the GTK, together with the STRAW Tracker measurements on the outgoing pions, will be used to reconstruct the squared missing mass. Simulations of the kaon decays in the detector have determined the GTK momentum and direction resolution requirements. Form this study and taking into account the expected STRAW resolution, it has been derived that the GTK must be able to measure the momentum with a resolution of $\sigma(P_K)/P_K \sim 0.2\%$ and the direction with a resolution of 16 μrad [53]. A 300 μm x 300 μm pixel is sufficient to achieve the required resolution.

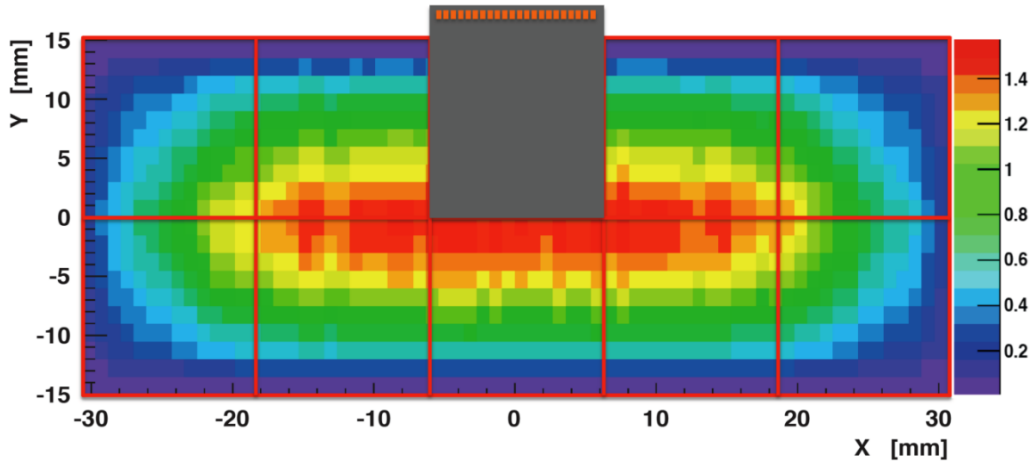


Figure 2.7: GTK beam intensity distribution expressed in MHz/mm^2. The ASICs placed in the central region of the beam must sustain a higher particle flux

Since it has to work in a strong radiation environment, the beam spectrometer is installed in vacuum with a minimal amount of crossed material to minimize the hadronic interactions and the beam defocusing. The amount of material crossed by the beam at each station influences the angle measurement. The upper limit, which has been set to 0.5% X_0, imposes the thickness of the sensor and the read-out ASIC to be respectively 200 μm and 100 μm (see Table 2.2).

Component	Material	Thickness (μm)	X_0 (%)
Sensor	Si	200	0.21
Bump bonds	Pb-Sn	26	0.001
Readout chip	Si	100	0.11
Support plate	C	100	0.05

Table 2.2: GTK components material budgets

Last but not least, due to the high rate, the matching between the incoming and outgoing particles imposes a time resolution of 200 ps RMS per station on the single hit, allowing to achieve a track resolution better than 150 ps RMS. This is an ambitious requirement for a silicon pixel detector and none of the existing system has such a capability. Table 2.3 summarizes the GTK specifications.

Material budget per station	0.5% X_0
Overall efficiency per station	$> 99\%$
Average particle rate	45 kHz/pixel
Maximum particle rate	135 kHz/pixel
Power dissipation	$<$ 2mW/pixel
Dynamic range	1-10 fC
Pixel size	300 μm x 300 μm
Time resolution per station	$<$ 200 ps RMS

Table 2.3: GTK detector requirements

2.2.2 The silicon sensor

The silicon sensor is based on the p-in-n planar technology, due to the simpler processing procedures, availability and the relatively low cost compared to other solutions. Its has been studied in simulations that a 200 μm thickness is a good compromise to match the material budget constraints with the signal requirements for precise timing. The sensor will operate at high over-depletion with 500 V bias voltage. To ensure a stable operation a multi-guard ring structure has been developed. The charge collection efficiency, speed and the capacitance of the sensor strongly influences the overall time resolution. Operating in a strong radiation environment, these parameters are deteriorated, the leakage current increases and the depletion voltage changes. A detailed study [54] on the radiation damage effects has been carried out using test p-in-n test diodes irradiated up to a fluence of 2 x 10^{14} 1 MeV n_{eq} cm^{-2}. It has been found that the maximum acceptable operating temperature for the GTK stations is 5° C, which allows an operation time of 50 days. Measurements indicated that the leakage current of a full size sensor at an operating temperature of 5° C and 50 days of operation will reach approximatively 270 μA.

Chapter 3

Front-end architectures for NA62 GTK

As described in the previous chapter, the design of the pixel readout for the GTK dictates challenging requirements in terms of pixel size, particle rate, time resolution, power consumption, material budget and radiation exposure. The integration of the analog front-end together with the data processing and the high speed data acquisition and readout logic is a critical issue, since the induced digital noise on chip might compromise the analog performance. Moreover, considering the data rate, the readout adopts a triggerless architecture and the communications to and from the pixels are sent via high speed differential signals.

3.1 Time-walk compensation

Fig. 3.1 shows the expected charge distribution for the experiment. With the available signal charge (from 1fC to 10fC) the time walk compensation is mandatory to achieve the required time resolution of 200 ps.

As already discussed in Chapter 1, given its systematic nature, it is possible to correct the time walk off-line using the ToT technique. The signal amplitude is measured by recording the times at which the leading and the trailing edges of the discriminator pulse cross the threshold. Besides increasing the amount of data to be transmitted, a very precise calibration of the time-walk vs ToT curve must be performed for each pixel to get the required timing accuracy.

Alternatively a self-compensating CFD based circuit can be used. The bipolar signal with the zero crossing time independent from the signal amplitude gives directly the precise time information without the burden of calibrations. Drawbacks are a more complex architecture, higher space occupation and power consumption.

For the GTK application both techniques have been investigated and appear to be promising. Compensation by sampling the signal shape with a Flash ADC has been excluded for size and power consumption reasons.

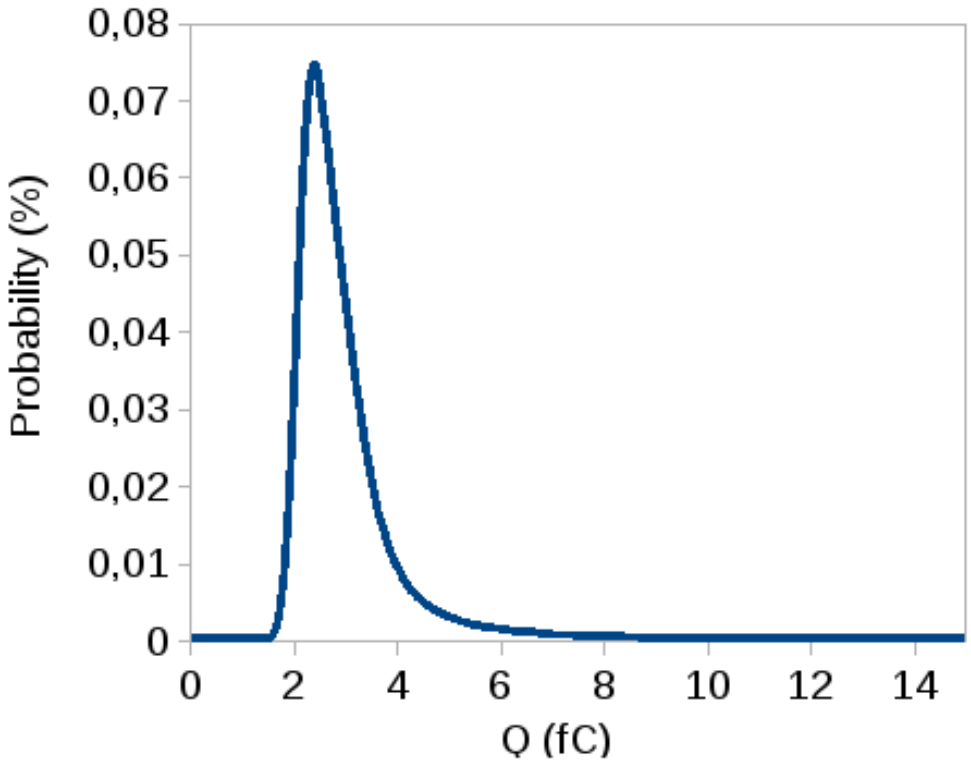


Figure 3.1: Landau distribution of input charges generated in 200 μm silicon layer with most probable value around 2.4 fC

3.2 Time to digital conversion

The implementation of the time measurement within the specified constraints is an interesting issue. While a coarse time information with the resolution of the clock is directly accessible, the precise time measurement with respect to the clock counter reference can be obtained using a Time to Digital Converter (TDC). Solutions using a Delay Locked Loop (DLL) based TDC and a Time to Analog Converter (TAC) followed by a dual slope Wilkinson ADC have been investigated in the R&D of the GTK detector.

The scheme of a DLL based TDC is shown in Fig. 3.2. A set of clock signals is generated by a chain of calibrated delay elements controlled in voltage by the charge pump. These signals are used to clock the hit register which samples the input signal and latches its time position. Finally, encoding the hit register content, the digital information is available. This fast circuit can be adopted only if the same TDC is shared by a group of pixels.

The dual slope Wilkinson TDC follows an analog approach and entails less electronic noise and a relatively small area. In principle it can be implemented on pixel. The time information is obtained using a TAC by charging a capacitor with a calibrated constant current at the signal arrival and stopping it on an appropriate clock edge. The result is a voltage ramp which maximum voltage is proportional to the charging time window. Subsequently the capacitor is discharged to the reference voltage using a lower current. This leads to a longer ramp whose duration can be measured with a clock counter. The length of the slower ramp is proportional to

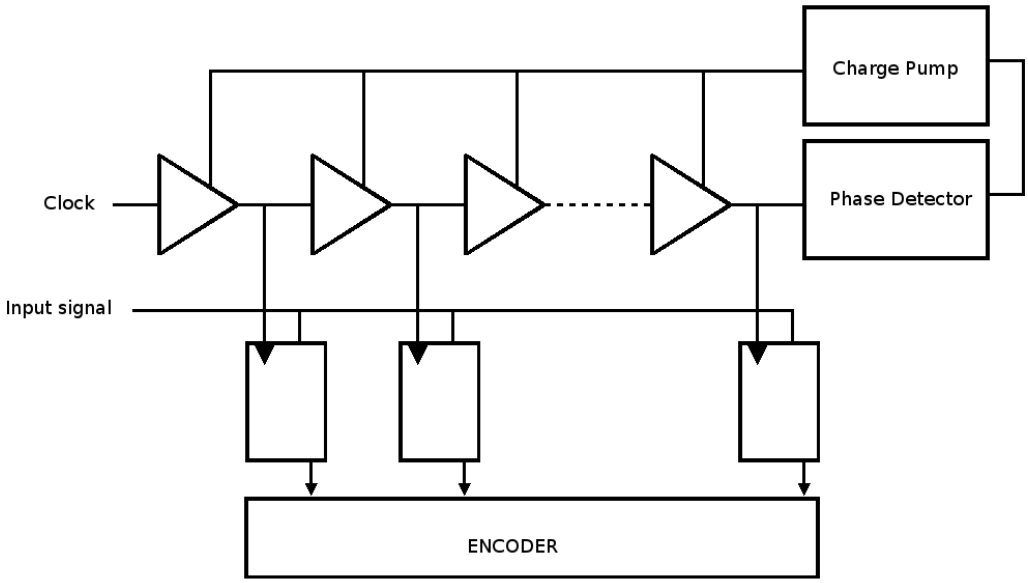


Figure 3.2: The DLL based TDC principle

the starting voltage, and thus to the time window.

3.3 Two complementary architectures

The final ASIC will contain 1800 independent channels organized in a matrix of 45 rows per 40 columns of pixels of 300 μm x 300 μm. The key constraint is the maximum power consumption of 2 mW per pixel. In fact at state of the art ICs developed for this purpose typically have a power consumption above 10 mW/channel and a number of channels in the order of 8-16 per chip [55].

Most modern CMOS technologies use a heavily doped p^+ substrate. The low resistivity of the substrate creates unwanted paths between various devices in the circuit, corrupting sensitive signals. For this reason and for other considerations about area, power specifications and radiation hardness, the 130 nm CMOS technology has been chosen. It has a relatively high substrate resistivity when compared to other technologies, such as the 250 nm. This makes it easier to insulate the digital and analog blocks by means of guard rings. However, the high sensitivity of the analog front end requires the use of insulations techniques. Dedicated wells for noisy and sensitive blocks should be used and the circuit should be implemented to reduce the digital noise, for example using differential analog and digital architectures.

In order to understand which timing solution have more adequate performances for this application, two complementary architectures have been explored [56] [59].

The P-TDC option (Fig. 3.3) follows an ambitious approach trying to exploit the relatively big area of the pixel to perform already at pixel level all signal processing, including time to digital conversion and online time walk compensation. A reference clock need to be distributed over the entire pixel matrix posing a possible noise source to the analog front end electronics.

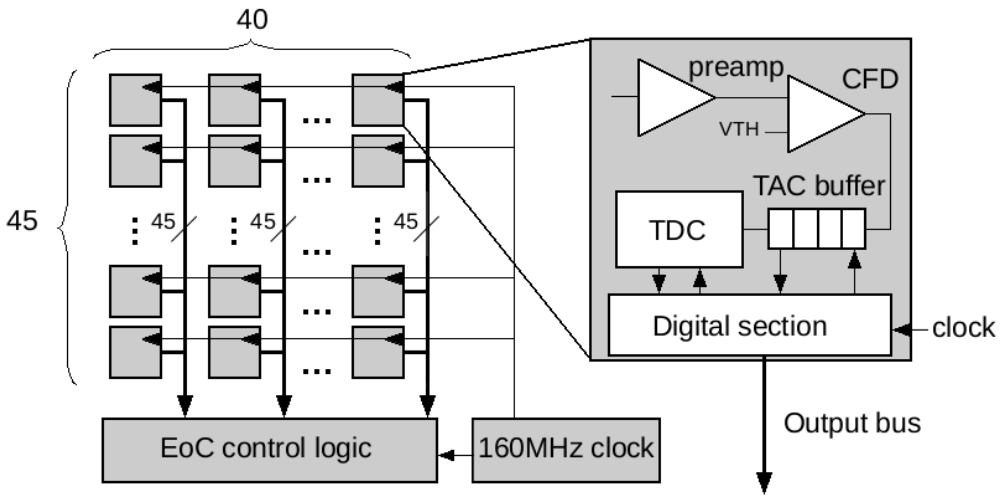


Figure 3.3: The P-TDC architecture block diagram

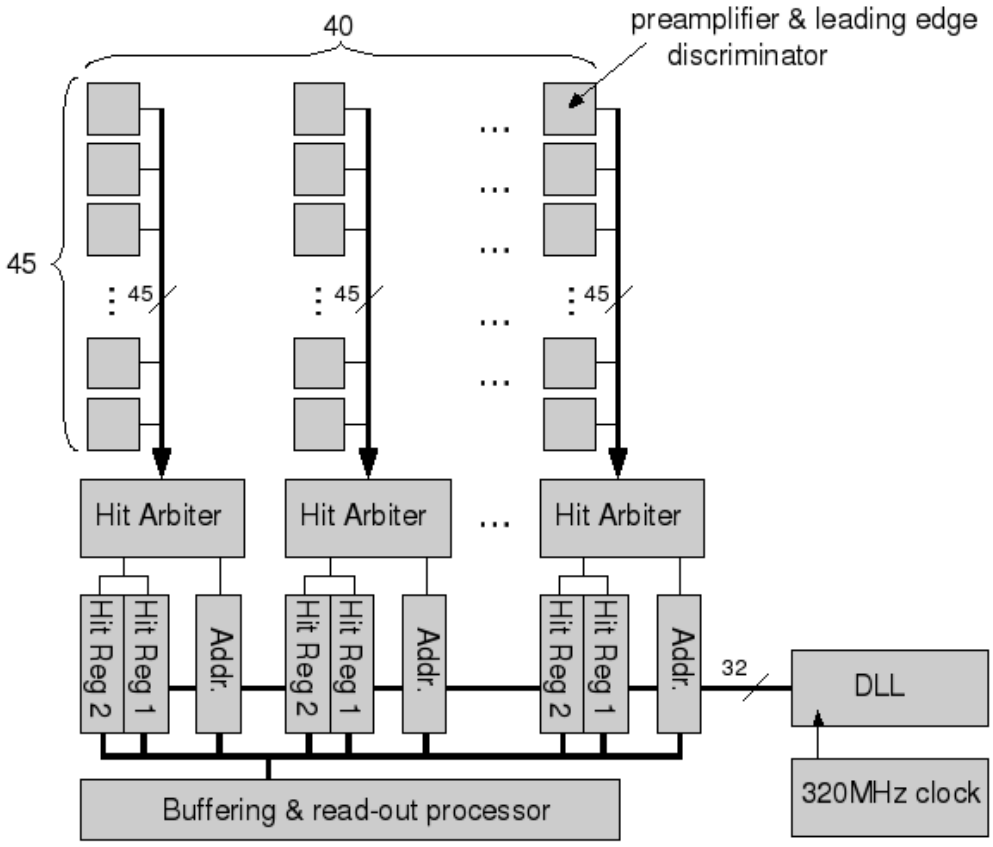


Figure 3.4: The EoC-TDC architecture block diagram

The complete separation between the analog and the digital sections is the key feature of the EoC-TDC solution (Fig. 3.4). The discriminator output of each pixel is sent to the end of column where a set of TDCs shared by a group of pixels store the arrival time of the particle and the ToT information. In this configuration, the pixel cell is maintained simple and no clock signal needs to be distributed to the matrix, but the discriminator output travels through the whole matrix to be evaluated in the end-of-column. The base idea of the EoC-TDC option is to maintain the pixel cell as simple as possible. At this scope each channel contains only the analog electronics with a transmission line driver which sends the discriminator signal to the end of column. Here a DLL based TDC [57] [58] tags the rising and the falling edges of the discriminator signal with a time precision of 100 ps. In order to minimize the amount of TDC registers, 5 not-neighboring pixels in a column are multiplexed together and connected to the same TDC using a combinatorial Hit Arbiter circuit. Simulations showed that for the worst case the hit efficiency stays above 99.5%. Finally the two timing words, together with the pixel address, are stored in a FIFO, serialized and sent out of the chip. The amplitude information is then available to perform off-line time walk compensation.

A block diagram of the pixel cell of the EoC solution is shown in detail in Fig. 3.5. Each cell is composed by a single ended transimpedance preamplifier followed by a single ended to differential post amplifier, by a two stage ToT discriminator (the second stage with hysteresis) and by a dynamic asynchronous latch comparator. The comparator output is sent to a line current driver with pre-emphasis which transmits on a coplanar transmission line.

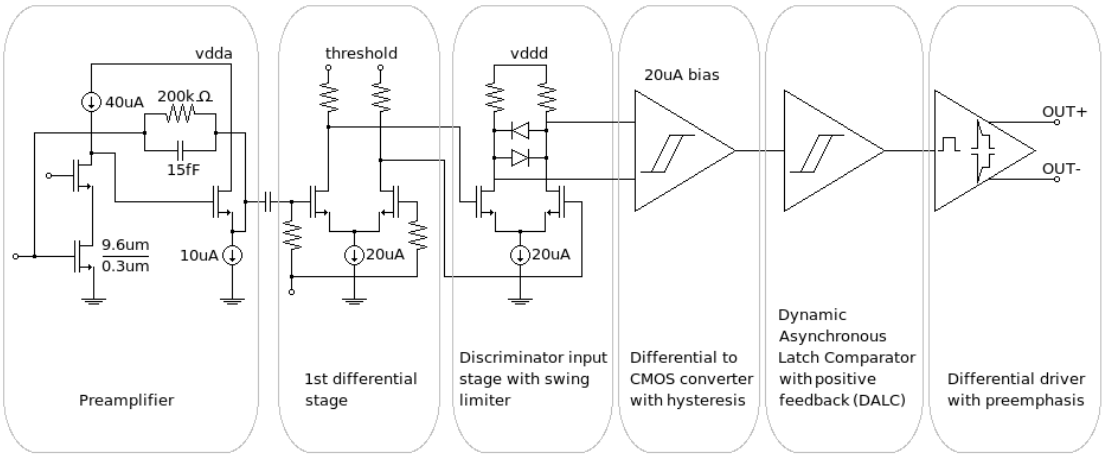


Figure 3.5: Block diagram of the EoC pixel cell

The preamplifier is a simple cascode amplifier with NMOS input transistors biased at 40 μA with an RC feedback. The dimensions of input transistors have been optimized for the detector capacitance of 250 fF. The external differential threshold voltage is applied to the input signal in the first differential stage. The fully differential structure of the comparator insures a very good rejection of the common mode noise arising from the digital power supply. The entire preamplifier shaper has an overall gain of 70 mV/fC with a 5.5 ns peaking time and a CR-RC3 like shaping function. The following comparator stages are characterized by high

sensitivity and high speed performance at a reasonable power of 50 μW.

During the transmission of the discriminator output to the end of column, both the rising and the falling edges of the ToT signal must be preserved to keep the jitter at low values. The use of traditional CMOS inverters as receivers is avoided by the fact that they introduce delays proportional to the input capacitance, hence to the transmission line length. Moreover the large voltage swing limits the transmission speed. Using transmission lines the resistive energy losses are limited [61] [62]. They are nothing more than coplanar waveguides where signal components of different frequencies travel at the same speed. The differential voltage swing of 240 mV is driven in current by the driver in the pixel cell in order to preserve the same signal amplitude, independently from the resistance of the transmission line. However the high series resistance of transmission lines degrades the signal edge. To cope with this effect, a current pre-emphasis is implemented in the line driver allowing to achieve a rise time of 1 ns at the receiver input for the farthest pixels.

The transmission line receiver is presented in Fig. 3.6. The input stage bias-

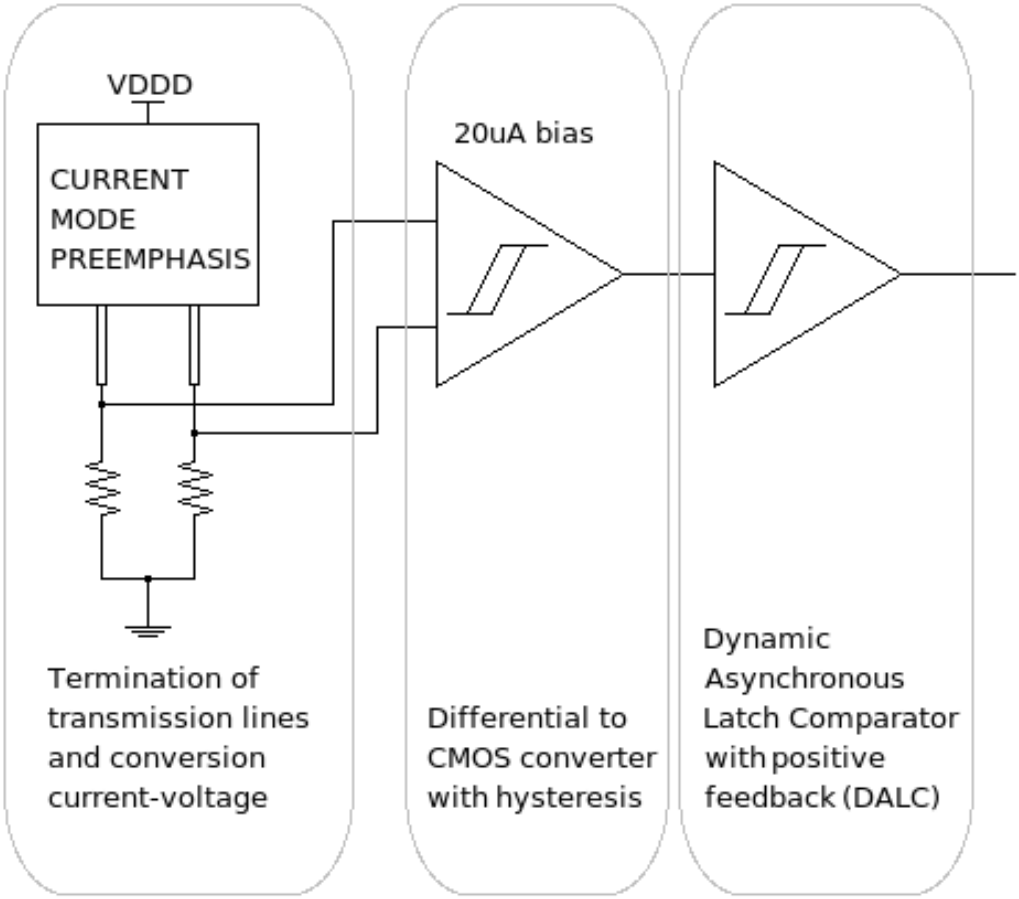


Figure 3.6: Block diagram of the transmission line receiver

ing is provided directly by the static current of the transmission line of about 150 μA. It is followed by a differential to CMOS converter with hysteresis and by a Dynamic Asynchronous Latch Comparator (DALC). The DALC does not consume static power. It uses a positive feedback during transitions to generate fast transition

signals, with 50 ps edges, to drive the TDC input.

At this point the precise time measurement is performed by the DLL based TDC. The DLL delay chain consists of 32 buffers connected in series. Once the DLL is locked, one clock period is exactly segmented by the number of buffers in the chain. Since the EoC TDC works with a 320 MHz clock reference, the TDC time bin is 100 ps. When a hit arrives, the state of these buffers is latched in the hit register to give the fine time information, while the coarse time is obtained by latching a clock counter. As already discussed, in order to reduce the amount of registers, each TDC is shared by 5 pixels. For a 45 pixel column, this leads to 18 registers for column, 9 for the rising edges and 9 for the falling ones. Moreover, in order to process clusters and pixel charge sharing, the pixel group feeding each TDC is formed by pixels that are not adjacent.

3.3.1 The P-TDC architecture

The principle of this solution is to perform time walk compensation, using a CFD, and digital conversion, by mean of a TAC based TDC, in each pixel cell (see Fig. 3.7). In this way only digital signals are exchanged from the pixel matrix to the end of column. Performing signal processing at pixel level involves the necessity of distributing the clock and the Gray-encoded coarse counter through the entire chip. For the transmission of the 160 MHz clock a dedicated transmission line is used for each pair of columns. The clock is the most critical signal and its distribution with high precision must be taken carefully into account. Each column is readout by a dedicated controller which data output is serially sent out of the chip. Finally, it is important to note that the presence of a considerable digital logic inside the pixel, thus directly on the beam, involves the need of Single Event Upset (SEU) protection [63]. For this reason all registers, buffers and state machines inside the pixel are Hamming encoded and capable of single error correction and double error detection.

3.3.1.1 The P-TDC pixel cell

In Fig. 3.8 it is sketched the implementation of the time measurement. A 10 bit bus time stamp with the resolution of the clock is distributed to all the pixels. A first coarse time information is obtained by storing the time stamp value at the rising edge of the CFD output. The fine time is provided by the TDC. A calibrated voltage ramp is started at the signal arrival and is stopped on the first half clock rising edge following a falling edge. The voltage reached by the ramp is proportional to the time elapsed between the occurrence of the hit and the next time stamp. This voltage, converted in a digital form by a Wilkinson ADC, gives the fine time information. While performing the conversion, one should take into account the potential misalignments within the coarse and fine time logic, which might occur when the CFD fires in proximity of a clock transition. For this reason the TDC works at half clock frequency. In this way the LSB of the coarse counter overlaps the MSB of the fine time, thus making digital error correction possible. Moreover a proper settling of the circuit generating the ramp is guaranteed, since the minimum voltage ramp duration is one master clock period. Similarly, an offset is added at the

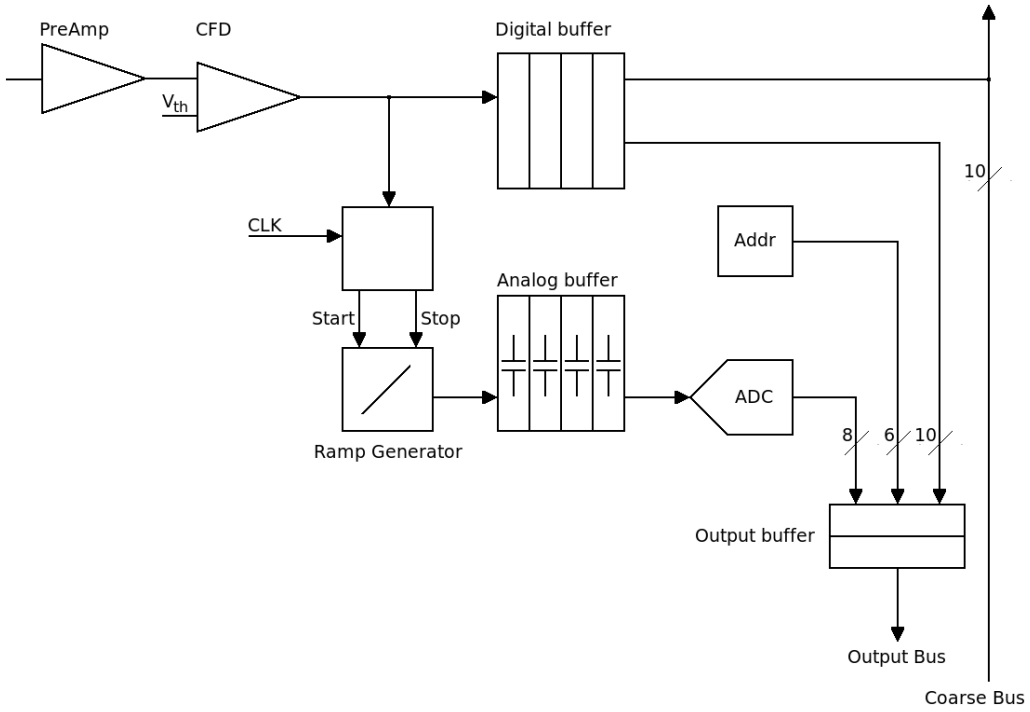


Figure 3.7: Block diagram of the P-TDC pixel cell

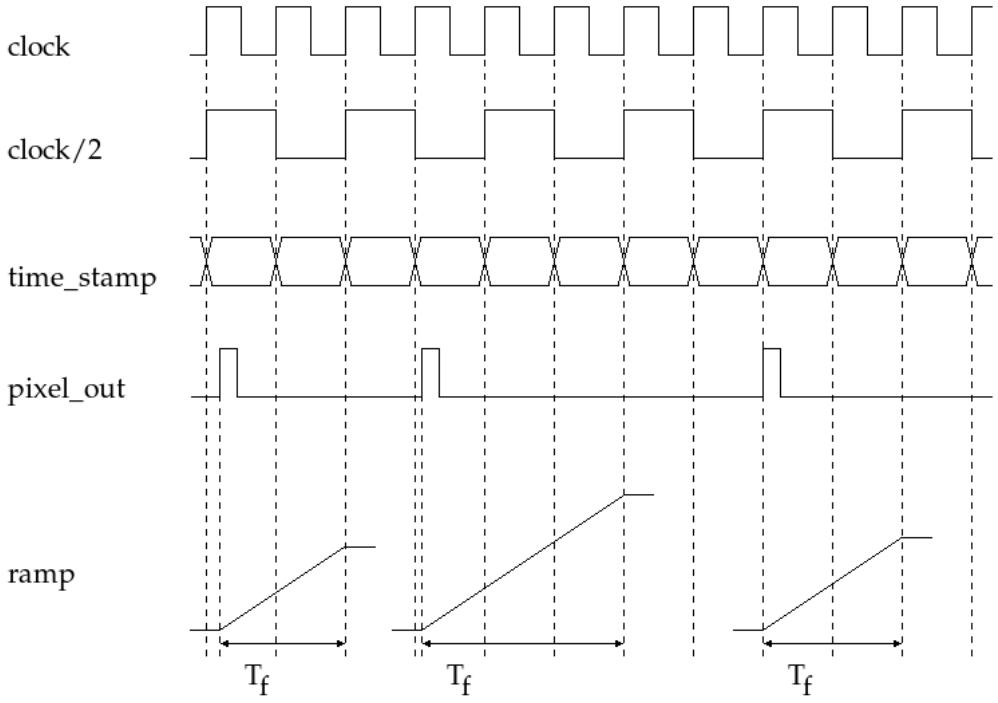


Figure 3.8: Generation of the time information in the TAC based TDC

end of the ramp to avoid that it is stopped too soon because of comparator offsets. Thus, since at the maximum the ramp lasts three master clock cycles, the TDC has been designed to cover four cycles. Using an 8 bit ADC to cover four master clock cycles corresponds to a bin of $\frac{4 \cdot 6.25 \text{ ns}}{2^8} = 98$ ps. This leads to a ratio between the fast and the slow ramp of 1:64. Thus the maximum time needed to perform the fine time conversion reaches $3 \cdot 64 \cdot 6.25$ ns $= 1.2$ μs. A complete 18 bit time word is then available to be readout and to reconstruct the total time information offline. Refferring to Fig. 3.8, depending on the value of the fine time and in the ideal case in which the TDC value is included between 64 and 192, the time of arrival of the signal can be calculated as shown in Table 3.1, where T_c is the coarse time given by the time stamp value times the clock period (namely 6.25 ns) and T_f is the fine time given by the TDC value times the TDC bin (98 ps).

T_f	TDC value	fine MSB	total time
$1T_{ck} \div 2T_{ck}$	$64 \div 127$	0	$T_c + 2T_{ck} - T_f$
$2T_{ck} \div 3T_{ck}$	$128 \div 192$	0	$T_c + 3T_{ck} - T_f$

Table 3.1: Total time reconstruction equations

Depending on the chip initialization the coarse counter can be in counter phase or in phase with the half clock. In the first case, for example, even coarse values (coarse LSB = 0) correspond always to ramps shorter than two clock cycles (fine MSB = 0) and viceversa. When the signal arrives in proximity of a clock transition, it may happen a condition of error which can be easily identified by the value of the coarse LSB and of the fine MSB, as shown in Table 3.2. For each error state in

coarse LSB	fine MSB	total time
0	0	$T_c + 2T_{ck} - T_f$
1	1	$T_c + 3T_{ck} - T_f$
0	1	Error 1
1	0	Error 2

Table 3.2: Error conditions in the particular configuration in which the coarse counter and the half clock are in counter phase

table 3.2 there are two possible conditions with different correction formulae. For example, referring to Fig. 3.9, if $T_f = 3T_{ck} - \epsilon$ and a even coarse time is recorded it means that the coarse counter is late with respect to the half clock and the previous coarse value has been latched instead of the right one. The error can be corrected by adding $1T_{ck}$ in the formula $T_c + 3T_{ck} - T_f$. Similarly if $T_f = 2T_{ck} + \epsilon$ and the coarse time is even, it means that the coarse counter arrives early with respect to the half clock and the cited formula is corrected by subtracting $1T_{ck}$. Similar corrections

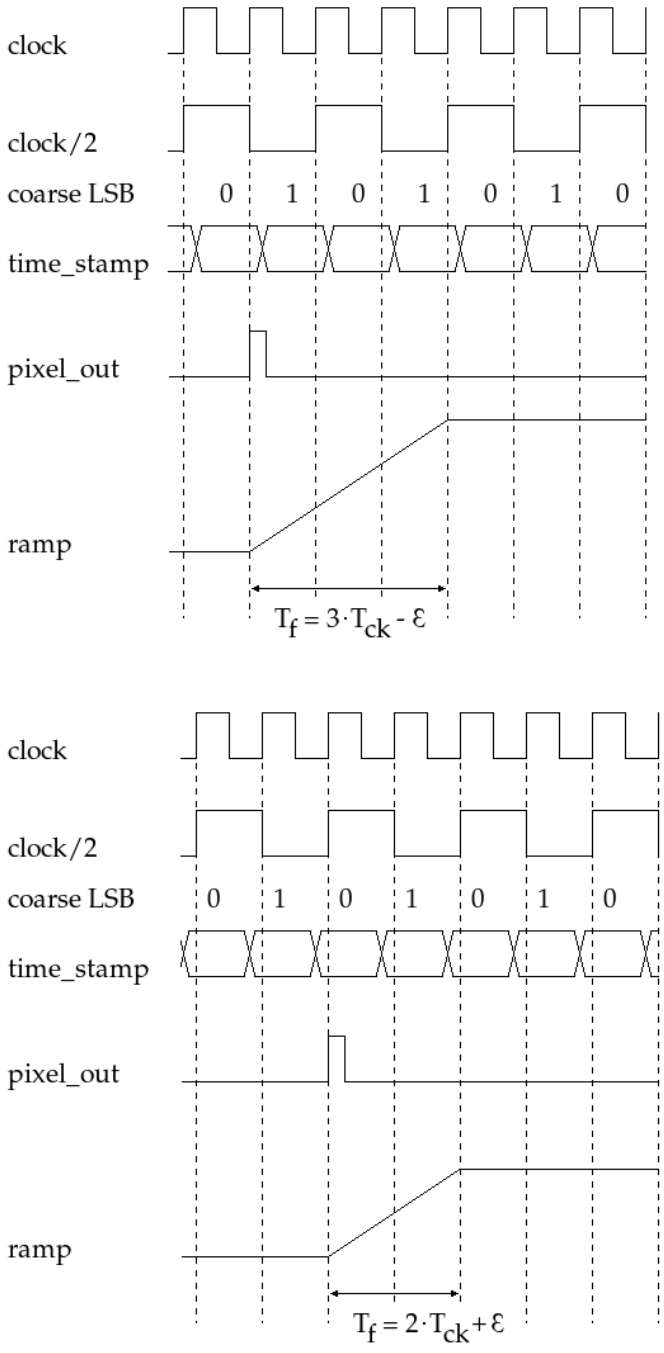


Figure 3.9: Possible conditions which can lead to the state *Error 1*

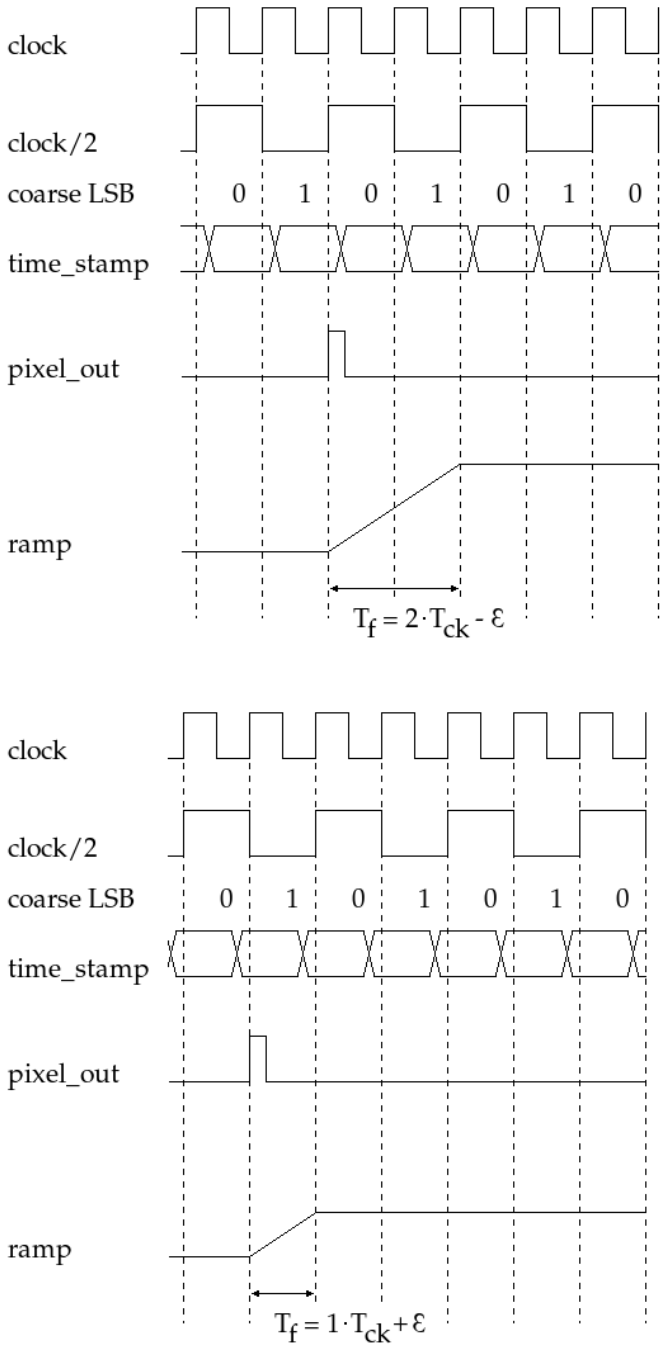


Figure 3.10: Possible conditions which can lead to the state *Error 2*

should be performed for the error state in which the fine MSB is equal to 0 (see Fig. 3.10). All the error conditions with their respective correction are summarized in Tables 3.3 and 3.4.

coarse LSB	fine MSB	T_f	total time
0	0		$T_c + 2T_{ck} - T_f$
1	1		$T_c + 3T_{ck} - T_f$
0	1	$3T_{ck} - \epsilon$	$T_c + 4T_{ck} - T_f$
0	1	$2T_{ck} + \epsilon$	$T_c + 2T_{ck} - T_f$
1	0	$2T_{ck} - \epsilon$	$T_c + 3T_{ck} - T_f$
1	0	$1T_{ck} + \epsilon$	$T_c + 1T_{ck} - T_f$

Table 3.3: Time reconstruction including error correction in the configuration in which the coarse counter and the half clock are in counter phase

coarse LSB	fine MSB	T_f	total time
0	1		$T_c + 2T_{ck} - T_f$
1	0		$T_c + 3T_{ck} - T_f$
1	1	$3T_{ck} - \epsilon$	$T_c + 4T_{ck} - T_f$
1	1	$2T_{ck} + \epsilon$	$T_c + 2T_{ck} - T_f$
0	0	$2T_{ck} - \epsilon$	$T_c + 3T_{ck} - T_f$
0	0	$1T_{ck} + \epsilon$	$T_c + 1T_{ck} - T_f$

Table 3.4: Time reconstruction including error correction in the configuration in which the coarse counter and the half clock are in phase

Considering the clock frequency of 160 MHz, the maximum expected pixel rate of 140 kHz and the maximum conversion time of 1.3 μs, a multi-buffering scheme is mandatory to ensure the required efficiency.

According to the queue theory [64] [65] and considering that physical events in the pixel follow a Poisson time distribution, the probability P(k) of arrival of k events in the time interval τ is given by:

$$P(k) = \frac{(\lambda\tau)^k e^{-\lambda\tau}}{k!} \tag{3.1}$$

where λ is the maximum expected event rate (140 kHz) and τ is the maximum conversion time of 1.3 μs. The required number of buffers n can be estimated using the following formula [64]:

$$P_{LOST}(n) = 1 - \Sigma_{k=1}^{n} \frac{(\lambda\tau)^{k-1} e^{-\lambda\tau}}{(k-1)!} \tag{3.2}$$

It gives the fraction of arriving events which will find the FIFO busy, thus the probability $P_{LOST}(n)$ of losing one event using n buffers. The result is shown in Fig. 3.11.

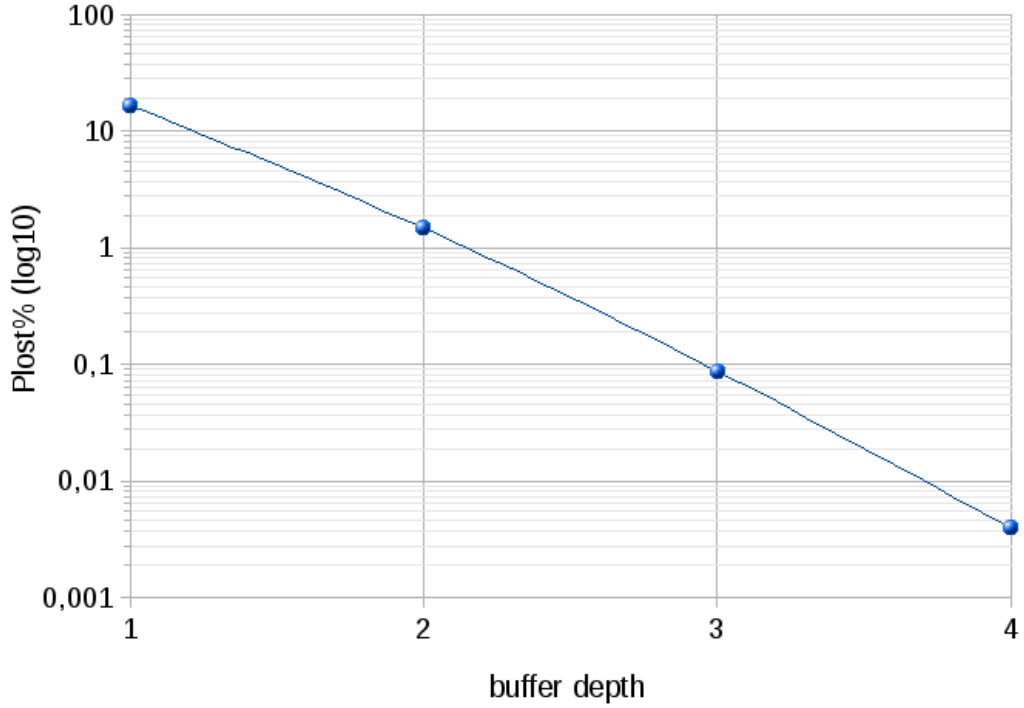


Figure 3.11: Probability of losing one event with a number of buffers from 1 to 4

The buffer depth has been simulated using the VHDL pixel model sketched in Fig. 3.12. The use of buffers allows to derandomize the data and to relax the requirements for the pixel readout. In the model the TDC is represented as a clock counter with 100 ps time resolution. When an event arrives, the coarse and fine times are stored in their respective FIFOs. After the conversion time the FIFOs are readout and the complete time information is written in the output buffer, where it remains until it is readout by the EoC. In the simulations 10000 events where generated. The conversion time follows a uniform distribution between 550 ns and 1.3 μs and the output buffer readout time is set to 575 ns, which is defined by the EoC logic. Simulations were performed for pixel rates higher than expected to evaluate the impact on the model. The results compared with the theoretical prediction are reported in Tables 3.5 and 3.6. The theoretical probability of event loss has been calculated in the cases of 3 and 4-level FIFOs using equation 3.2. The value of τ has been chosen as the maximum conversion time of the circuit (1.3 μs). In VHDL simulations the dead time is uniformly distributed between 550 ns and 1.3 μs, which is a more realistic situation. Thus the theoretical prediction of lost events is overestimated. The results of simulations and of predictions show that a 4-level FIFO gives a large margin to keep the overall inefficiency well below the 1% even at rates much higher than expected.

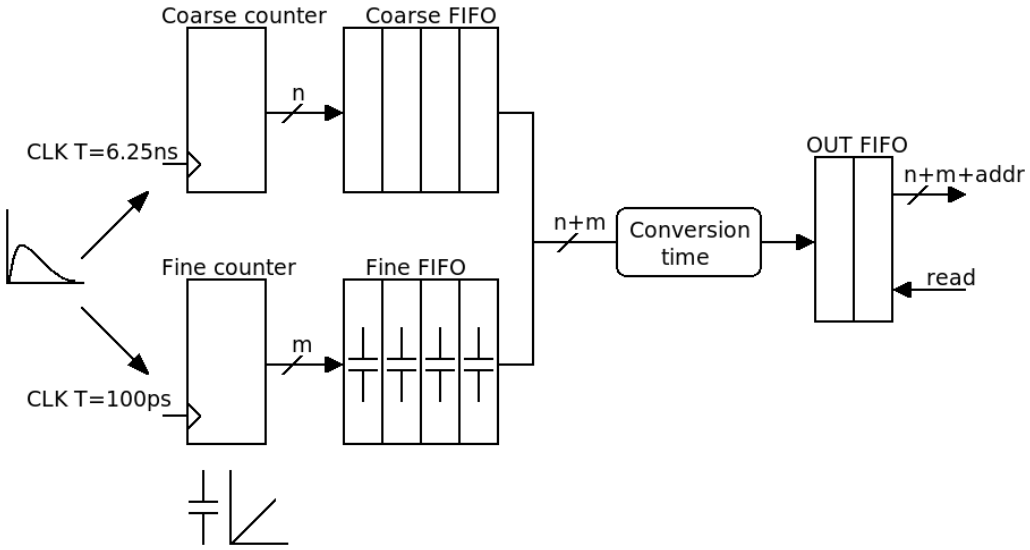


Figure 3.12: The pixel model for multi-event buffer simulations with VHDL

Hit rate (kHz)	Lost data with 3-level FIFOs (%)	Theoretical prediction of lost events with n=3 (%)
140	0.05	0.09
150	0.05	0.11
160	0.05	0.13
170	0.08	0.15
180	0.10	0.18
190	0.11	0.21
200	0.13	0.24
210	0.16	0.28
220	0.19	0.32
230	0.22	0.36
240	0.28	0.40
250	0.36	0.45

Table 3.5: VHDL simulations results and theoretical predictions for 3-level multi-buffer FIFO

Hit rate (kHz)	Lost data with 4-level FIFOs (%)	Theoretical prediction of lost events with n=4 (%)
140	0	0.004
150	0	0.005
160	0	0.007
170	0	0.008
180	0	0.010
190	0.01	0.013
200	0.01	0.015
210	0.01	0.019
220	0.01	0.022
230	0.01	0.026
240	0.01	0.031
250	0.01	0.036

Table 3.6: VHDL simulations results and theoretical predictions for 4-level multi-buffer FIFO

3.3.1.2 The P-TDC end of column logic

The architecture of the column controller is shown in Fig. 3.13. A state machine sends a *read enable* signal to all the 45 pixels in the column using a token ring mechanism. The *read enable* is passed from pixel to pixel and each cell, when this signal is active, writes out the data content and its *empty FIFO* flag in two clock cycles. Thus the whole time to read the full column is 575 ns. A *busy* signal alerts the EoC FSM if there are available data in at least one pixel. In order to avoid ambiguities in the time reconstruction, events belonging to the same turn of the coarse counter are grouped together. At this scope an 11^{th} bit counting the frames is distributed together with the time stamp. This information is used to write in two different FIFOs events belonging to data frames of type 0 or 1. Moreover each pixel sets an *old-data* flag whenever the frame changes and it still contains data from the previous one. A second state machine merges the data from the two FIFOs and puts the data frames in the right order adding an header and a trailer between consecutive frames. From VHDL simulation it has been concluded that the FIFOs depth could be safely set to 32. The maximum nominal rate is 3.3 MHz per column. To ensure more contingency, a data rate of 4.5 MHz was used in simulations. At this frequency the maximum FIFO occupancy is 20. Finally, being just at the border of the beam, the EoC, as well as the pixel logic, is SEU protected using Hamming encoding with single error correction capability.

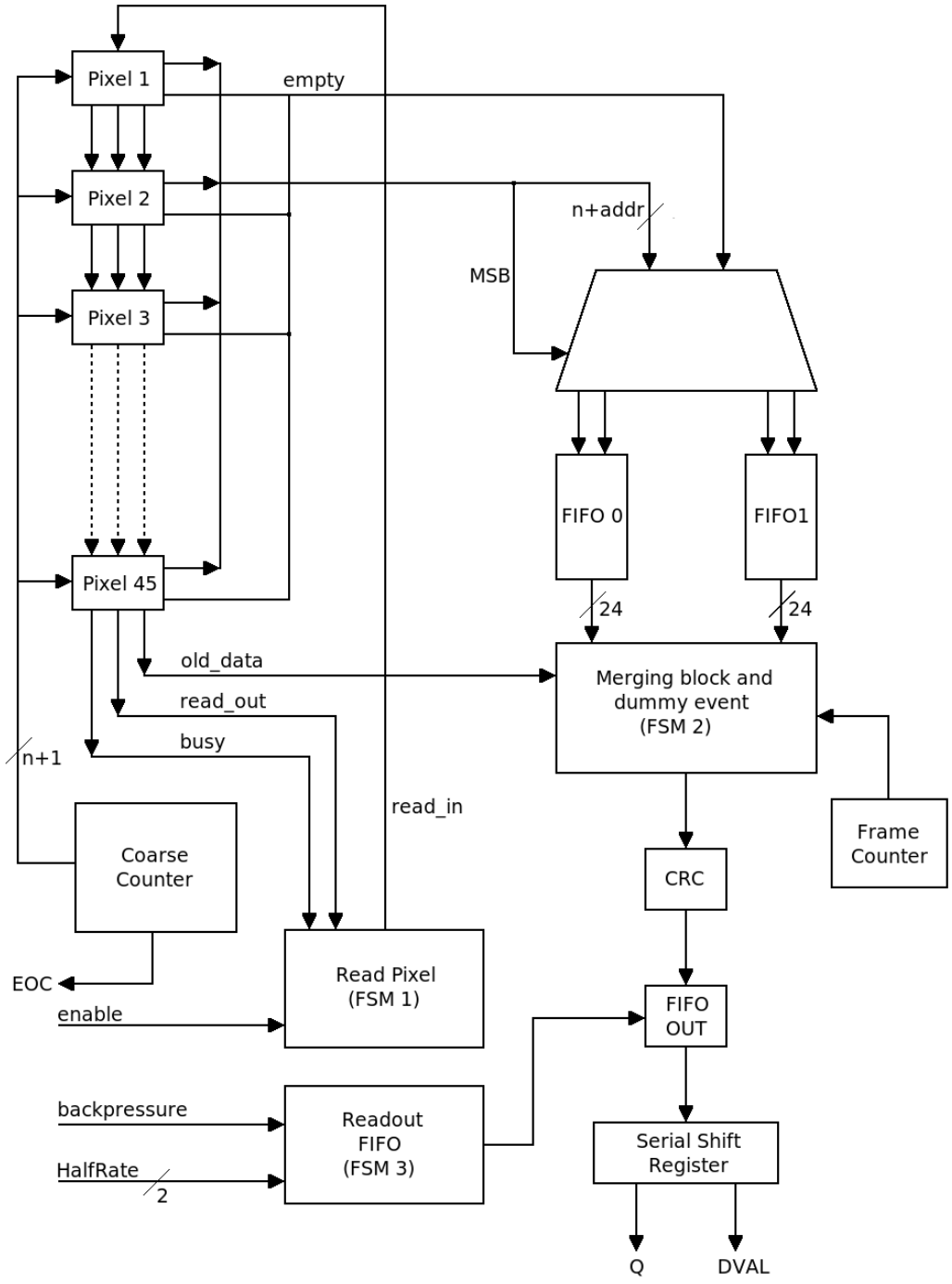


Figure 3.13: The P-TDC end of column block diagram

Chapter 4

Results from the first prototypes of the P-TDC architecture

Two prototype chips implementing precise time measurement suitable for multi-channel mixed mode ICs have already been designed and tested within the R&D of the GTK for NA62 experiment. The first prototype implementing only the analog front-end was meant to test mainly the CFD implementation chosen [66]. A second and more complex prototype aims to have an architecture as complete as possible, so that all the critical issues associated to this option could be evaluated and a future extension to a larger final ASIC could be done with a minimum risk. Therefore, all the blocks contained in the pixel cell (including the analog front-end, the DAC for the threshold setting, the full pixel logic and the EoC control logic) are implemented in their final form.

4.1 The first prototype chip for CFD testing

The first prototype chip is formed by three pixel cells (C1, C2 and C3 in Fig. 4.1), one preamplifier (B) and one CFD block (A). The signal charge is injected to the input of two pixel cells and of the preamplifier block through a calibration capacitor connected at their input. The third pixel cell and the CFD block have the input connected directly to the pads and can be stimulated externally with a shaper or a function generator. Moreover the outputs of the preamplifier and of the CFD blocks are buffered by operational amplifier in follower configuration. Finally, a 10 GHz gated digital Voltage Controlled Oscillator (VCO) [67] has been integrated on the die in order to test the robustness of the analog blocks to heavy digital noise. The VCO has a dedicated power supply in order to avoid the coupling of the noise through the power rail.

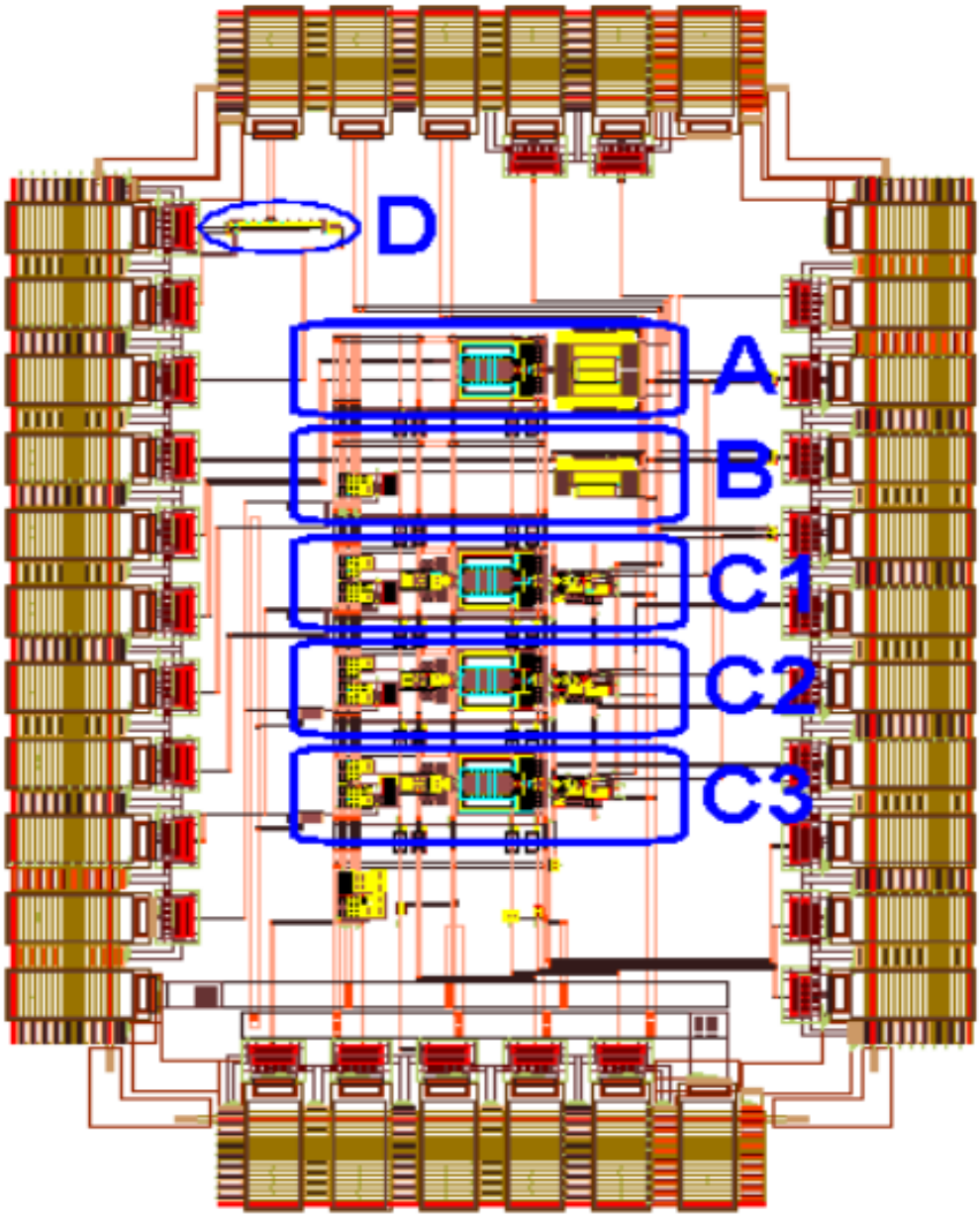


Figure 4.1: First prototype chip layout

4.1.1 The pixel cell architecture

The layout of the pixel cell, shown in Fig. 4.2, fills an area of 280 μm x 80 μm. Each cell is formed by a preamplifier, a single-ended to differential buffer, the CFD, a zero crossing discriminator with hysteresis and a digital driver (see Fig.4.3). No leakage current compensation scheme has been implemented in this prototype. The power consumption of all the building blocks is summarized in Table 4.1

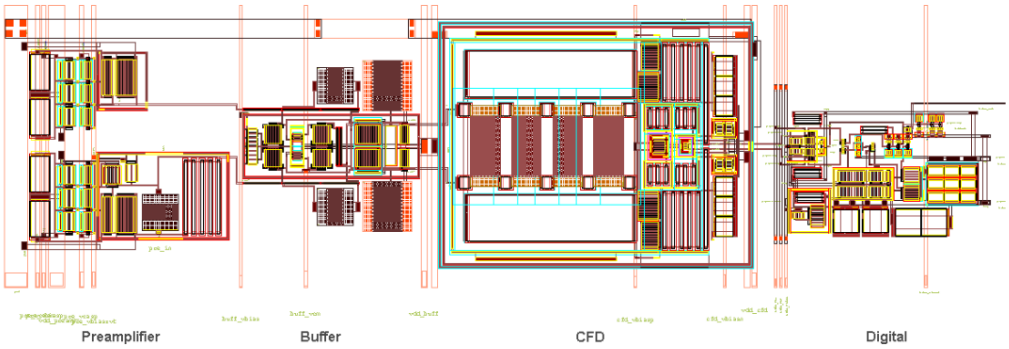


Figure 4.2: First prototype pixel cell layout

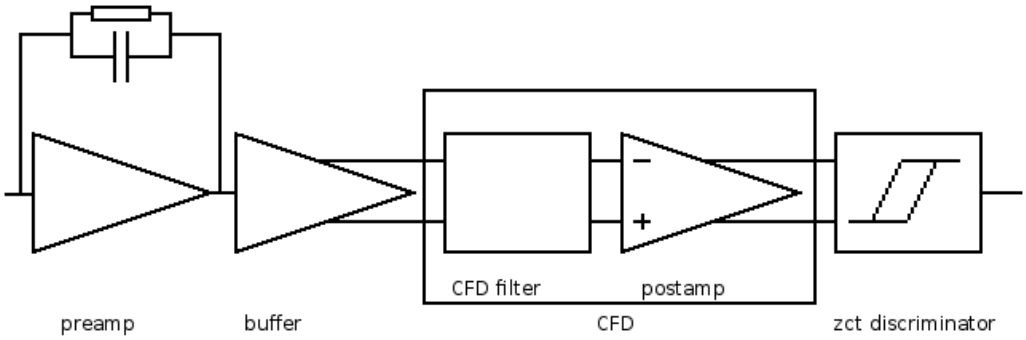


Figure 4.3: Block diagram of the pixel cell of the first prototype

Block	I_{bias} (μA)	P@V_{DD} = 1.2 V
Preamplifier	70	84
Buffer	250	300
CFD	110	132
ZC discriminator	70	84

Table 4.1: Power consumption of all the block in the pixel cell

4.1.1.1 The low noise preamplifier

The preamplifier, shown in Fig. 4.4, consists of a cascode common source (M1 and M2) with a current source load (M3 and M4) and a source follower (M7 and M8). The charge sensitive function and the signal shaping is provided by the feedback circuitry (R1 and C1).

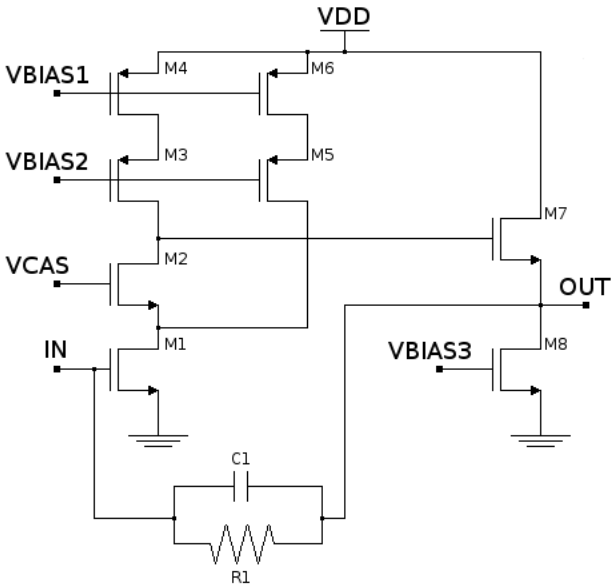


Figure 4.4: Low noise preamplifier schematic

The input referred white noise of the stage, neglecting the cascodes, is given by:

$$\overline{v_{n,in}^2} \simeq 4kT\frac{2}{3}\left(\frac{1}{g_{m1}} + \frac{g_{m4}}{g_{m1}^2} + \frac{g_{m6}}{g_{m1}^2}\right) \tag{4.1}$$

where g_{m1}, g_{m4} and g_{m6} are the transconductance of M1, M4 and M6 respectively. In an ideal front-end the main contribution to noise should come from the input transistor M1. Thus the transconductance of the current sources (g_{m4} and g_{m6}) should be minimized with respect to g_{m1}. This fact involves the use of an nMOS input transistor and of pMOS loads, since for these technologies the mobility of the electrons can be a factor 5 higher than the mobility of the holes. Moreover M1 is biased to work in weak inversion while M4 and M6 work in strong inversion. Thus the transconductance of M1, M4 and M6 can be written as:

$$g_{m1} = \frac{I_D}{nV_T} \tag{4.2}$$

$$g_{m4} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_4 I_{D4}} \tag{4.3}$$

$$g_{m6} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_6 I_{D6}} \tag{4.4}$$

Where μ_P is the hole mobility, C_{ox} is the gate capacitance per unit area, W and L are the width and the length of the transistors channels and I_D is the drain current. The thermal voltage V_T and the slope factor n are given by:

$$V_T = \frac{kT}{q} \tag{4.5}$$

$$n = 1 + \frac{C_D}{C_{ox}} \tag{4.6}$$

In the previous equations k is the Boltzmann constant, T is the temperature expressed in Kelvin, q is the electron charge and C_D is the capacitance of the depletion layer. Referring to equations 4.3 and 4.4, g_{m4} and g_{m6} are minimized using long transistors. As a drawback, increasing the L of the loads at fixed current, a higher drain-source voltage is needed to maintain the loads in saturation. For this reason the current source has been splitted into two branches and the majority of the current is provided by M5 and M6, where there are only two transistors to be maintained in saturation. Thus the presence of the current source M5 and M6 improves the noise performance by increasing g_{m1} and decreasing g_{m4} and g_{m6}. Furthermore having two current source branches allows to tune independently g_{m1} and the output resistance of the stage R_{out} giving the possibility to control the gain. For simplicity let's neglect the cascodes. In this case, calling R_{o1} and R_{o4} the output resistance of M1 and M4, the gain of the stage is given by:

$$A = g_{m1}R_{out} \tag{4.7}$$

$$= g_{m1}\frac{R_{o1}R_{o4}}{R_{o1} + R_{o4}} \tag{4.8}$$

The output resistance of the transistors are inversely proportional to the current flowing through them:

$$R_{o1} = \frac{1}{\lambda_n I_{D1}} \tag{4.9}$$

$$R_{o4} = \frac{1}{\lambda_p I_{D4}} \tag{4.10}$$

where λ_n and λ_p are constants depending on the technology. Thus the resulting gain is:

$$A = \frac{I_{D1}}{nV_T(\lambda_n I_{D1} + \lambda_p I_{D4})} \tag{4.11}$$

In this case it is possible to tune the gain just changing the current in M4 and without changing the total current I_{D1} flowing in the stage. On the other hand, if $I_{D4} = I_{D1}$ the previous equation reduces to:

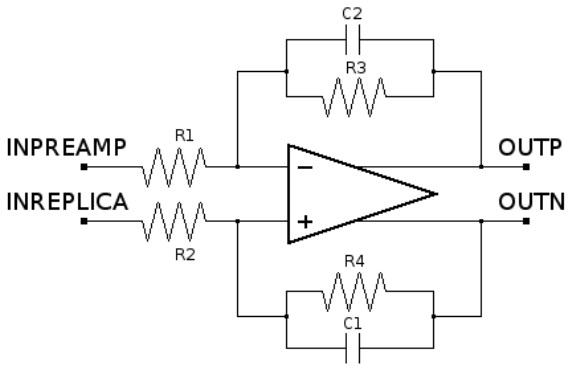
$$A = \frac{1}{nV_T(\lambda_n + \lambda_p)I_{D1}} \tag{4.12}$$

thus leaving no possibility to tune the gain without changing the value of I_{D1}, introducing a trade-off between the gain of the stage and its speed.

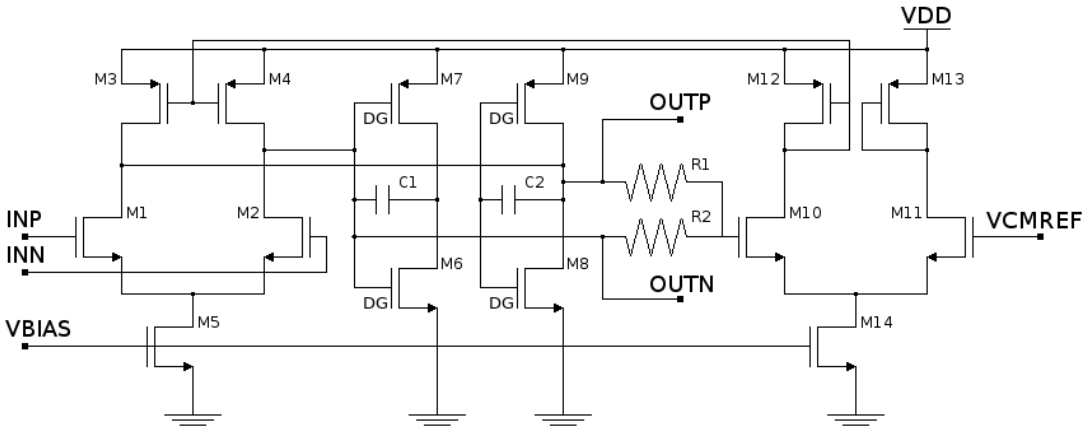
The preamplifier dissipates 70 μA, providing a gain of 40 mV/fC in 3.5 ns of peaking time, and has an ENC of 150 electrons for a 200 fF detector capacitance.

4.1.1.2 The buffer

As it will be explained later, a buffer stage with good current drive capability is needed at the output of the preamplifier to provide the dynamic current required by the CFD block. Moreover this stage also performs the single-ended to differential conversion. Referring to Fig. 4.5 A, the inputs of the buffer are connected respectively to the outputs of the preamplifier and to a replica circuit of the preamplifier, providing the correct DC bias at this node. Capacitors C1 and C2 provide nested compensation for better stability. The buffer op-amp, shown in Fig. 4.5 B, consists of a fully differential amplifier stage (M1-M5), two inverter output stages (M6-M9) and a common mode feedback circuit (M10-M14). The inverter stages use thick oxide transistors providing lower gate capacitance, and thus improving speed and compensation efficiency. Furthermore they have a higher threshold voltage than normal transistors, leading to class-AB operation of the stage. As a drawback the class-AB operation is not controlled by any additional circuit and is subject to process variations affecting both performance and power consumption.



(A)

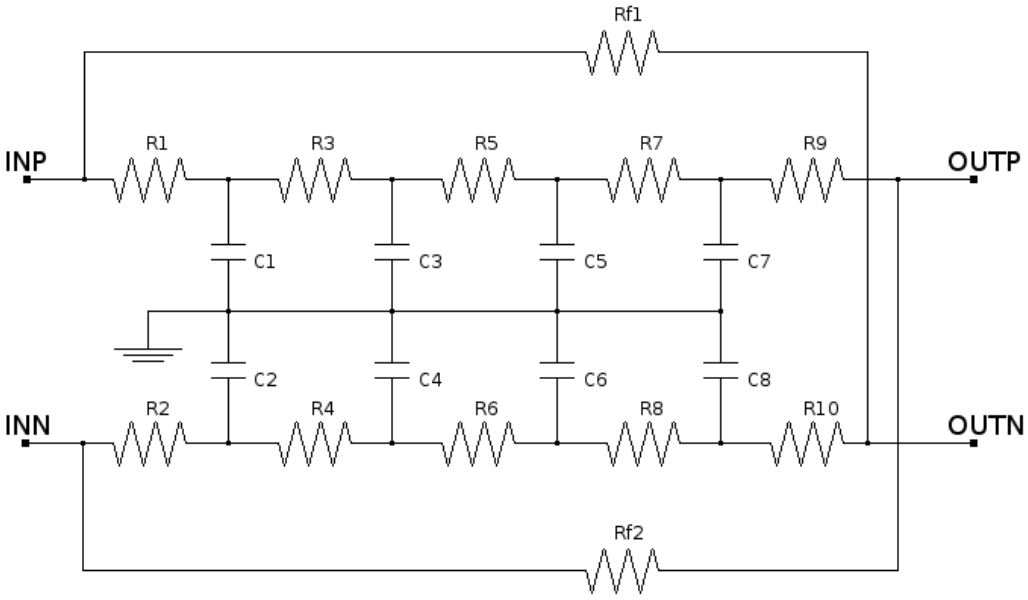


(B)

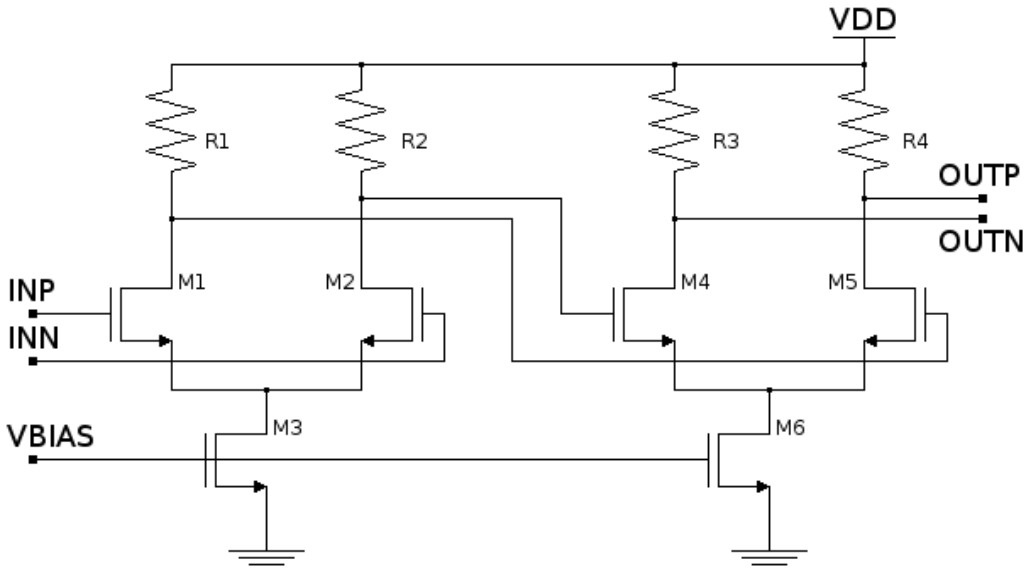
Figure 4.5: (A) Buffer single-ended to differential configuration and (B) op-amp schematic

4.1.1.3 The Constant Fraction Discriminator

The CFD filter has been implemented as a 4^{th} order RC distributed network, as shown in Fig. 4.6 A. A differential configuration has been chosen for better rejection of common mode noise. Resistors R1-R8 and capacitors C1-C8 form the distributed low pass network, while resistors R9, R10, Rf1 and Rf2 implement the fraction. Resistors and capacitors are implemented respectively using poly-silicon and nMOS-in-well structures (ncap).



(A)



(B)

Figure 4.6: (A) CFD filter (B) and zero crossing post amplifier schematics

The CFD filter is followed by a postamplifier, sketched in Fig. 4.6 B, composed

by two cascaded differential stages. Resistive loads were preferred to improve speed performance.

Finally, the CFD block includes also a current mode dynamic offset compensation circuit, as shown in Fig. 4.7. M2 and M3 are the differential pair of an amplifier, while M4 is the current source. The gates of M2 and M3 are connected to the output of the postamplifier through a low-pass filter with high time constant. The resulting output current is then injected into the resistive network of the CFD filter compensating for offsets from the front-end stages. This slow feedback provides also a high pass overall transfer function cutting the low frequency noise. The parameters

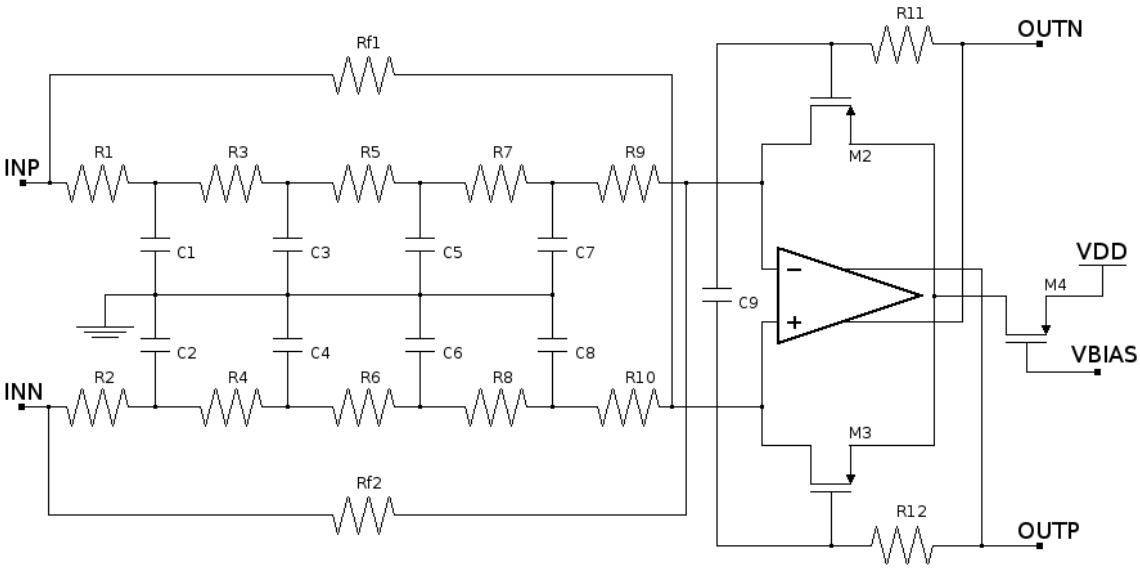


Figure 4.7: Complete schematic of the CFD block, including the dynamic offset compensation circuit

of the offset compensation circuit, such as the time constant, the gain and the tail current, have been chosen as a compromise between compensation efficiency and rate capability. A solution to obtain better compensation efficiency without worsening the rate capability would be the implementation of a reset circuit which discharges capacitor C9 in Fig. 4.7 every time that a high amplitude signal occurs. However the reset circuit circuit was not implemented in this prototype. The resistors R1-R10 were chosen small ($\simeq$ 1 kΩ), in order to limit their contribution to the noise, while the capacitors have a value of 170 fF. With these values, the dynamic current drown by the offset compensation circuit has a peak of nearly 100 μA. This current is provided by the buffer stage at the output of the preamplifier.

4.1.1.4 The zero crossing discriminator with non-symmetrical hysteresis

In traditional configurations a zero crossing discriminator is put in AND with an arming leading edge discriminator (see Fig. 4.8). In presence of noise the output of the zero crossing discriminator is continuously bouncing. For this reason it is gated by the arming discriminator which switches only when the input signal goes

over a certain threshold level. However, in a multichannel IC, the noise injected in the substrate by thousands of circuits continuously switching on noise might not be tolerable. This problem has been avoided by mean of a discriminator implement-

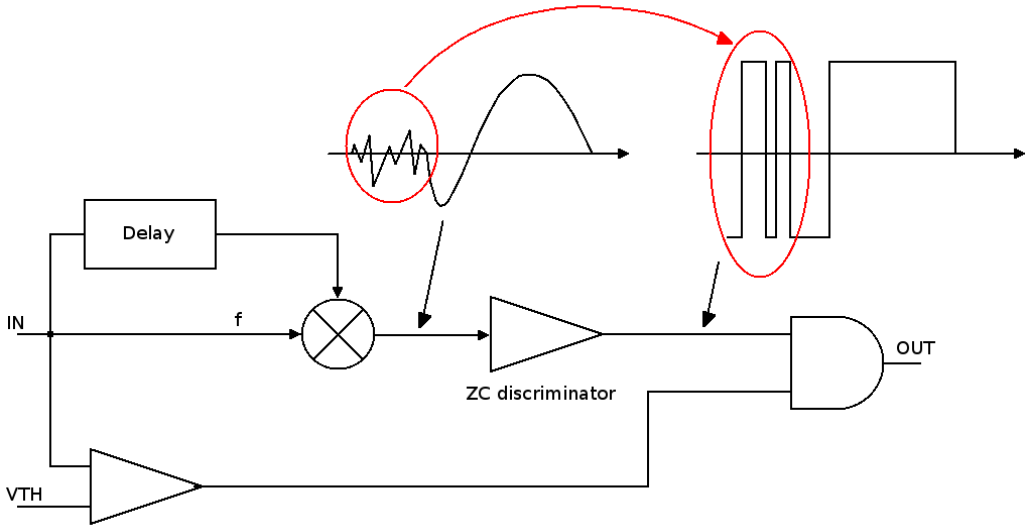
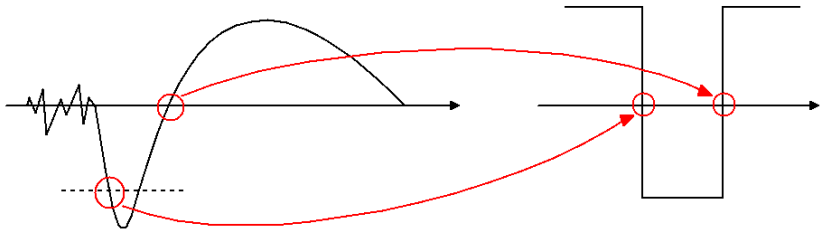
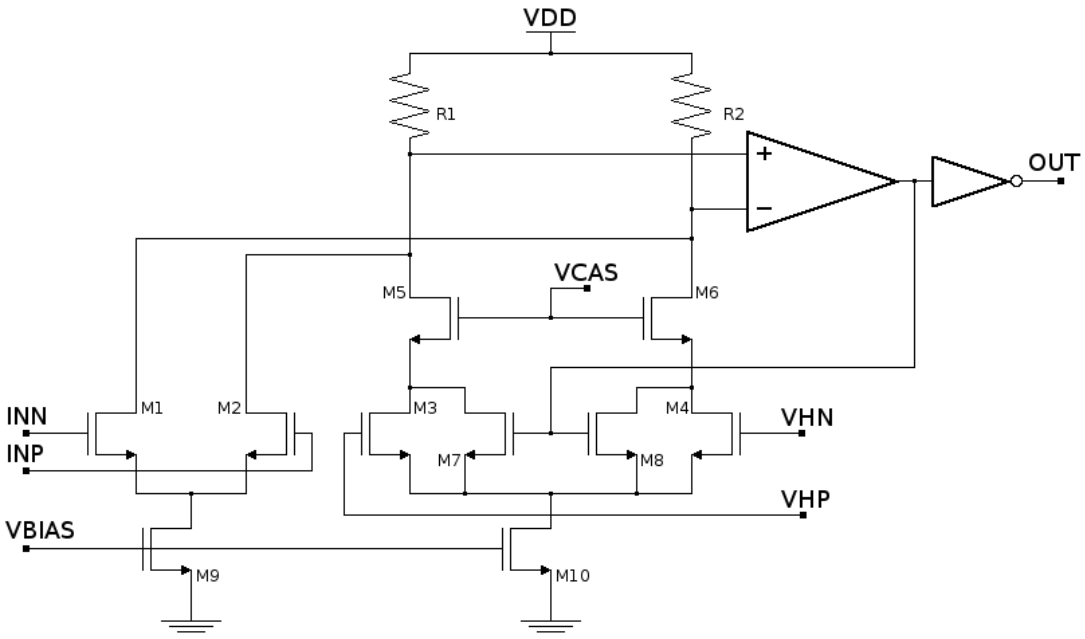


Figure 4.8: Traditional implementation of the zero crossing discrimination circuit

ing non-symmetrical hysteresis. The principle is shown in Fig. 4.9 A. A threshold level is applied at the underdrive of the bipolar signal. When the signal crosses the threshold, the latter is cancelled and the discriminator acts a zero crossing discriminator. Keeping the threshold well above noise avoids the formation of spurious switching in absence of the signal. In Fig. 4.9 B it is presented the circuital implementation of the discriminator. Two differential pairs, M1-M2 and M3-M4, sharing the same resistive load, are connected respectively to the output of the zero-crossing amplifier and to the differential threshold voltage. The switches M7 and M8 short-cut the threshold differential pair when the discriminator itself switches to the high logic state. In order to disable the threshold before the zero crossing of the bipolar signal, the circuit that controls the hysteresis must be very fast ($\sim$ 2-3 ns). As a consequence, transistors implementing this circuitry are chosen as small as possible. However small transistors are subject to a bigger mismatch resulting in a higher offset and thus in additional time walk.



(A)



(B)

Figure 4.9: (A) Non-symmetrical hysteresis principle. (B) Schematic of the zero crossing discriminator implementing the threshold hysteresis

4.1.1.5 Test results

Three prototype chips have been mounted on three different boards and tested in laboratory in order to understand the performance of the CFD implemented [68] [69]. The block diagram of each prototype chip is shown in Fig. 4.10 and described in Table 4.2. Both channels DF1 and DF2 are formed by the full front-end, but

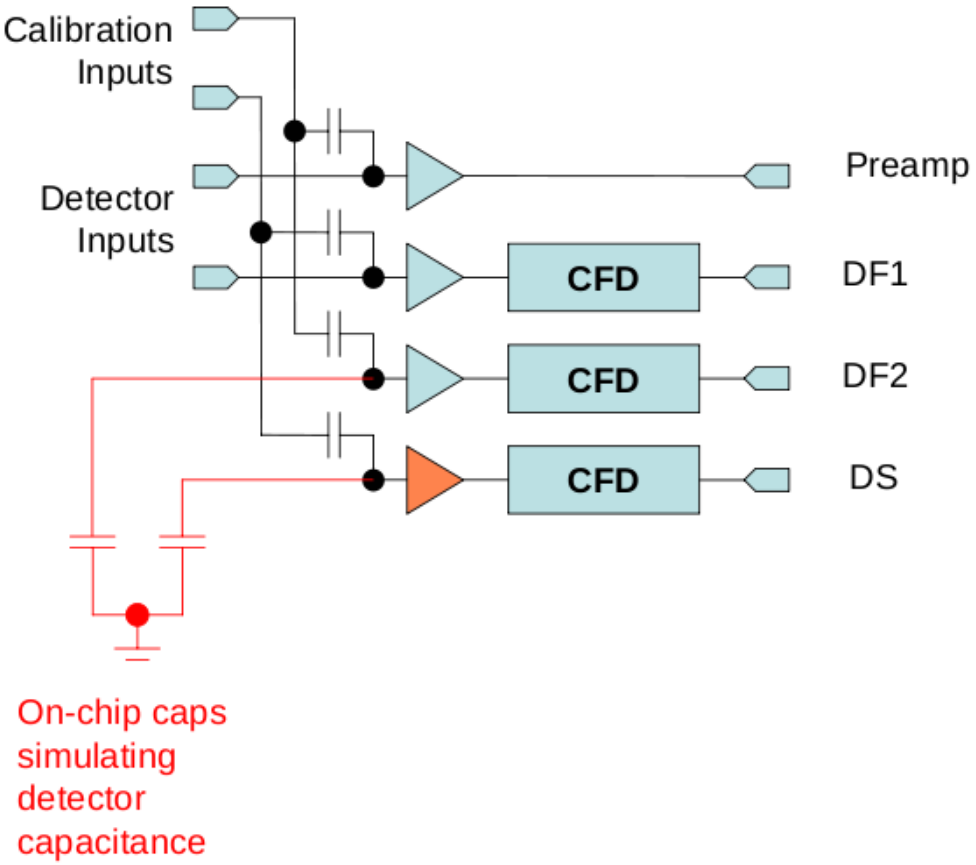


Figure 4.10: Block diagram of the prototype chip

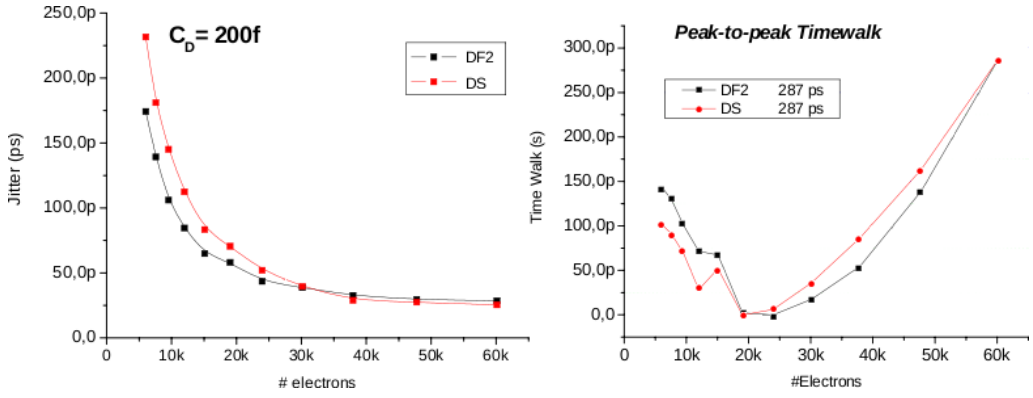
	Output type	Shaping time	Input capacitance
preamplifier	analog	3.5 ns	pad
DF1 (fast)	digital	3.5 ns	pad
DF2 (fast)	digital	3.5 ns	200 fF
DS (slow)	digital	5.5 ns	200 fF

Table 4.2: Parameters of each channel of the prototype chip

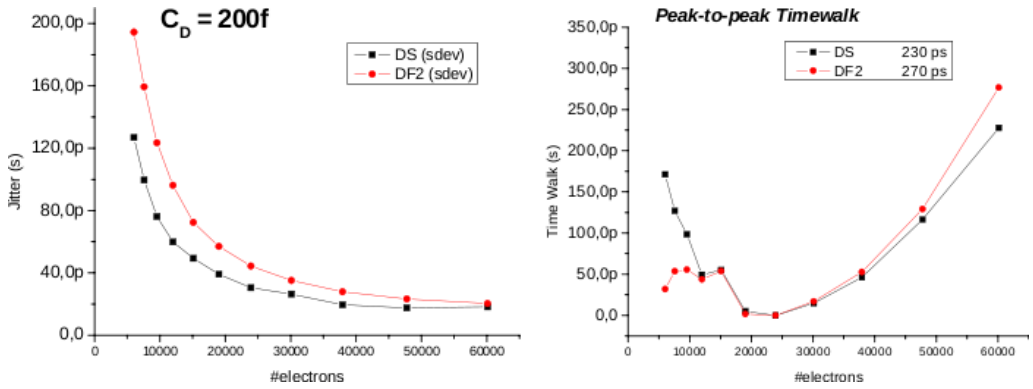
the first sees only the pad capacitance at its input, while the second has a 200 fF capacitance to simulate the detector. In both channels the preamplifier is biased with the nominal current value, leading to a 3.5 ns peaking time. Channel DS is

identical to DF2, but the preamplifier current is lower, causing a higher peaking time.

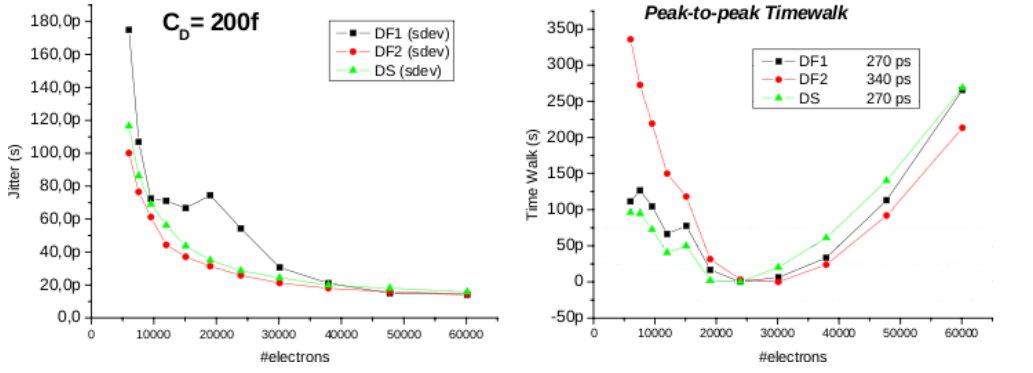
The jitter and the time walk performance has been measured for the different channels in the three boards in the dynamic range from 6 ke$^-$ to 60 ke$^-$ (corresponding to nearly 1 fC to 10 fC) and the results are shown in Fig. 4.11. The final



Board A



Board B



Board C

Figure 4.11: Jitter and time walk resulting from the electrical tests of boards A, B and C

time resolution has been estimated as the convolution of the measured time walk and jitter curves with the expected Landau of the experiment. An example is shown in fig. 4.12. The Minimum Ionizing Particle (MIP) for a 200 μm thick silicon sensor is 14 ke$^-$, corresponding to 2.4 fC [70]. A Montecarlo simulation extracts charge

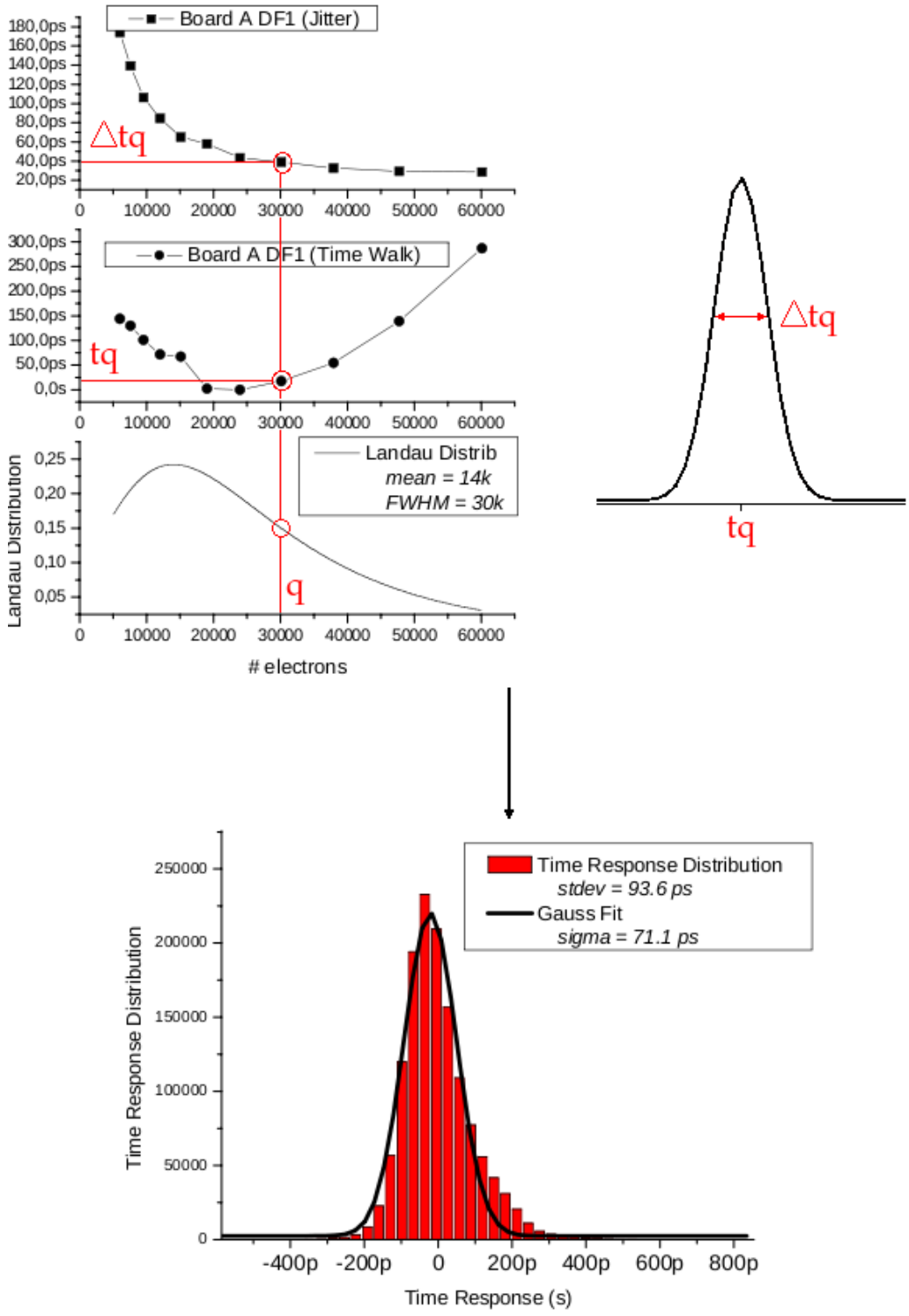


Figure 4.12: Example of the convolution of the jitter and the time walk curves with the expected Landau of the experiment centered at 1 MIP

		Jitter @14ke$^-$	Jitter @6ke$^-$	Peak-to-peak time walk (ps)	Timing error due to time walk and jitter
Board A	DF1	65	174	287	93.6
	DS	84	232	287	109.6
Board B	DF1	73	195	270	93.7
	DS	50	127	230	75.02
Board C	DF2	40	100	340	86.1
	DF1	67	175	270	103.9
	DS	45	116	116	71.03

Table 4.3: Summary of the electrical test results from the three boards

events following the Landau distribution centered at 1 MIP. Each charge value q is associated to the corresponding time value t_q from the time walk curve. Finally each time t_q is corrected adding or subtracting a certain value extracted from a gaussian jitter distribution with a standard deviation equal to Δt_q. Table 4.3 summarizes the timing performance measured for the different boards. The timing error due to time walk and jitter ranges from a minimum of 71.03 ps RMS to a maximum of 109.6 ps RMS which is well below the 200 ps specification.

4.2 The second prototype for full functionality test

In order to test all the building blocks of the P-TDC architecture and to evaluate the timing performance, a second prototype has been submitted in 2009 in 0.13 μm CMOS technology [71] [72]. The prototype, shown in Fig. 4.13, includes two columns of 45 cells, in folded configuration in order to have an acceptable form factor, and one short column of 15 cells. Two spared pixels containing only the front-end are provided for analog testing. The EoC circuit with buffers and control logic has also been implemented [72]. The clock works at the nominal frequency of 160 MHz and is distributed to the pixel matrix through clock drivers located in the EoC.

In Fig. 4.14 it is shown a picture of the chip wire bonded to the Printed Circuit Board (PCB). It has 118 pads organized as follows:

- 40 pads for the analog front-end, laid out on two rows of 20 pads each, in the left part of the chip top side
- 60 pads for the digital part, arranged on two rows of 30 pads each, in the right part of the chip top side
- 9 pads for the analog test cells located on one column on the chip left side
- 9 pads for the digital debug placed on one column on the chip right side

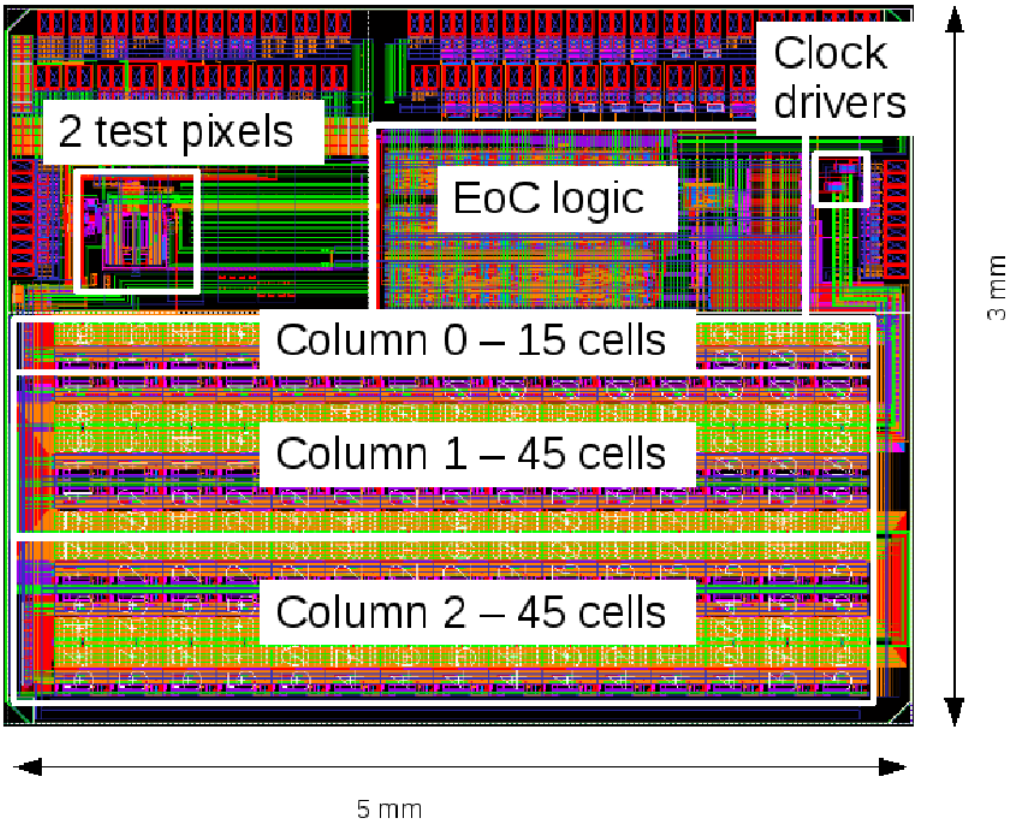


Figure 4.13: Second prototype chip layout

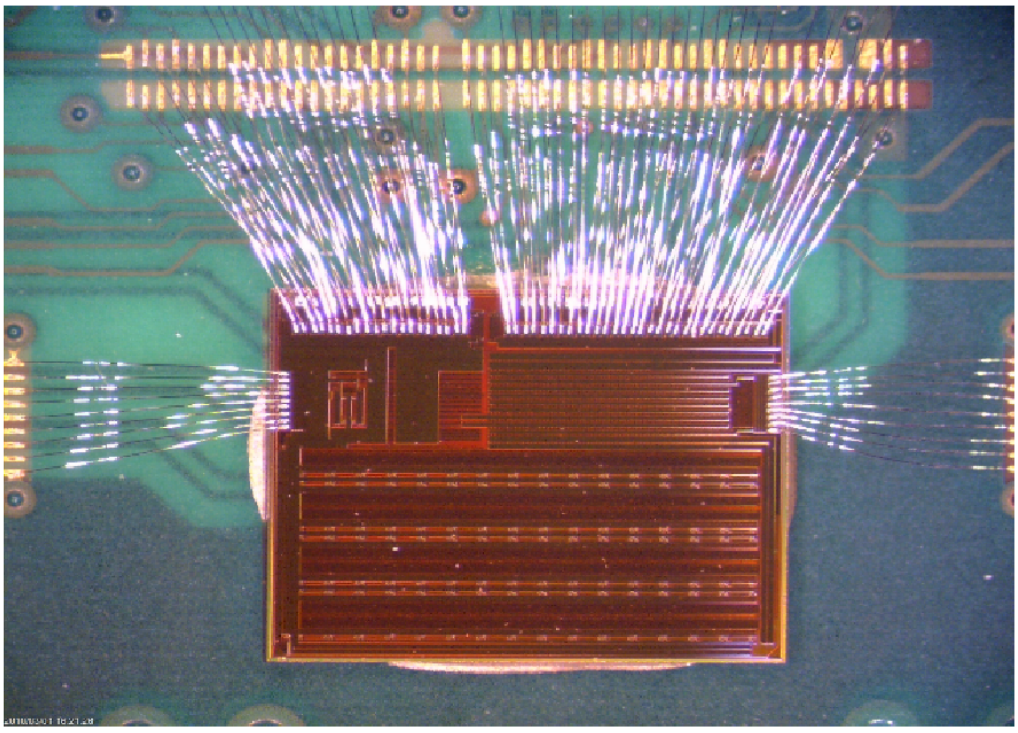


Figure 4.14: Picture of the P-TDC ASIC prototype wire bonded to the PCB

A single 10 bit coarse counter is distributed to the whole pixel matrix and can be configured both in binary and gray mode. Identical EoC controllers working in parallel perform the readout of the columns as shown in Fig. 4.15. For each single pixel it is possible to configure the discriminator threshold and the TAC discharge current. Furthermore the pixel can be configured to work in test mode or masked.

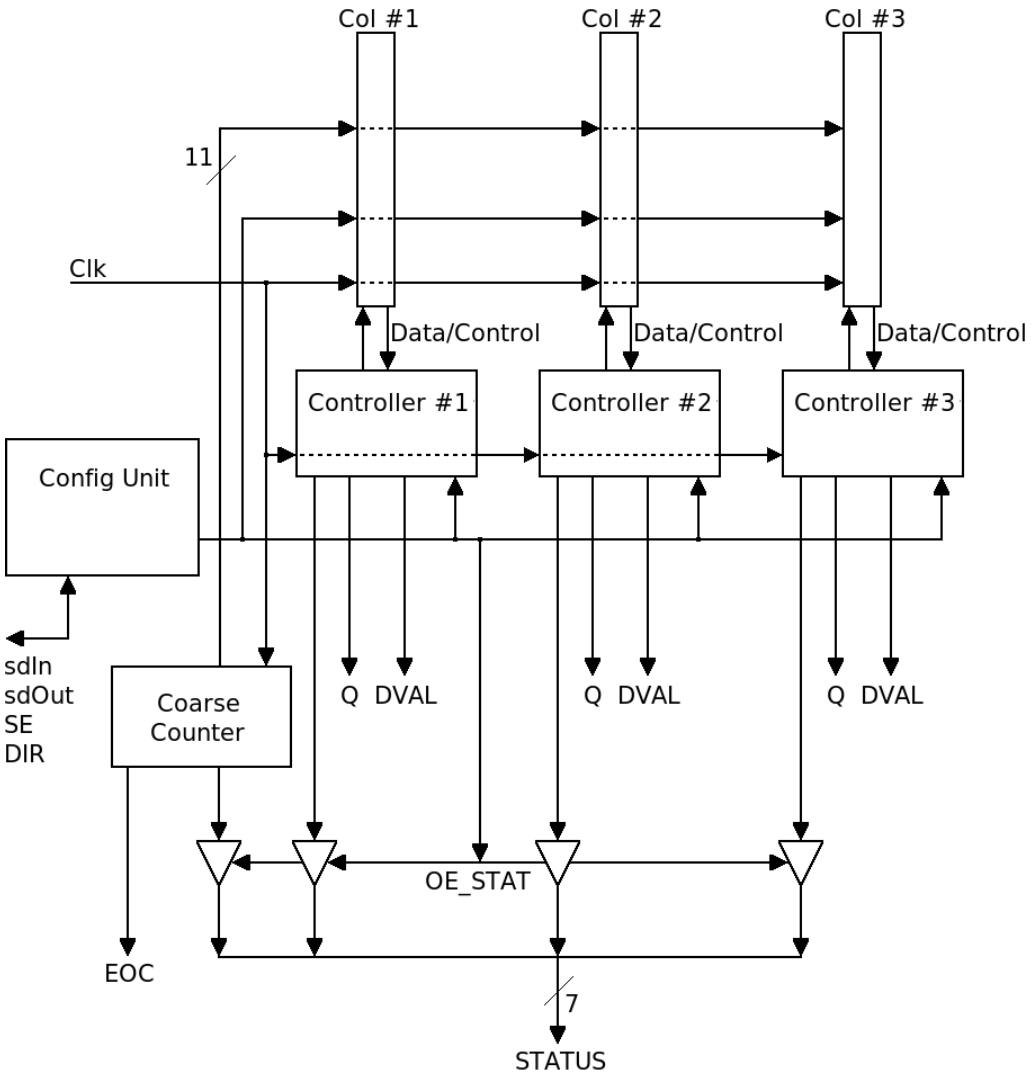


Figure 4.15: P-TDC demonstrator ASIC block diagram

4.2.1 The P-TDC demonstrator: the pixel analog section

The architecture of the pixel cell has already been discussed in the previous section (see Fig. 3.7). Each cell contains an analog and a digital section, as shown in Fig. 4.16. The analog front end is formed by a preamplifier, followed by the CFD and by the TAC based TDC. The implementation of each block is presented in the following sections.

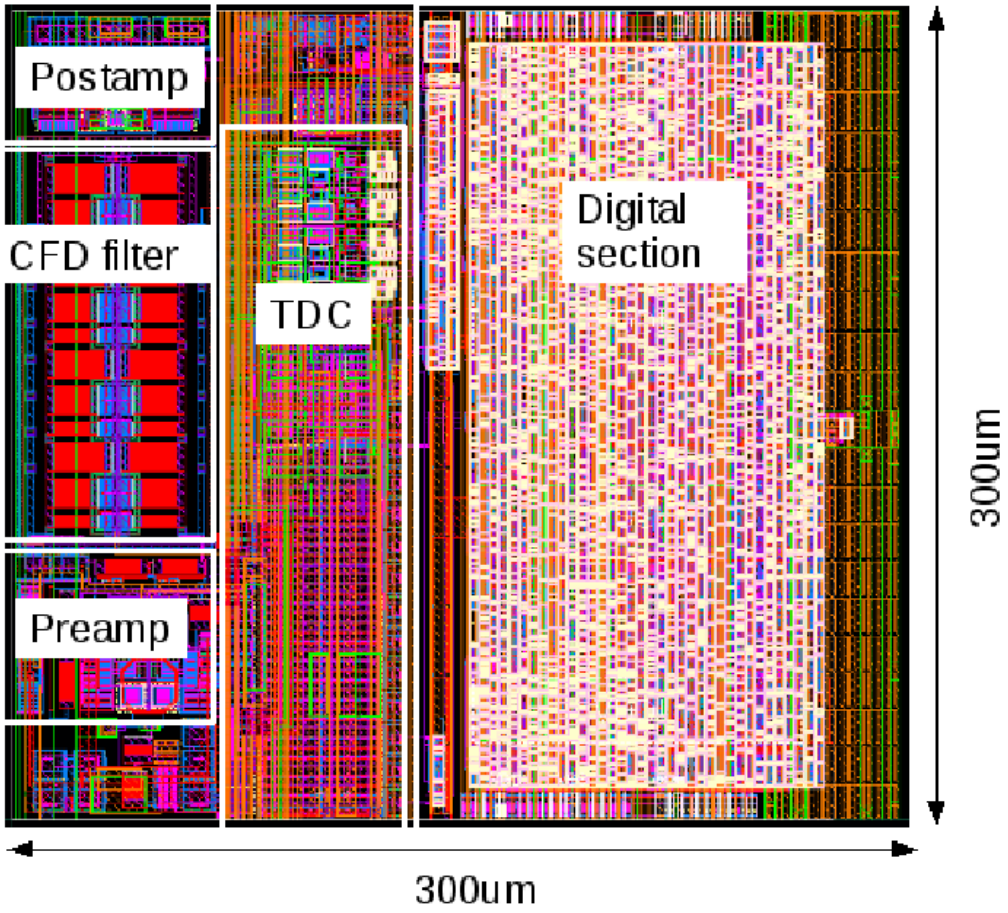


Figure 4.16: Second prototype pixel cell layout

4.2.1.1 The preamplifier

The front-end preamplifier is a fully differential amplifier with common mode feedback (Fig. 4.17) and class AB output stage (Fig. 4.18). It is common practice, in many front-ends for silicon detectors to optimize the input stage for the type of detector used, depending on wether it collects electrons or holes on the input plate. However in this way the circuit is suitable only for that kind of detector. Due to the very expansive process of fabrication it is important to have a flexible circuit. In the case of the GTK the use of a front-end optimized for both polarities is further motivated by the fact that the n-in-p sensors are more radiation hard than the p-in-n types. At the present time it has been forseen to use p-in-n sensors, due to costs

reasons, but in a future upgrade it could be convenient to use a n-in-p sensor. For these reasons the front-end amplifier has been designed to be compliant with signals of both polarities. In the first stage the differential pair M1-M2 is cascoded by transistors M3-M4. Fixed current sources I2 and I3 absorb current from the cascode transistors optimizing the noise. The load transistors M5 and M6 are piloted by the common mode feedback amplifier M9-M12. In the latter stage, cascodes have been

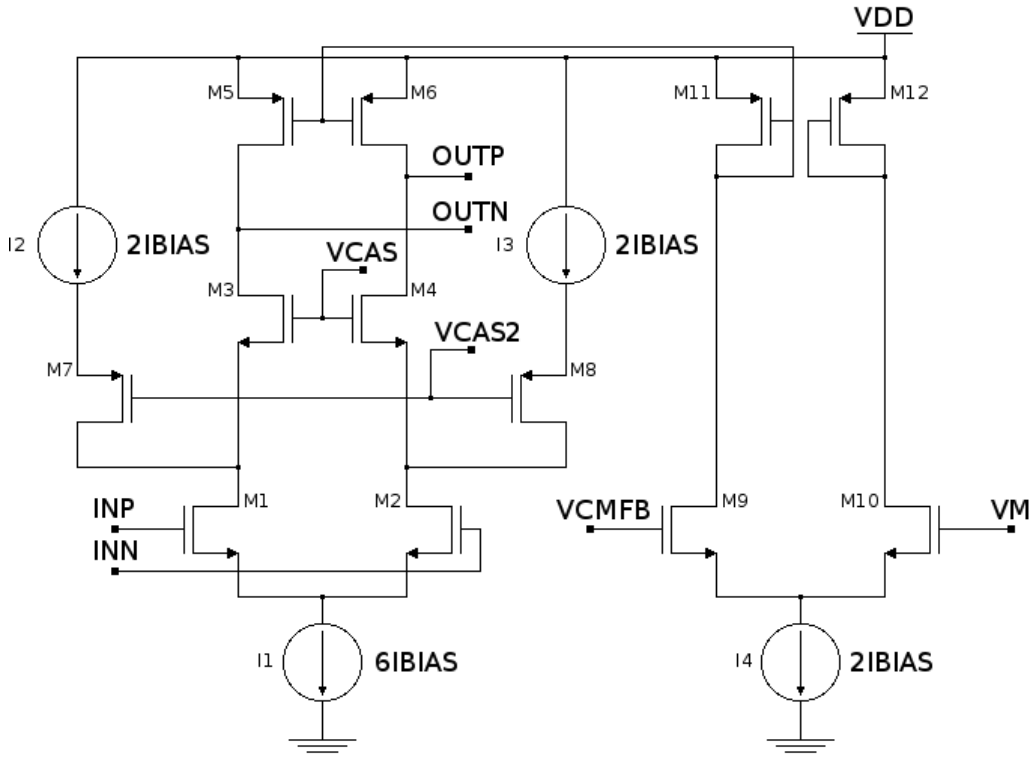


Figure 4.17: First stage of the preamplifier

omitted, since a higher gain of the stage would lead to instability. The preamplifier has a nominal peaking time of 3.5 ns, a gain of 80 mV/fC and is designed to be linear up to 10fC.

The feedback circuit, shown in Fig. 4.19, will try to compensate for common mode mismatch, due for example to leakage current, by creating a differential offset at the output of the preamplifier. It consists of two low pass filters formed by resistors R5-R6 and capacitors C3-C4. Resistors R5 and R6 are long pFET transistors connected as diode with an effective resistance of the order of the GΩ and C3 and C4 are ncap capacitor. In absence of common mode mismatch no currend flows through R1 and R2. With mismatch and in absence of leakage current from the detector, this current is provided by the leakage compensation opamp to resistor R2. This, in turn, calls for a differential offset at the output of the preamplifier. The following stages should be able to fully compensate this second-order differential offset. The leakage compensation circuit is connected to the mid point of the feedback network (R1-R2, C1-C2) as a compromise between compensation efficiency and noise.

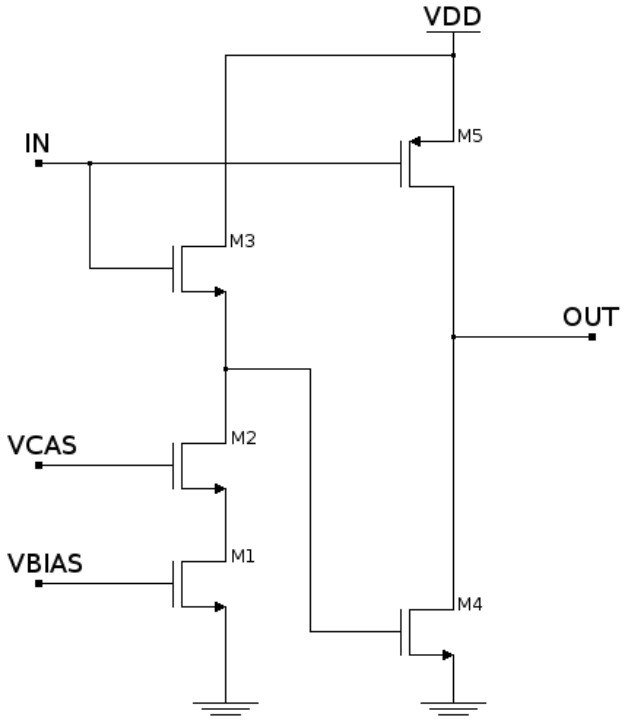


Figure 4.18: Simplified schematic of the class AB output stage of the preamplifier

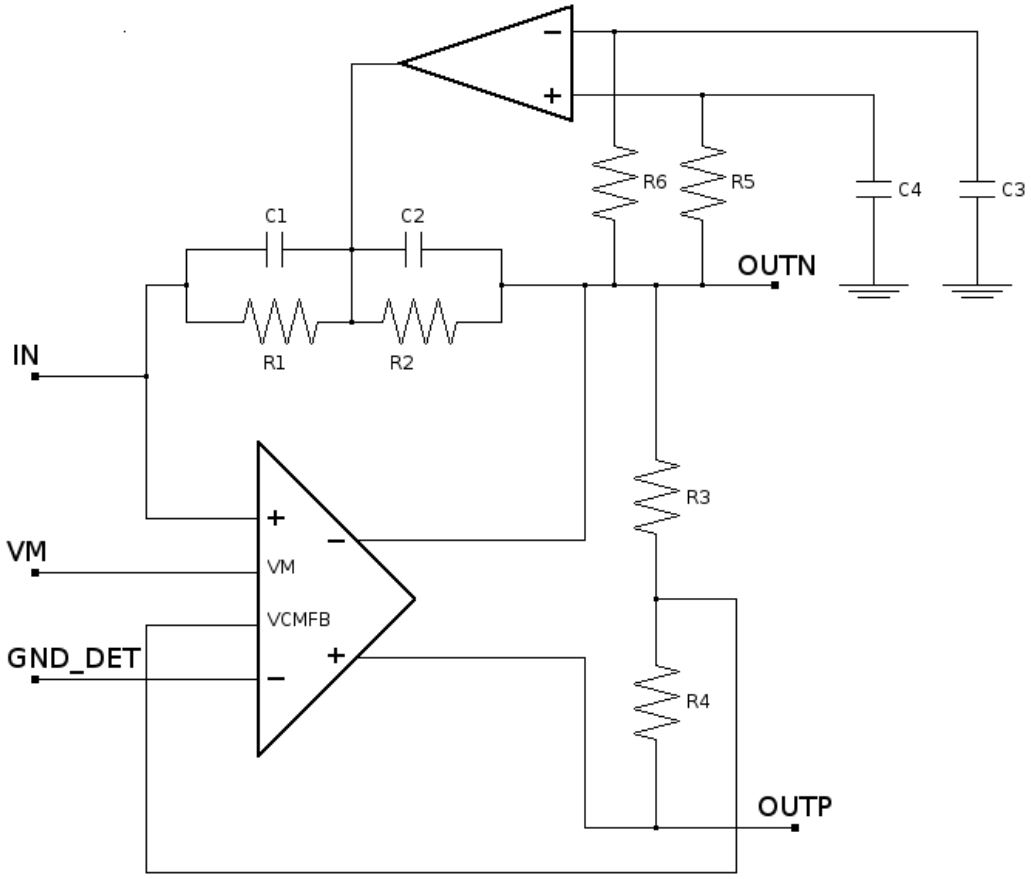


Figure 4.19: Schematic of the preamplifier with the leakage compensation circuit

4.2.1.2 The CFD

The discriminator can be separated in four stages. The first stage is the CFD filter which generates the bipolar signal. It is followed by the postamplifier which amplifies the signal to near rail-to-rail level. The third stage applies the threshold and detects the zero crossing and, finally, the last stage is a differential to CMOS level translator. In order to reduce the effect of noise injection, the analog and digital grounds are separated inside the chip. The first two stages are on the same analog ground with the preamplifier, while the last two stages use the digital ground together with the TAC and TDC blocks.

The CFD filter topology is the same implemented in the first prototype. However, it has been improved by making the delay and the fraction programmable, as sketched in Fig. 4.20. The values of the resistors and capacitors are reported in Table 4.4. From the point of view of jitter minimization, the zero crossing

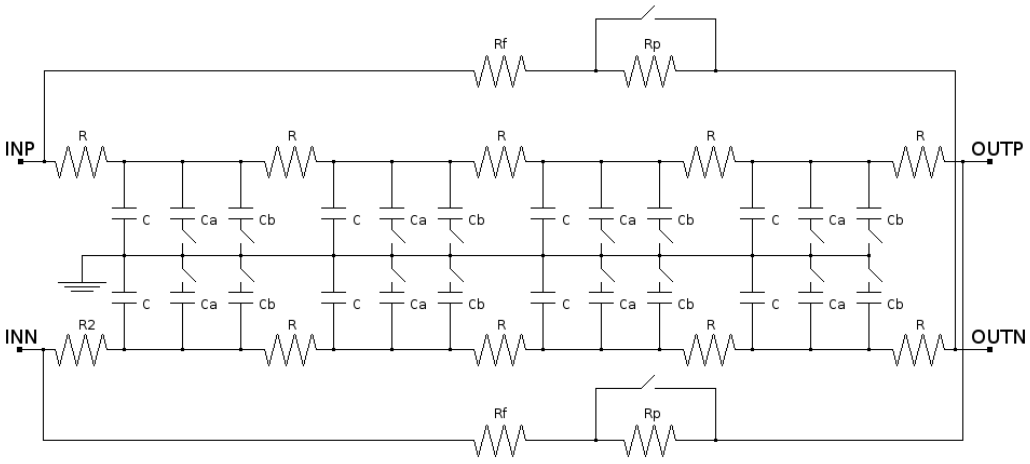


Figure 4.20: Schematic of the programmable CFD filter

Component	value
R	994.38 Ω
R_f	6R
R_p	R
C	104 fF
C_a	33.2 fF
C_b	74.9 fF

Table 4.4: Values of the passive components of the CFD filter

should occur at the point of maximum slope. This requirement is satisfied by using a 50% fraction. However, the higher is the fraction, the bigger is the underdrive of the bipolar signal on which the discriminator triggers. Statistical fluctuations of

the signal generation process in the sensor may result in the variation of the signal shape, leading to an additional walk error. To minimize this effect it is necessary to reduce the amplitude of the underdrive, thus the fraction at which the zero crossing occurs. For this reason the fraction can be programmed to be either 50% or 30% of the preamplifier signal. Moreover, to face the effects of the ASIC process variations, the delay too is made programmable by a two bit configuration. Depending on the process corner it is possible to connect or not additional capacitors in the RC line.

The second discriminator stage (Fig. 4.21) contains two cascaded fast differential amplifiers with resistive loads and the dynamic offset compensation loop. In order to optimize slew-rate, the transistors of the second differential stage are smaller than those of the first one. This stage functionality, together with the dynamic offset compensation circuit principle of work, have already been described in the previous section when describing the first prototype. C1 is a linear metal-to-metal capacitor (MIM-cap). In the first prototype, where MIM-caps were not available and two ncap capacitors were used. The presence of the offset compensation loop creates a

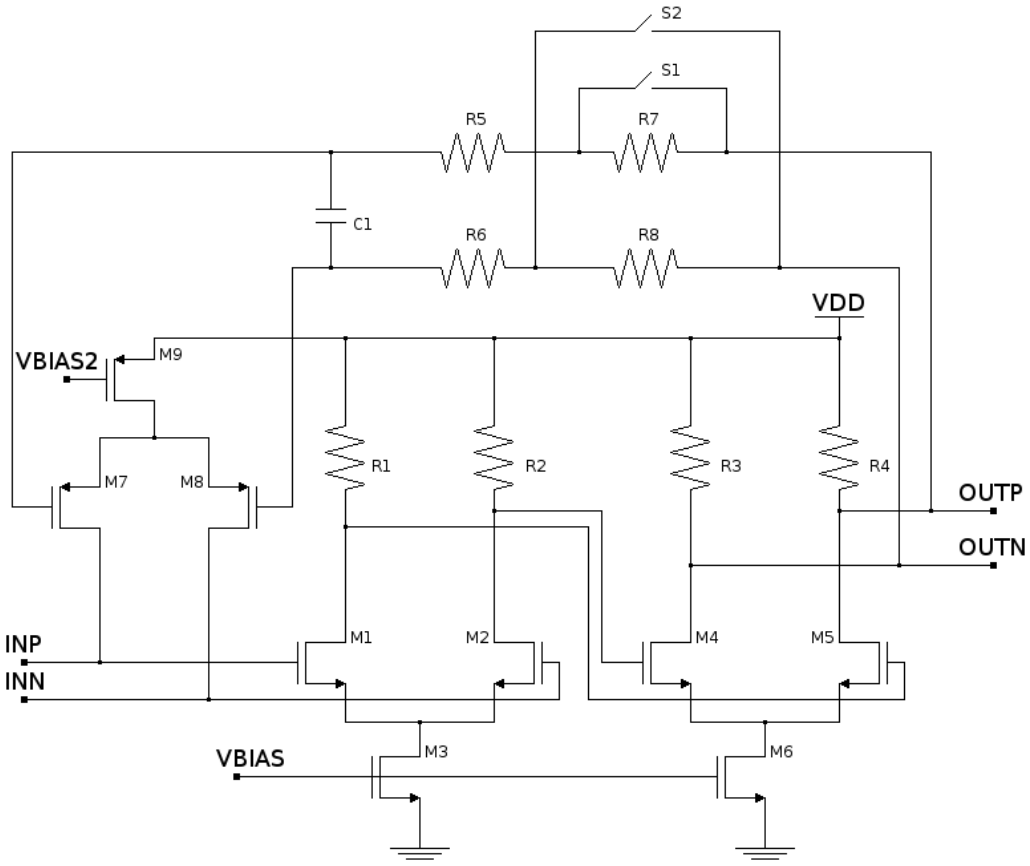


Figure 4.21: Post amplifier stage with the dynamic offset compensation circuit. For high amplitude signals it has been forseen a reset in order to prevent a big dead time

second zero crossing of the bipolar signal and a long tail, increasing the dead time. For high amplitude signals, this second pulse may cross the threshold and cause a second long digital pulse at the output of the discriminator. In order to avoid this,

a reset circuit, which was not implemented in the first prototype, has been included. The switches S1 and S2 in parallel to R7 and R8 are meant to reduce the time constant of the low pass filter. By closing them after each pulse, the system regains equilibrium faster. The switches are controlled by the *deadtime* signal issued by the TAC Control circuit.

The third stage of the discriminator employes the threshold hysteresis configuration presented in the first prototype section (see Fig. 4.9) to perform the zero crossing discrimination. A 3 bit DAC has been included in the circuit to equalize the thresholds of all the discriminators in the matrix.

A scheme of the last stage of the discriminator is sketched in Fig. 4.22. It is a differential to single-ended converter. It is formed by a single stage OTA (M1-M5) followed by a transconductance inverter (M6-M7). Feedback resistor R1 transforms M6-M7 inverter into a transconductance amplifier. This reduces the swing at the drain of M2 and M4, maximizing the speed. The stage is completed by a biasing loop that ensures the matching of equilibrium point of the OTA and the one of the inverter. Transistors M10-M12 form a half replica of the OTA and M13-M14 are identical to inverters M6-M7 and M8-M9. The error amplifier feedback controls the bias currents of M5 and M12 until mid point of the inverter and the gate voltage of M11 are equal.

At the output of this stage there is a polarity selector, not shown in figure. Based on the polarity configuration, the output is inverted or not.

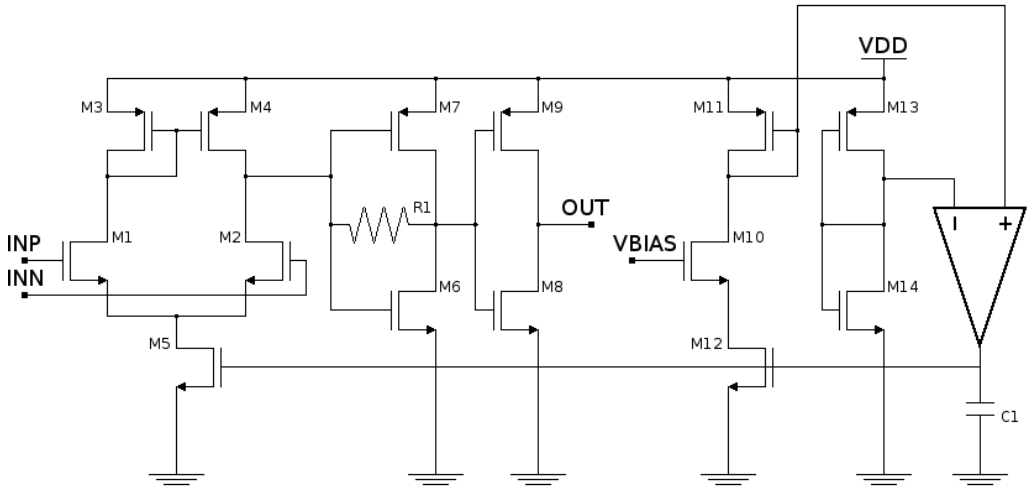


Figure 4.22: Last discriminator stage

4.2.1.3 The TAC based TDC

The circuit used to generate the voltage ramp for the TDC is shown in Fig. 4.23 It is formed by a cascoded common source amplifier and by a MIM capacitor C1. Switches S2-S4 select from reset and normal running mode, as follows:

- Reset: S3, S4 closed and S2 open

- Normal: S2 closed and S3, S4 open

The principle of operation of the two modes can be better understood from Fig. 4.23 B. In reset mode, the amplifier is short-cut and the output terminal of the capacitor is connected to the reference voltage. The voltage charged on the capacitor is $V_{ref} - V_{gs1}$. In normal operation mode, the capacitor acts as a battery pulling the output of the buffer to V_{ref}, since V_{gs1} remains constant. Two non-overlapping control signals are generated in order to switch between the two modes, such as to avoid accidental discharge of C1 through S4 and S3.

When a signal arrives, the CFD triggers the closing of S5 for all the duration of the signal. During the TAC time window, a constant current is injected into the input node (see Fig. 4.24). Thus the voltage at the output node drops linearly until the end of the time window, after the settling time of the amplifier. The resulting voltage value reached by the ramp is then stored until it is readout by the TDC. Four TAC buffer are located in each pixel providing the analog multi-buffering capability.

The TDC is composed by a current mirror, the four TAC buffers, a capacitor four times as big as the TAC capacitor and a synchronous comparator (see Fig. 4.24). M3-M5 branch of the current mirror is used to charge the TAC capacitors through one of the S2-S5 switches. In idle mode, S1 is closed so the current is diverted to ground. In a second phase, the charge stored in one of the TAC buffers is sampled on the TDC capacitor C1 through switch S10. It should be noted that, since the output voltage of the TAC will be less than V_{ref}, the sampling will actually discharge C1. Thus a current source (M1-M2) of the same polarity of the one that generates the fast voltage ramp is needed to charge C1 again and restore the baseline. After the TAC voltage has been completely copied on C1, S10 is disconnected and the charge current is switched from ground to the capacitor C1 by opening S13 and closing S12. C1 charges back to the reference level and the instant when it crosses that level is sensed by the synchronous comparator. Switch S11 is used in reset mode to charge C1 to the reference voltage V_{ref}.

The required time bin of the TDC is 100 ps covering a dynamic range of three clock cycles (corresponding to 18.75 ns working with a 160 MHz clock). It is equivalent of having a resolution of 8 bits over a range of 25 ns (four clock cycles). In fact, as already discussed in the previous chapter, the TDC has been designed in such a way that the ramp can last from one to three clock cycles even if the TDC can cover a range of 4 clock cycles. Thus, in an ideal case, the TDC uses only 7 bits and the permitted output values are only 128, ranged between 64 and 192 (thus the maximum conversion time is equal to 192 clock cycles, meaning 1.2 μs). This solution has been adopted in order to ensure to the ramp a settling time of at least one clock cycle and an offset of another clock cycle to guarantee that the capacitor C1 is completely charged back to the reference value before the ramp is stopped.

To achieve the 100 ps time resolution just by scaling the currents, a mirroring factor of 64 would be required. Using a sampling TDC capacitor four times bigger than the TAC storage one is equivalent to a four fold charge amplification, reducing by the same amount the ratio between currents. Therefore the ratio necessary between the two currents is 16 [73]. Finally the charge branch of the current mirror contains only 2 cascoded transistors. Since the output node of the branch is a slow-mover, a low-power error amplifier can be used to keep the drain of M2 at constant

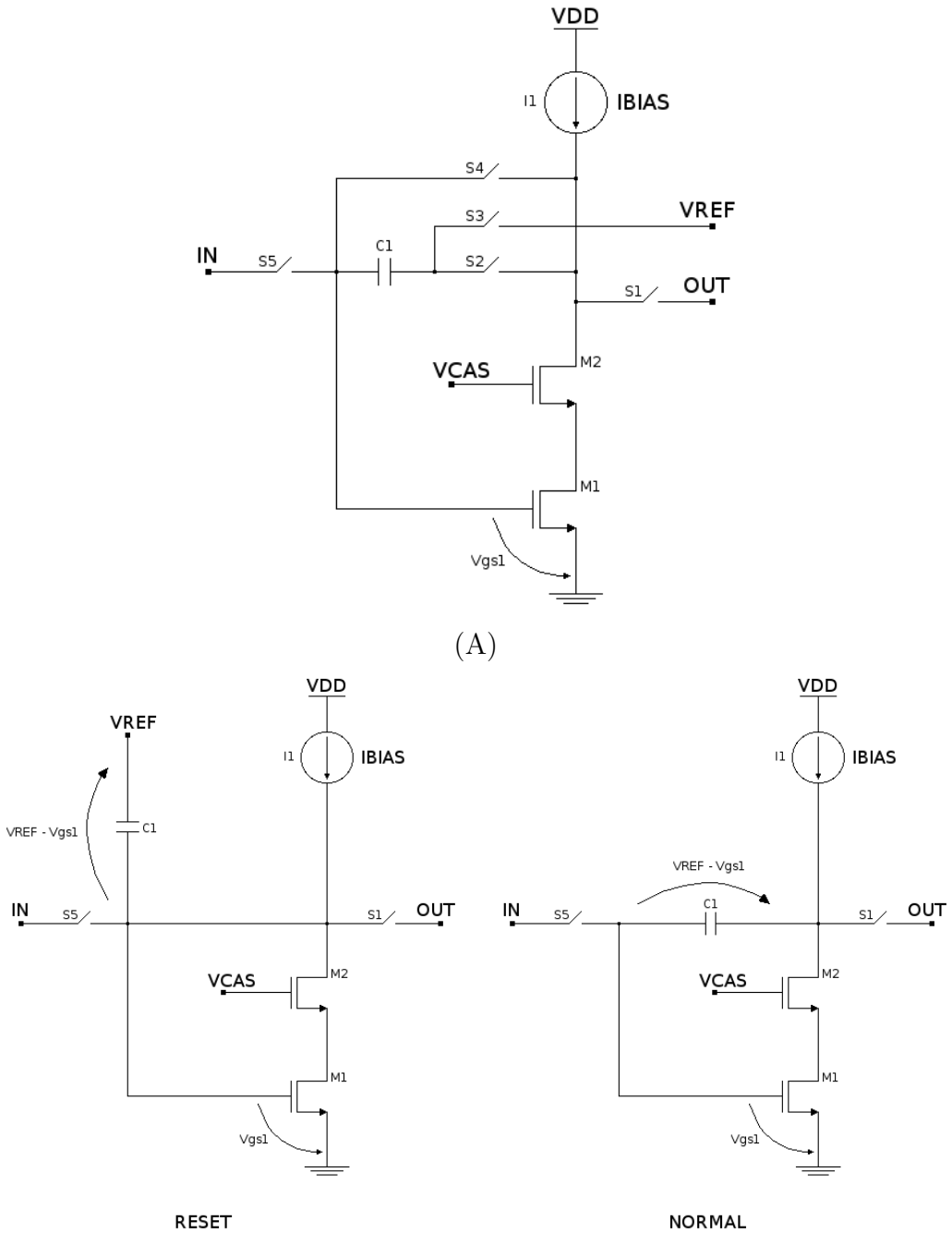


Figure 4.23: (A) Schematic of the TAC buffer and (B) principle of operation in reset and normal mode

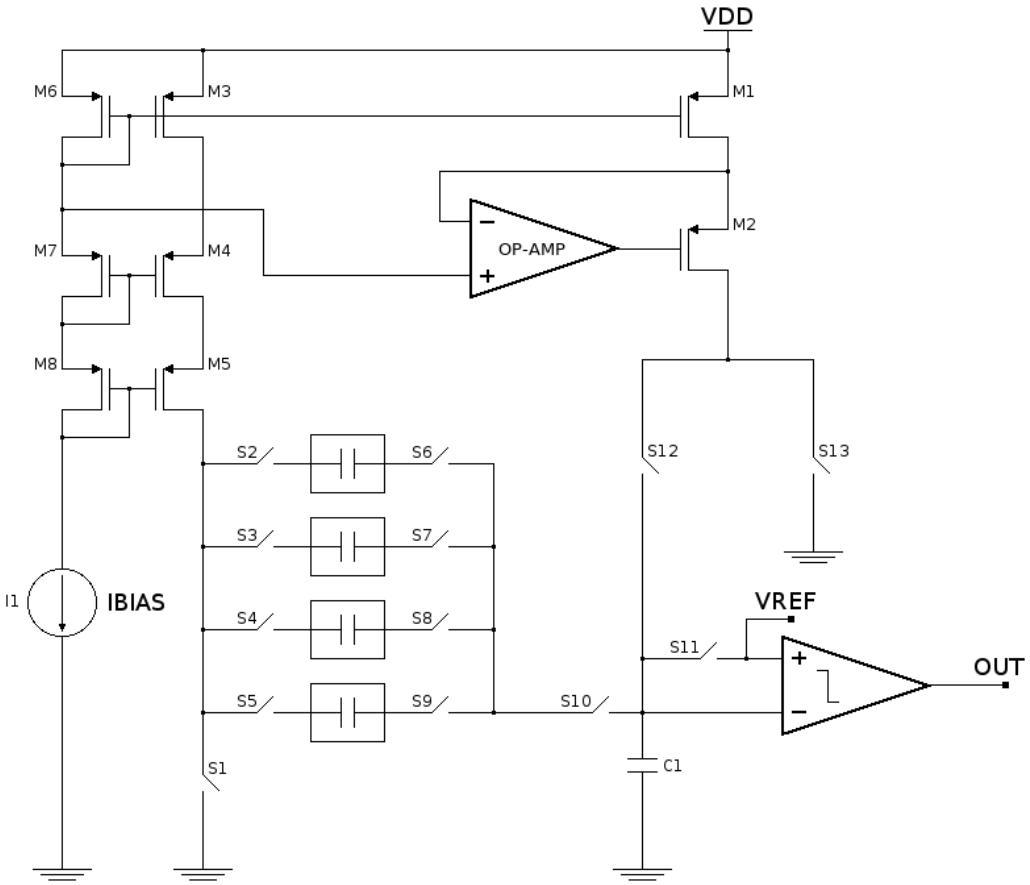


Figure 4.24: TAC based TDC block diagram

level, thus keeping the current constant.

The TAC and TDC control circuits work at half clock frequency. When a signal arrives, the TAC ramp is started and it is stopped at the first rising edge of the half clock, following a falling edge. The circuit then waits for one or three clock cycles and is automatically reseted for another clock cycle. The time window between the end of the ramp and the reset phase of the circuit is selectable via a global configuration pin *deadtime*. This means that the artificial dead time of the circuit is given by:

$$t_{dead} = TW + (n + 1)2T_{ck} \tag{4.13}$$

where TW is the ramp time window, lasting from one to three clock cycles. n is 1 or 3, depending of the *deadtime* configuration bit and T_{ck} is the master clock period. This implies a minimum dead time of $5T_{ck} = 31.25$ ns up to a maximum of $11T_{ck} = 68.75$ ns. The circuit issues an output signal which is asserted from the beginning of the ramp to the beginning of the auto-reset phase. The signal feeds the *pixel_out* output signal, that goes to the digital section of the pixel, and the feedback output signal that controls the time constant of the dynamic offset compensation circuit of the CFD. The two signals are separated due to layout reasons.

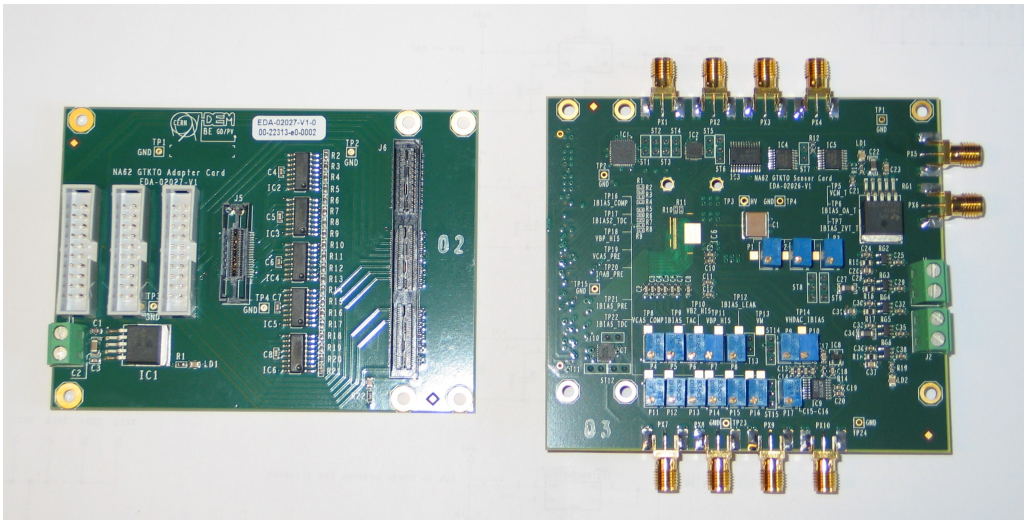
Finally, the TDC can be tested independently from the CFD section, by using the two global configuration pins, as reported in Table 4.5. In running mode the TDC input is feeded directly from the output of the discriminator and the TDC is tested through the whole front-end. In test mode the linearity of the TDC can be evaluated separately from the other blocks by sending calibrated *Test Pulses* directly at its input. Finally it is possible to measure for each pixel in the matrix the minimum and maximum ramp duration configuring the TDC in calibration mode and sending synchronous signals to its input. In this mode it is possible to equalize and calibrate the TDCs pixel by pixel by means of a 3 bit DAC which adjust the mirroring factors between the charge and discharge currents in the TDC.

TDC configuration	
00	Running mode
01	Calibration mode ($1T_{ck}$)
01	Calibration mode ($3T_{ck}$)
11	Test mode

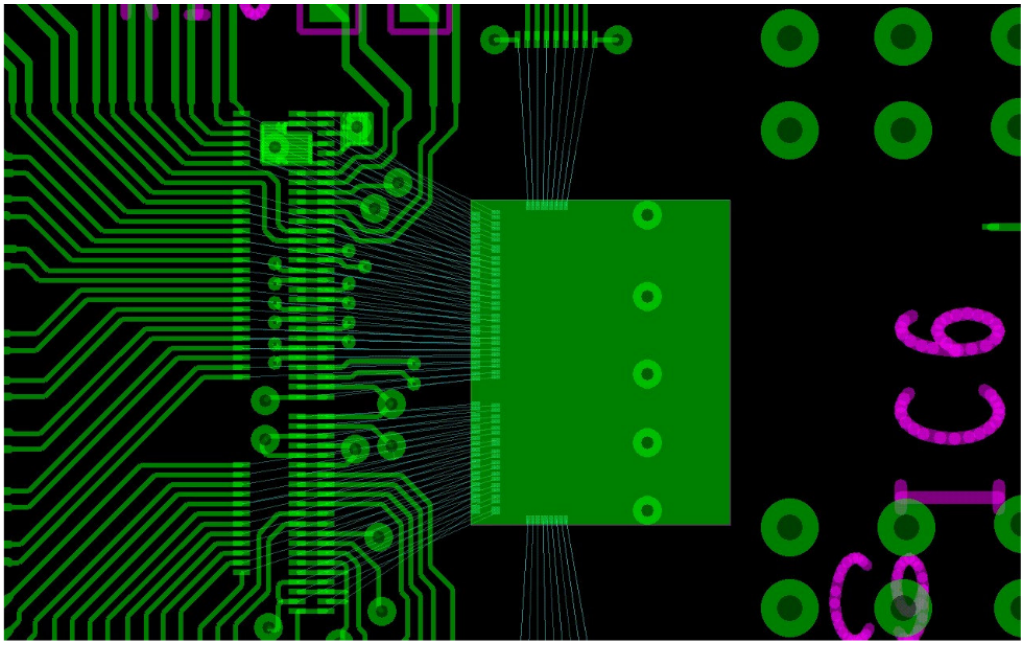
Table 4.5: Possible TDC configurations

4.2.1.4 Test results

Two PCBs have been developed to test the second prototype (Fig. 4.25). The chip is wire bonded to the sensor card which hosts also the trimmers for the analog bias of the ASIC, a 12 bit DAC to control the reference voltages that were forseen to be changed more often during the tests and the LVDS chips for clock and *Test*



(A)



(B)

Figure 4.25: (A) Picture of the PCBs used for the ASIC tests. On the right the sensor card with the chip wirebonded, on the left the adapter card used with the DPG and the LSA. (B) Detail of the bonding area of the sensor card

Pulse distribution. The pads pitch is 150 μm and they are organized in two rows as illustrated in Fig. 4.25 B.

The sensor card can be connected to the adapter card through a High Speed Mezzanine Card (HSMC) connector to perform the tests using a Data Pattern Generator (DPG) and a Logic State Analyzer (LSA). The data pattern for configurations and for tests are created using VHDL simulations. The sensor card and the instruments are triggered by the same clock. The chip can be readout also connecting the sensor card directly to an FPGA based system through the same HSMC connector. The acquisition and data analysis is based on Labview routines.

The analog and digital test pads allow the inspection of internal analog outputs on the test pixels and of digital internal nodes. These pads cannot be used with the sensor connected.

The chip is powered by 1.2 V voltage regulators accommodated on the PCB. Different power supplies have been foreseen for the analog and digital sections of the chip to minimize the effects of digital noise crosstalk. Moreover the EoC logic has a dedicated bias with respect to the digital section in the pixels. Power consumptions have been measured at 1.2 V and 160 MHz, leading to 2.43 mW/pixel. The details of single contributions are given in Table 4.6. However the power consumption for each pixel is overestimated, in fact the prototype ASIC contains two bias cells for the pixels analog references, one for the matrix and one for the two test pixels. Their contribution to power consumption is shared between the 107 pixels in the prototype. On the other hand the full size chip would have only one bias cell for 1800 channels. The extra contribution of the bias cells have been estimated of about the 30% of the analog power consumption, resulting in a total dissipation of 2.16 mW/pixel.

Supply	Power consumption @ 1.2 V
Analog	897 μW/pixel
Digital (pixel)	343 μW/pixel
EoC	125 mW @ 160 MHz
Total	2.43 mW/pixel

Table 4.6: Dissipation of the analog and digital sections of the prototype with 1.2 V power supply

The EoC and digital sections The chip configuration registers are correctly uploaded and read back at 160 MHz. However the *End of Count* output, which flags the coarse counter end of count, does not behave properly at 160 MHz. This malfunctioning is due to an under sized buffer that drives the signal. With this failure the End of Column state machines can not recognize the data frames and no headers or trailers are added to the data stream. The problem has been partially solved by slowing down the system at 80 MHz. Increasing the power supply up to 1.5 V, the EoC state machine works properly up to 130 MHz. However, for the analog tests it has been decided to work with 1.2 V supply to reduce the effects of the digital noise.

The three EoC FSM outputs during data readout are shown in Fig. 4.26.

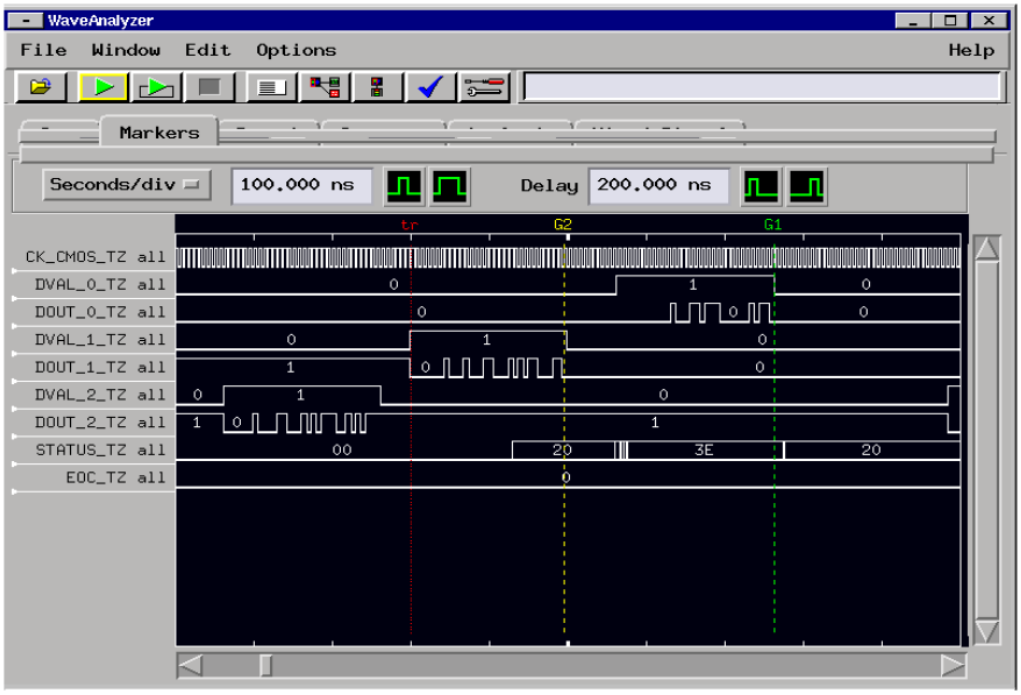


Figure 4.26: LSA screenshot of the EoC output data

The EoC digital power supply serves all the standard cells in the ASIC, including the clock distribution and the differential data bus drivers. As a consequence the power consumption scales linearly with the clock frequency as showed in Fig. 4.27. These results have been obtained with one pixel in each column receiving a the *Test Pulse* and the coarse counter in gray mode. The total dissipation without clock is 36 mA.

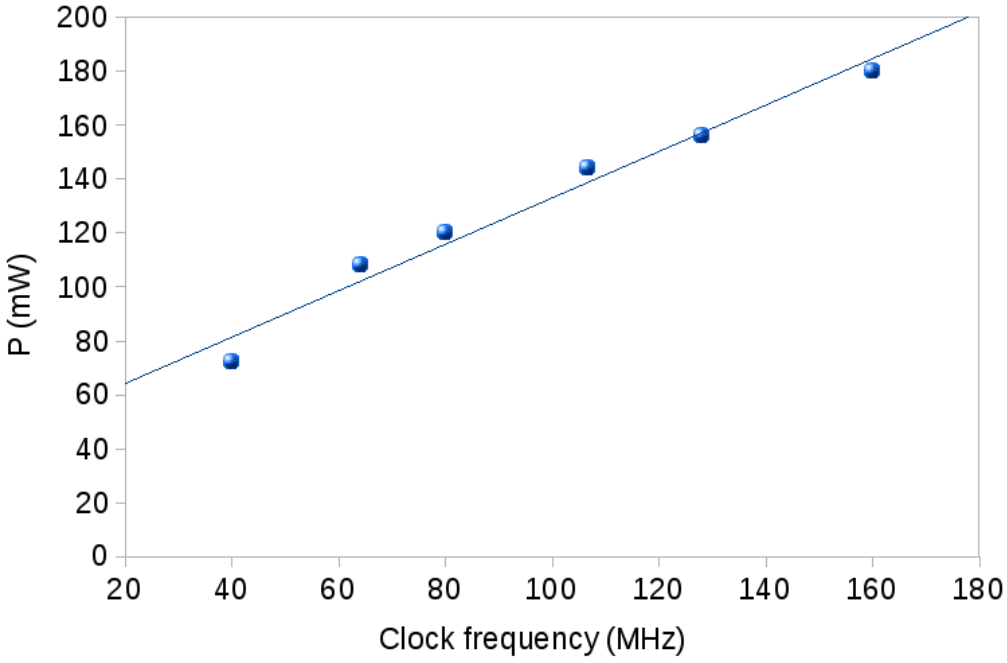


Figure 4.27: Dependency of the power consumption of the EoC on clock frequency

The preamplifier The preamplifier has been characterized through the analog outputs of the test pixels. Fig. 4.28 illustrates the on chip calibration and buffering circuits. The switches steer the calibration capacitance C_{cal} between the chip reference (GND_DET) and the calibration voltage. Both voltages are controlled by the on board DAC. The nominal value of the calibration capacitance is 22.1 fF, thus the nominal voltage step to provide 1 fC charge is 45.5 mV. The switches are triggered by the external LVDS signal *Test Pulse*. In order to avoid performance overestimation, a local RC filter is provided in each pixel to smooth the calibration signal giving a rise time approximately equal to the one expected from the detector. Moreover, on the test pixel a capacitance C_{det} of 170 fC is provided to emulate the effect of the detector capacitance, while the pixels in the columns do not present the same capacitance. There is the possibility to monitor analog signals in one of the pixels by means of two integrated inverting buffers. The gain of the buffers is set to 1/3 to reduce distortion due to high slew of the signal. An extra attenuation comes from the $R_{osc} = 50\ \Omega$ load of the oscilloscope which forms a voltage divider with the parasitic resistance R_{line} of the routing. The value of R_{line} has been estimated from the layout to be around 7 Ω, resulting in an output attenuation of 0.88.

The preamplifier linearity has been measured in the dynamic range from 1 fC to 10 fC on the two phases of the differential output. Fig. 4.29 shows a good correlation between simulation and measurements. The actual gain, evaluated by correcting for the signal attenuation, is 80 mV/fC. The rise time (20%-80%), shown in Fig. 4.30, is nearly constant with respect to the signal amplitude and ranges from 3.15 ns to 3.4 ns. Finally, the SNR has been estimated from measurements with a 80 MHz clock to be $SNR_{meas} = 24$, which matches the value of $SNR_{sim} = 31.4$ found in simulations.

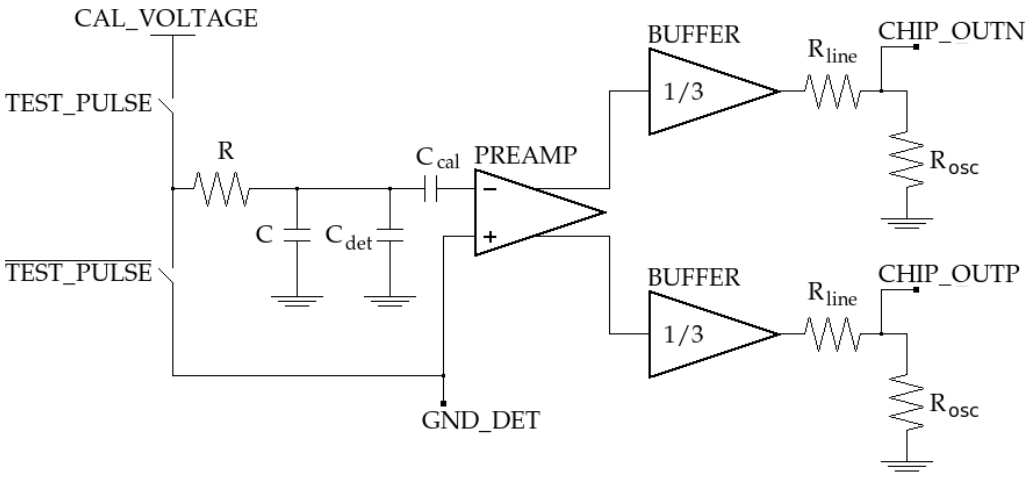


Figure 4.28: On chip charge injection mechanism and preamplifier output buffering in the test pixel

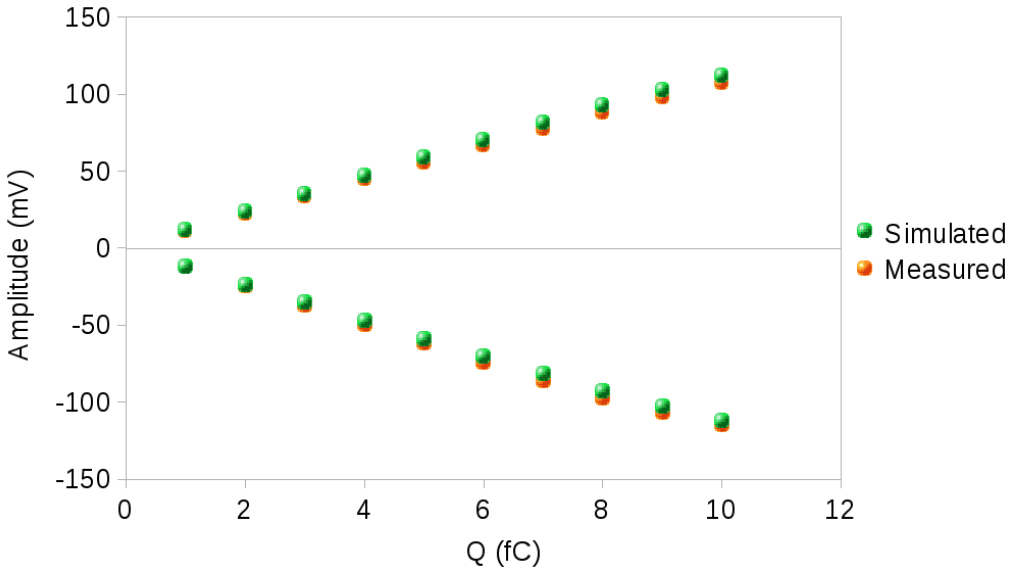


Figure 4.29: Preamplifier output peak amplitude compared with the simulation results in the dynamic range from 1 fC to 10 fC

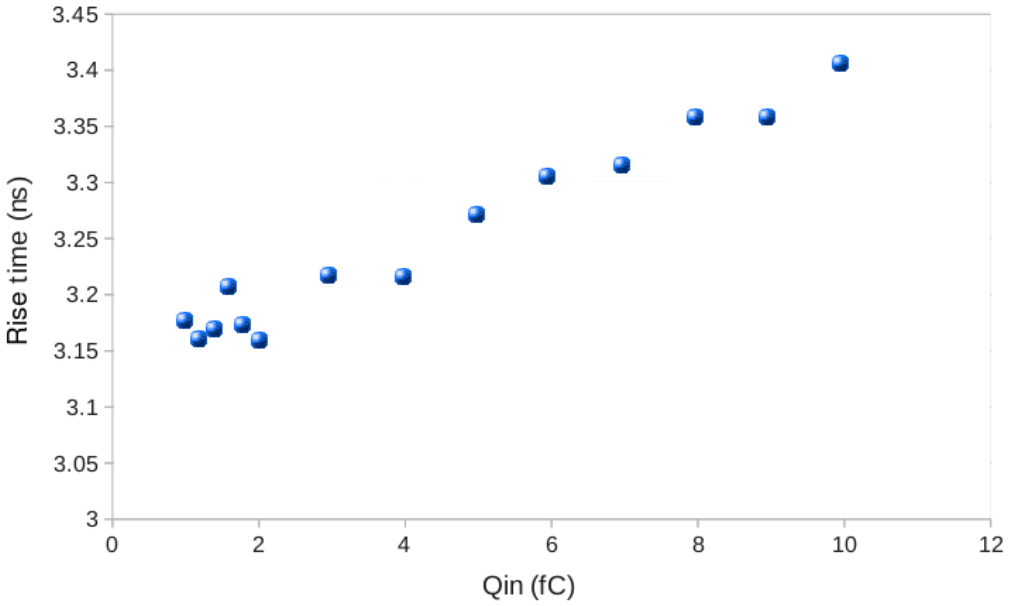


Figure 4.30: Peaking time of the preamplifier signal measured in the dynamic range from 1 fC to 10 fC

The CFD The CFD performance have been initially measured from the test pixels by injecting the reference charge and observing the analog output at the oscilloscope. The time walk and the jitter measured with the clock switched off are shown in Fig. 4.31. The overall time resolution at the output of the CFD has been estimated by convoluting the time walk curve and the jitter with the expected Landau of the experiment (see Appendix A). A set of 10^4 events distributed in charge as the Landau of the experiment have been extracted. To each charge value it has been associated a time extracted from a Gaussian distribution centered on the time walk experienced for that charge and large as the jitter measured for the same charge. The result, shown in Fig. 4.32, leads to 53 ps RMS.

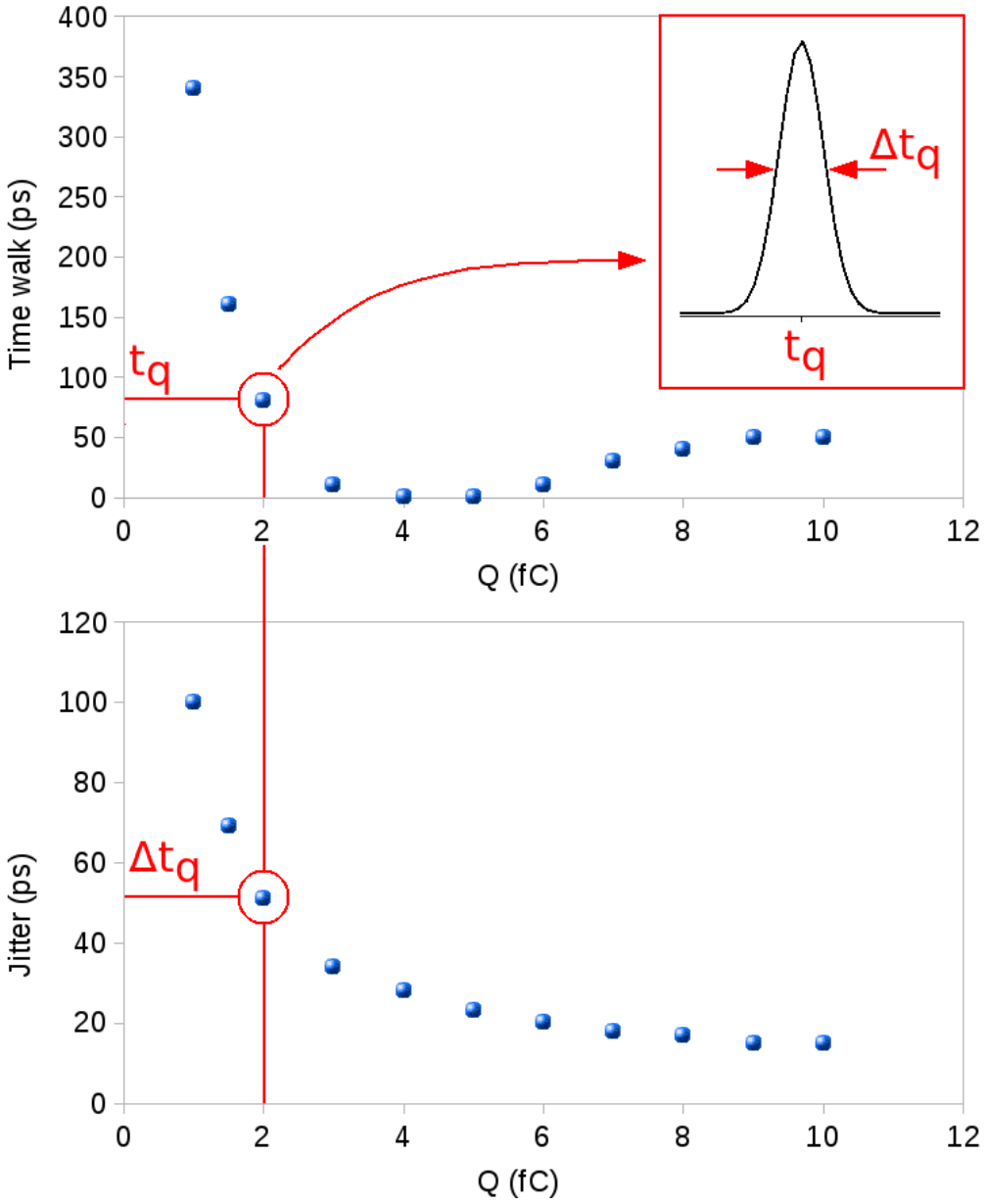


Figure 4.31: Time walk curve and jitter measured from the test pixel on the bipolar signal at the oscilloscope

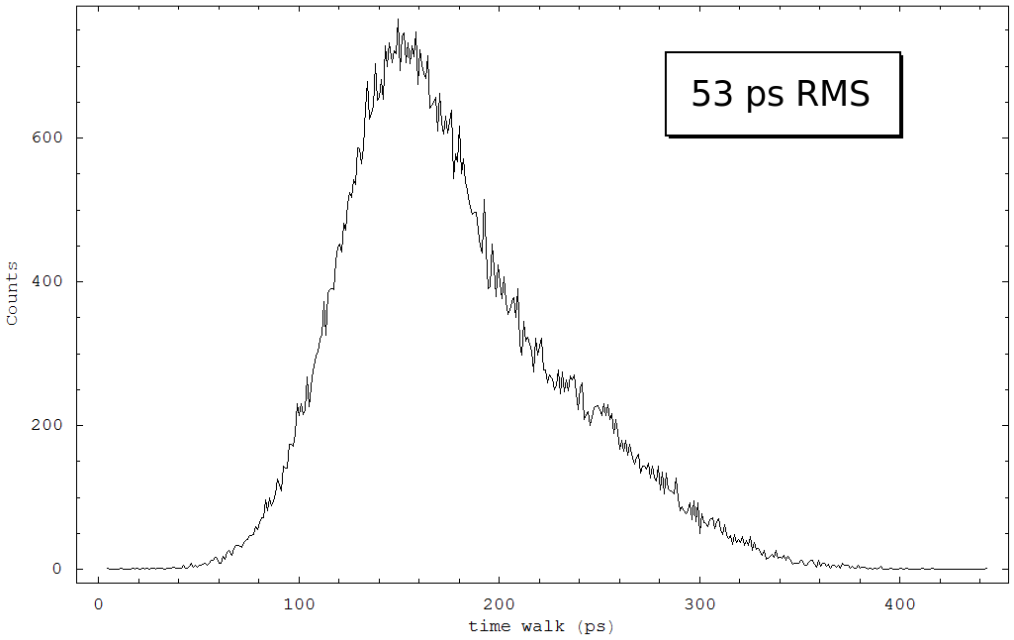


Figure 4.32: Convolution of the time walk and of the jitter measured from the test pixel with the expected Landau of the experiment

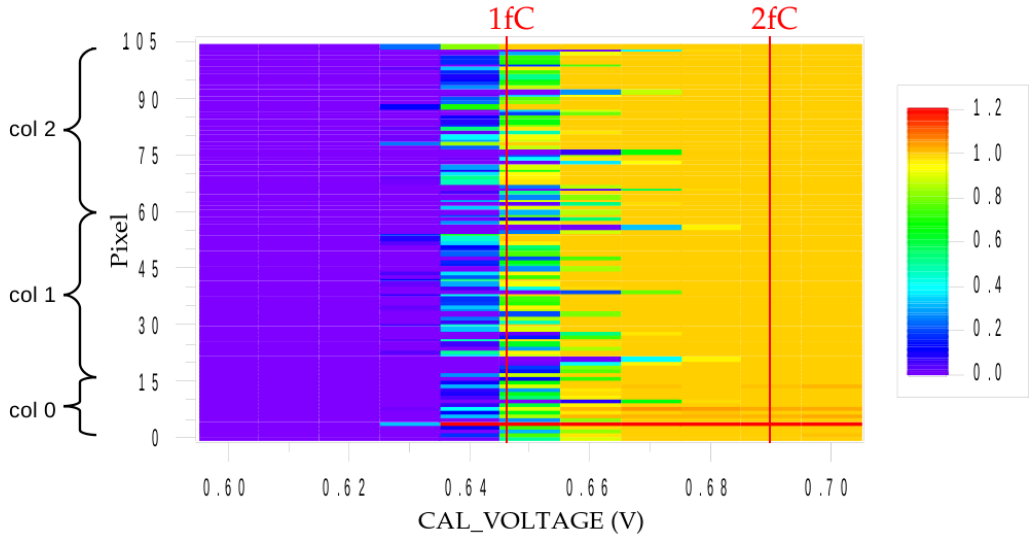
The zero crossing discriminator The chip is provided with a 3 bit DAC for the equalization of the thresholds of the discriminators. Fig. 4.33 shows the efficiency with respect to the charge for all the pixels in the matrix before and after the threshold equalization. Due to the noise, the full efficiency is reached at 1.45 fC instead of the nominal 1 fC. The S curve after equalization is plotted in Fig. 4.34 for the pixels with the worse and the best efficiencies and in Fig. 4.35 for the one with the average final efficiency.

Fig. 4.36 show an example of the threshold histogram before and after the equalization. The threshold dispersion after equalization for all the pixels of four different ASICs is shown in Figg. 4.37 and 4.38. The result of equalizations is summarized in Table 4.7.

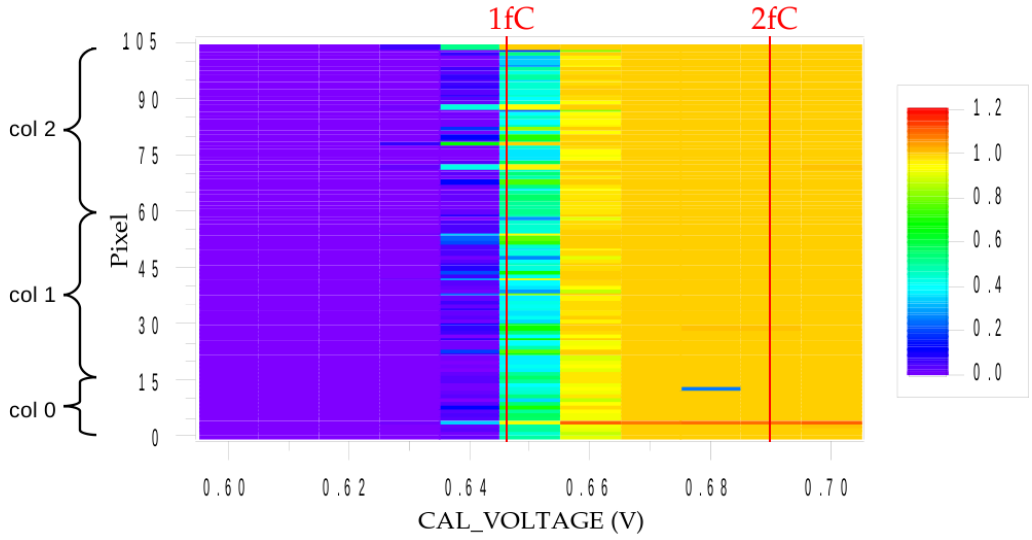
	50% S-curve (fC)	Threshold dispersion (fC RMS)
BOARD III	0.97	0.48
BOARD IV	0.97	0.49
BOARD VI	0.97	0.51
BOARD VII	1.21	0.50

Table 4.7: Avarage value of the input charge at which the efficiency is 50% for the tested boards after threshold equalization

The slope of the S curves reported in Table 4.7 gives a direct measurement of

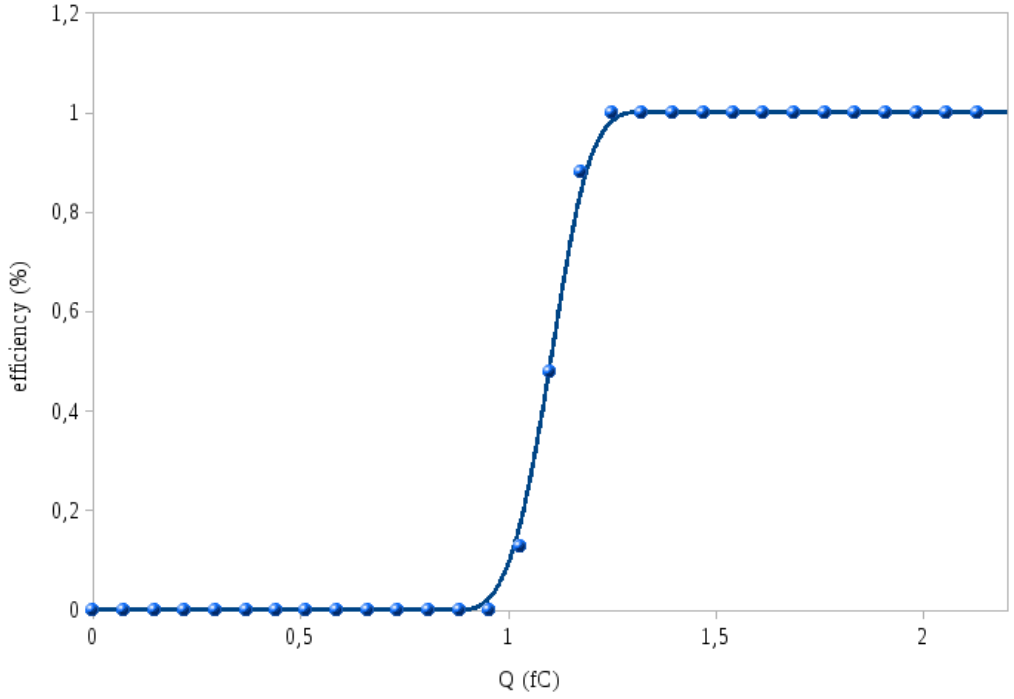


(A)

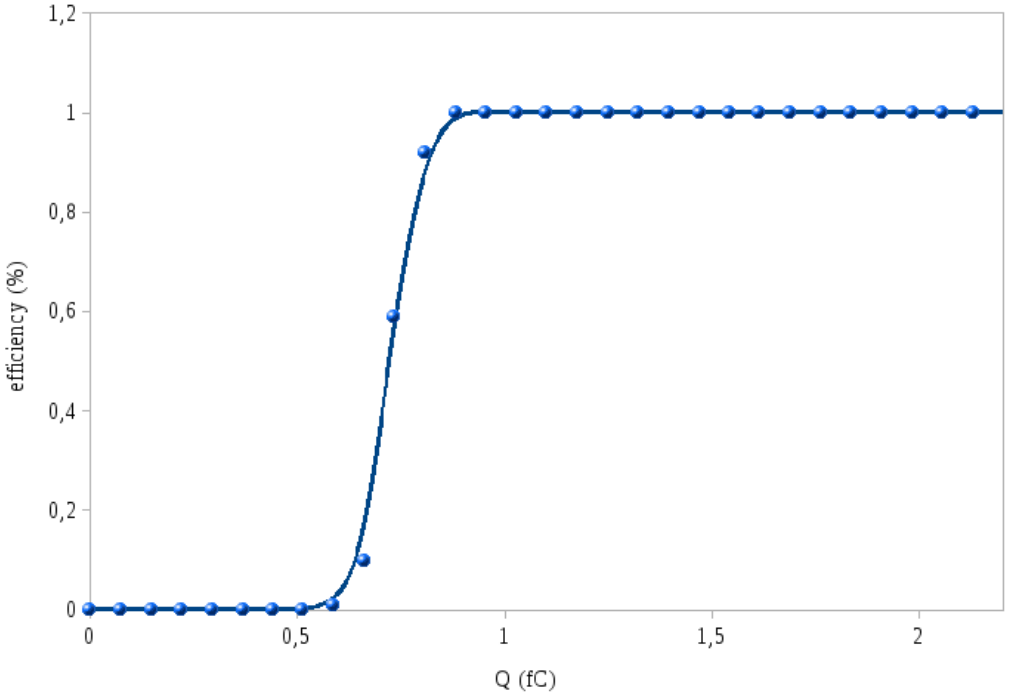


(B)

Figure 4.33: Scan of the threshold of all the discriminators in the matrix (A) before and (B) after the equalization with the DAC on chip



(A)



(B)

Figure 4.34: S curves after threshold equalization in the cases of (A) worse and (B) best efficiency

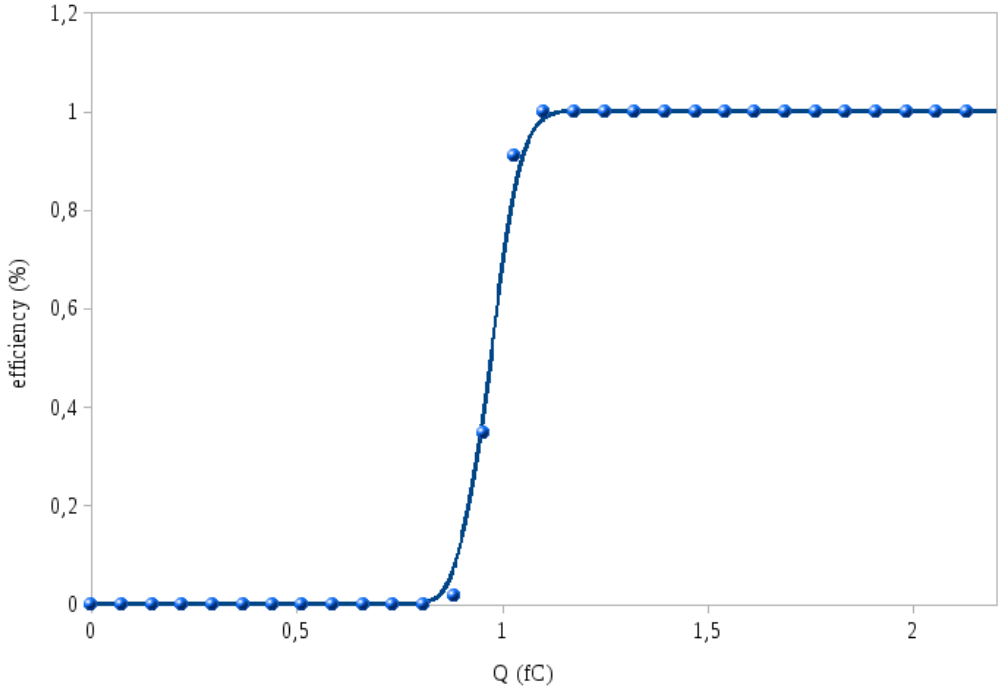


Figure 4.35: S curves after threshold equalization in the cases of typical efficiency

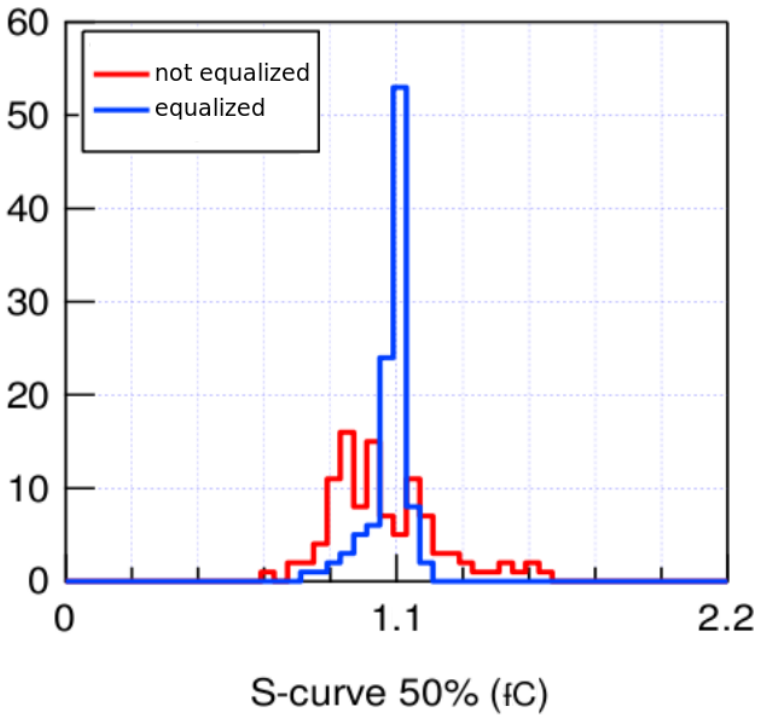


Figure 4.36: Histogram of the charge value at which the efficiency is 50% for all the matrix pixels before and after the threshold equalization

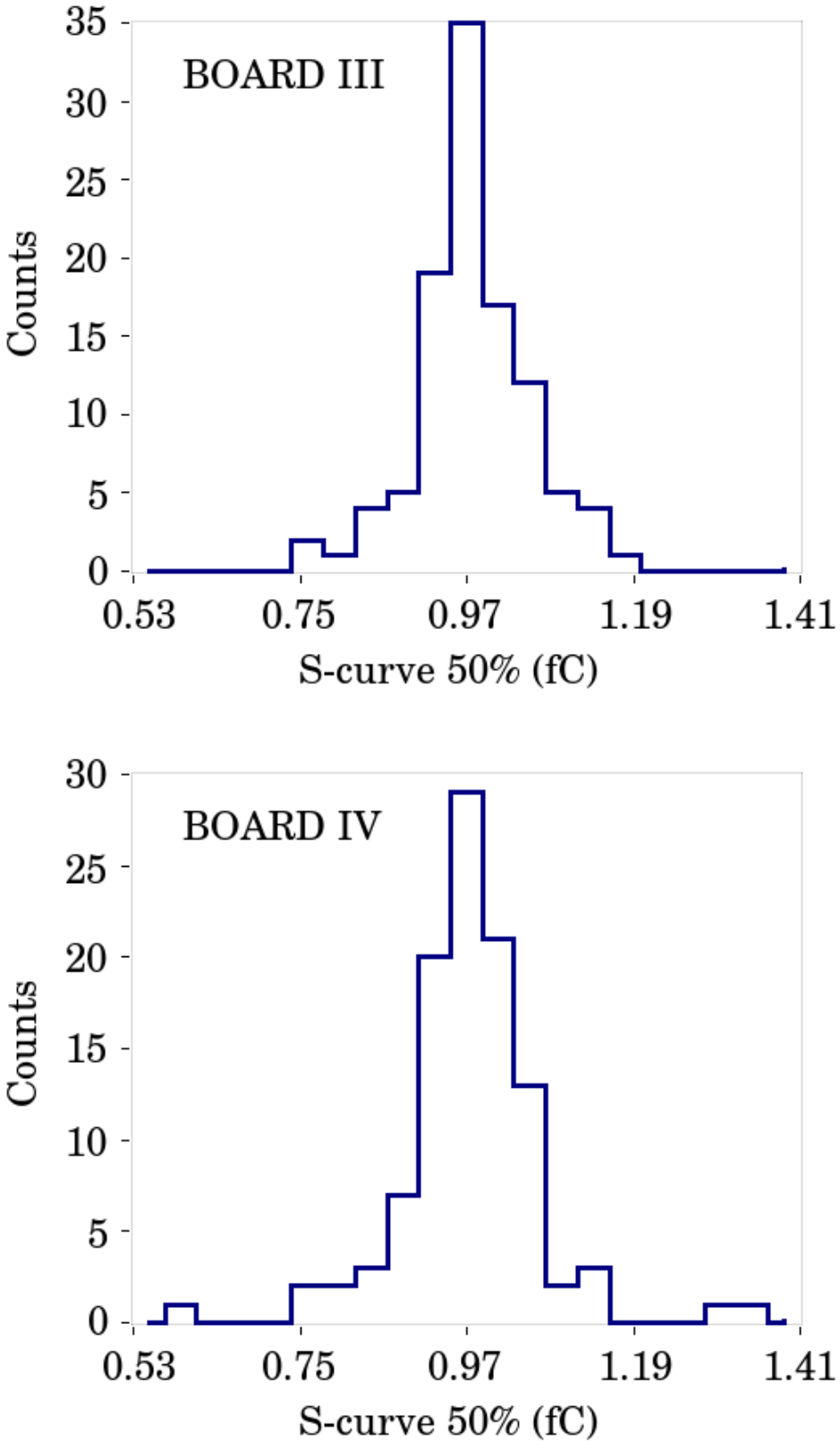


Figure 4.37: Threshold dispersion after equalization for different chips mounted on boards III and IV

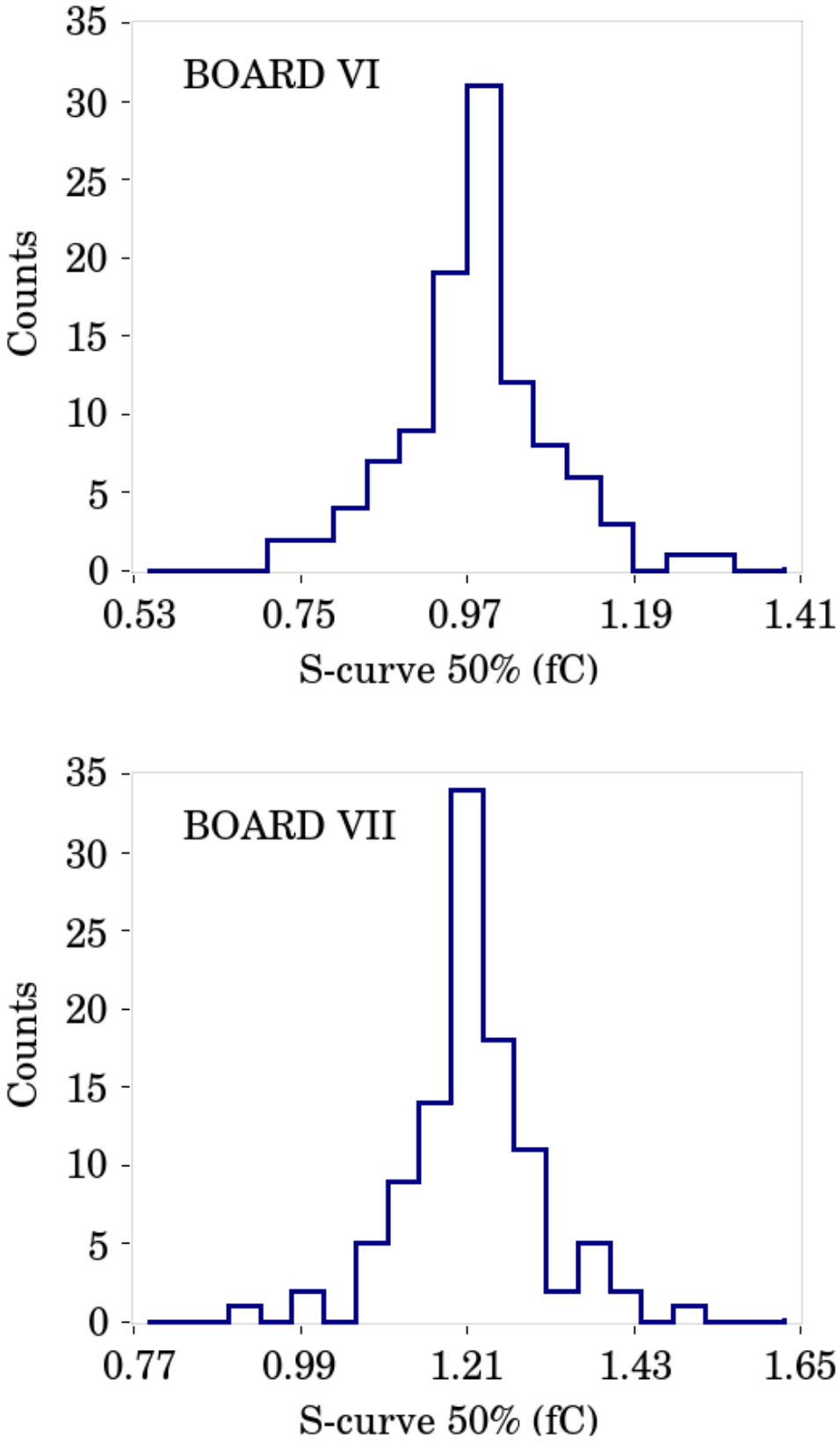


Figure 4.38: Threshold dispersion after equalization for different chips mounted on boards V and VII

the noise at the output of the front-end. Thus the average ENC and the SNR have been calculated for the four chips and the results are summarized in Table 4.8. It

	ENC	SNR @ 1 fC
BOARD III	300 e^-	20.8
BOARD IV	303 e^-	20.6
BOARD VI	319 e^-	19.6
BOARD VII	315 e^-	19.8

Table 4.8: Avarage value of the ENC and corresponding SNR at 1fC for the tested boards after threshold equalization

should be noted that the SNR measured from the matrix (with the sensor bump bonded to the chip) agrees with the same measure performed on the preamplifier output of the test pixel (see paragraph 4.2.1.4).

The TDC Fig. 4.39 shows the output of the TDC measured by sending a set of *Test Pulses* synchronous to the clock. An input signal every 256 clock cycles is feeded to the pixel, thus the coarse time assumes only four values (each frame lasts 1024 clock cycles). The TDC works properly since the measured fine time is always the same. If an asynchronous signal is sent to the pixel (using a *Test Pulse* with a frequency of 67.7 MHz against the 80 MHz of the clock), the relative phase between the signal and the clock changes continuously and the fine time assumes all the possible allowed values, as shown in Fig. 4.40.

In the plots of the fine time the first point assumes always a big value out of the allowed range. This phenomenon, which is clearly visible in Fig. 4.39, has been studied and reproduced in simulation. Referring to Fig. 4.23 B, when the TAC does not receive a signal, it waits in normal mode. In this configuration the leakage current flowing through S5 discharges the storage capacitor changing the starting voltage of the TAC. When the signal arrives, the capacitor is further discharged. As a consequence a longer slow ramp is generated. This error cannot be calibrated since it depends on the time distance between two consecutive events, which is unknown. The introduced error is not significant if it is lower than the TDC LSB. It has been measured that the minimum rate which satisfies this condition is 1 kHz.

A 3 bit DAC for the equalization of the TDCs has also been implemented on chip. The ramp length before and after the equalization for all the pixels of the four tested chips has been measured with the TDC in calibration mode. As already described, in this modality it is possible to send at the input of the TDC a synchronous *Test Pulse* lasting one or three clock cycles (which represent the minimum and maximum ramp length). The offset before the equalization is due to the operational amplifier which controls the discharge current in the TDC. Referring to Fig. 4.24, the amplifier generates an offset on the drain of M1 with respect to M3. Moreover the area dedicated to the TDC is limited, thus the transistors of the mirror cannot be made big as it is required by matching rules. This fact explains why, after the equalization,

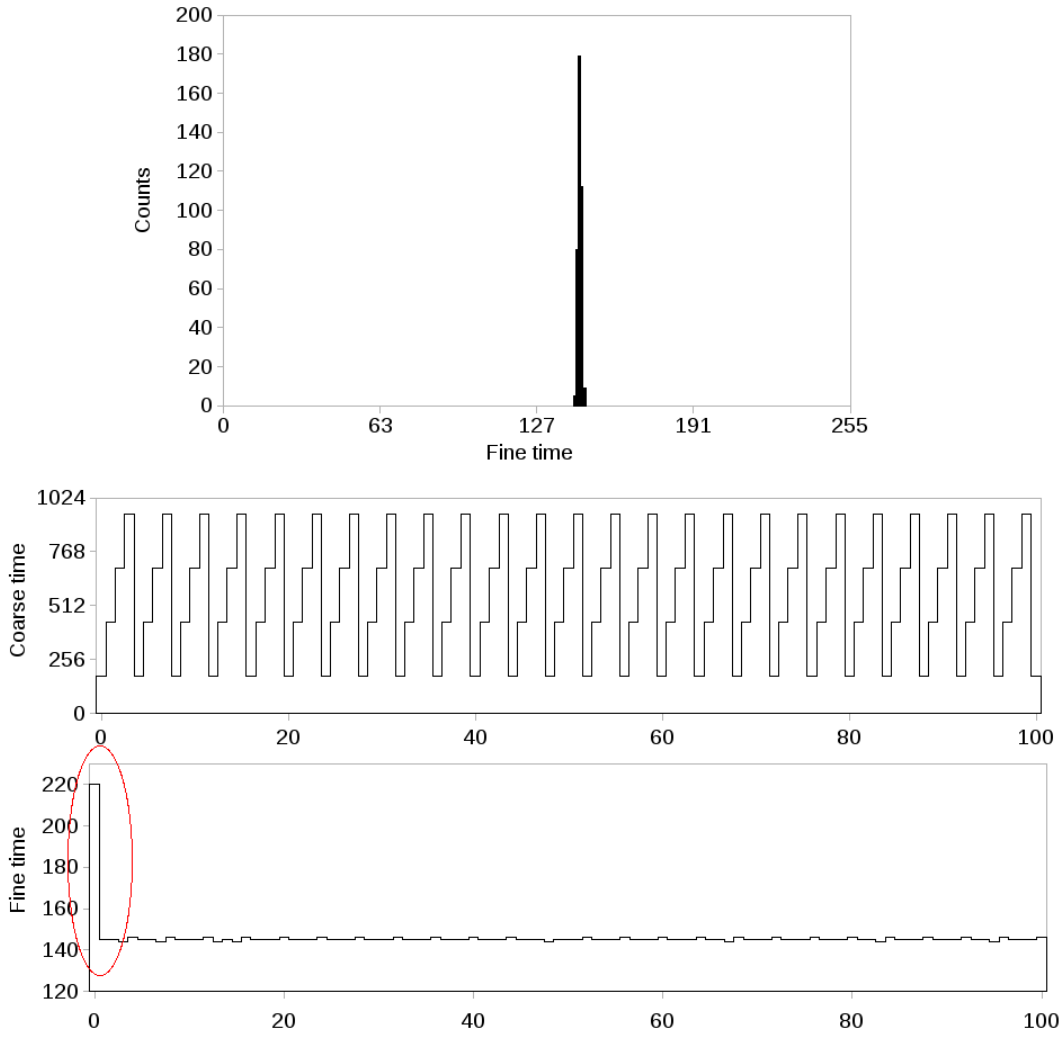


Figure 4.39: Coarse and fine times measured by sending a *Test Pulse* synchronous to the clock. To be noted the first point in the fine time plot due to the discharging of the TAC storage capacitor in idle mode

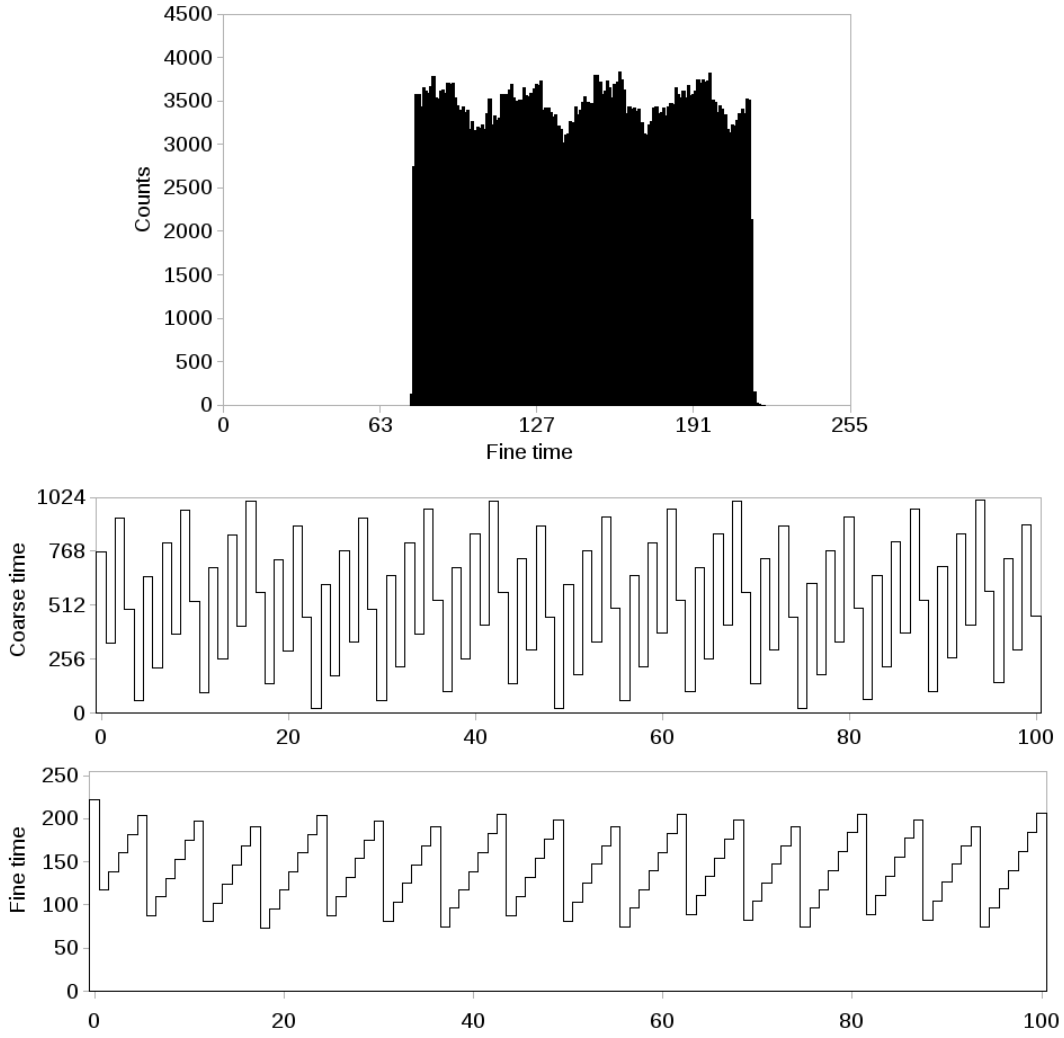


Figure 4.40: Coarse and fine times measured by sending a *Test Pulse* asynchronous to the clock

the maximum ramp length varies between 95 and 100 instead of being 128 (Figg. 4.41 and 4.42). The result is a larger bin of 132 ps at 160 MHz with respect to the nominal 98 ps. The resulting quantization error is $132/\sqrt{12} = 38$ ps RMS, which is only 10 ps worse than the nominal one. Working at 80 MHz the bin with doubles leading to 76 ps RMS.

After the equalization, the linearity of the TDCs have been measured by sending a set of 10^6 random *Test Pulses*. The resulting fine time histogram is shown in Fig. 4.43, a flatten distribution is expected in a perfect TDC. In an ideal 7 bit TDC, the expected number of counts for each bin would be:

$$N_{th} = \frac{10^6}{2^7} \tag{4.14}$$

The experimental value differs from N_{th} because of non linearities. The Differential Non Linearity (DNL) is a measure of the uniformity of the channels over the range of the TDC. Thus the DNL assesses the deviation of each bin from the ideal bin width. The Integral Non Linearity (INL) describes the maximum error done in a measure. The DNL and the INL are defined as follows:

$$DNL(i) = \frac{N_{meas}(i) - N_{th}(i)}{N_{th}(i)} \tag{4.15}$$

$$INL(i) = \Sigma_{k=0}^{i} DNL(k) \tag{4.16}$$

To ensure that there is no missing code in the TDC ramp, the following conditions should be respected:

$$|DNL(i)| < 0.5 \tag{4.17}$$

$$|INL(i)| < 1 \tag{4.18}$$

Typical DNL and INL, plotted in Fig. 4.44, show a good linearity, since they do not exceed the values mentioned in disequations 4.17 and 4.18. This results is the consequence of the use of the Wilkinson ADC, which has been adopted because it is very compact and fits the specifications. This ADC topology has intrinsically a good DNL and no missing code, since the bin width is defined by the clock, which is very precise, and by the non-linearities of the ramp. The same measure repeated on a full column (Fig. 4.45) shows a good uniformity for pixels near or far from the EoC.

The linearity of the TDCs has also been measured on the single ramp by feeding to the pixels a set of *Test Pulses* with the delay increasing in steps of 20 ps. Six clock cycles have been covered, corresponding to 2 complete TDC ramps. The reconstructed times with respect to the input times are plotted in Fig. 4.46. A zoom on the plot shows a modulation on the ramp. To evaluate the entity of this modulation, the difference between the measured value and the expected one has been calculated (see Fig. 4.47). The distribution has a dispersion of 73 ps RMS. The peak-to-peak error of 350 ps corresponds to plus/minus one TDC bin at 80 MHz (at this frequency one bin corresponds to 196 ps) and agrees with the INL measure shown in Fig. 4.45 B. This non linearity effect has been studied and reproduced in simulation. The critical point is the amplifier that controls the current mirror in

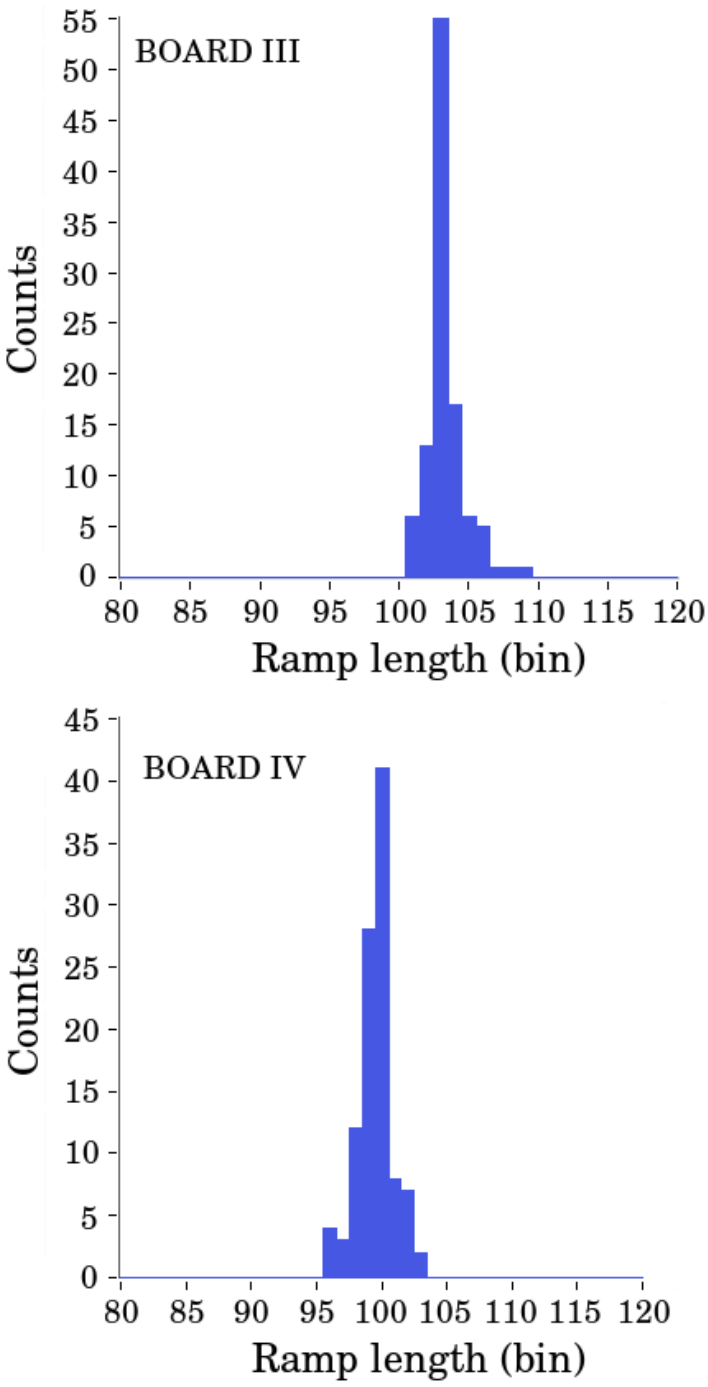


Figure 4.41: TDC ramp length after the equalization for all the matrix pixels of chips mounted on board III and IV

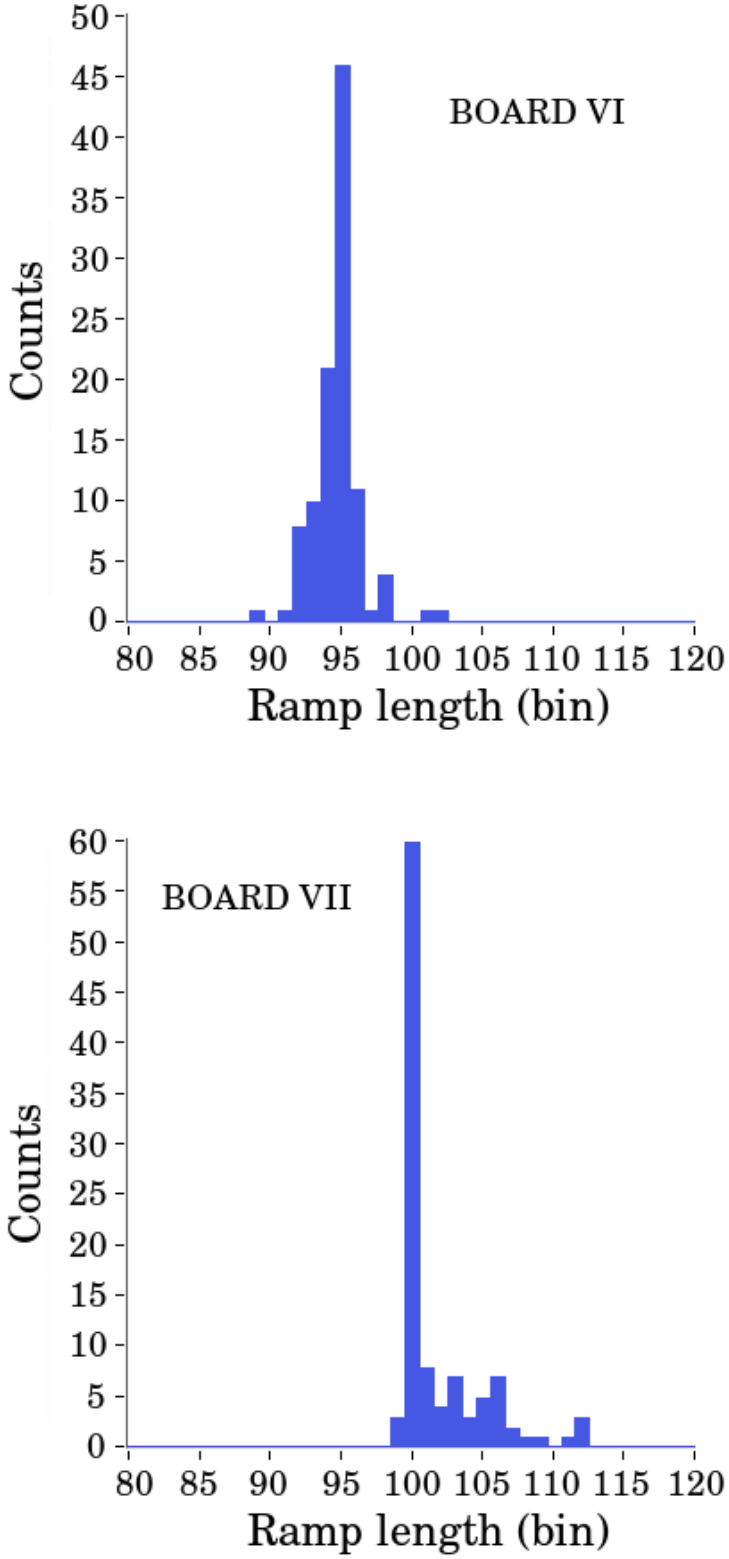


Figure 4.42: TDC ramp length after the equalization for all the matrix pixels of chips mounted on board VI and VII

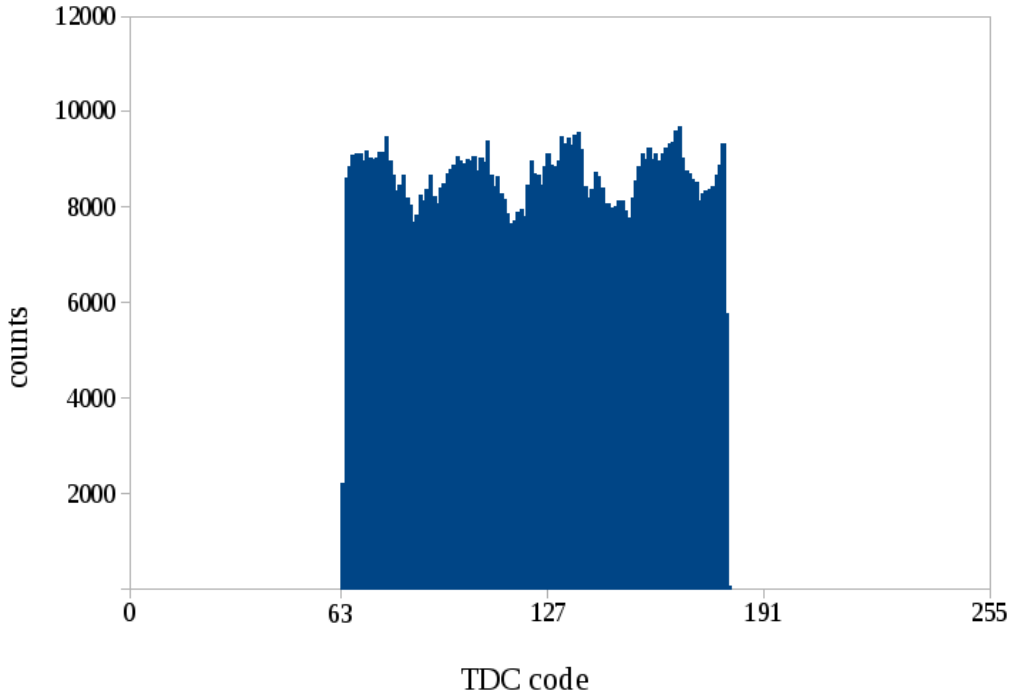
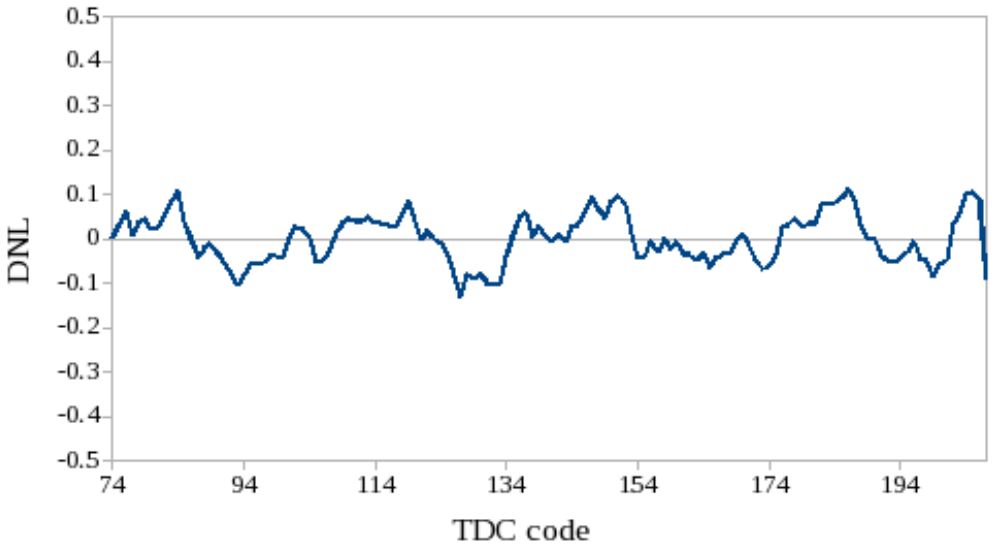


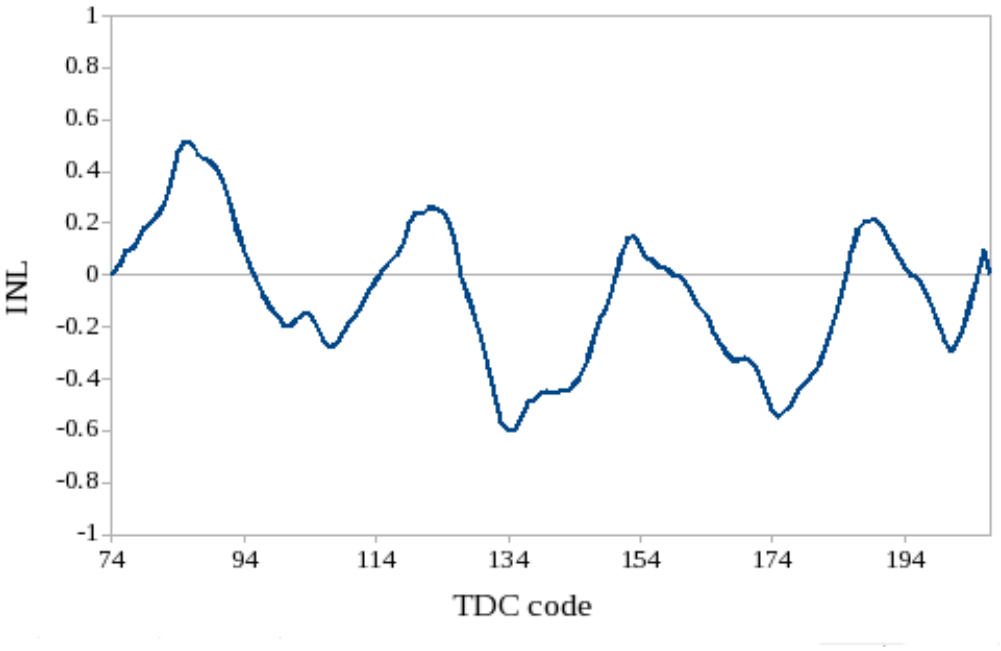
Figure 4.43: Output of the TDC obtained by sending a set of asynchronous *Test Pulses*

the TDC (see Fig. 4.24), which is sensible to the noise on the supply voltage. This sensitivity leads to a modulation of the drain voltage of the transistor that provides the current for the slow ramp introducing a non linearity between the charge and discharge currents in the TDC.

Finally the multibuffer has been tested by sending a *Test Pulse* every 16 clock cycles. The first four events are stored, while the other are lost. However it has been noticed that for a high number of *Test Pulses* the logic in the pixel fails and keeps the entire column in busy state. The same problem came out from the beam test, where for high particle rate the columns stop working. It is caused by a bug in the interface between the digital section in the pixel and the EoC logic. For what concerns the linearity of the TAC buffers, the time measured by the four of them has been compared. The result are plotted in Figg. 4.48, 4.49 and 4.50 and summarized in Table 4.9. While the mean value of the differences can be calibrated, the dispersion of the distribution introduces an additional jitter to the measure. However in this prototype it is not possible to measure the actual mismatch of the buffers since the measure is dominated by the non linearities of the ramp shown in Fig. 4.47. This is due to the fact that the buffer mismatch has been measured on different clock cycles and it has been shown that the TDC suffers of non linearities linked to the clock period. Thus it is not a case that the 80 ps RMS non uniformity obtained from this measure matches exactly the 73 ps RMS due to non linearities.



(A)

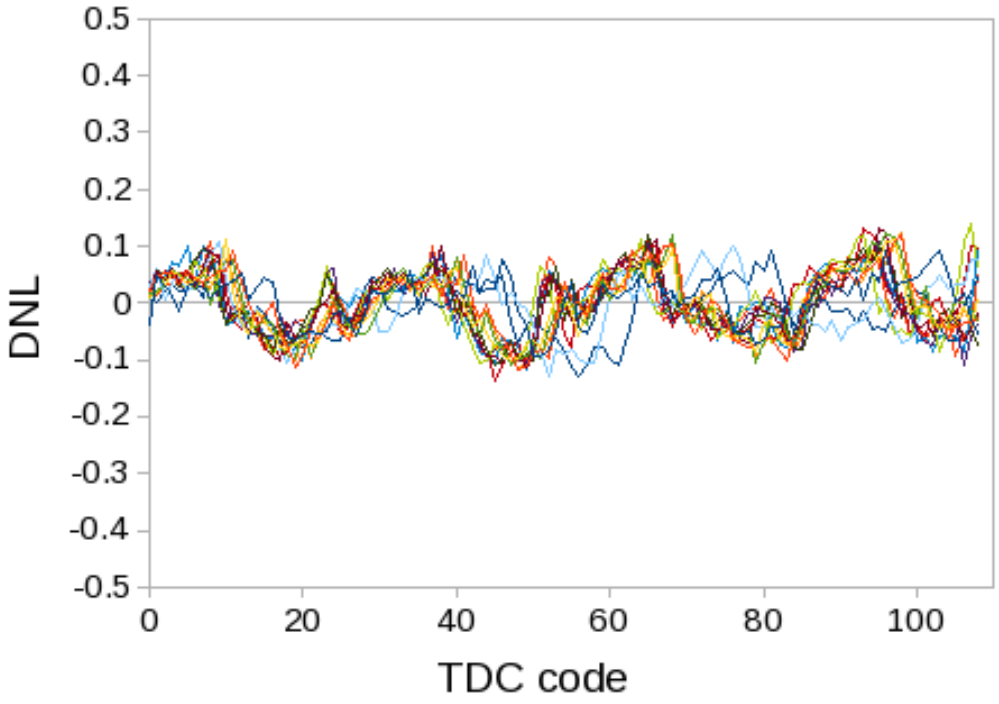


(B)

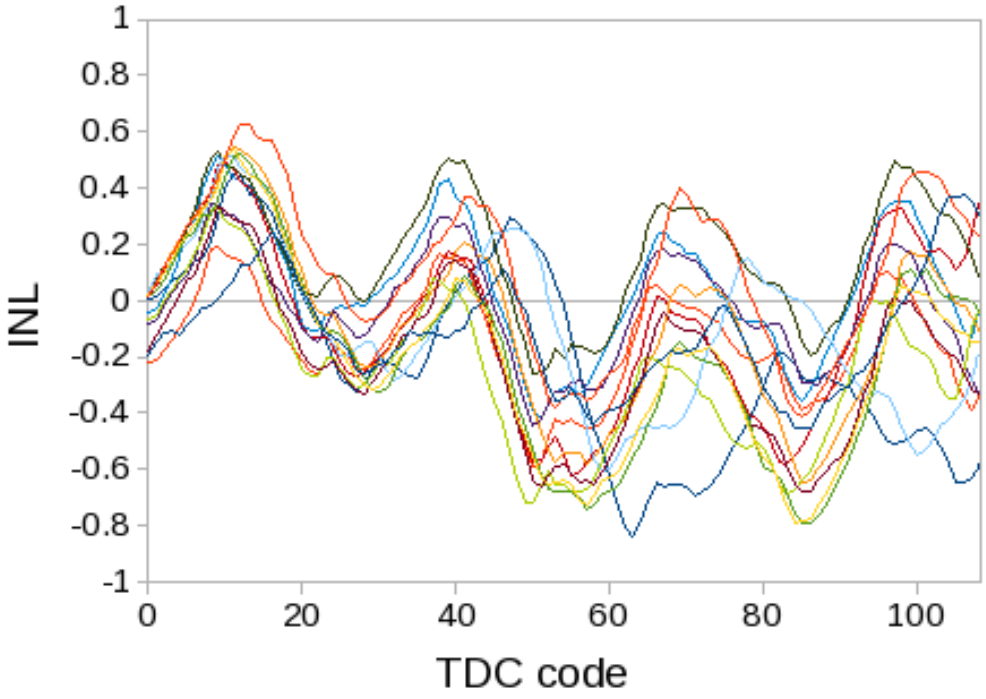
Figure 4.44: DNL and INL calculated for one pixel

	Measured quantity	Mean value (ps)	Standard deviation (ps)
BUFFER II	T_2 - T_1	-149.83	41.35
BUFFER III	T_3 - T_1	-111.46	79.71
BUFFER IV	T_4 - T_1	-211.50	61.05

Table 4.9: TAC buffers mismatch with respect to the first one measured at 80 MHz

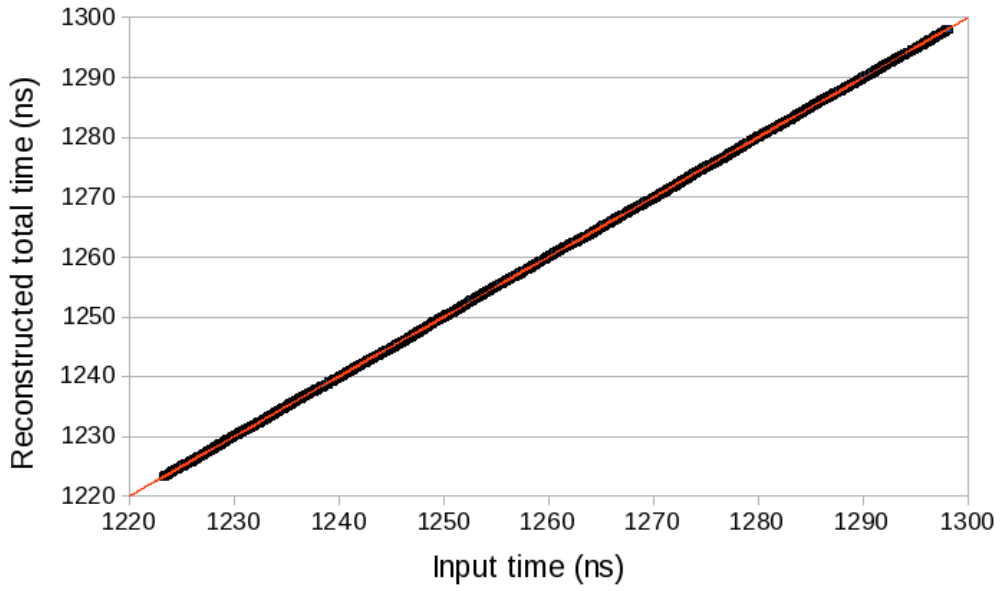


(A)

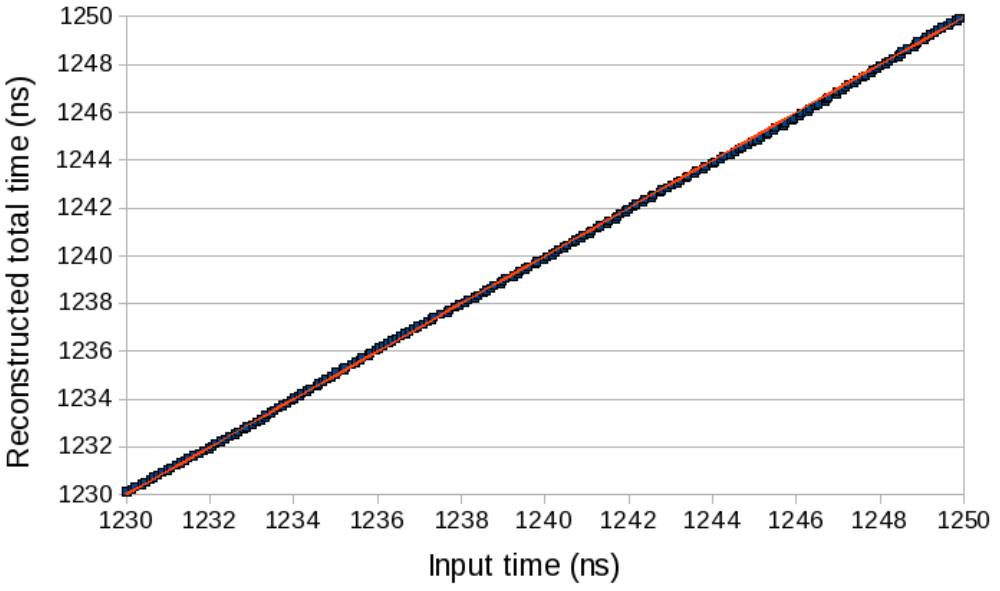


(B)

Figure 4.45: DNL and INL of a full column



(A)



(B)

Figure 4.46: (A) Total output times reconstructed on 6 clock cycles and (B) a zoom on the same measure

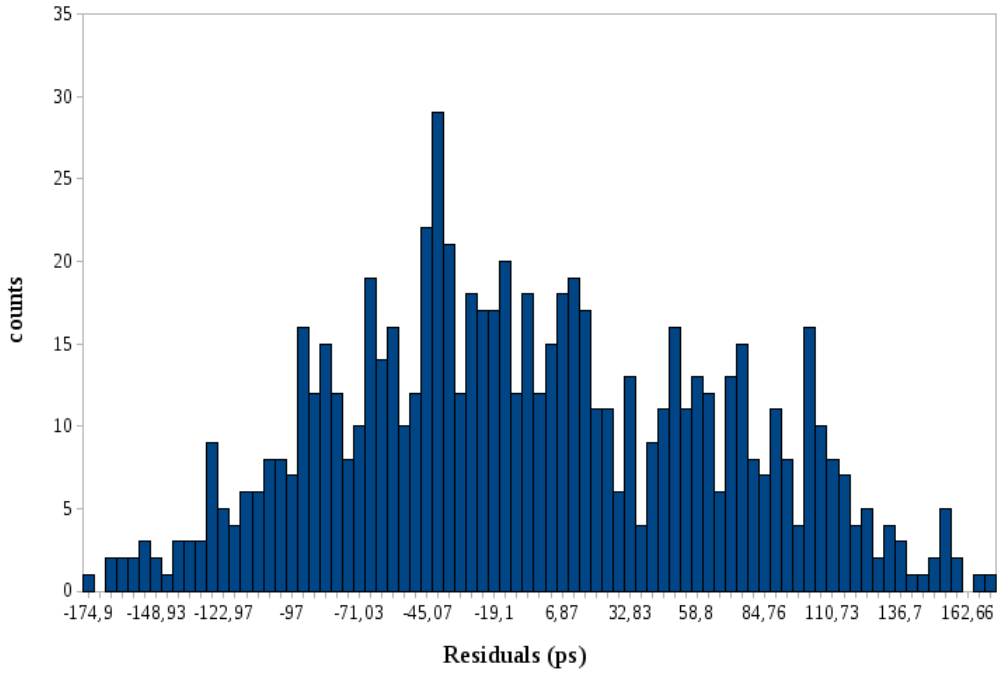


Figure 4.47: (Histogram of the difference between the reconstructed and the expected times

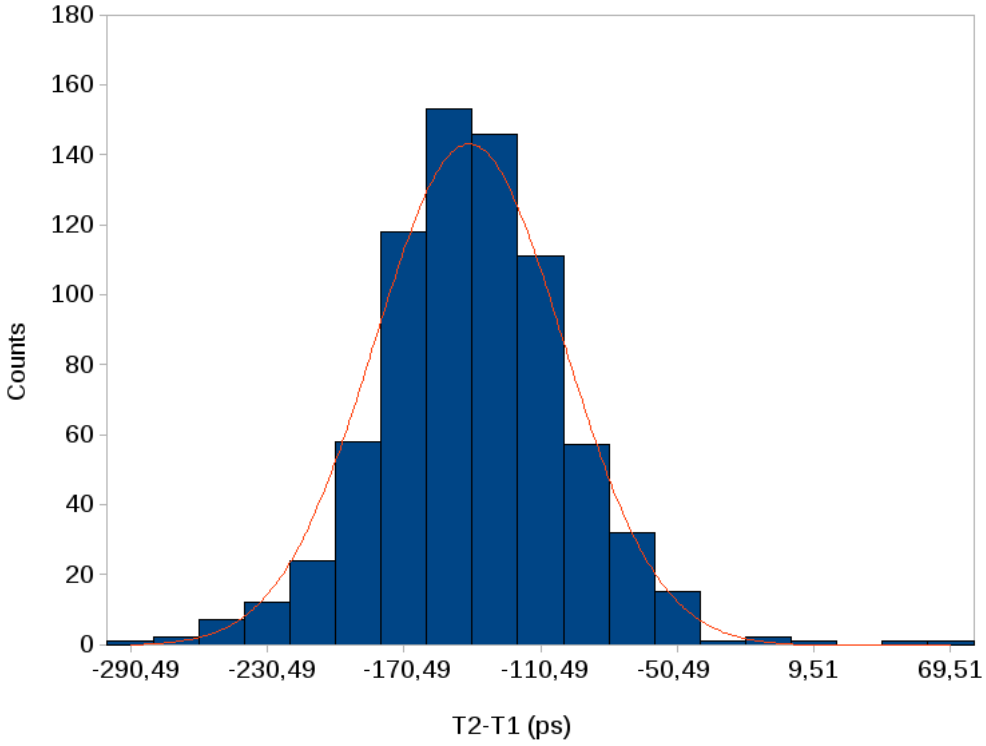


Figure 4.48: Measure of the mismatch of the second TAC buffer with respect to the first

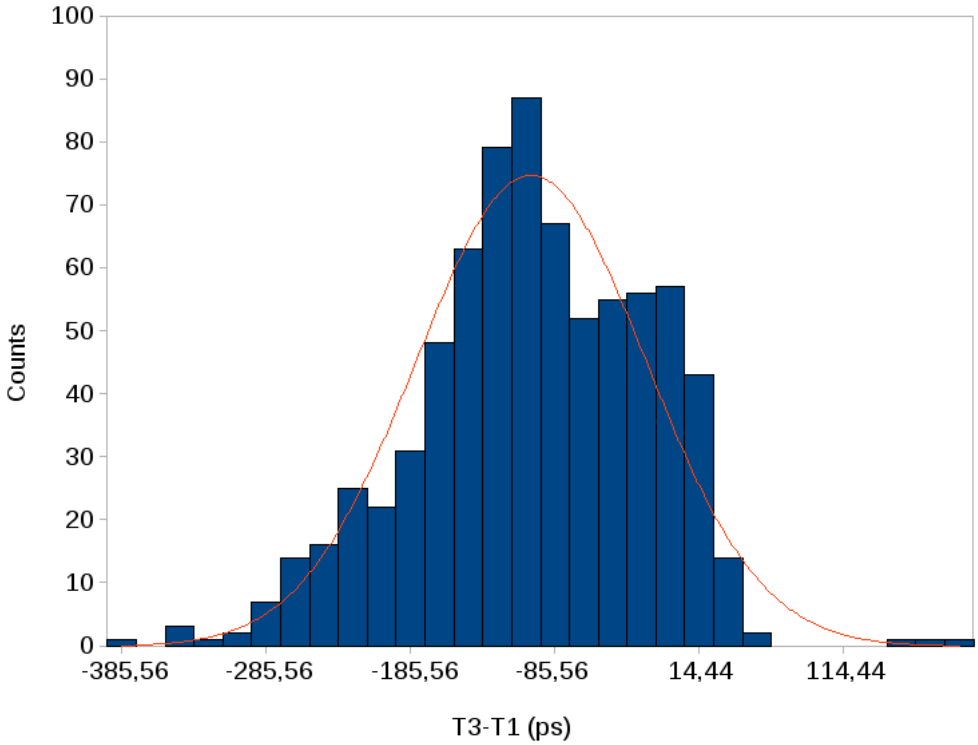


Figure 4.49: Measure of the mismatch of the third TAC buffer with respect to the first

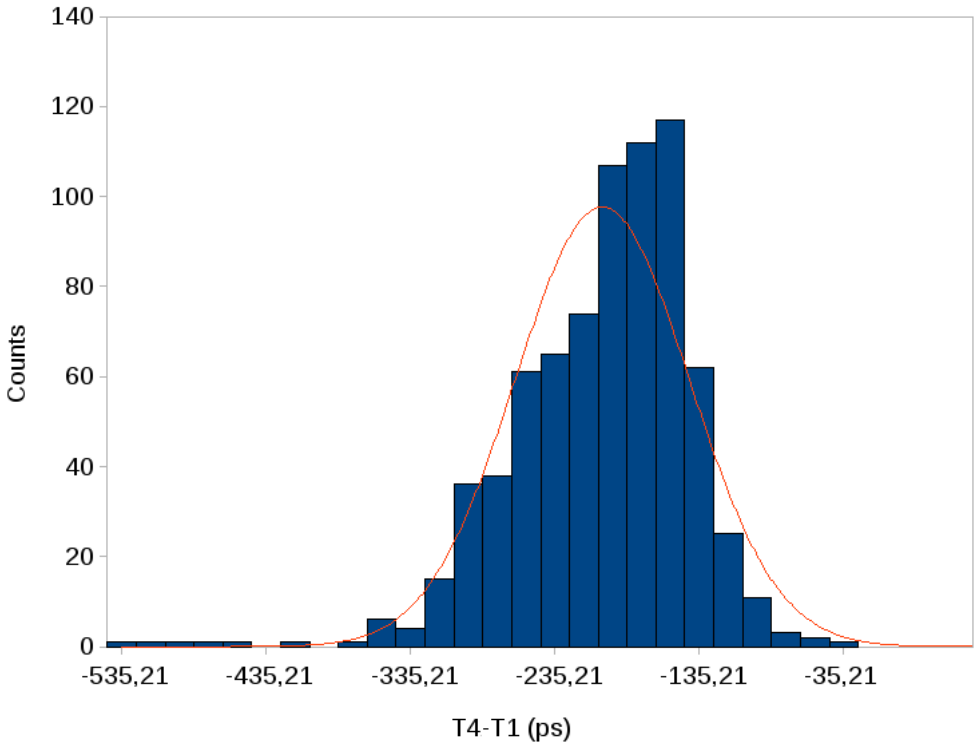
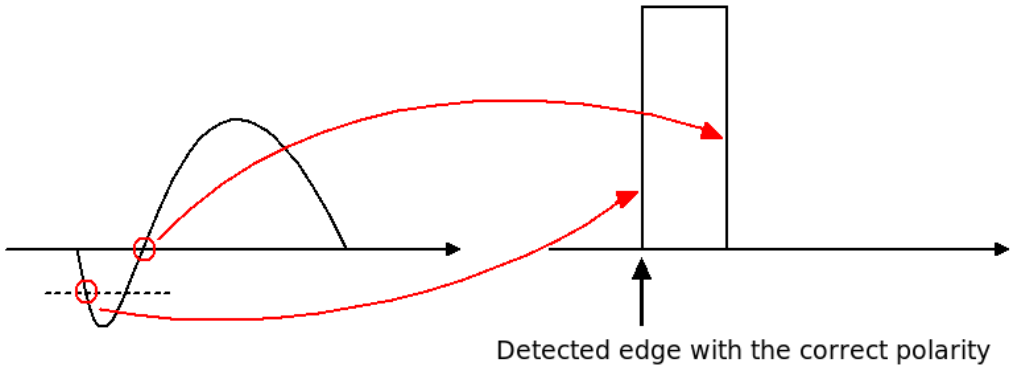
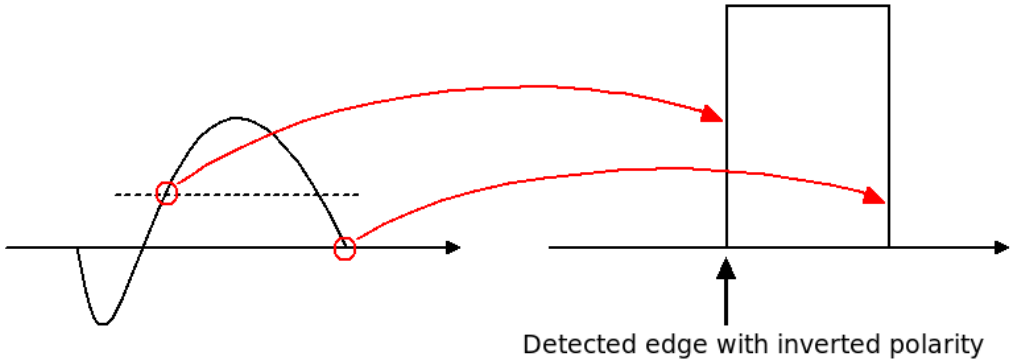


Figure 4.50: Measure of the mismatch of the fourth TAC buffer with respect to the first

The final time resolution Two main problems have been experienced in the test of the full front-end chain from the end of column. The first is linked to an issue in the asynchronous digital logic of the CFD. Due to this issue the corrected edge of the discriminator, corresponding to the zero crossing, is not accessible in the pixels of the matrix (see Fig 4.51 A). A partial solution is obtained by changing the pixel polarity configuration and the sign of the threshold in the discriminator. In this way it is possible to trigger near to the zero crossing on the leading edge of the bipolar signal, as shown in Fig. 4.51 B. With this patch the expected time walk is lower



(A)



(B)

Figure 4.51: (A) An issue in the asynchronous digital logic of the CFD causes the TDC to work on the wrong edge of the discriminator. (B) In this situation, better performance are obtained by changing the polarity bit and triggering on the leading edge of the bipolar signal overdrive

than the time walk on the leading edge of the preamplifier since the bipolar signal is sharper. However triggering on the leading edge of the bipolar signal re-introduces a time walk to the measure, but a simulation shows that in these conditions the time walk is still acceptable (the result is shown in Fig. 4.52).

The second problem is due to an interference that is injected in the substrate mainly by the clock drivers inside the chip. The interference is picked up by the GND_DET voltage reference at the input of the preamplifier. This voltage was initially provided by the DAC on board and filtered with a 100 pF capacitance. The noise injection has been qualitatively reproduced in simulation modulating the

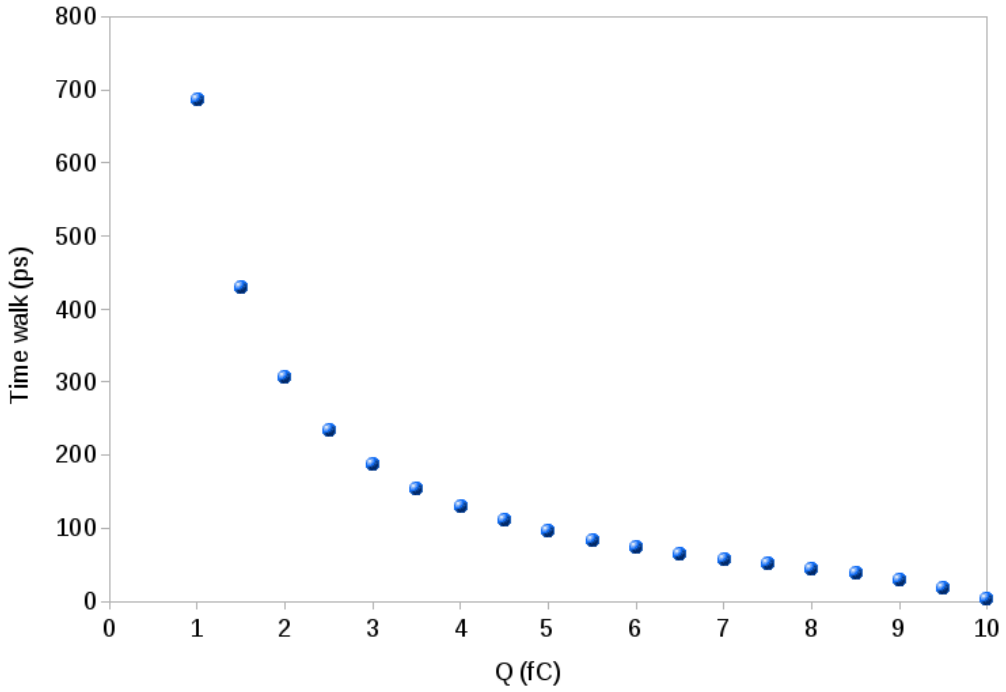


Figure 4.52: Time walk obtained in simulation by triggering on the leading edge of the CFD signal

reference ground with a 500 μV periodical noise at different frequencies. In the simulations the interference is picked up by the reference node of the preamplifier through an injection circuit composed by a voltage divider and a capacitor as sketched in Fig. 4.53. The simulation has been repeated for different frequencies of the interference and the result shows that a higher noise is expected at lower clock frequency, as it is clear from Figg. 4.54, 4.55 and 4.56. This fact can be explained in terms of charging and discharging effects on the input capacitance, which compensate each others at higher frequencies. However, the scope waveforms for different clock frequencies (see Fig. 4.57) show a lower noise at 128 MHz rather than at 160 MHz. This is due to the capacitance on the PCB filtering the reference voltage GND_DET which generates an oscillation at multiple frequencies of 80 MHz. The problem has been treated on the PCB and the resonance frequency has been eliminated by removing the filter capacitance. The noise effect is also visible in Fig. 4.58, where it is clear the dependency of the baseline modulation on the clock frequency.

The noise injection at the preamplifier input leads to the distorsion of the baseline and thus to an additional jitter due to the variation of the relative phase between the signal and the clock. The effect of the modulation has been evaluated before the removal of the filter capacitance on GND_DET. The phenomenon is clearly visible from Fig. 4.59, where a *Test Pulse* with different charge values has been feeded to the input of a pixel in the matrix bump bonded to the sensor. The same measure has been repeated delaying the *Test Pulse* in steps of 100 ps. Four clock cycles at 80 MHz have been explored and the total output times have been reconstructed from the coarse and fine time informations. The distorsion is more evident on lower signals since these have slower slopes. Height humps are visible in Fig. 4.59,

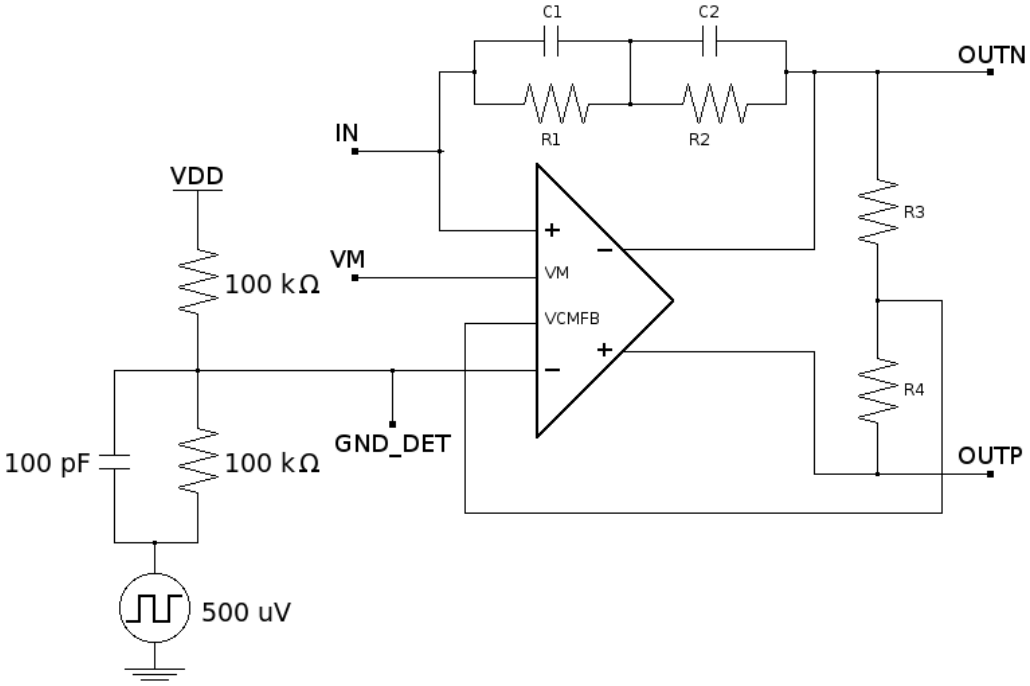


Figure 4.53: Schematic of the injection circuit used to reproduce the clock interference mechanism on GND_DET

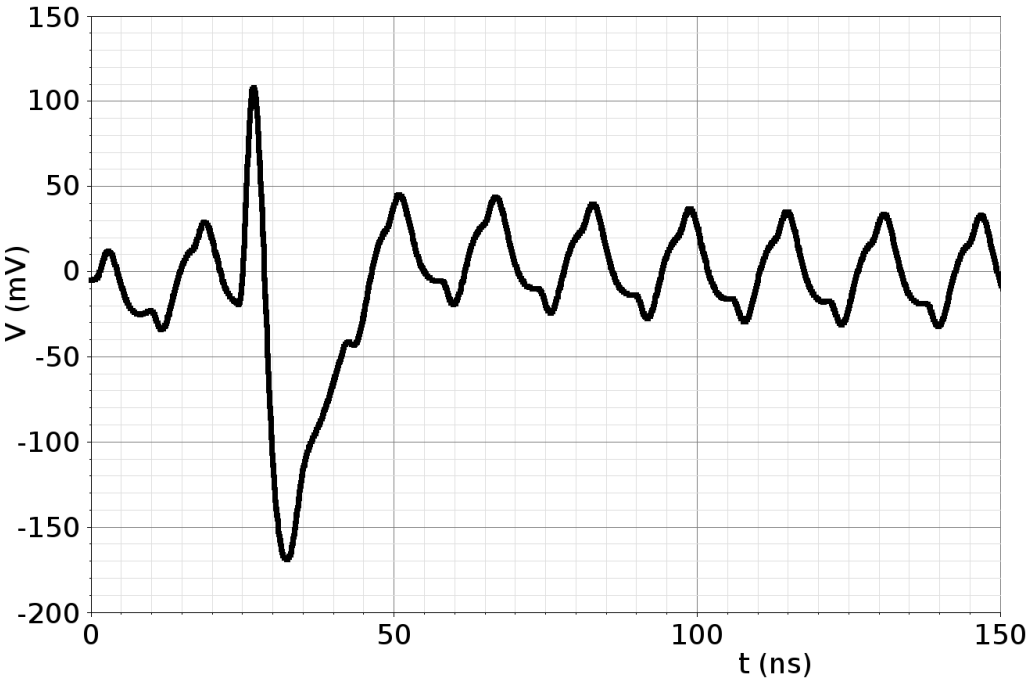


Figure 4.54: Result of the simulations of the clock interference on the front-end with the 500 μV noise on the reference ground at 62.5 MHz

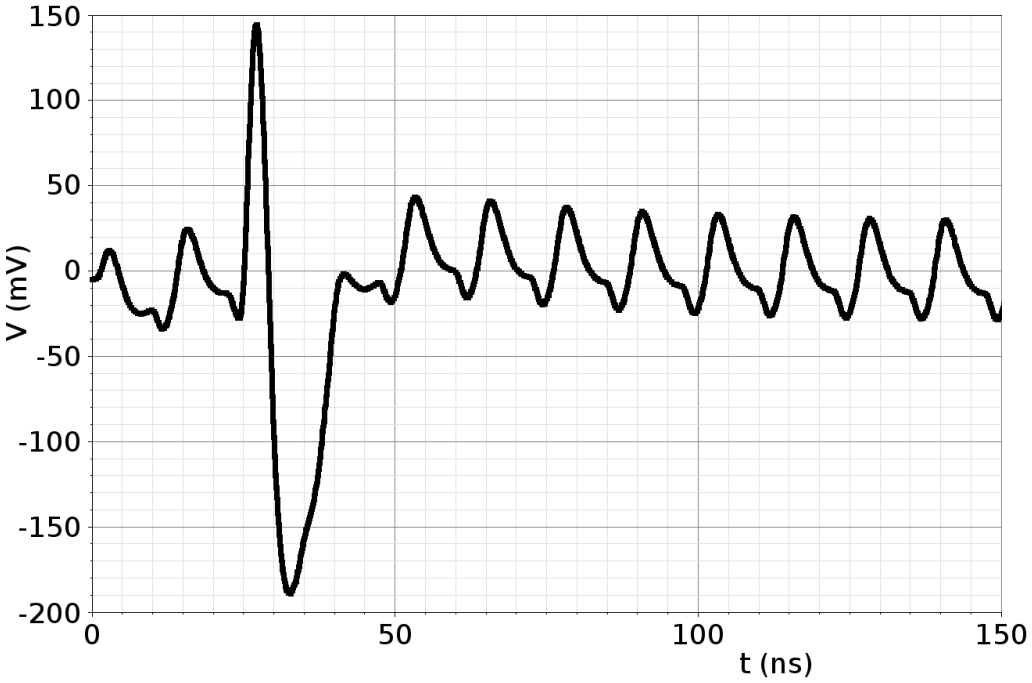


Figure 4.55: Result of the simulations of the clock interference on the front-end with the 500 μV noise on the reference ground at 80 MHz

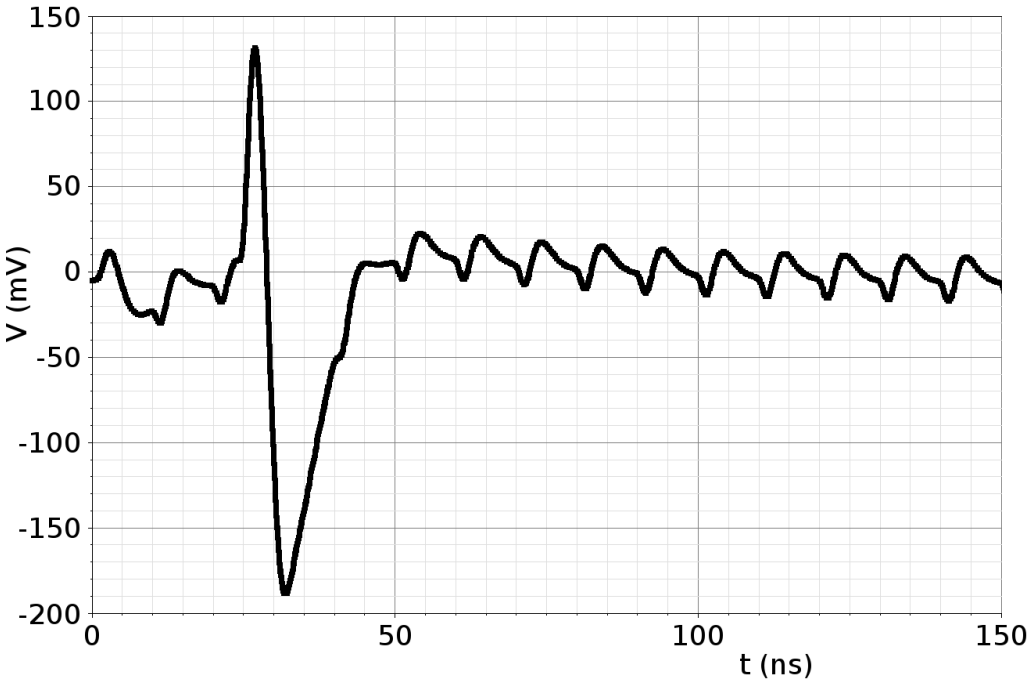
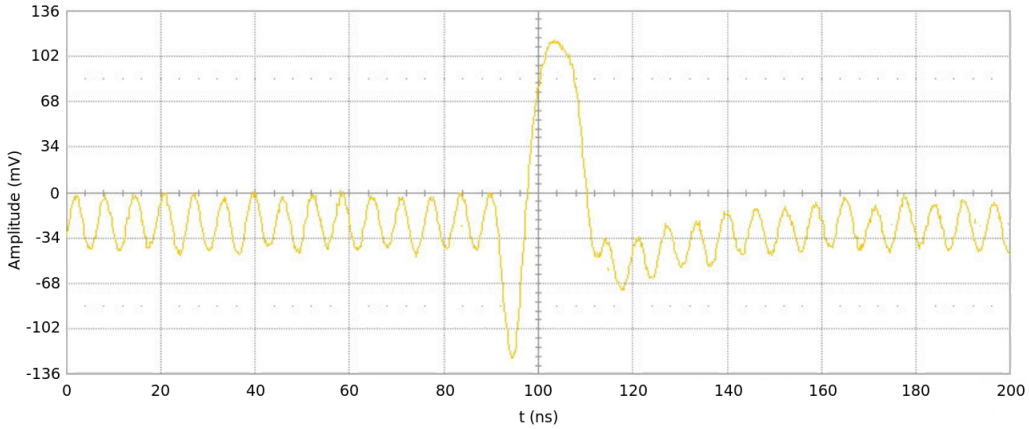
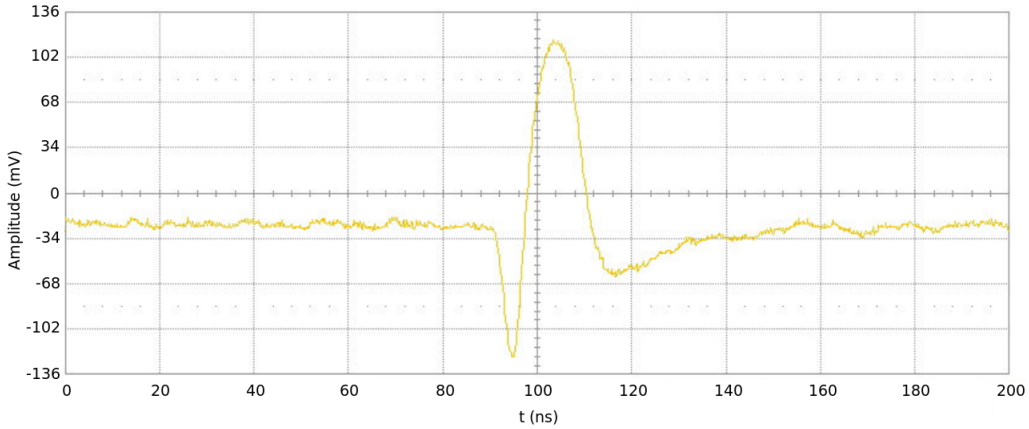


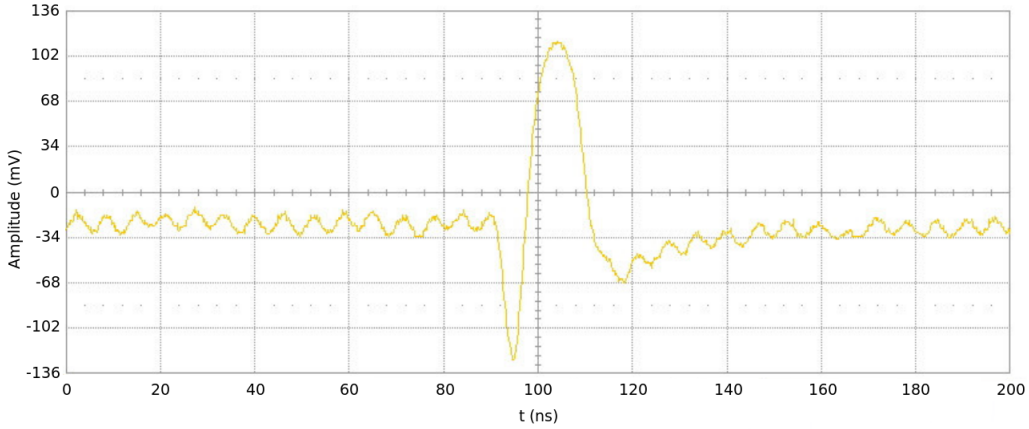
Figure 4.56: Result of the simulations of the clock interference on the front-end with the 500 μV noise on the reference ground at 160 MHz



(A)



(B)



(C)

Figure 4.57: Oscilloscope screenshots of the CFD output from the test pixel for a 3.5 fC input charge and for different values of clock frequency. Waveforms (A), (B) and (C) have been obtained with a clock frequency of 80 MHz, 128 MHz and 160 MHz respectively

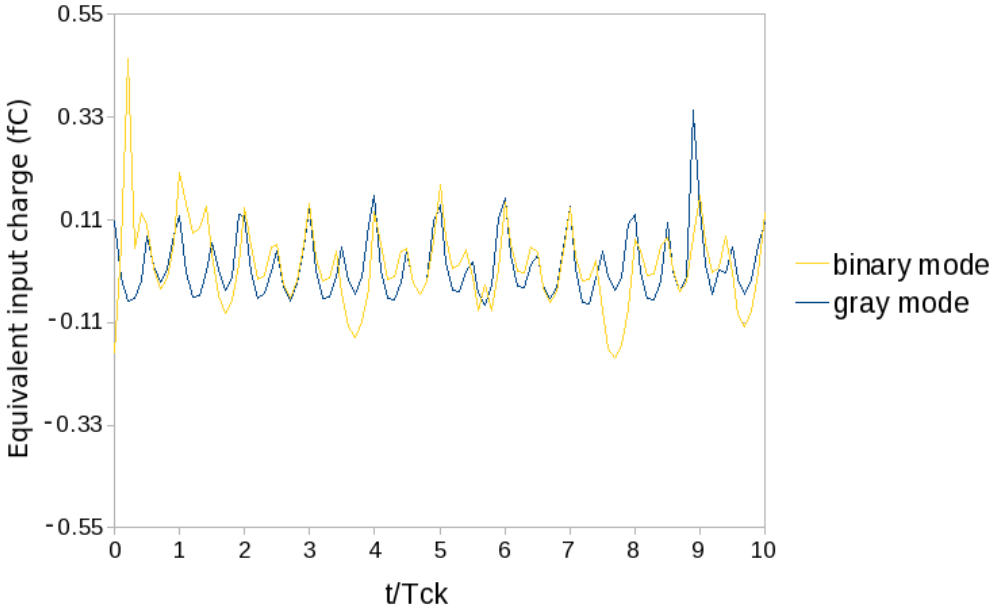


Figure 4.58: Measurement of the baseline noise at 80 MHz from a pixel in the matrix with the counter in gray and in binary modes

each corresponding to a clock raising or falling edge. The same measure after the removal of the capacitor on the GND_DET and other PCB optimizations, plotted in Fig. 4.61, shows a significant improvement of the performance of the circuit. The modulation leads to the measurement of a family of time walk curves depending on the phase between the signal and the clock. The time walk curves for different values of *Test Pulse* delay are plotted before and after the PCB optimization in Fig. 4.60 and in Fig. 4.62 respectively.

A beam test has been performed before the PCB optimizations (in the conditions shown in Fig. 4.59) in September 2010 at the T9 beam line at CERN PS East Area [74] [75]. The bench test is shown in Fig. 4.63. The PS provides a secondary beam in the momentum range between 1 GeV/c and 15 GeV/c. Due to noise injection, the time resolution measured on two boards biased at 1.5 V at 118 MHz resulted in 910 ps RMS which is highly higher than the specifications. The histogram of the difference of the times measured from the two boards is shown in Fig. 4.64. The expected resolution has been evaluated from the time walk curves measured in electrical tests in laboratory before the optimizations (see Fig. 4.60). At this scope a Montecarlo simulation has been run using Mathematica language. 10^4 charge events weighted on the Landau distribution are extracted from two boards (see Fig. 4.65). Each charge is associated in time to a time walk curve randomly chosen between the family of measured curves. The resulting times of the coincident events are compared and a time difference distribution is obtained. The RMS of this distribution divided by the square root of two (since the measure is performed on two boards) gives the expected time resolution. The result before the PCB optimization is 955 ps RMS, which is compatible with the measured 910 ps RMS of the beam test.

Clearly this result is highly inadequate for the experiment and for this reason

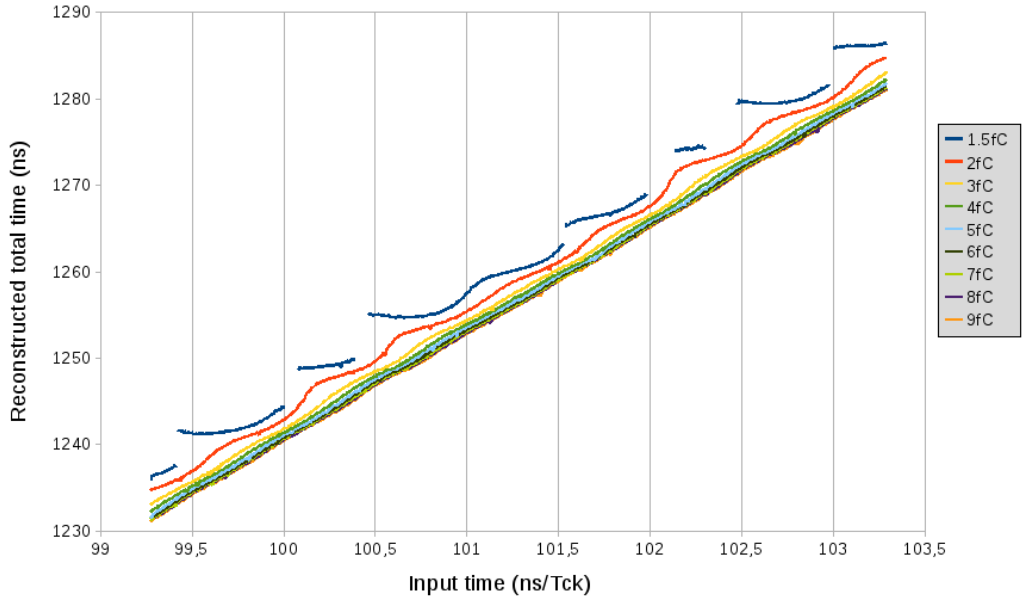


Figure 4.59: Reconstruction of the total output times from a pixel of the matrix for different values of input charge before the PCB optimization

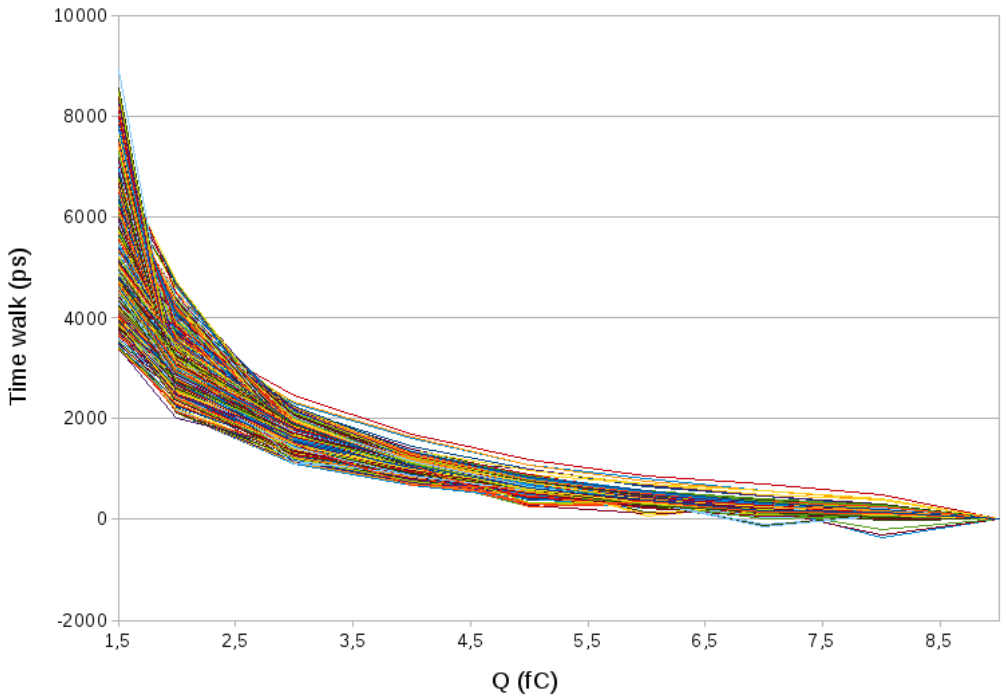


Figure 4.60: Time walk curves measured from a pixel in the matrix obtained for different values of *Test Pulse* delay before the PCB optimization

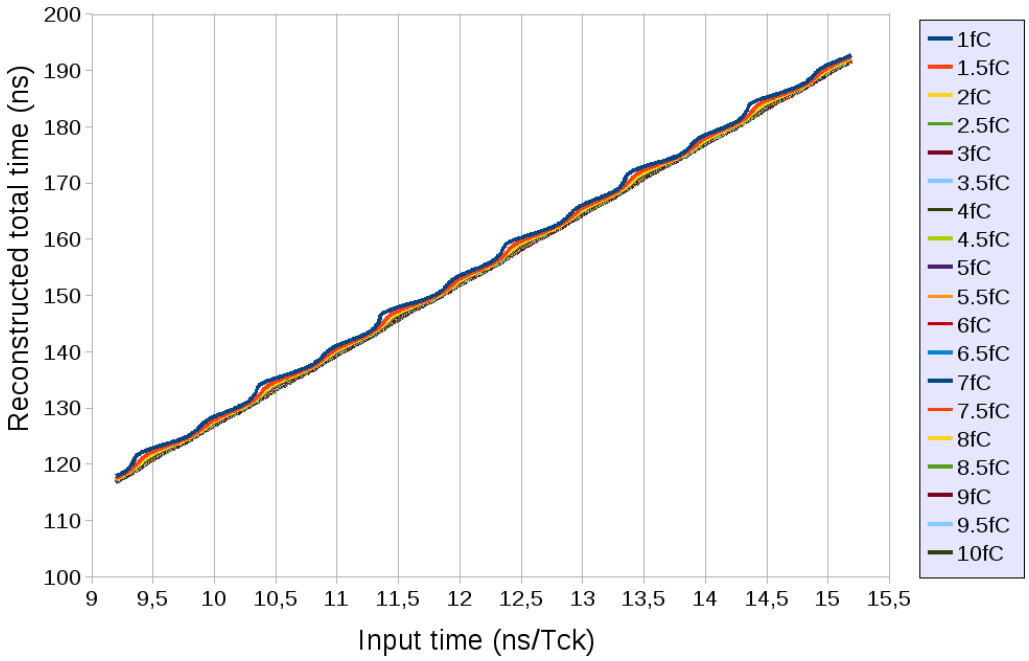


Figure 4.61: Reconstruction of the total output times from a pixel of the matrix for different values of input charge after the PCB optimization

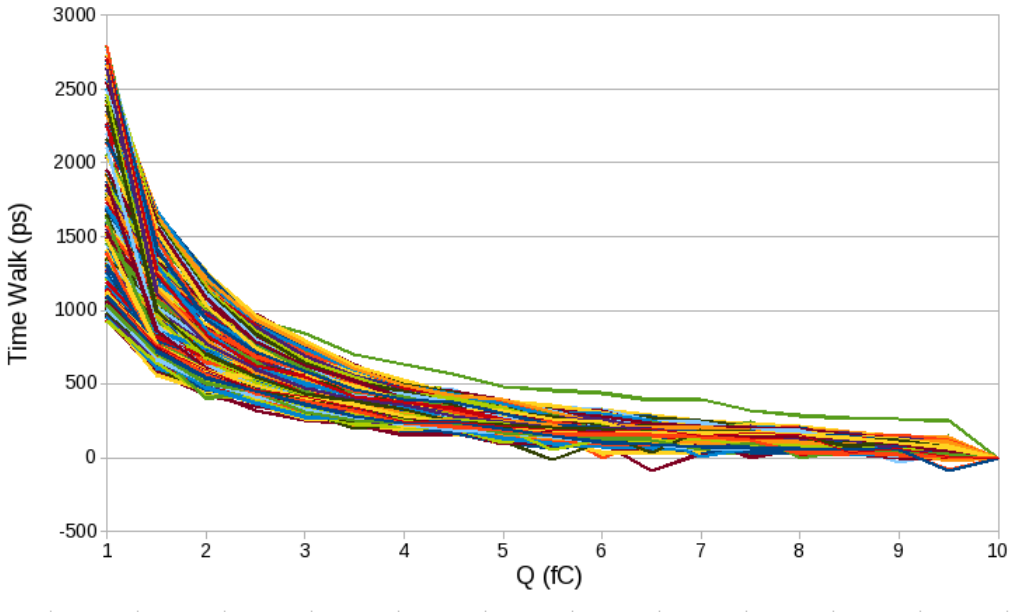


Figure 4.62: Time walk curves measured from a pixel in the matrix obtained for different values of *Test Pulse* delay after the PCB optimization

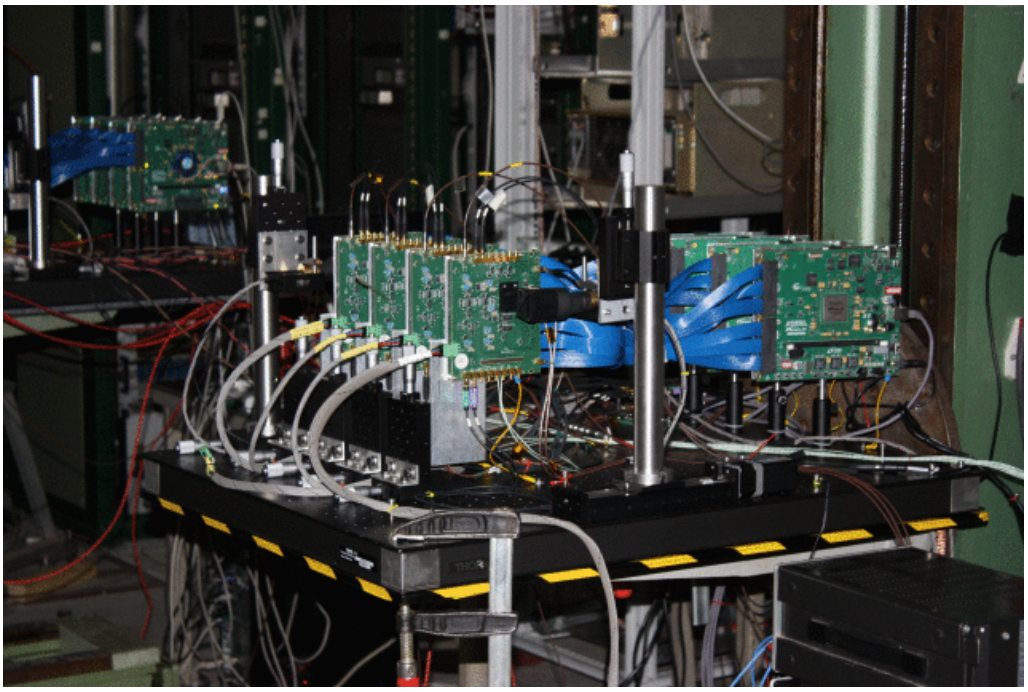


Figure 4.63: Test bench of the beam test at CERN PS

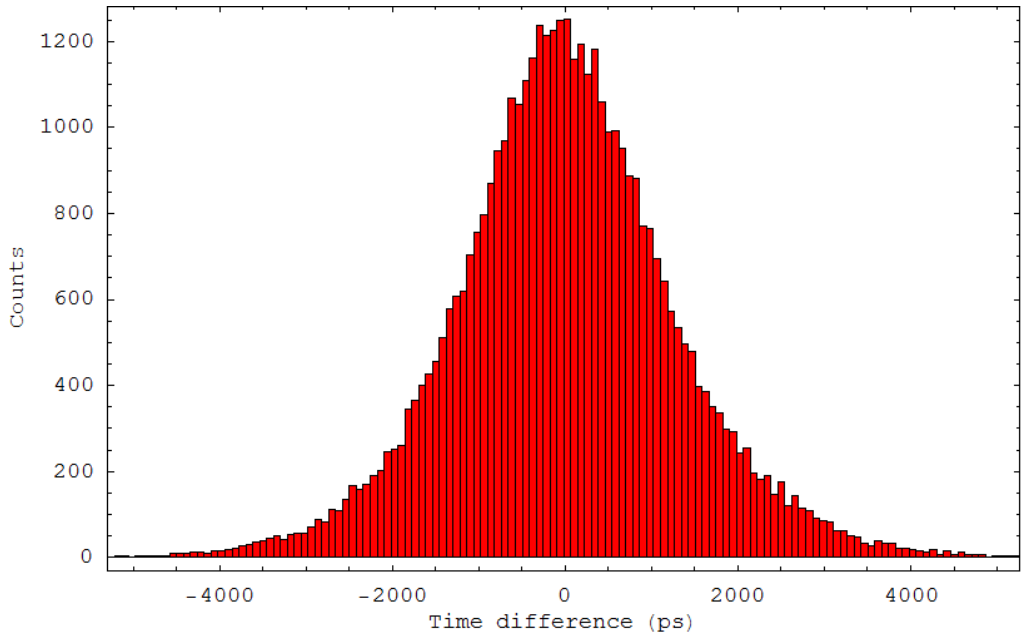


Figure 4.64: Time difference distribution of 43041 coincident events on two boards measured at the beam test

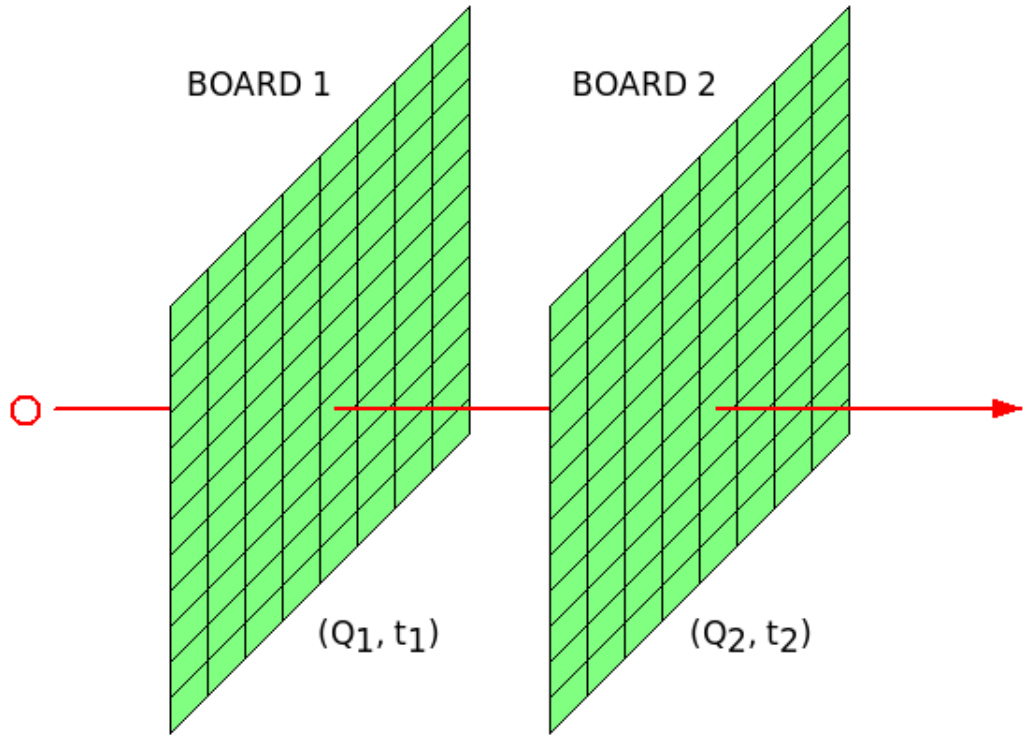


Figure 4.65: Principle of the Montecarlo simulation performed to evaluate the expected time resolution of the system

the effect of baseline modulation has been investigated after the beam test. As already discussed it has been discovered that the sensible node is the reference voltage GND_DET of the preamplifier. The presence of the filter capacitance at this node increases the noise pick up at the preamplifier input and introduces a resonance frequency at multiples of 80 MHz. The time walk has been measured after the removal of this capacitance and other PCB optimizations and the result, plotted in Fig. 4.61, shows an important improvement. The Montecarlo simulation performed after the optimizations using the family of time walk curves plotted in Fig. 4.62 gives a time walk of 184 ps RMS.

In order to evaluate the final time resolution expected after the optimizations, the jitter should be added to the time walk measured. In Fig. 4.66 it is illustrated the procedure followed to measure the jitter from the matrix pixels. A *Test Pulse* is feeded to the pixels and the number of events corresponding to a determined TDC bin are counted. The measure is repeated moving the delay of the *Test Pulse* in steps of 20 ps. When a whole TDC bin has been explored, the profile of that bin is reconstructed. Due to the electronic noise in the discrimination process, the resulting TDC bin boundaries are not sharply defined. This gives a direct measure of the jitter of the system. The measure has been repeated for different values of input charges and the jitter is slightly higher than the same measure performed on the text pixel (see Fig. 4.67). This difference is due to the fact that the test pixels are placed relatively far from the end of column and from the matrix. Moreover the digital part in the text pixels is reduced to the minimal logic needed to generate the start and stop signals for the TDC ramp. Thus it is normal that the matrix pixels

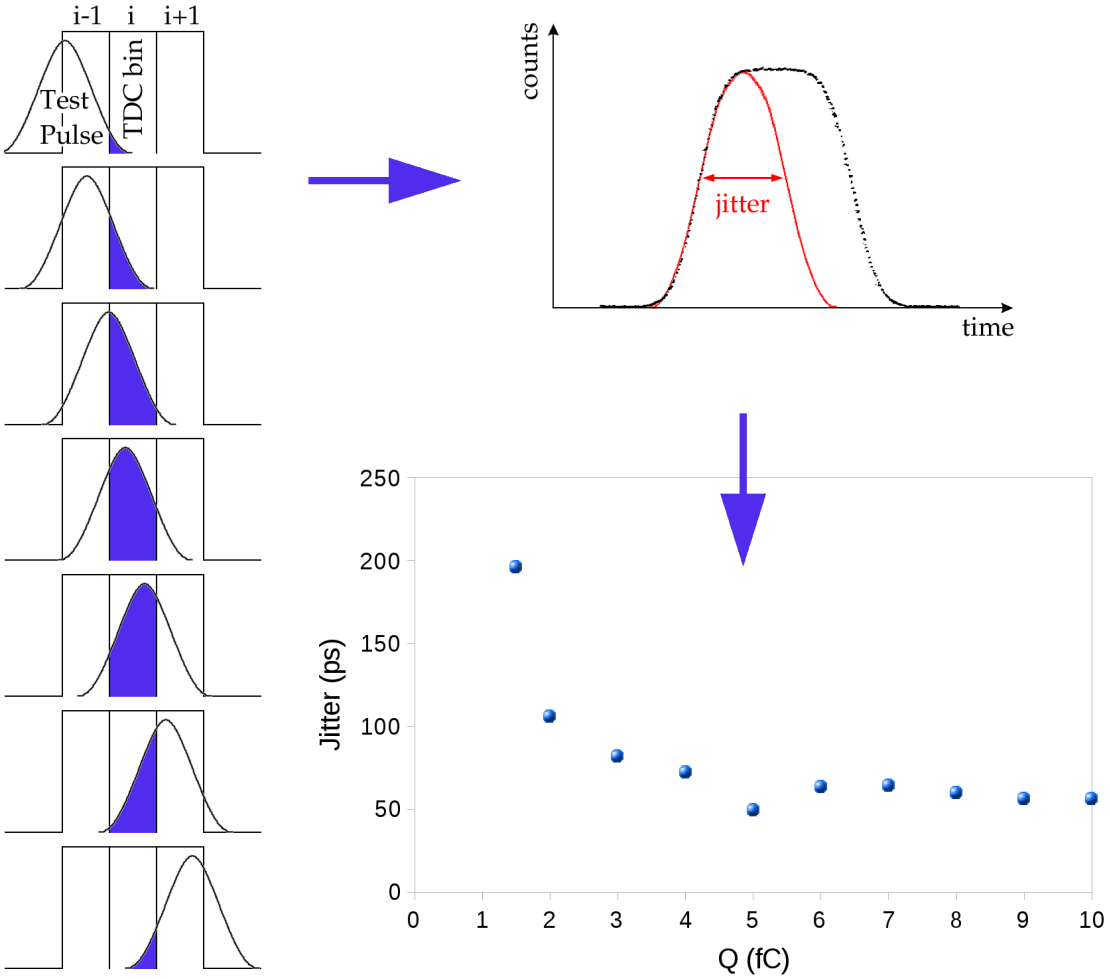


Figure 4.66: Jitter measured from a pixel in the matrix

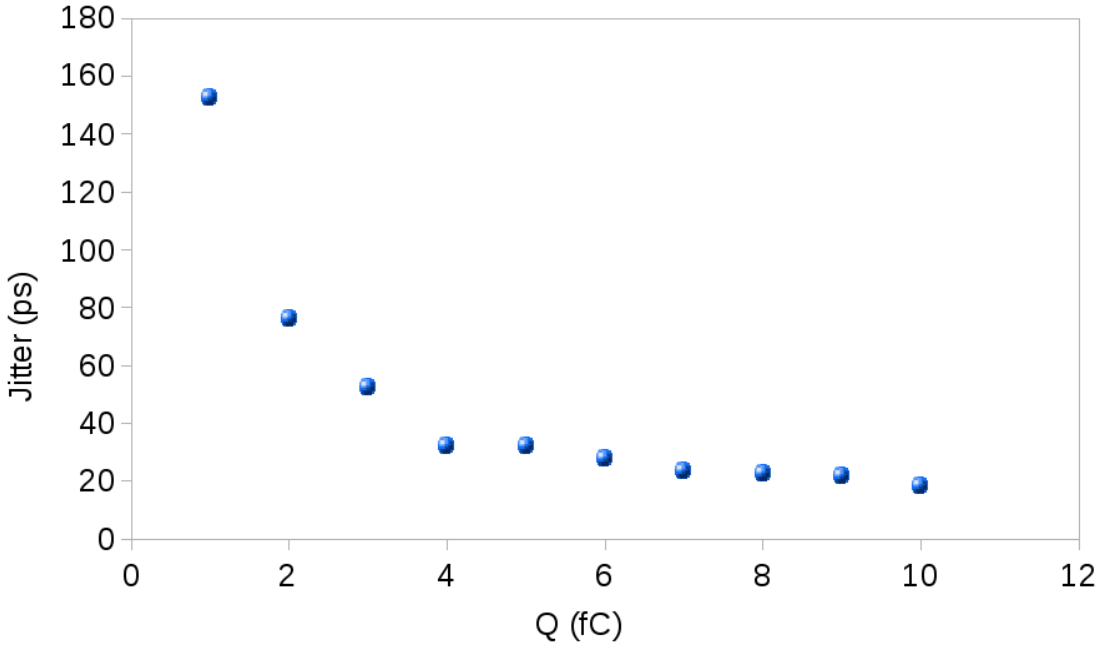


Figure 4.67: Jitter measured from the text pixel with a 80 MHz clock

are more noisy.

The 184 ps RMS time walk convoluted with the measured jitter leads to an expected final time resolution of 210 ps RMS. This value is at the limit of the specification, but considering that the chip is working in leading edge mode and in presence of digital noise it represents a very interesting result. However it has still not been confirmed by a second beam test. It should be noted that when this ASIC was produced the only method to separate the analog and digital circuit in the 0.13 μm IBM technology was the use of the BF MOAT layer. This consists of a high resistivity layer which allows to insulate the sensitive circuits. However in this prototype the area of the pixel was completely filled by the front-end and there were not space enough to insert the BF MOAT. With the recent new specifications of the experiment the event rate has been halved. This fact allows to reduce the number of buffers in the TDC and in the digital logic in the pixel. Since the TDC fills almost one fourth of the pixel area and the digital registers are Hamming encoded, the area released would be enough to insert the BF MOAT. Moreover the IBM recently developed a new separation layer, called T3, which consists of a deep n-well and allows to separate the analog and digital substrates. The use of the BF MOAT and of the layer T3 would give, in a future prototype, the insulation needed to cope with the substrate noise injection.

Chapter 5

A new front end ASIC with improved pulse shape rejection

As discussed in Section 1.4.4, signal shape variation can affect timing. Electrical field border effects in the pixel and statistical fluctuations in the charge released along the sensor are responsible for peaking time variations (see Figg. 5.1 and 5.2).

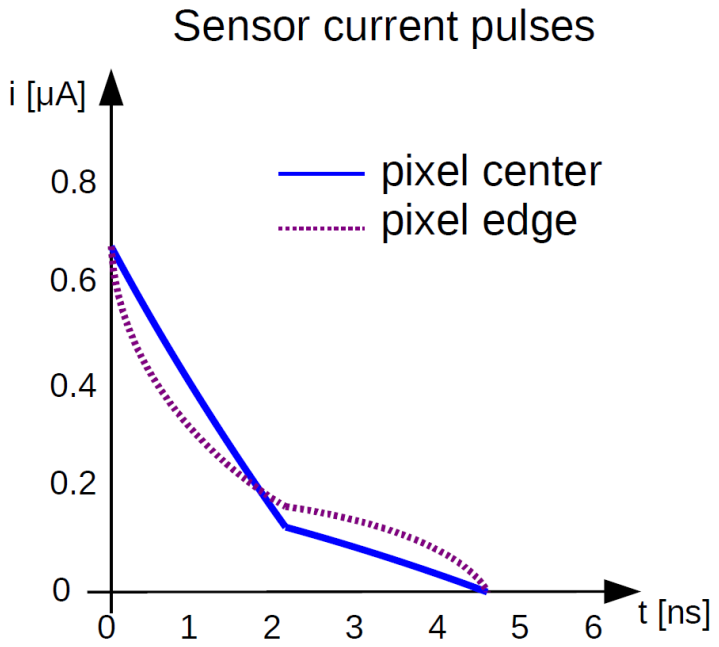


Figure 5.1: Signal shape variations due to border effects

On the basis of the acquired experience from the first prototype the full analog front-end has been optimized. The new design aims to improve the time precision by minimizing the sensitivity of the CFD to signal shape fluctuations. As shown in Section 1.4.4, this fact involves the necessity of having a shorter delay and consequently an arming discriminator to enable the zero crossing one (see Fig. 1.28 B) [38]. Moreover a 3 bit amplitude measurement is forseen. It has the twofold goal of flagging an event with very high charge deposition, due to heavy particles, and to provide further information useful to compensate the time walk.

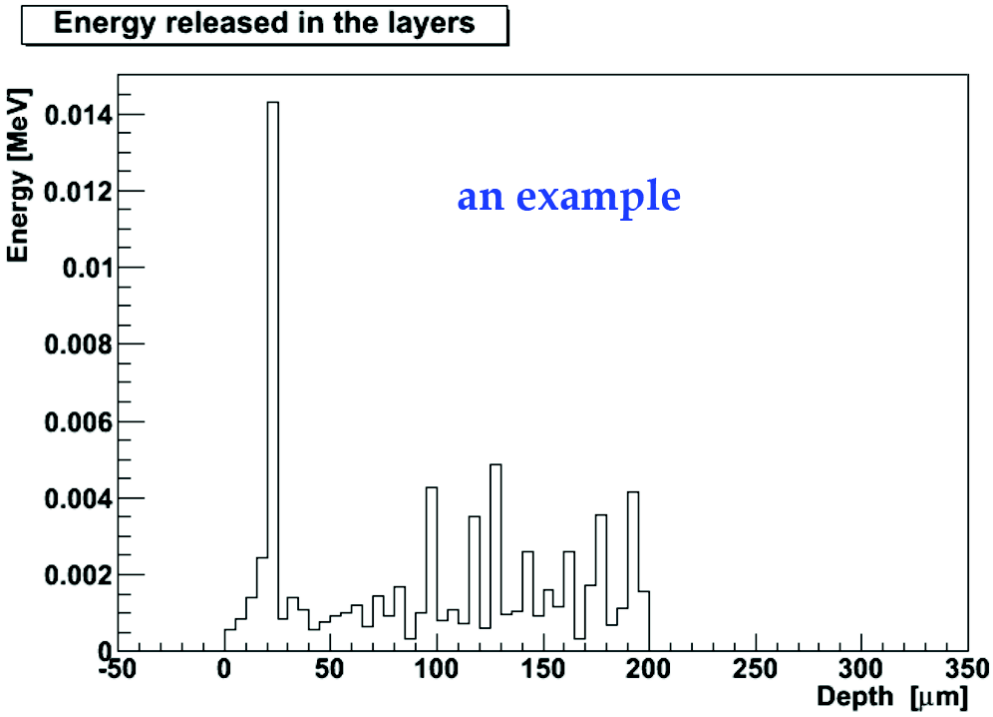


Figure 5.2: Charge straggling along the sensor

5.1 The CFD filter

The schematic of the CFD is the same sketched in Fig. 4.20, but the value of the passive components have been changed in order to have slightly more than one half of the delay with respect to the previous design. Besides a shorter delay, the CFD optimization requires a an accurate control on the parasitic capacitors and of the process variations which can change the transfer function by slowing down the signal and by increasing the delay. Thus the value of the programmable capacitors have been optimized in order to maintain the zero crossing at the same value in the typical mean and in the process corners. At this scope the process variations of the resistor and capacitor values, their parasitics and the leakage current of the switches use to program the filter have been considered. The details of this calculations can be found in Appendix B. The optimized values are reported in Table 5.1 and the layout of the CFD in shown in Fig. 5.3.

To evaluate the performance of the new CFD design in correcting both the time walk due to amplitude variations and the jitter induced by statistical fluctuation on the signal shape, an input data sample as similar as possible to the reality must be used. This fact implies a considerable number of simulations and thus the need of an automated test bench. At this scope 200 files representative of the input signals have been generated considering the charge release process in a 200 μm thick silicon sensor. This includes the Landau of the experiment, the electrical field border effects and the statistical fluctuations in the charge released along the sensor (see Fig. 5.4). Finally the files have been feeded to the circuit using the Ocean programming Cadence tool. Details about the Montecarlo simulations with Ocean can be found in Appendix D.

Component	value
R	629.1 Ω
R_f	6R
R_p	R
C	7.64 fF
C_a	76.18 fF
C_b	166.18 fF

Table 5.1: Values of the passive components of the CFD filter optimized for signal shape rejection

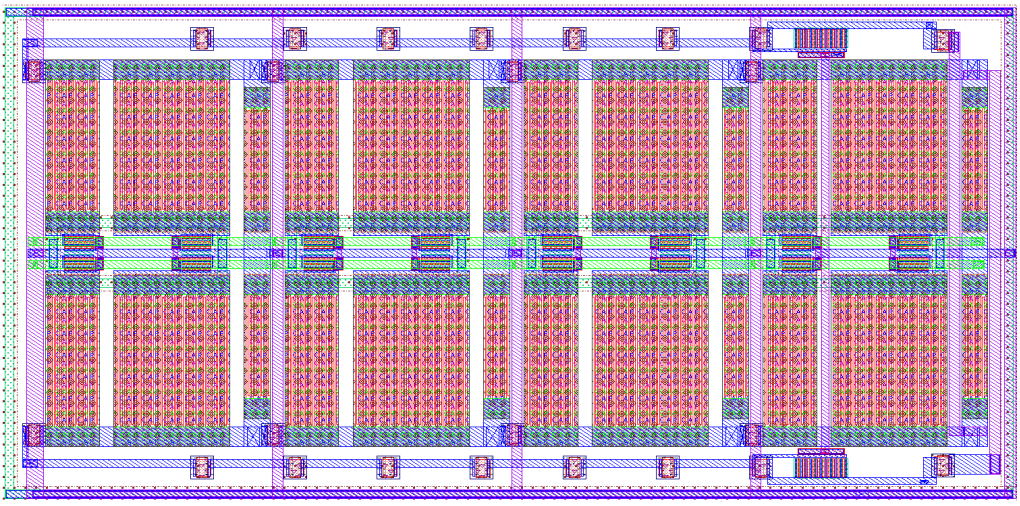


Figure 5.3: Layout of the optimized CFD

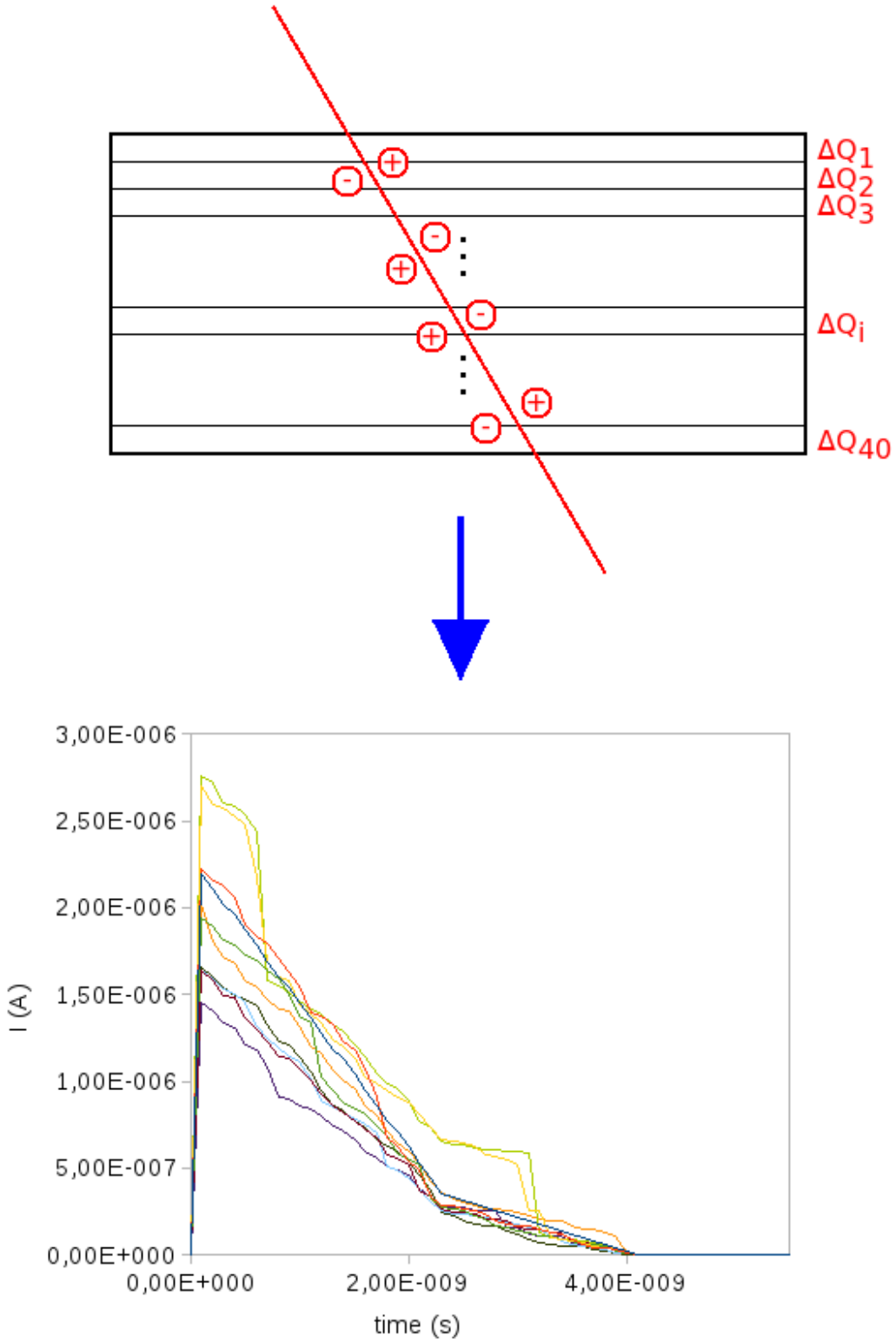


Figure 5.4: Generation of input signals for Montecarlo simulation. The sensor has been divided in 40 slices. The resulting current pulses differ for amplitude and shape due to statistical fluctuations in the charge release process

5.2 The preamplifier

The preamplifier shown in Fig. 4.19 has a fully differential architecture which allows a better rejection of the common mode noise due for example to the digital logic in the pixel. However the limited power budget do not allow to implement an optimal fully differential architecture and the required gain is obtained applying the feedback only on one polarity of the signal. This solution re-introduces a single ended structure and cancels in part the advantages of the differential topology. Moreover this preamplifier is composed by a reactioned second order amplifier, thus its transfer function has two poles and the connection with the detector may be critical for the stability. Finally the absence of the feedback network on the reference voltage makes the biasing of this node difficult. For these reasons it has been preferred to return

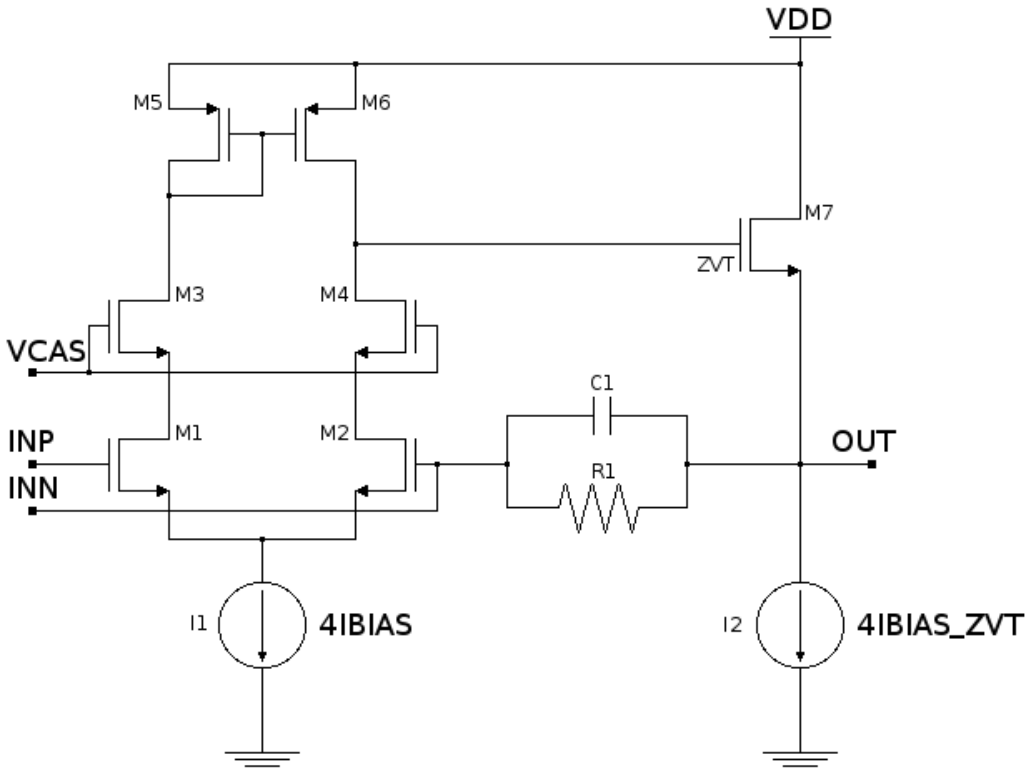


Figure 5.5: Schematic of the first stage of the preamplifier

to a more conventional two stage configuration. The first stage, shown in Fig. 5.5, is a one pole single ended amplifier which ensures a good stability. The single ended to differential conversion is performed in the second stage. This stage as well is a reactioned second order amplifier but in this case the coupling with the previous stage is performed inside the chip in controlled conditions. The reference voltage for the second stage is given by a replica circuit, shown in Fig. 5.6, made four times smaller in order to reduce the impact on area and on power consumption. The layout of the first stage of the preamplifier and of the replica circuit is shown in Fig. 5.7. A differential to single ended solution has been preferred with respect to a fully single ended architecture (as the one used in the first prototype shown in Fig. 4.4) since

it can be used with both p-in-n or n-in-p detectors. However the reference voltage should be as coupled as possible to the ground of the preamplifier to prevent the injection of noise on this node. On the contrary, the fully single ended configuration does not need a voltage reference but its output DC level allows to use it only for signals of a pre-established polarity.

The second stage of the preamplifier (Fig. 5.8 and 5.9) converts the signal from single ended to differential and provides the further amplification to reach the total gain of 95 mV/fC. It has been also provided of a programmable resistor to increase its gain of a factor two to face the effect of detector deterioration. In fact due to high radiation exposure the charge collected in the sensor decreases. The layout of this stage is shown in Fig. 5.10.

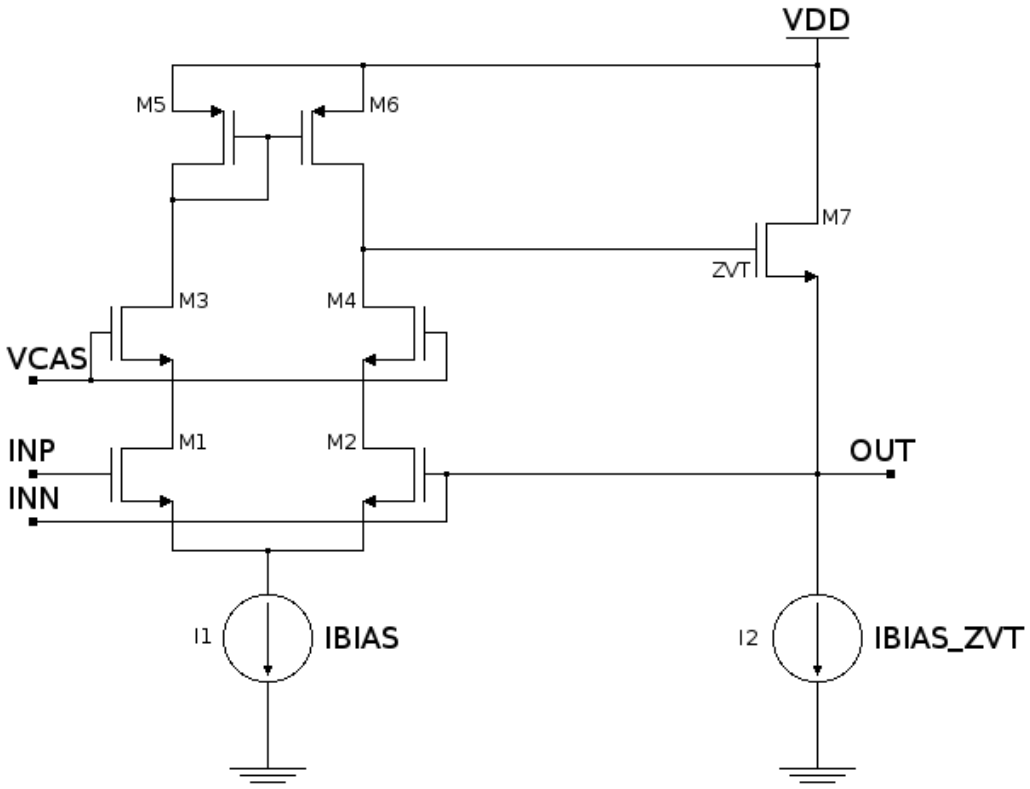


Figure 5.6: Replica circuit of the first preamplifier stage

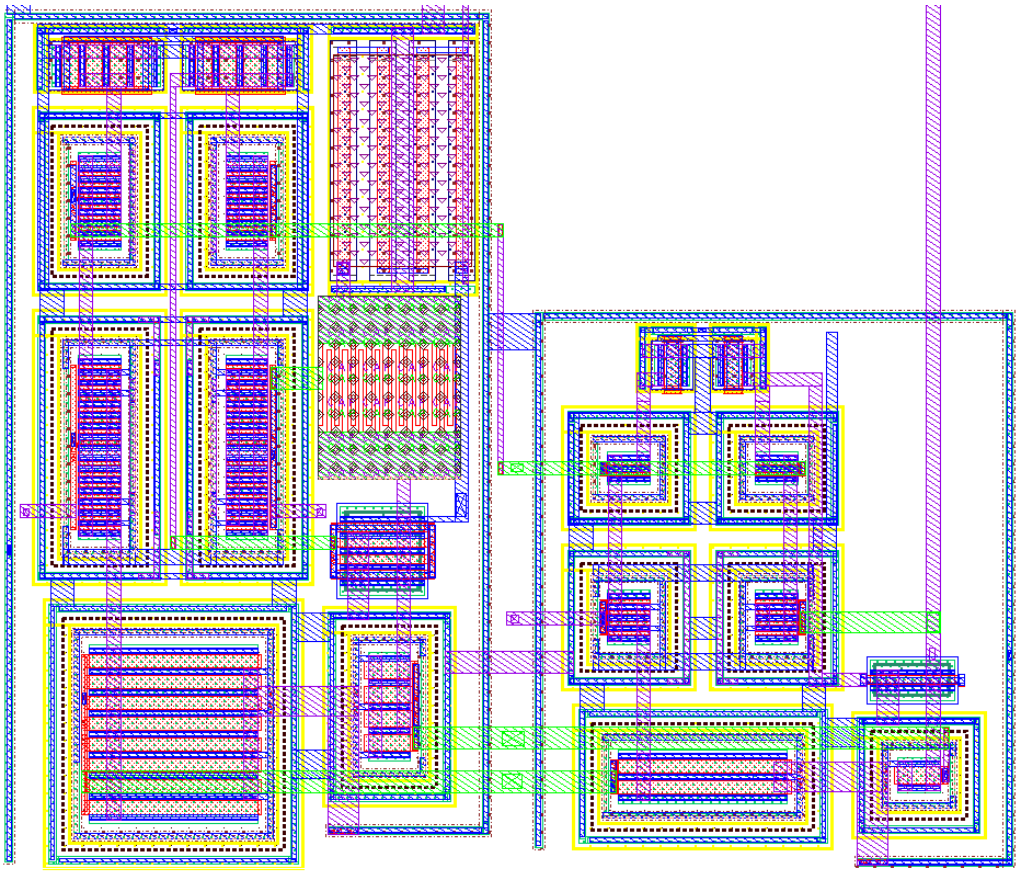


Figure 5.7: Layout of the first stage of the preamplifier with the replica circuit

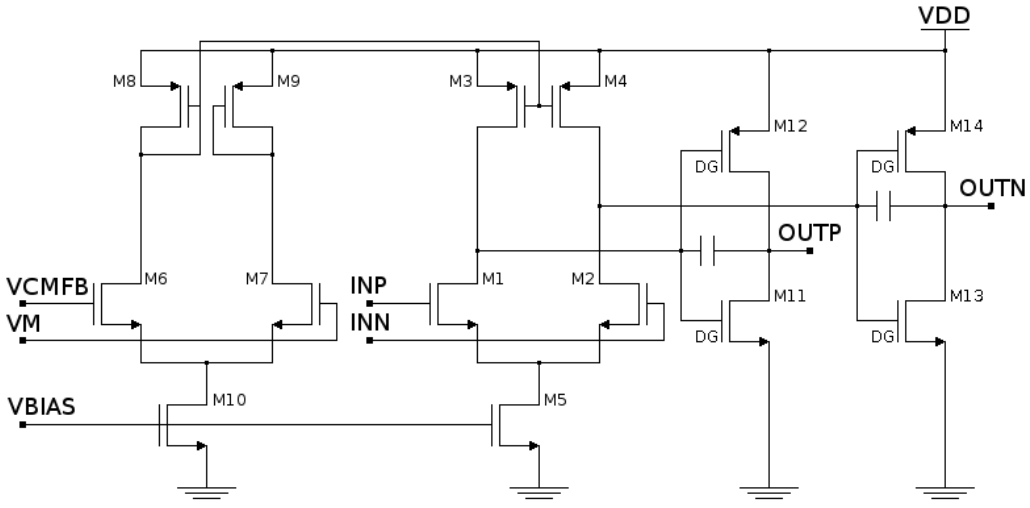


Figure 5.8: Schematic of the op-amp of the second preamplifier stage

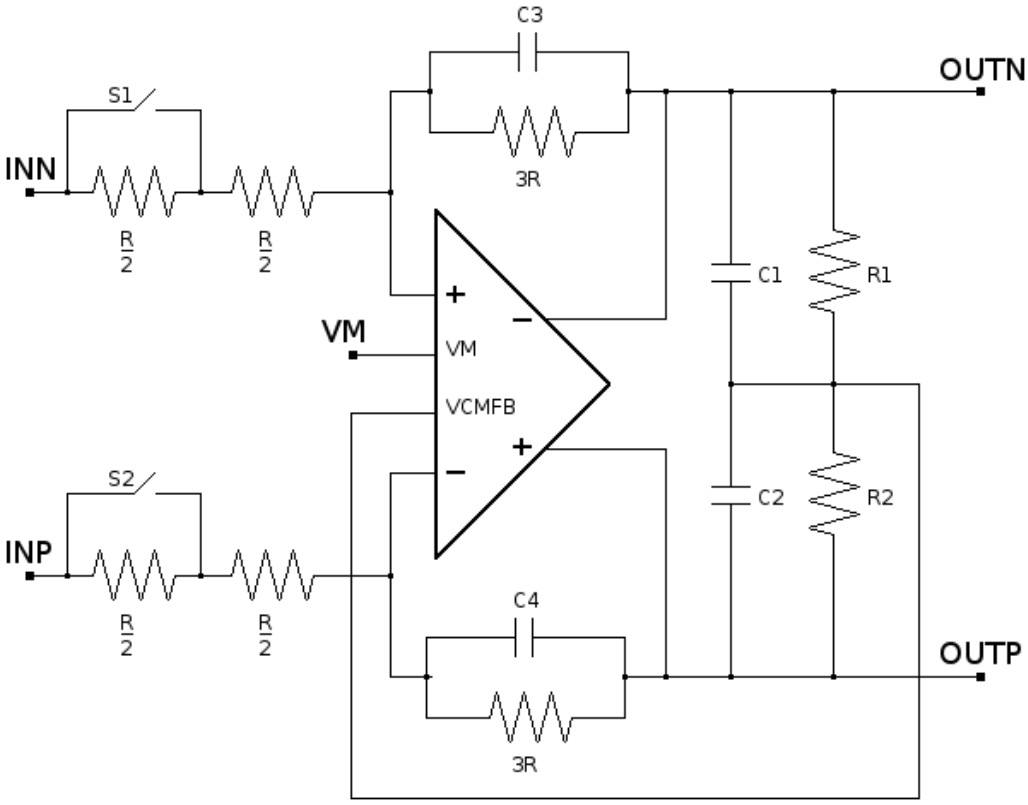


Figure 5.9: Block diagram of the second stage of the preamplifier

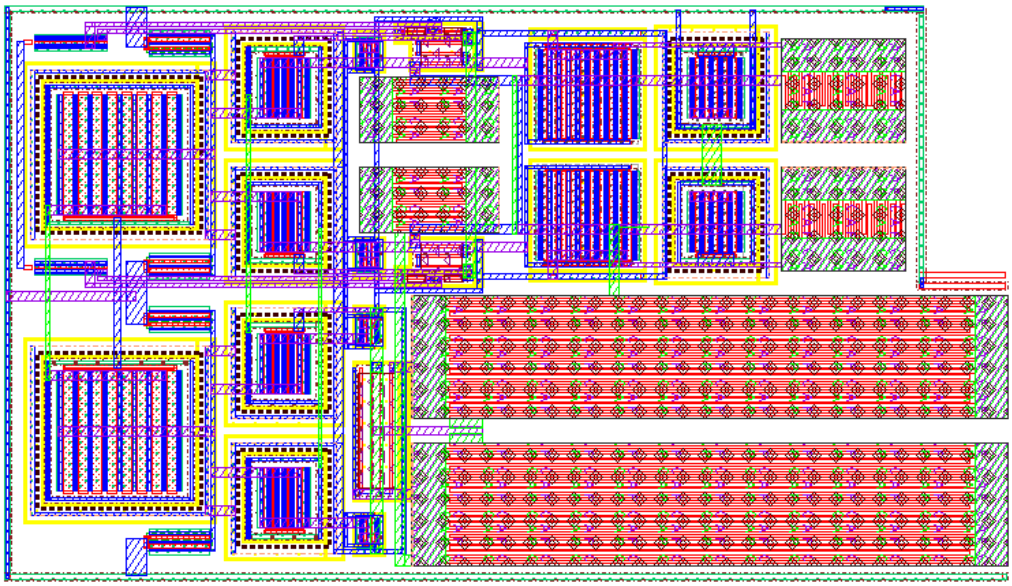


Figure 5.10: Layout of the second stage of the preamplifier

5.3 The CFD amplifier output stage

The amplifier stage following the CFD filter is based on the same principle used in the previous prototype. It is composed by two cascaded differential gain stages with resistive loads. In the previous design the differential pair of the second stage was made smaller to improve the slew rate. However better results in term of time walk have been obtained optimizing the dimensions of the resistors and of the transistors. The current in the first stage has been halved and consequently the load resistor doubled resulting in a factor $\sqrt{2}$ higher gain. On the other hand the current in the second stage is increased of a factor $\frac{3}{2}$ leading to an overall gain slightly higher than in the old version. This allows to have the main amplification in the first stage, which is less sensible to slew rate effects since the output signal is smaller. On the other hand the higher current in the second stage improves the slew rate and allows to use bigger transistors at its input without degrading the performance of the amplifier.

The dynamic offset compensation circuit is the same shown in Fig. 4.21. The dimensions of the transistors have been increased to bias it with a higher currents, improving its compensation capability (see Fig. 5.11). It has also been necessary to make the capacitor bigger to maintain the stability of the circuit. The improvement of the offset compensation capability allows to remove the leakage compensation circuit, since the offset introduced by the leakage is compensated directly at the output of the CFD.

The complete stage is shown in Fig. 5.12

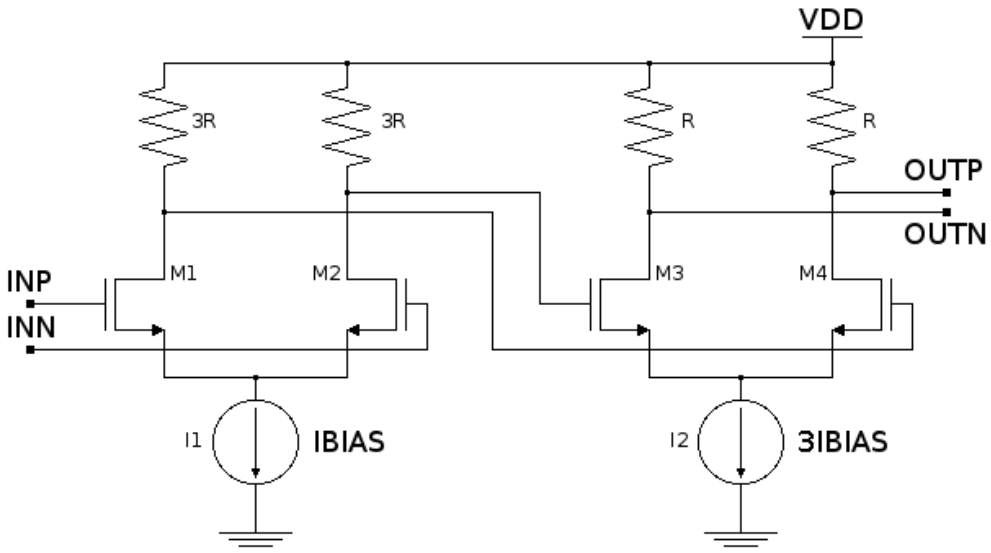


Figure 5.11: Optimized CFD amplifier output stage

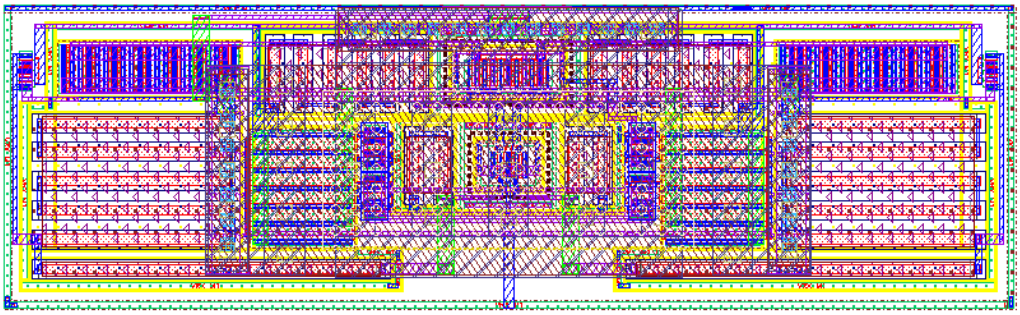


Figure 5.12: Layout of the CFD amplifier output stage with dynamic offset compensation circuit

5.4 The discriminators

The discriminator has been changed with the design shown in Fig. 5.13, which has better performance. The same scheme has been used for the arming and for the zero crossing discriminators. It is composed by a first stage, where the threshold is applied through the source followers M5 and M6, and by an amplifying stage. The two amplifiers use a cascode configuration to improve the gain and a resistive load has been chosen for a faster response. The clipping transistors M8 and M9 limit the swing at the output of the first stage by preventing from the saturation of the second and thus improving the speed of the circuit. Finally the output digital pulse is generated by the inverters M17-M24.

This design is not symmetrical and is faster in one direction than the other. Thus, to make it possible to work with both polarities at the maximum of its potentialities, the thresholds and the signals are applied as shown in Fig. 5.14. When *POL* signal is high, switches S2-S3 and S6-S7 are closed and S1-S4 and S5-S8 are open. The negative output of the preamplifier and of the CFD are connected respectively to the negative input of the arming discriminator and of the zero crossing one and viceversa for the positive inputs. On the contrary, when the control signal is low, the inputs of the discriminators are inverted. In this way it is possible to program the discriminators in such a way that they receive always a signal of the same polarity at their input. Switches S9-S12 apply the threshold cancellation to the zero crossing discriminator. When the output of the arming discriminator is high S10 and S12 are closed and the threshold is applied to the circuit. When a signal arrives the *TH_EN* signal goes down and switches S9 and S11 are closed. In this case a common voltage is applied to the zero crossing discriminator and the threshold is cancelled.

Fig. 5.15 shown the discriminator layout.

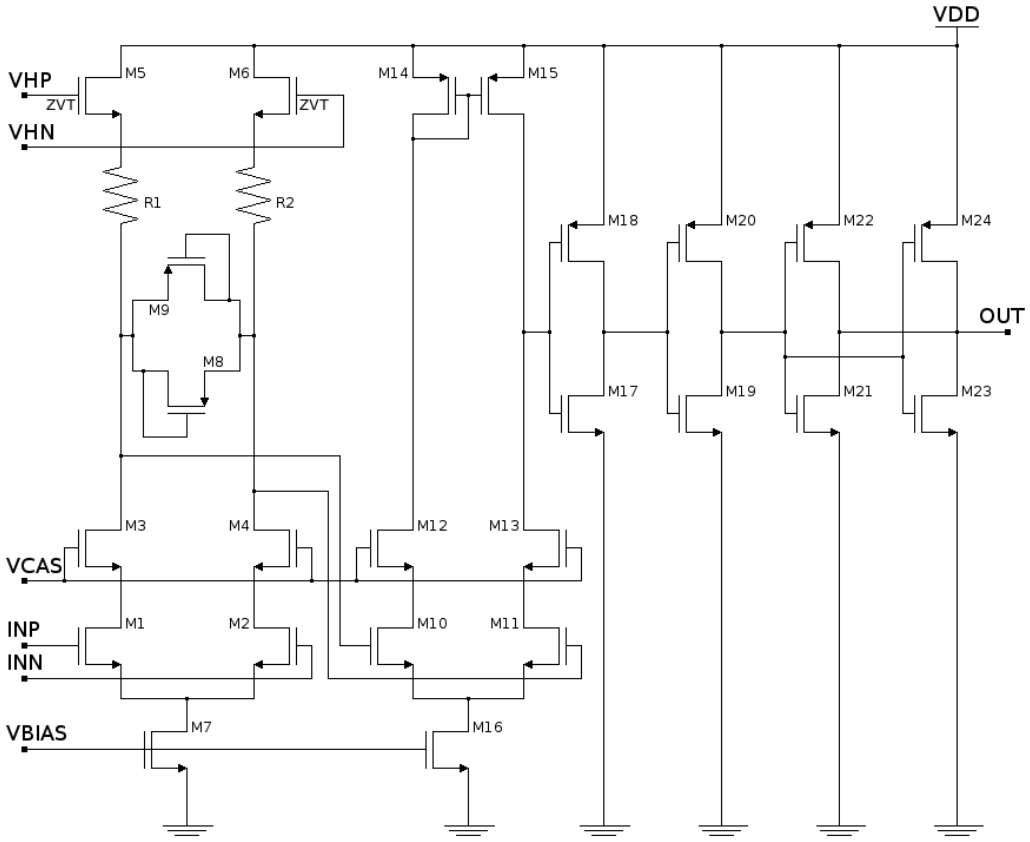


Figure 5.13: Schematic of the discriminator used both for the arming and for the zero crossing

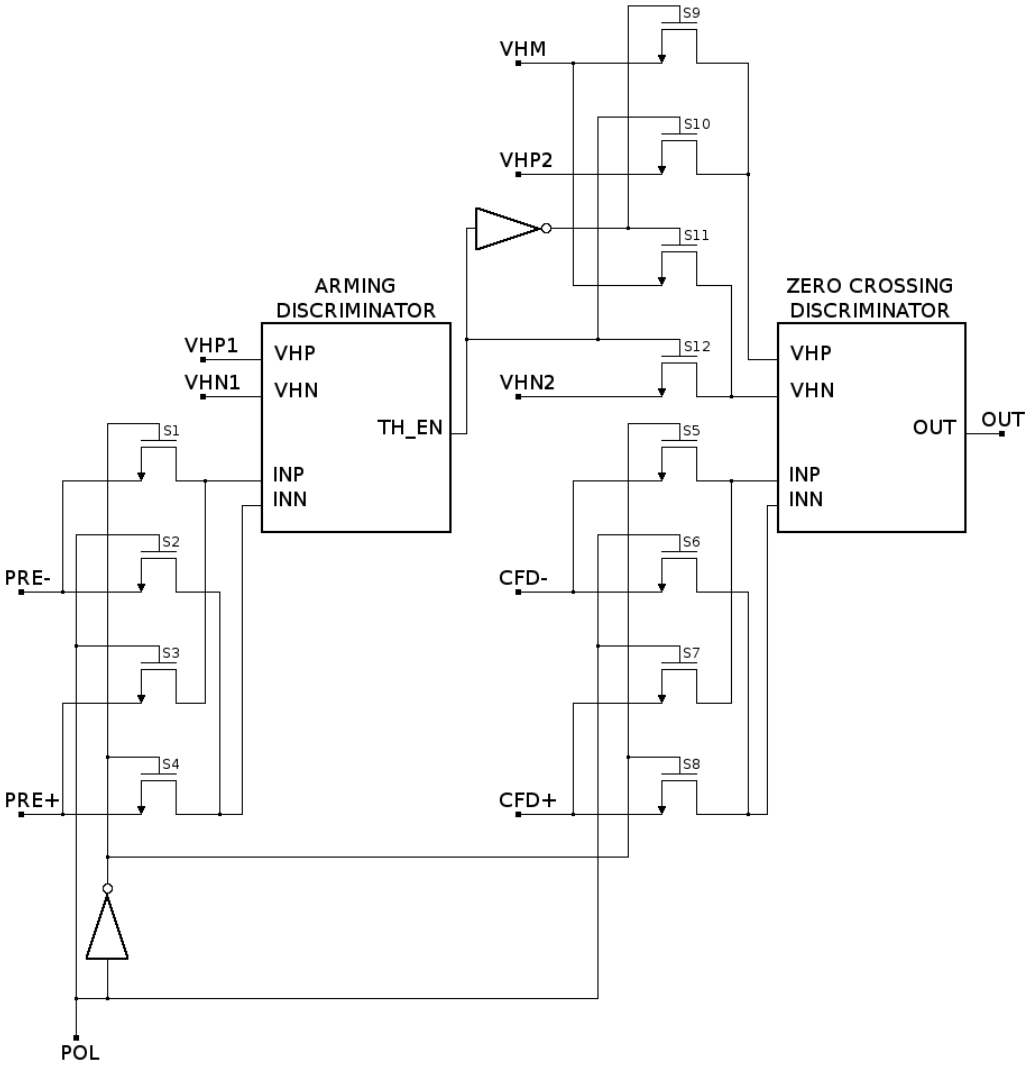


Figure 5.14: polarity selection in the discriminator system

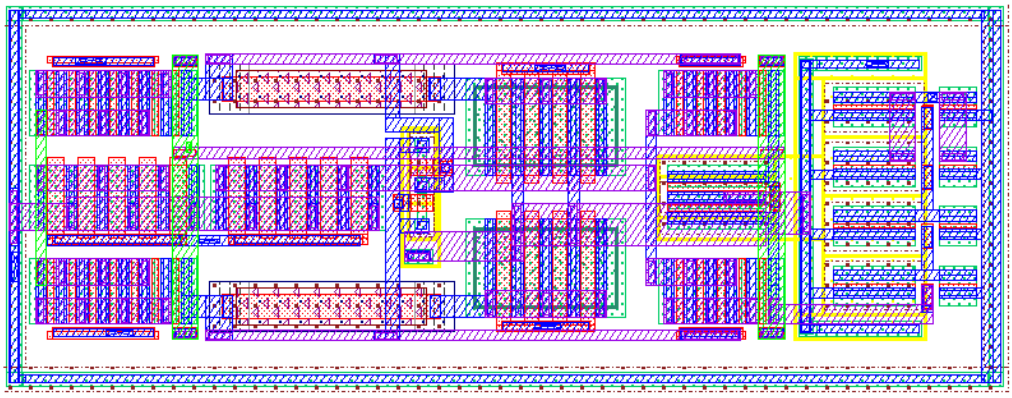


Figure 5.15: Layout of the discriminator

5.5 Simulation results

The layout of the described architecture has been designed and simulated. Simulation results of the single blocks and of the overall analog chain are now discussed in detail.

5.5.1 The linearity and the noise

The preamplifier output for a 2.4 fC input charge is plotted in Fig. 5.16. It has

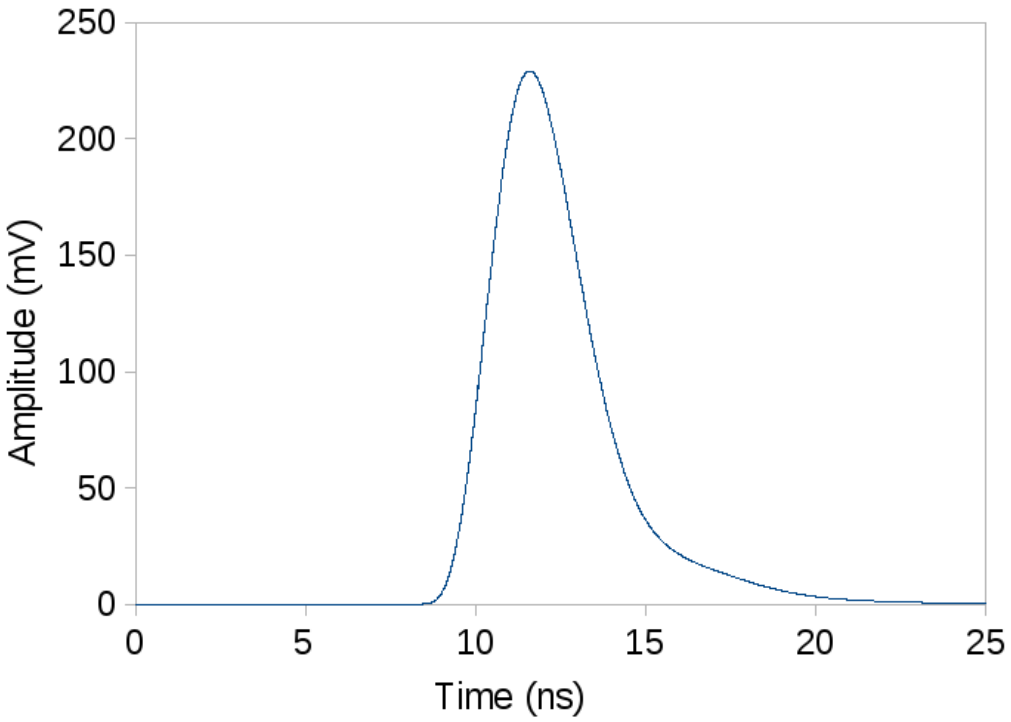


Figure 5.16: Output of the preamplifier for 1 MIP

a gain of 95 mV/fC and a peaking time of 3 ns. Fig. 5.17 shown that the linearity of the preamplifier degrades for charges higher than 6 fC. However, for this application, where the vast majority of the input charge ranges between 1.5 fC and 8 fC, the linearity of the preamplifier is not the primary concern, as far as it is sufficient to keep the overall time resolution low. In this perspective other factors, such as the gain and the speed of the preamplifier, are more relevant.

The ENC is 308 e^- and Table 5.2 shows that it is mainly due to the current noise of the input transistors of the preamplifier and of the load transistor M6 (see Fig. 5.5). Thus the noise can be optimized by increasing the width of the input pair of the preamplifier. Moreover M4 and M6 could be made longer, but their maximum length is limited by the presence of the cascode transistors M3 and M4 which should be maintained in saturation.

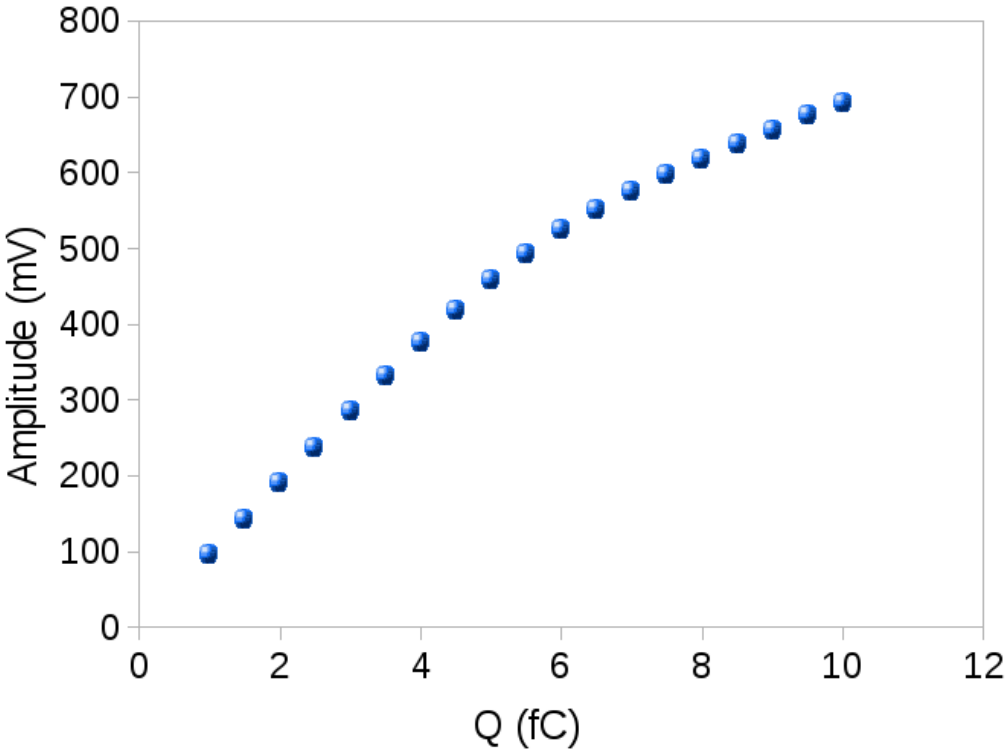


Figure 5.17: Linearity of the preamplifier

Component	Contribution to total noise (%)
M1 of 1st preamp stage	21.83
M2 of 1st preamp stage	18.06
M6 of 1st preamp stage	6.40
M1 of CFD postamp	5.57
M2 of CFD postamp	5.57

Table 5.2: Main contributors to total noise

5.5.2 The leakage current and the offset compensation

A leakage current up to 700 nA has been simulated. This value is a significant overestimation of the expected maximum leakage which has been measured to be of around 270 μA on the full sensor operating at 5°C after 50 days, thus of 15 nA per pixel. A leakage current of 700 nA, introduces an offset of 84 mV at the output of the first preamplifier stage, through the 120 kΩ feedback resistor, and 240 mV at the output of the second stage. For higher values of leakage current the preamplifier stage begins to saturate. The dynamic offset compensation circuit, when biased with the nominal current of 20 μA, reduces this offset to 62 mV at the input of the zero crossing discriminator and to 26 mV if the bias current is increased to 50 μA. The offset compensation capability of the circuit is shown in Fig. 5.18 for a p-in-n like signal. The result is analogous for a signal of the inverse polarity. Even if the offset is well compensated, the distortion introduced by the offsets in the preamplifier may destroy the timing of the front-end. The convolution of the measured time walk with the Landau distribution in presence of a leakage current of 700 nA leads to 5.4 ps RMS, showing that for these values the distorsion is not an issue. Moreover, since the presence of offsets and/or of leakage current could disable the threshold of the arming discriminator or lead to situations where the threshold is never disabled, the arming discriminator has been biased in AC.

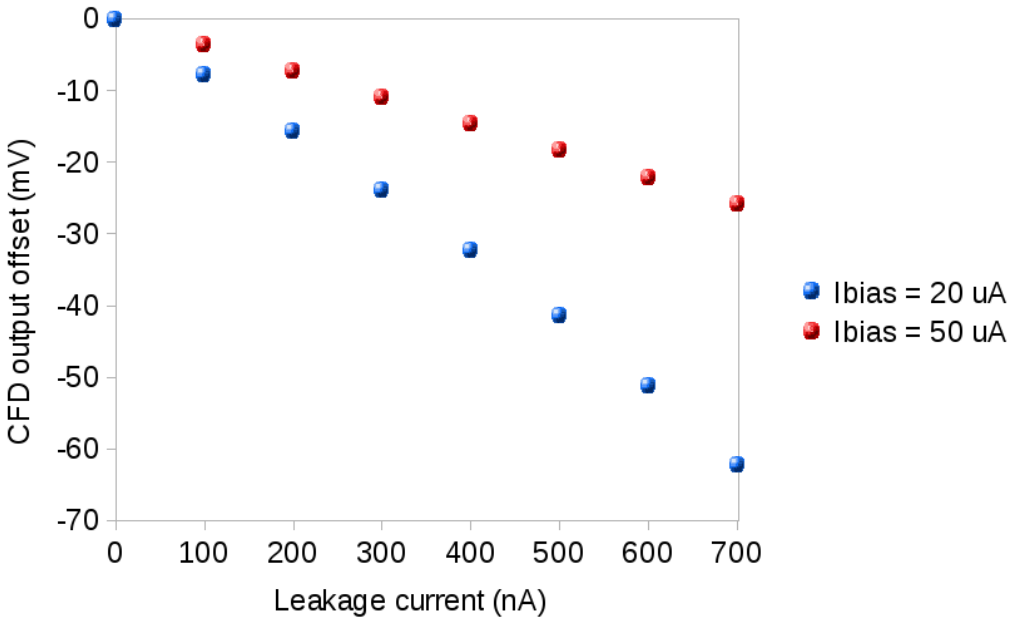


Figure 5.18: Offset at the input of the zero crossing discriminator for leakage currents up to 700 nA

The offset introduced by the mismatch of the components has also been evaluated with Montecarlo simulations. In the worst cases it has been found an offset of 32 mV and of -22 mV at the input of the zero crossing discriminator. The overall offset of the circuit referred at the input of the discriminator, including the offset of the discriminator itself, is 38 mV and -26 mV. The presence of the offset is equivalent of applying a threshold to the zero crossing discriminator as shown in Fig. 5.19,

introducing a leading edge error. The extent of the additional time walk induced by the offsets has been simulated introducing an offset of ±50 mV at the input of the discriminator. When convoluted with the Landau, the time walk does not change significantly in the two cases, leading to 19.2 ps RMS and 11.4 ps RMS against 5.3 ps RMS of the ideal offsetless case. It should be noted that in the simulations the dynamic offset compensation circuit has been biased with the nominal current of 20 μA. The overall offset can be further reduced by increasing this bias. Since the dynamic offset compensation circuit is placed at the input of the discriminator, the limit to the minimum offset is imposed by the mismatches in the zero crossing discriminator. The maximum offset introduced in this stage has been simulated to be of around ±10 mV referred at the input of the discriminator itself. Besides causing

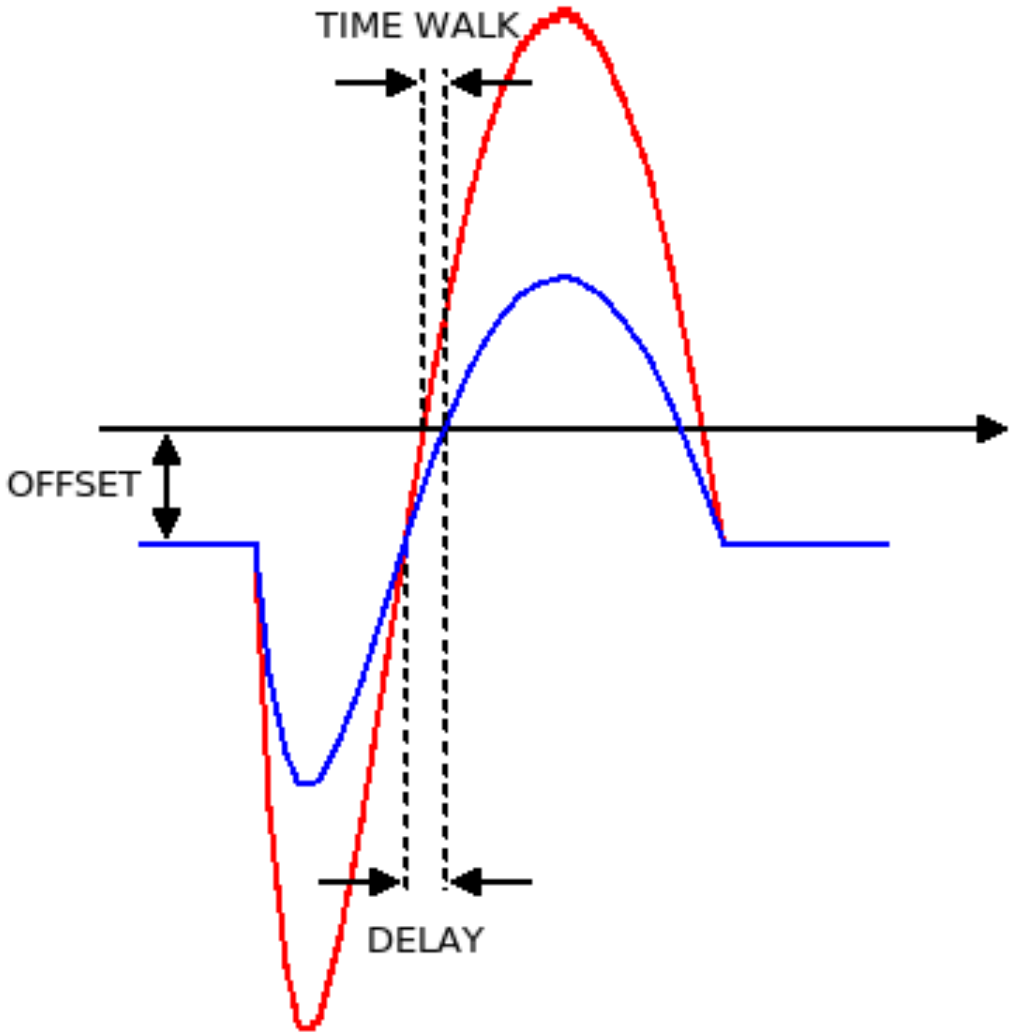


Figure 5.19: Additional time walk introduced by offsets

an additional time walk, the offset introduces also a delay in the discriminator signal (see Fig. 5.19) which is different from pixel to pixel. However this translates in a systematic error which can be calibrated.

5.5.3 The overall time resolution

The charge sensitivity of the zero crossing discriminator has been evaluated by measuring the delay of the discriminator output with respect to the actual zero crossing occurrence. The result, plotted Fig. 5.20, shows that the maximum time walk introduced by the discriminator is 30 ps.

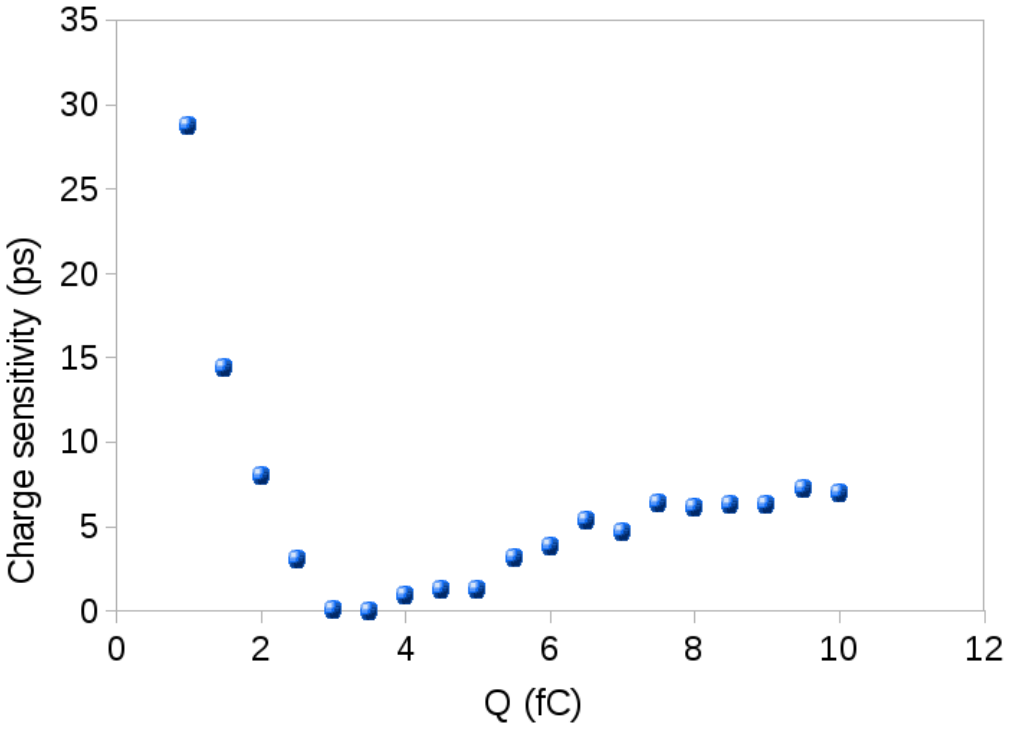


Figure 5.20: Charge sensitivity of the discriminator

The overall time walk and the jitter of the new design have been evaluated by simulating both the schematic and the layout of the circuit. Fig. 5.21 shows the time walk curve in the dynamic range from 1 fC to 10 fC. The observed degradation due to parasitics introduced in the layout design is not a concern since, when weighted on the Landau, the final error due to time walk becomes 5.3 ps RMS and does not change significantly with respect to the schematic result of 4.9 ps RMS.

The actual timing error due to amplitude and shape variations can be estimated using Montecarlo simulations, as previously described. The results are reported in Table 5.3 showing a good performance in correcting time walk and in rejecting shape variations in all process corners.

In Table 5.3 it is also reported the jitter at 1 MIP. It has been calculated as the ratio between the noise at the output of the CFD postamplifier, obtained with Cadence AC noise simulations, and the slope of the bipolar signal. It can be also estimated using transient noise analysis tool by Cadence, which uses components models to simulate the circuit with its noise. Fig. 5.22 shows the result of a transient noise simulation of the schematic of the circuit with 1 MIP input charge. The discriminator output jitters of 31 ps RMS. The result is compatible with the jitter measured in typical mean using AC noise simulations. Due to parasitic in the layout

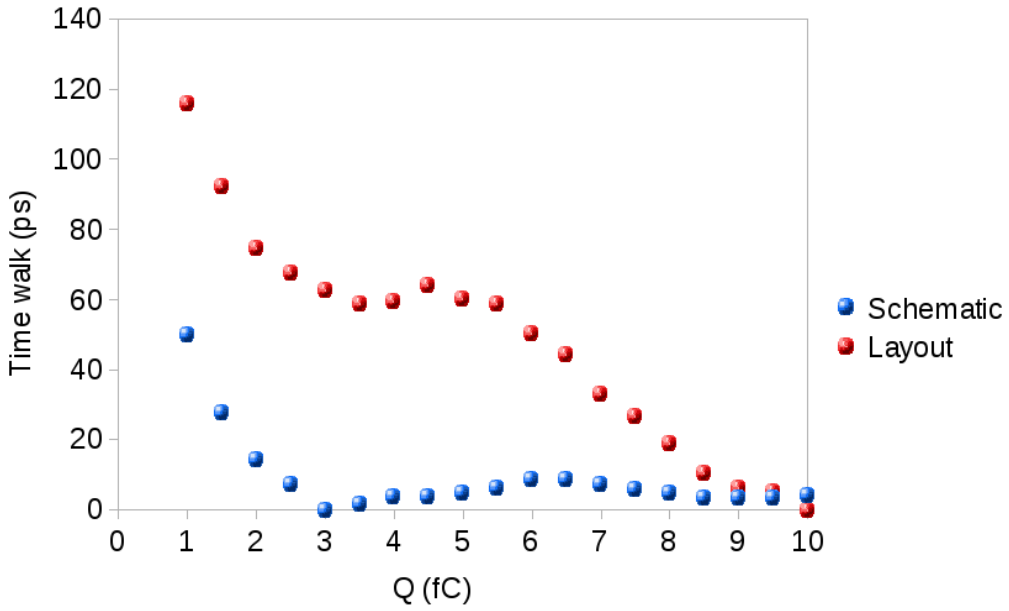


Figure 5.21: Time walk of the full analog chain obtained by both schematic and layout simulations in typical mean

Schematic results		
Process corner	RMS Jitter @ 1MIP (ps)	Error due to signal variations (ps RMS)
Typical mean	40	20
$+1.5\sigma$	45	27
$+3\sigma$	52	23
-1.5σ	38	23
-3σ	38	21
Layout results		
Process corner	RMS Jitter @ 1MIP (ps)	Error due to signal variations (ps RMS)
Typical mean	47	27
$+1.5\sigma$	50	31
$+3\sigma$	59	30
-1.5σ	44	27
-3σ	45	24

Table 5.3: Simulation results of shape correcting CFD design.

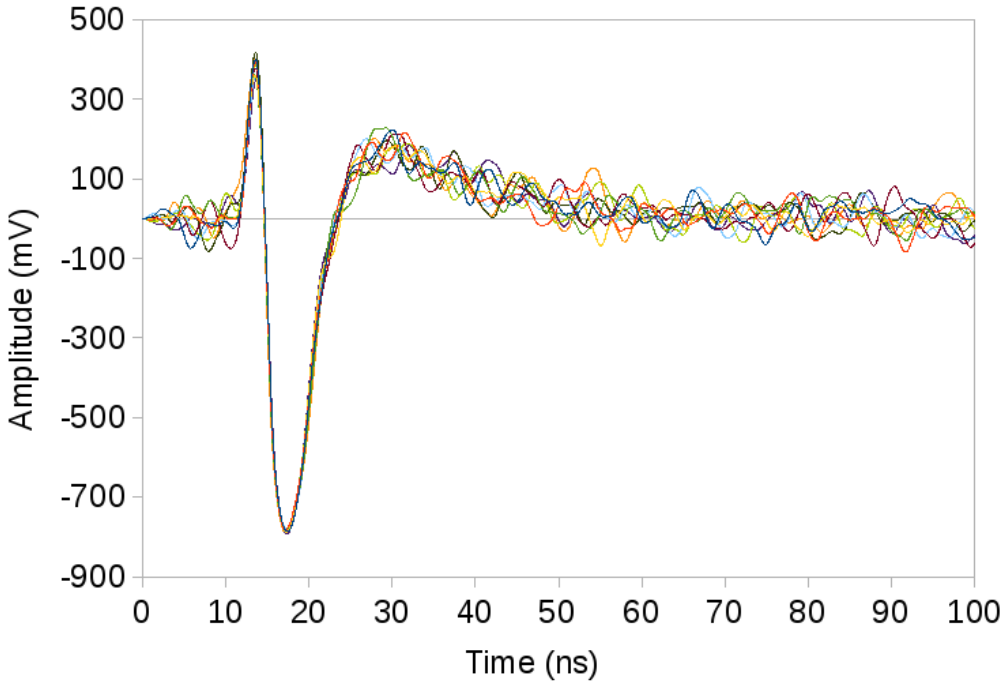


Figure 5.22: CFD output for 2.4 fC input charge obtained with a transient noise analysis

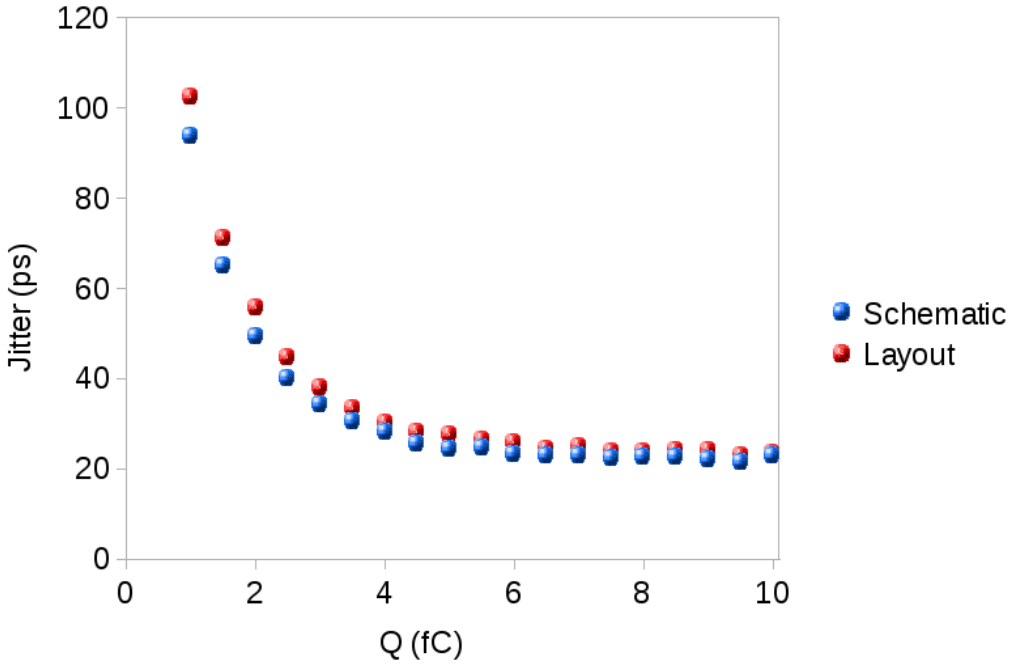


Figure 5.23: Jitter of the new front-end design obtained by schematic and layout simulations in typical mean

the jitter is slightly higher with respect to the schematic. Fig. 5.23 shows the jitter in the two cases in all the dynamic range. This good matching between schematic and layout simulations is the result of a careful schematic and layout co-design. The layout of the circuit have been studied in detail to find out the main parasitics affecting the circuit performance. In many cases this led to the modification of the scheme of the circuit, to a new layout design and so on.

Finally, the total time resolution can be quantified from the convolution of two contributors. On one hand, in the Montecarlo simulations the timing error due to amplitude and shape variations are taken into account, but the jitter due to noise is not considered. On the other hand, the AC simulations allow to estimate the noise contribution to jitter for different charges, without considering any signal variations. An estimation of the final time resolution can be obtained performing the Montecarlo simulations with the 200 files including the noise of the components through the Transient noise analysis tool. This simulation took more than one day, but the resulting timing error includes the amplitude and shape variations of the signal, the jitter due to noise,the charge sensitivity, the non linearities of the circuit and the layout parasitics. The results are reported in Table 5.4 The only contribution which is not considered in this simulation is the effect of the offset, which generates an additional time-walk. However, comparing the results of Tables 5.3 and 5.4, it is clear that the timing error is dominated by the jitter, thus the total time resolution is expected to be lower than 100 ps RMS in almost all process corners including the effect of the offsets.

Schematic results	
Process corner	Time resolution (ps RMS)
Typical mean	53
$+1.5\sigma$	48
$+3\sigma$	59
-1.5σ	52
-3σ	67
Layout results	
Process corner	Time resolution (ps RMS)
Typical mean	68
$+1.5\sigma$	55
$+3\sigma$	86
-1.5σ	65
-3σ	95

Table 5.4: Simulation results of the overall time resolution including jitter due to noise and signal shape variations and amplitude time walk.

The characteristic of the front-end are summarized in Table 5.5. The area filled

by the new CFD filter is slightly lower than in the old prototype, while the overall power consumption of the circuit has grown up to 1.18 mW/channel and is mainly dissipated by the preamplifier.

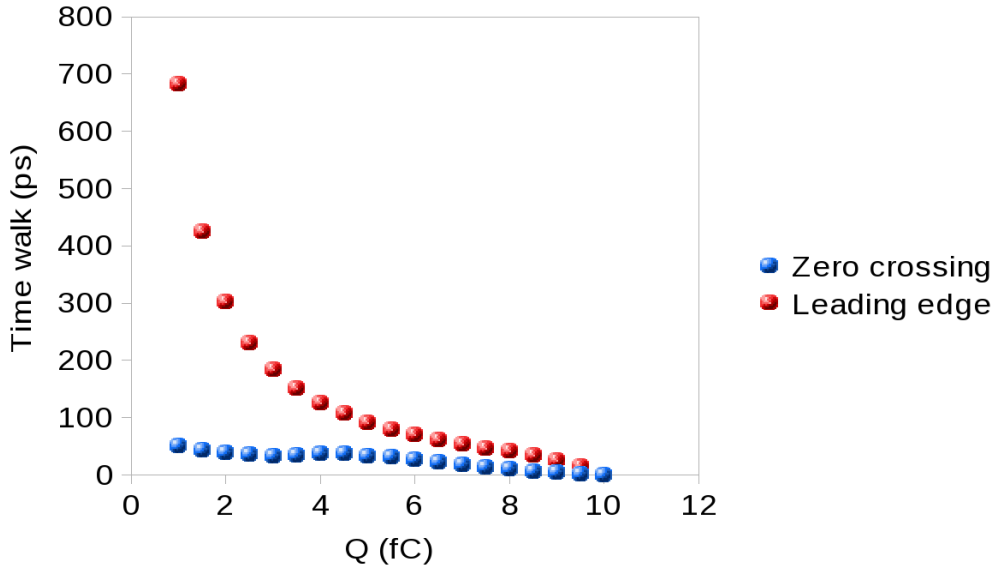
Preamplifier gain		95 mV/fC
Preamplifier peaking time		3 ns
ENC		308 e^-
Dynamic range		1-10 fC
Leakage compensation capability		± 700 nA
Overall offset referred at the discriminator input		+38 mV ÷ −22 mV
ZC discriminator contribution to offset referred at its input		±10 mV
ZC discriminator charge sensitivity		28 ps peak-to-peak
Time resolution in typical mean		68 ps RMS
Power consumption		1.18 mW
	Component area (μm^2)	Power consumption (μW)
First stage preamplifier	29 x 51	180
Preamplifier replica	29 x 33	45
Second preamplifier stage	48 x 84	606
CFD filter	141 x 69	0
CFD postamplifier	25 x 82	156
Arming discriminator	31 x 12	96
ZC discriminator	31 x 12	96

Table 5.5: Characteristics of the new front-end design

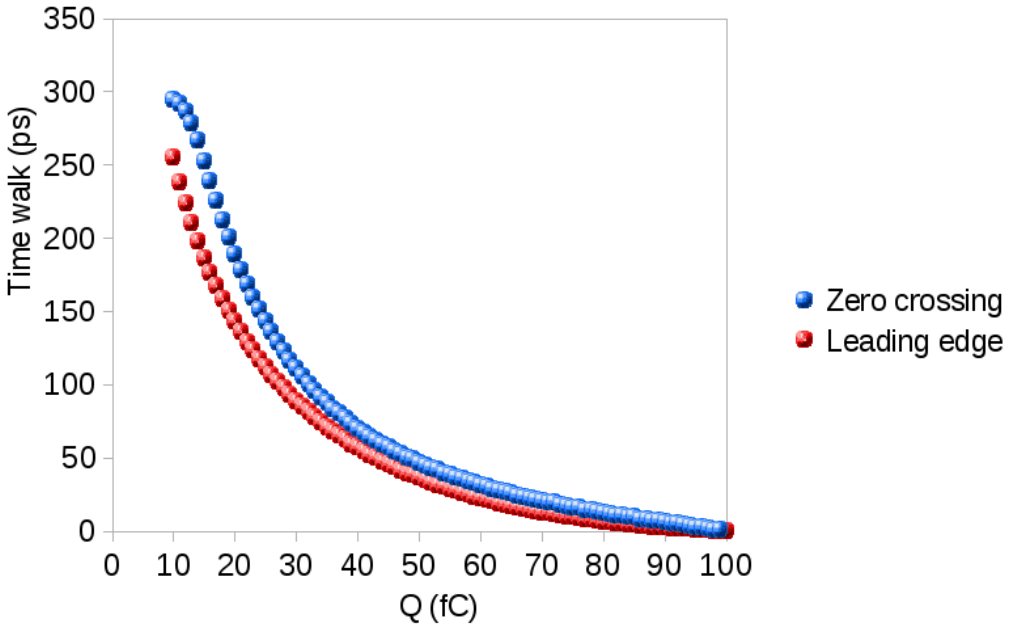
5.6 A flexible front-end for timing measurements

The CFD is very attractive for the potential resolutions which can be reached in this charge range, with respect to the ToT technique. However it is based on a very refined optimization of the components and thus depends critically on the quality of the models provided by the foundry and from the accuracy of the design. As a consequence it is strictly mandatory, besides having post-layout simulations, to perform a schematic and layout co-design.

On the other hand, since the CFD block is relatively compact and since it incorporates a leading edge discriminator, a circuit implementing both the ToT technique



(A)



(B)

Figure 5.24: Time walk of the zero crossing and of the leading edge discriminators in the dynamic range (A) from 1f C to 10 fC and (B) from 10 fC to 100 fC

and the CFD can be designed. This solution gives the possibility to choose in a second phase the configuration which gives the best performance. Moreover, using a high resolution TDC and with some more circuitry, it is possible to combine the two techniques. In this case, the ToT information could be useful to further correct the time walk measured from the CFD and/or to improve the spatial resolution by calculating the barycenter of the charge distribution.

In conclusion, an architecture implementing both techniques provides the maximum of the flexibility with a circuit optimized on large dynamic ranges. For example, a simulation of the described front-end, plotted in Fig. 5.24, shows that the CFD time walk is highly lower with respect to the leading edge time walk for charges between 1 fC and 10 fC, while if the dynamic range is one order of magnitude higher the two are comparable. In this way the circuit would be able to work as a simple CFD or as a leading edge depending on the application with a minimum overhead in terms of power consumption and area. Moreover, with a minimum of programmability it is possible to choose the circuit to be used and to switch off the other, thus saving power. Otherwise a merged configuration could be the optimal solution. Instead of measuring the amplitude from the leading edge discriminator, it is possible to use the ToT of the overdrive of the bipolar signal as shown in Fig. 5.25. A simulation of the ToT measured from the arming and from the zero crossing discriminators (Fig. 5.26) shows that the the the ToT ranges between 8.1 ns and 11.5 ns in the first case and between 3.6 ns and 7.8 ns in the second. Thus, using the same TDC in the two cases, the amplitude measured from the overdrive of the bipolar signal has a slightly lower resolution, but using this signal allows to combine the precise timing information from the CFD with the amplitude measurement.

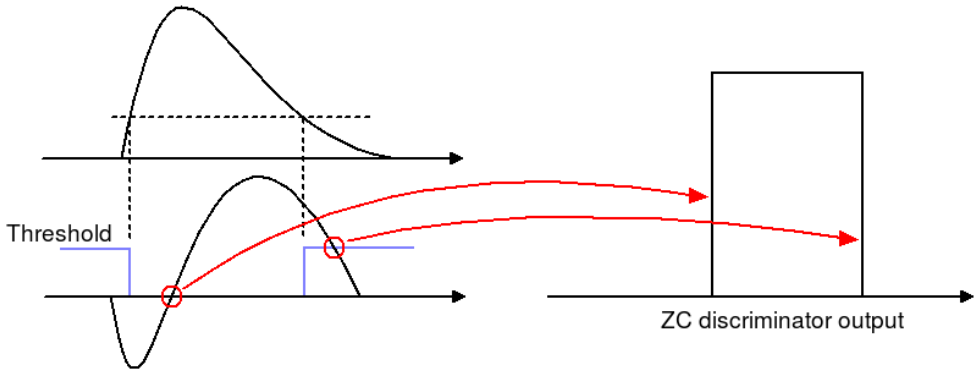
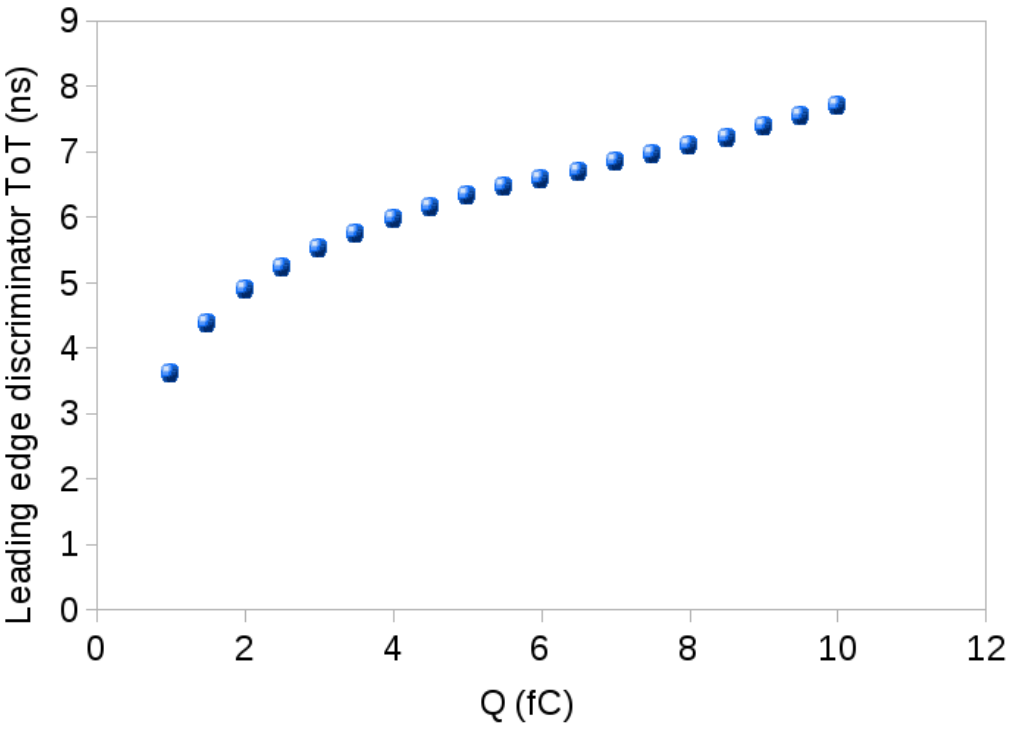


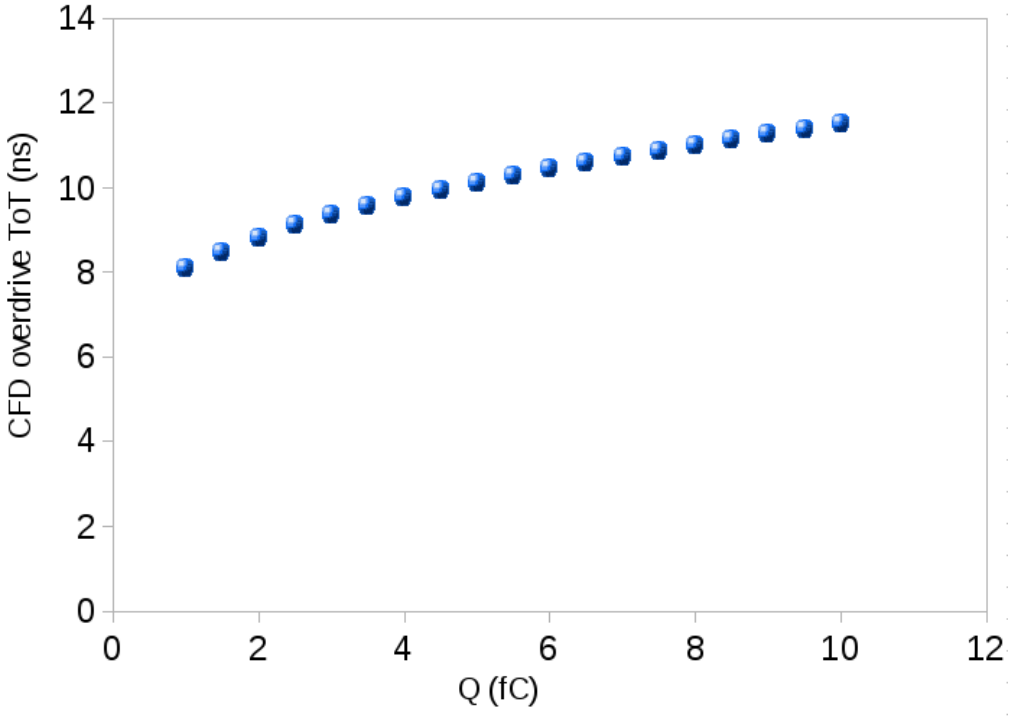
Figure 5.25: Output of the ZC discriminator

Furthermore, where it is possible, two TDC in parallel can be used, one measuring the timing signal from the CFD and the other the amplitude from the leading edge discriminator.

In conclusion, the designed front-end incorporates all the components needed to implement a highly flexible ASIC, suitable for precise measurements in large dynamic ranges, with sensors of both polarities and providing the possibility of programming the circuit in a lot of different configurations.



(A)



(B)

Figure 5.26: ToT measured from (A) the leading edge discriminator and from (B) the ZC discriminator

Chapter 6

Conclusions

Silicon detectors have become one of the standard tools for particle detection, over the last decades. More accurate and versatile detector systems have been developed thanks to the extensive research in the last years and have found applications in a wide range of scientific domains. The constant performance improvement of silicon detector systems has gone in parallel with the development of the front-end electronics, which was required to become more and more faster, smaller and radiation tolerant. However new issues emerged with modern deep submicron technologies. The requirement of large detection areas with high position, momentum and time resolutions impose strict limits on the power consumption and on the amount of material used for mechanical support, cooling and so on. For multichannel systems the size and power consumption of the front-end electronics are critical concerns.

This work focused on the development of a low power front-end for precise timing multichannel applications. The measurement of the time of occurrence of a physical event is of primary importance for many radiation detection systems found both in basic research and in medical applications. A time resolution in the order of 100 ps or better is required, for example, to perform particle identification in high energy physics and to add time of flight capability to the techniques employed for Positron Emission Tomography (PET). State of the art integrated circuits developed for this purpose typically have a power consumption above 10 mW/channel and a number of channels in the order of 8-16 per chip. However the general tendency is towards better resolution and higher granularity, implying an increasing number of readout channels and a more compact front-end electronics.

The front-end described in this work has been developed in the framework of the R&D of the GTK for NA62 at CERN SPS. The experiment aims to have a direct measurement of the CKM matrix parameter V_{td} in order to test the SM. At this scope it will collect about 80 events of the rare kaon decay into a pion and neutrino-antineutrino pair. Since the channel of interest has a S/B = 1:10, the time of arrival of the kaons must be detected with a 150 ps time resolution, to ensure the right match with the outgoing pion track. Thus the crucial detector for the experiment is the beam spectrometer, the GTK. It consists of three stations of hybrid silicon pixels detectors with a time resolution of 200 ps RMS on the single station and 100 μm RMS space resolution. In addition, due to the high rate, the system will operate under a high radiation environment.

The precision required involves the use of timing techniques to correct for am-

plitude variations of the signal and optimized to reduce noise effects. It is well known that in leading edge discriminators signals of different amplitudes will cross the threshold at different times, thereby generating time walk. In order to evaluate which solution is the better for this application, two ASICs implementing complementary architectures have been developed. One is based on the ToT technique while the other uses a CFD. The two architectures have been presented and described concentrating on the second one. The CFD represents an effective approach to minimize time walk when the dynamic range is not too large so that the linearity of the system can be maintained. Moreover, the absence of calibrations for the time walk correction, makes this option more flexible and suitable for a lot of other modern timing applications besides the GTK.

The practical implementation of monolithic CFDs suitable for multichannel ICs entails several issues. The area of the circuit and the power consumption have to be minimized and the impact of process spreads must be taken into account. Furthermore the arming circuitry must be designed to prevent the generation of full swing logic levels at the outputs of the zero-crossing detector. Moreover detector signals are subject to statistical fluctuations that affect not only the amplitude but also the signal shape. All these issues have been analyzed and discussed in this work.

Due to the high costs and to its complexity, the development of an ASIC usually goes through one or more prototyping step. The performances obtained from a prototype are fundamental to test the functionality of the blocks, but the final evaluation of the of the functionality of an architecture is possible only from the full size chip. In this perspective, a complex prototype, which embeds all the critical blocks, minimizes the risks which are usually encountered in the transition from the prototyping phase and the final ASIC design. A monolithic CFD for highly integrated applications has been designed and produced in 0.13 μm CMOS technology as a first prototype, to test its performances in detail. A second prototype, implementing an almost complete architecture has been submitted in 2009 and tested in 2010. While the first prototype is formed only by four channels with the analog front end, the second contains a small matrix of three columns and three complete EoC controllers. Each pixel is formed by the front end, followed by a TAC based TDC and by a digital section interfaced with the EoC. This prototype aims to test the complete functionality of the architecture under study by implementing a circuitry as similar as possible to the full chip version. Results from the two prototypes shown the functionality of the single blocks, but brought to light problems linked to substrate noise and to signal shape variations.

A new design under development aims to improve the performances of the circuit and to fix the noticed problems. It uses a shorter delay to better reject the signal shape variations due to border effects and charge straggling. At this scope, all the analog front-end has been re-designed leading to a better timing performance, but also to a higher power consumption. The preamplifier design has been revised in order to make the coupling with the sensor less critical. While maintaining the hysteresis topology, the triggering system has been changed to improve the efficiency and to relax the constraints on the delay and fraction of the CFD. This fact leads to the introduction of a leading edge discriminator to gate the zero crossing one. The

developed front-end is thus highly flexible since it includes both leading edge and CFD techniques, which can be used in turn depending on the application. Moreover it allows to combine the amplitude and the timing informations. This solution gives the possibility to further improve the time resolution by adding an off-line time walk correction to the CFD data. Moreover the double measurement allows to improve the spatial resolution by measuring the charge sharing between pixels. Exhaustive simulations have been performed on the new prototype considering noise rejection, process variations, mismatch effects and layout parasitics.

As already pointed out, thanks to its high flexibility, this architecture can be exploited for other timing applications with relatively few modifications.

Appendix A

The time walk and jitter convolution with the Landau

The time walk curve and the jitter measured or simulated can be convoluted with the probability density of the experiment to evaluate the final resolution. The fluctuations of energy loss by ionization of a charged particle in a thin layer of matter was first described theoretically by Landau [77]. They give rise to an asymmetric probability density function characterized by a narrow peak with a long tail towards positive values. The mathematical definition of the probability density function is:

$$L(\lambda) = \frac{1}{2\pi i} \int_{c-i\infty}^{c+i\infty} e^{x \log x + \lambda s} ds \tag{A.1}$$

where λ is a dimensionless number and is proportional to the energy loss, and c is any real positive number. Other expressions and formulae are indicated in [78] and [79], e.g.:

$$L(\lambda) = \frac{1}{\pi} \int_{0}^{\infty} e^{-x \log x - \lambda s} \sin(\pi s) ds \tag{A.2}$$

Moyal [80] has given a closed analytic form:

$$L(\lambda) = \sqrt{\frac{e^{-(\lambda + e^{-\lambda})}}{2\pi}} \tag{A.3}$$

where $\lambda = R(E\text{-}E_P)$. E_P is the most probable energy loss and R is a constant depending on the absorber. This curve reproduces the asymmetric features of the Landau distribution and avoids the pitfalls of numerical integration. It is, however, too low in the tail and unrelated to $L(\lambda)$ as defined above. On the other hand, Moyal's curve is useful in some situations. As the layer over which energy loss is integrated becomes thicker, the tail of the Landau distribution, according to the central limit theorem of statistics[1], has a tendency to diminish. Thus the Landau distribution becomes the more general Vavilov distribution. Vavilov introduced the parameter $k = E_{av}/E_{max}$, with E_{av} the average energy loss over the layer, and

[1]The sum of many random variables converges towards a Gaussian distribution if the number of variables is large, whatever the individual distribution function

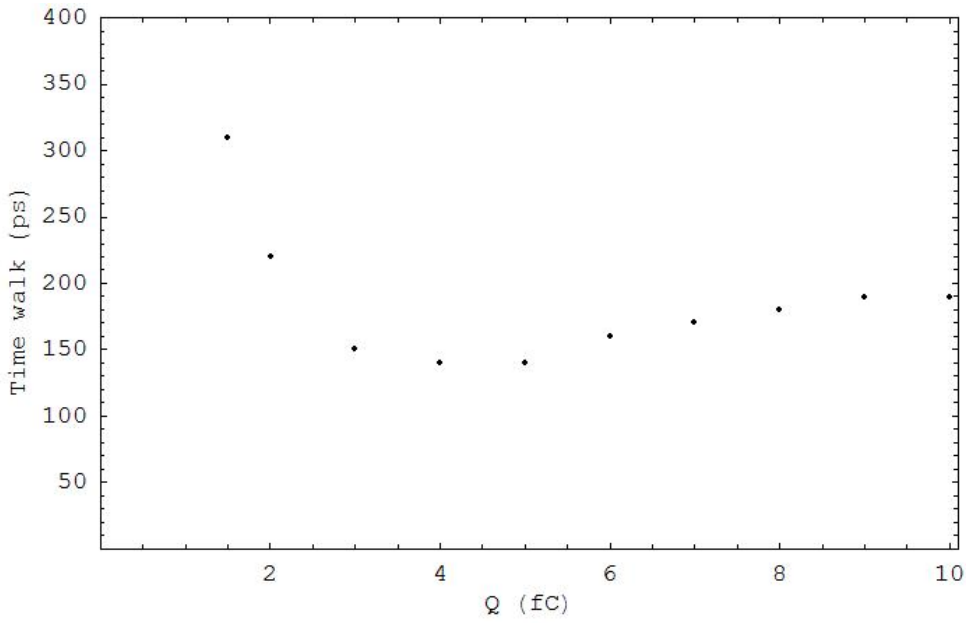
E_{max} the maximum energy loss in a single collision. The Landau distribution is the limiting case for $k = 0$ and a good approximation for $k < 0.01$, while the Gaussian is the limiting case for $k = \infty$ and a reasonable approximation for $k > 10$. For more details, see [81].

The following code for the Landau convolution has been developed in Mathematica 7 using the Moyal's curve. The `NormalDistribution` and `Graphics` packets are required to execute it.

```
<< Statistics`NormalDistribution`
<< Graphics`Graphics`
```

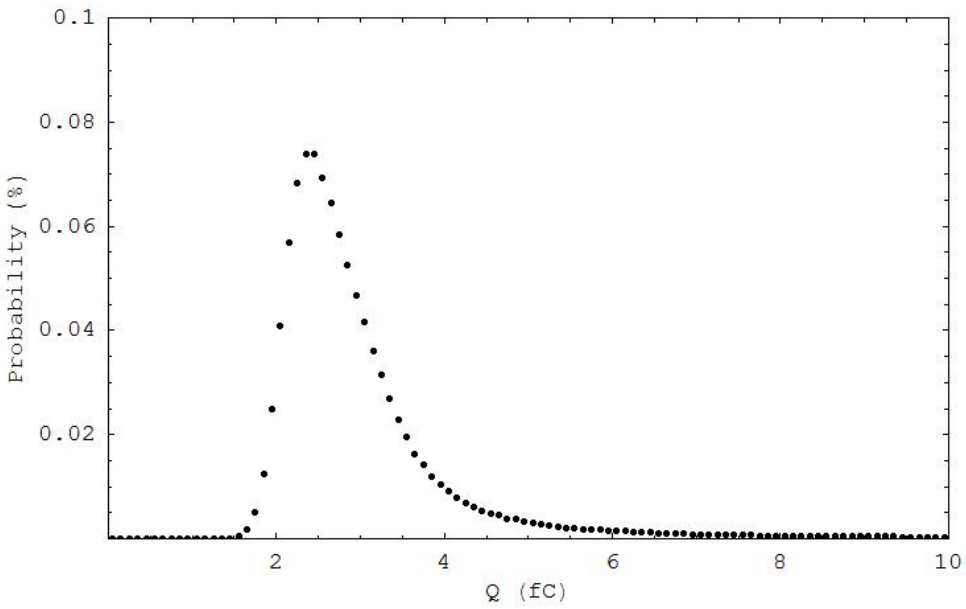
The variable `num` is the number of events generated. The time walk and the jitter measured for different charge values (list `q`) are contained in the lists `t` and σ`t`.

```
num = 900000;
q = {1, 1.5, 2, 3, 4, 5, 6, 7, 8, 9, 10};
t = 1000*{19.38, 19.21, 19.12, 19.05, 19.04, 19.04,
   19.06,
 19.07, 19.08, 19.09, 19.09} - 18900;
σt = {97, 66, 51, 33, 28, 22, 21, 18, 17, 16, 14};

tw = Table[{q[[i]], t[[i]]}, {i, 1, Length[q]}];
ListPlot[tw, AxesOrigin → {0, 0}, PlotRange → {{0,
   10.1}, {0, 400}}, TextStyle → {Font → "Times New
   Roman", FontSize → 18}, Frame → True, FrameLabel
   → {"Q (fC)", "Time walk (ps)"}]
```

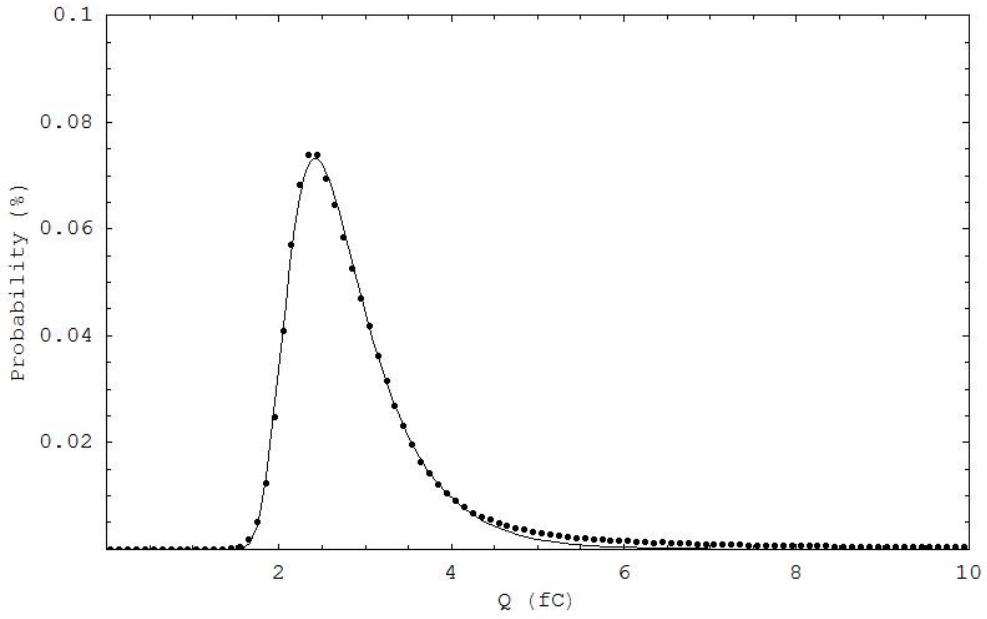


The proability distribution of the experiment obtained with Geant simulations has been fitted with the Moyal's curve.

```
str = OpenRead["D:\\Landau.txt"];
weight = {};
i = 0;
While[i < 200,
  weight = Append[weight, {Read[str, Number], Read[
     str, Number]}];
  i = i + 1
  ]
Close[str];

ListPlot[weight, PlotRange → {{0, 10}, {0, 0.1}},
   TextStyle → {Font → "Times New Roman", FontSize
   → 18}, Frame → True, FrameLabel → {"Q (fC)", "
   Probability (%)"}]
```

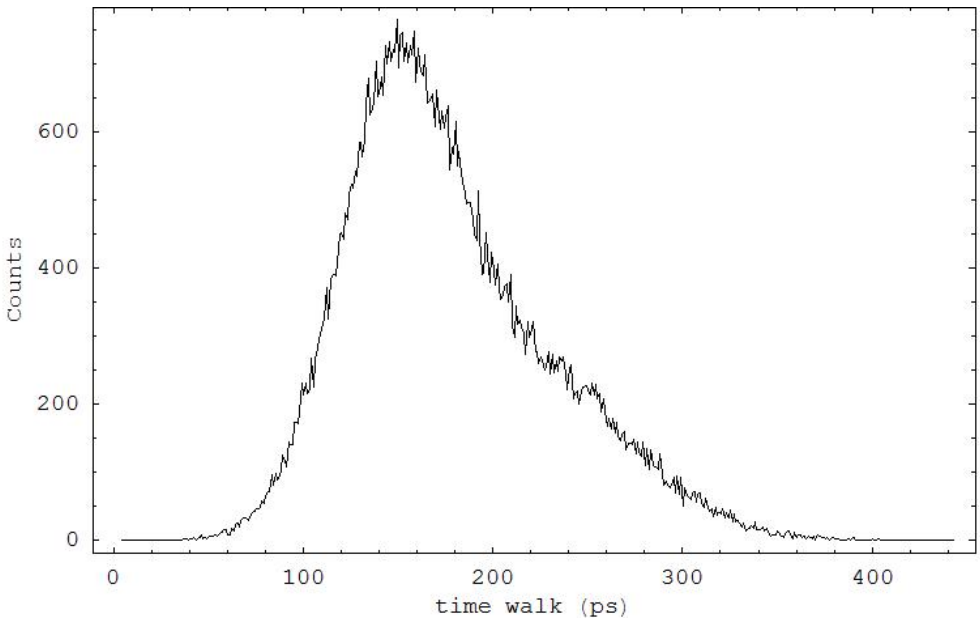


```
Clear[A, qm, r]

FindFit[weight,A*Sqrt[Exp[-r*(x-qm)-Exp[-r*(x-qm)
   ]]/(2*Pi)],{{A,0.3},{qm,2.2},{r,3}},x]
{A → 0.302525,qm → 2.42308,r →3.21284}

A = %[[1, 2]];
qm = %%[[2, 2]];
r = %%%[[3, 2]];

f[x_] = A*Sqrt[Exp[-r*(x - qm) - Exp[-r*(x - qm)
   ]]/(2*Pi)];

Show[ListPlot[weight, PlotRange → {{0, 10}, {0,
   0.1}}, TextStyle → {Font → "Times New Roman",
   FontSize → 18}, Frame → True, FrameLabel → {"Q (
   fC)", "Probability (%)"}], Plot[f[x], {x, 0, 10},
   TextStyle → {Font → "Times New Roman", FontSize
   → 18}, Frame → True, FrameLabel → {"Q (fC)", "
   Probability (%)"}, DisplayFunction → Identity]]
```



The probabilities of the events with a certain charge have been calculated from the obtained fit function f(x) and listed in `qp`. At this point everything is ready to extract the events based on the measured time walk and jitter and following the Landau distribution. For each value of charge in the list `q` a normal distribution centered in the time `t[[i]]` and with a standard deviation equal to the jitter σ`t[[i]]` have been extracted and listed in `jitter`. The `num` random events have been generated from this list of normal distributions and stored in `t_T` and `q_T`. Thus the histogram of the extracted data have been plotted.

```
qp = Table[f[q[[i]]], {i, 1, Length[q]}];

i = 1;
t_T  = {};
q_T  = {};
u = {};
While[i ≪ Length[q],
        jitter = NormalDistribution[t[[i]], σt[[i]]];
        t_T  = Join[t_T, Table[Random[jitter], {j, 1,
            qp[[i]]*num}]];
        q_T = Join[q_T, Table[q[[i]], {j, 1, qp[[i]]*
           num}]];
        i = i + 1
]

histoT = BinCounts[t_T, {Min[t_T], Max[t_T], 1}];

ListPlot[Table[{i + 1 + Min[t_T], histoT[[i]]}, {i,
   1, Length[histoT]}], PlotJoined → True, Frame →
   True, FrameLabel → {"time walk (ps)", "Counts"},
   AxesOrigin → {Min[t_T], 0}, TextStyle → {Font →
   "Times New Roman", FontSize → 18}]
```



Finally the rms of the distribution calculated, resulting in 92.37 ps.

```
55 RootMeanSquare[t_T - Mean[t_T]]
56 52.67
```

Appendix B

The CFD programmable capacitors optimization

The value of the programmable capacitors in the CFD filter have been calculated considering the process spreads and the parasitic capacitors which load the filter through the open switches. Referring to Fig. 4.20, in the process corners the CFD filter is supposed to be programmed as follows:

$$\begin{array}{ll} C_{TOT} = C + C_a & \text{in typical mean} \\ C_{TOT} = C & \text{in } +3\sigma \text{ corner} \\ C_{TOT} = C + C_a + C_b & \text{in } -3\sigma \text{ corner} \end{array}$$

In order to have the same RC time constant in the three corners the following equations should be verified:

$$R|_{tm}(C + C_a + C_{xb})|_{tm} = R|_{+3\sigma}(C + C_{xa} + C_{xb})|_{+3\sigma} \quad \text{(B.1)}$$

$$R|_{tm}(C + C_a + C_{xb})|_{tm} = R|_{-3\sigma}(C + C_a + C_b)|_{-3\sigma} \quad \text{(B.2)}$$

where C_{xa} and C_{xb} are the values of the capacitors viewed by the filter when the switches are open (see Fig. B.1) and are equal to:

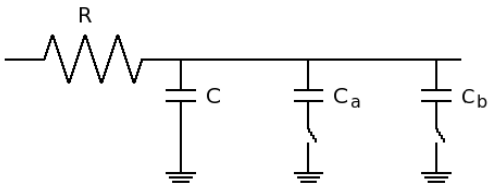
$$C_{xi} = \frac{C_s + C_{li} + C_i}{C_i(C_s + C_{li})} - C_{li}, i = a, b \quad \text{(B.3)}$$

C_{li} are the parasitic plate capacitance of capacitor C_i and depend on the dimension of the capacitor itself, while C_s is the parasitic capacitance of the switches, that in our case are equal for C_a and C_b. To determin the value of C, C_a and C_b a third equation must be added to the system B.1, B.2. The last condition is given by the total value of the three capacitors. This value has been chosen as 250 fF for reasons linked to the area.

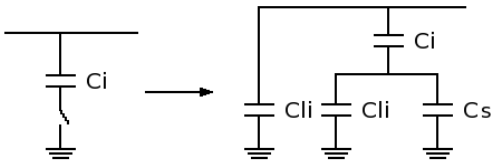
$$C + C_a + C_b = 250 \quad \text{(B.4)}$$

The values of the resistors in the corners have been extracted from the simulations.

```
rt = 627.9;
rp = 907;
rm = 403.4;
```



(A)



(B)

Figure B.1: (A) The delay of the CFD is programmable to front the variation of their value with the process. (B) The switches, when open, have a parasitic capacitance C_s which couples with the parasitic plate capacitance C_l of C_1 and C_2

Due to the process, the effective value of the capacitors is a fraction of the nominal one:

$$C|_{+3\sigma} = aC|_{\mathrm{tm}} \tag{B.5}$$
$$C|_{-3\sigma} = bC|_{\mathrm{tm}} \tag{B.6}$$

The value of the parameters a and b has been obtained from simulations.

```
4  cp = a*ct;
5  cap = a*cat;
6  cbp = a*cbt;
7  cm = b*ct;
8  cam = b*cat;
9  cbm = b*cbt;
10
11 a = 1.38;
12 b = 0.797;
```

The value of C_{xi} in the corners depends on the value of C_{li} which on turn depends linearly from C_i:

$$C_{li} = mC_i + q \tag{B.7}$$

The parameters m and q in the different corners have been extracted from simulations.

```
13 cxb = (cx + clb)*cbt/(cx + clb + cbt) + clb;
14 cxap = (cxp + clap)*cap/(cxp + clap + cap) + clap;
15 cxbp = (cxp + clbp)*cbp/(cxp + clbp + cbp) + clbp;
16
17 clb = mt*cbt + qt;
```

```
clap = mp*cap + qp;
clbp = mp*cbp + qp;

mt = 0.0789;
qt = 5.34;
mp = 0.0647;
qp = 5.43;
```

Finally the parasitic capacitance of the switches has been extracted from corner simulations.

```
cx = 12;
cxp = 10.33;
```

At this point all the variables have been set and it is possible to define and solve the system.

```
eqn1 = rt*(ct + cat + cxb)-rp*(cp + cxap + cxbp);
eqn2 = rt*(ct + cat + cxb)-rm*(cm + cam + cbm);
eqn3 = ct + cat + cbt - 250;

NSolve[{eqn1 == 0, eqn2 == 0, eqn3 == 0}, {ct, cat,
   cbt}]
```

There are four possible results, but the the last one is the only phisically acceptable.

```
{{ct → -26.6143, c0t → 291.137, c1t → -14.5227}, {
   ct → 93.1276, c0t → -9.30445, c1t → 166.177}, {
   ct → 274.84, c0t → -10.317, c1t → -14.5227}, {ct
    → 7.64453, c0t → 76.1787, c1t → 166.177}}
```

Appendix C

Functions fitting the analog signals of the P-TDC prototype

The analytical transfer functions of the outputs of the preamplifier and of the CFD of the new front-end design have been found. They can be useful to study the behavior of the described architecture using programming tools, such as C++. The preamplifier has been fitted with the function h(t) which Laplace transform function is:

$$\mathrm{H(s)} = \frac{\mathrm{k_0}}{(1+\mathrm{s}\tau_\mathrm{a})^3(1+\mathrm{s}\tau_\mathrm{b})^6} \tag{C.1}$$

where:

$$\begin{aligned} \mathrm{k_0} &= 2.1 \cdot 10^{-10} \\ \tau_\mathrm{a} &= 0.43 \text{ ns} \\ \tau_\mathrm{b} &= 0.23 \text{ ns} \end{aligned}$$

The result of the plot is shown in Fig. C.1 for a delta like input signal. If the preamplifier is stimulated by a typical sensor signal, like the one shown in Fig. C.2, the convolution with equation C.1 gives the signal shown in Fig. C.3.

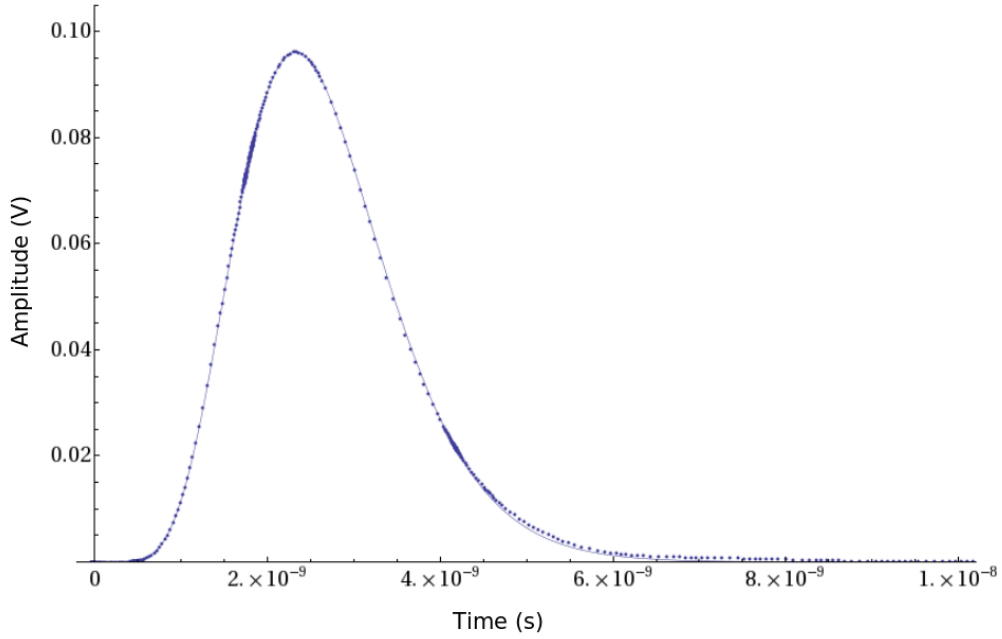


Figure C.1: Fit of the output of the preamplifier when stimulated with a delta signal

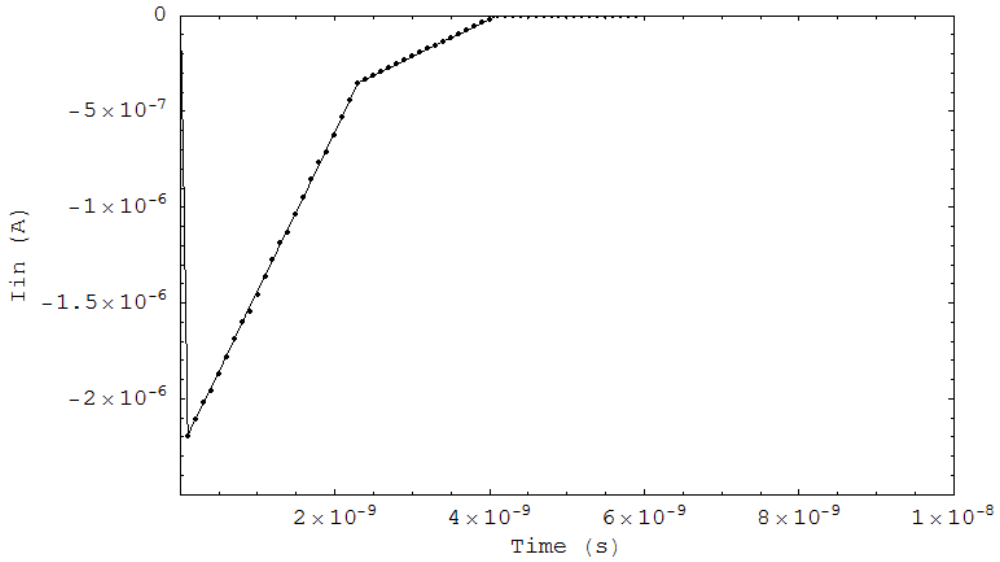


Figure C.2: Sensor triangular typical signal

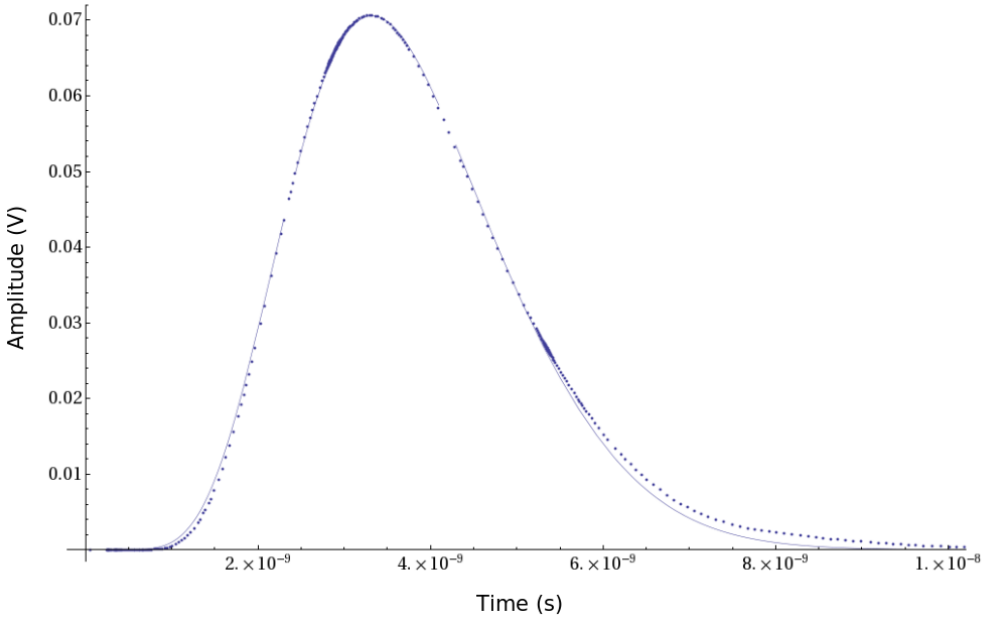


Figure C.3: Fit of the output of the preamplifier when stimulated with a sensor like triangular signal

The output of the CFD is fitted by:

$$g(t) = k[h_1(t - t_d) - \frac{h_2(d)}{A}] \tag{C.2}$$

where:

$$\begin{aligned} k &= 5.76021 \cdot 10^{-11} \\ A &= 2.46207 \\ t_d &= 433 \text{ ps} \end{aligned}$$

and $h_1(t)$ and $h_2(t)$ are the Laplace antitransfer functions of H(t) with:

$$\begin{aligned} \tau_{a1} &= 0.43 \text{ ns} \\ \tau_{b1} &= 0.31 \text{ ns} \end{aligned}$$

and:

$$\begin{aligned} \tau_{a2} &= 0.43 \text{ ns} \\ \tau_{b2} &= 0.22 \text{ ns} \end{aligned}$$

The result of the fits for a delta input signal and a sensor like input signal are shown respectively in Fig. C.4 and C.5.

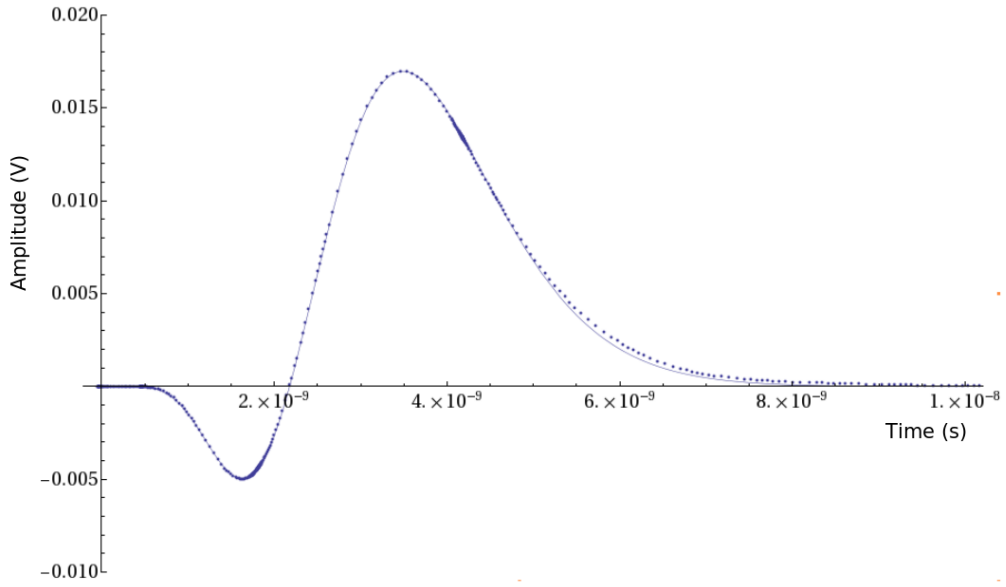


Figure C.4: Fit of the output of the CFD when stimulated with a delta signal

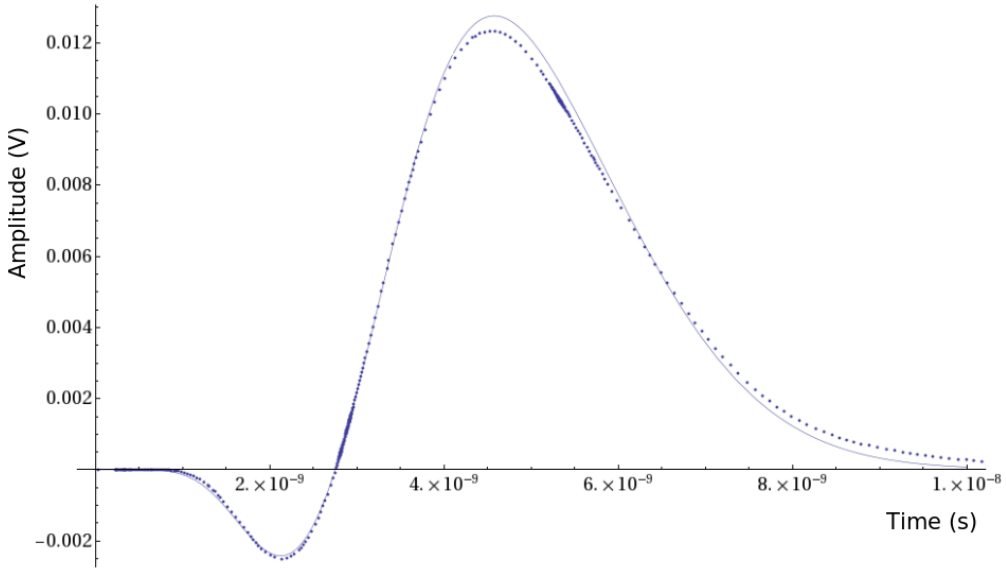


Figure C.5: Fit of the output of the CFD when stimulated with a sensor like triangular signal

Appendix D

Ocean Montecarlo simulations

The Montecarlo simulations with the current files have been performed exploiting the Ocean script tool from Cadence [82]. Ocean is a script language which allows to simulate and analyze data through a shell. It allows to organize long simulations with efficiency without opening the graphic Cadence interface. Ocean has revealed very useful to simulate the circuit in all process corners with 200 input signals. At any new simulation the script re-writes the netlist changing only the file in the input generator and sets the circuit parameters. Finally it saves the result of the simulation in a text file. This tool allowed to run hundreds of simulations reducing the time taken for all the process and suppressing the errors due to human interaction.

The 200 input files have been generated with C++ taking into account signal fluctuations due to both amplitude and shape variations and are written in the text files in the form (time, current). In this way they can be used as input files for the *ipwl* current generator component from Cadence. The files are read out from the working directory and stored in the list `slice_list` (line 1). A copy of the circuit netlist has been previously created (`netlist_01`) containing all the elements of the circuit but the *ipwl* component. For each current file, `netlist_01` is copied line by line to the `netlist` file (lines 9-15). Subsequently the *ipwl* with the correct current file is added to the `netlist` file (line 17). At this point everything is ready for the simulation. The simulator, the model libraries and the simulation folders are defined in lines 22-29, while the definition of the analysis, of the variables and parameters is made in lines 30-64. All this part can be copied directly from ADE L environment by choosing "Session" → "Save Ocean Script". Subsequently it is possible to change the parameters of the simulations by editing the file. Finally the simulation is run at line 66 and the outputs are defined and saved to the file `result.txt` (lines 68-74). The Montecarlo simulation is defined by the described code, which will be saved in a file called, for example, "MCsimulation.ocn". To run the simulation it is sufficient to type in the Virtuoso terminal the command `load("path/MCsimulation.ocn")`.

```
1 slice_list = getDirFiles("/home/garbolin/designs/
     ibm_cmos8_dm/correnti_wp/")
2
3 foreach(val slice_list
4    case(
5       val
6       ("." nil)
```

```
7       ("." nil)
8       (t
9          fin = infile("/home/garbolin/designs/
              ibm_cmos8_dm/SimDir/fullchain_study/
              spectre/schematic/netlist/netlist_01")
10         fout = outfile("/home/garbolin/designs/
              ibm_cmos8_dm/SimDir/fullchain_study/
              spectre/schematic/netlist/netlist" "w")
11
12         for(i 1 22156
13            gets(a fin)
14            fprintf(fout "%s" a)
15         )
16
17         fprintf(fout "I73 (gnda vin) isource \\\n
              file=\"/home/garbolin/designs/
              ibm_cmos8_dm/correnti_wp/%s\" dc=0 mag=0
              \\\n type=pwl delay=20n offset=0 scale=1
              \n" val)
18
19         close(fin)
20         close(fout)
21
22         simulator('spectre)
23         design("/home/garbolin/designs/ibm_cmos8_dm/
              SimDir/fullchain_study/spectre/schematic/
              netlist/netlist")
24         resultsDir("/home/garbolin/designs/
              ibm_cmos8_dm/SimDir/fullchain_study/
              spectre/schematic")
25         modelFile(
26            '("/home/garbolin/designs/ibm_cmos8_dm/
                 corner_designs.scs" "")
27            '("/usr/ibm_lib/cmos8_relDM/IBM_PDK/
                 cmrf8sf/relDM/Spectre/models/allModels
                 .scs" "tt")
28            '("/usr/cadence/IC_6.1.3/tools/dfII/etc/
                 cdslib/artist/functional/allFunc.scs"
                 "")
29         )
30         analysis('dc ?saveOppoint t)
31         analysis('tran ?stop "100n"  ?errpreset "
              conservative")
32         desVar(    "ipre2" 60u     )
33         desVar(    "vcas_pre" 800m )
34         desVar(    "vcas_arm" 900m )
35         desVar(    "Ileak" 0    )
36         desVar(    "vcas_his" 900m )
37         desVar(    "vbn_arm" 40u      )
```

```
38          desVar(     "offset" 0      )
39          desVar(     "ipre1" 100u    )
40          desVar(     "fraction" 0    )
41          desVar(     "vbp_his" 20u       )
42          desVar(     "vb2_his" 30u       )
43          desVar(     "izvt" 50u      )
44          desVar(     "d0" 1.2      )
45          desVar(     "d1" 0     )
46          desVar(     "pol" 1       )
47          desVar(     "vh2" 50m     )
48          desVar(     "vhm" 1       )
49          desVar(     "vbn_his" 40u       )
50          desVar(     "Q" 1         )
51          desVar(     "vdd" 1.2     )
52          desVar(     "vh" 200m     )
53          desVar(     "vhm2" 1      )
54          desVar(     "vbn_pa" 40u    )
55          desVar(     "s" 0         )
56          desVar(     "c_p" "s"     )
57          desVar(     "c_n" "s"     )
58          desVar(     "c_r" "s"     )
59          desVar(     "c_c" "s"     )
60          option(  'nthreads  "4"
61             'multithread  "on"
62             'reltol  "1e-2"
63          )
64          temp( 27 )
65
66          run()
67
68          out = outfile("/home/garbolin/Desktop/
               new_design/fullchain_study/results.txt" "
               a")
69          selectResult('tran)
70          plot(getData("/vout_cfd_amp3"))
71          zct\ discr = (cross(VT("/out3") 0.6 1 "
               raising" nil nil) - 2e-08)
72          zct\ cfd\ amp = (cross(VT("/vout_cfd_amp3")
               0 1 "falling" nil nil) - 2e-08)
73          fprintf(out "%g %g \n" zct\ discr zct\ cfd\
               amp)
74          close(out)
75       )
76    )
77 )
```

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