TOFPET ASIC Characterization Results

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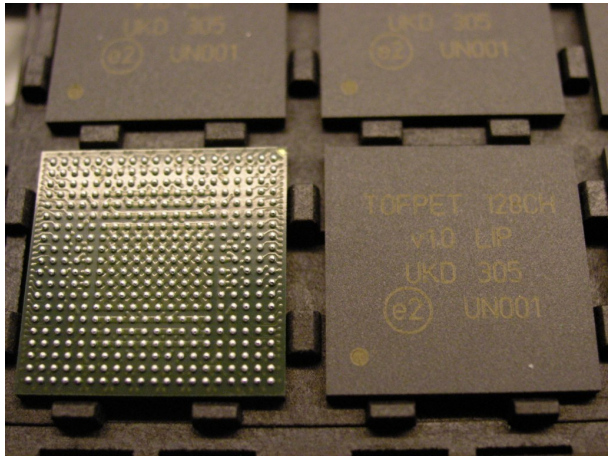
"The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/ 2007-2013) under Grant Agreement n°256984."

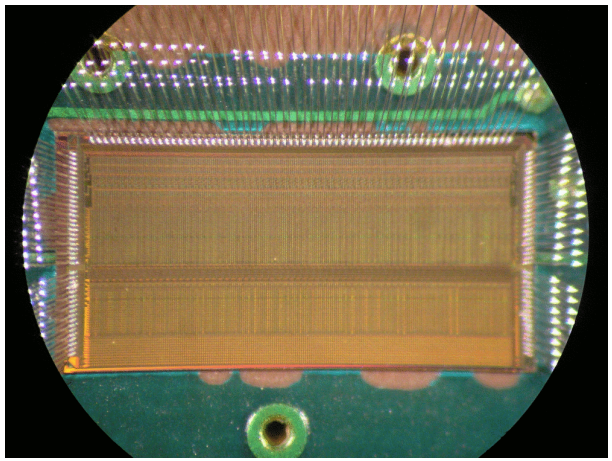
Workshop on Real time, self triggered
front end electronics for multichannel detectors
INFN Torino 27-28 November 2013

Outline

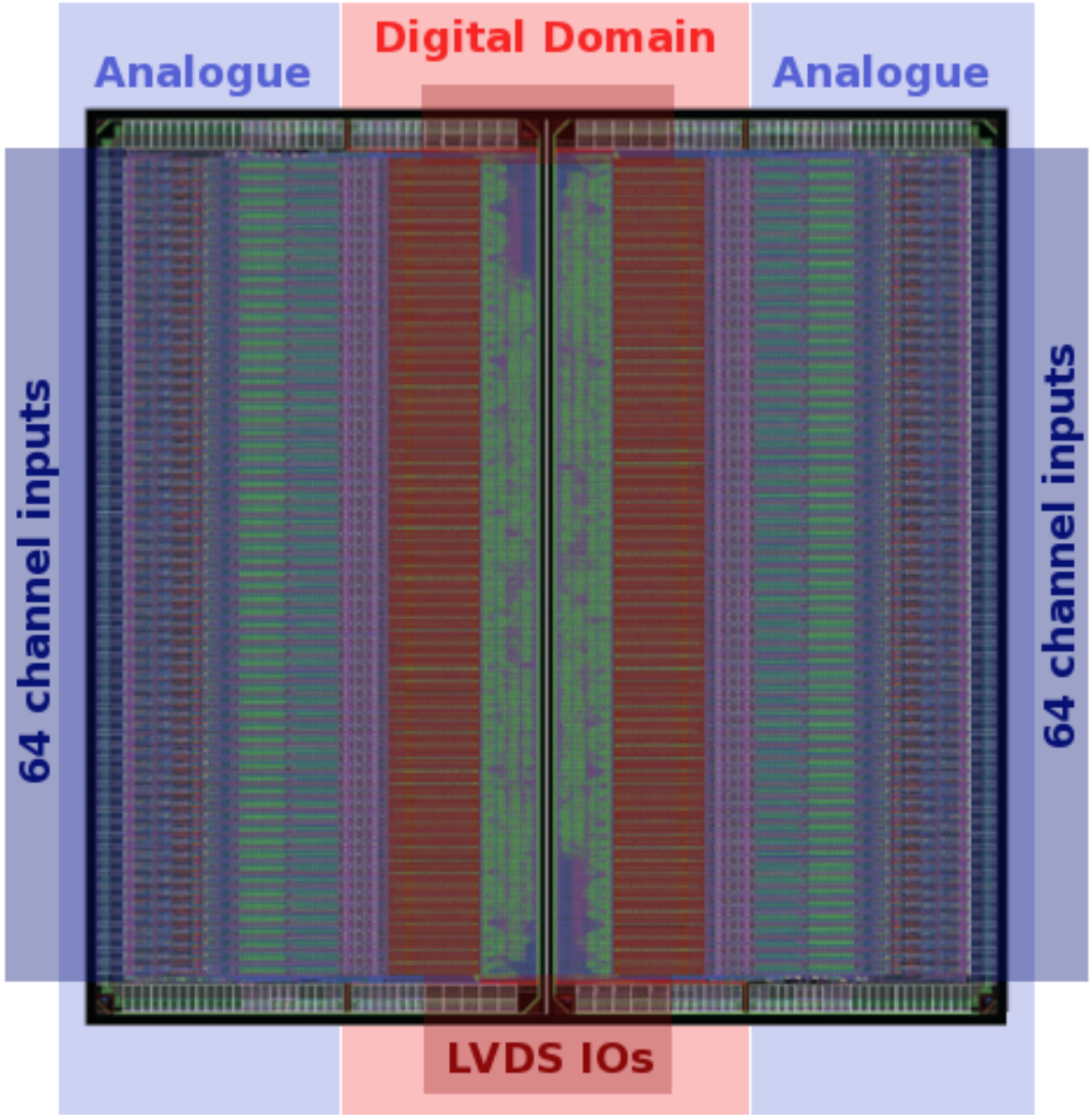
from last session...

- one-shot submission (prototype, system chip) with CERN engineering run (June 2012)
- 64-channel ASIC
- CMOS 130 nm
- 17x17mm BGA package for 128 SiP
- chips received February 2013
- 2 independent test setups (Torino, Lisboa)
- setups for test of packaged and bare dice





128-channel System-in-a-Package



Context

- **Design of a low power SiPM readout ASIC for Time of Flight applications**
- integrates signal conditioning and discrimination circuitry and high-performance TDCs for each of 64 independent channels
- targets 25 ps r.m.s. intrinsic resolution and features fully digital output
- TOFPET ASIC developed in the framework of the **FP7 project EndoTOFPET-US**
  - PET time-of-flight detector plate (4000 channels)
  - MPPC (16-channel arrays, 3x3 mm2) and LYSO crystals
  - Coincidence time resolution (CTR) 200 ps (FWHM)

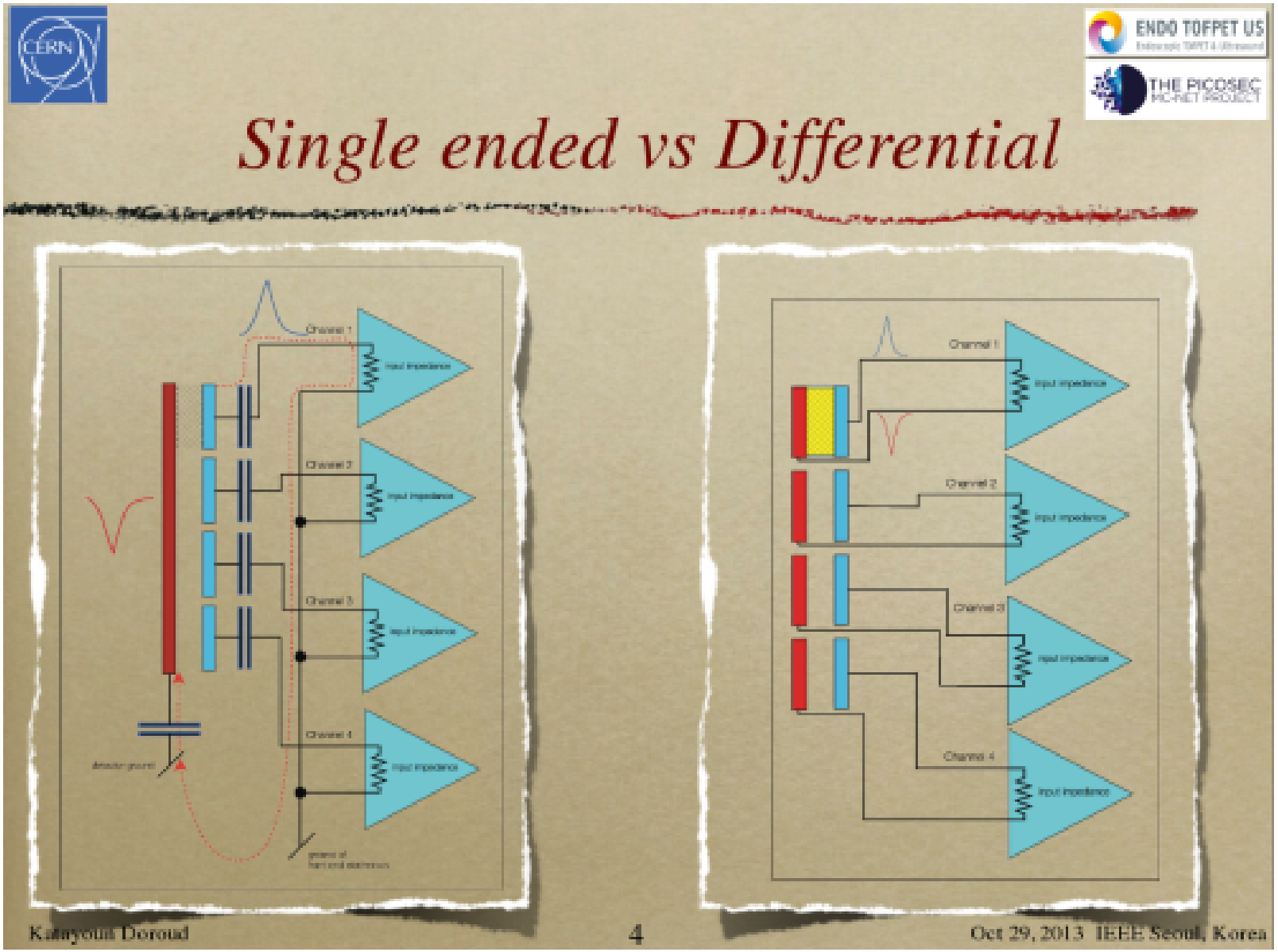
Questions and Answers - part I

- The TOFPET ASIC features **single-ended inputs**

↪ Is such a chip suitable for Fast Timing Applications?

Outline

Differential vs. Single-Ended readout



Differential vs. Single-Ended readout

The message is:

- *Differential readout is essential to minimize cross-talk and common mode noise.*

Therefore absolutely necessary for precise timing.

What we need for differential readout:

(a) A fast differential amplifier/discriminator

(b) A detector that generates a differential signal

Katsuyuki Doroud 5 Oct 29, 2013 IEEE Seoul, Korea

Differential: to be or not to be?

- less sensitive to ground bounce, board-to-board (MPPC, ASIC) ground disturbances, crossing power boundaries
- In principle, no signal return through ground.
- This holds true if:
  - current flows in a closed loop and if the differential sum is 0 everywhere in the loop
  - ↪ Otherwise, current does flow to ground and ground caring is needed!
- Severe routing constraints: symmetry of pair signalling is crucial
  - same length, to avoid current return to ground
  - same separation, to keep differential impedance constant
- The large signal of the SiPM does induce coupling into neighbouring traces or planes
  - inductive or capacitive, even if differential impedance is low
  - use of a plane under differential lines?
    - reduces self-impedance
    - but sets these lines at loop currents
- Excess off-chip passive components (AC coupling)
- Chip pad number doubled

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Single-Ended: to be or not to be?

- A flood of disadvantages...
  - very susceptible to ground loops
  - suspeptible to board-to-board ground disturbances
  - signal return via common ground - can cause electrical crosstalk
  - ground bounce due to switching currents
- But, all above can be minimized:
  - with an appropriate grounding scheme
  - if signal travels in a low noise surrounding and/or is properly shielded
- Question of The Day:

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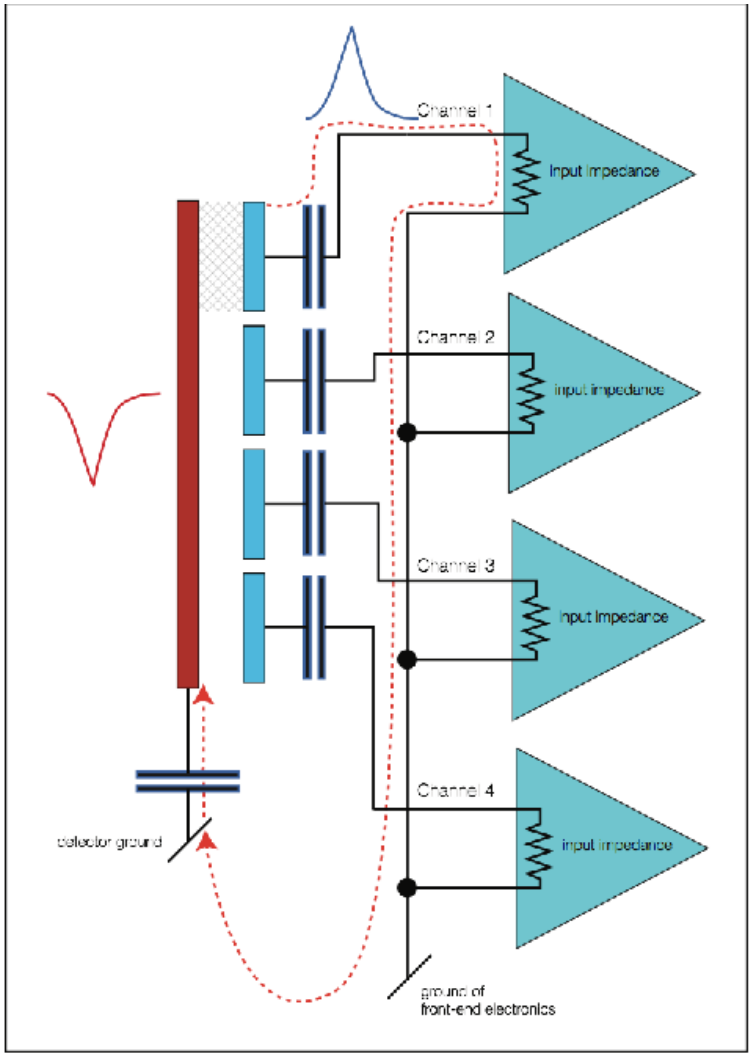
Good timing performance with a Single-Ended chip. How?



- minimize the stray inductance of the current return path
- care the ground of the ASIC
- design a proper HV biasing scheme

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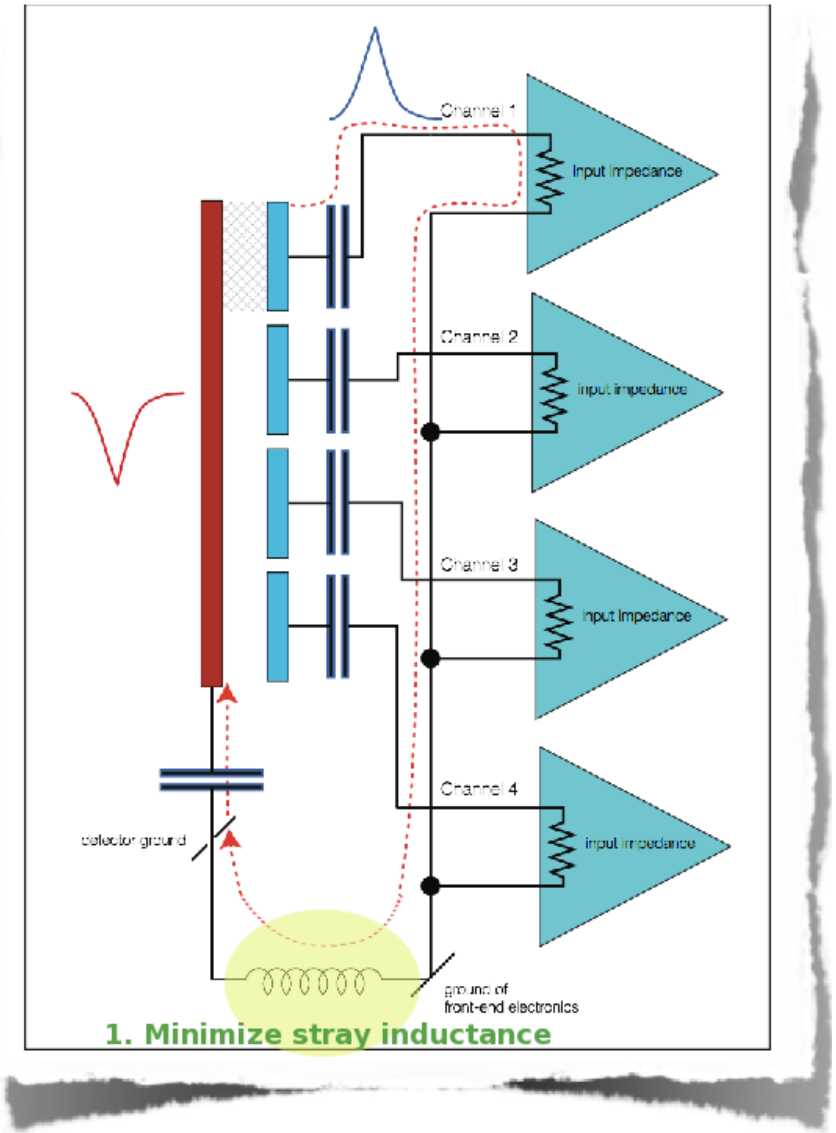

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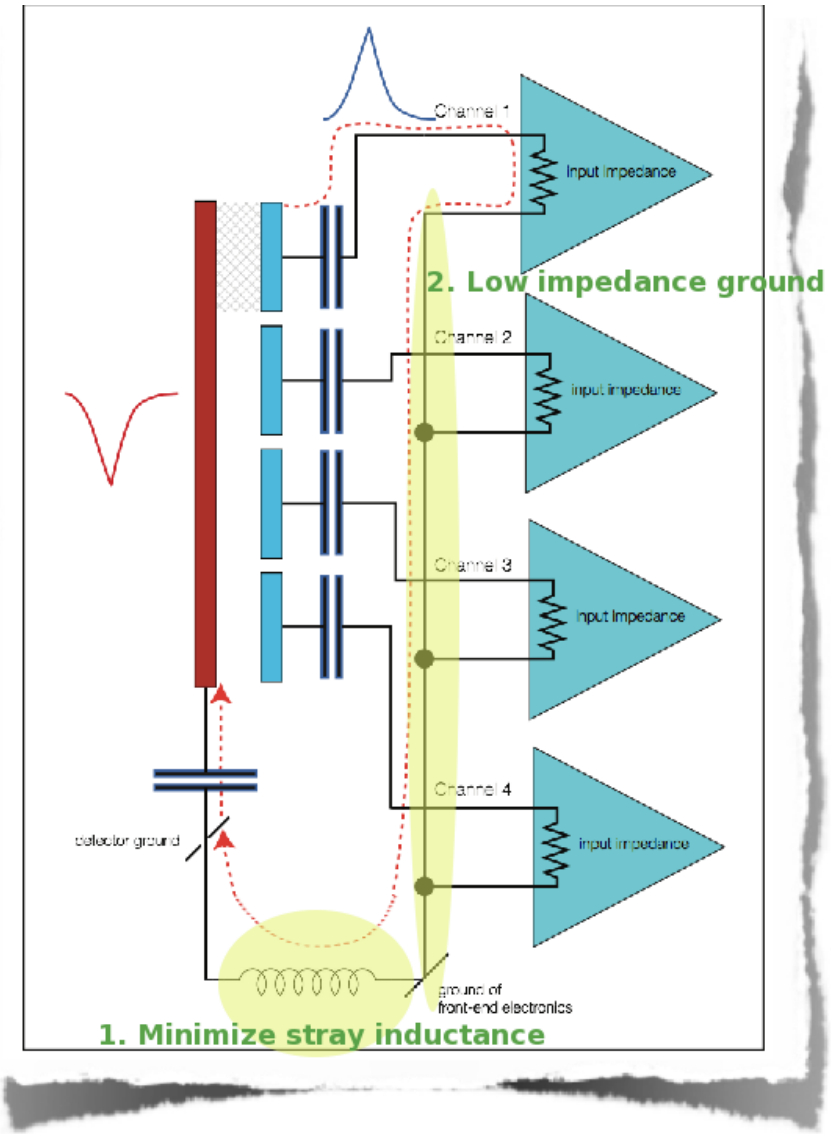

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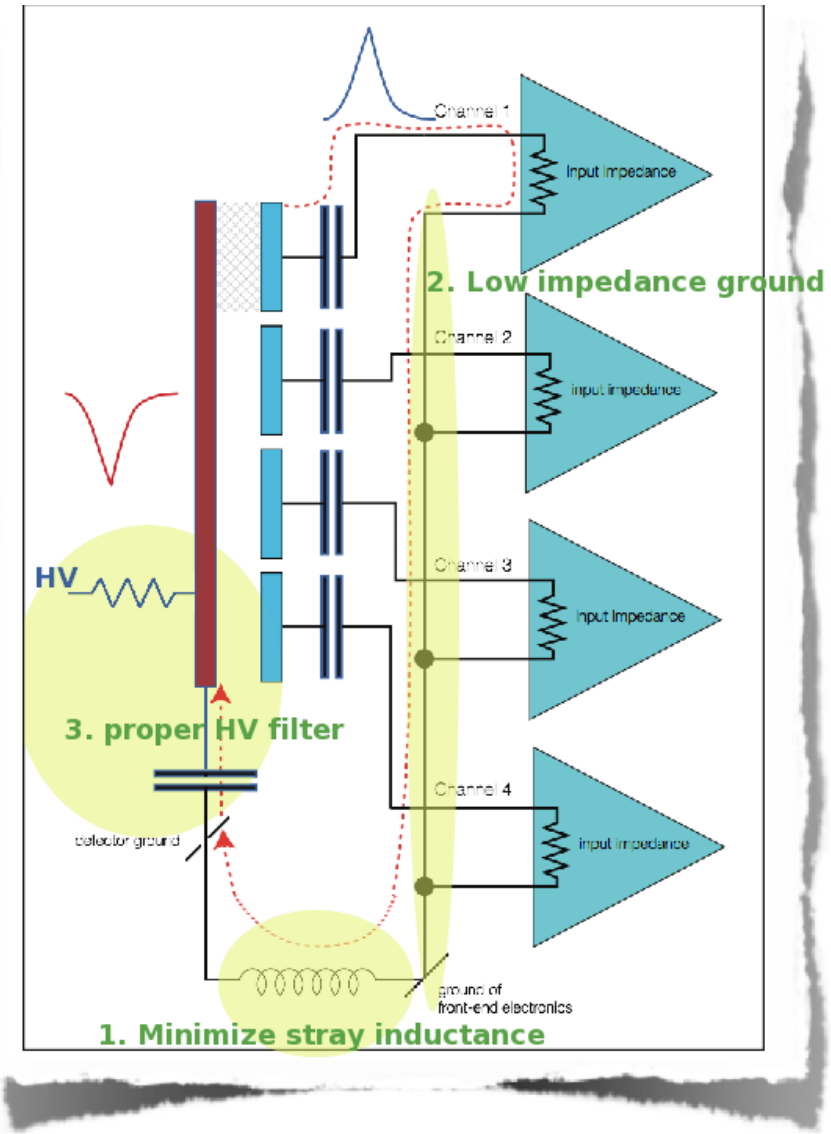

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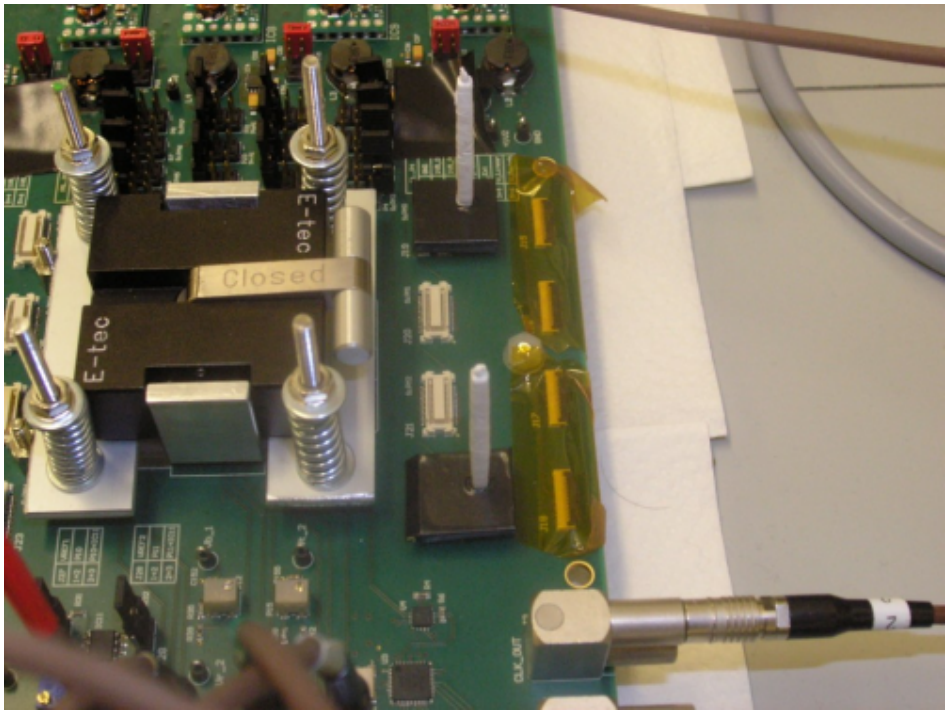
Outline

Test Setups Packaged Dice 1&2

First test boards with/without BGA socket

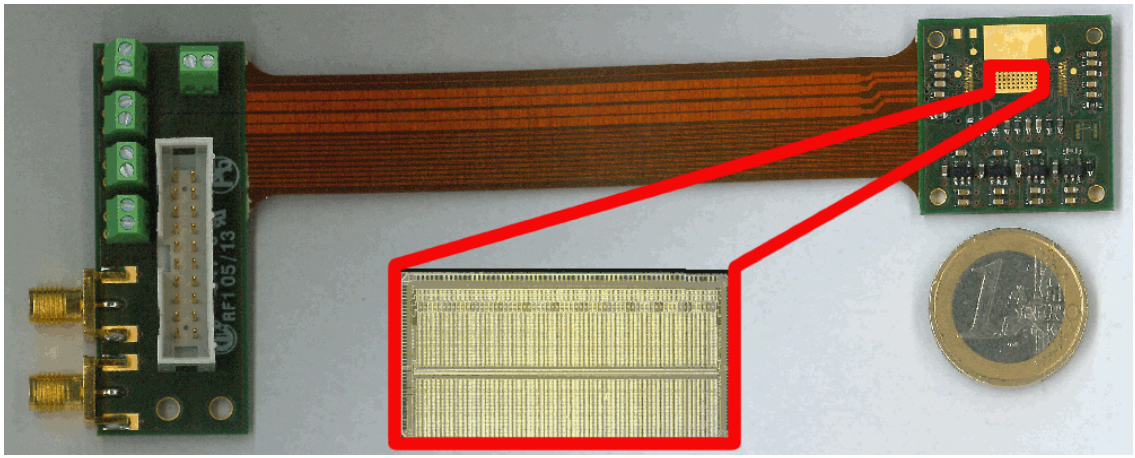
- Electrical characterization
- Coincidence tests: single crystal and matrices
- Severe power bouncing - package, test board, setup

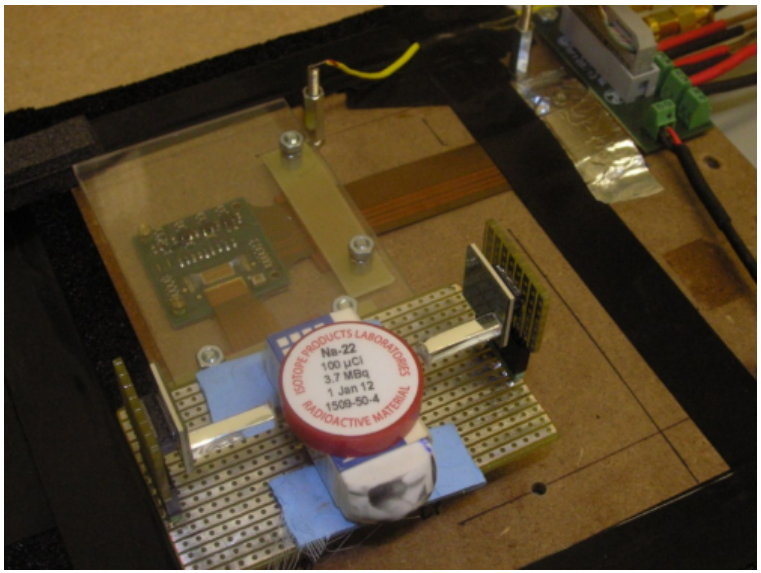


Test Setup Bare Die 1

Test board designed for and by the 4DMPET collaboration[1]

- Electrical characterization
- Tests with MPPCs (SPTR, MPTR)
- Coincidence tests



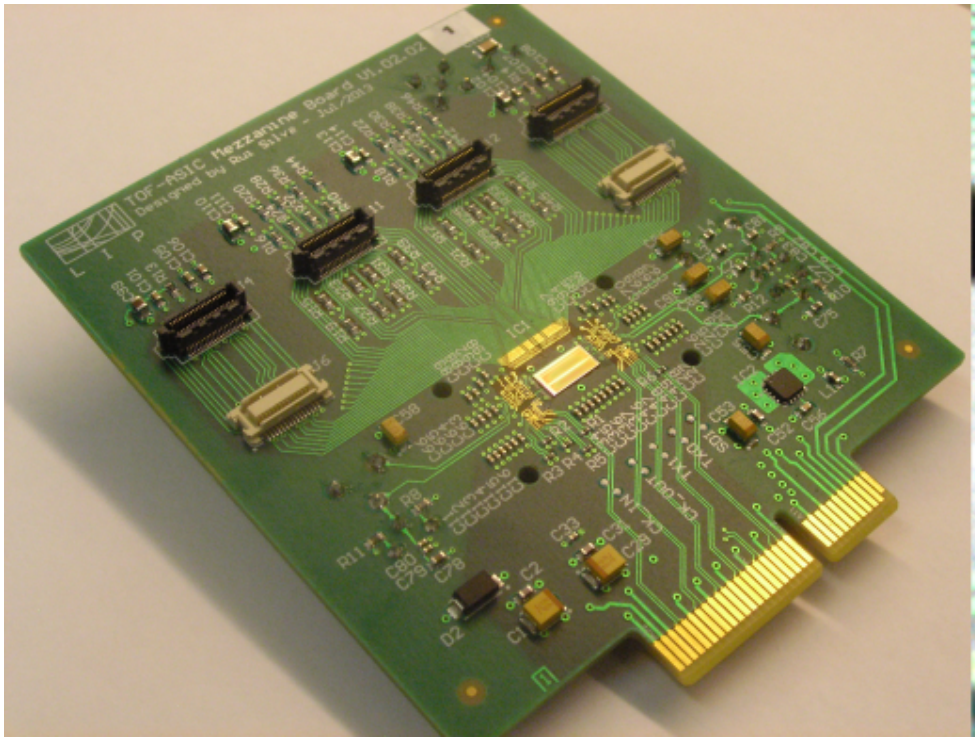


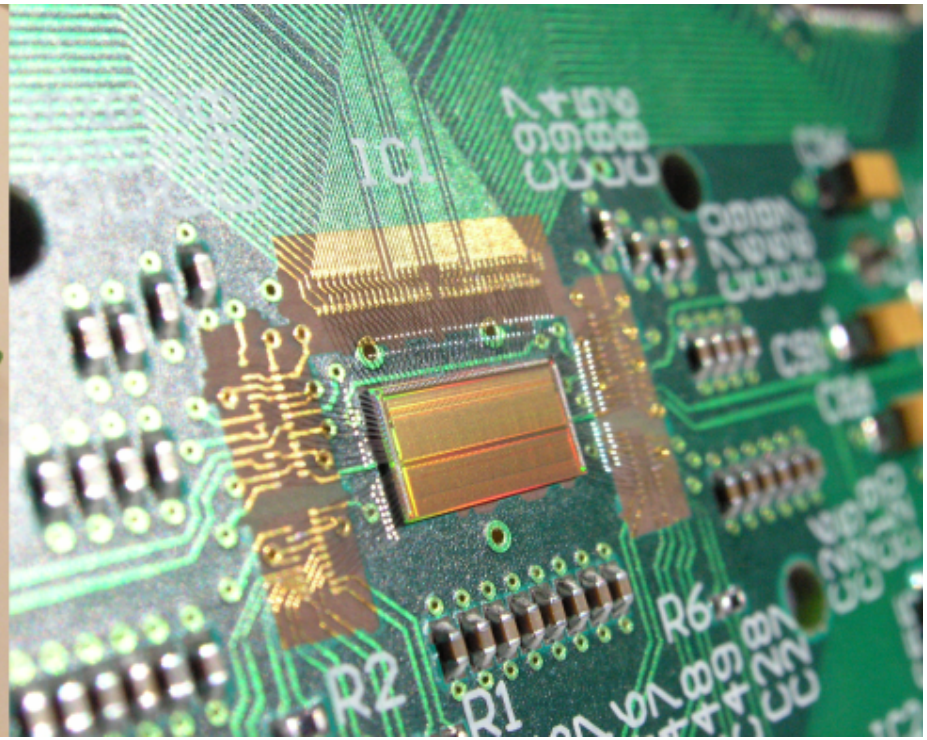
[1] Acknowledgement: Marco Mignone, Richard Wheadon

Test Setup Bare Die 2

New board designed at LIP - ready since October 2013

- Electrical characterization
- ~~Tests with MPPCs (SPTR, MPTR)~~
- Coincidence tests



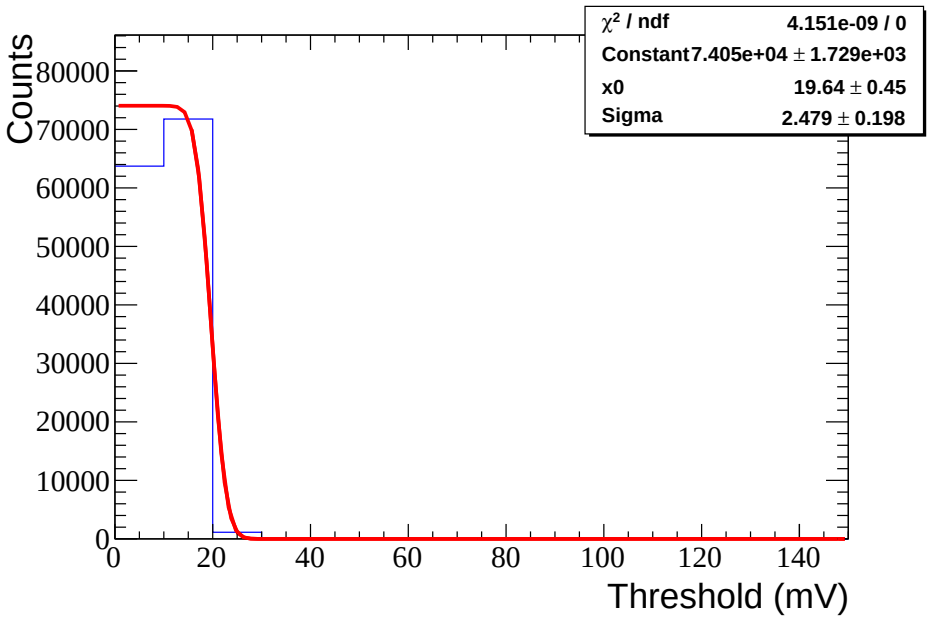


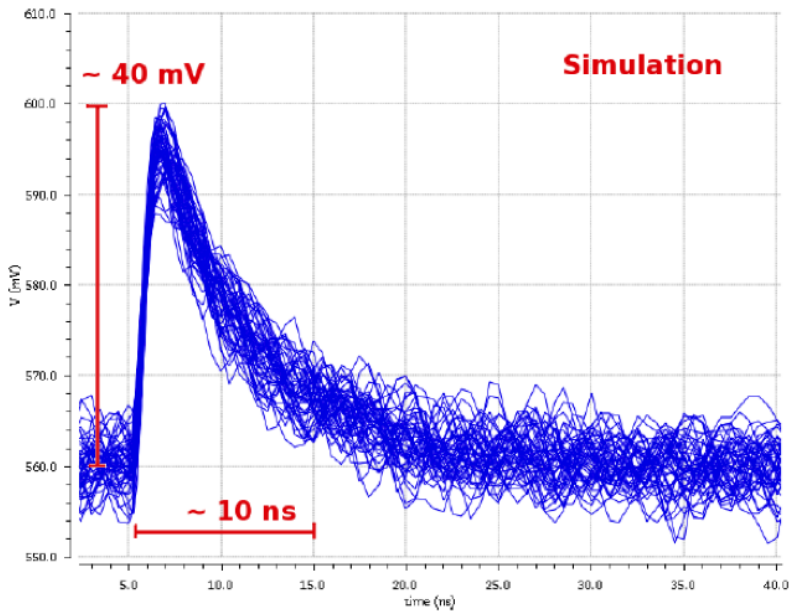
Setup for Characterization

- bare die directly bonded on the test board
- setup includes power supplies, low jitter reference clock source, FPGA interface and bias voltage for the SiPM arrays
- latest tests with MPPC S12642-0404PB-50 (TSV MPPC array)
- FPGA handles:
  - ASIC configuration and data reception
  - generates a test pulse which is delivered to the ASIC or to a pulsed laser driver for testing purposes
  - TP: ajustable timing but synchronous to the reference clock

Front-end noise estimation

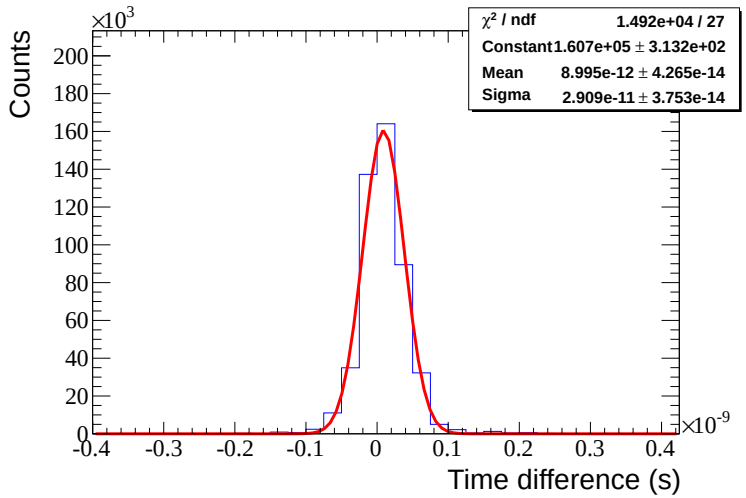
- number of events as function of threshold (both thresholds set to the same value)
- fit to a cumulative probability distribution function
- **2.5 mV r.m.s.** (agrees to simulation results)





TDC Quantization Error

- **Step 1**: TDC calibrated with a test pulse sweep across 50 ns (500 ps step, 10000 pulses p/ step)
- **Step 2**: Correct for TDC non-linearity
- **Step 3**: Trigger simultaneously two channels and measure time difference (removes common mode test pulse jitter)



- Distribution with 29 ps r.m.s.,
  corresponds to a **per channel error of 21 ps r.m.s.**

Test setup for SPTR and MPTR tests

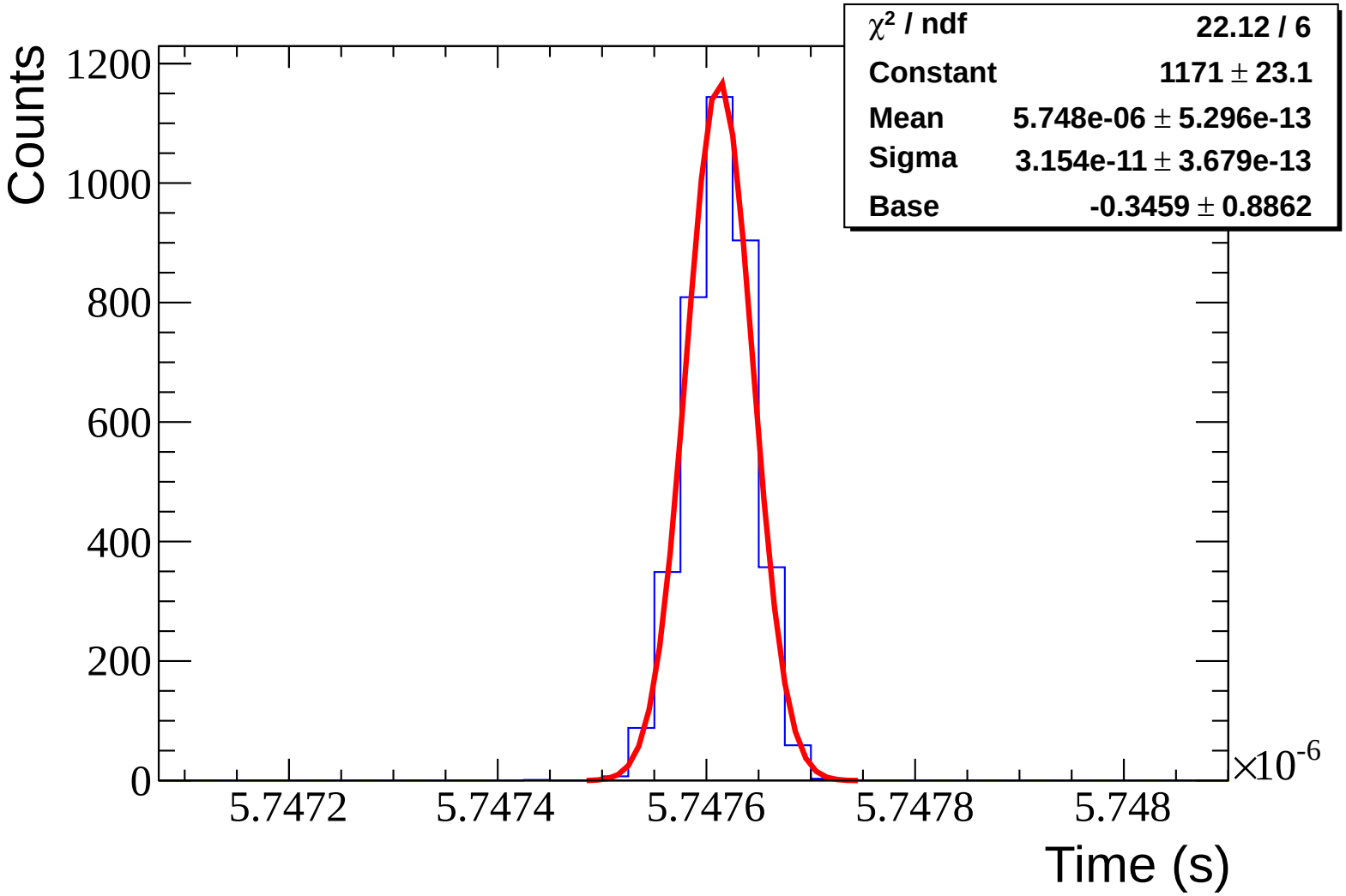
- Tests with Bare Die
  - MPPC: TSV arrays (3x3 mm2)
  - (for CTR only): $3.1x3.1x15mm^2 LYSO$
  - nominal: 160 MHz, DVDD=1v5
- PicoQuant Laser
  - MPTR: LI=1.5, no optical attenuator ($N_{ph} >> 1000$)
  - SPTR: LI=7.5, WITH optical attenuator ($N_{ph} = 1$)
- Nominal test conditions:
  - T = 18-20 C
  - TP rate = 80 KHz
  - V_{thE} approx 500mV above $V_{th,noise}$
  - V_{thT} approx 10mV[2] above $V_{th,noise}$

[2]for CRT with LYSO, nominal V_{thT} setting is to 100 mV above noise (corresponds to a threshold of 2-3 equivalent photoelectron charge)

Multi-Photon Time Resolution

- Laser: no optical attenuator ($N_{ph} > 1000$)

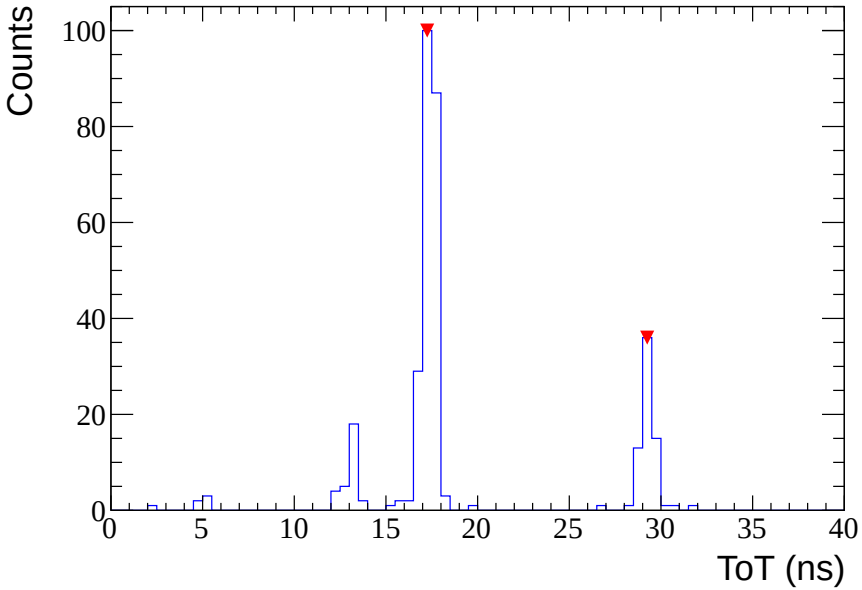
↪ 32 ps r.m.s., includes jitter from the laser and the test pulse

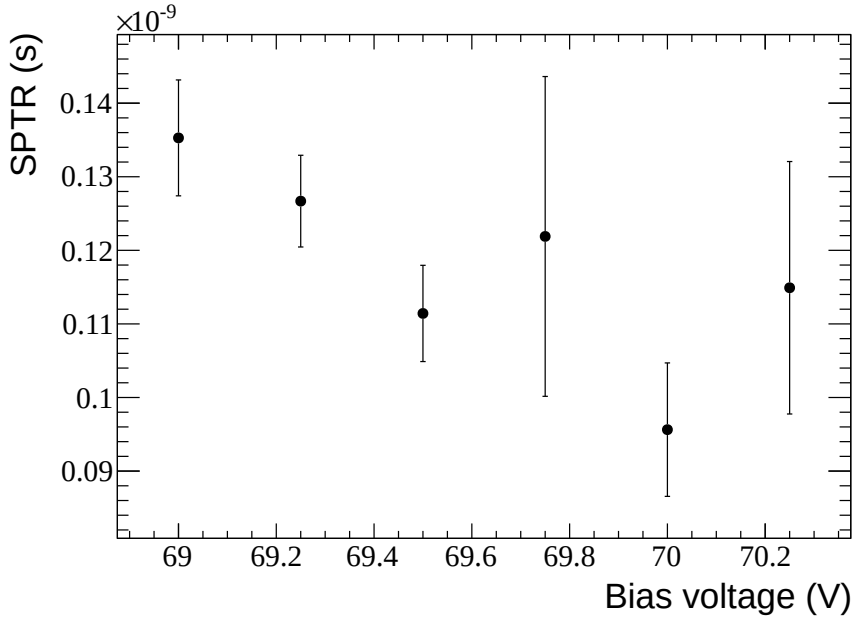


Single-Photon Time Resolution

- Laser: w/ optical attenuator ($N_{ph} = 1$)
- both thresholds set to 0.5 p.e. level
- laser triggered at 80 kHz rate, known time in respect to the start-of-frame
- ToT distribution of events within 1 ns of the expected laser pulse time show the 1 photon and 2 photon peaks

↪ 110 ps r.m.s., after optimization of the HV

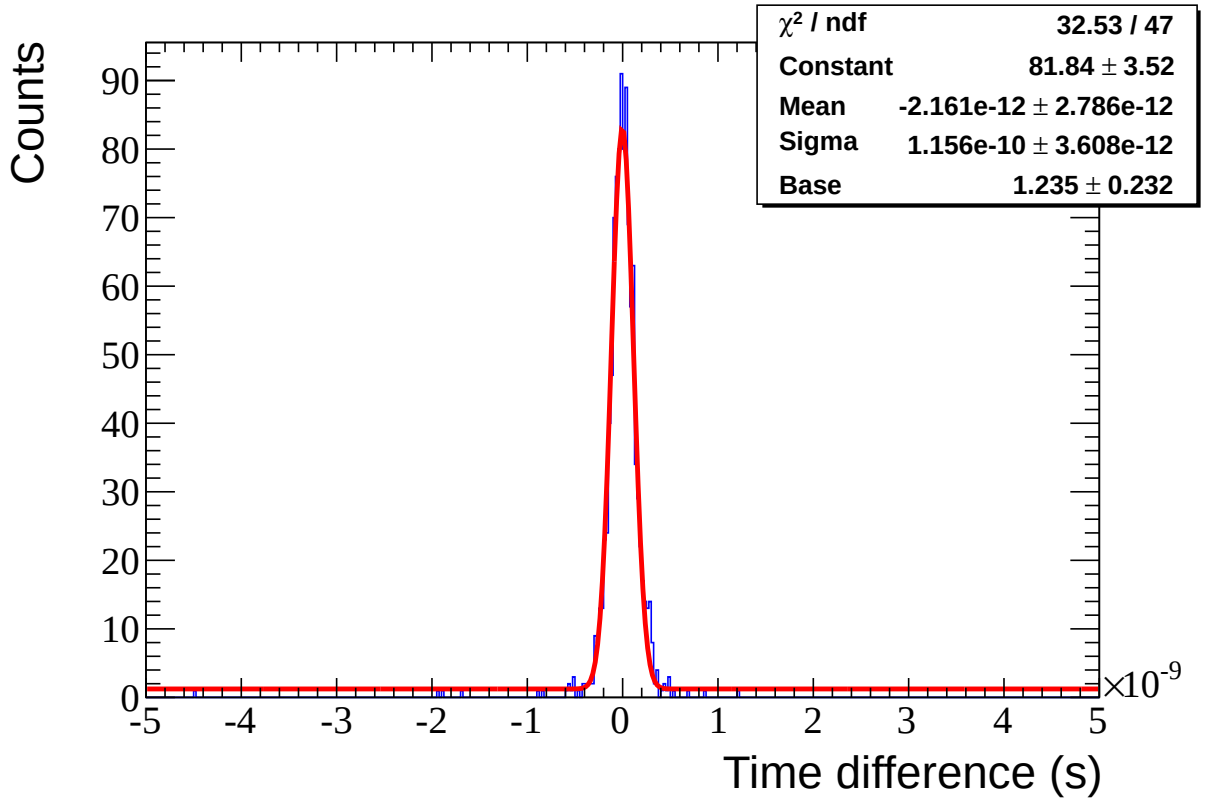




Coincidence Time Resolution

- Two MPPC S12642-0404PB-50 (TSV MPPC 16-channel matrices)biased and connected to the ASIC
- Only one pixel with a 3.1x3.1x15 mm3 LYSO crystal
- All channels set to a 2 p.e. charge (sweep 1-10 p.e.) equivalent threshold
- Geometrically neighbouring channels (avg 4-6) produce data due to optical crosstalk on epoxy
- Events selected within 1σ of the photopeak

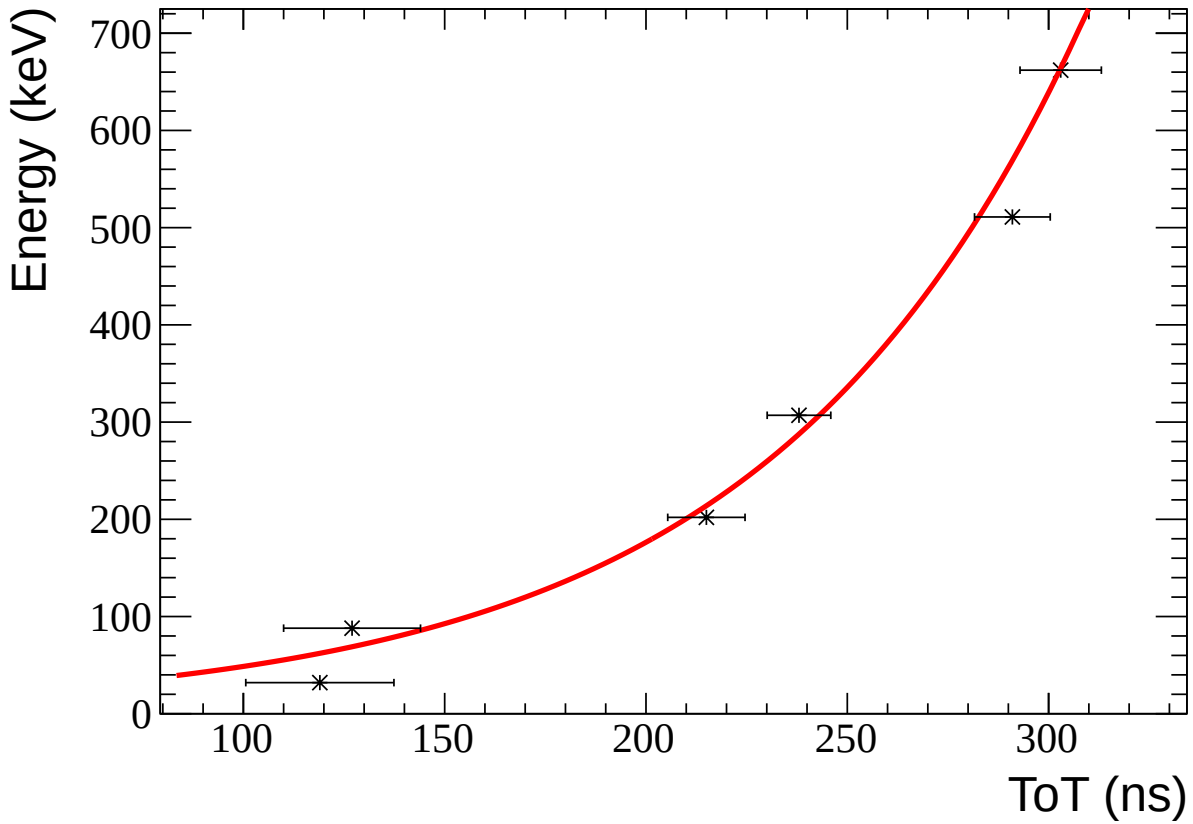
Coincidence Time Resolution - **preliminary**



- **CTR = 270 ps FWHM**
- Result does not depend on the threshold setting other channels
- CTR value is higher than the extrapolation based on SPTR meas.
  ↪ under investigation

Energy Calibration - **preliminary**

- ToT vs. Qin characteristic is non-linear
- Data aquired with ^{22}Na, ^{176}Lu, ^{137}Cs
- Fit to an exponential function to correct energy spectrum
- **Preliminary** energy resolution 17%



Outline

Status and Outlook

- ASIC distributed to several groups for Medical Imaging and HEP
- offspring under way
  - PASTA chip for Panda
    - readout of strips
    - Linear ToT
  - TOFPET v2.0
    - Targets time resolution better than 10 ps r.m.s.
    - Rate per channel more than 1 MHz
    - Linear ToT
    - improved energy resolution

EndoTOFPET-US FP7: Endoscopic PET and Ultrasound

Thank you!