

# Time-based readout of silicon strip sensors

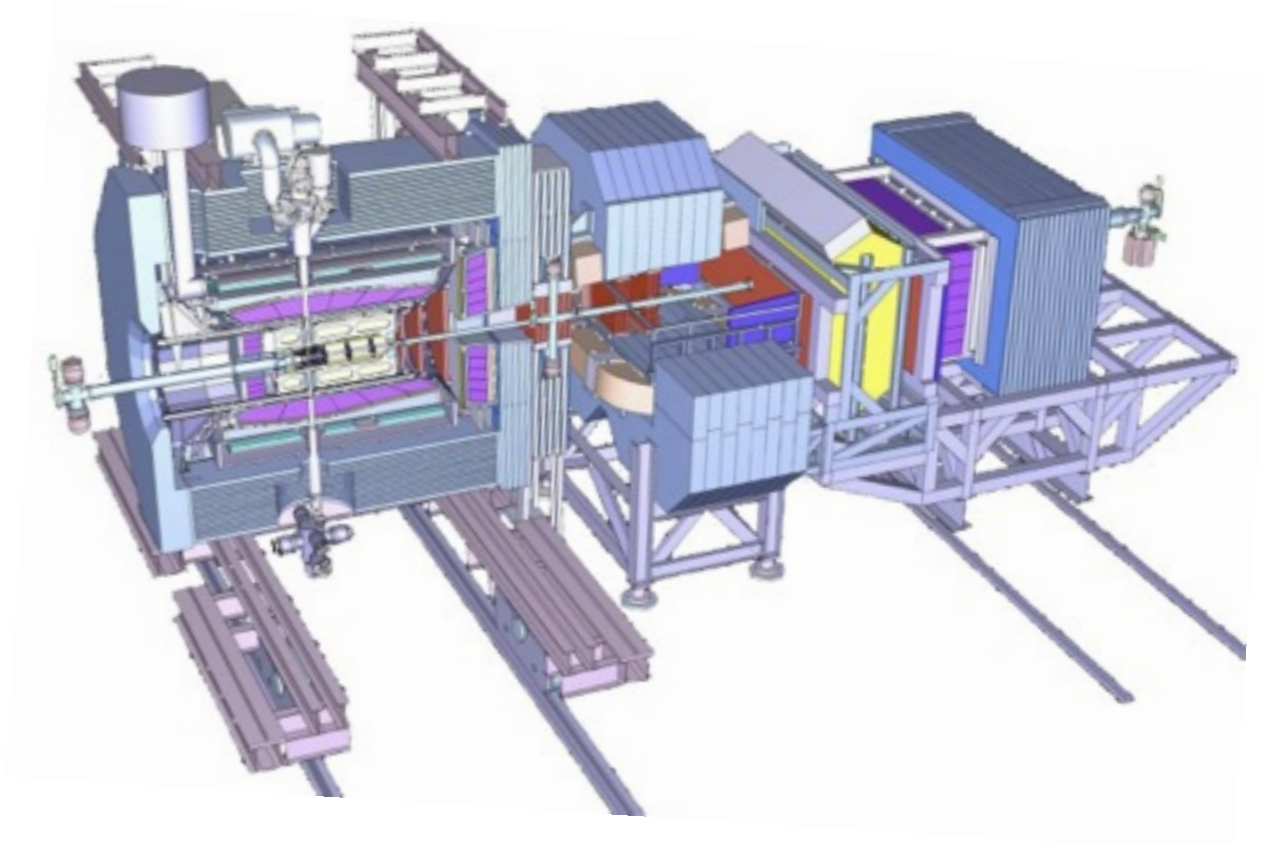
*Concept and status of the **PANDA Strip ASIC***

André Goerres

28 November 2013

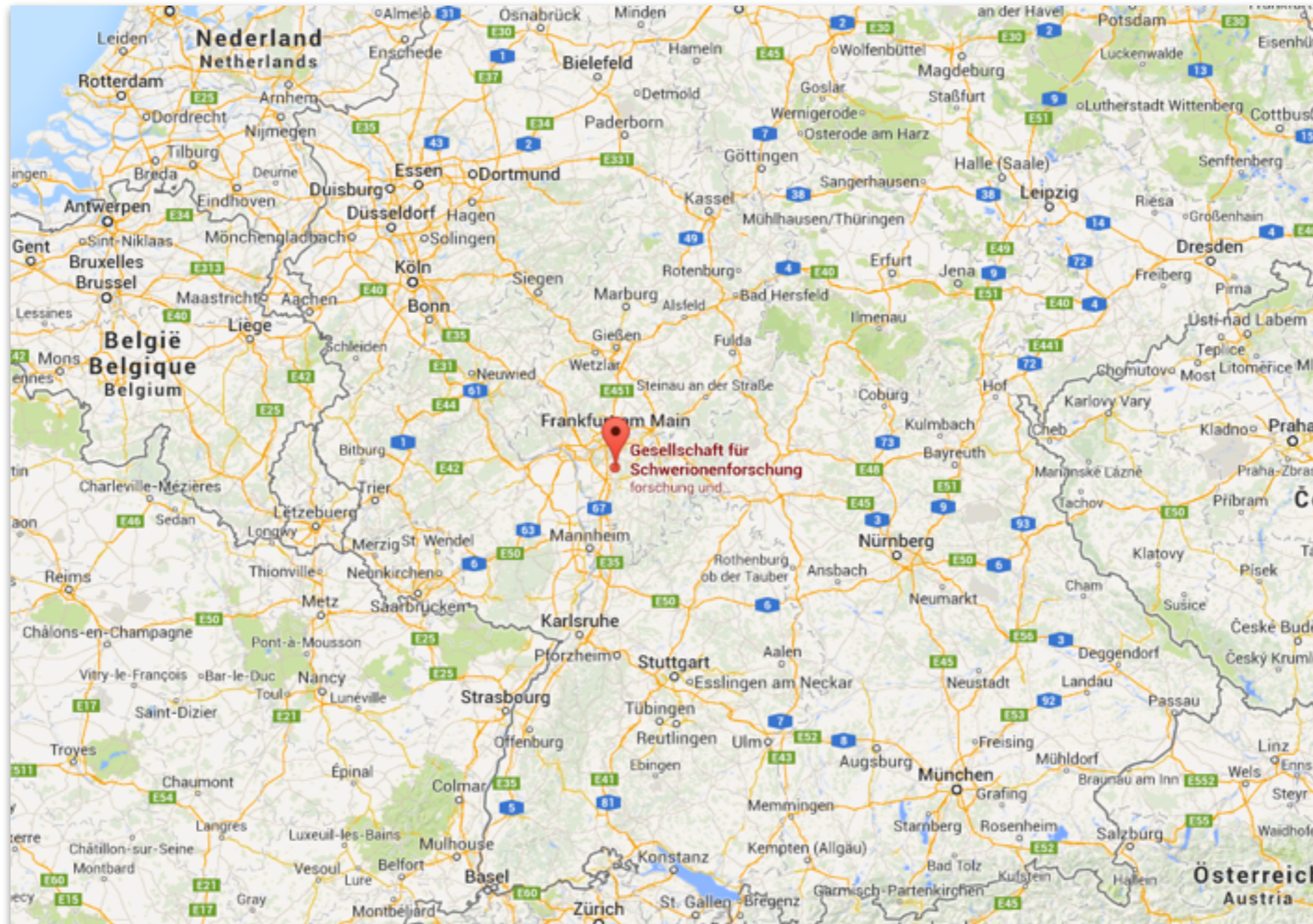
Workshop on front end electronics, INFN Torino

- Introduction
  - GSI, FAIR, PANDA, MVD
- **PANDA Strip ASIC (PASTA)**
  - Concept of the ASIC
  - Changes to TOF-PET ASIC
  - Current Status of Development
- Conclusion & Outlook





- Facility for Antiproton and Ion Research
  - Accelerator complex next to GSI





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  - Construction in progress, finish planned for 2018



Jan Schäfer, 27.07.2013

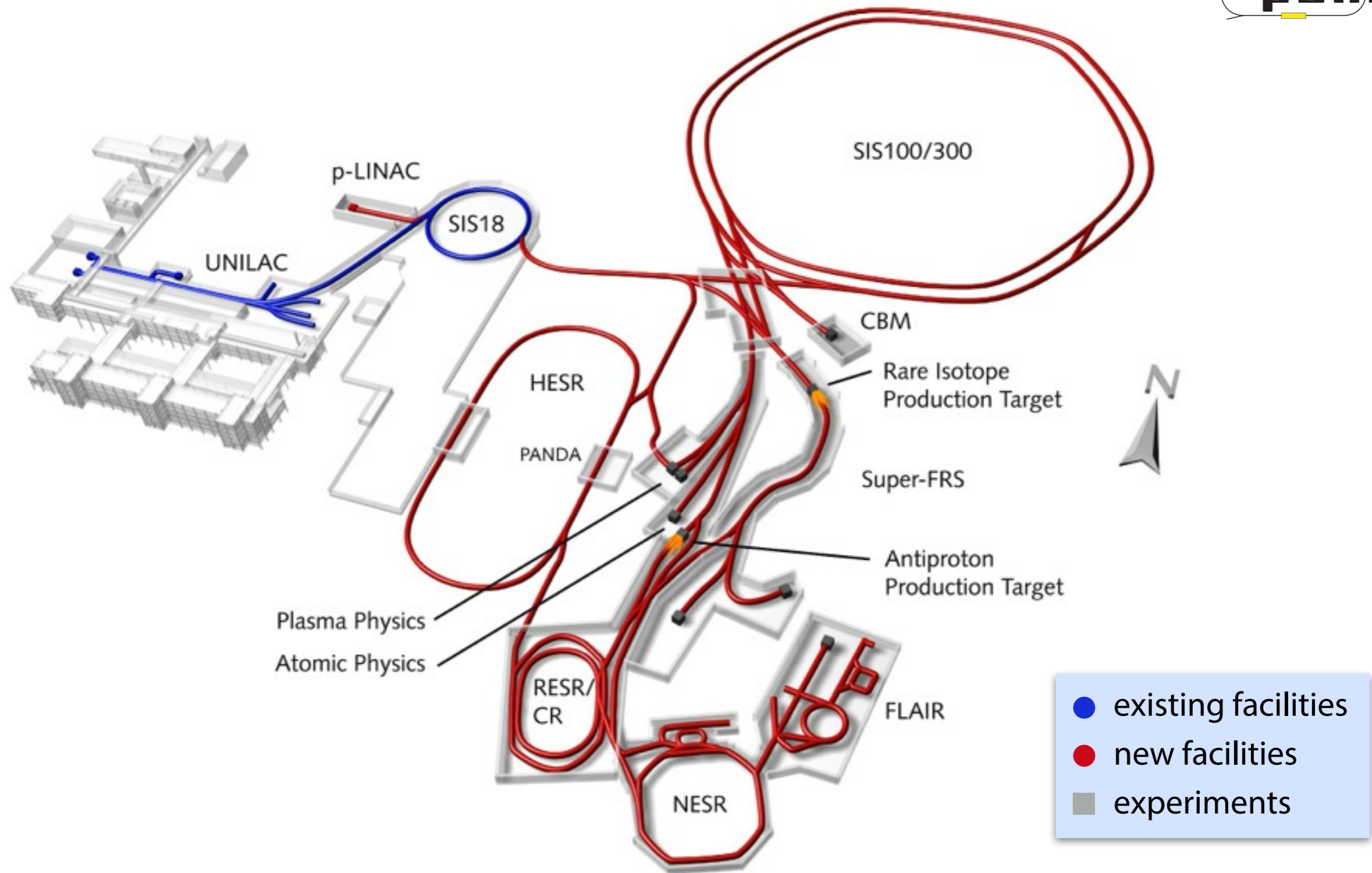


- Facility for Antiproton and Ion Research
  - Accelerator complex next to GSI
  - Construction in progress, finish planned for 2018
  - Four pillars of research:

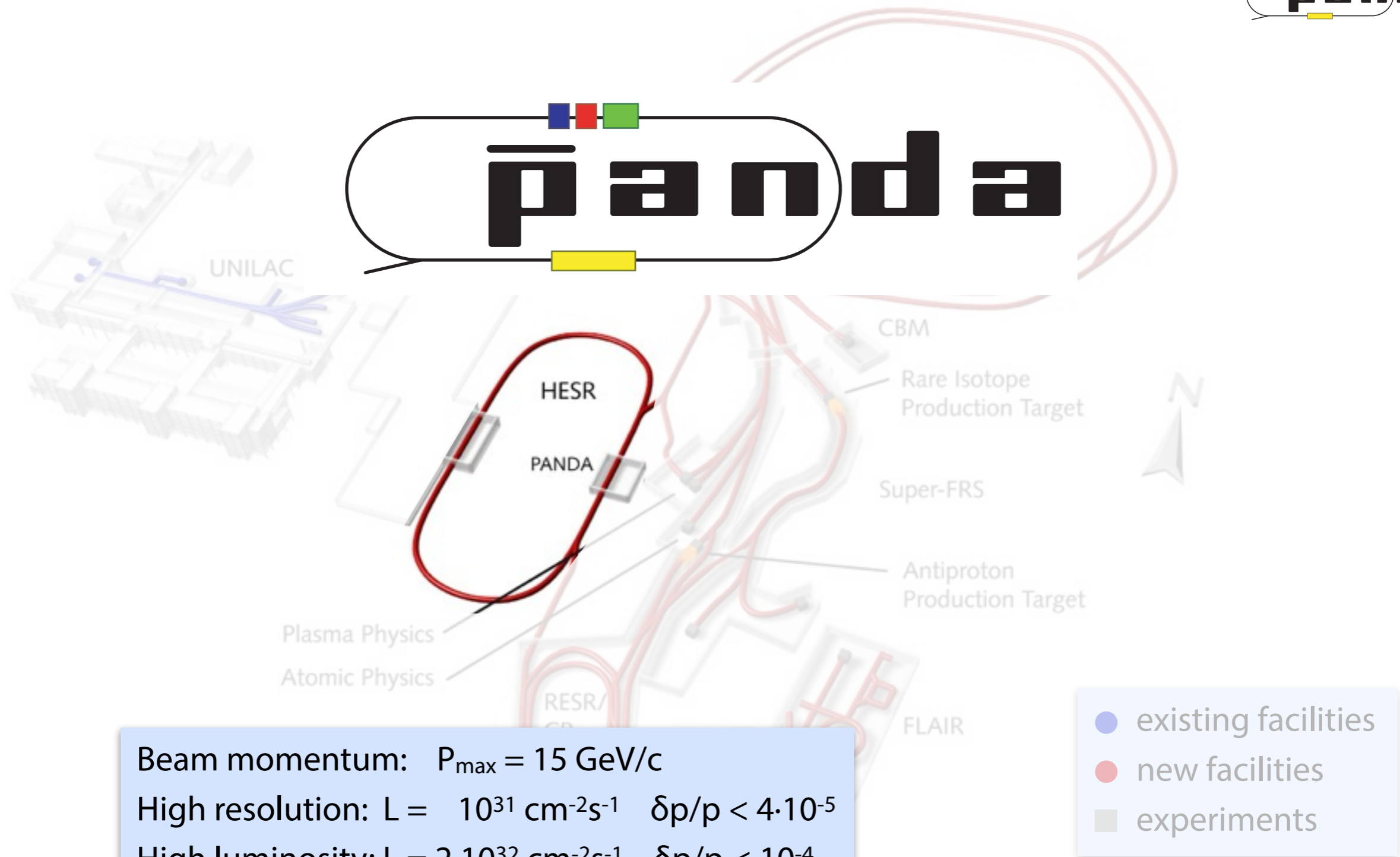
ABBA	CBM	NUSTAR	PANDA
Atom & plasma physics	Hadron physics	Nuclear structure, astro physics	Hadron physics



# FAIR Accelerator Complex



# FAIR Accelerator Complex

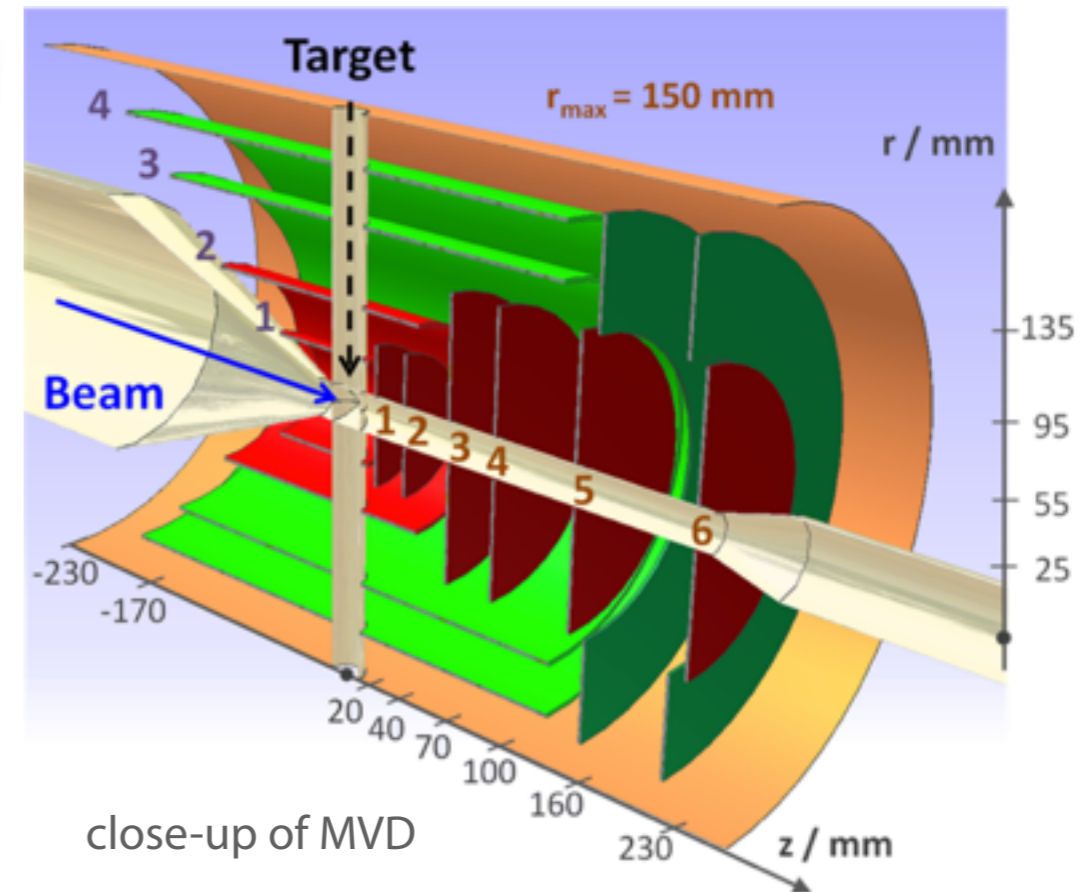
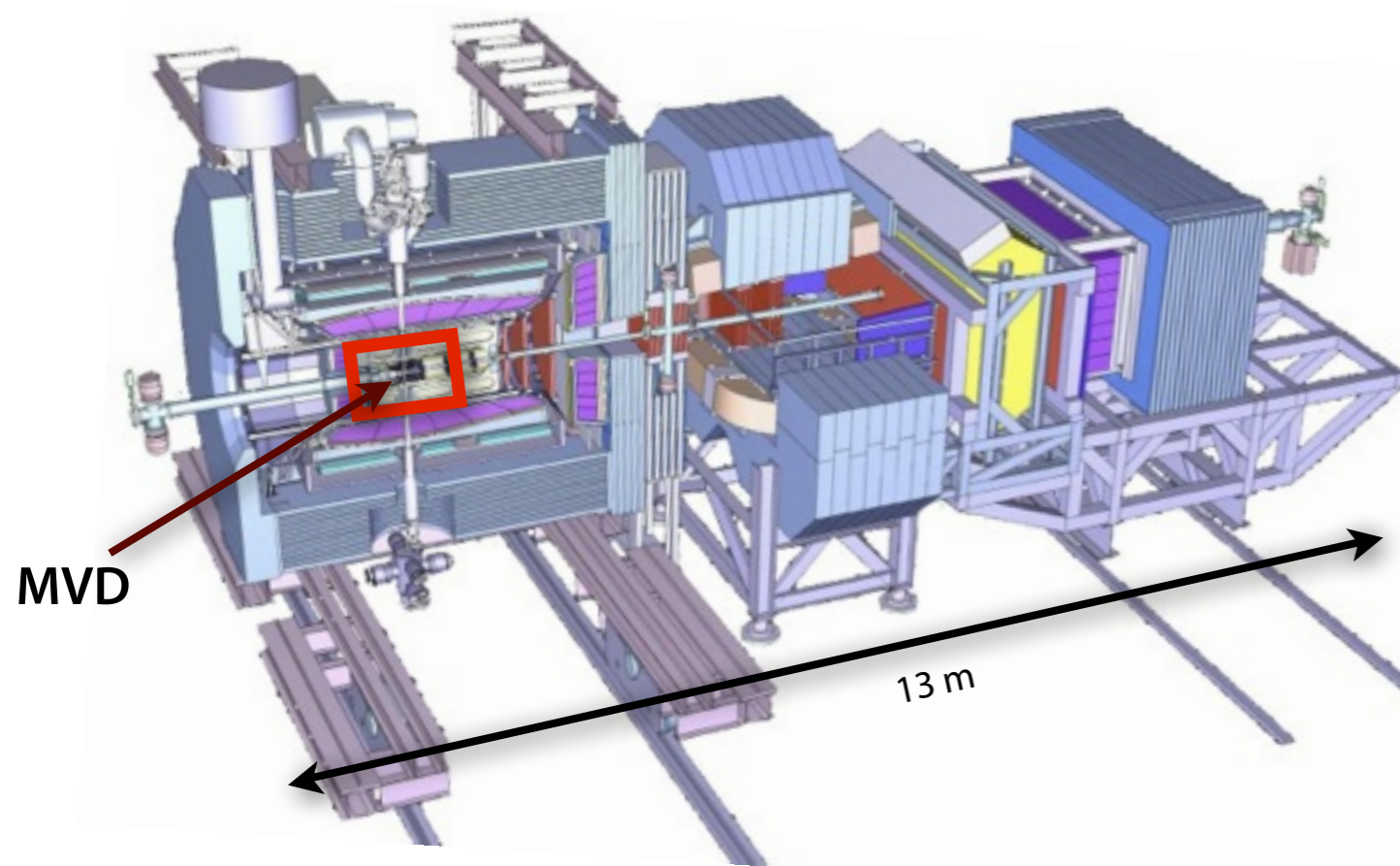


Beam momentum:  $P_{\max} = 15 \text{ GeV}/c$   
 High resolution:  $L = 10^{31} \text{ cm}^{-2}\text{s}^{-1}$   $\delta p/p < 4 \cdot 10^{-5}$   
 High luminosity:  $L = 2 \cdot 10^{32} \text{ cm}^{-2}\text{s}^{-1}$   $\delta p/p < 10^{-4}$



# PANDA Experiment and Micro Vertex Detector

Anti-Proton Annihilation at Darmstadt



- PANDA: particle detector,  $p^+p^-$  collisions with 1.5-15 GeV
  - $2 \cdot 10^7$  collisions per second, event taking untriggered
- MVD: **M**icro **V**ertex **D**etector, innermost tracker
  - Two parts: silicon **pixel** ( $10.5 \cdot 10^6$  ch.) and **strip** ( $1.6 \cdot 10^5$  ch.)



# Requirements of the MVD to Readout

- No central trigger information  
⇒ Autonomous data taking
- High event rate ( $2 \cdot 10^7$  collisions per second)  
⇒ Minimized dead time < 6  $\mu$ s  
⇒ High rate capability 40.000  $s^{-1}$
- Event building afterwards  
⇒ Accurate time information < 20 ns
- Support event identification  
⇒ Measure charge deposition  $\geq 8$  bit over dyn. range
- MVD as compact as possible  
⇒ Low power consumption < 4 mW/ch

**Time-based readout**  
- Simple & low power  
- Experience with concept (TOF-PET ASIC)

# Concept of the ASIC

- Time-based readout of silicon strips

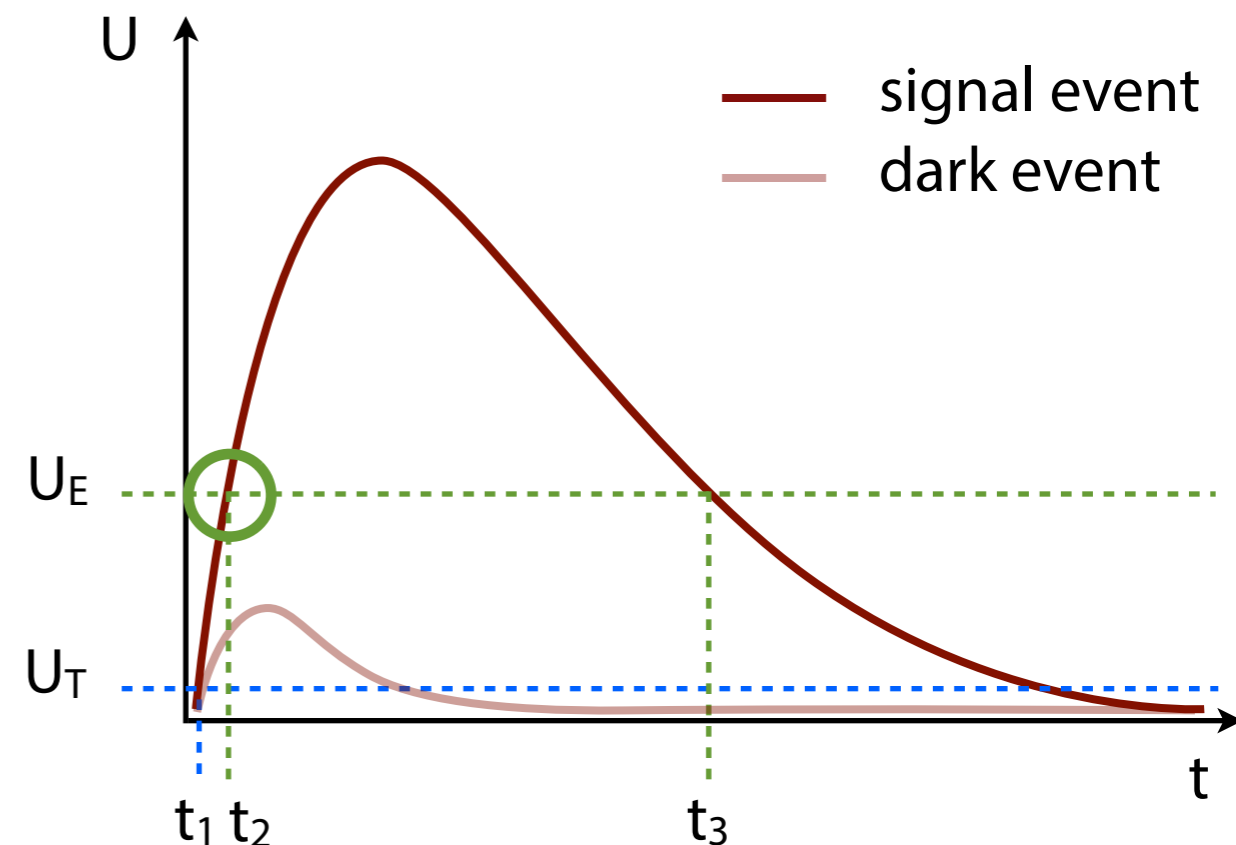
- Save time stamps (50 ps)
- Leading edge discriminator
- Charge by time over threshold

- Two TDCs per channel

- Time and energy branch (low and high threshold)
- Energy trigger ( $t_2$ ) validates time trigger ( $t_1$ )
- Reduces susceptibility to dark counts

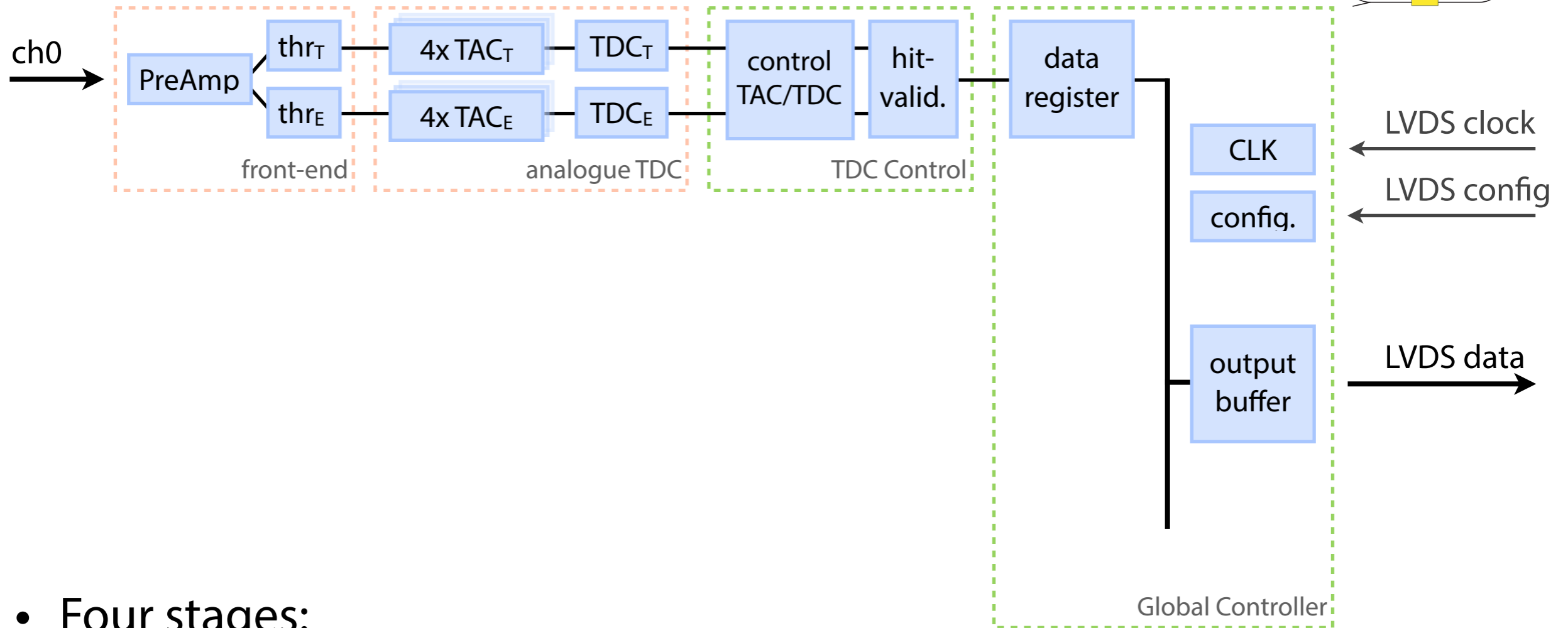
- Concept already realized: TOF-PET ASIC

→ Talks by Manuel D. Rolo (Tuesday, Thursday)



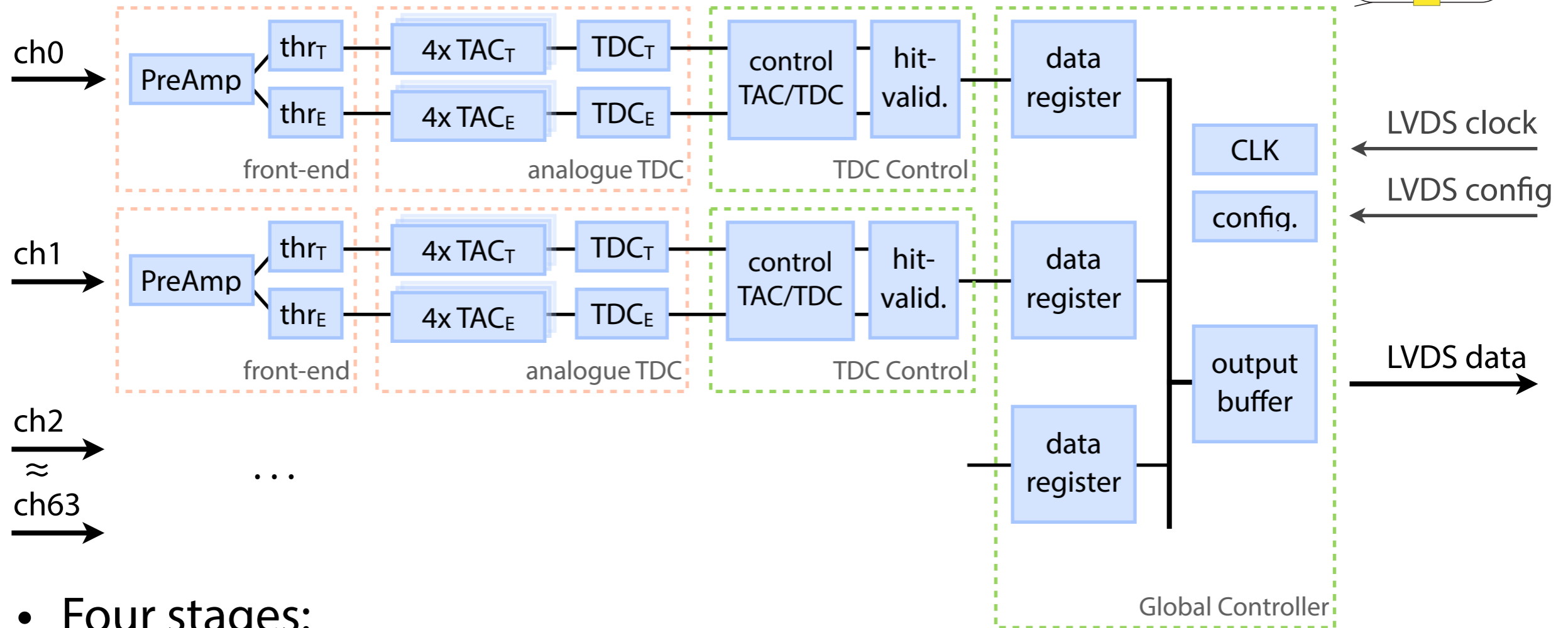


# Concept of the ASIC



- Four stages:
  - **Front-end** (analogue)
  - **TDC** (analogue)
  - **TDC Control** (digital)
  - **Global Controller** (digital)

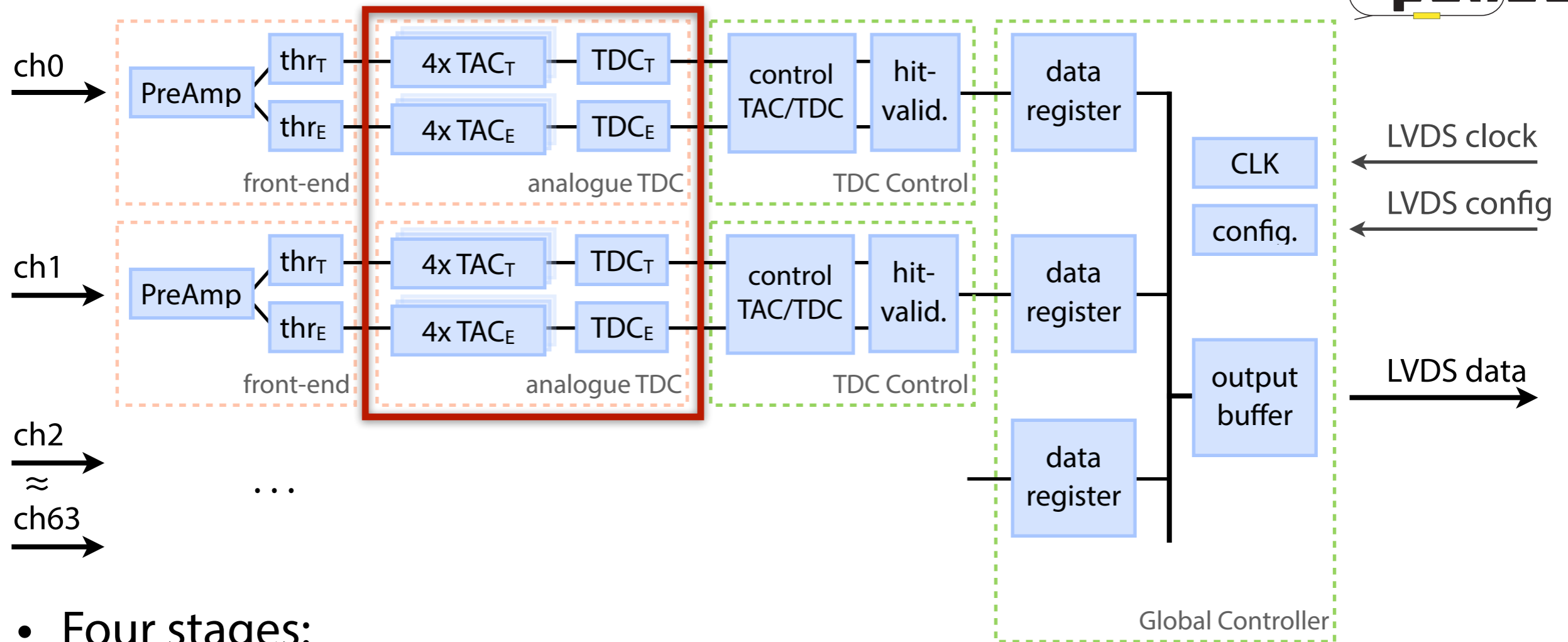
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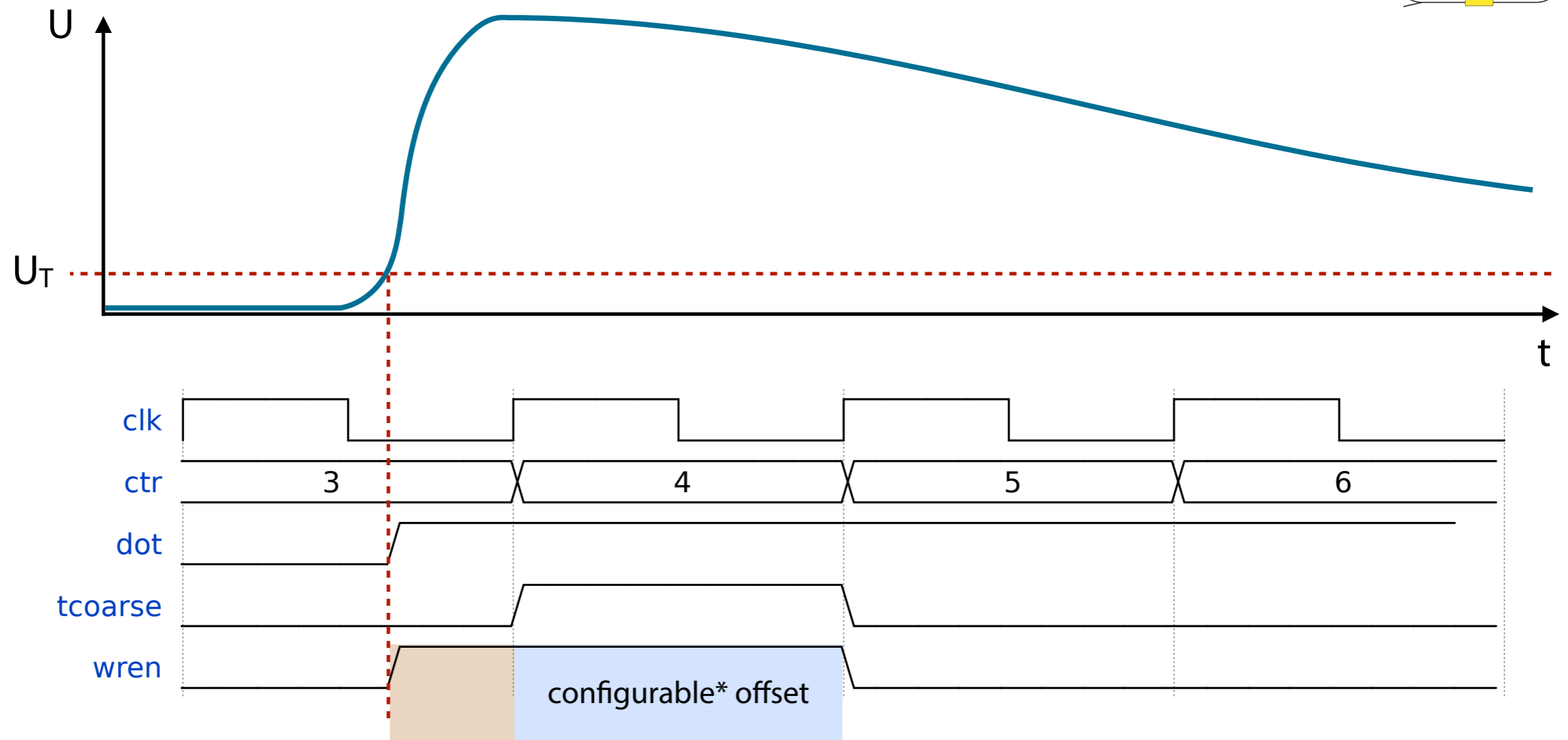


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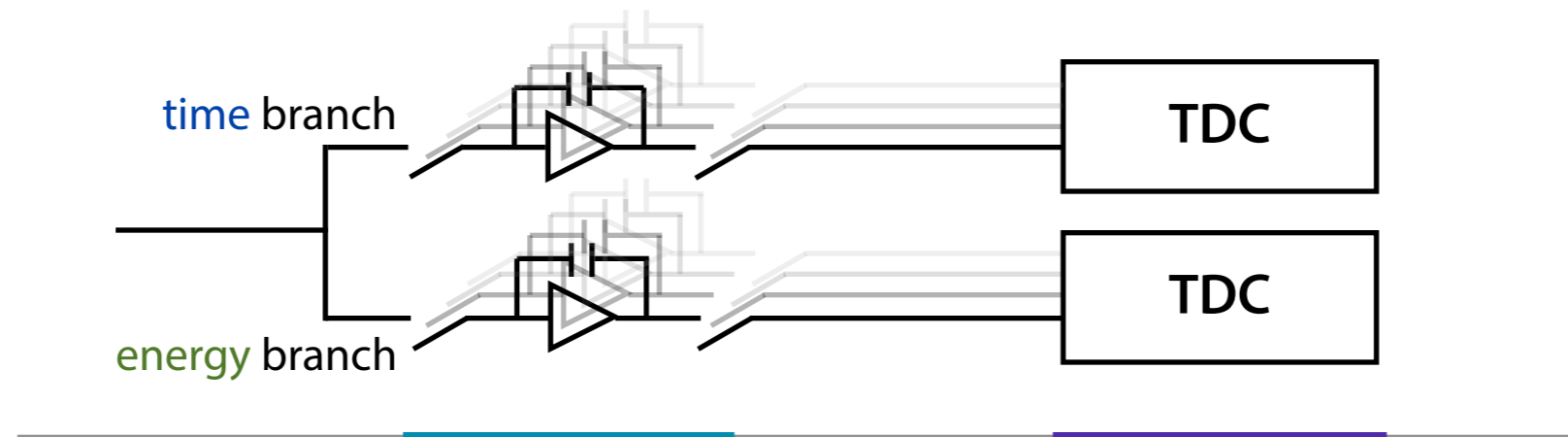
# Accurate Time Measurement



\*offset values: 0.0; 0.5; 1.0; 1.5 clock cycles

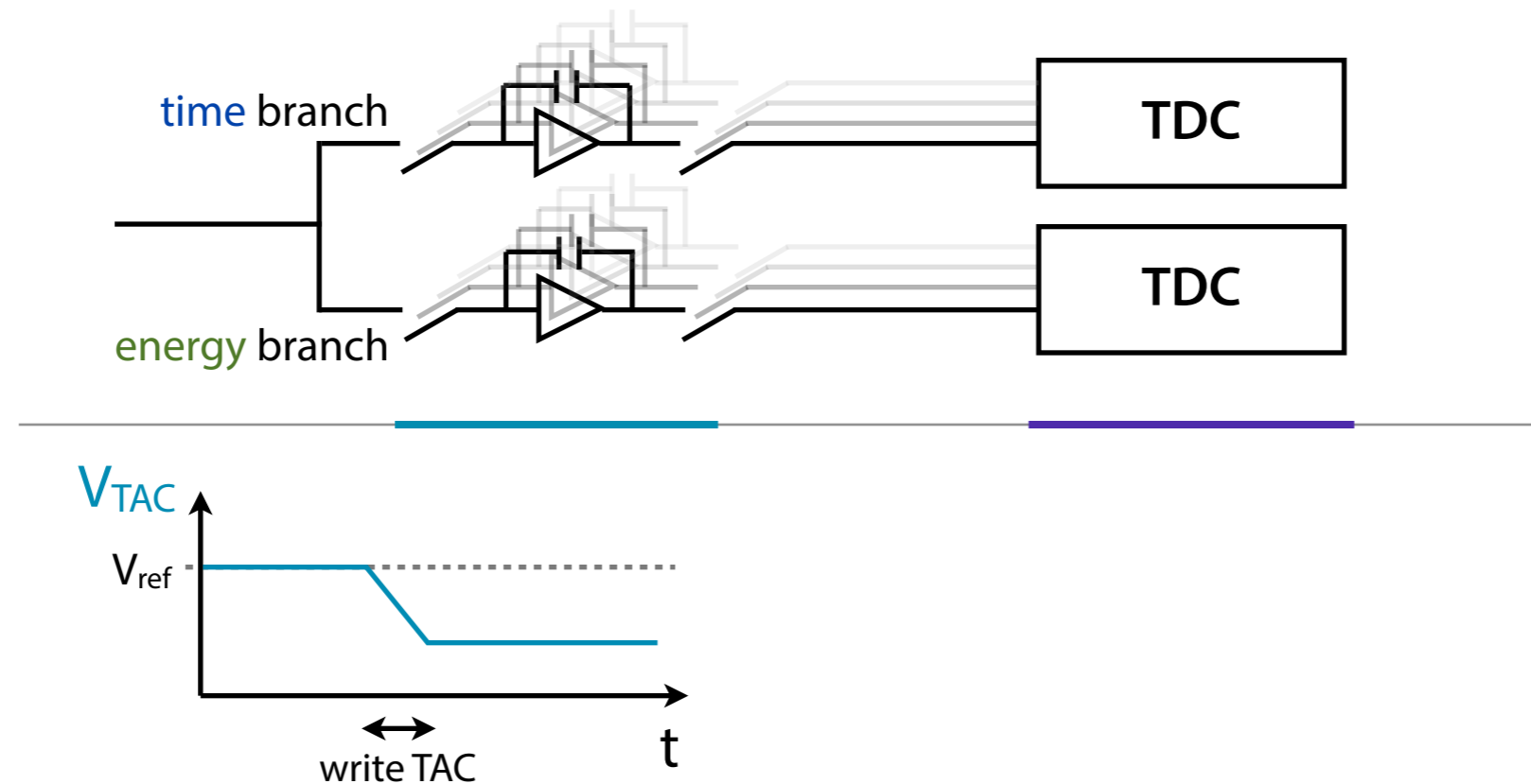


# Time-to-Digital Converter



- Two stages: **buffer** and **convert** signal

# Time-to-Digital Converter

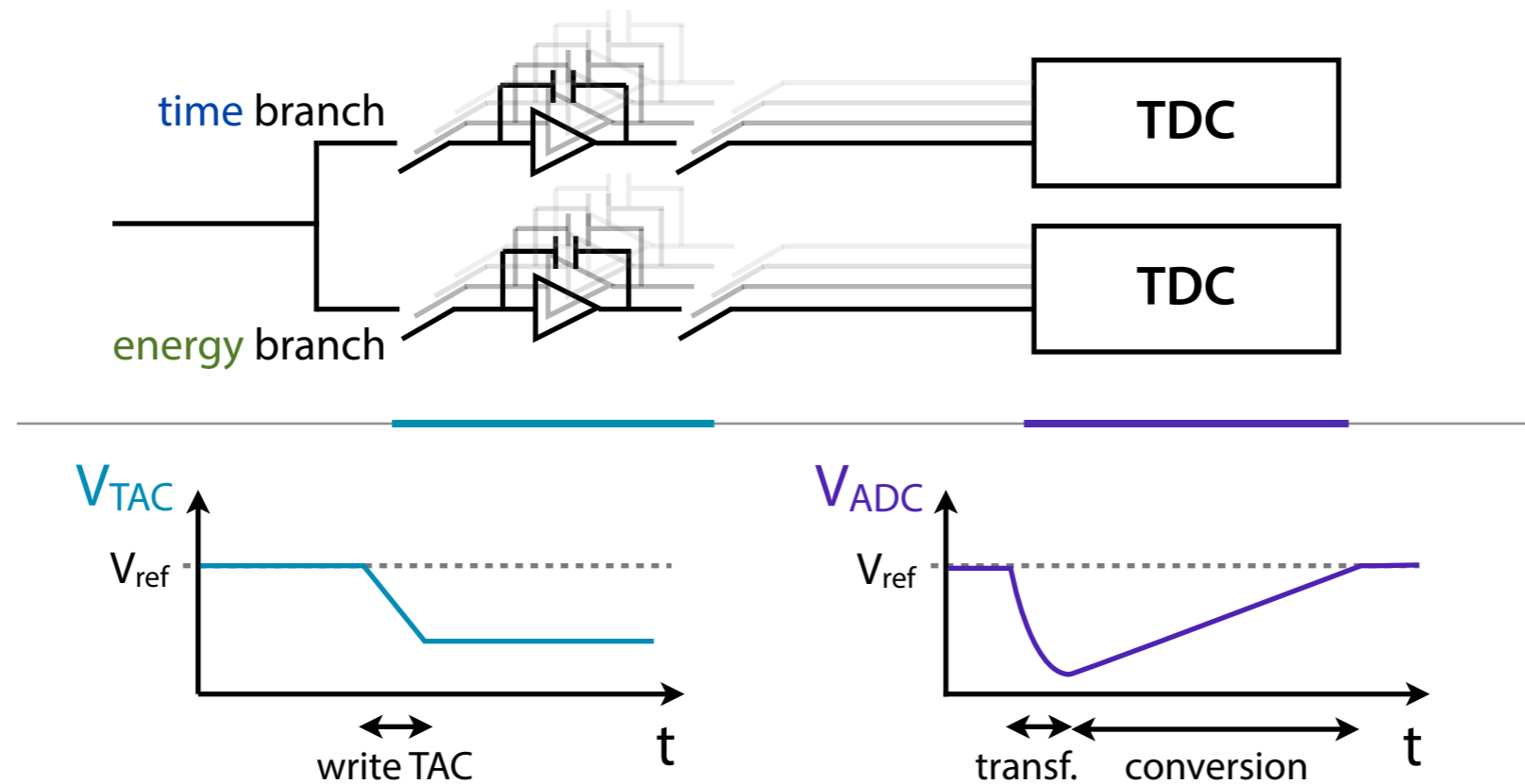


- Two stages: **buffer** and **convert** signal
  - Buffering: discharge a capacitor (**TAC**)
    - **Start**: threshold; **End**: next edge of clock\*

ADC: Analogue to Digital Converter  
TAC: Time to Analogue Converter

\*: Dynamic range 0-2.5 clock cycles

# Time-to-Digital Converter



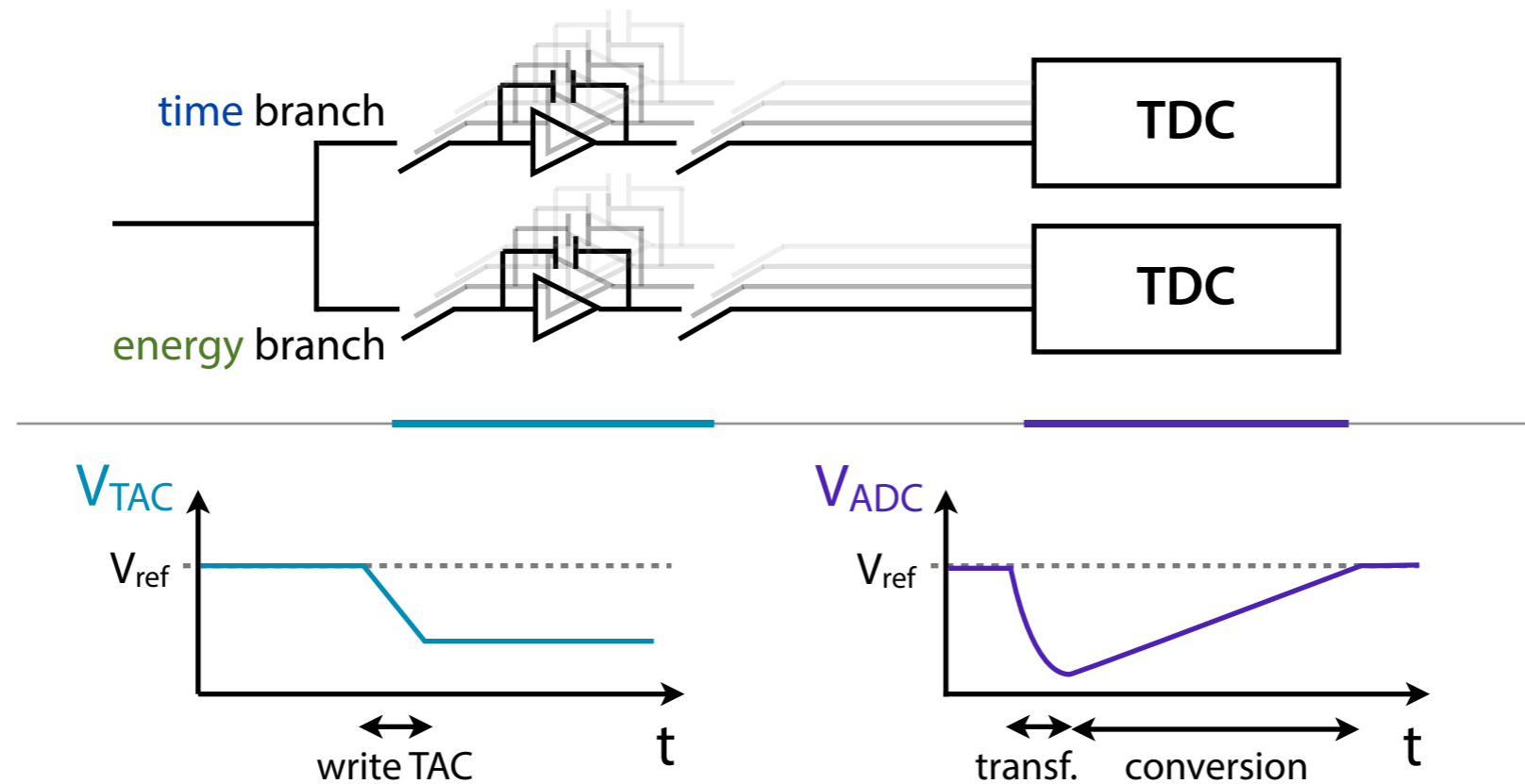
- Two stages: **buffer** and **convert** signal
  - Buffering: discharge a capacitor (**TAC**)
    - **Start**: threshold; **End**: next edge of clock\*
  - Transfer to **4x** larger **capacitor**, linearly recharge with **32x** smaller current (*Wilkinson ADC*)

ADC: Analogue to Digital Converter  
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# Time-to-Digital Converter



- Two stages: **buffer** and **convert** signal
  - Buffering: discharge a capacitor (**TAC**)
    - **Start:** threshold; **End:** next edge of clock\*
  - Transfer to **4x** larger **capacitor**, linearly recharge with **32x** smaller current (*Wilkinson ADC*)
- Increase time resolution by **128** (50 @ 160 MHz)
  - Conversion takes  $\sim 3 \mu\text{s}$   $\rightarrow$  TAC buffer **multiplicity of 4**

ADC: Analogue to Digital Converter  
TAC: Time to Analogue Converter

\*: Dynamic range 0-2.5 clock cycles

# Readout of MVD Silicon Strips

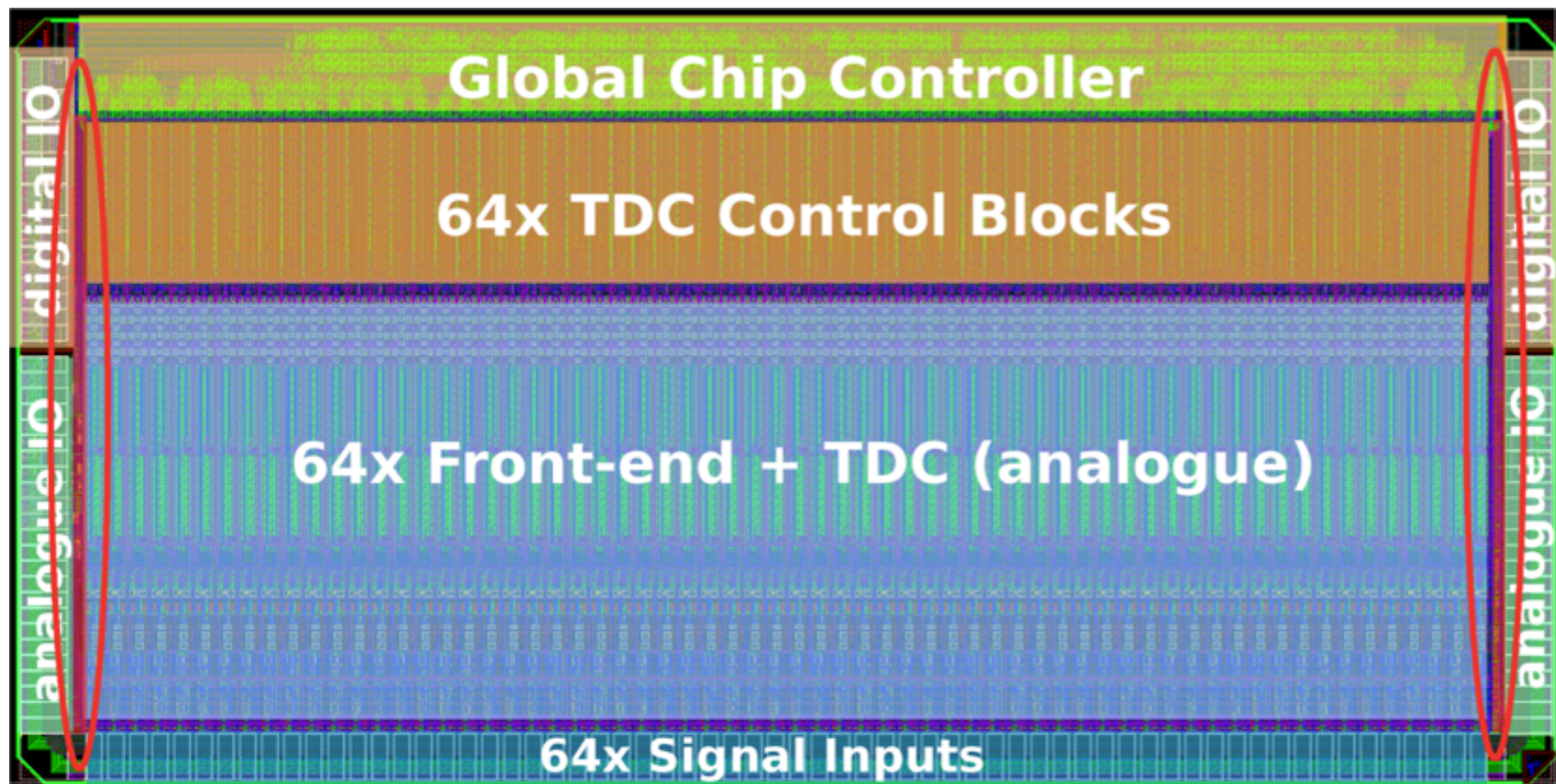
- Most parameters at least near the MVD requirements

	Area	Ch. pitch	Hit rate	Time bin.	CLK	Power
TOF-PET	7.1 x 3.5 mm <sup>2</sup>	102 μm	< 100 kHz	50 ps	80-160 MHz	7-8 mW/ch
MVD req.	4.2 x 5.0 mm <sup>2</sup>	60 μm	< 40 kHz	< 20 ns	155.56 MHz	< 4 mW/ch

- Differences to handle:
  - Signal shape / capacitance ⇒ redesign analogue part
  - Area / Channel pitch
  - Different technology
  - Radiation hardening
  - Power consumption
  - General improvements

# Floorplan of TOF-PET ASIC

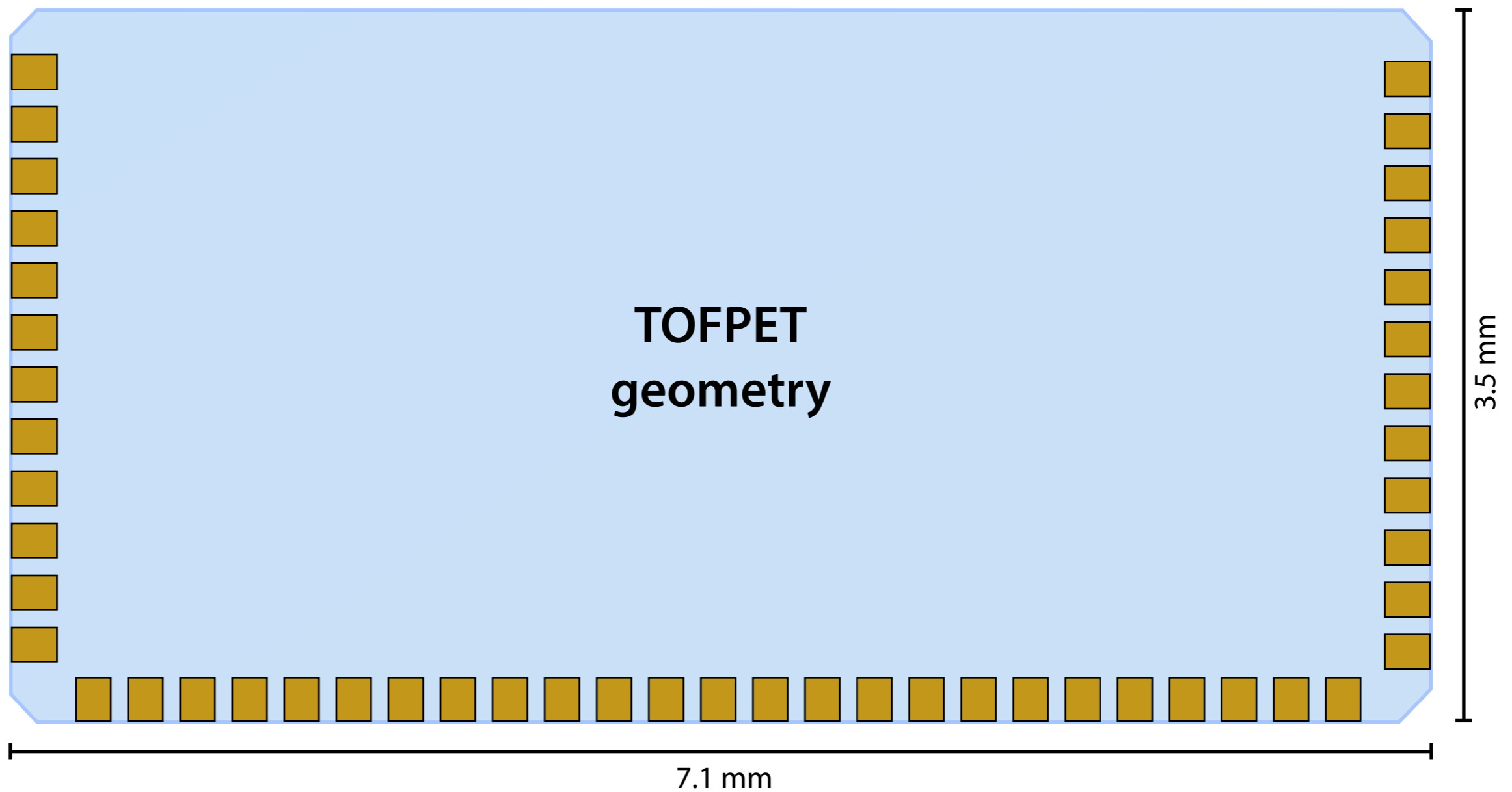
- CMOS 130 nm, 64 channels on 25 mm<sup>2</sup>
- One pad-free edge to attribute two twin chips back-to-back



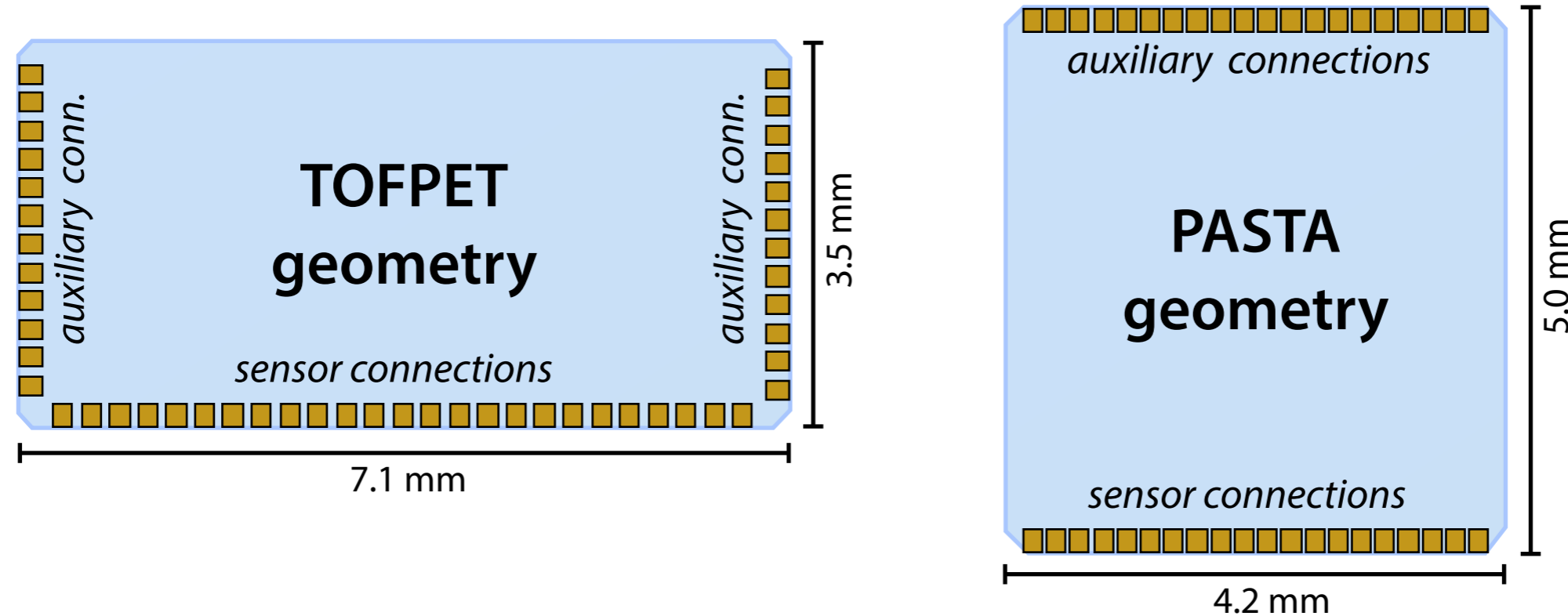
Red ellipses: bias and calibration circuitry



# Changes in Geometry for PASTA



# Changes in Geometry for PASTA



- Footprint:  $7.1 \times 3.5 \text{ mm}^2 \rightarrow 4.2 \times 5.0 \text{ mm}^2$   
( $25 \text{ mm}^2 \rightarrow 21 \text{ mm}^2$ )
- Smaller channel pitch:  $102 \mu\text{m} \rightarrow 60 \mu\text{m}$
- Position of bonding pads: front, sides  $\rightarrow$  front, back

- Switch towards area optimized technology (tecB)
  - Supports the reduction of the pitch
  - Structure size: 130  $\mu\text{m}$ , tecA → 110  $\mu\text{m}$ , tecB
  - Less development costs
    - Shared wafer instead of full engineering run
- Typical changes in digital project
  - Area occupation: ↘ 30-50 %
  - Power consumption: ↗ 10-20 %

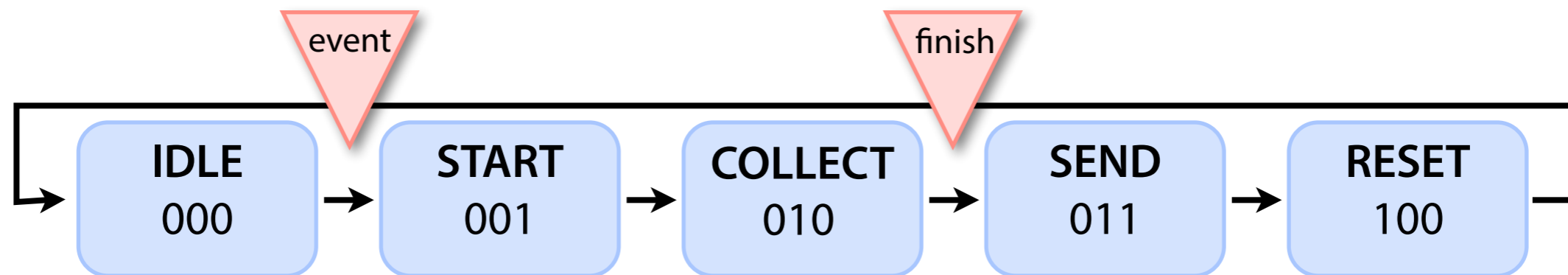


# Radiation Damage

- Charge deposition in electronics can lead to:
- **Hard errors**
  - Destruction of gates
  - Permanent damage
- **Soft errors**
  - Effects only temporary
  - Single Event Upset (SEU)
    - Change a value inside a flip flop (buffer)

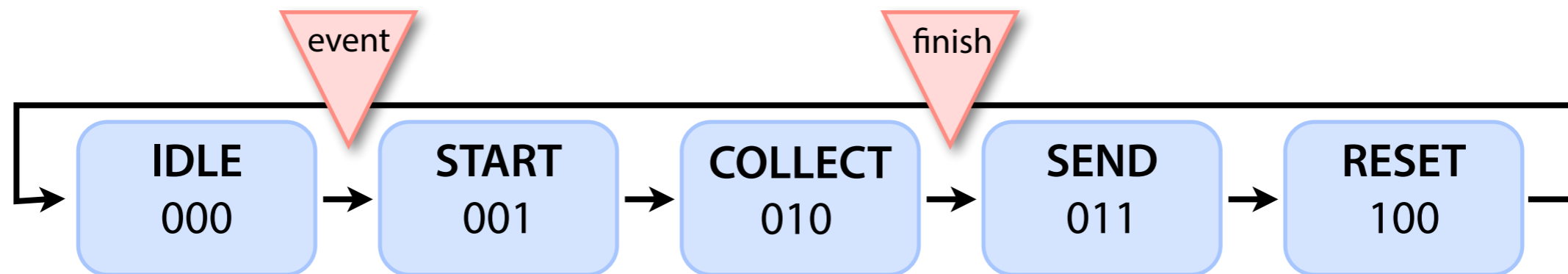
# Single Event Upset

- *Example:* a fictional readout control
- Normal operation



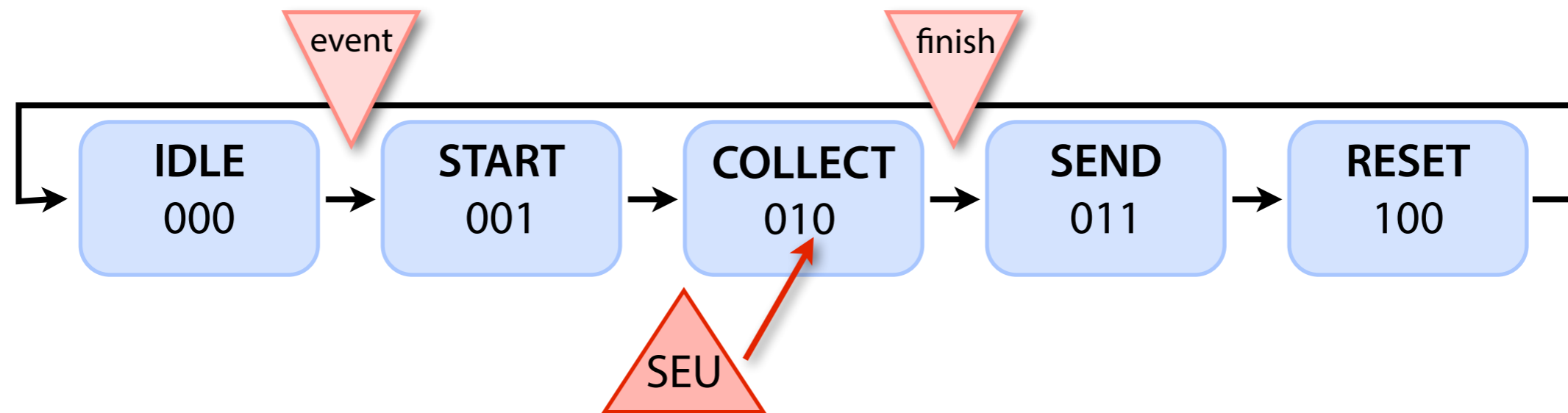
# Single Event Upset

- *Example:* a fictional readout control
- **Radiation** environment



# Single Event Upset

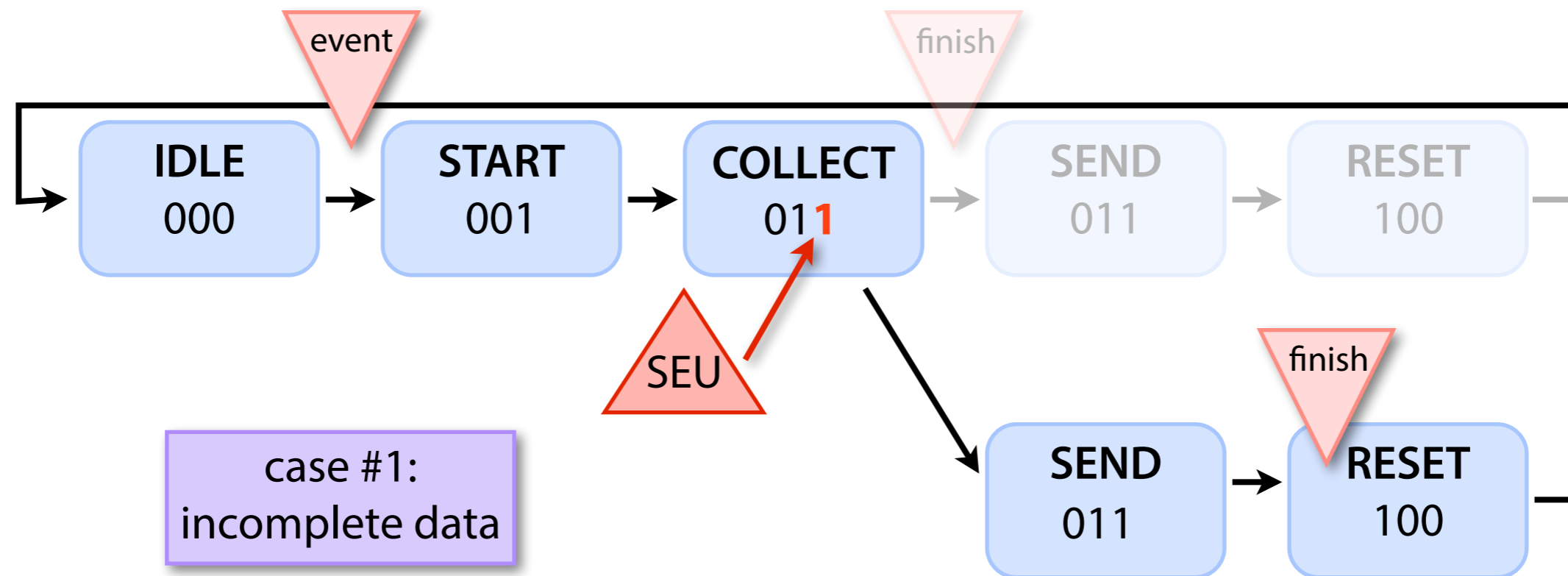
- *Example:* a fictional readout control
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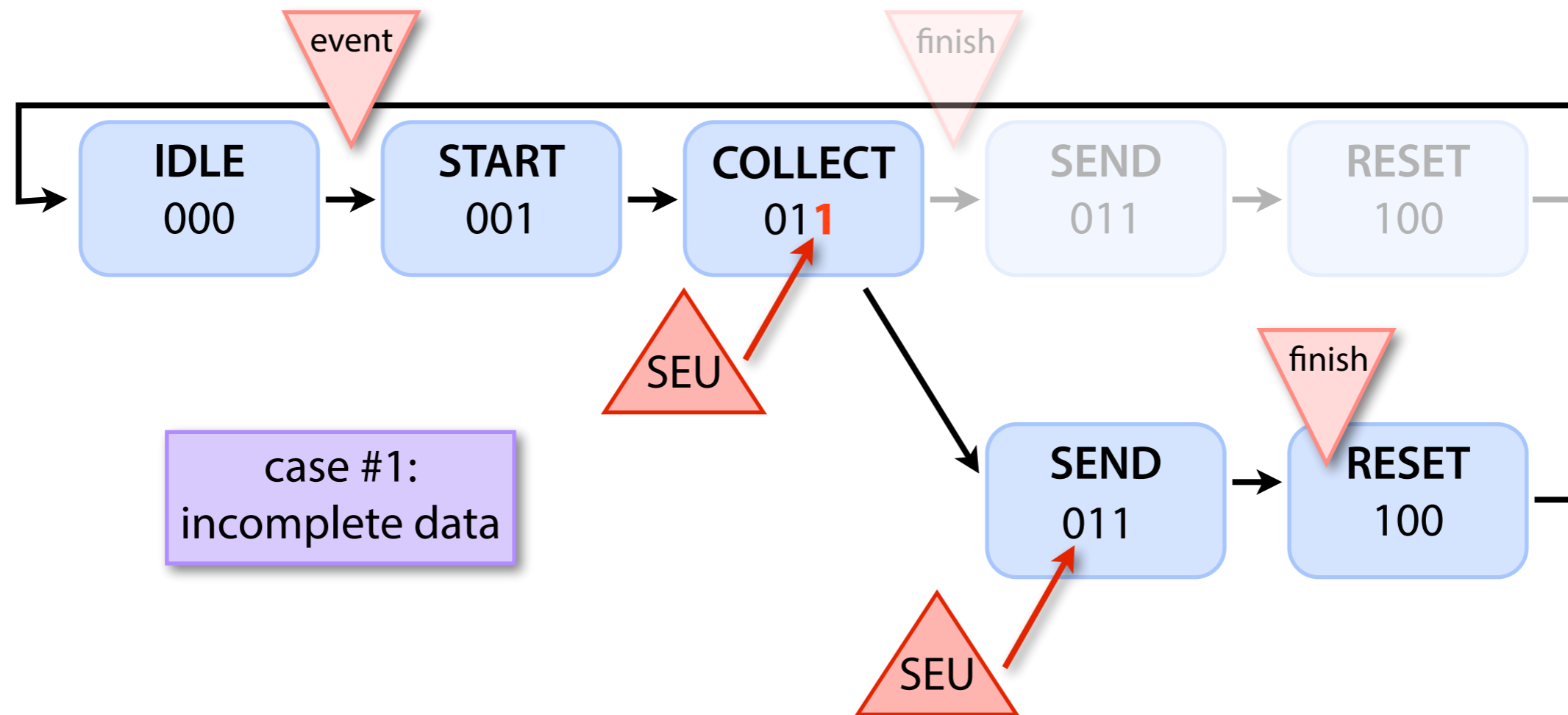
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- *Example:* a fictional readout control
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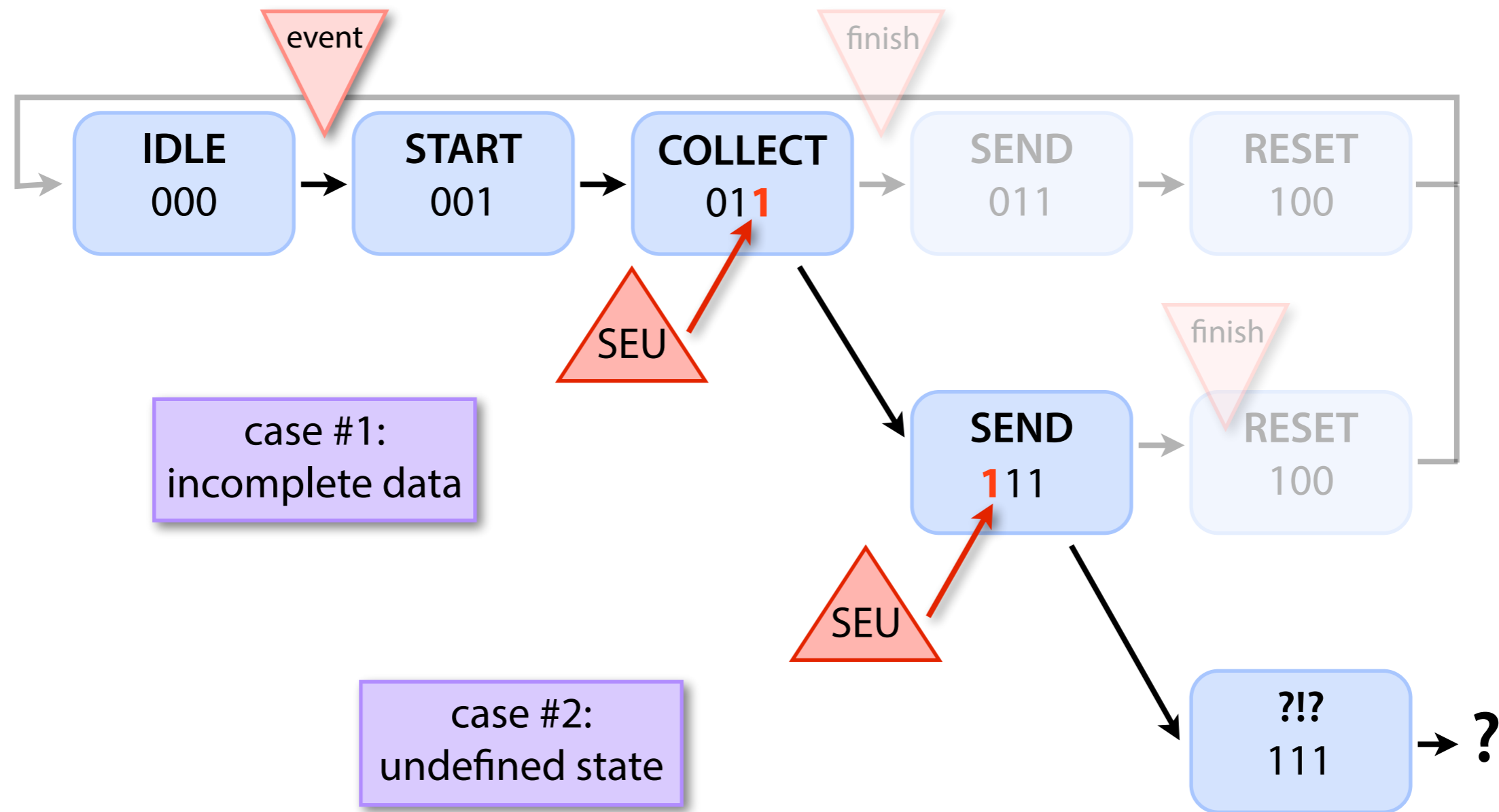
# Single Event Upset

- *Example:* a fictional readout control
- **Radiation** environment



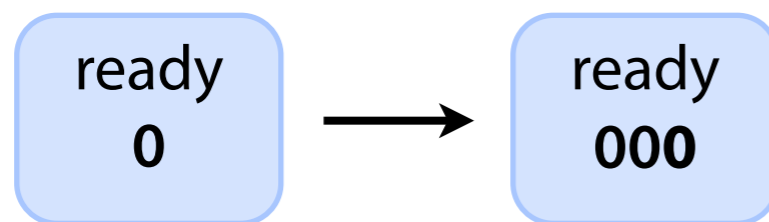
# Single Event Upset

- *Example:* a fictional readout control
- **Radiation** environment



# Prevent Logic Freeze

- Single bit:
  - Triple Mode Redundancy (TMR)

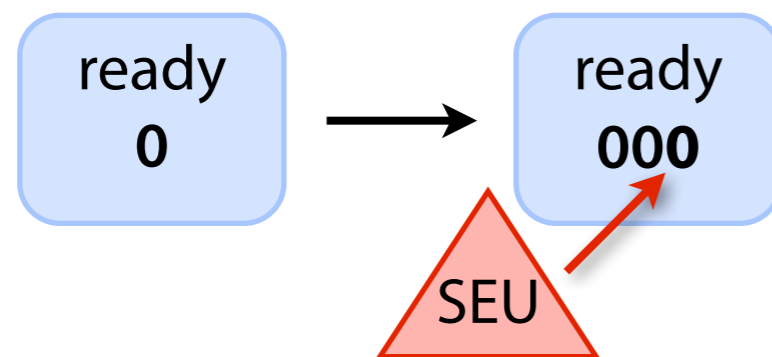


**TDC CTRL v1**  
Single bit FF: 140  
TMR protected: 30



# Prevent Logic Freeze

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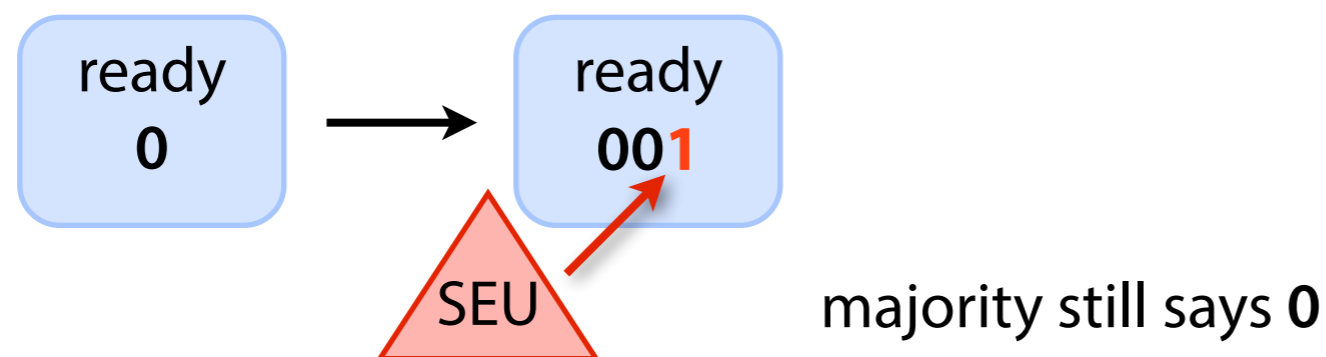
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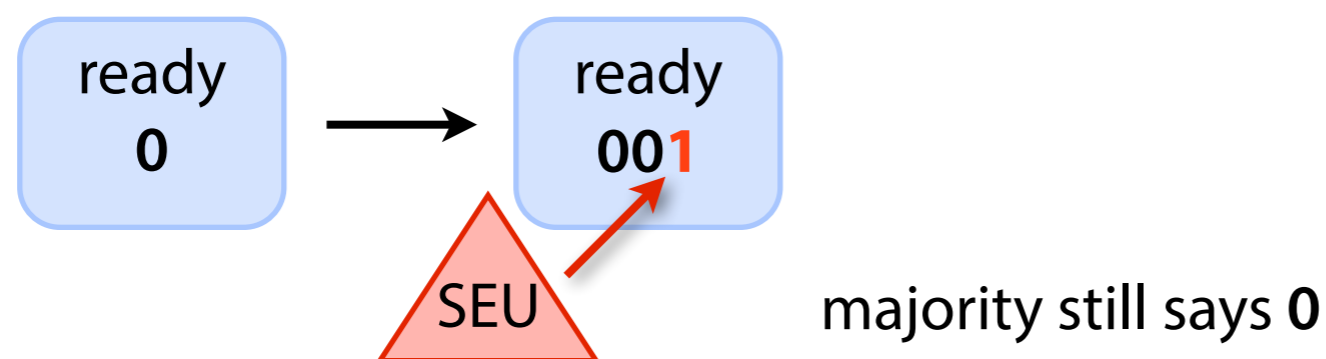
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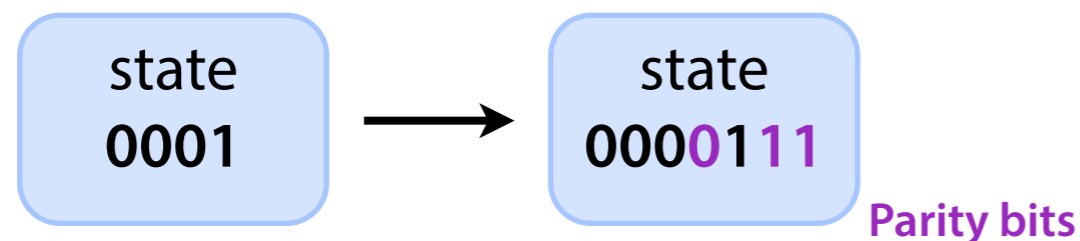
- Single bit:
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TDC CTRL v1	
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- Multiple bits (e.g. state machine):

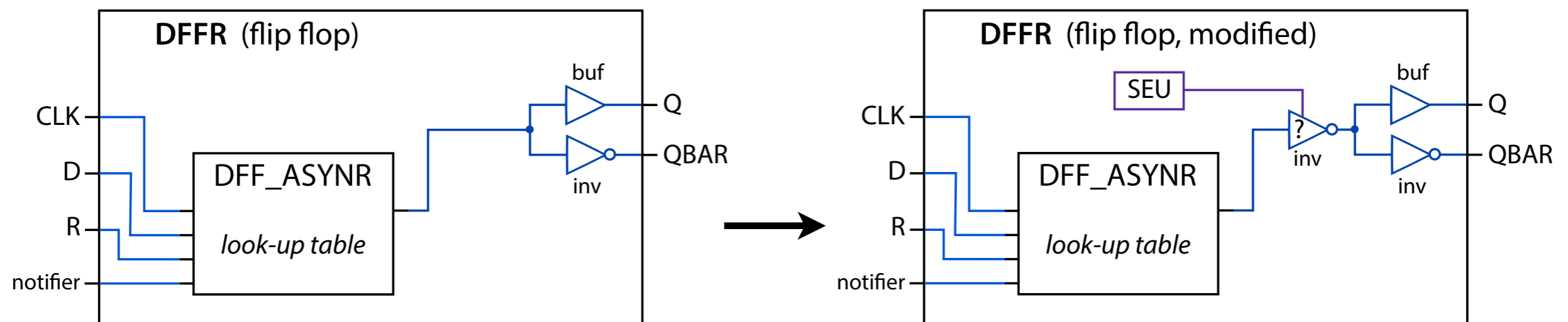
- Hamming encoded states



TDC CTRL v1	
Multiple bit FF:	320
Hamming protected:	133
(state machines:	100)

- additional parity bits to detect and correct SEU

- Step 1: Ability to simulate a SEU
  - Functions of development environment »Cadence«
    - nc\_force: forces a signal inside the logic to a given value
    - nc\_release: releases a previous force
  - Problem: flip flop in simulation without internal memory
    - Idea 1: Flipped value in input wire
    - Idea 2: Modified standard cell library





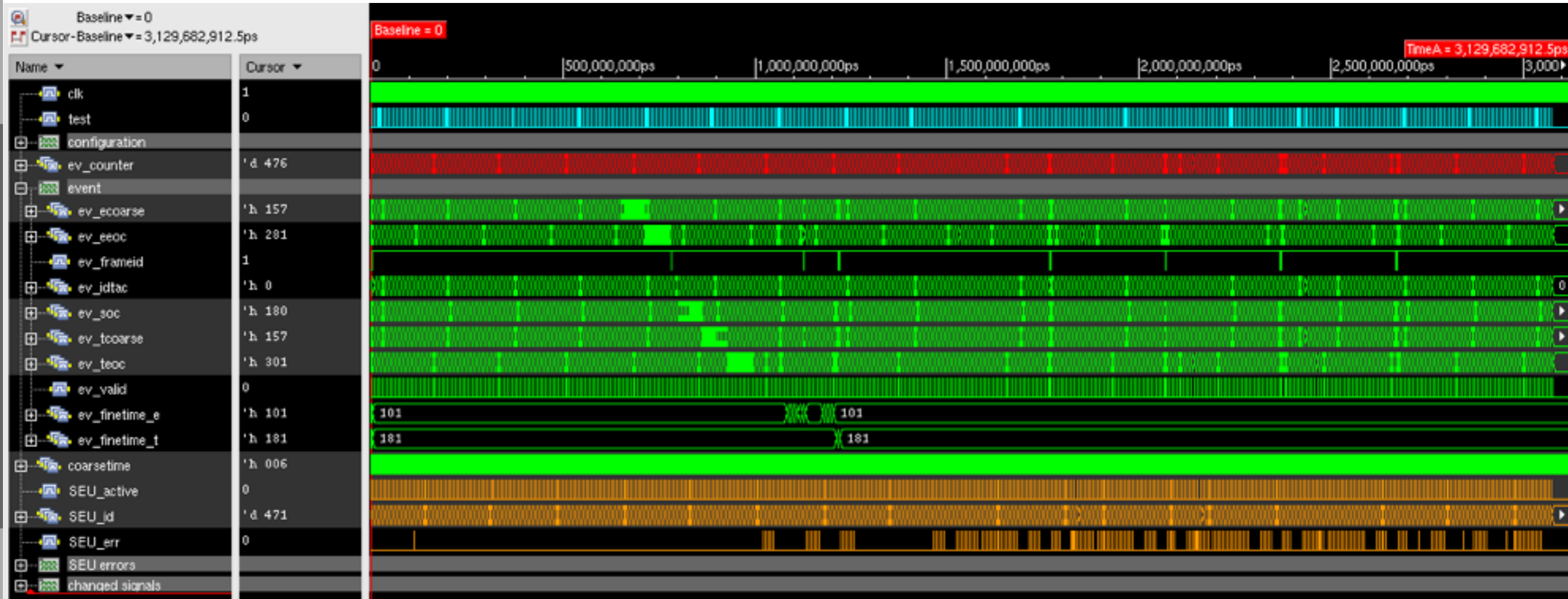
# Simulate SEU in Project

- Step 2: Check all flip flops
  - Which flip flops are critical?  
(besides state machines)
  - Tool to generate list of flip flops
    - Input: design after synthesis
    - Python parser filters input
    - Output: VHDL package
  - Test bench implementation
    - Include generated file
    - One command generates the SEU:  
`sim_SEU_FF( ID, clk, clk_period );`
  - Found 24 critical flip flops

```
118 -- get a flip flop name and path by its ID
119 function getFlipFlop( n : in integer; seuf_ff : in std_logic := '0' )
120 return string is
121 begin
122     if seuf_ff = '1' then
123         -- the variant with the modified std_cell, that has a SEU flag inside the FF
124         case n is
125             when 0 => return "ttest_TDC_CTRL_top.D001_buf1_Q_reg.18_SEU";
126             when 1 => return "ttest_TDC_CTRL_top.D001_buf1_Q_reg.18_SEU";
127             when 2 => return "ttest_TDC_CTRL_top.D001_buf2_Q_reg.18_SEU";
128             when 3 => return "ttest_TDC_CTRL_top.D001_buf3_Q_reg.18_SEU";
129             when 4 => return "ttest_TDC_CTRL_top.D001_gen_Q_reg.18_SEU";
130             when 5 => return "ttest_TDC_CTRL_top.det_async_bitvalidation.falsehit_buf1_Q_reg.18_SEU";
131             when 6 => return "ttest_TDC_CTRL_top.det_async_bitvalidation.falsehit_buf2_Q_reg.18_SEU";
132             when 7 => return "ttest_TDC_CTRL_top.det_async_bitvalidation.falsehit_buf3_Q_reg.18_SEU";
133             when 8 => return "ttest_TDC_CTRL_top.det_async_bitvalidation.falsehit_buf3_Q_reg.18_SEU";
134             when 9 => return "ttest_TDC_CTRL_top.det_async_bitvalidation.falsehit_gen_Q_reg.18_SEU";
135             when 10 => return "ttest_TDC_CTRL_top.det_async_bitvalidation.validhit_buf1_Q_reg.18_SEU";
136             when 11 => return "ttest_TDC_CTRL_top.det_async_bitvalidation.validhit_buf2_Q_reg.18_SEU";
137             when 12 => return "ttest_TDC_CTRL_top.det_async_bitvalidation.validhit_buf3_Q_reg.18_SEU";
138             when 13 => return "ttest_TDC_CTRL_top.det_async_bitvalidation.validhit_buf3_Q_reg.18_SEU";
139             when 14 => return "ttest_TDC_CTRL_top.det_async_bitvalidation.validhit_gen_Q_reg.18_SEU";
140             when 15 => return "ttest_TDC_CTRL_top.det_coarsereg.eoc_buf1_Q_reg.18_SEU";
141             when 16 => return "ttest_TDC_CTRL_top.det_coarsereg.test_buf1_Q_reg.18_SEU";
142             when 17 => return "ttest_TDC_CTRL_top.det_coarsereg.SEU_err_state_reg.18_SEU";
143             when 18 => return "ttest_TDC_CTRL_top.det_coarsereg{TAC_ID_buf1_reg{0} }_18_SEU";
144             when 19 => return "ttest_TDC_CTRL_top.det_coarsereg{TAC_ID_buf1_reg{1} }_18_SEU";
145             when 20 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{0} }_18_SEU";
146             when 21 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{1} }_18_SEU";
147             when 22 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{2} }_18_SEU";
148             when 23 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{3} }_18_SEU";
149             when 24 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{4} }_18_SEU";
150             when 25 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{5} }_18_SEU";
151             when 26 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{6} }_18_SEU";
152             when 27 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{7} }_18_SEU";
153             when 28 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{8} }_18_SEU";
154             when 29 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{9} }_18_SEU";
155             when 30 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{10} }_18_SEU";
156             when 31 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{11} }_18_SEU";
157             when 32 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{12} }_18_SEU";
158             when 33 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{13} }_18_SEU";
159             when 34 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{14} }_18_SEU";
160             when 35 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{15} }_18_SEU";
161             when 36 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{16} }_18_SEU";
162             when 37 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{17} }_18_SEU";
163             when 38 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{18} }_18_SEU";
164             when 39 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{19} }_18_SEU";
165             when 40 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{20} }_18_SEU";
166             when 41 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{21} }_18_SEU";
167             when 42 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{22} }_18_SEU";
168             when 43 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{23} }_18_SEU";
169             when 44 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{24} }_18_SEU";
170             when 45 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{25} }_18_SEU";
171             when 46 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{26} }_18_SEU";
172             when 47 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{27} }_18_SEU";
173             when 48 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{28} }_18_SEU";
174             when 49 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{29} }_18_SEU";
175             when 50 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{30} }_18_SEU";
176             when 51 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{31} }_18_SEU";
177             when 52 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{32} }_18_SEU";
178             when 53 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{33} }_18_SEU";
179             when 54 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{34} }_18_SEU";
180             when 55 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{35} }_18_SEU";
181             when 56 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{36} }_18_SEU";
182             when 57 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{37} }_18_SEU";
183             when 58 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{38} }_18_SEU";
184             when 59 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{39} }_18_SEU";
185             when 60 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{40} }_18_SEU";
186             when 61 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{41} }_18_SEU";
187             when 62 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{42} }_18_SEU";
188             when 63 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{43} }_18_SEU";
189             when 64 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{44} }_18_SEU";
190             when 65 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{45} }_18_SEU";
191             when 66 => return "ttest_TDC_CTRL_top.det_coarsereg{coarse_buf1_08_reg{46} }_18_SEU";
```

# Result of SEU Tests

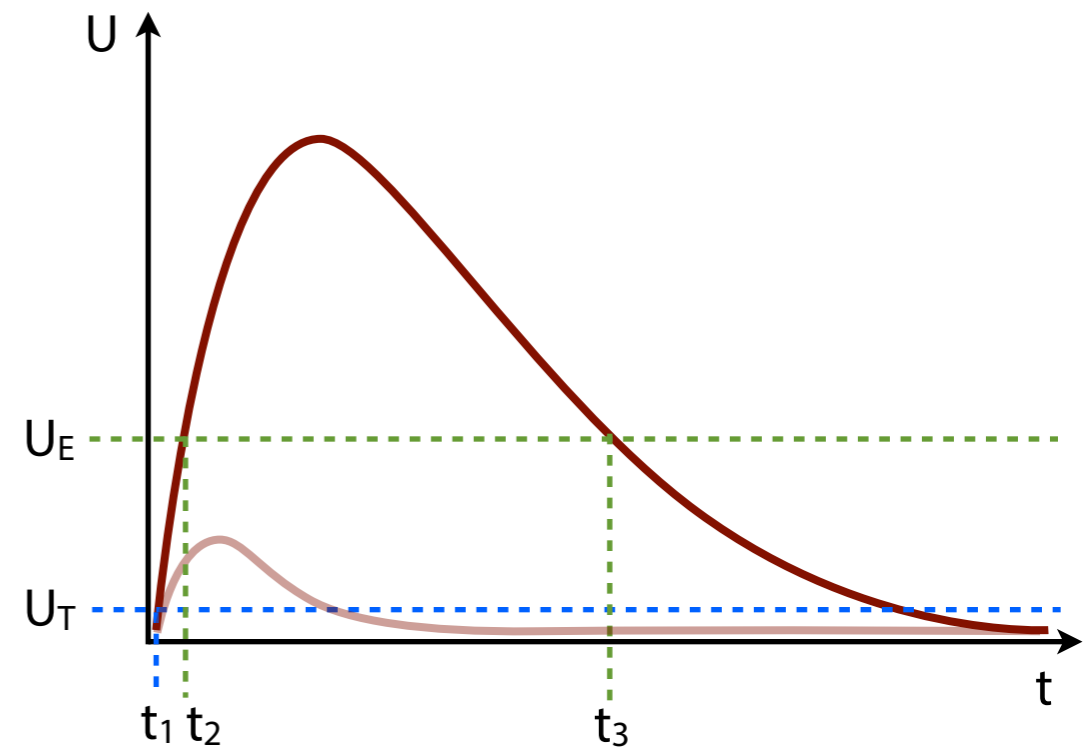
- Test of all 460 flip flops: (TDC CTRL v1)



- No logic freeze
- Only corrupted data (→ parity bit)

# Some Conceptual Differences

- **New TDC control** (clearer & simpler structure)
- **Time buffers** move to global controller
  - Saves connections, speed up simulations
- **Hit validation** in two ways (delayed & synchronous)
- More **flexibility** what to store ( $t_1-t_3$ ,  $t_1-t_2$ , test pulse)
- Optimization in **charging** time
  - Smaller offset in TAC charging
  - Conversion end on falling edge
- **TAC refresh** local instead global (Capacitors back to reference level after inactivity)



# Current Status of TDC Control

- Basic concept is implemented
  - Trigger, TAC selector, charge transfer and measurement, ...
- Left to do:
  - Solve inefficiency for events close to clock
  - SEU protection (*TDC CTRL v1* has it, *v2* not yet)

	TDC_CTRL v1 (incl. SEU, tecA)	TDC_CTRL v1 (incl. SEU, tecB)	TDC_CTRL v2 (current status, tecB)
Occupancy (1.1 x 0.1 mm <sup>2</sup> )	84.8 %	37.0 %	5.6 %
Cells	3155	2850	261
Power (@ 160 MHz)	1.57 mW/ch	1.78 mW/ch	0.05 mW/ch

Estimate for final TDC Control:

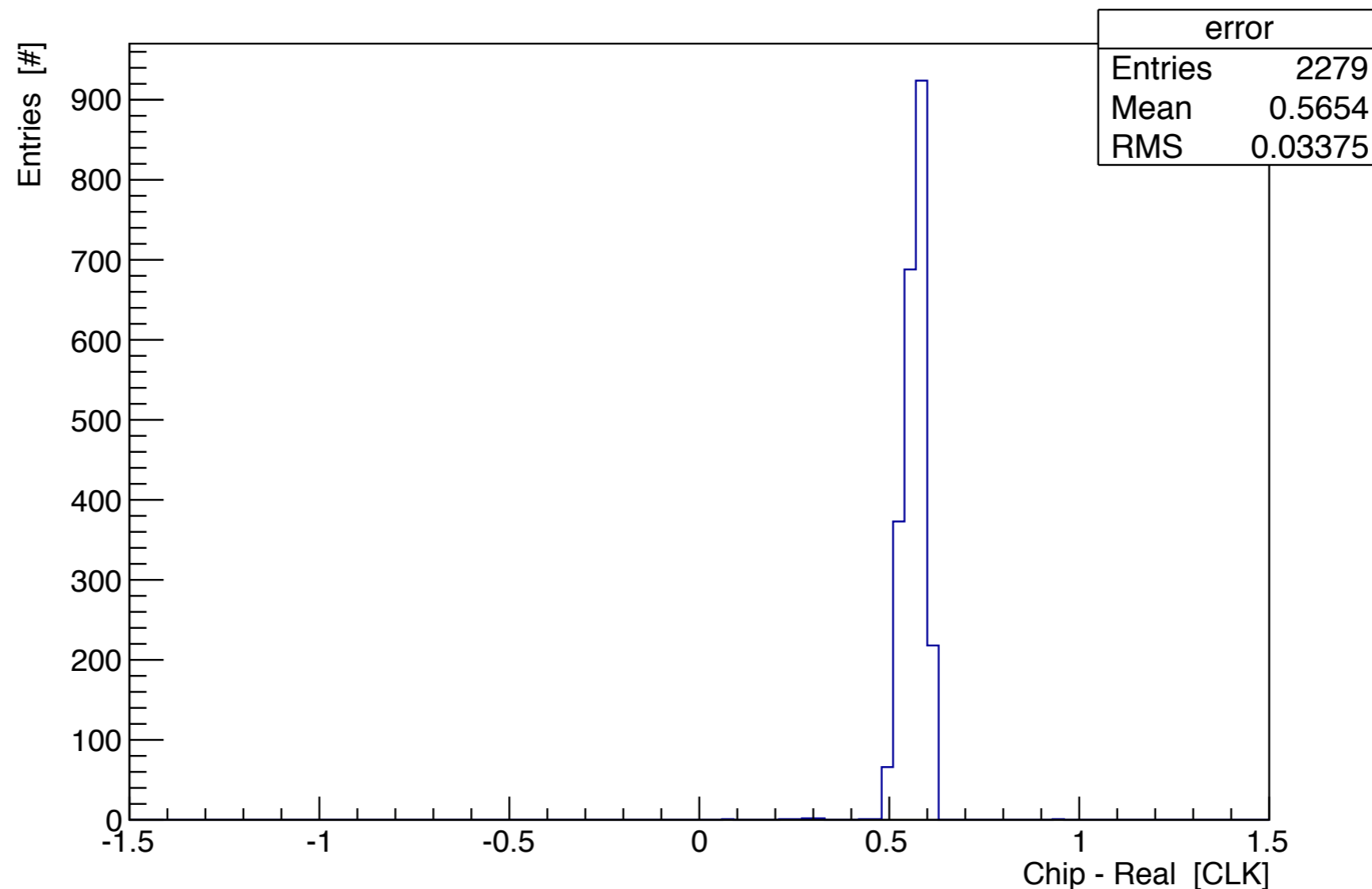
Save up to **80-90%** in terms of **power/occupancy**



# Current Status of GCTRL

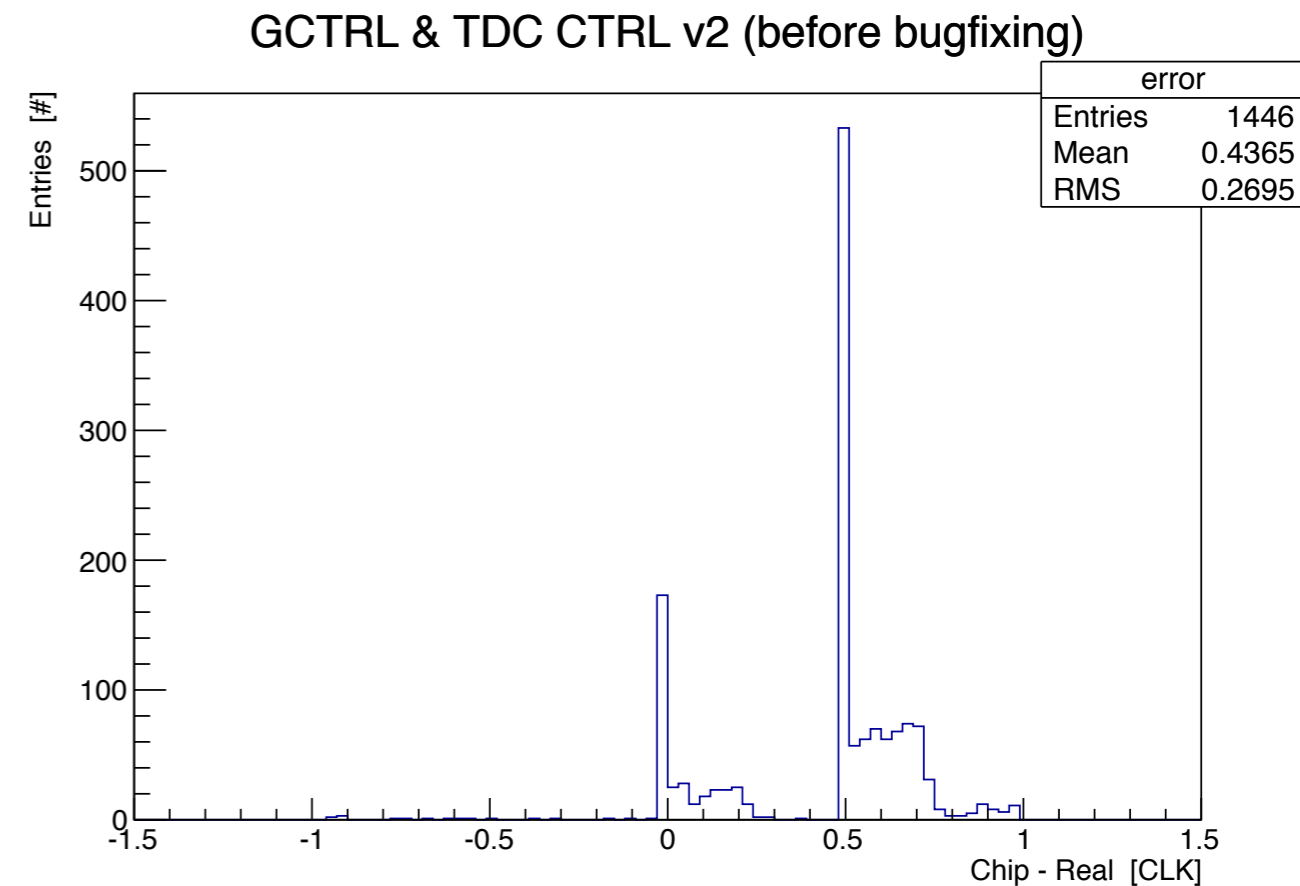
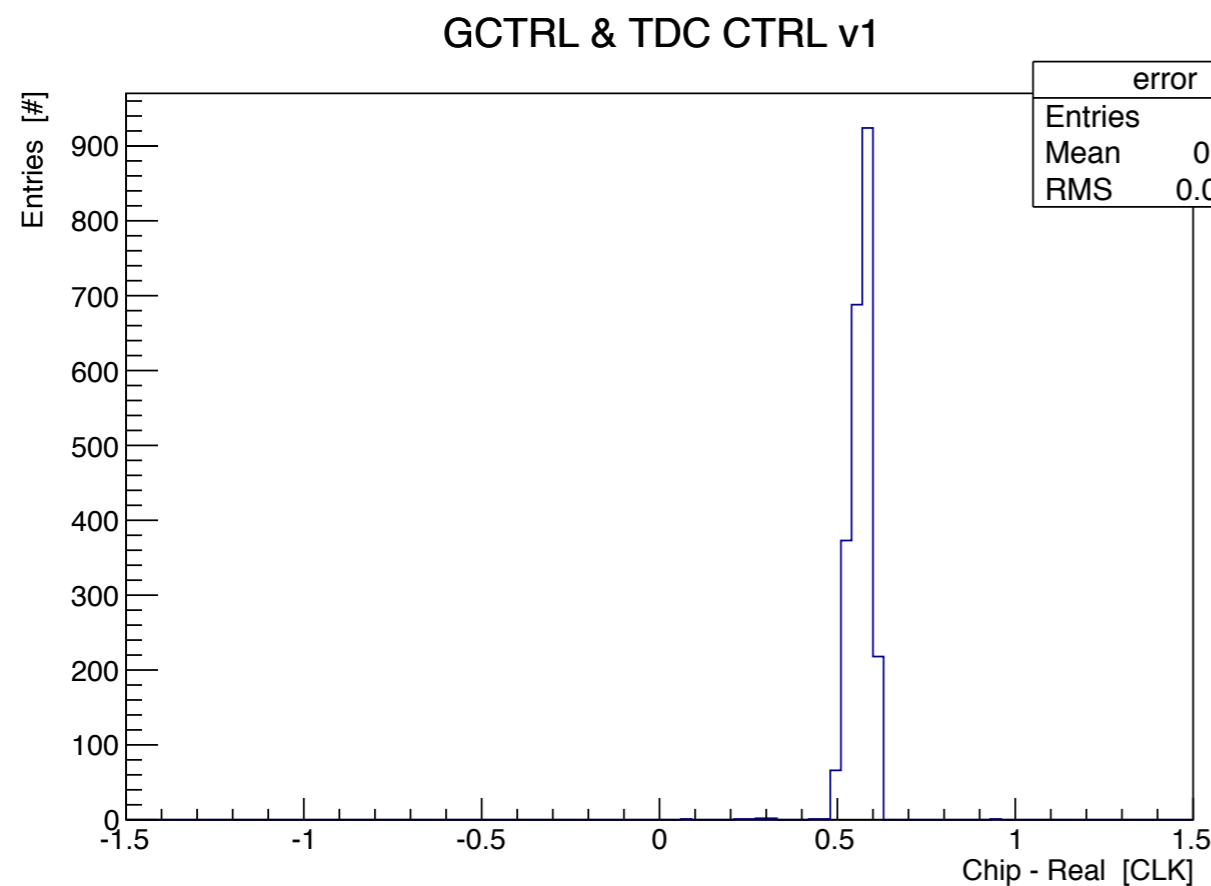
- Global controller merged to TDC\_CTRL v2
  - Time stamps moved, different connections, small adaptations
  - Test bench for digital part ...

GCTRL & TDC CTRL v1



# Current Status of GCTRL

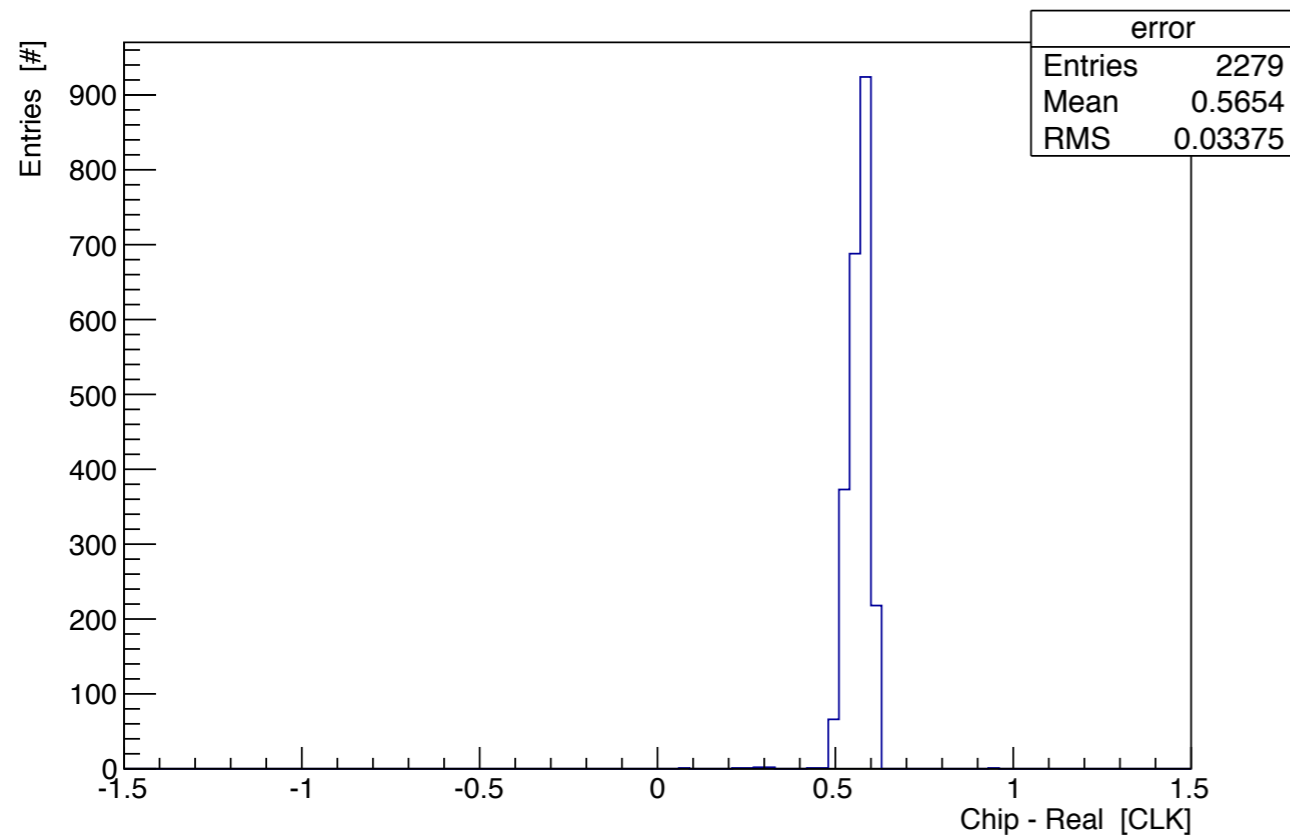
- Global controller merged to TDC\_CTRL v2
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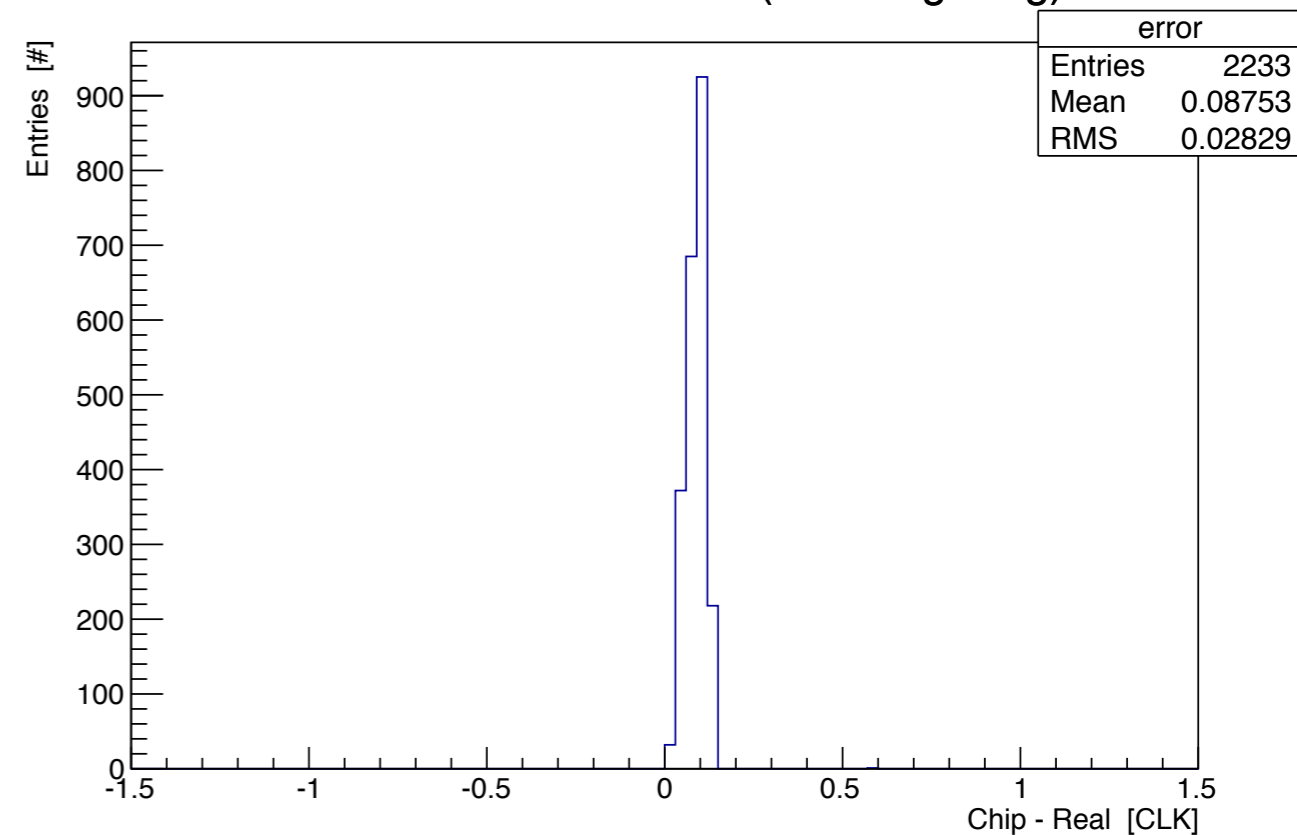
# Current Status of GCTRL

- Global controller merged to TDC\_CTRL v2
  - Time stamps moved, different connections, small adaptations
  - Test bench for digital part ...

GCTRL & TDC CTRL v1



GCTRL & TDC CTRL v2 (after bugfixing)



# Current Status of GCTRL

- Global controller merged to TDC\_CTRL v2
  - Time stamps moved, different connections, small adaptations
  - Test bench for digital part ✓
- Left to do:
  - TAC refresh
  - SEU protection

	GCTRL v1 (tecA)	GCTRL v1 (tecB)	GCTRL v2 (current status, tecB)
Occupancy (0.35 x 6.6 mm <sup>2</sup> )	70.5 %	38.1 %	34.5 %
Cells	44,949	45,695	57,703
Power (@ 160 MHz)	52.2 mW	61.3 mW	65.4 mW

- Time-based MVD strip sensor readout
  - High time precision (50 ps)
  - Charge by ToT
  - Two thresholds
- First PASTA version in development
  - Based on experience from TOF-PET
  - Enhancements towards strip readout (Diff. preamplifier, changed geom.)
- Future:
  - Include SEU protection
  - Production in course of 2014

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# Thank you!

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- [ 2, PANDA detector] PANDA Collaboration (2013)
- [ 3, map showing GSI] Screenshot Google Maps (2013) [[→ direct link](#)]
- [ 3, FAIR construction] Jan Schäfer; FAIR homepage (2013) [[→ direct link](#)]
- [ 4, FAIR] GSI Helmholtzzentrum für Schwerionenforschung (2013)
- [ 7, PANDA & MVD] PANDA Collaboration (2013)
- [11, MVD requirements] PANDA Collaboration; *PANDA Technical Design Report for the Micro Vertex Detector* (2013) [[→ direct link](#)]
- [12, floorplan] Manuel D. Rolo, LIP Lisboa / INFN Torino (2013)