JÜLICH
FORSCHUNGSZENTRUM

panda

Time-based readout of silicon strip sensors

*Concept and status of the **PA**NDA **St**rip **A**SIC*

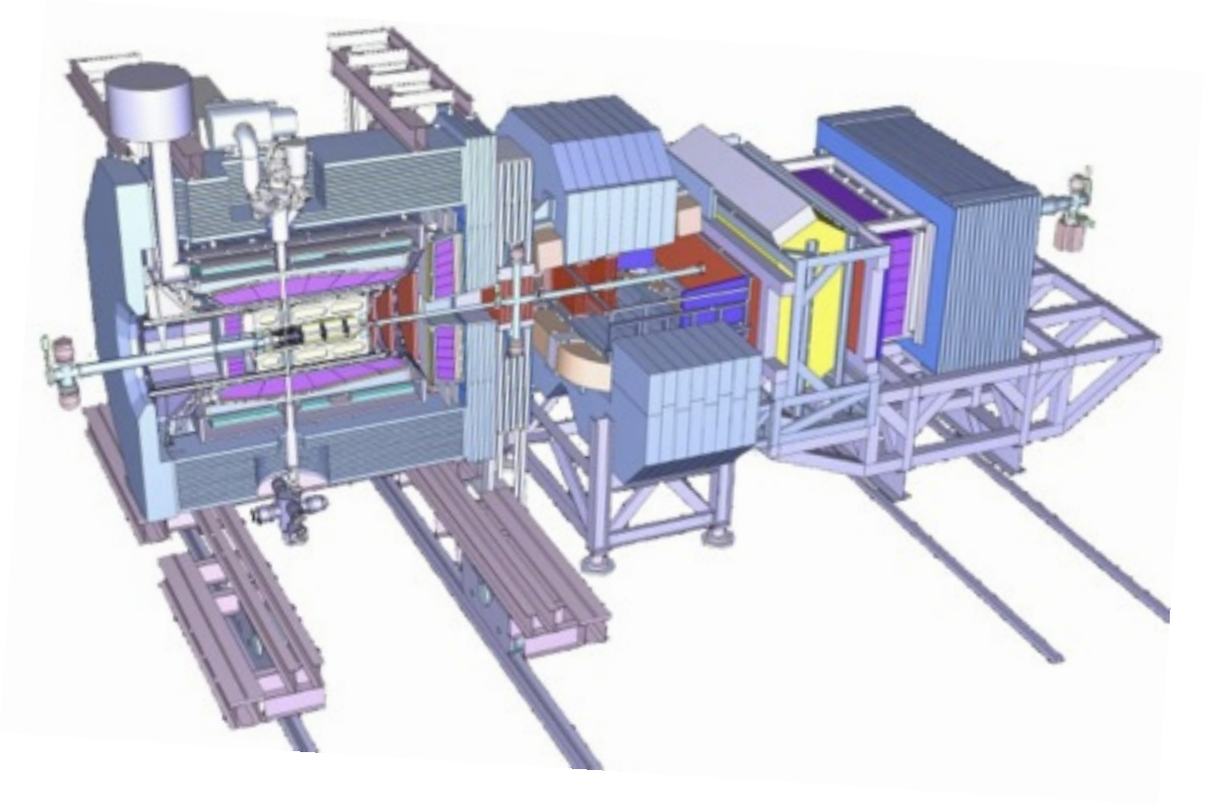
André Goerres

28 November 2013

Workshop on front end electronics, INFN Torino

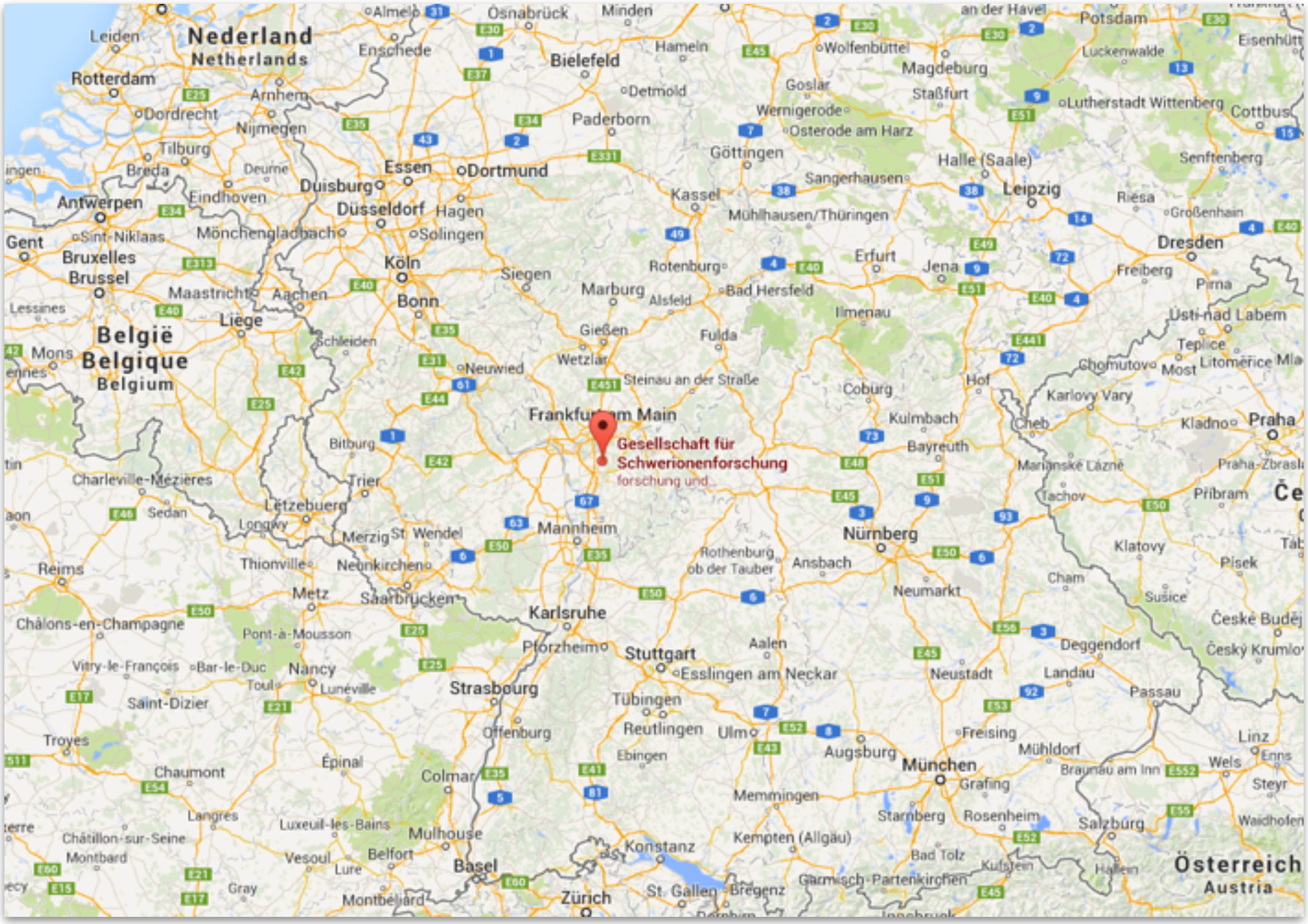
Content

- Introduction
  - GSI, FAIR, **PANDA**, MVD
- **PA**NDA **St**rip **A**SIC (PASTA)
  - Concept of the ASIC
  - Changes to TOF-PET ASIC
  - Current Status of Development
- Conclusion & Outlook



FAIR @ GSI

- Facility for Antiproton and Ion Research
  - Accelerator complex next to GSI



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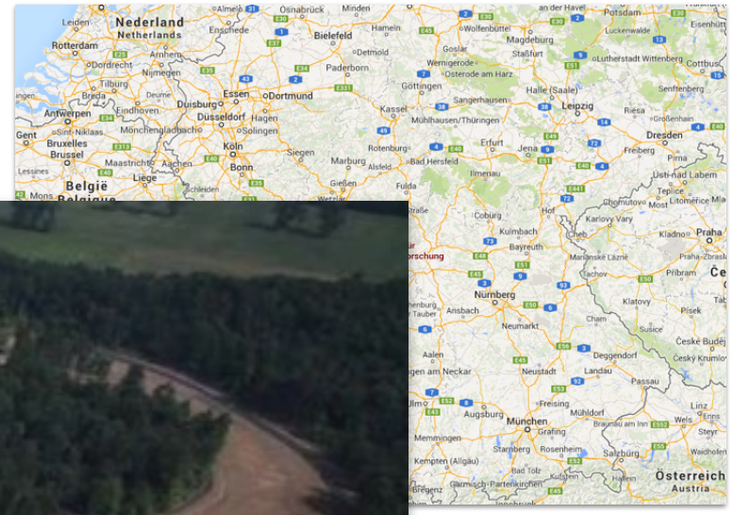
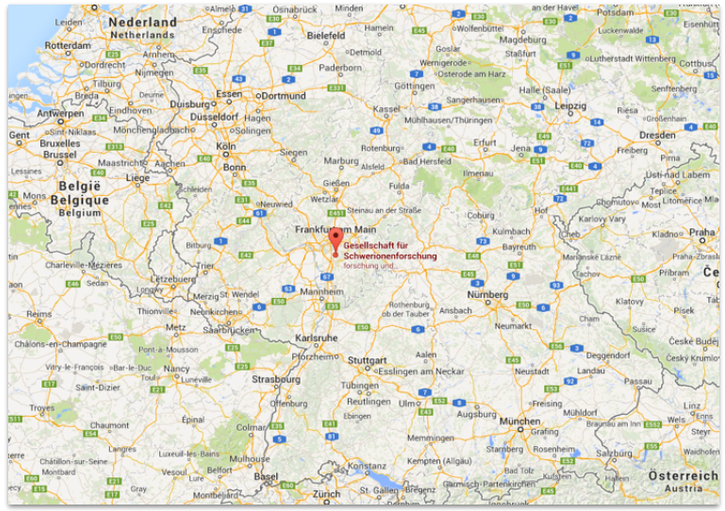


FAIR @ GSI

- Facility for Antiproton and Ion Research
  - Accelerator complex next to GSI
  - Construction in progress, finish planned for 2018
  - Four pillars of research:

ABBA	CBM	NUSTAR	PANDA
Atom & plasma physics	Hadron physics	Nuclear structure, astro physics	Hadron physics



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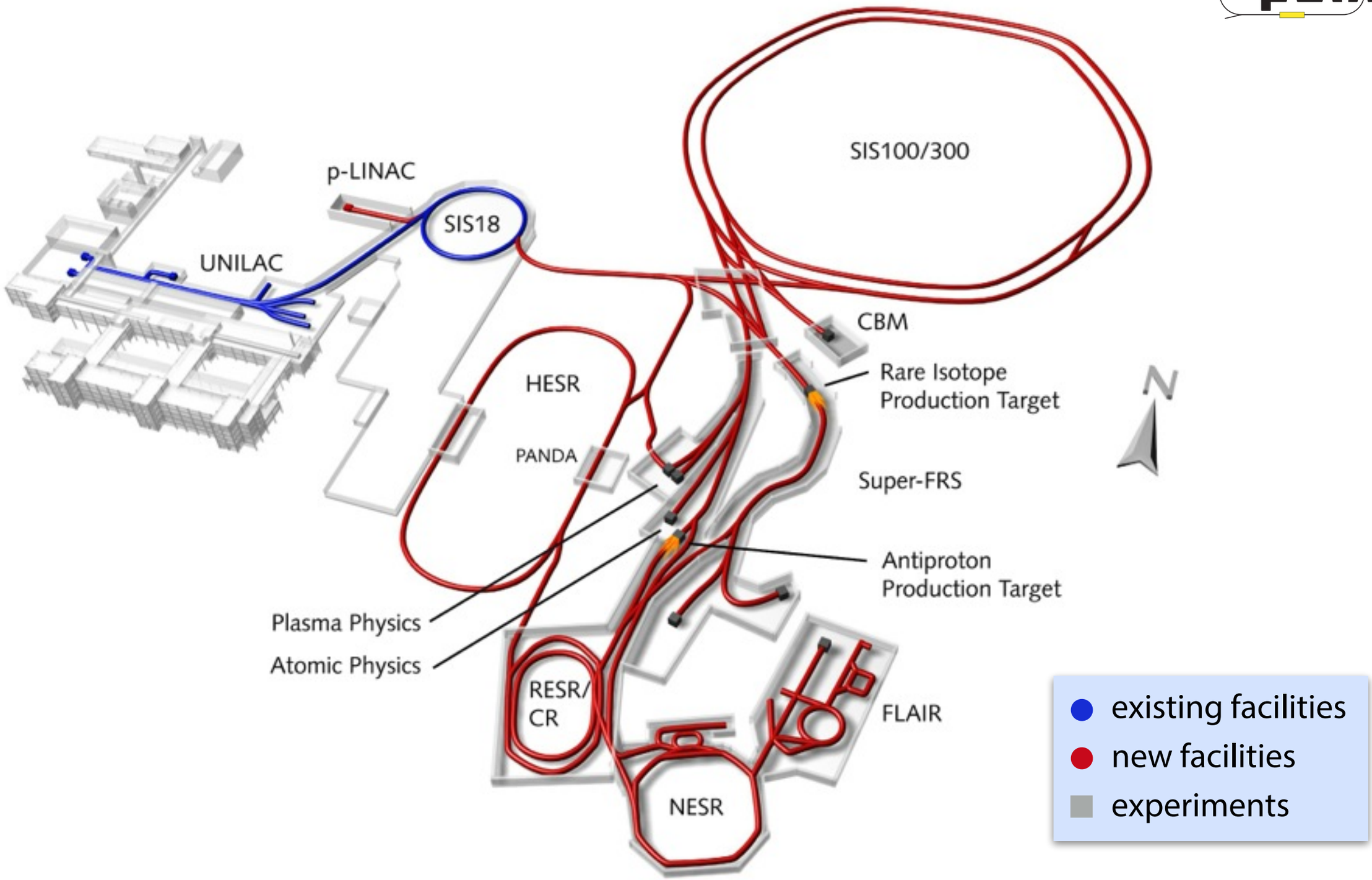

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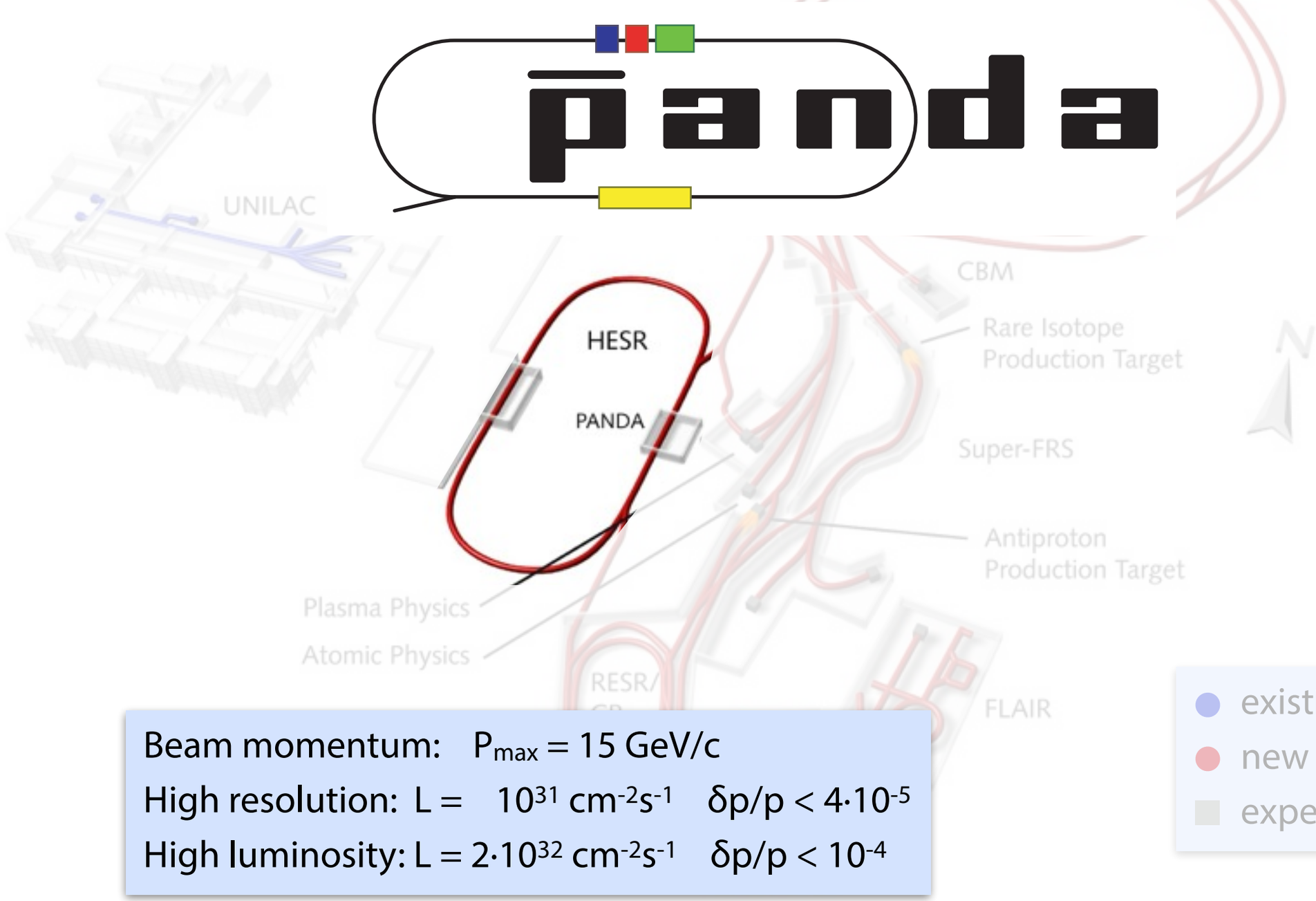


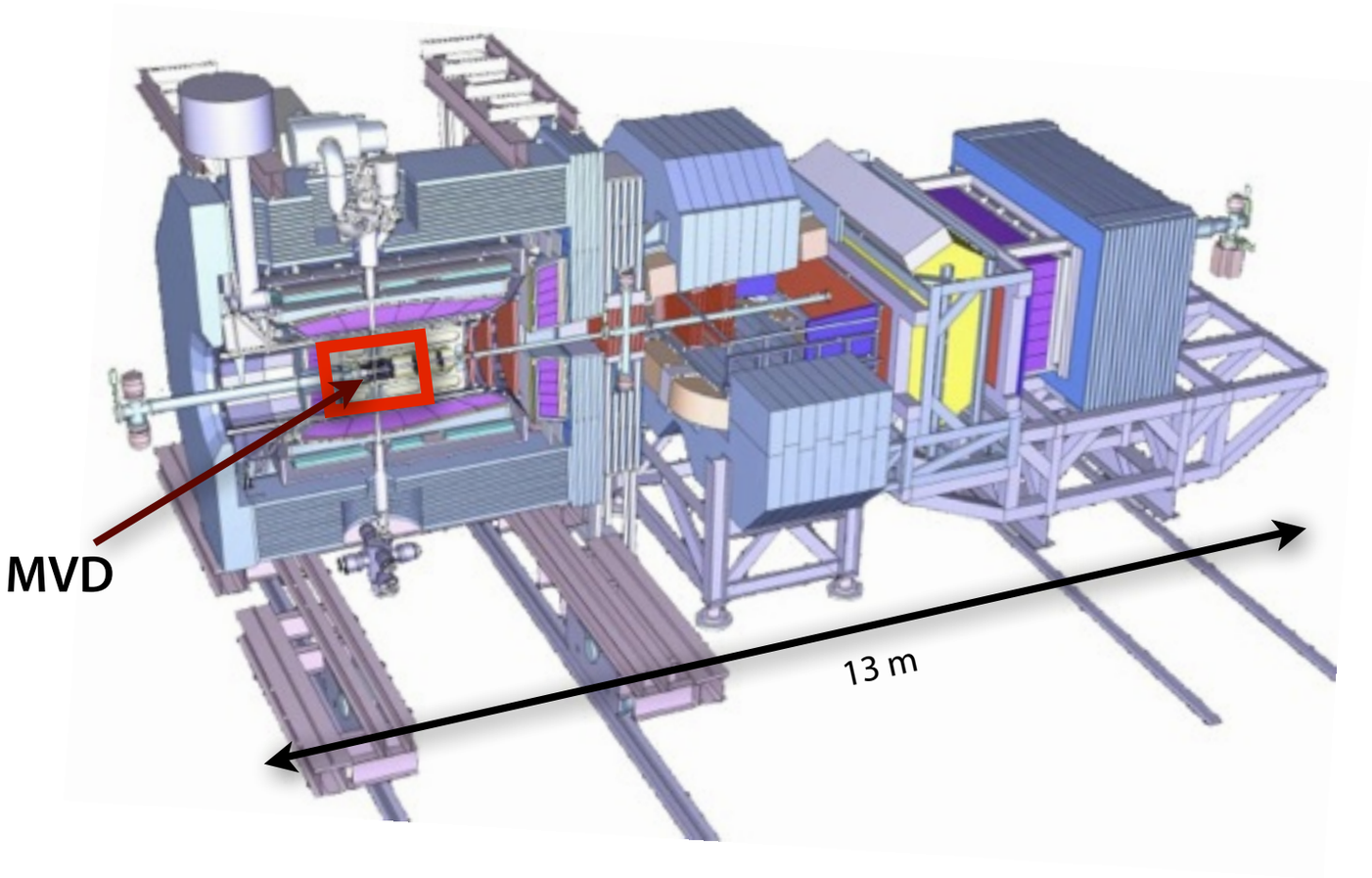
Beam momentum: $P_{max} = 15$ GeV/c

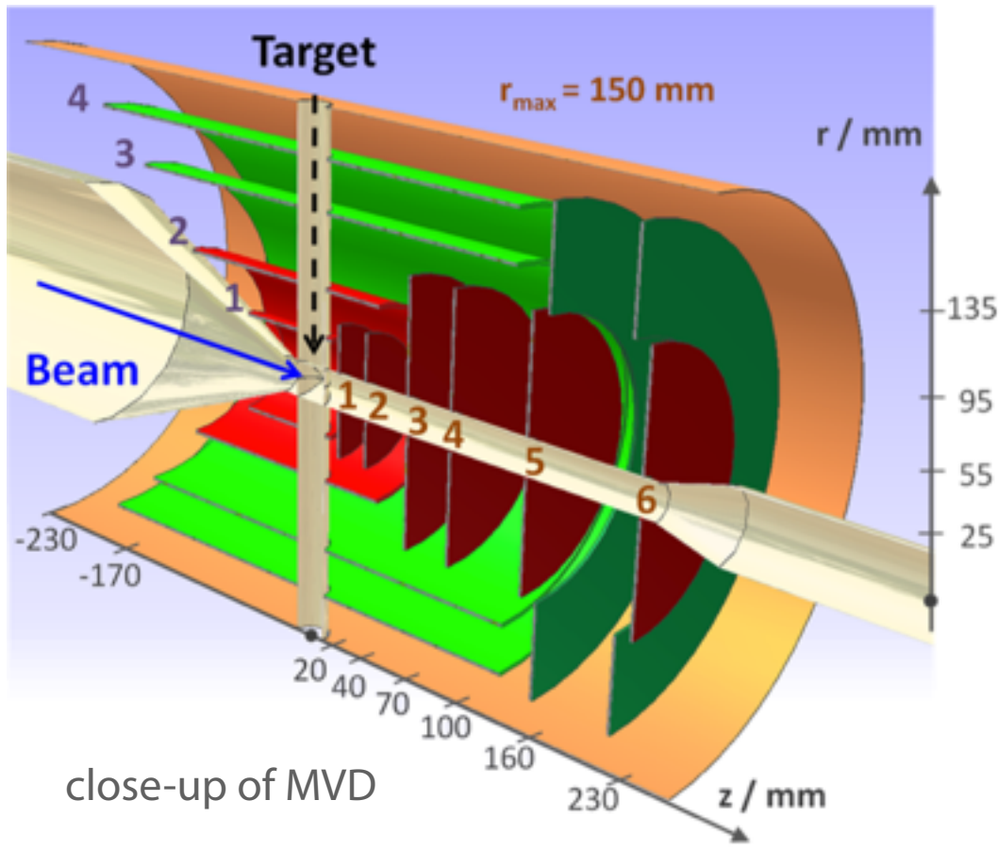
High resolution: $L = 10^{31}$ cm^{-2}s^{-1} $\delta p/p < 4 \cdot 10^{-5}$

High luminosity: $L = 2 \cdot 10^{32}$ cm^{-2}s^{-1} $\delta p/p < 10^{-4}$

$\bar{P}$ANDA Experiment and Micro Vertex Detector

Anti-**P**roton **An**nihilation at **Da**rmstadt





close-up of MVD

- PANDA: particle detector, p^+-p^- collisions with 1.5-15 GeV
  - $2 \cdot 10^7$ collisions per second, event taking untriggered
- MVD: **M**icro **V**ertex **D**etector, innermost tracker
  - Two parts: silicon pixel ($10.5 \cdot 10^6$ ch.) and strip ($1.6 \cdot 10^5$ ch.)

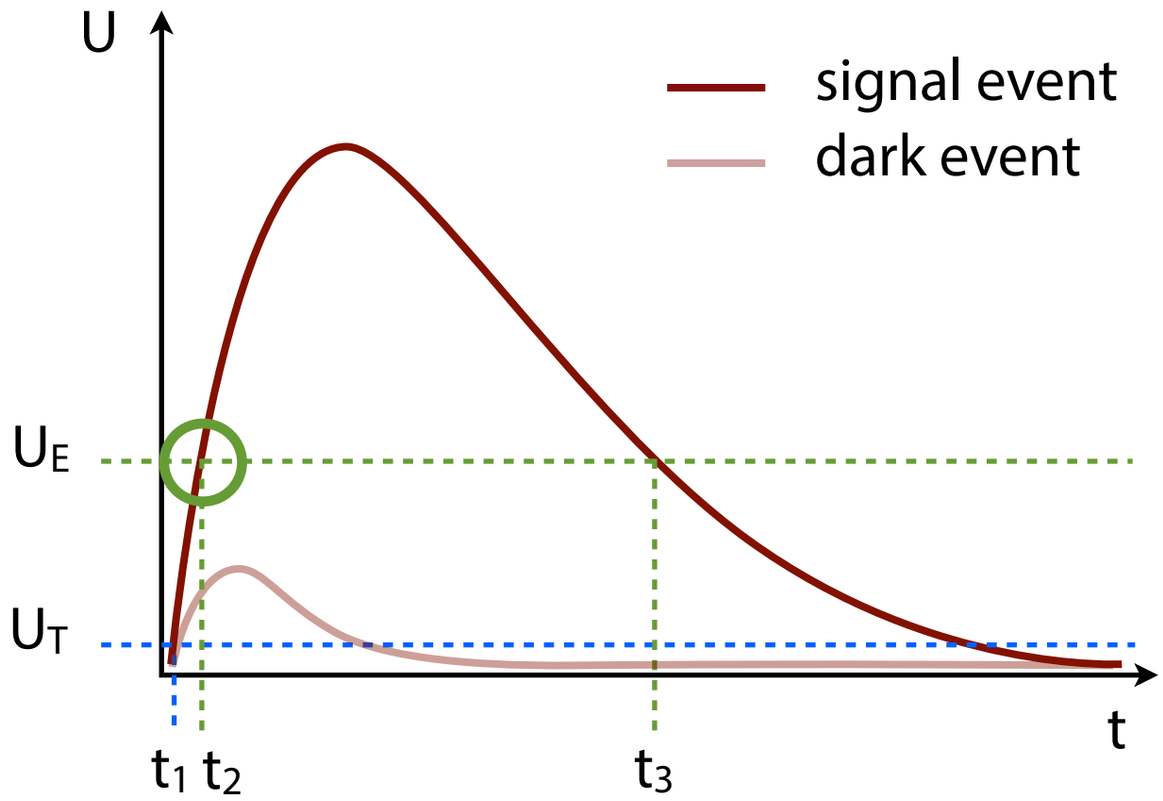
Requirements of the MVD to Readout

- No central trigger information
  - ⇒ Autonomous data taking
- High event rate (2·10^7 collisions per second)
  - ⇒ Minimized dead time — < 6 µs
  - ⇒ High rate capability — 40.000 s^{-1}
- Event building afterwards
  - ⇒ Accurate time information — < 20 ns
- Support event identification
  - ⇒ Measure charge deposition — ≥ 8 bit over dyn. range
- MVD as compact as possible
  - ⇒ Low power consumption — < 4 mW/ch

Time-based readout
- Simple & low power
- Experience with concept (TOF-PET ASIC)

Concept of the ASIC

- Time-based readout of silicon strips
  - Save time stamps (50 ps)
  - Leading edge discriminator
  - Charge by time over threshold

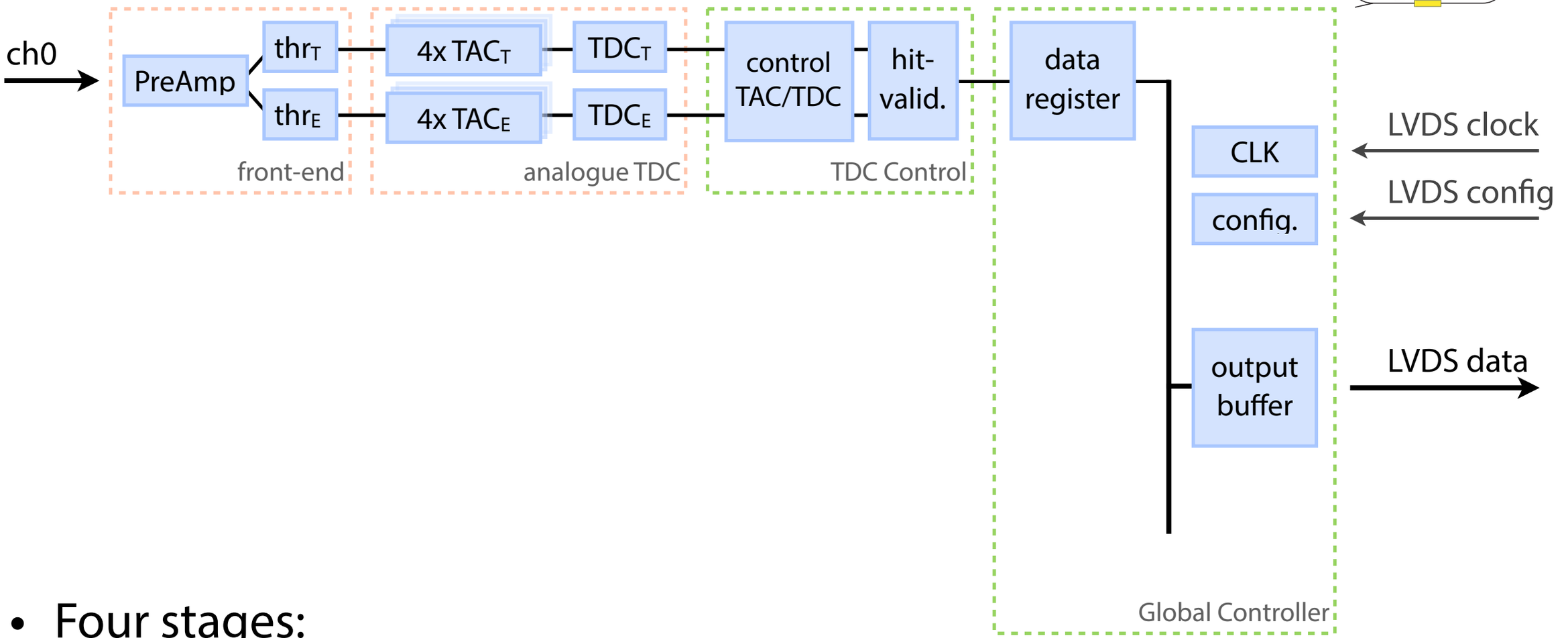


- Two TDCs per channel
  - Time and energy branch
    (low and high threshold)
  - Energy trigger (t_2)
    validates time trigger (t_1)
  - Reduces susceptibility to dark counts

- Concept already realized: TOF-PET ASIC

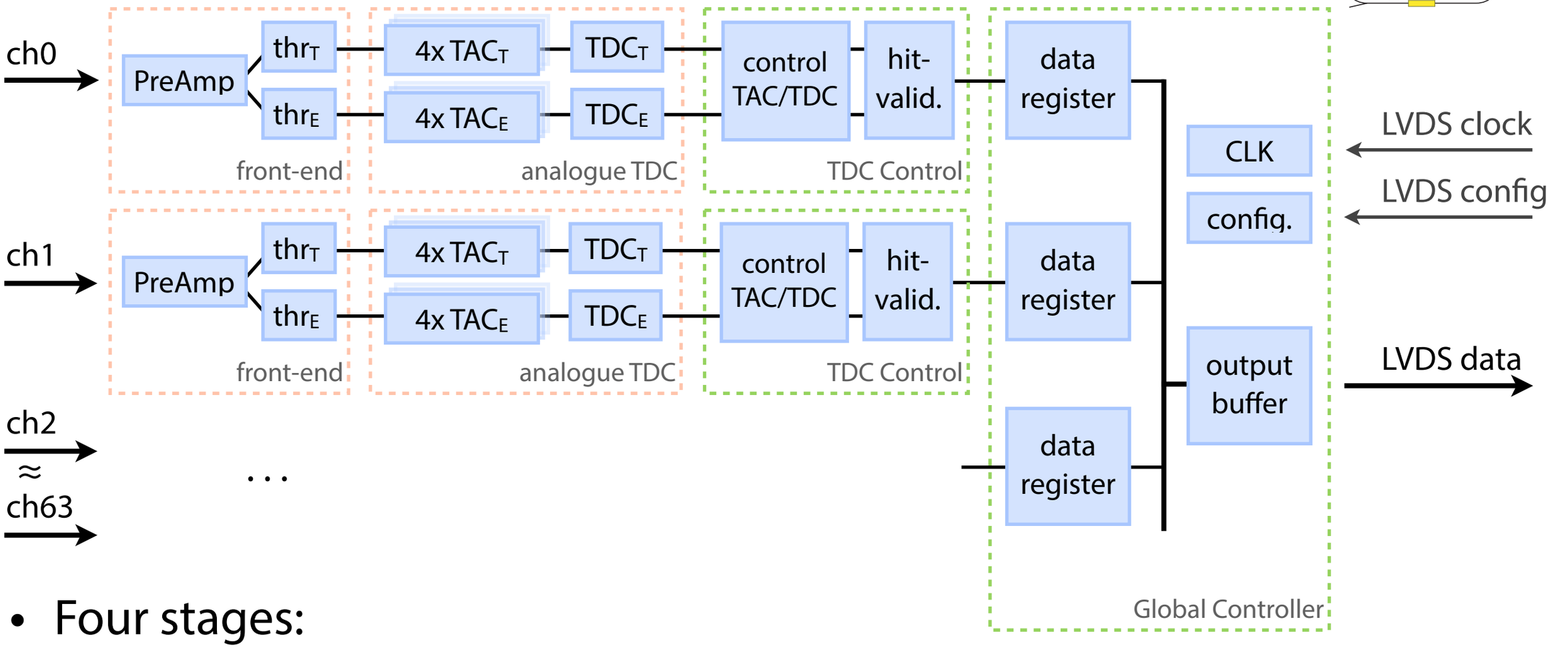
  → Talks by **Manuel D. Rolo** (Tuesday, Thursday)

Concept of the ASIC



- Four stages:
  - **Front-end** (analogue)
  - **TDC** (analogue)
  - **TDC Control** (digital)
  - **Global Controller** (digital)

Concept of the ASIC



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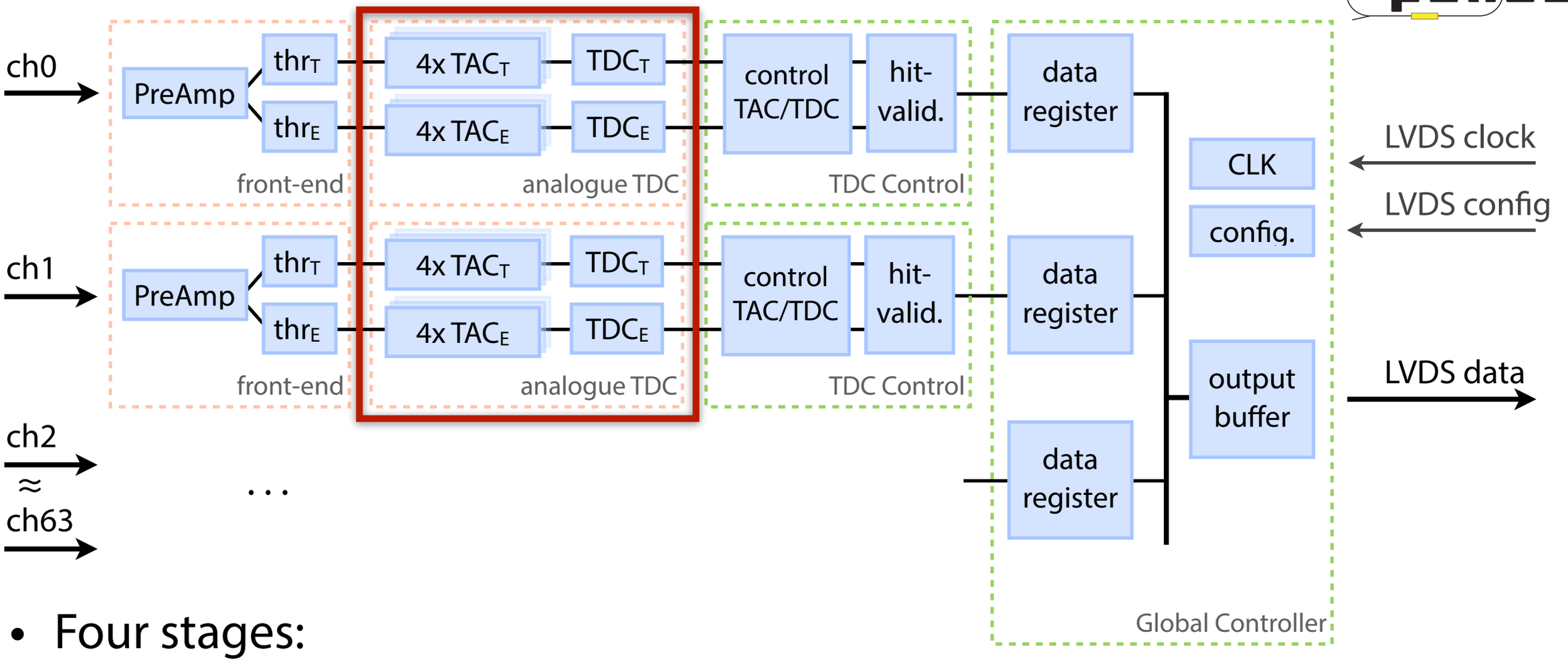

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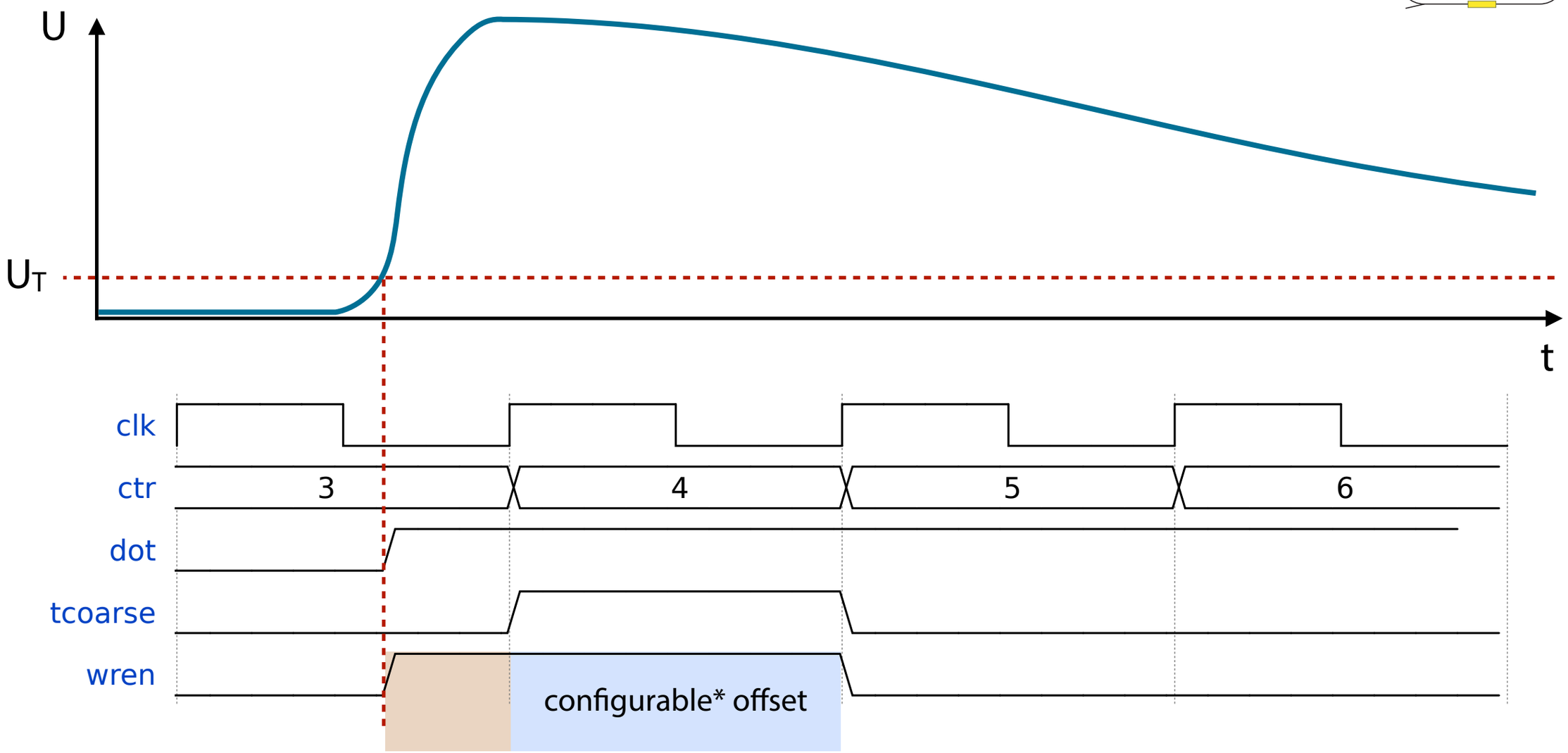
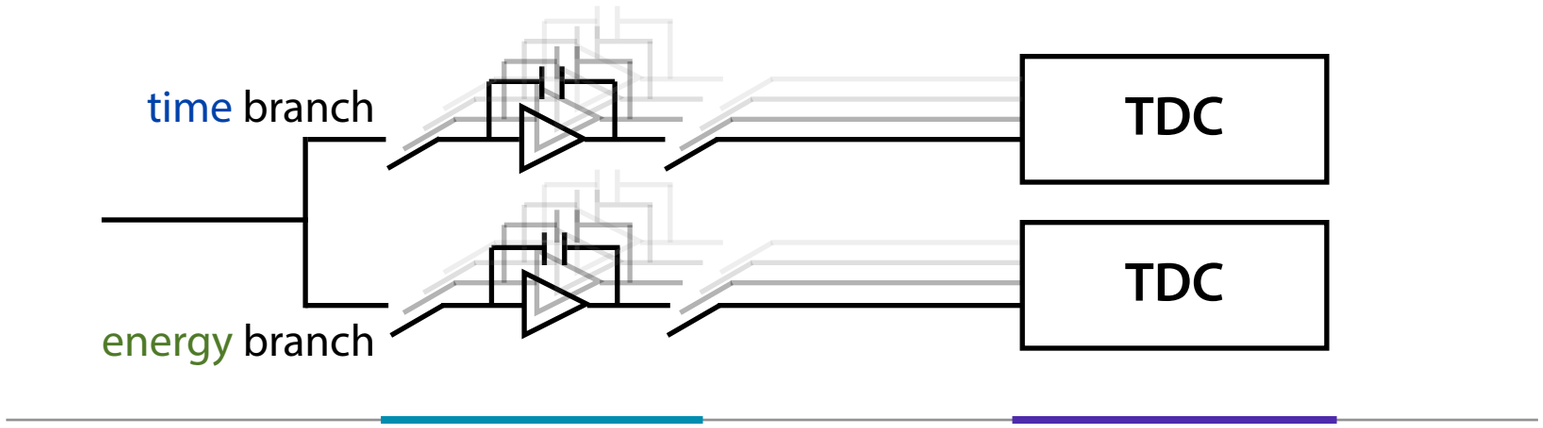
Accurate Time Measurement



*offset values: 0.0; 0.5; 1.0; 1.5 clock cycles

Time-to-Digital Converter



stage 1
front-end

stage 2
analogue TDC

stage 3
TDC CTRL

stage 4
global CTRL

- Two stages: buffer and convert signal

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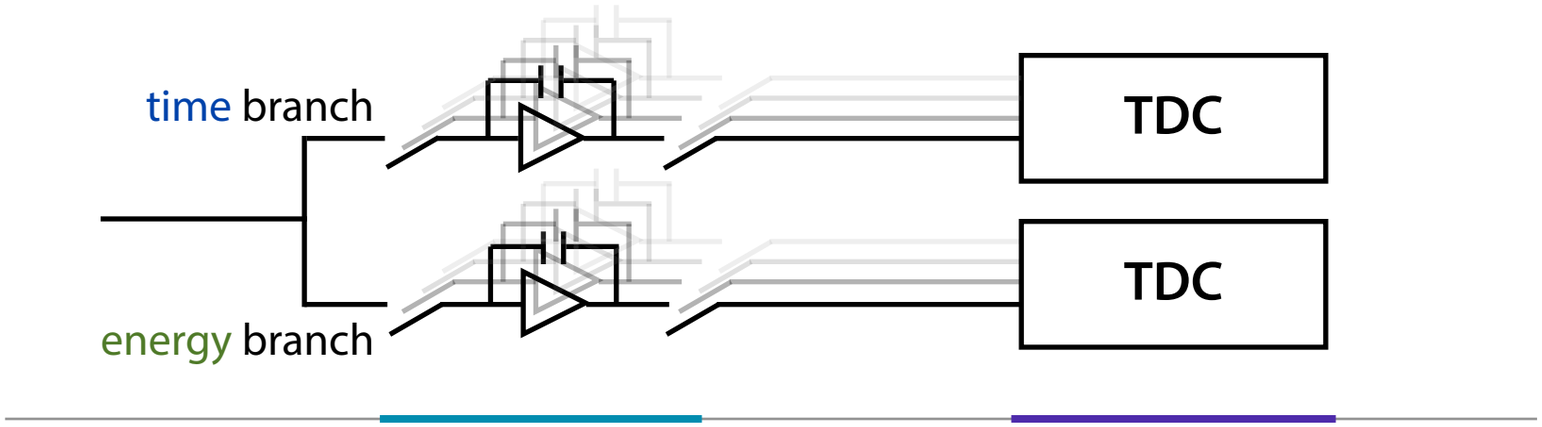

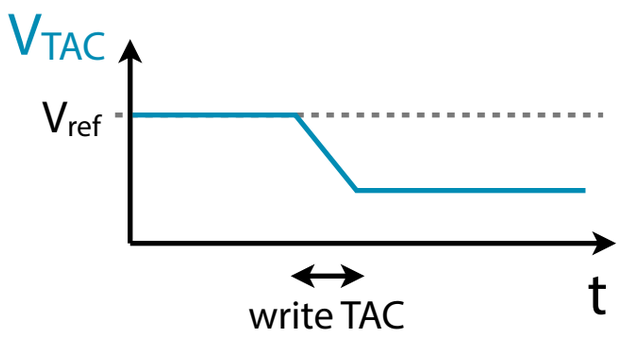

- Two stages: buffer and convert signal
  - Buffering: discharge a capacitor (TAC)
    - **Start**: threshold; **End**: next edge of clock*

stage 1
front-end

stage 2
analogue TDC

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stage 4
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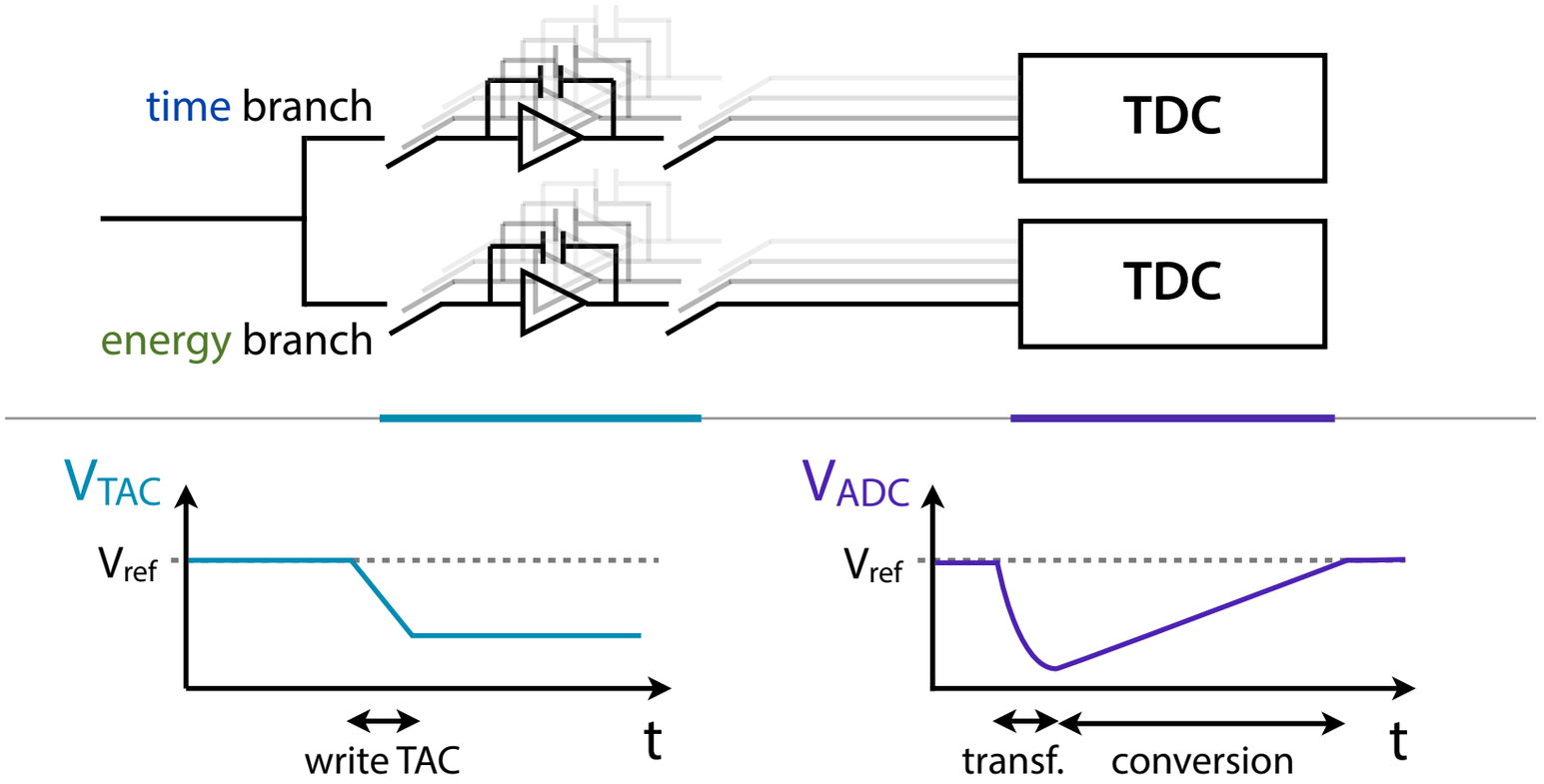
ADC: Analogue to Digital Converter
TAC: Time to Analogue Converter

*: Dynamic range 0-2.5 clock cycles

Time-to-Digital Converter



- Two stages: buffer and convert signal
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  - Transfer to **4x** larger capacitor, linearly recharge with **32x** smaller current (*Wilkinson ADC*)

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*: Dynamic range 0-2.5 clock cycles

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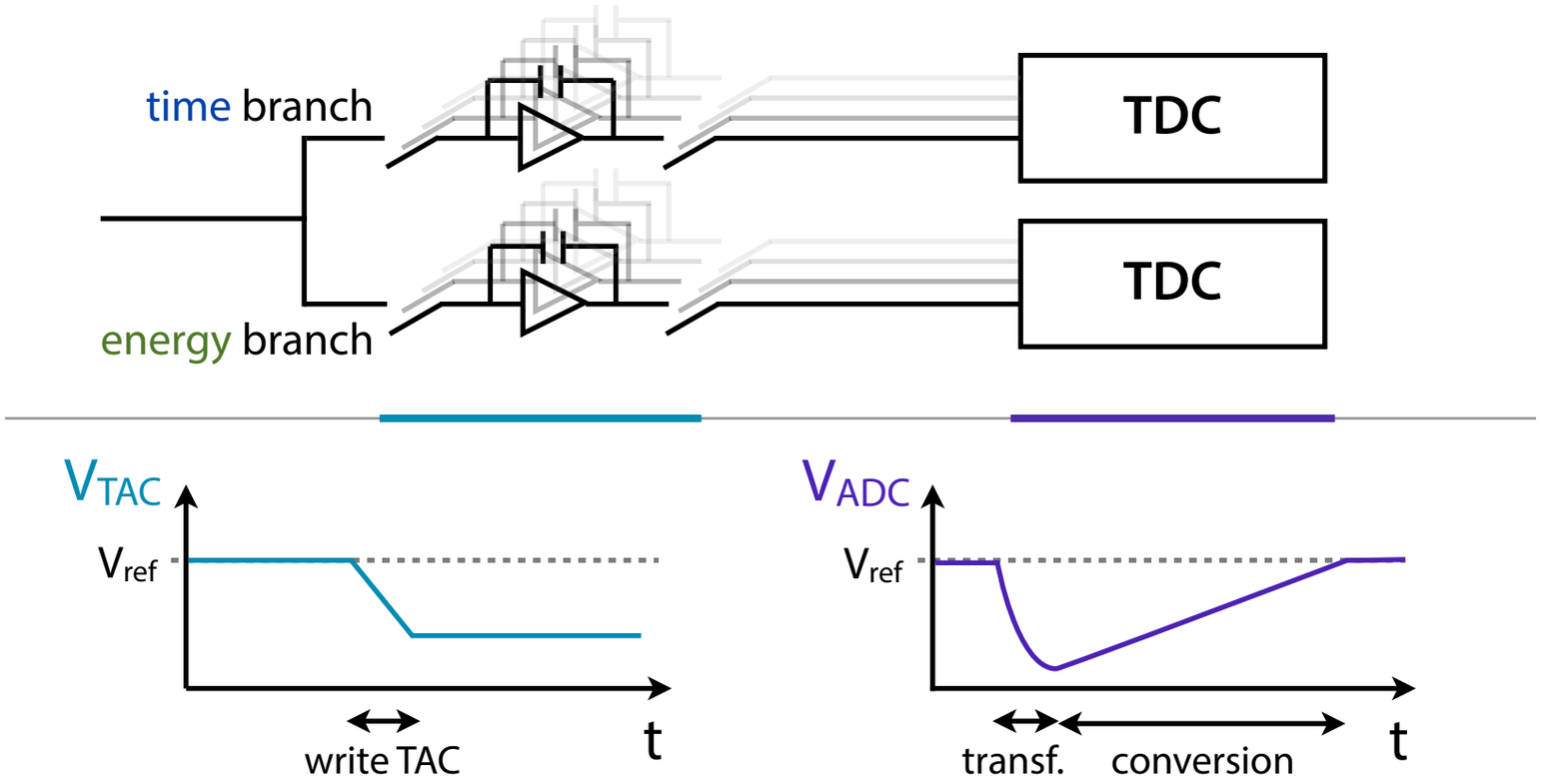

stage 1
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analogue TDC

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global CTRL

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  - Buffering: discharge a capacitor (TAC)
    - **Start**: threshold; **End**: next edge of clock*
  - Transfer to **4x** larger capacitor, linearly recharge with **32x** smaller current (*Wilkinson ADC*)
- Increase time resolution by **128** (50 @ 160 MHz)
  - Conversion takes ~ 3 µs → TAC buffer **multiplicity of 4**

ADC: Analogue to Digital Converter
TAC: Time to Analogue Converter

*: Dynamic range 0-2.5 clock cycles

Readout of MVD Silicon Strips

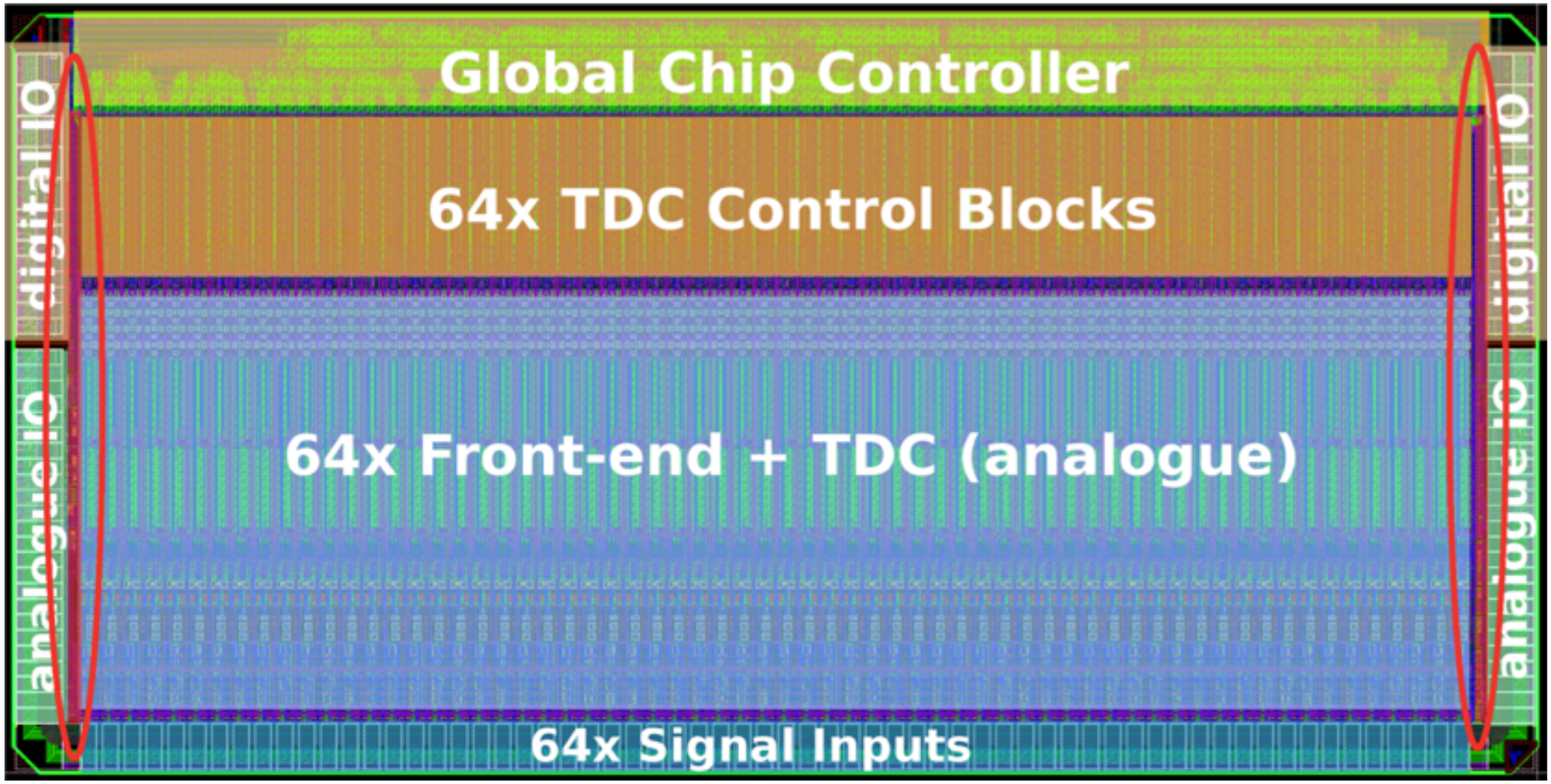
- Most parameters at least near the MVD requirements

	Area	Ch. pitch	Hit rate	Time bin.	CLK	Power
TOF-PET	7.1 x 3.5 mm²	102 µm	< 100 kHz	50 ps	80-160 MHz	7-8 mW/ch
MVD req.	4.2 x 5.0 mm²	60 µm	< 40 kHz	< 20 ns	155.56 MHz	< 4 mW/ch

- Differences to handle:
  - Signal shape / capacitance ⇒ redesign analogue part
  - Area / Channel pitch
  - Different technology
  - Radiation hardening
  - Power consumption
  - General improvements

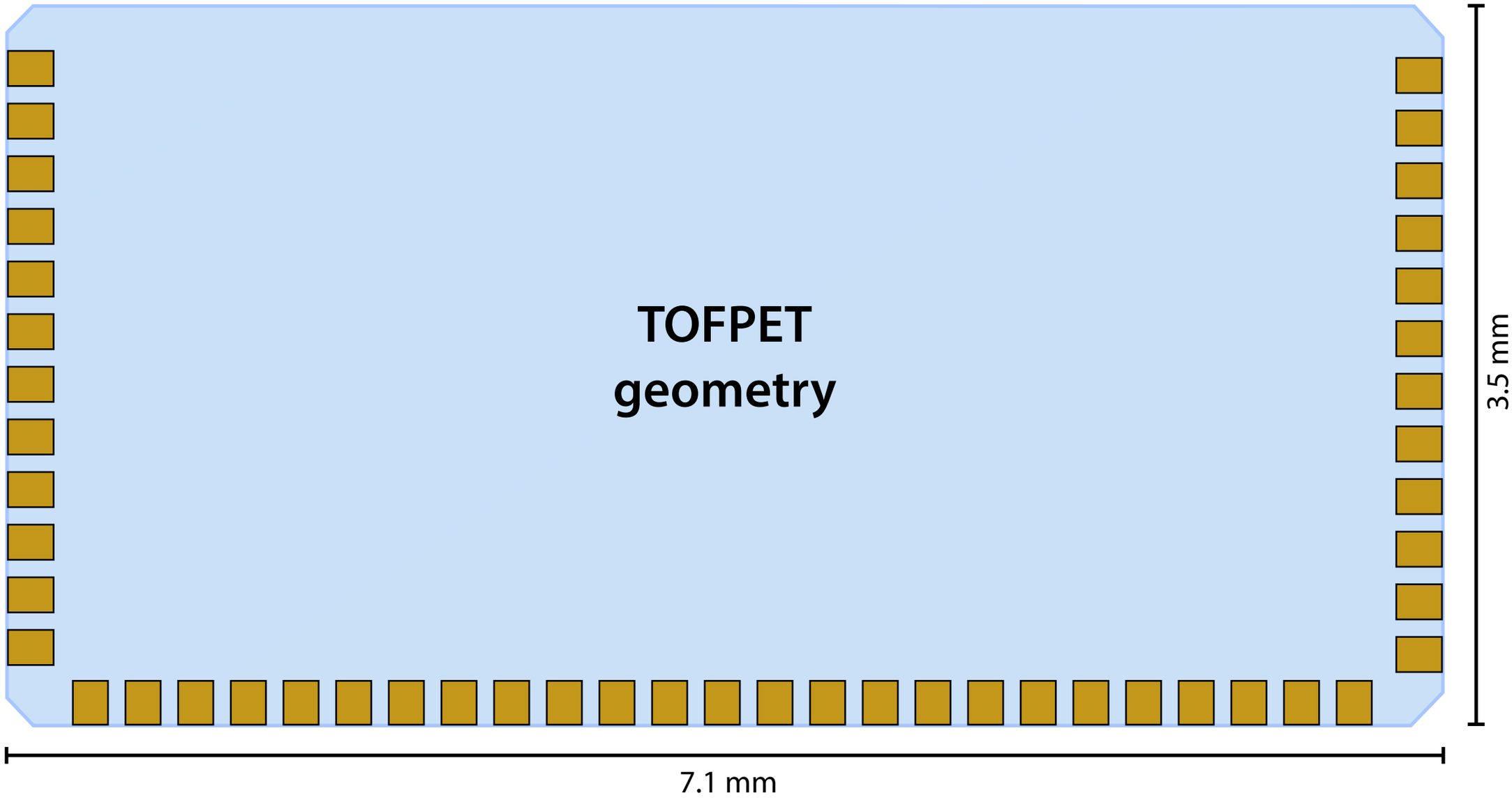
Floorplan of TOF-PET ASIC

- CMOS 130 nm, 64 channels on 25 mm^2
- One pad-free edge to attribute two twin chips back-to-back



Red ellipses: bias and calibration circuitry

Changes in Geometry for PASTA



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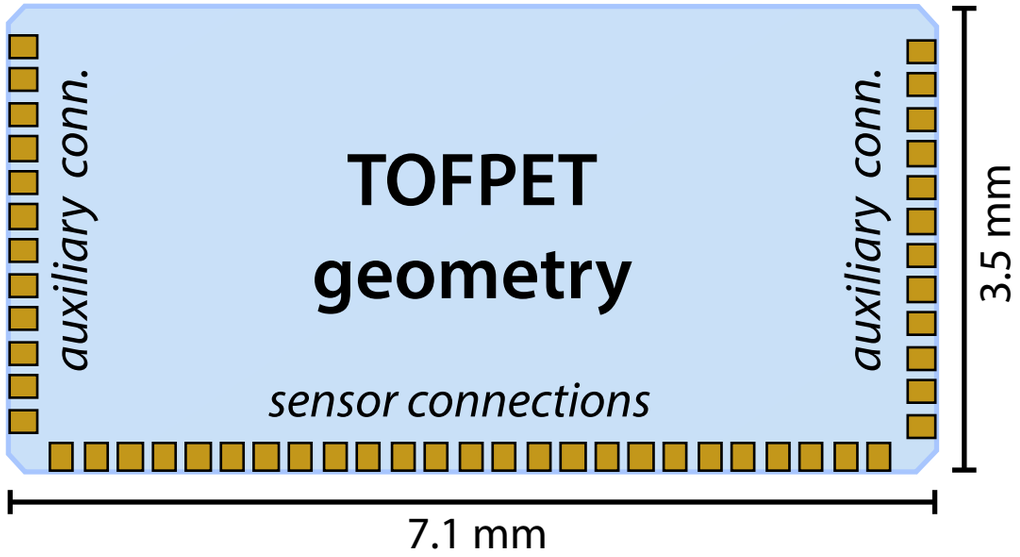
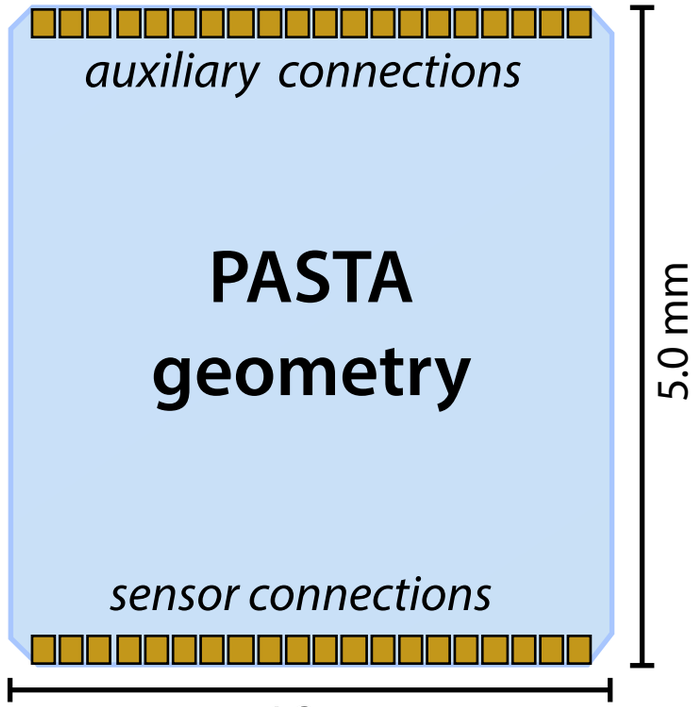




- Footprint: 7.1 × 3.5 mm² → 4.2 × 5.0 mm²
  (25 mm² → 21 mm²)
- Smaller channel pitch: 102 µm → 60 µm
- Position of bonding pads: front, sides → front, back

Change of Technology

- Switch towards area optimized technology (tecB)
  - Supports the reduction of the pitch
  - Structure size: 130 µm, tecA → 110 µm, tecB
  - Less development costs
    - Shared wafer instead of full engineering run

- Typical changes in digital project
  - Area occupation: ↘ 30-50 %
  - Power consumption: ↗ 10-20 %

Radiation Damage

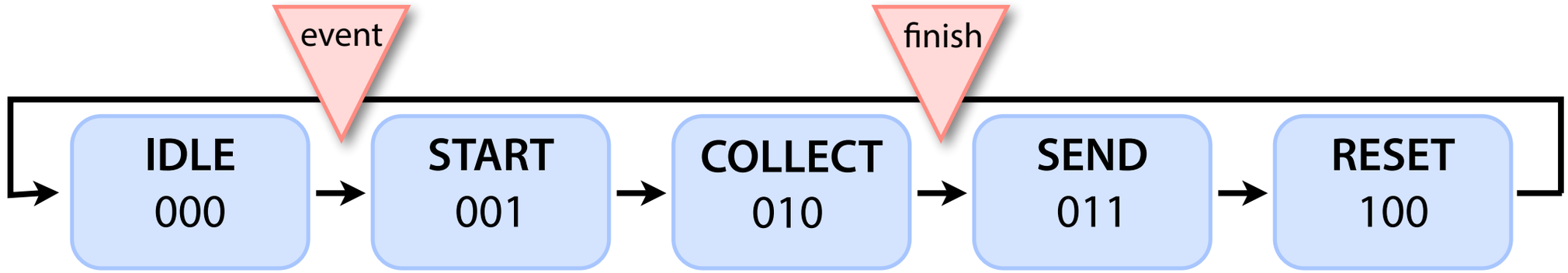
- Charge deposition in electronics can lead to:

- **Hard errors**
  - Destruction of gates
  - Permanent damage

- **Soft errors**
  - Effects only temporary
  - Single Event Upset (SEU)
    - Change a value inside a flip flop (buffer)

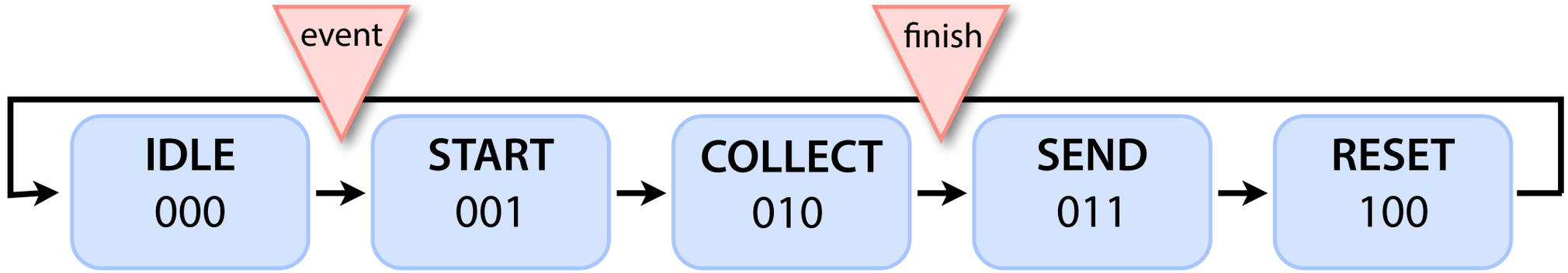
Single Event Upset

- *Example:* a fictional readout control
- Normal operation



Single Event Upset

- *Example:* a fictional readout control
- Radiation environment



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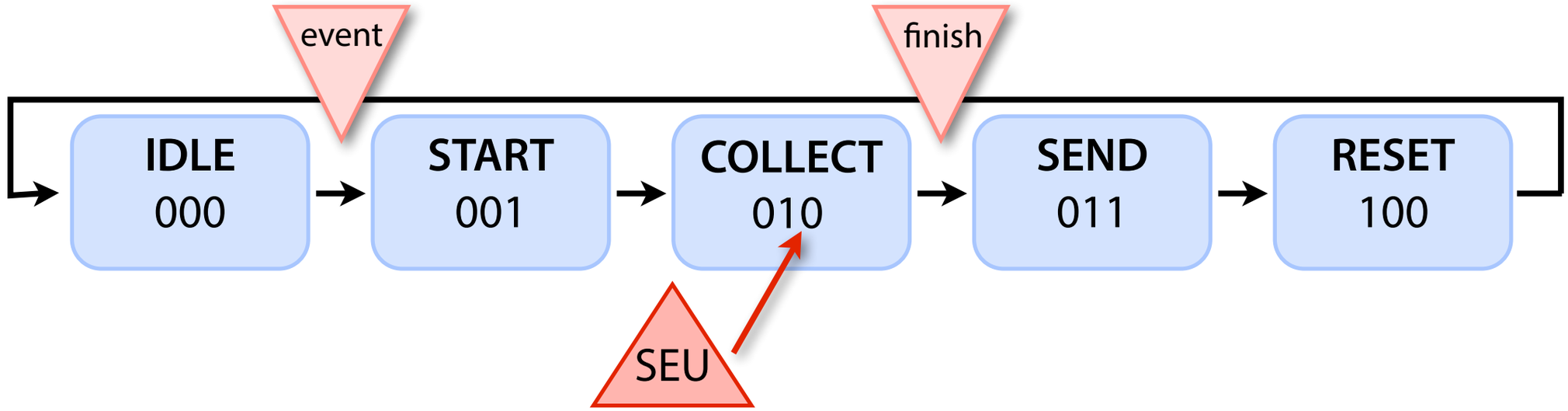

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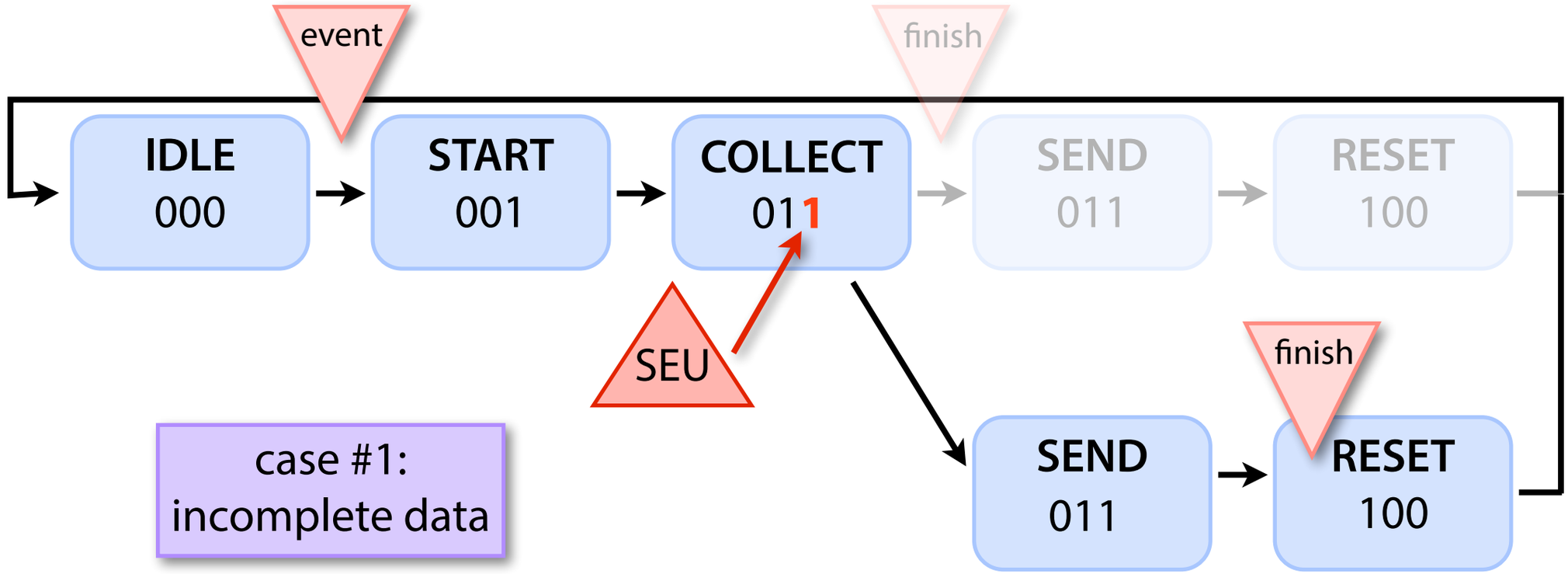

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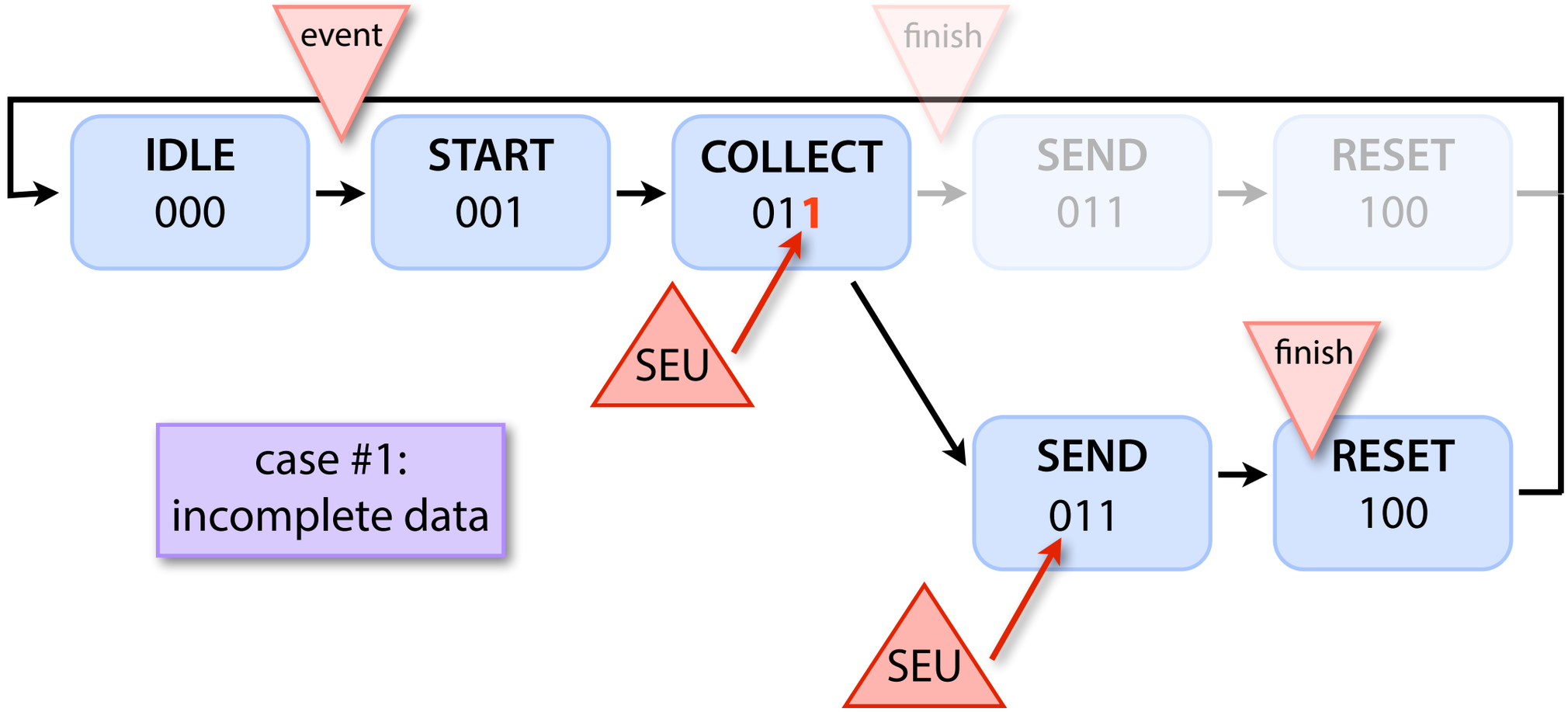

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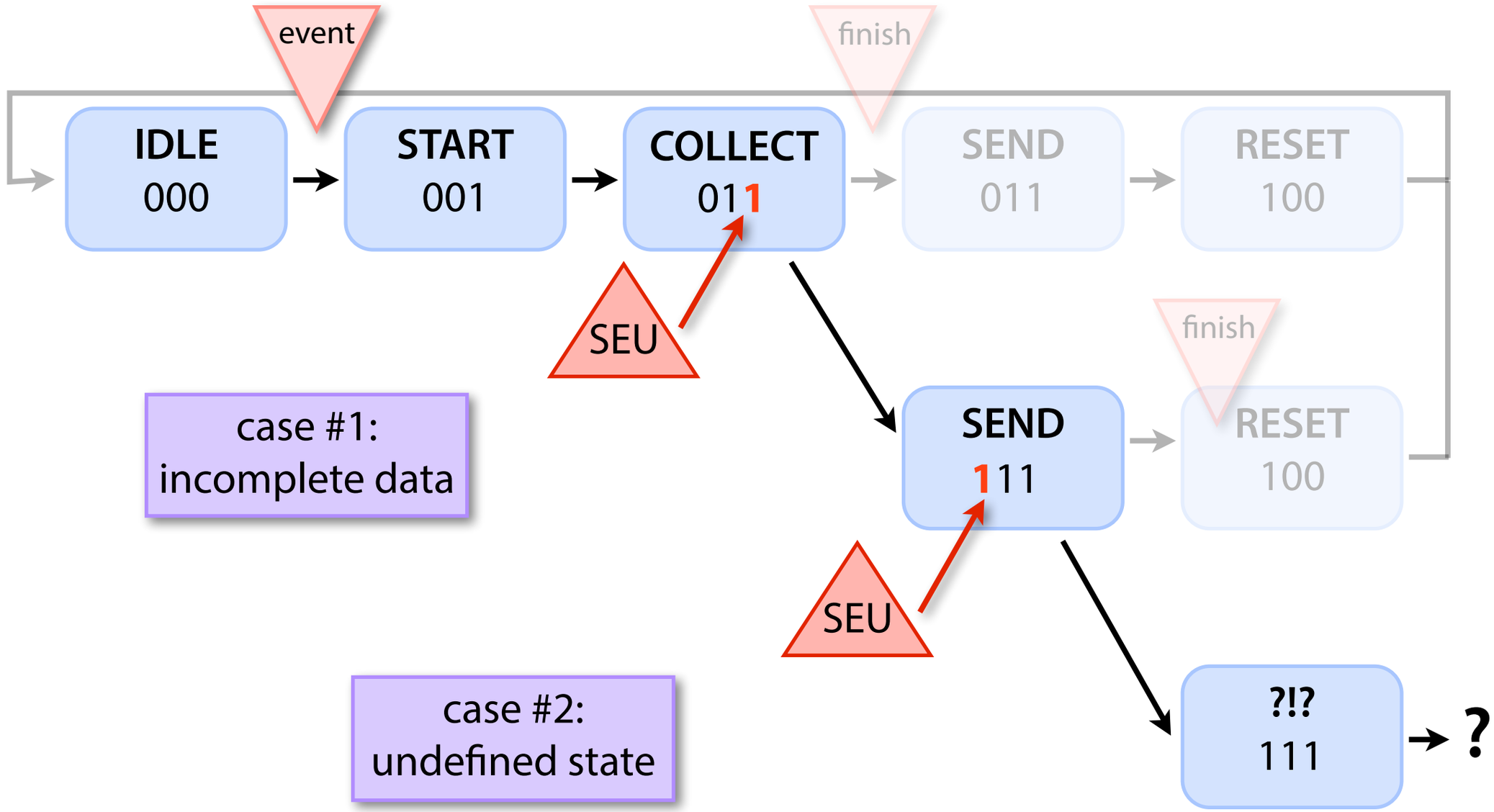
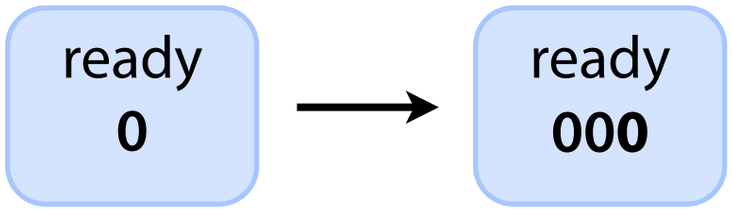


Prevent Logic Freeze

- Single bit:
  - Triple Mode Redundancy (TMR)



TDC CTRL v1

Single bit FF: 140

TMR protected: 30

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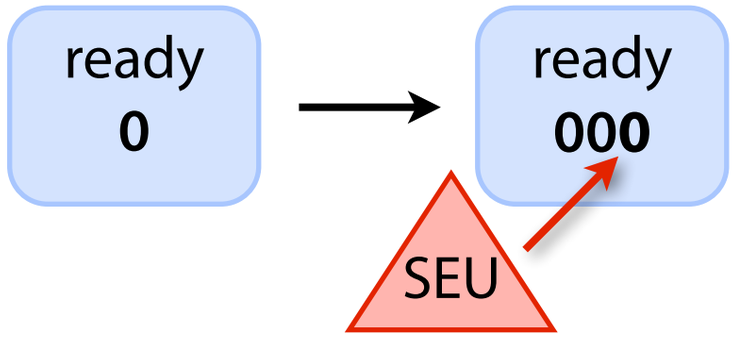

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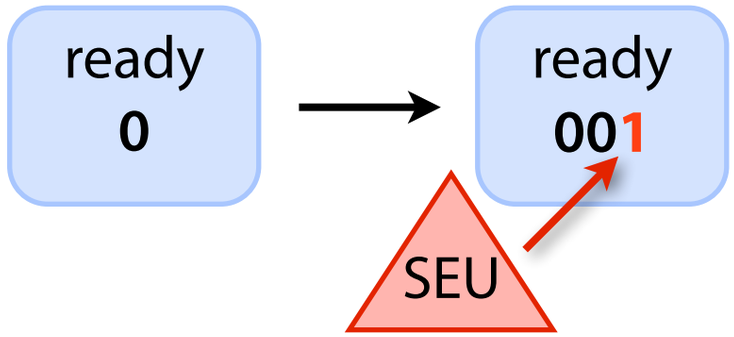

majority still says **0**

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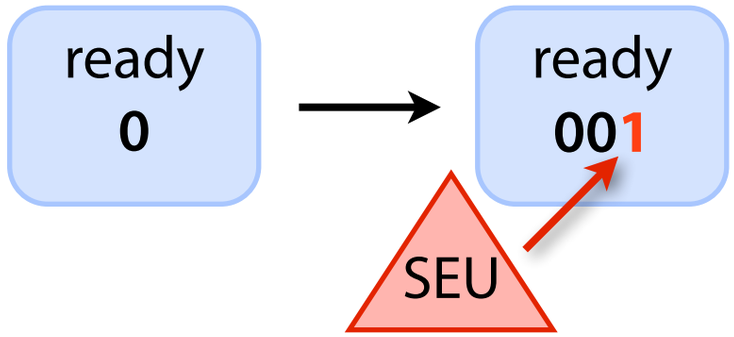
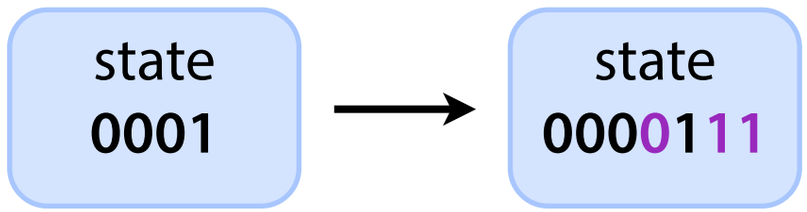


majority still says **0**

TDC CTRL v1

Single bit FF:	140
TMR protected:	30

- Multiple bits (e.g. state machine):
  - Hamming encoded states



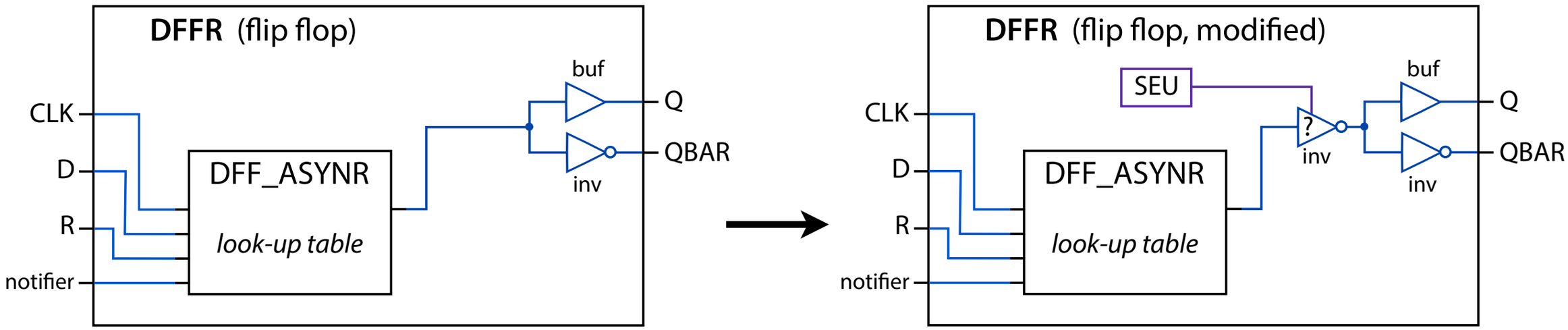
  - additional parity bits to detect and correct SEU

TDC CTRL v1

Multiple bit FF:	320
Hamming protected:	133
(state machines:	100)

Simulate SEU

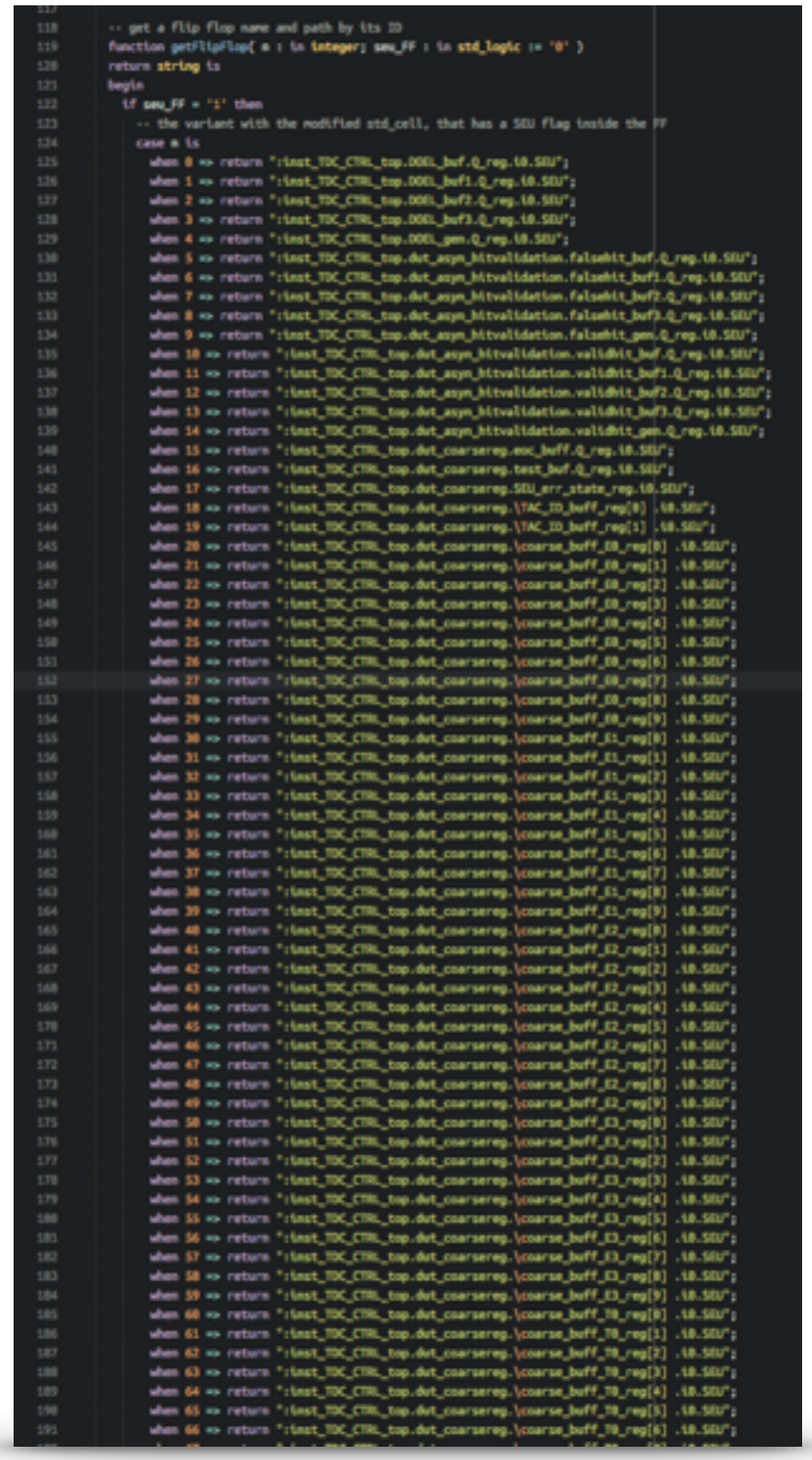
- Step 1: Ability to simulate a SEU
  - Functions of development environment »Cadence«
    - `nc_force`: forces a signal inside the logic to a given value
    - `nc_release`: releases a previous force
  - Problem: flip flop in simulation without internal memory
    - Idea 1: Flipped value in input wire
    - Idea 2: Modified standard cell library



Simulate SEU in Project

- Step 2: Check all flip flops
  - Which flip flops are critical? (besides state machines)
  - Tool to generate list of flip flops
    - Input: design after synthesis
    - Python parser filters input
    - Output: VHDL package
  - Test bench implementation
    - Include generated file
    - One command generates the SEU:

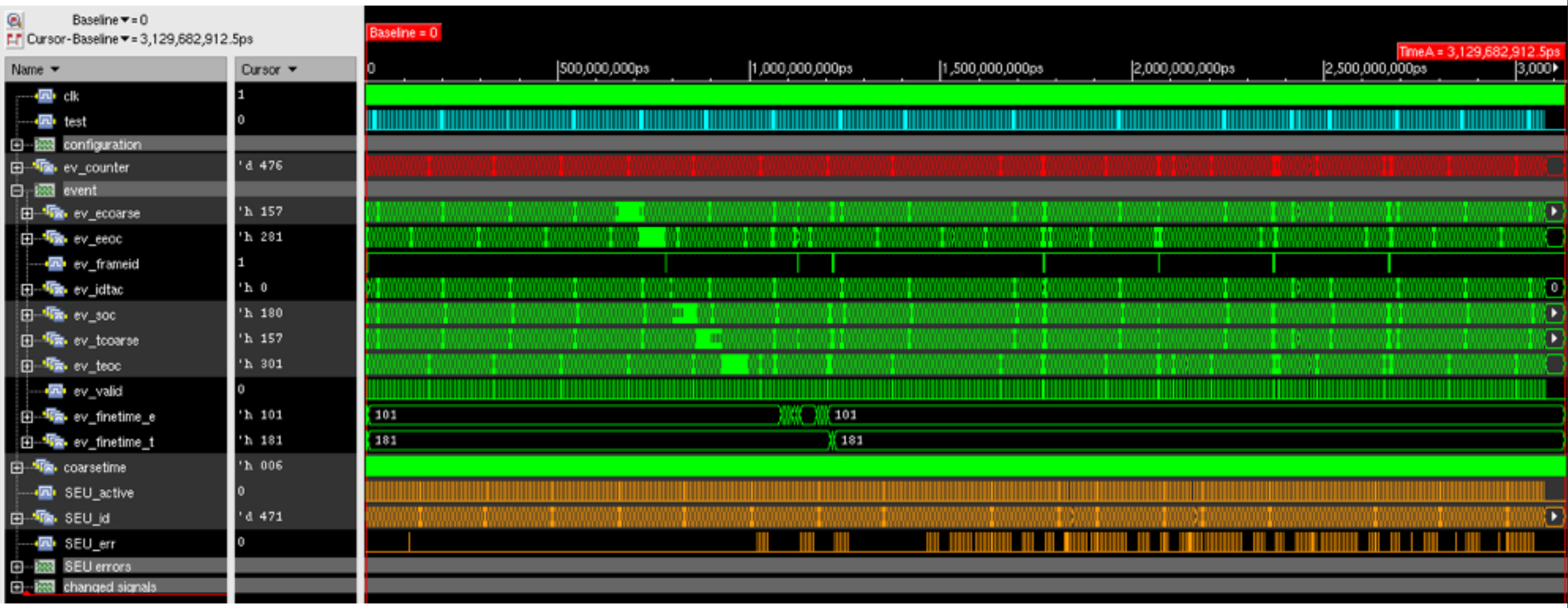
      ```
      sim_SEU_FF( ID, clk, clk_period );
      ```
  - Found 24 critical flip flops



→ Code at: https://github.com/Nepomuk/HDL-radiation-tools

Result of SEU Tests

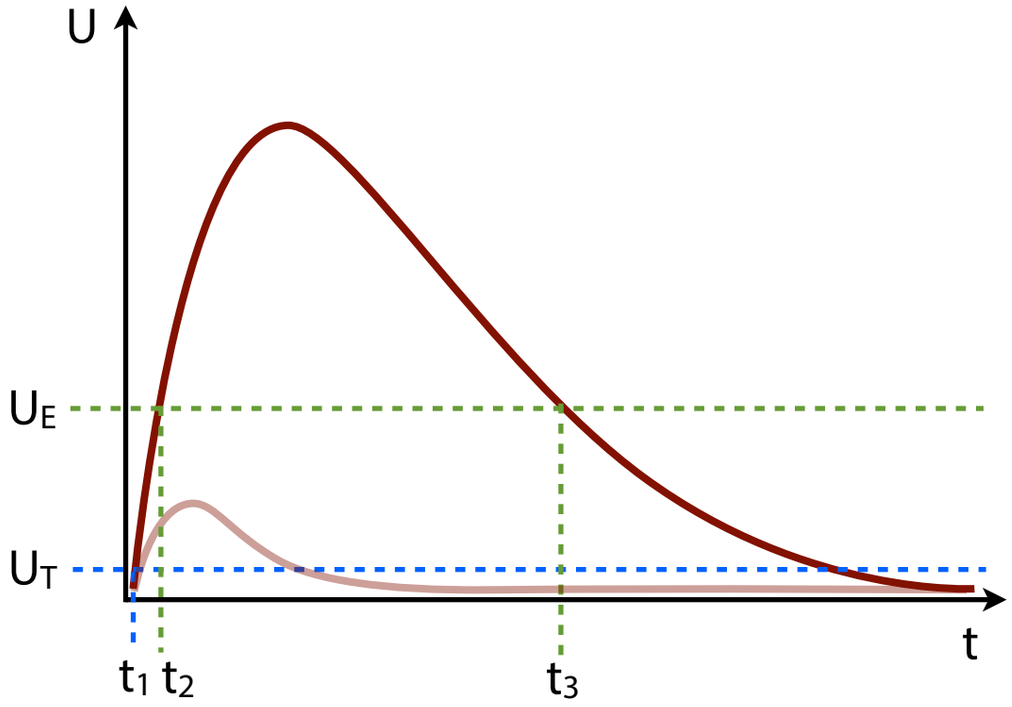
- Test of all 460 flip flops: (TDC CTRL v1)



- No logic freeze
- Only corrupted data (→ parity bit)

Some Conceptual Differences

- **New TDC control** (clearer & simpler structure)
- Time buffers move to global controller
  - Saves connections, speed up simulations
- Hit validation in two ways
  (delayed & synchronous)
- More flexibility what to store
  (t_1-t_3, t_1-t_2, test pulse)
- Optimization in charging time
  - Smaller offset in TAC charging
  - Conversion end on falling edge
- TAC refresh local instead global
  (Capacitors back to reference level after inactivity)



Current Status of TDC Control

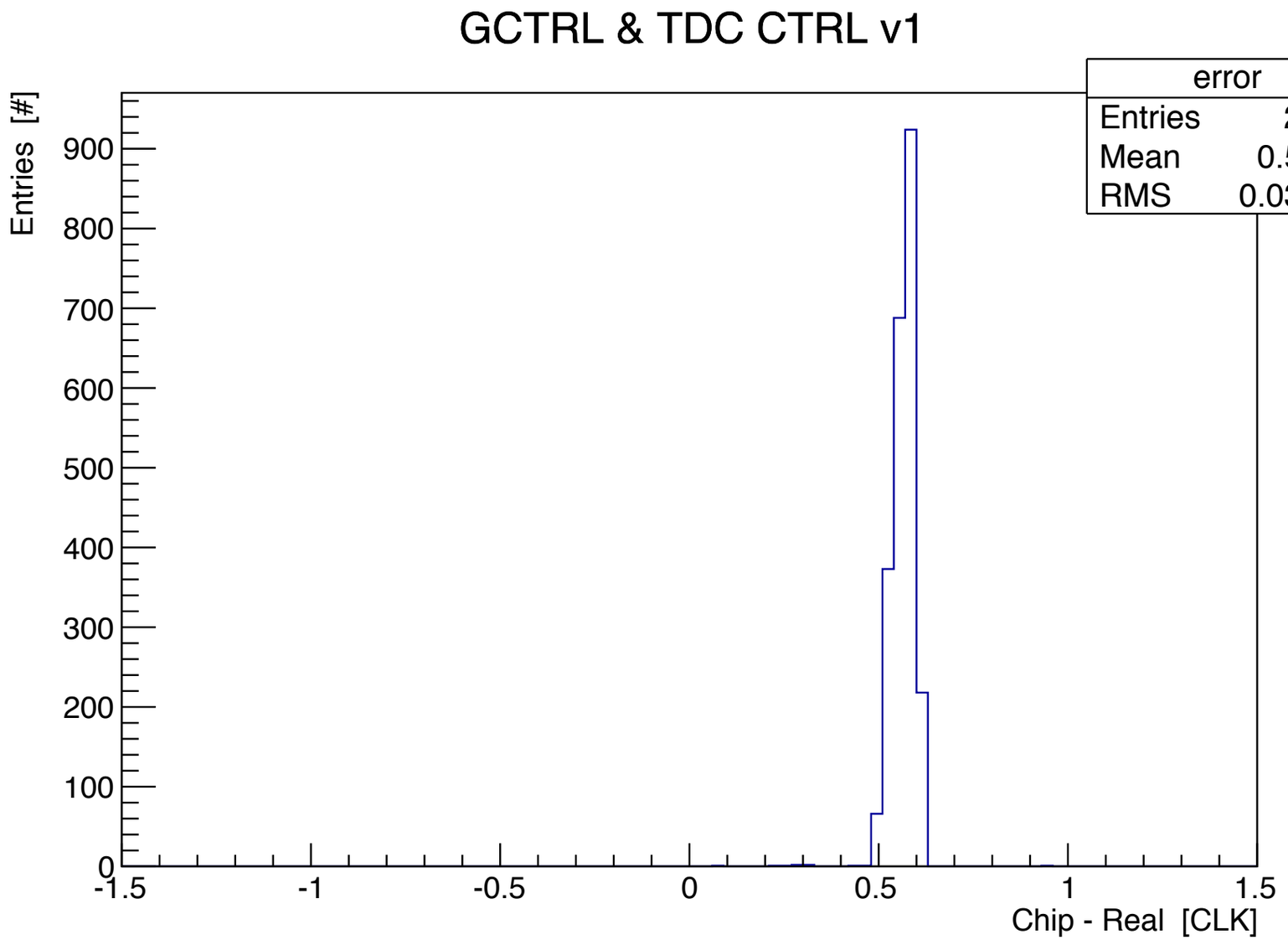
- Basic concept is implemented
  - Trigger, TAC selector, charge transfer and measurement, …
- Left to do:
  - Solve inefficiency for events close to clock
  - SEU protection (*TDC CTRL v1* has it, *v2* not yet)

	TDC_CTRL v1 (incl. SEU, tecA)	TDC_CTRL v1 (incl. SEU, tecB)	TDC_CTRL v2 (current status, tecB)
Occupancy (1.1 x 0.1 mm²)	84.8 %	37.0 %	5.6 %
Cells	3155	2850	261
Power (@ 160 MHz)	1.57 mW/ch	1.78 mW/ch	0.05 mW/ch

Estimate for final TDC Control:
Save up to 80-90% in terms of power/occupancy

Current Status of GCTRL

- Global controller merged to TDC_CTRL v2
  - Time stamps moved, different connections, small adaptions
  - Test bench for digital part …



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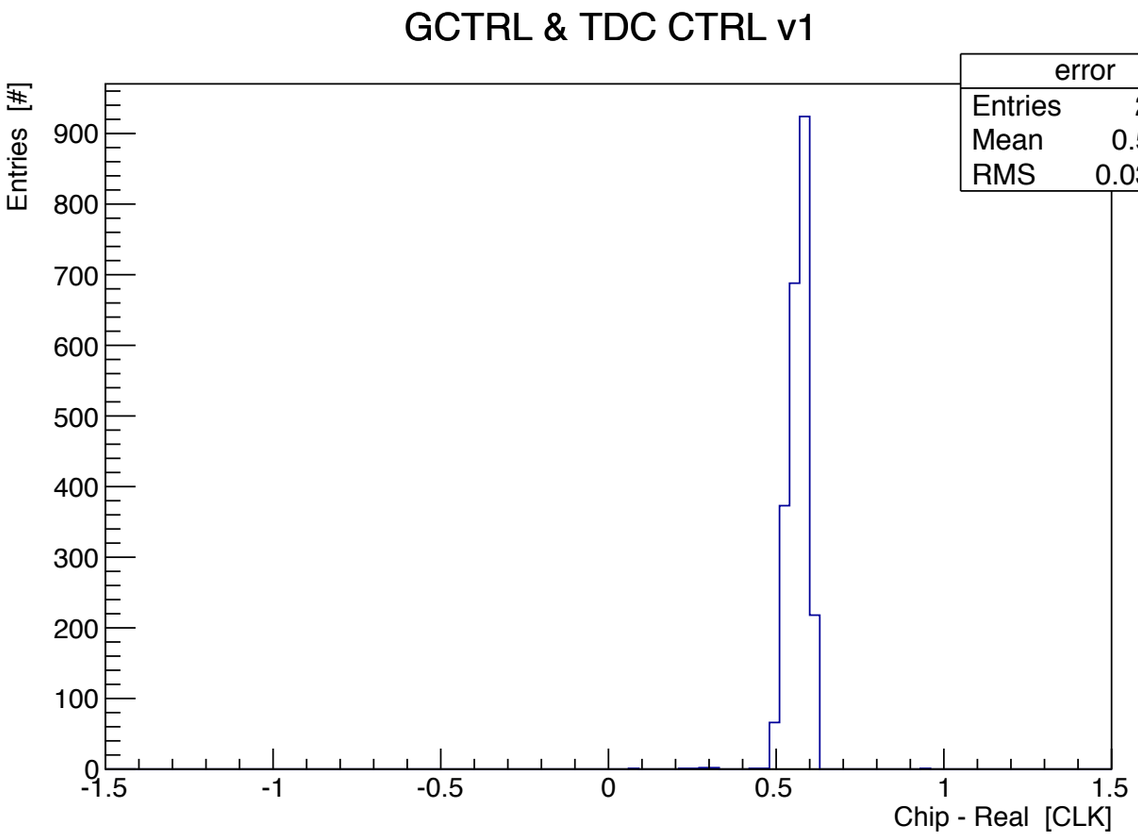
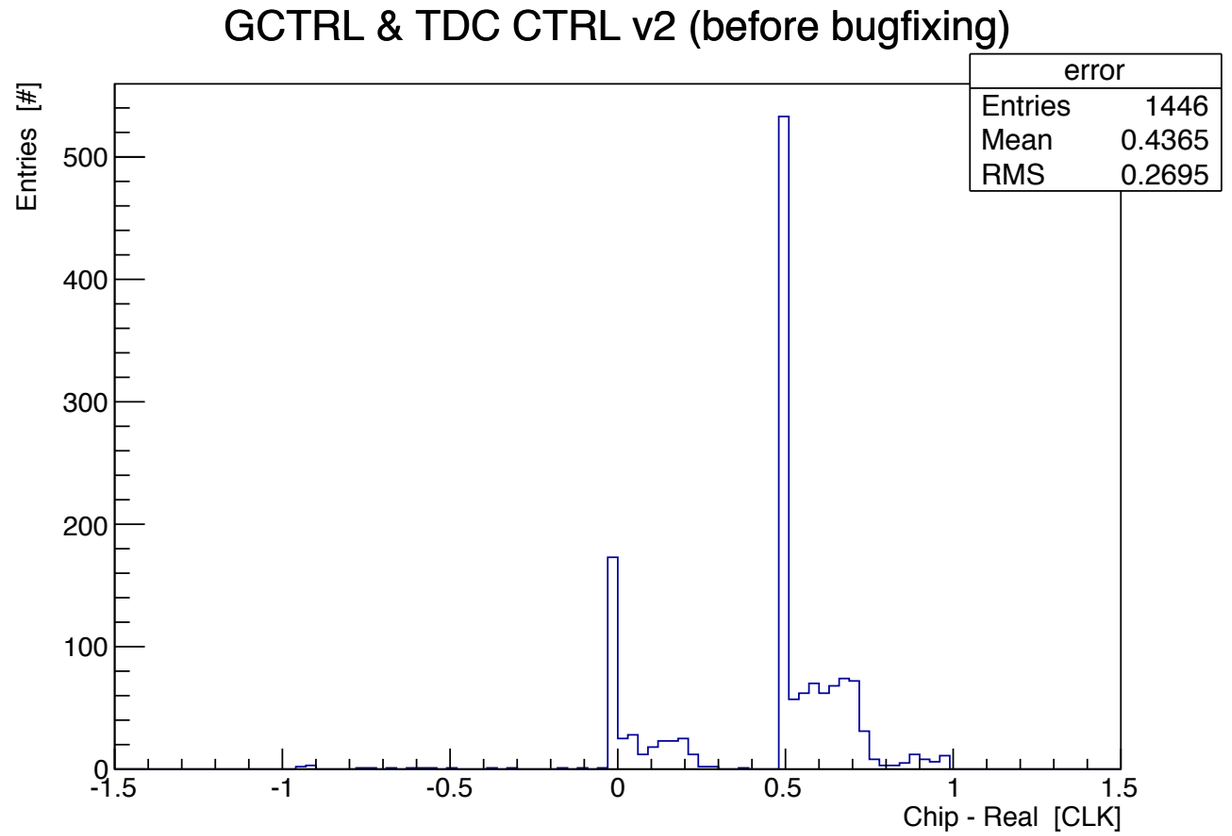
  - Test bench for digital part …





Current Status of GCTRL

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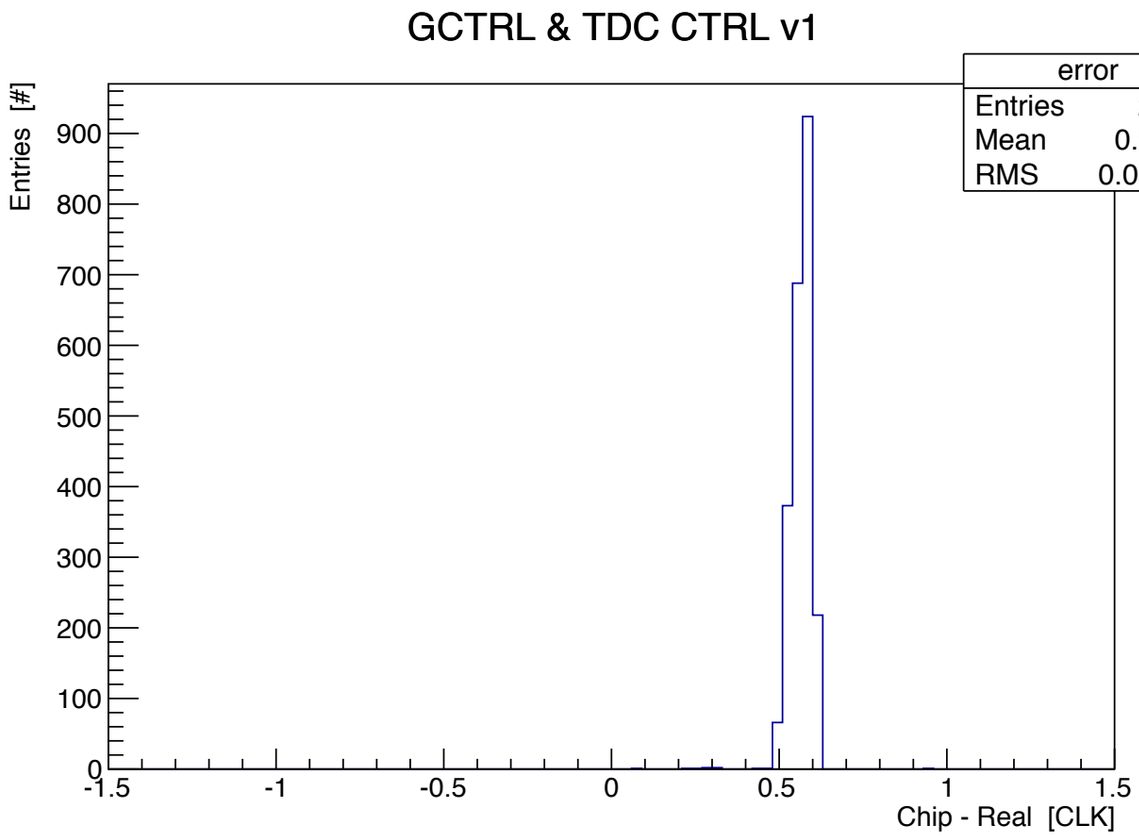

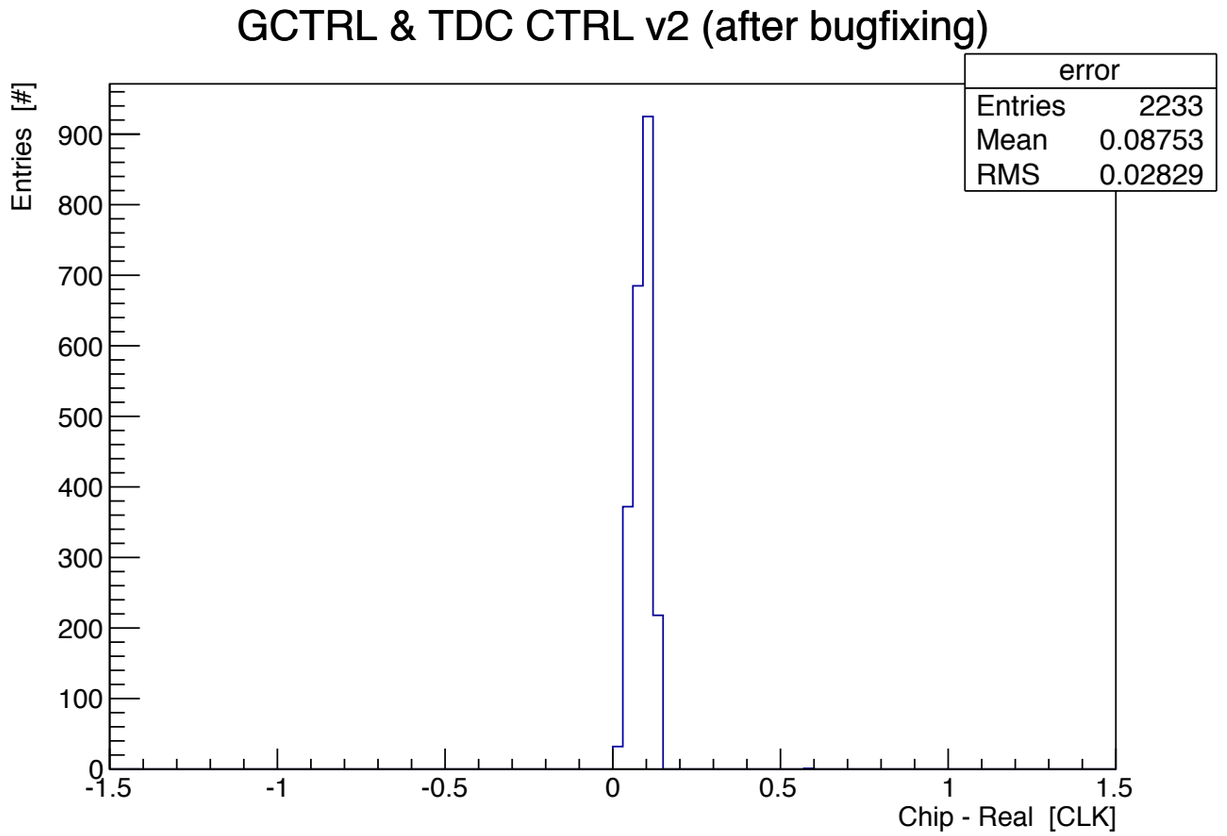

Current Status of GCTRL

- Global controller merged to TDC_CTRL v2
  - Time stamps moved, different connections, small adaptions
  - Test bench for digital part ✓
- Left to do:
  - TAC refresh
  - SEU protection

	GCTRL v1 (tecA)	GCTRL v1 (tecB)	GCTRL v2 (current status, tecB)
Occupancy (0.35 x 6.6 mm²)	70.5 %	38.1 %	34.5 %
Cells	44,949	45,695	57,703
Power (@ 160 MHz)	52.2 mW	61.3 mW	65.4 mW

Conclusion & Outlook

- Time-based MVD strip sensor readout
  - High time precision (50 ps)
  - Charge by ToT
  - Two thresholds
- First PASTA version in development
  - Based on experience from TOF-PET
  - Enhancements towards strip readout (Diff. preamplifier, changed geom.)
- Future:
  - Include SEU protection
  - Production in course of 2014

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Thank you!

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Resources

- [**2**, PANDA detector] PANDA Collaboration (2013)
- [**3**, map showing GSI] Screenshot Google Maps (2013) [→ direct link]
- [**3**, FAIR construction] Jan Schäfer; FAIR homepage (2013) [→ direct link]
- [**4**, FAIR] GSI Helmholtzzentrum für Schwerionenforschung (2013)
- [**7**, PANDA & MVD] PANDA Collaboration (2013)
- [**11**, MVD requirements] PANDA Collaboration; *PANDA Technical Design Report for the Micro Vertex Detector* (2013) [→ direct link]
- [**12**, floorplan] Manuel D. Rolo, LIP Lisboa / INFN Torino (2013)