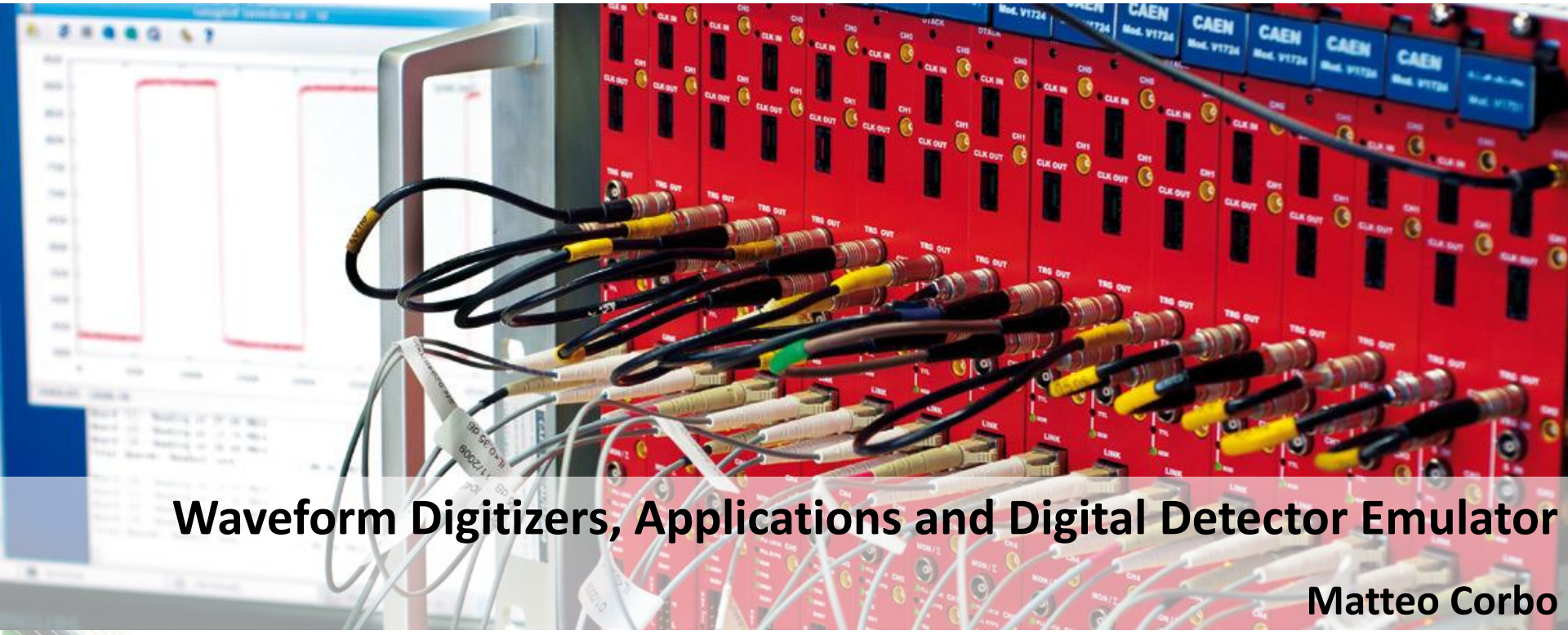
CAEN

Tools for Discovery

www.caen.it

ISO 9001:2000
CERT. N. 9105.CAEN



Waveform Digitizers, Applications and Digital Detector Emulator

Matteo Corbo

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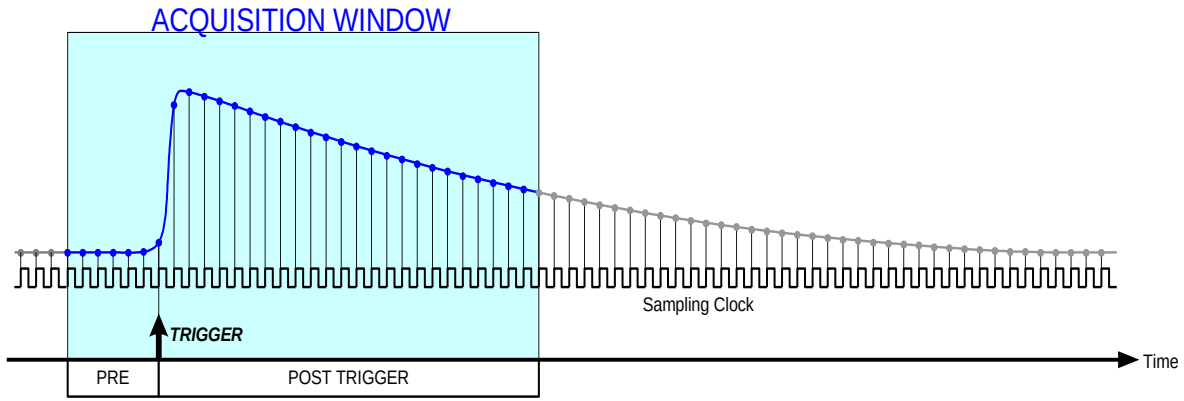
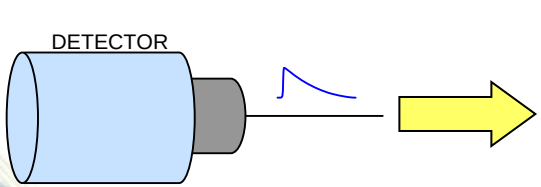
Why Digitizers 1

- Digitizers as oscilloscopes operate in waveform mode
  - Waveforms, time and voltage amplitude





Memory Buffer

TIME STAMP
S[0]
S[1]
S[2]
S[3]
⋮
S[n-1]

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Why Digitizers 2

… and something more

- Onboard analysis through dedicated firmware tools
- Designed for demanding data transfer
- Easy integration of acquisition and data analysis on personal computers with CAEN libraries and software demos

- Digitizers V.S. Analog acquisition systems
  - Real time and remote monitoring/setting
  - Adapt to detector improvements/modifications
  - Room for later offline analysis

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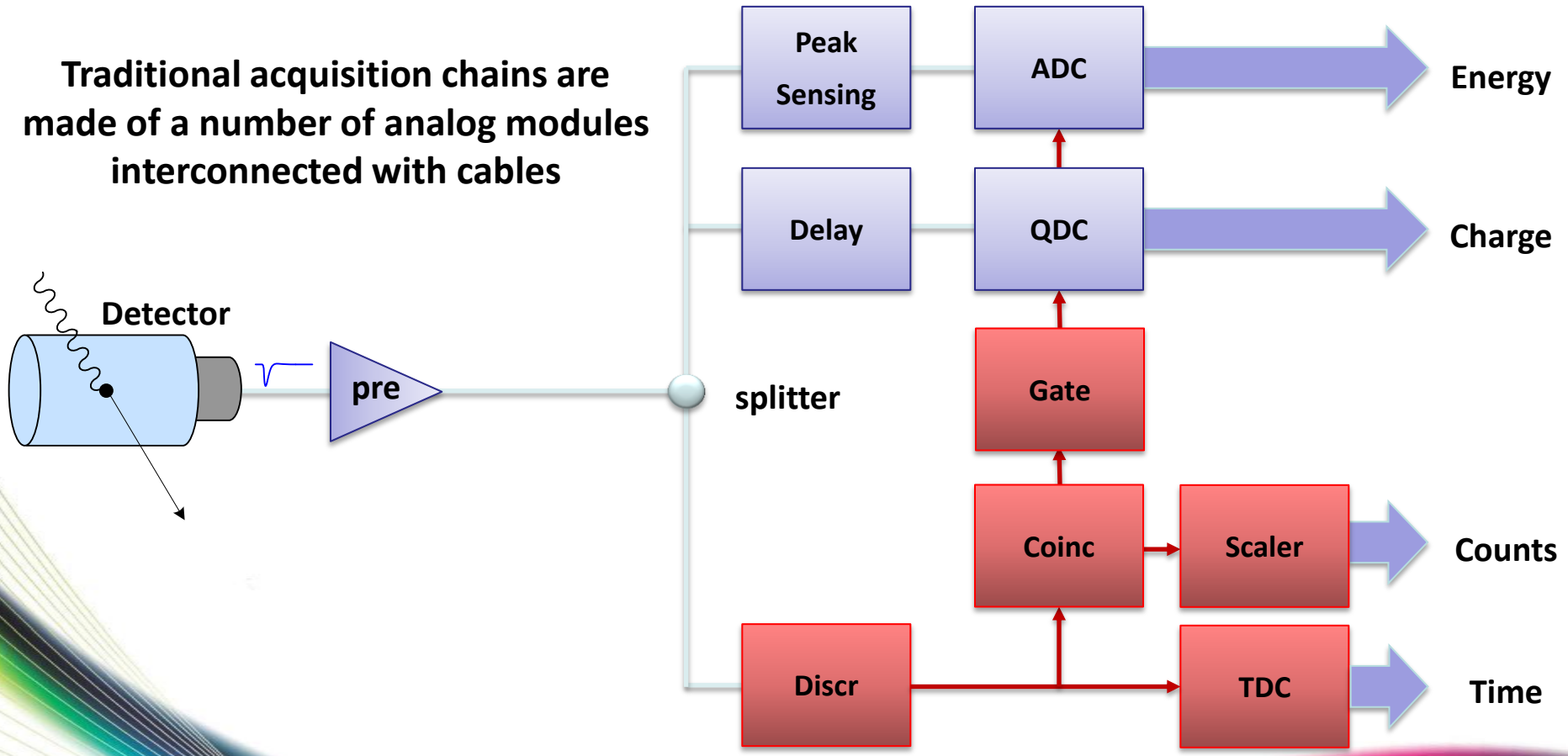
Traditional acquisition chain

A/D conversion at the end of the chain

Traditional acquisition chains are made of a number of analog modules interconnected with cables



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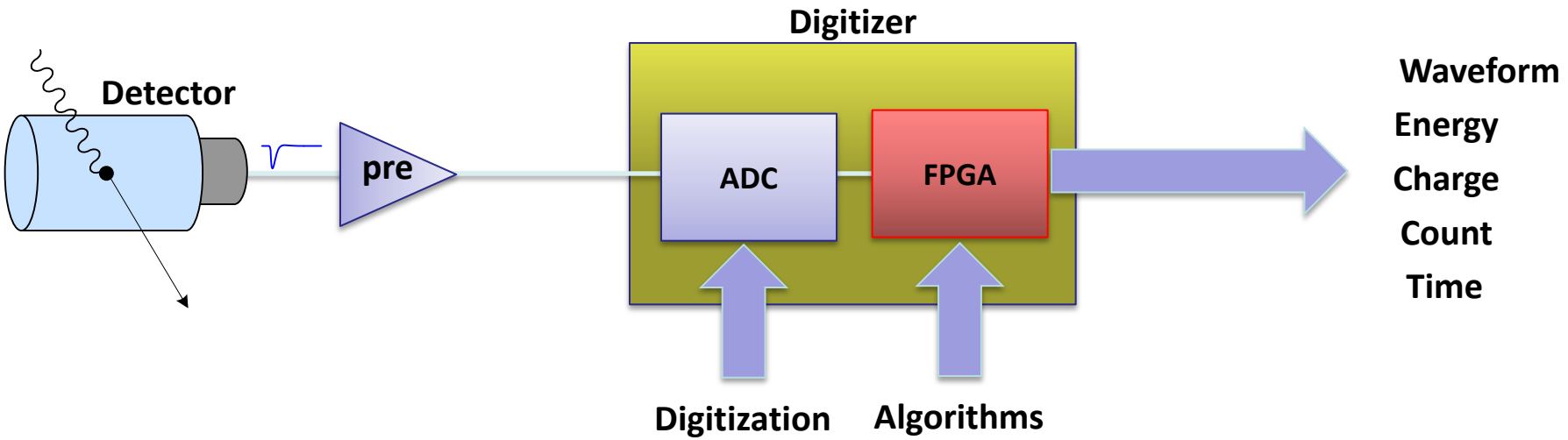
Fully digital acquisition chain



The aim of the Digital Pulse Processing is to make a "all in digital" version of analog modules such as Shaping Amplifiers, Discriminators, QDCs, Peak Sensing ADCs, TDCs, Scalers, Coincidence Units, etc.

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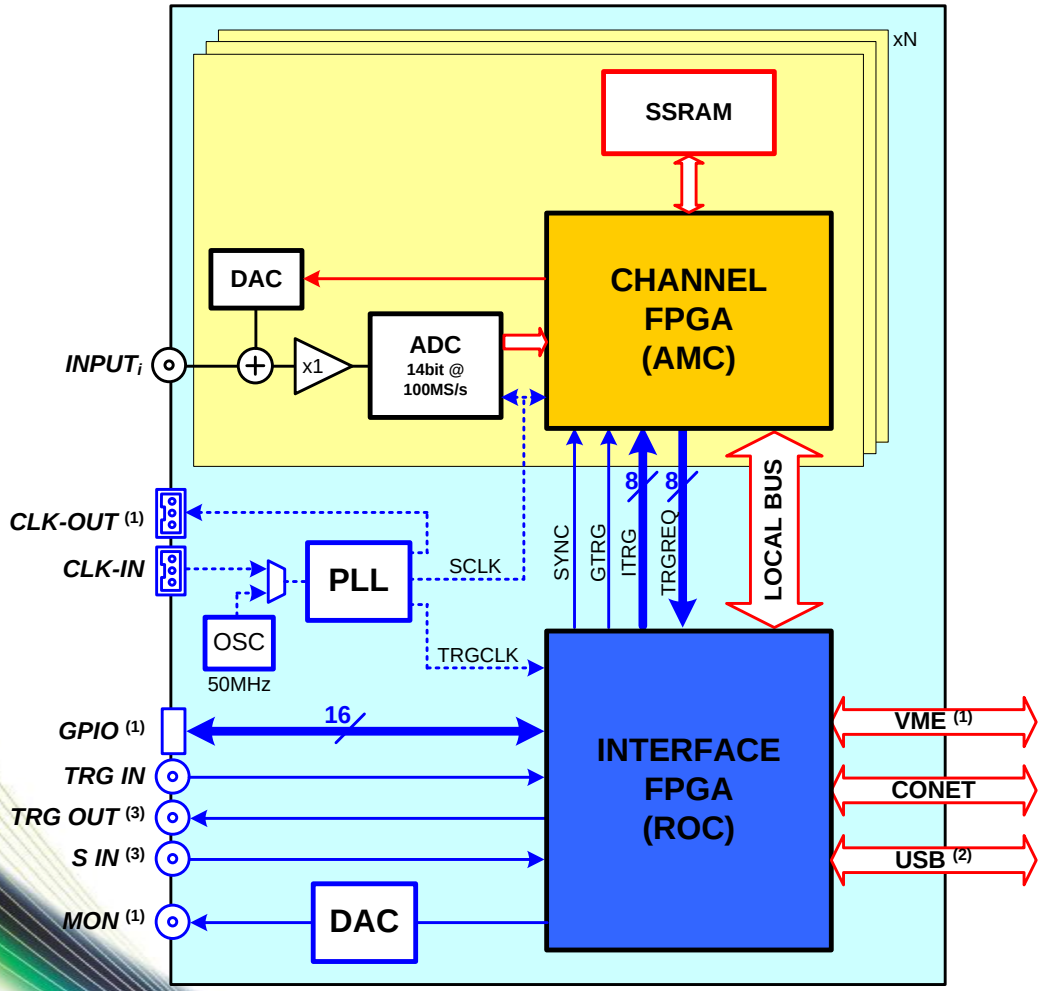
Architecture



(1) VME boards only
(2) Desktop/NIM boards only
(3) for Desktop/NIM baords, TRG-OUT = GPO, S-IN = GPI

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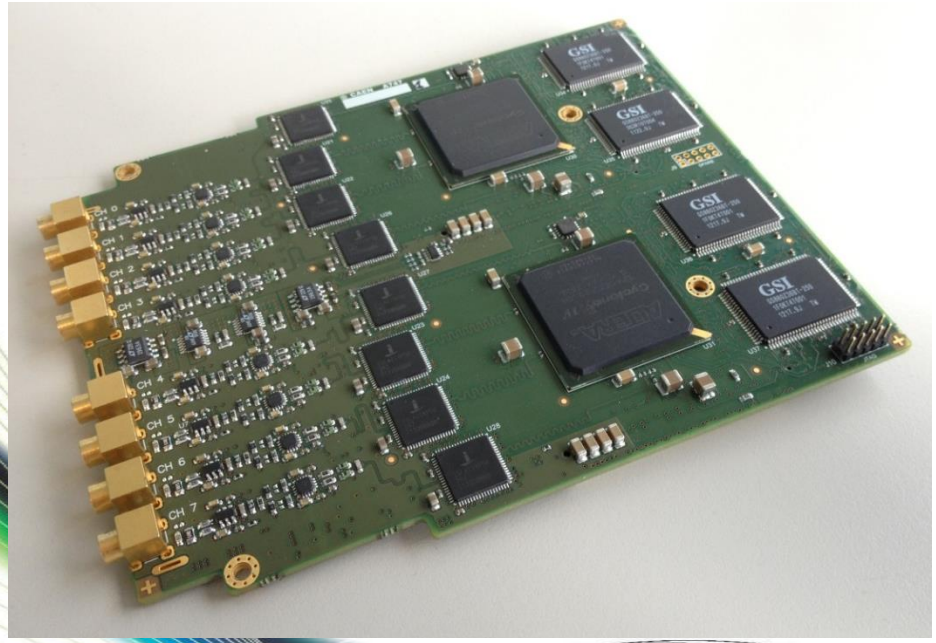
Fast ADC Technology

- **FADC**
  - Solutions for multiple experimental applications
  - Sampling frequency: from 62.5 MHz to 4 GHz
  - Resolutions: from 8 up to 14 bits



- **Latest waveform digitizer: x730**
  - Up to 16 channels in one board
  - 500 MS/s, 250 MHz analog bandwidth, with 14 bits dynamic
  - Double input dynamic range: 0.5 and 2 Vpp software set
  - Prototypes released and tested, firmwares under development
  - Available in VME, NIM and Desktop form factors

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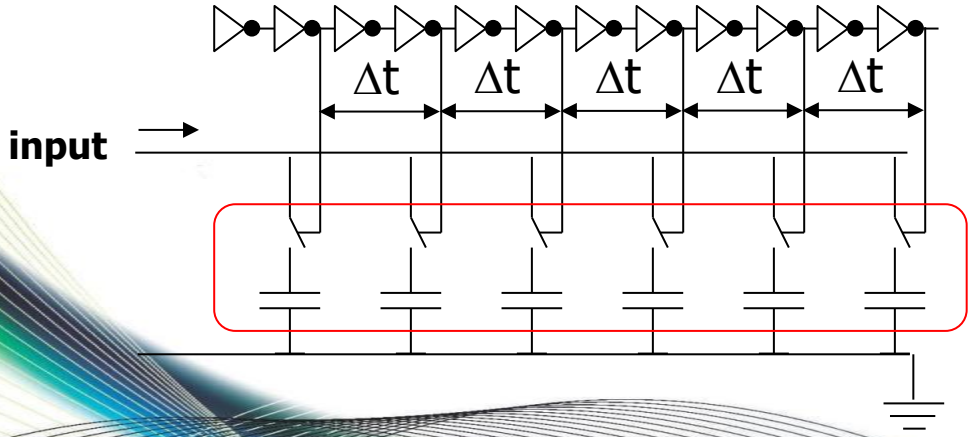
Switched Capacitor Arrays

- Digitizer family x742
  - Chip Domino Ring Sample, **DRS4**
  - Design of PSI, Switzerland: http://www.psi.ch/drs/
  - **32(+2 fast trigger)** channels on VME board

new

- Digitizer family x743
  - Chip Swift Analog Memory (LONG), **SAMLONG**
  - Design of CEA/IRFU - LAL Orsay, France
  - **16 channels** on VME board (with autotrigger)



- **Pros**
  - ✓ **High sampling frequency**
  - ✓ **Low channel cost**
- **Cons**
  - ✘ **Conversion times of ~ 100 µs**
  - ✘ **Calibration is needed**

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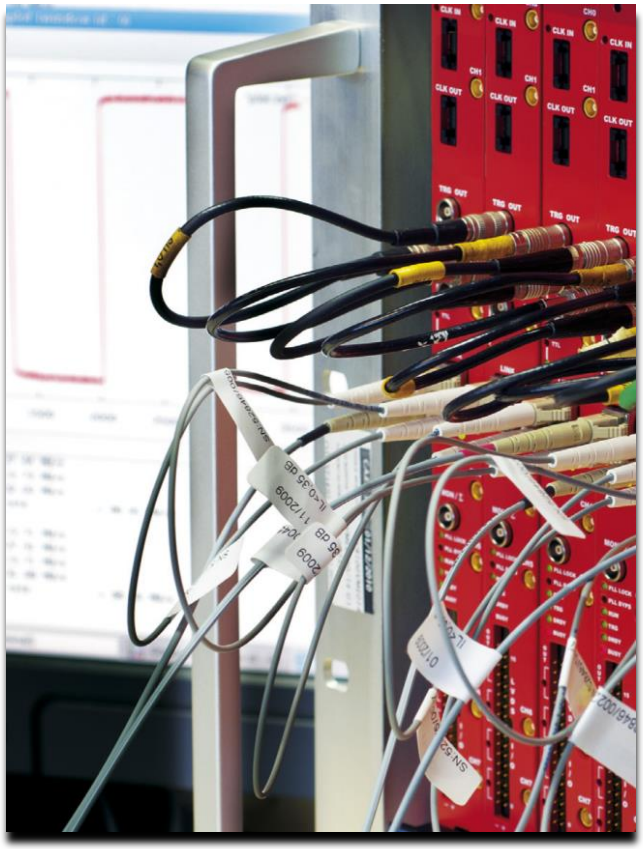
Multi-board Synchronization

- Basics
  - Clock phase-alligned
    - Clock input/output, programmable phase adjust
  - Same time reference
    - Time stamp reset, input/output connectors
  - Trigger propagation and/or correlation
    - Possible use of external logic units
  - Readout synchronization and event alignment
    - Input/output to propagate BUSY or VETO signals

- Software demo:
  - **SyncTest** source code, ANSI C
  - **Application Note** with simple examples (AN2086)

- **Some examples** follow



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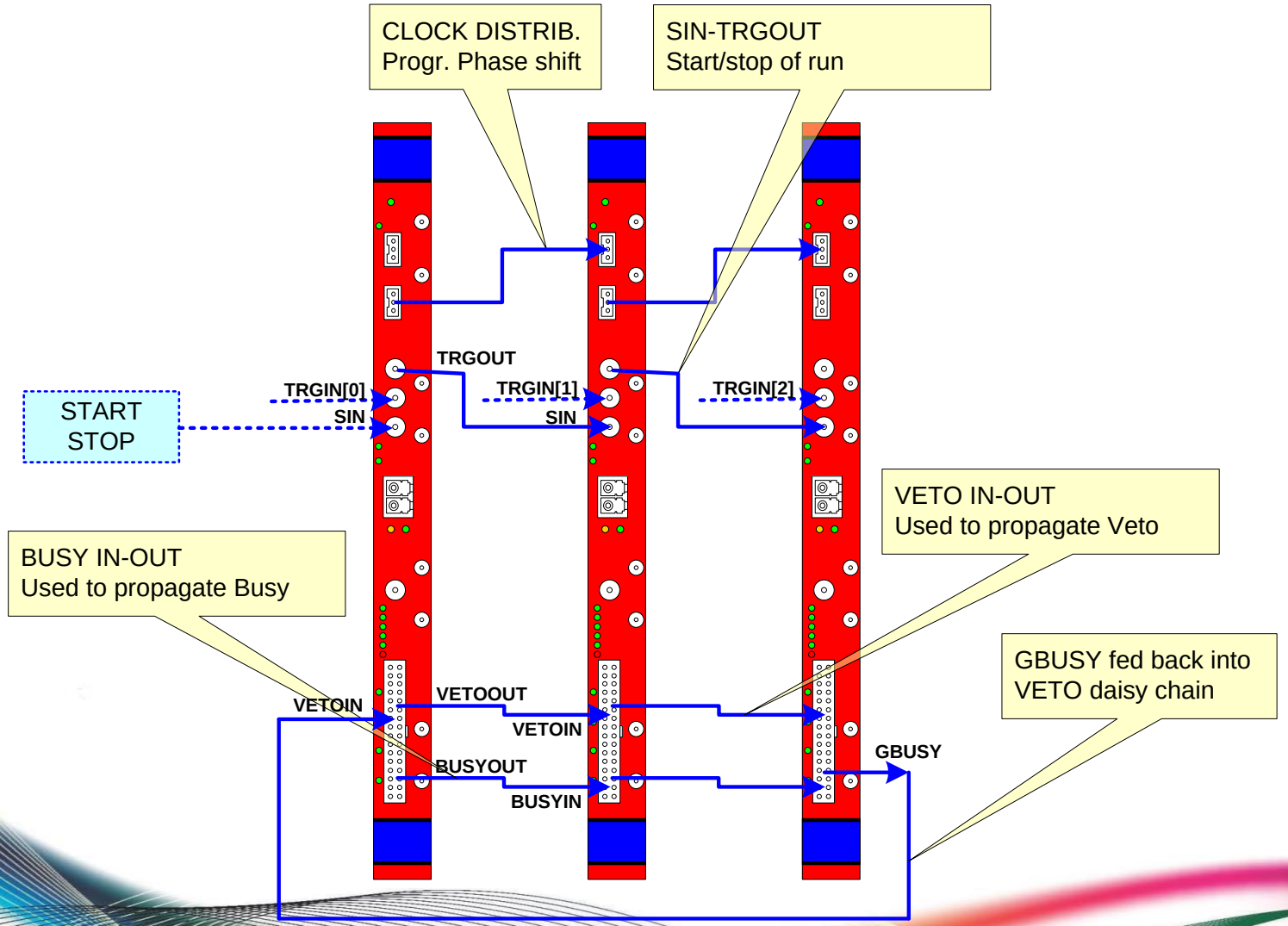
Multi-board Synchronization: example 1



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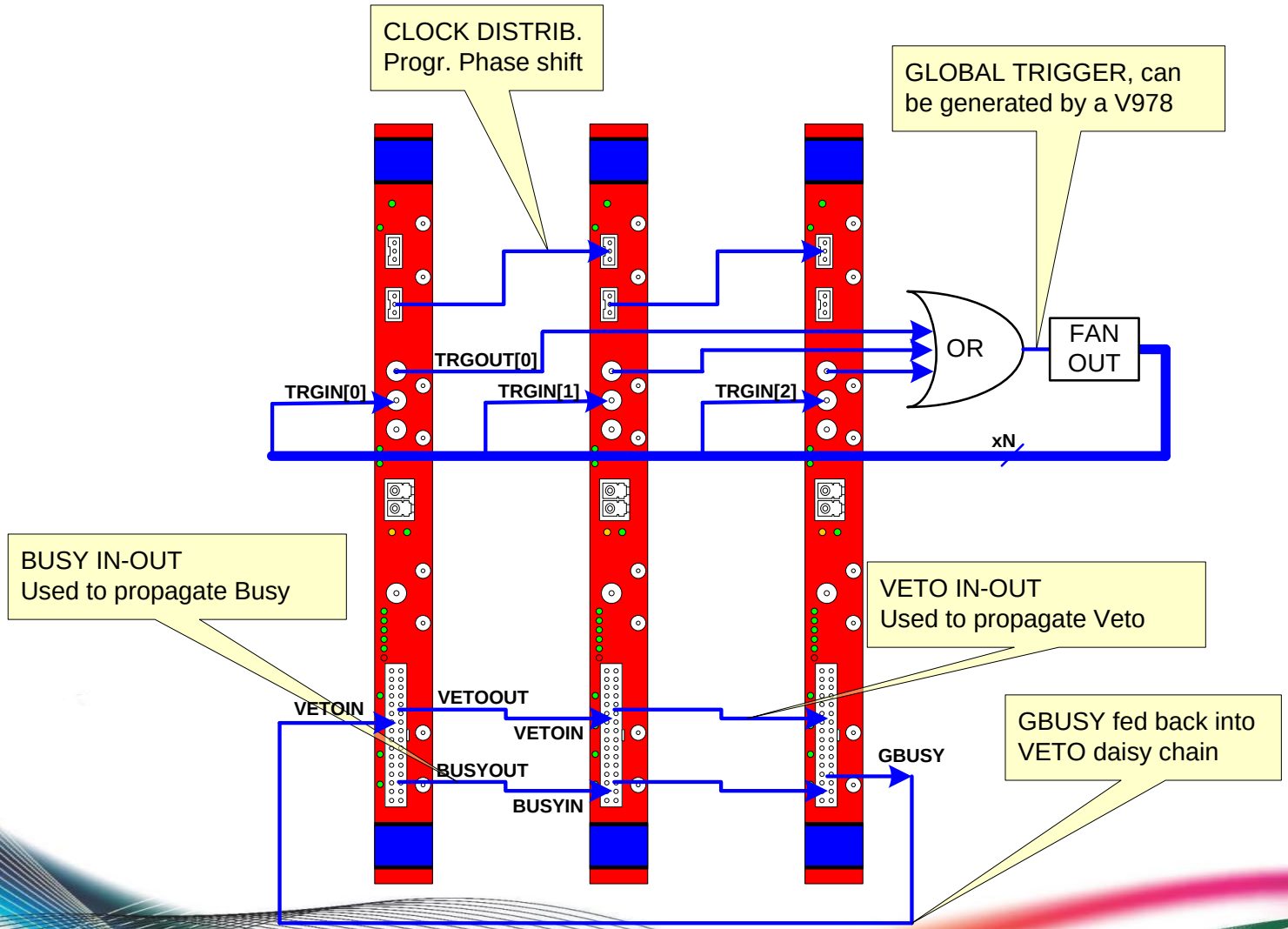
Multi-board Synchronization: example 2



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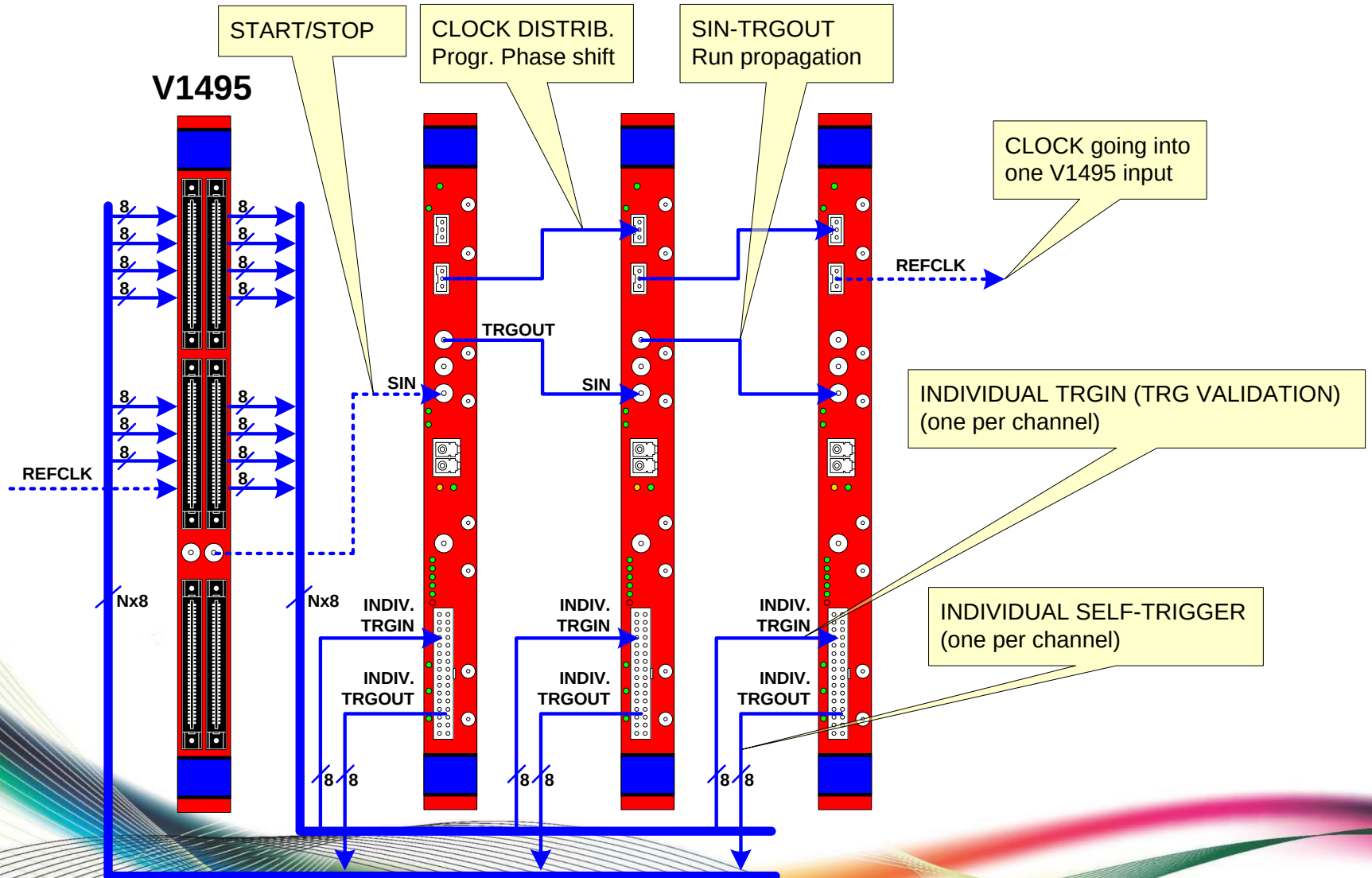
Multi-board Synchronization: example 3



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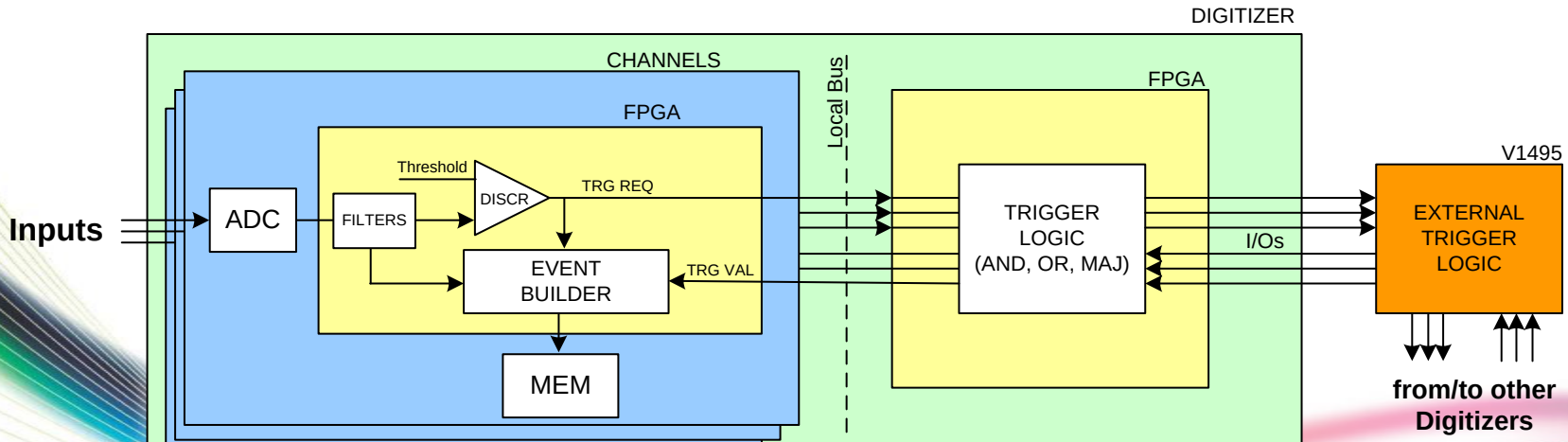
Coincident Event and Correlation

- Each channel has a digital discriminator that generates a **Trigger Request** (TR); the TRs of all channels are combined in the mother board (Mask + AND, OR, Majority) in order to generate a **Trigger Validation** (TV)
- Likewise, the TRs can be propagated to external logic units (such as the V1495), implementing a **multi board coincidence logic**
- Channels use TR to start event building and TV to accept/reject the event (coincidence/anti-coincidence)
- **Documentation**
  - All Waveform Digitizer are correlated with guides on the FPGA register
  - **Dedicated Guide GD2827 on event coincidence**



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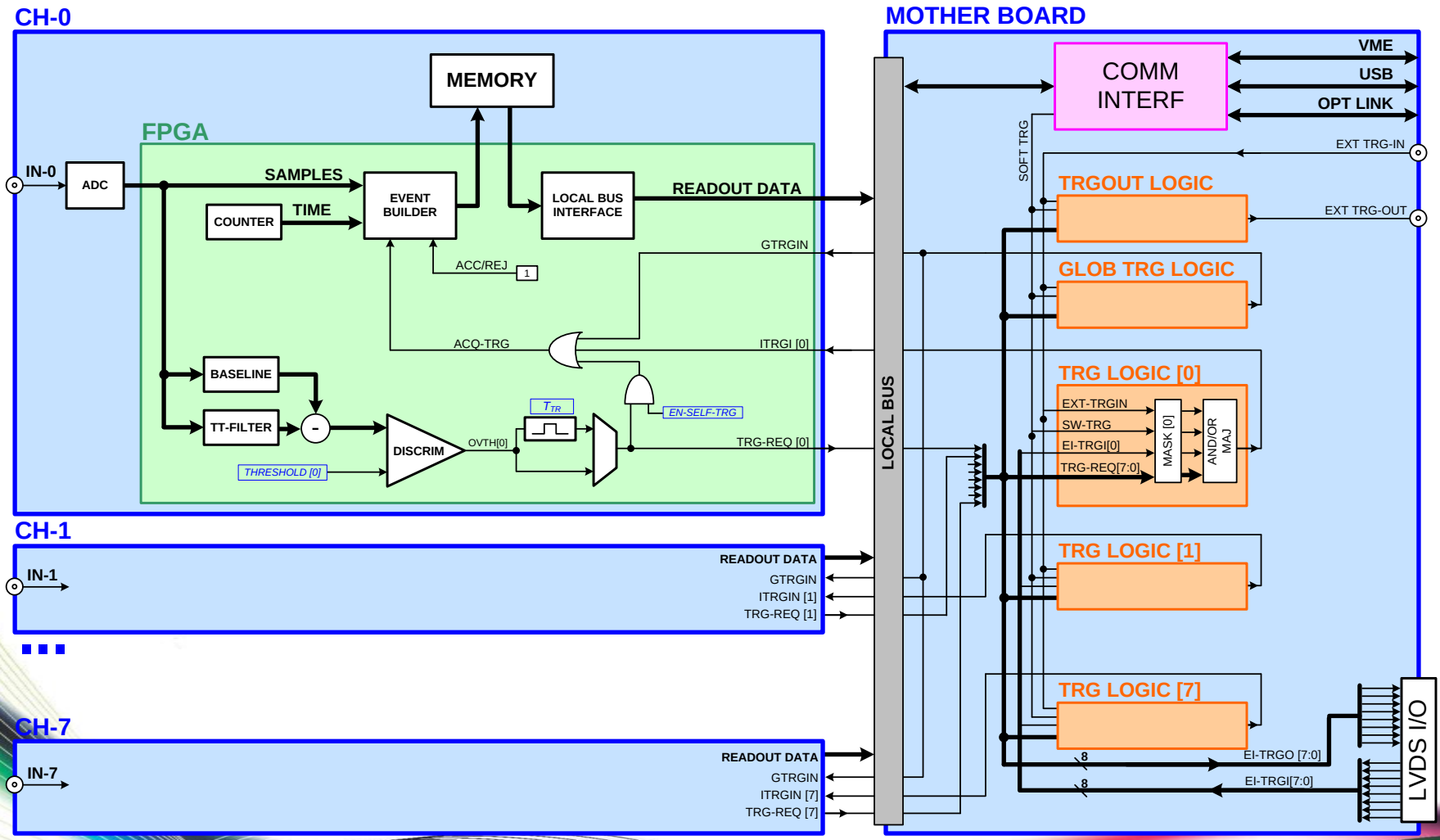
Trigger Logic (Normal Mode)



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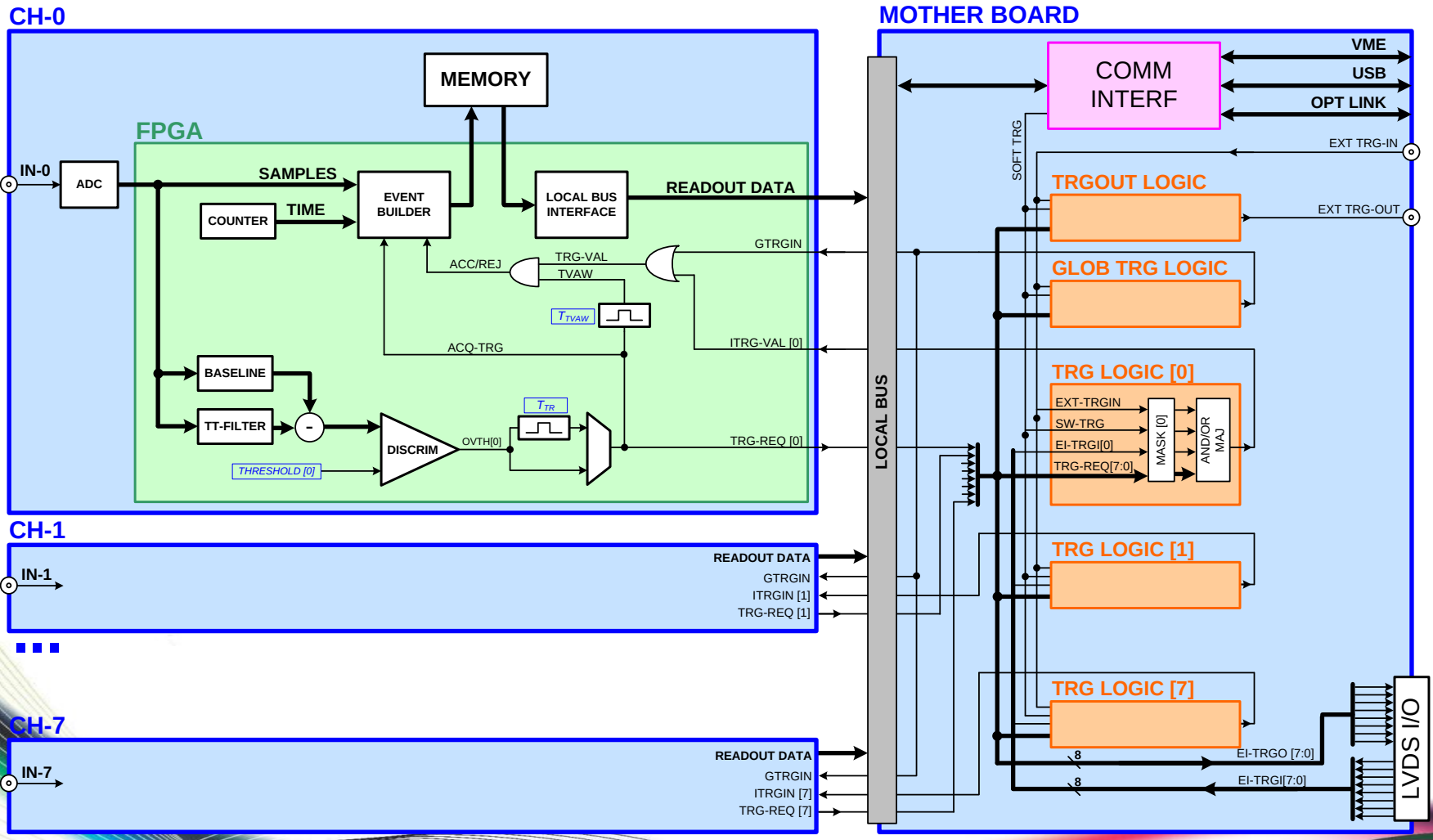
Trigger Logic (Coincidence Mode)



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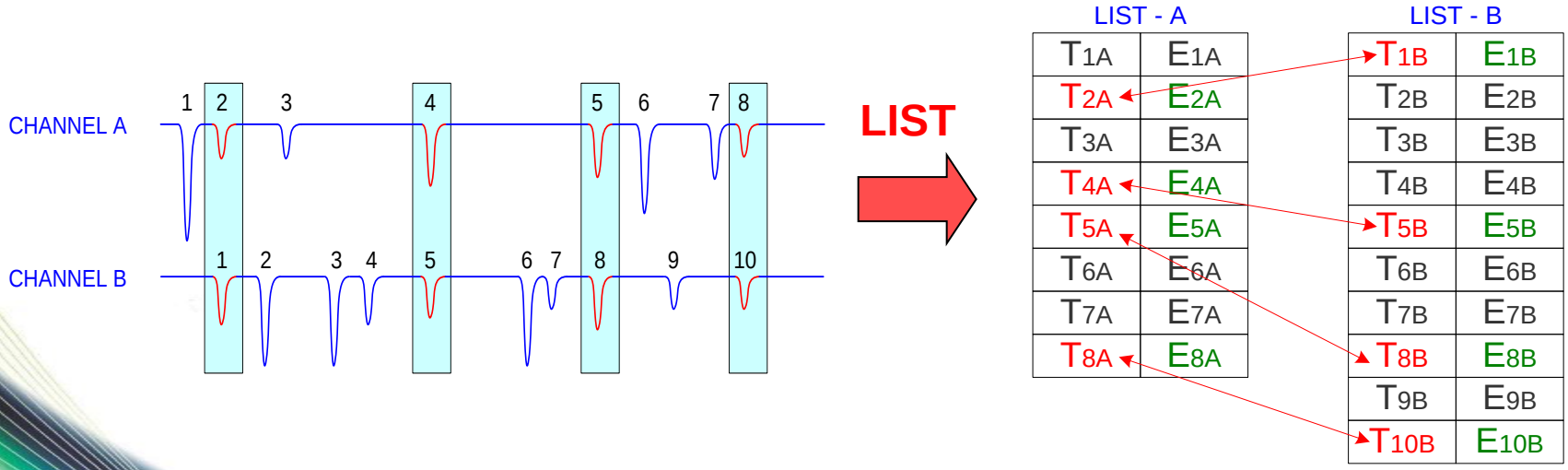
Coincident Event through Software

- Read all events as long as you have readout bandwidth (i.e. make data suppression as late as you can): **preserve the information**!
- In list mode, the bandwidth requirement is very little (e.g. 8 bytes per event). **Example: 8 channels at 100 KHz trigger rate gives 6.4 MB/s**
- In a modern multi-core computers, the readout process takes a small fraction of the CPU resources and the processing is extremely fast



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Firmware Tools

- **Standard Firmware**
  - Trigger on Leading Threshold
  - Waveforms, Time stamps

- **Digital Pulse Processing (DPP) Firmware**
  - Zero Length Encoding **(ZLE)** or Zero Suppression, to extract signal interest regions
  - Pulse Height Analysis **(PHA)** for spectroscopic applications
  - Charge Integration **(CI)**, to measure particle released energy
  - Pulse Shape Discrimination **(PSD),** to measure particle released energy and identify through the ionization density

  - **On-board and real time analysis**
  - Supporting multiboard synchronization and event correlation

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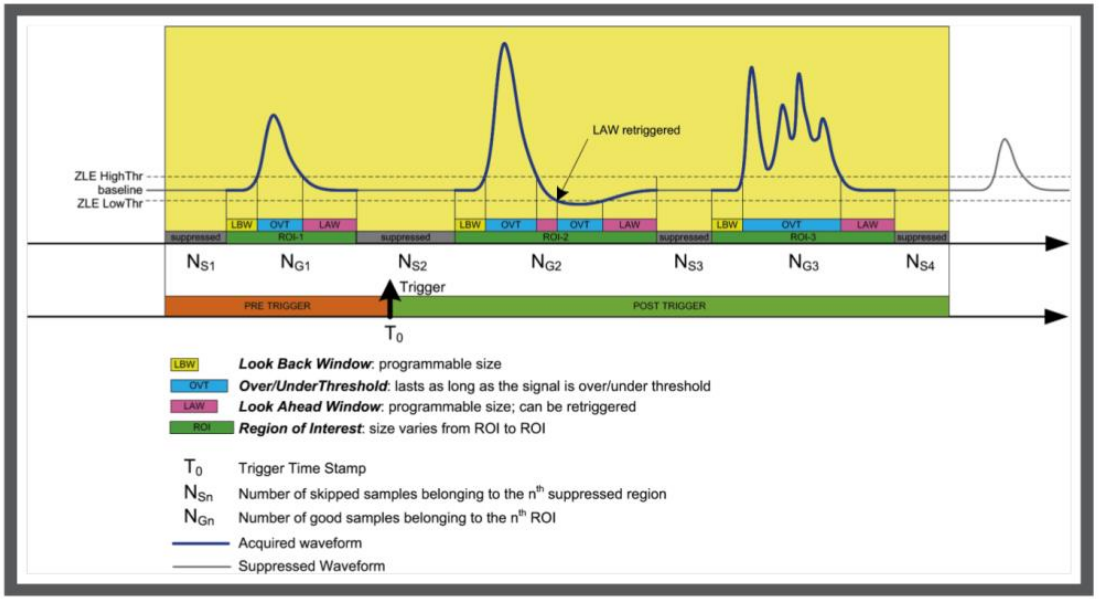
DPP-ZLEplus Firmware

- Enhanced Zero Suppression of input signals
- Implemented in the **751 digitizer** family (10 bit @ 1 GSps)
- Input signal baseline calculation
- Acquisition window generated by external trigger
- Upper and Lower Thresholds referred to the baseline or to absolute values
- Dead-timeless acquisition (no conversion time)
- Provides also timing information (trigger time stamps)



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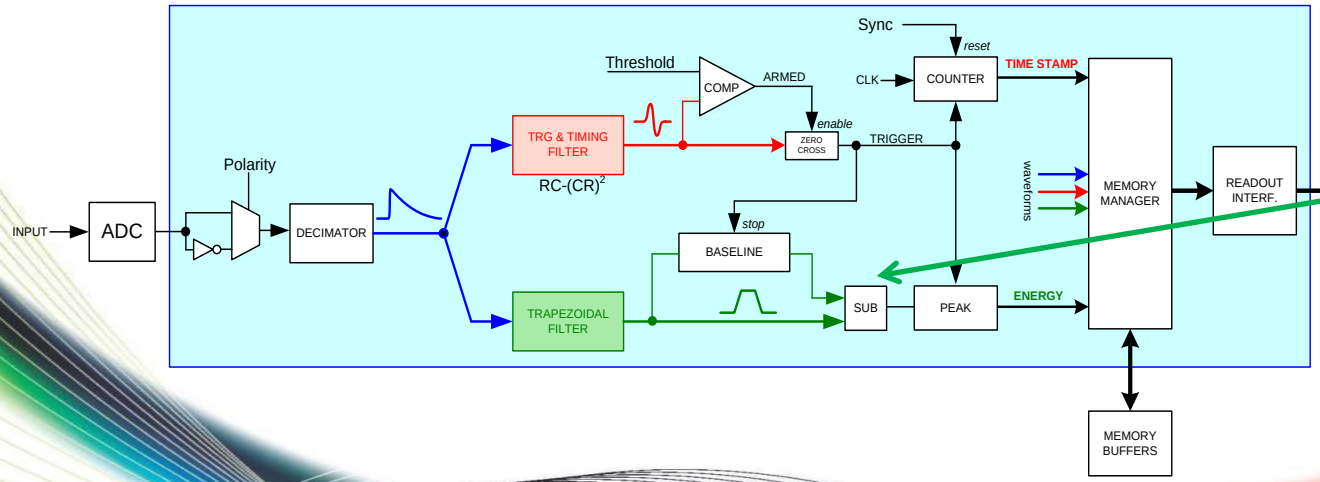
DPP-PHA Firmware

- Digital solution equivalent to shaping amplifier + peak sensing ADC (Multi-Channel Analyzer)
- Implemented in the **724 digitizer** family **and DT5780** (14 bit @ 100 MSps)
- The digitizer is directly connected to the charge sensitive preamplifier
- Programmable input offset, trigger and energy filter parameters
- Better correction of pile-up and ballistic deficit
- Higher counting rate (live time)
- Provides also timing information (pulse time stamps and/or rise/fall time)
- Free downloadable Trial version



- Programmable pole-zero cancellation
- The baseline restoration
- Programmable shaping time and peak sampling

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Multichannel Analyzer DT5780

- Suited for high resolution X-ray and Gamma-ray Spectroscopy
- **16K Digital MCA**
- **Two channels,** in the form factor of the Desktop Digitizers
  - Two BNC inputs with four SW selectable dynamic ranges
  - Two SHV high voltage supplies (± 6kV, 1mA) with individual inhibit
  - Two DB9 low voltage supplies for the pre-amplifiers (±12V, ±24V),
- Readout from USB (30MB/s) and Optical Link (80MB/s)
- **Free software**
  - DPP-PHA Control Software
  - Analysis software **MC² Analyzer** coming soon

Front View

Back View

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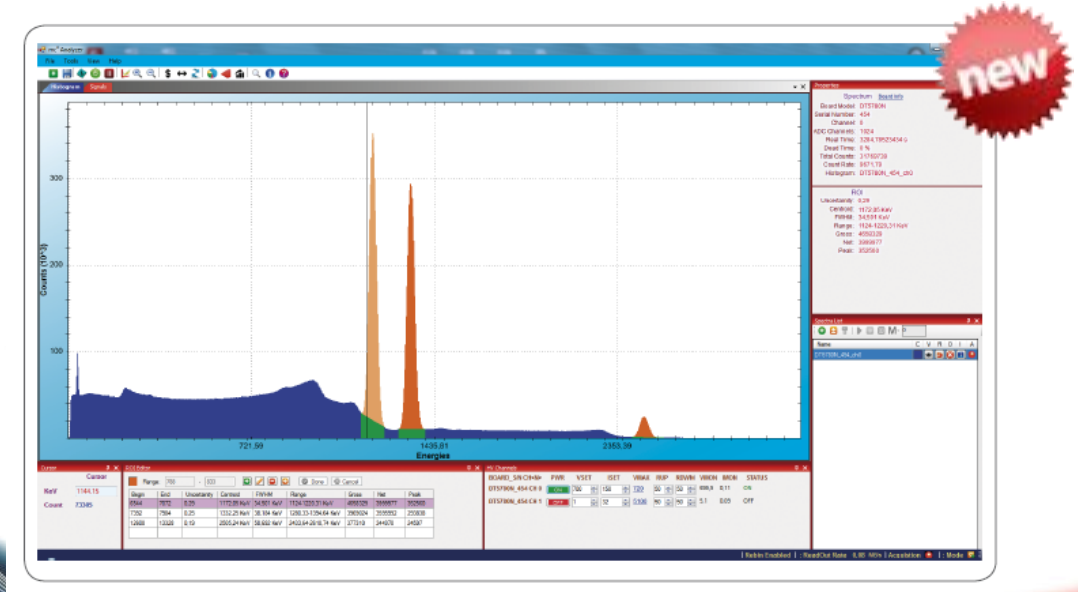
MC² Analyzer (MC²A)

Graphical software tool for digitizers running DPP-PHA firmware

Overview:

- Designed for digitizers running DPP-PHA like 724 family or the Dual Digital MCA DT5780.
- Complete simultaneous control of different boards
- Full setting of all the relevant DPP-PHA parameters and power supplies for DT5780
- Advanced mathematical analysis on collected spectra (peak search, background subtraction, peak fitting, etc.)
- Provides Energy - Time Stamp lists and histograms in ASCII and ANSI N42.42 format



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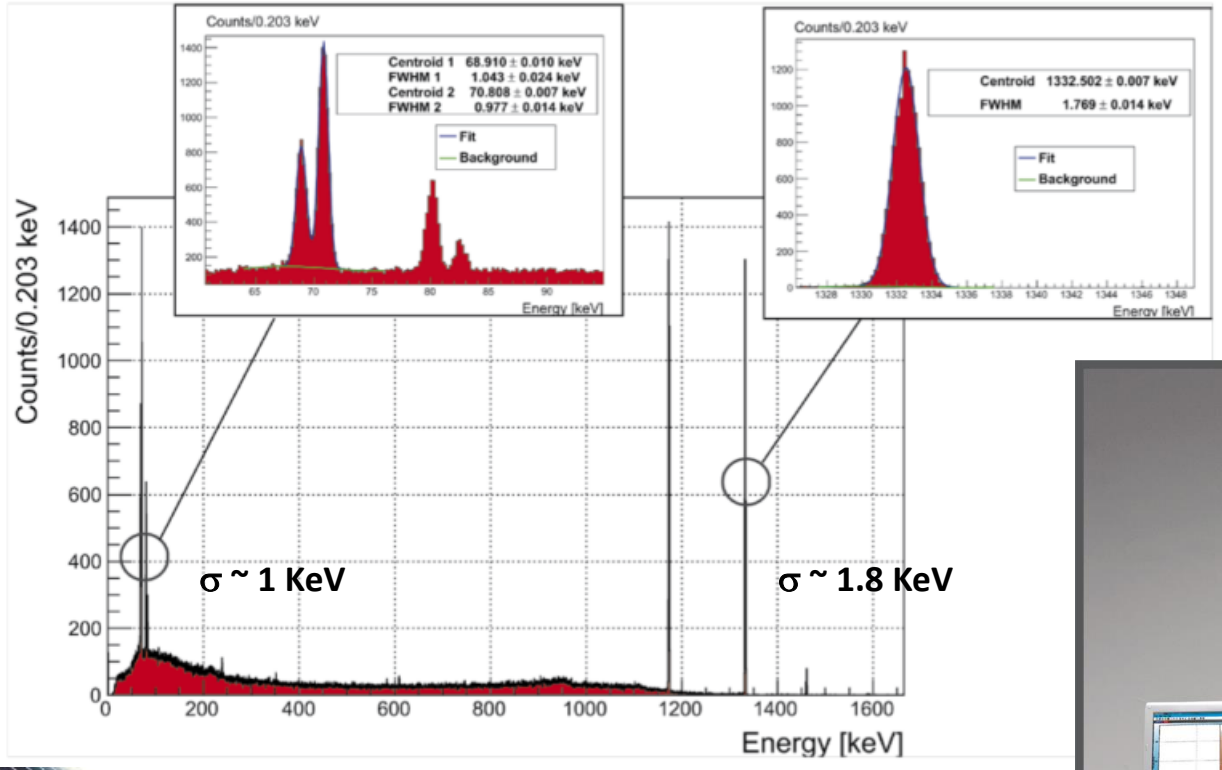
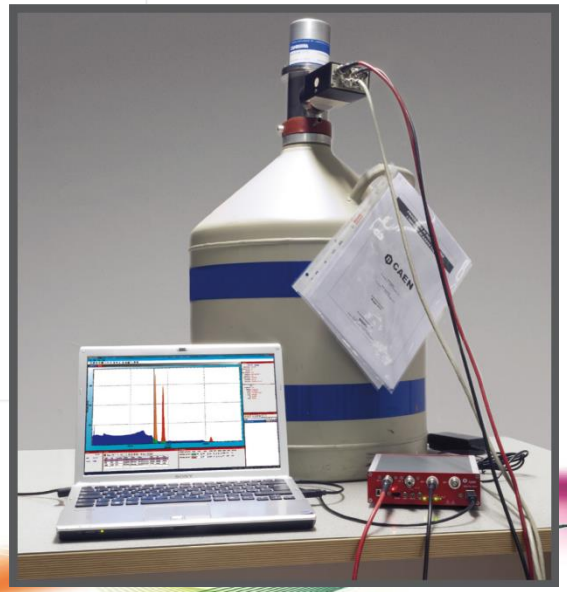
Test Results with HPGe Detector

- Tests with CANBERRA Standard Coaxial P-Type detector
  - Application Note will be released





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Application: Medical Imaging (ProSPECTus)

Single Photon Emission Computed Tomography: SPECT Localization of a gamma-ray source through the reconstruction of interaction sequences in position and energy sensitive strip detectors.

- 32 channel orthogonal strip HPGe planar detector
- Independent MCAs (with DPP-PHA) and waveform recorders
- Trigger Logic: a fired strip forces trigger in the neighbour strips (although these might be under threshold). Channel trigger propagation from any to any, event across boards. Implemented in a V1495 FPGA Trigger Unit.
- Readout from a single PC (A2818 PCI Optical link + V2718 VME master)
- The DAQ reads Pulse Height, Time Stamp and a portion of the waveform (rising edge) for further pulse shape analysis (off-line) to improve the intrinsic spatial resolution

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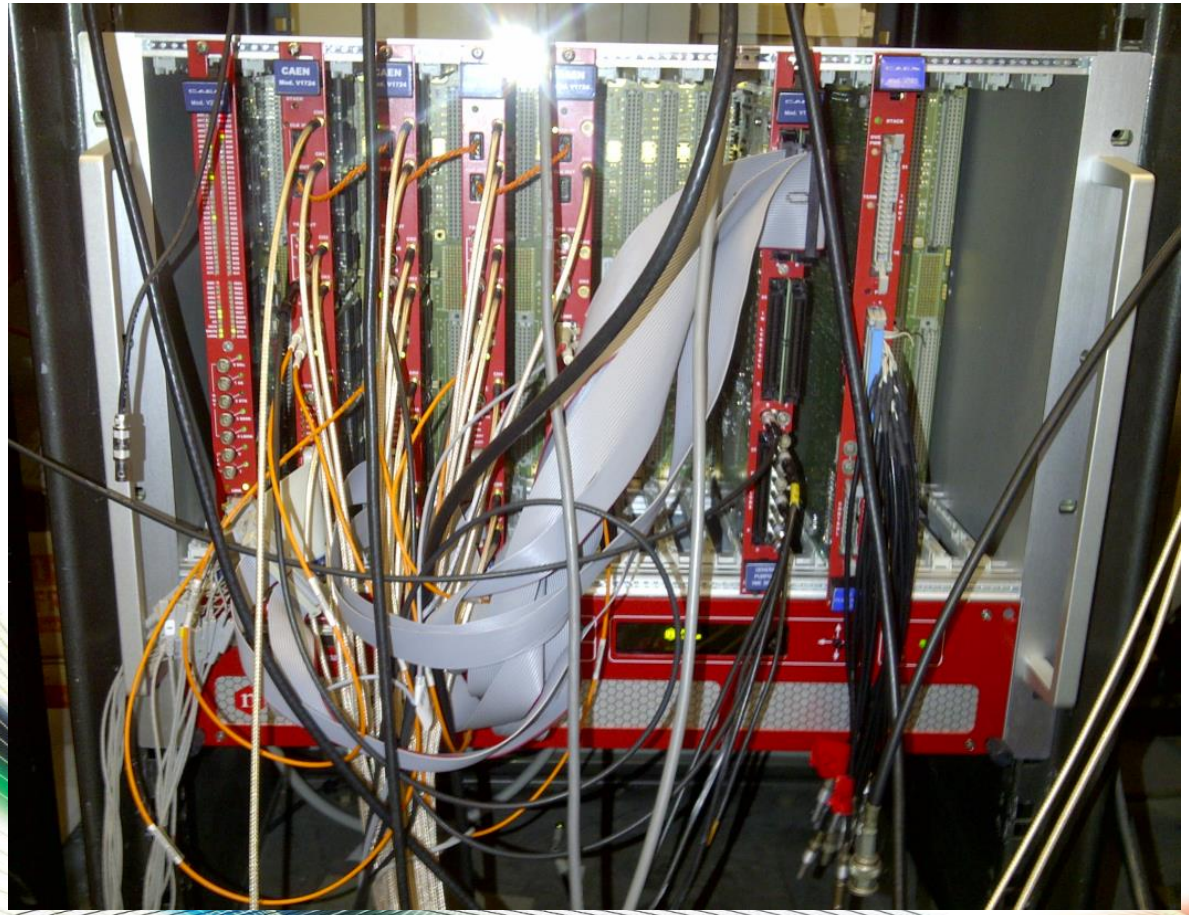
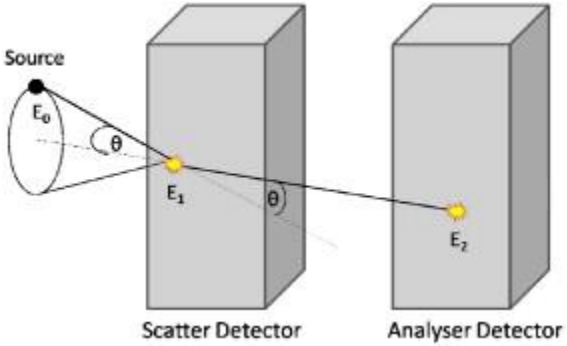
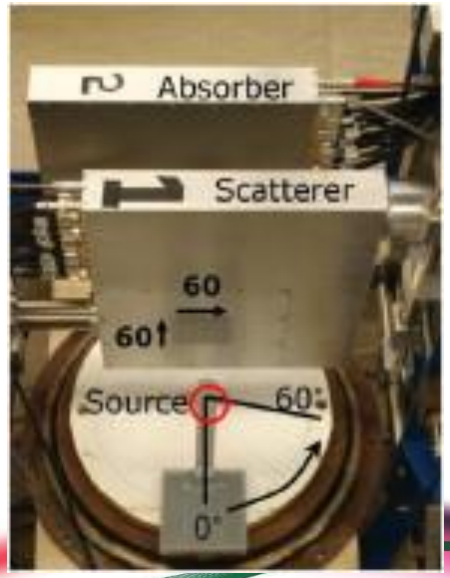
Application: Medical Imaging (ProSPECTus)

SETUP: VME crate with 4 V1724 + DPP-PHA; VME readout through V2718 + A2818 PCI Optical Link; V1495 FPGA Trigger Unit with custom firmware







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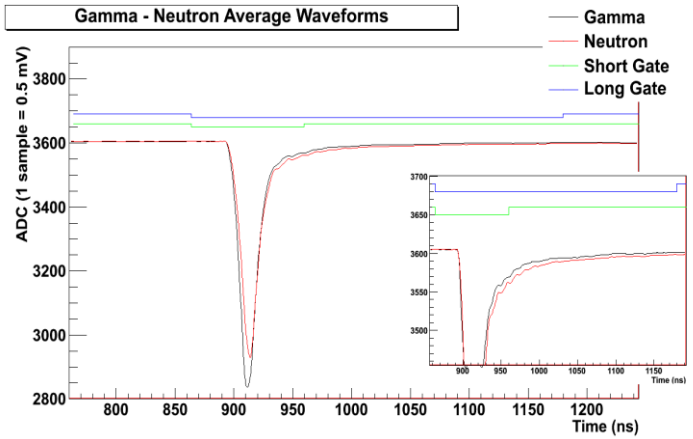
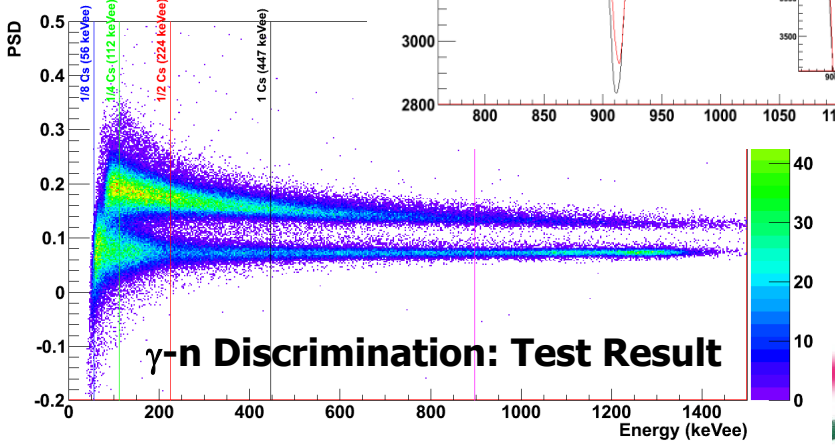
DPP-CI/PSD

- Digital implementation of the QDC + discriminator and gate generator
- **CI: single gate; PSD: dual gate** (fast and slow components)
- Pulse Shape Discrimination for n-γ separation: **$PSD = (Q_{LONG} - Q_{SHORT})/Q_{LONG}$**
- DPP-CI is implemented in the **720 digitizer** family
- DPP-PSD is implemented in the **720, 730 & 751 digitizer** families
- Will be implemented on the new **x730 family**
- Dead-timeless acquisition (no conversion time)



Application Note AN2506

Detector: BC501A 5x2 inches,
PMT: Hamamatsu R1250



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Application: Homeland Security

- **Three projects**
  - **SLIMCHECK:** mobile inspection system based of the correlation between n-γ spectra in multiple detectors (and PSD)
  - **MODES** and **Plutonium Hunter**: portable systems with single detector and online analysis based on PSD
- DPP-PSD with fast scintillators
  - Liquid scintillators: NE-213 and EJ-309
  - ARKTIS Pressurized Xe + 4He tubes (scintillation in Xe gas)
- Readout of different gamma-ray and neutron detectors for the **identification of illegal radioactive materials** inside volumes tagged as "suspect" by conventional surveys as X-ray scans
- The DAQ reads Charges and Time Stamp (List Mode). In some cases, waveform can also be read to improve PSD by single photon counting

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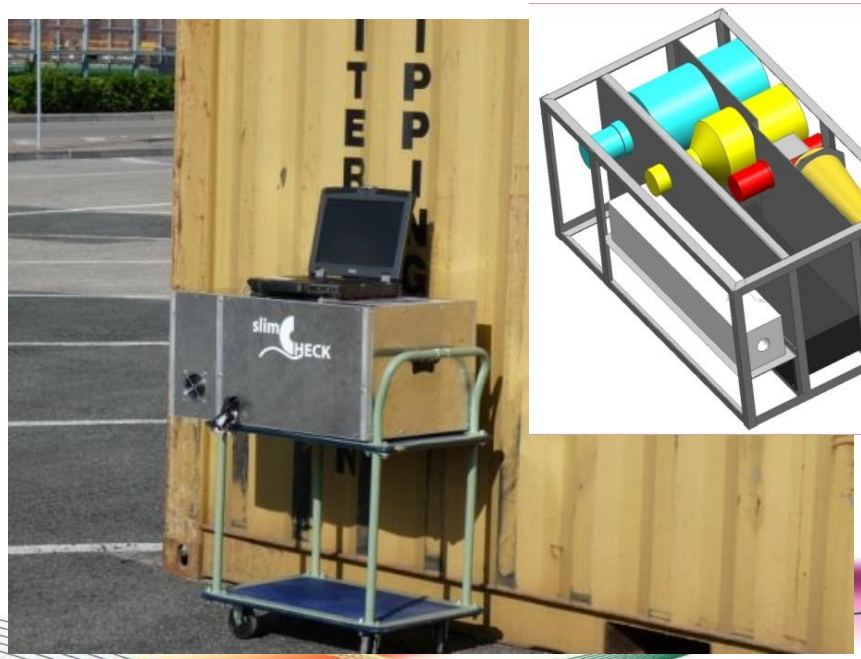
Application: Homeland Security

- **Plutonium Hunter**
  - one DT5790: two HV channels and two 12 bit 250 MS/s acquisition channels
- **MODES-SNM (on going)**:
  - three DT5730; three Desktop High Voltage modules
- **SMANDRA**
  - VME crate 4 slots
  - One V1720 + DPP-PSD
  - One V6533 6 ch. High Voltage Power Supply
  - One VME to USB bridge V1718
- And others...



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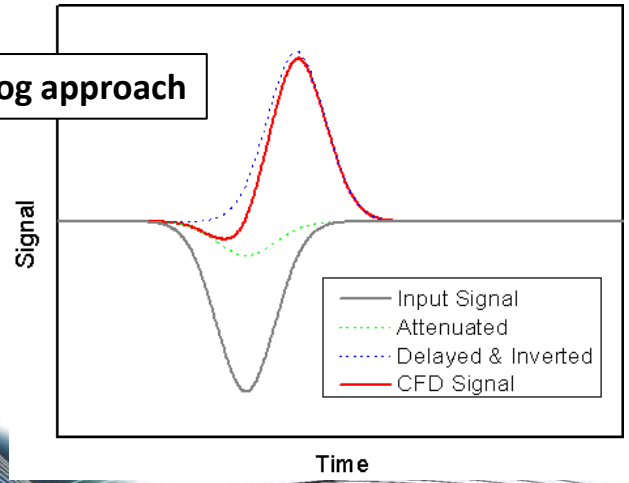
Time Measurements

- Interpolation of waveforms can provide very accurate time measurements
  - **But very high data bandwidth is required**
- Interest in developing **dedicated firmware**
  - Providing zero crossing and two points to interpolate
  - Interpolation improves time stamp resolution of a factor the order of 100
- DPP firmware provides baseline, energy, time stamp and waveform with variable record lenght

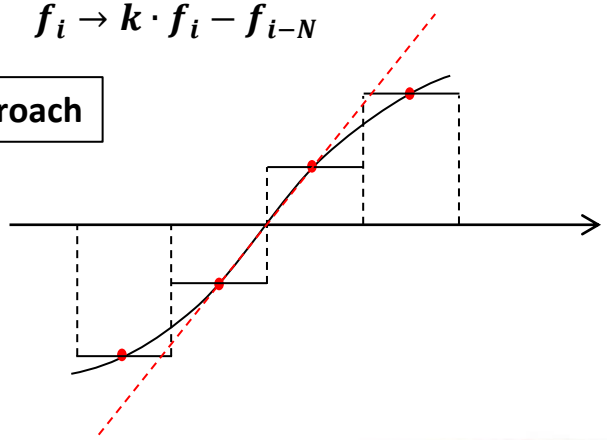
$$f(x) \rightarrow k \cdot f(x) - f(x - \Delta t)$$

Analog approach



$$f_i \rightarrow k \cdot f_i - f_{i-N}$$

Digital approach



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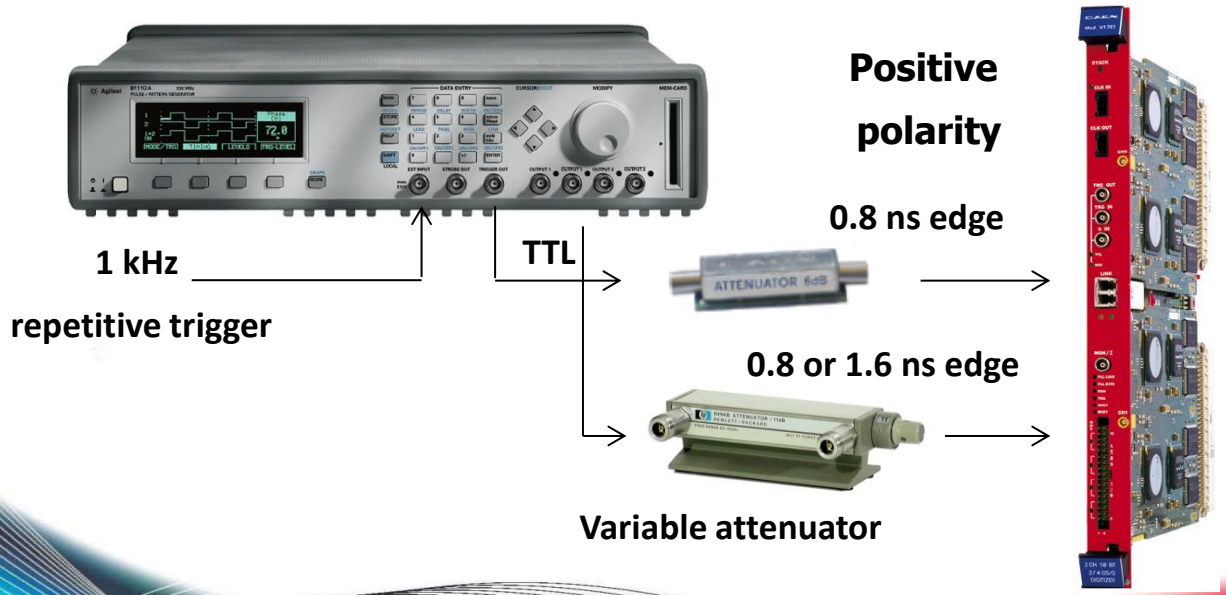
Hardware Setup

- Pattern Generator Agilent 81110A:
  - signals with **0.8 and 1.6 ns** rising and falling edges
- Two signals used
  - One used as start was kept unchanged
  - One used as stop was delayed and/or attenuated
  - Digital CFD with 100% fraction and delay equal to the pulse width to have maximum signal slope at the zero crossing



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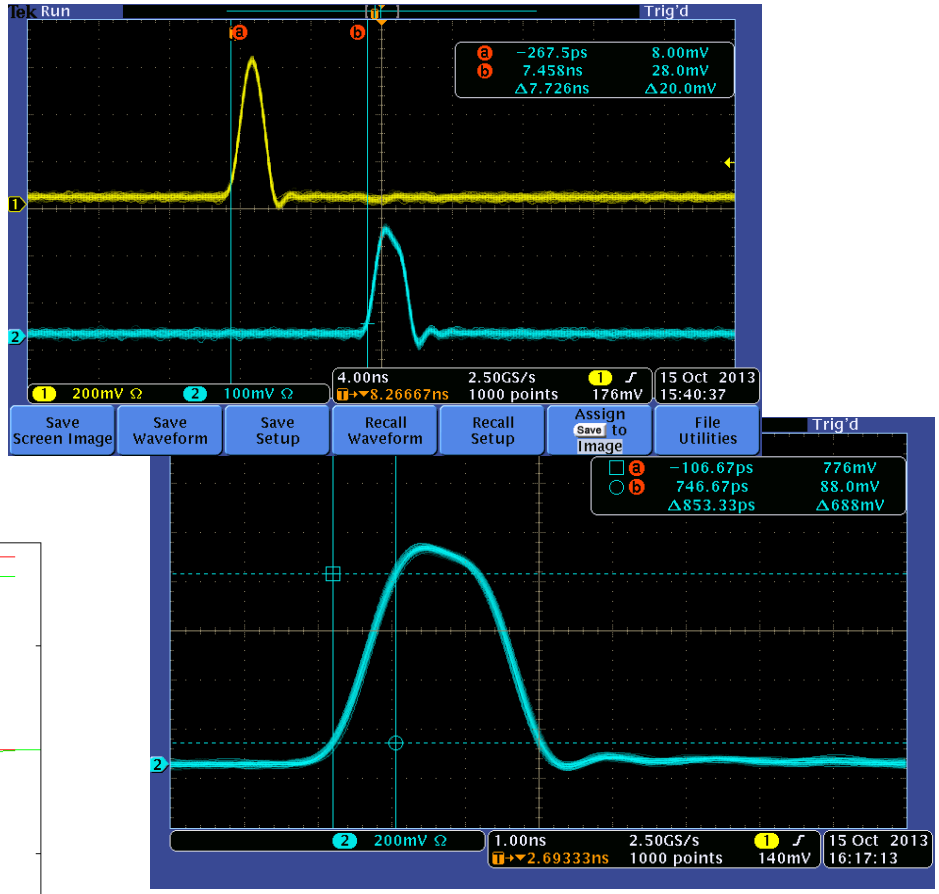
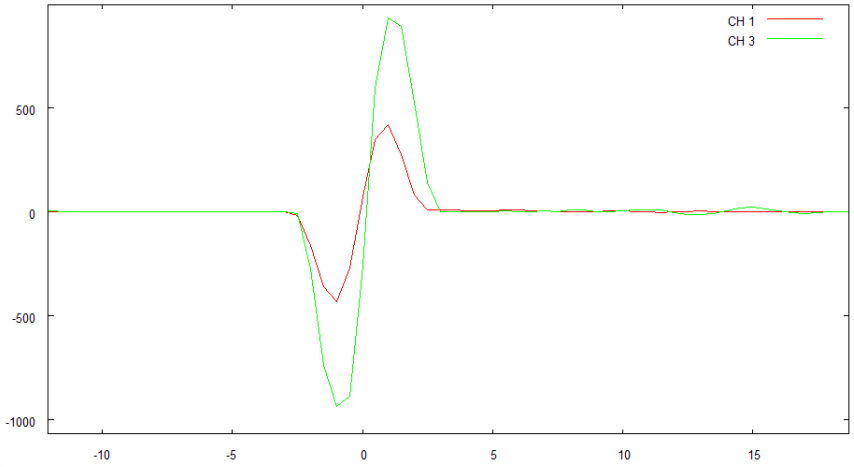
Generated Signals

- Start signal
  - 0.8 ns rise and fall time
  - amplitude +600 mV
- Stop signal
  - 0.8 ns/1.6 ns rise and fall time
  - amplitude +950 mV
  - pulse width set 2 ns
- CFD parameter
  - CFD fraction 100% , delay ~ 2 ns



Signal with 0.8 ns edge



CFD with 0.8 ns edge signals using DT5751

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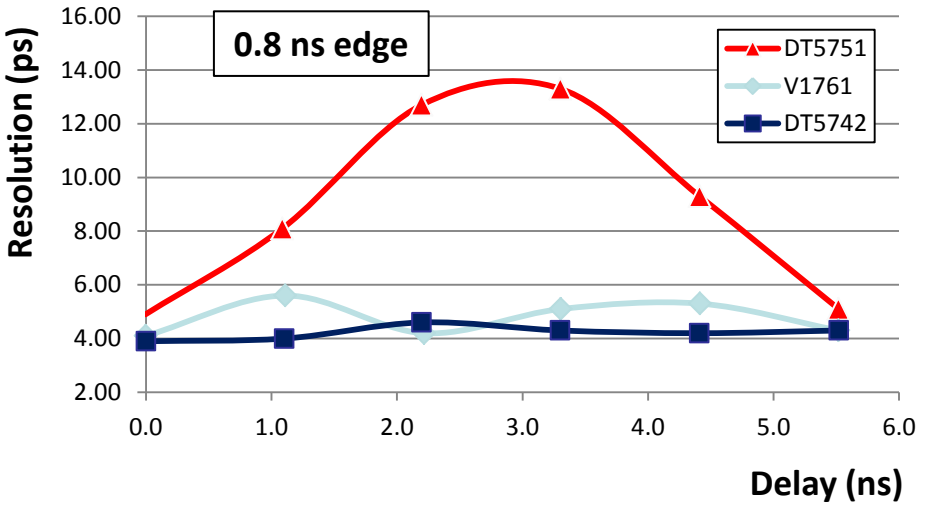
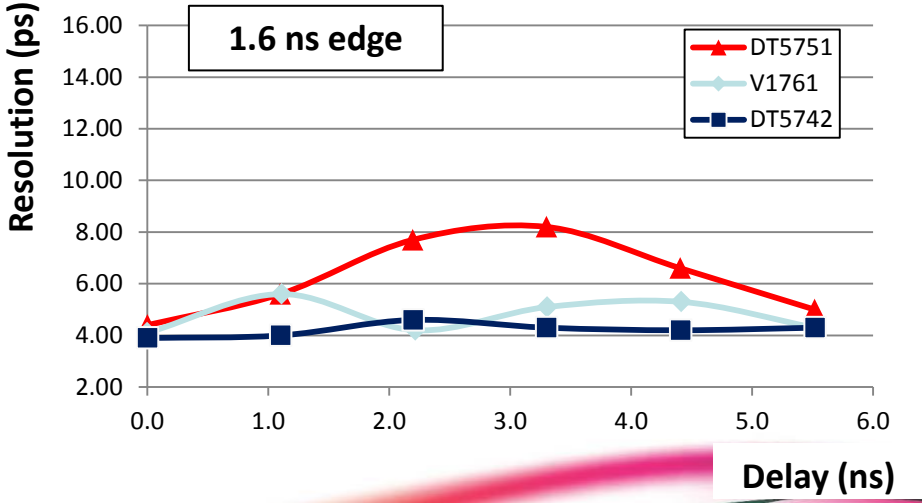
Dependency on the Delay: Results

- Digitizer used
  - V1761: sampling at 4 GHz, bandwidth 1 GHz
  - DT5751: sampling at 2 GHz, bandwidth 0.5 GHz
  - DT5742: sampling at 5 GHz, bandwidth 0.5 Ghz
- **Delay added in 1.1 ns steps**
- Interpolation of two points to find the zero crossing
- Ultimate performances in time measurement provide resolutions of the order of 4 ps
  - In this particular test V1761 and DT5742 have comparable resolutions
  - DT5751 provided degraded resolution because of the fast transition of the signal





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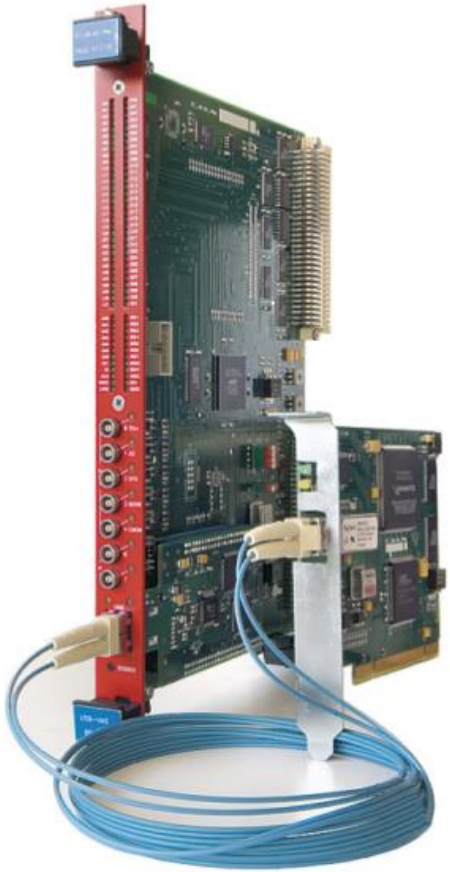
Readout and Communication: CONET

- **Readout is a fundamental aspect!**
- **Chainable Optical NETwork**
- Available for all waveform digitizers
- Benefits of fiber optics: long distance (>500m); no ground loop.
- **Daisy chain** (up to 8 boards) or point to point connection
- VME Bridge available, A2718
- **Controllers**:
  - A2818 PCI (1 link)
  - A3818 PCIe (1, 2 or 4 links)
- Up to 80MB/s per link
  - Real test with 4 link A3818 in a Linux Quad-core PC: ~320 MB/s total aggregate bandwidth
- **Pros**
  - **High flexibility** and integration in commercial computers
  - CONET can be parallelized thus giving higher total bandwidth compared to data transfer of the VME bus in 2eSST



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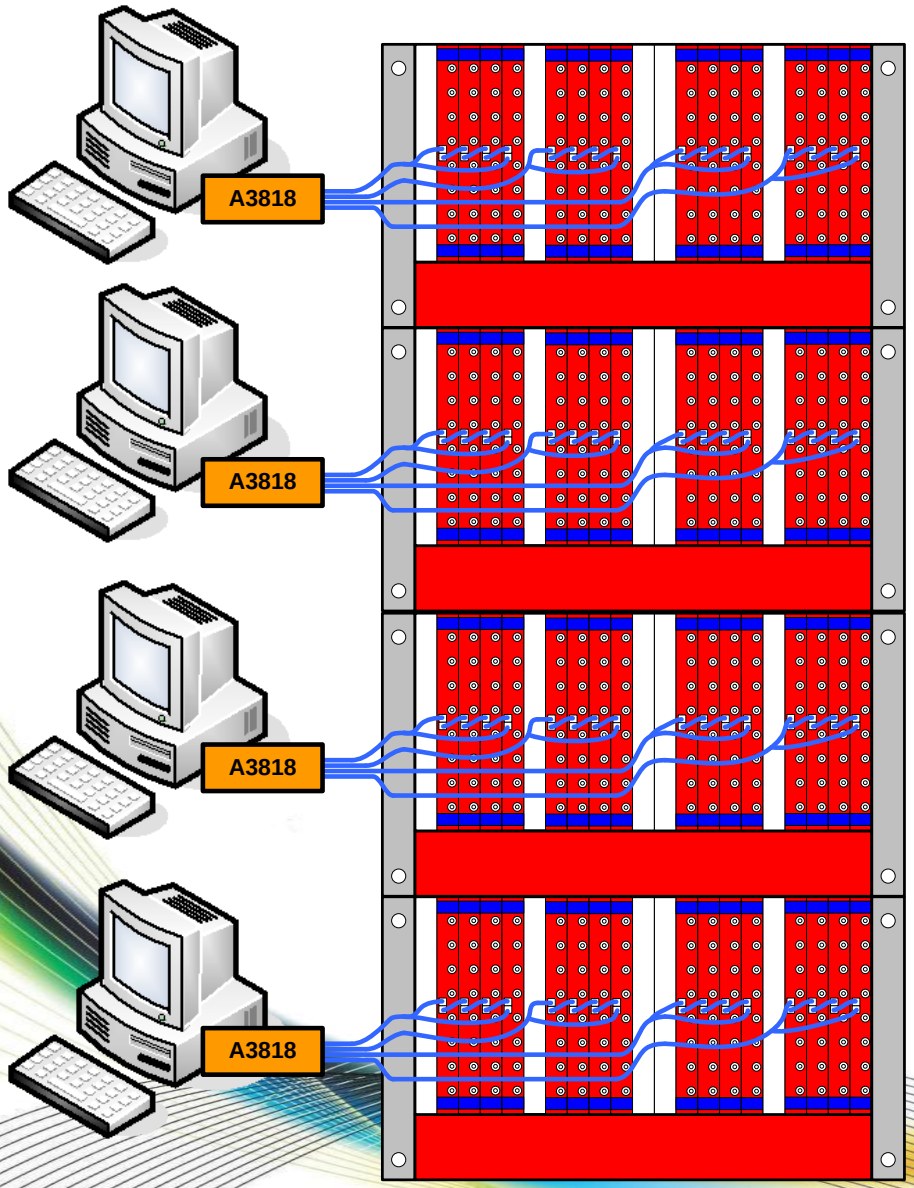
CONET example: XMASS experiment



64 V1751 modules in 4 VME crates

512 channels (10 bit @ 1GHz)

4 A3818 4 link PCIe cards

16 parallel CONET links

4 digitizers daisy chained

Readout Bandwidth = ~2 MB/s/ch

Total Bandwidth = ~ 1GB/s

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Readout and and Communication: VME and USB

- **Compliant with VME 64 and 64X**
  - D32 for register access
  - MBLT, 2eVME and 2eSST for data readout
- **USB 2.0**
  - Available for Desktop and NIM versions
  - Bridge for VME crates
  - ~30MB/s max bandwidth
  - Easy connection to any PC, including laptops
  - Ideal for low/medium data rate systems

NIM

Desktop

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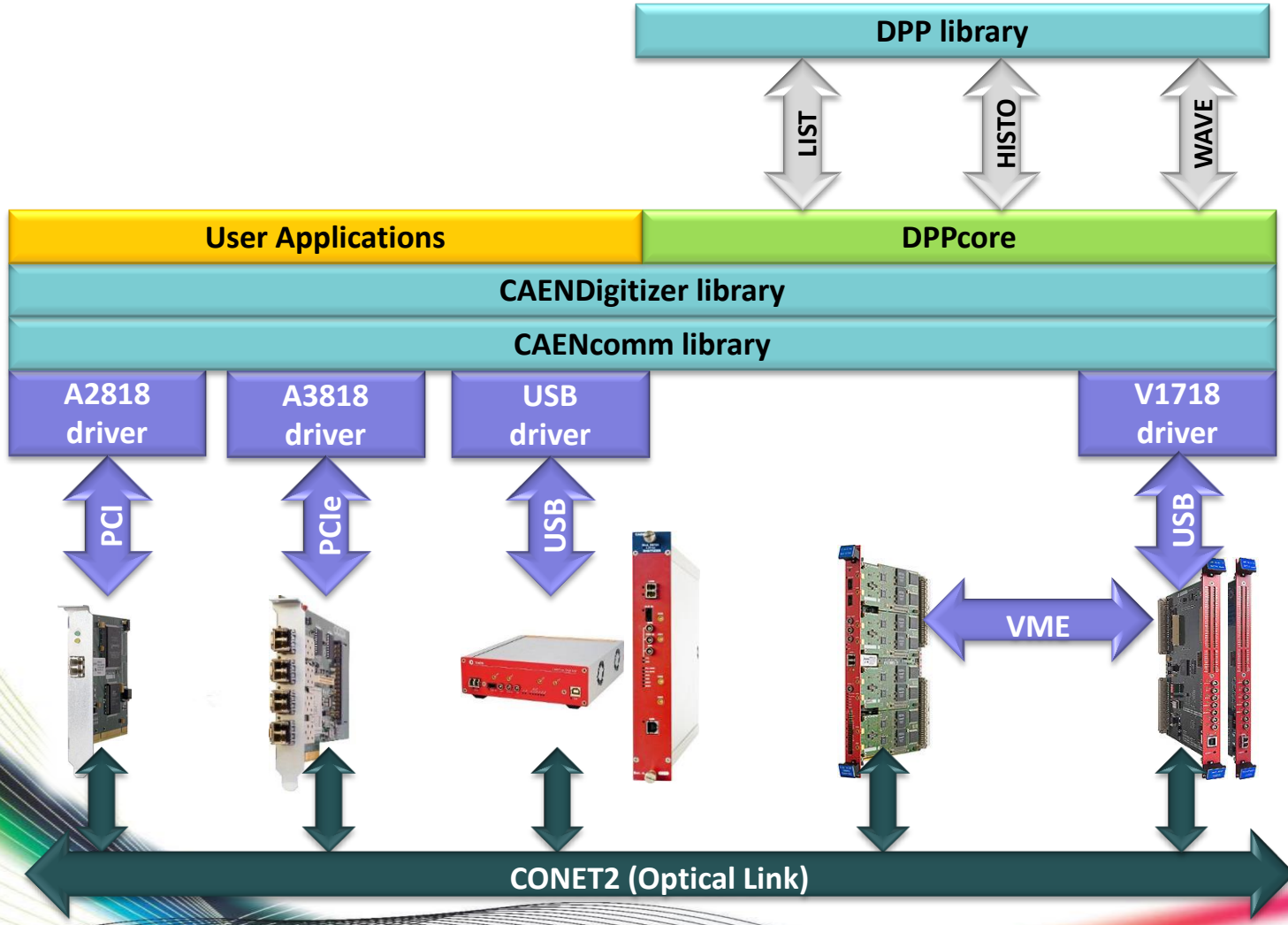
Communication Protocols and Libraries



Set/Get Params, Start/Stop
Read Events, etc.

Open/Close, Read, Write

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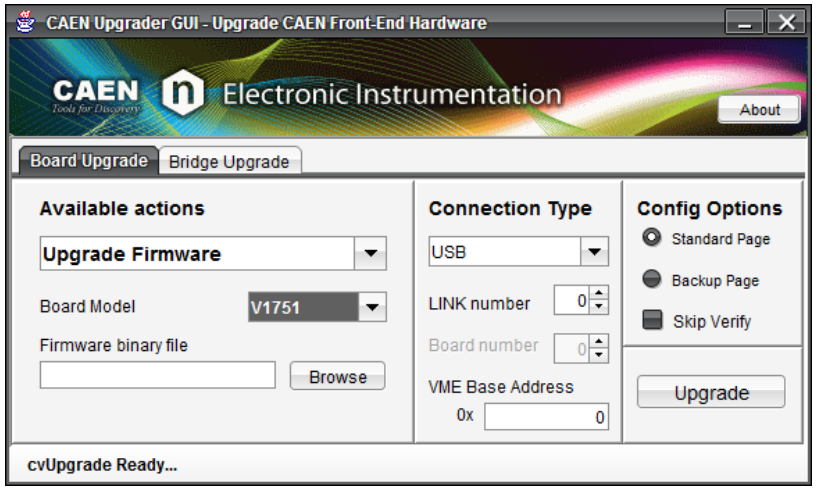
CAEN Software

- All CAEN software **is free** to be downloaded
  - Available on the website www.caen.it
- Many software tools available, e.g. :
  - **CAEN Upgrader**: Graphical User Interface to upgrade the firmware of Waveform Digitizers, VME Power Supplies and Bridges.



  - **Wavedump**: CAEN Digitizer readout application. It represents an extensive demo on how to configure boards running Standard Firmware.
  - **CAEN Scope**: Graphical User Interface software which emulates a multichannel oscilloscope
  - **DPP Control Software**: DPP firmware management and Java Grafical User Interface. Data monitoring, acquisition and storage in easy steps.

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Digital Detector Emulator

This is the first synthesizer of random pulses that is also an emulator of radiation detector signals with the possibility to configure the energy and time distribution

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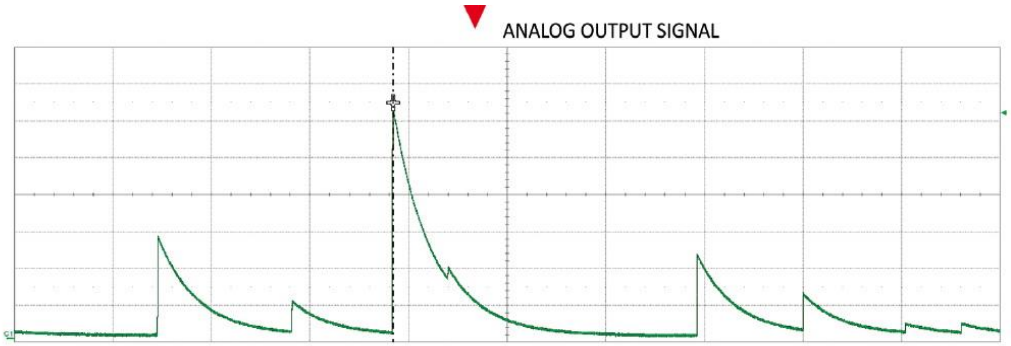
Operating Principle

- The Digital Detector Emulator combines
  - Time and energy distributions
  - Detector waveforms
  - Models of interference and noise

  … to provide an emulation the closest possible to real setups

- At the same time it is
  - Delay generator
  - Arbitrary function generator
  - Time and Energy calibrator



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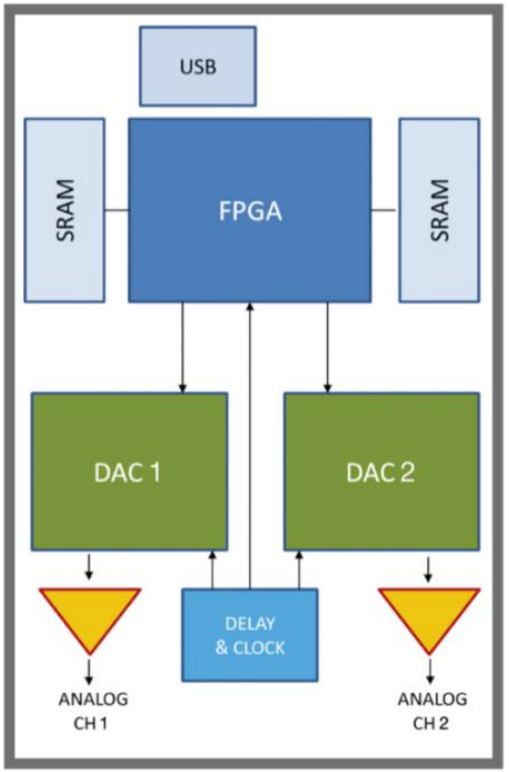
Technical Specification

- Two analog output for waveform generation
  - ±4 V output range
  - 16 bit DAC precision at 125 MHz
- Two digital input
  - External trigger, gate, baseline reset
- Two digital output
  - Trigger output, warnings

- Emulation
  - Up to 16 pile-up events in **Function Generator** mode
  - Unlimited pile-up in **Integrator Circuit** emulation (Digital RC)
  - Minimum time between events of 8 ns



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Getting start: OneTouch Interface

OneTouch interface

- **Simple interface**
- **Digital RC emulation**
- **Exponential shape only**

Set the

- **Time distribution**
- **Amplitude**
- **Rise and decay time**
- **Noise**

Go to the main software GUI for all the DDE functionalities

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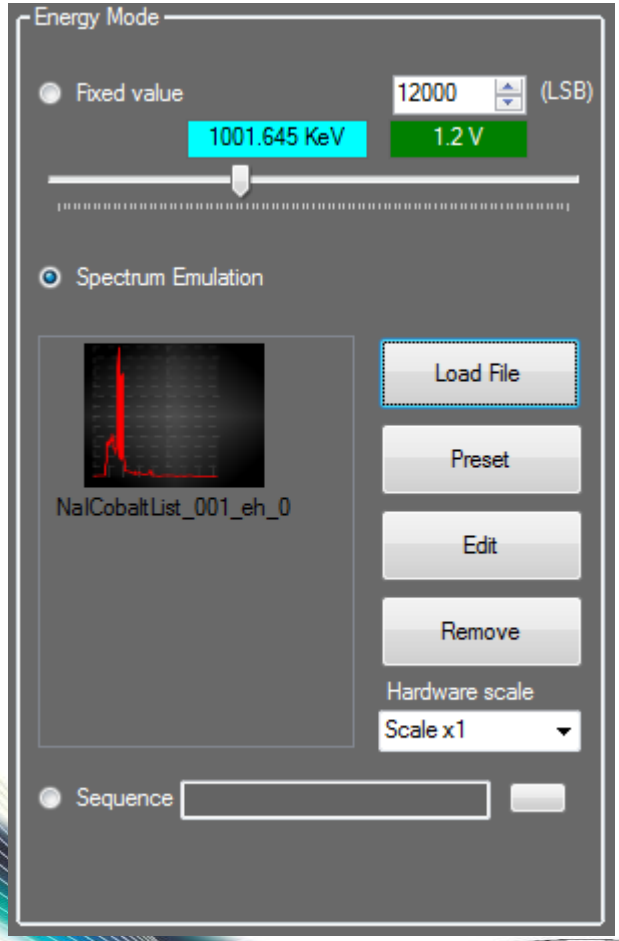
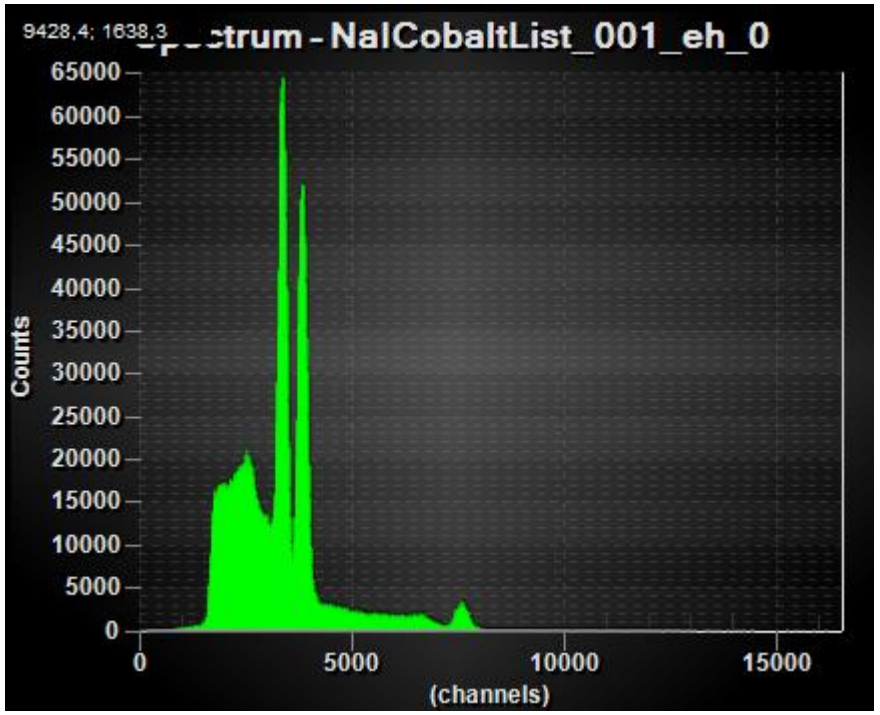
Spectrum Emulator

Main Software GUI: channel settings





- **Select a fixed energy value in three ways: LSB, KeV, Volt**
- **Load a custom spectrum file**

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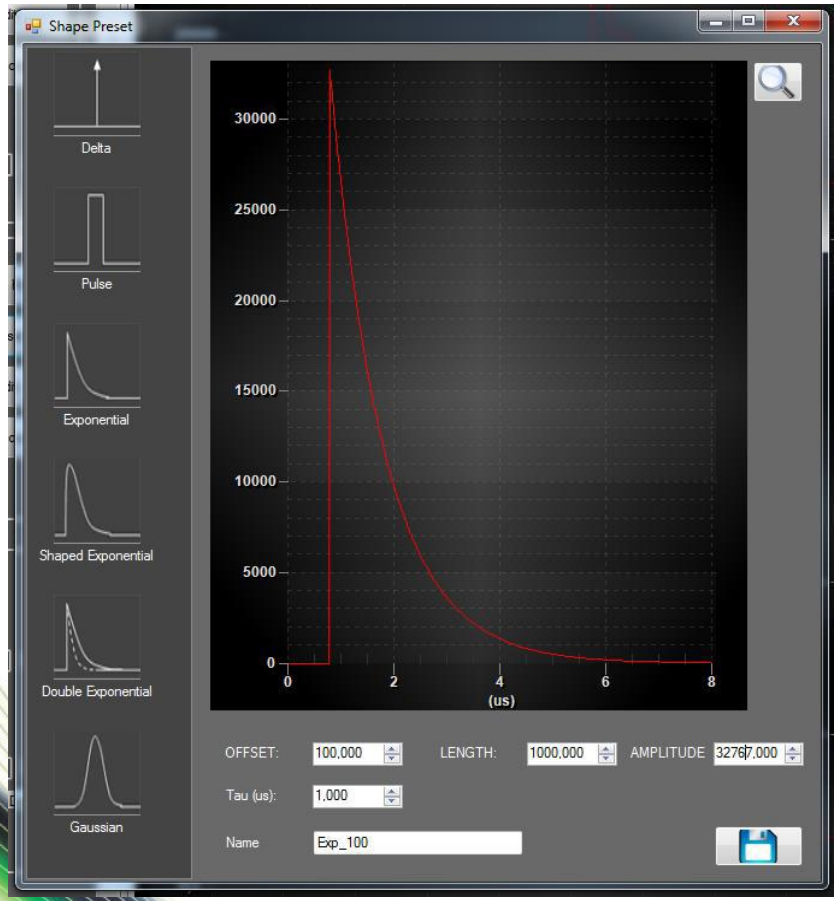
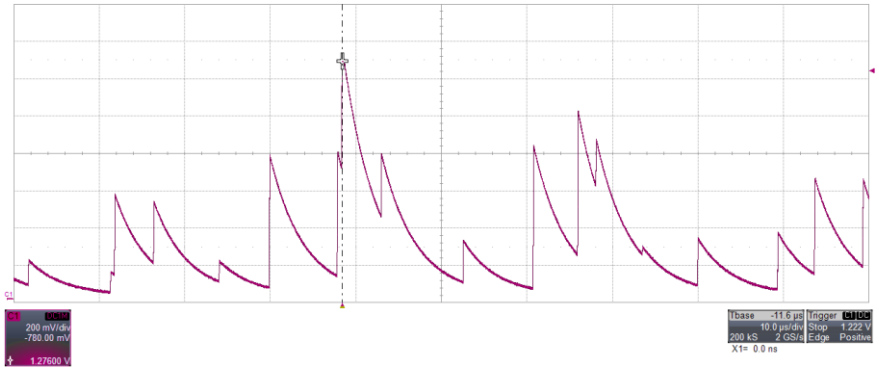
Arbitrary Waveform Generator



- Choice between
  - Software preset shapes
  - User defined shape
- Up to 4096 points in the memory buffer
  - possibility to interpolate (up to 26 ms wave duration)
- Up to two different shapes per channel



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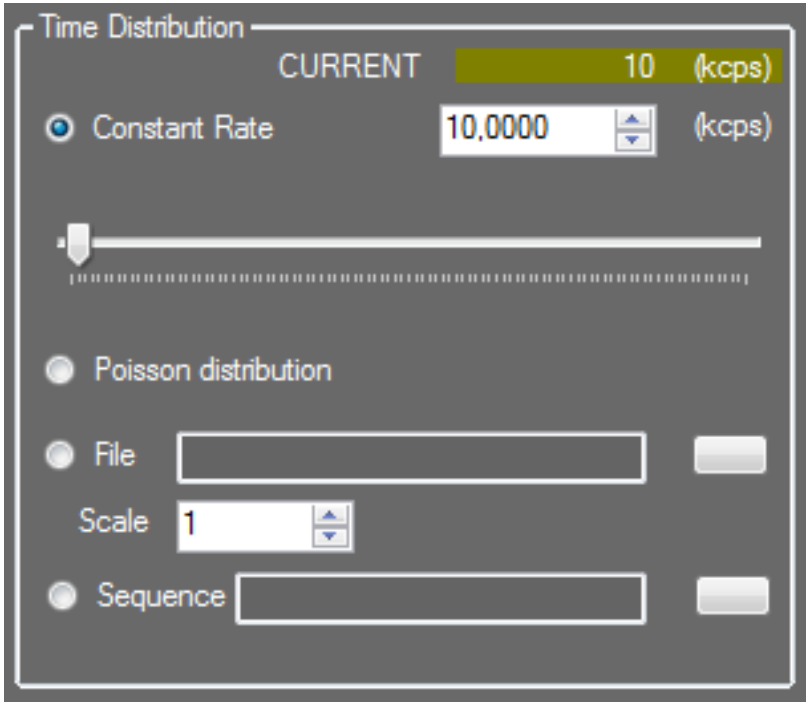
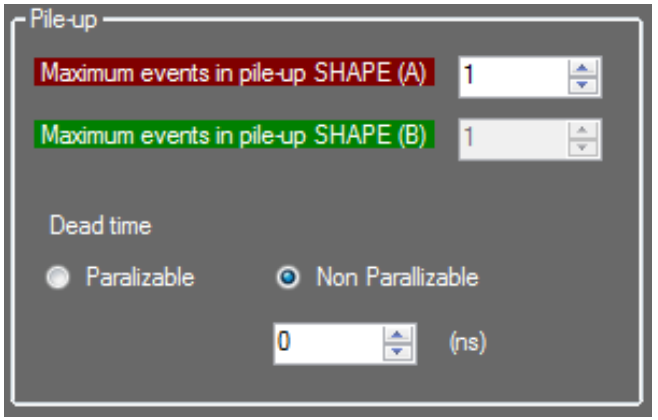
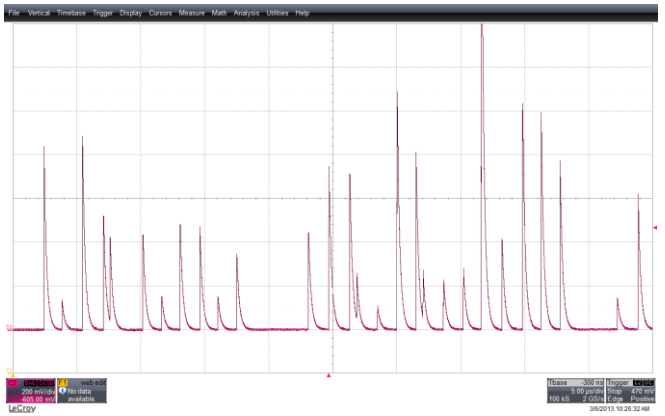
Time Distribution







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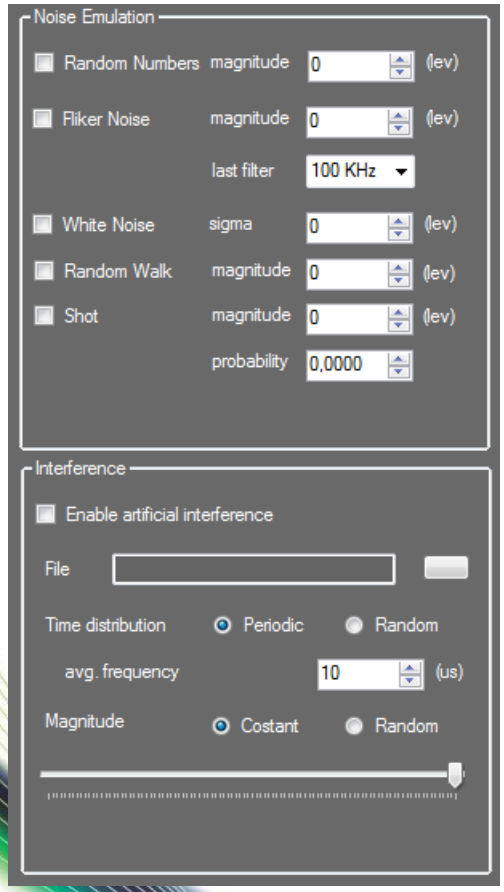
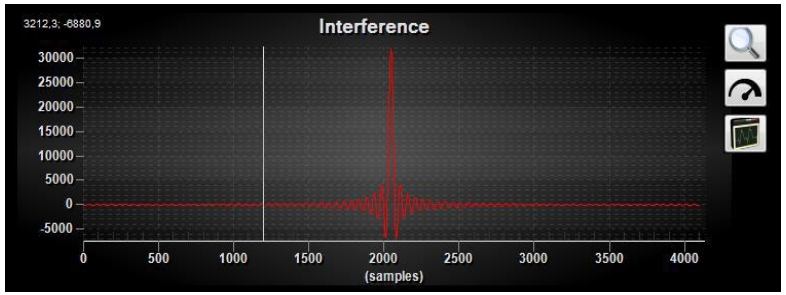
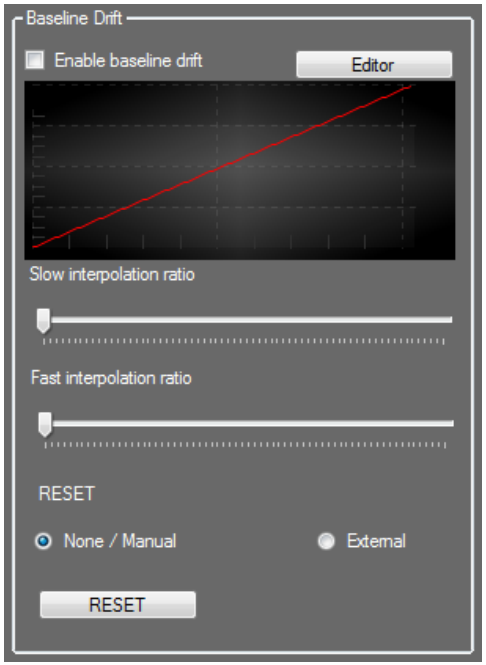
Interference, Noise and Baseline Drift







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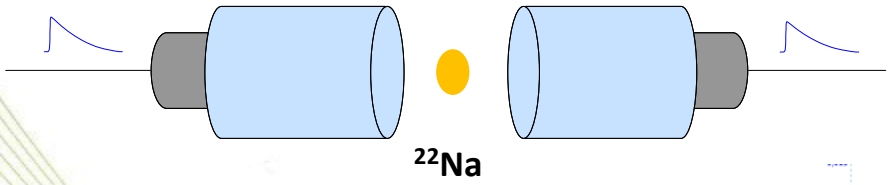
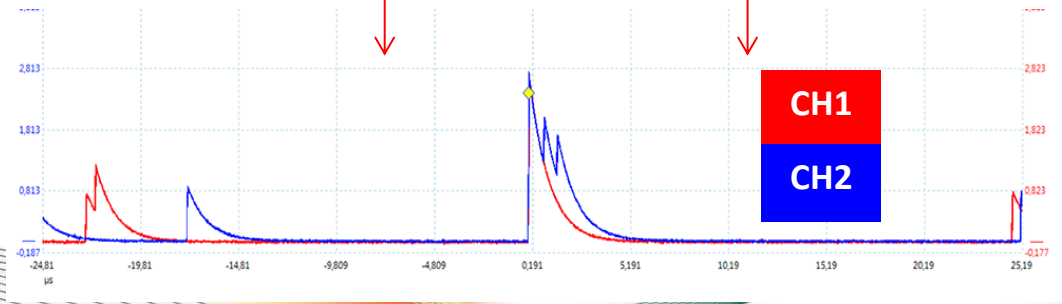
Example of Application

- Emulation of Events in coincidence
  - Event energy spectrum
  - Poisson time distribution
  - Channels perfectly correlated or introduction of accidental background (poisson distributed)



CH1

CH2



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Highlights

- Waveform Digitizers
  - Suited both for small laboratory tests and highly segmented systems such as particle physics experiments
  - Possibility to implement sofisticated event correlation on-line with board connectivity
  - Easy settings with CAEN software demos and Grafical User Interface software. Starting point for more sofisticated data acquisition and analysis.
  - Different technical specifications and possible customizations to match costumer needs
- Digital Detector Emulator
  - Combine energy, time distributions and programmable waveforms to emulate detector signals
  - Suited for educational laboratories and tests of acquisition instrumentation
  - Arbitrary function, delay and pattern generators represent subelements of the device

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CAEN
Tools for Discovery

Demo!

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Outline

- Waveform Digitizers
  - Motivation for the use of digital acquisition devices
  - Overview of technical specification, sinchronization and connectivity
  - Digital Pulse Processing Firmware and applications
  - Overview of CAEN Software tools
- **NEW** Digital Detector Emulator (DDE)
  - Introduction to its functions and related software features
- Demo
  - Use of the DDE and the MCA DT5780

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CAEN Digitizers Highlights

- VME, NIM, Desktop form factors
  - VME64, VME64X compliant
- Hardware
  - Optical Link (CONET), USB 2.0
  - Programmable digital I/Os on front pannel
  - Memory buffer: up to 14.4 MSa/ch
  - FPGA firmware for Digital Pulse Processing
- Multi-board synchronization and trigger distribution
  - Clock synthesis and distribution
  - Time stamp reset
- Software for Windows and Linux

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CAEN Digitizer Offer

Model [1]	Form Factor	N. of ch. [2]	Max. Sampling Frequency (MS/s) [2]	N. of Bits	Input Dynamic Range (Vpp) [2]	Single Ended / Differential Input	Bandwidth (MHz) [2]	Memory (MS/ch) [2]
x720	VME	8	250	12	2	SE / D	125	1.25 / 10
	Desktop/NIM	4 / 2				SE		
x721	VME	8	500	8	1	SE / D	250	2
x724	VME	8	100	14	0.5 / 2.25 / 10	SE / D	40	0.5 / 4
	Desktop/NIM	4 / 2				SE		
x730	VME	16	500	14	0.5 - 2	SE	250	0.64 / 5.12
NEW	Desktop/NIM	8						
x731	VME	8 - 4	500 - 1000	8	1	SE / D	250 / 500	2 / 4
x740	VME	64	62.5	12	2 / 10	SE	30	0.19 / 1.5
	Desktop/NIM	32						
x751	VME	8 - 4	1000 - 2000	10	1	SE / D	500	1.8 - 3.6 / 14.4 - 28.8
	Desktop/NIM	4 - 2				SE		
x761	VME	2	4000	10	1	SE / D	1000	7.2 / 57.6
	Desktop/NIM	1				SE		
SWITCHED CAPACITOR x742	VME	32+2	5000 [4]	12	1	SE	500	0.128 / 1
	Desktop/NIM	16+1						
x743	VME	16	3200 [4]	12	2.5	SE	500	0.007
NEW	Desktop/NIM	8						

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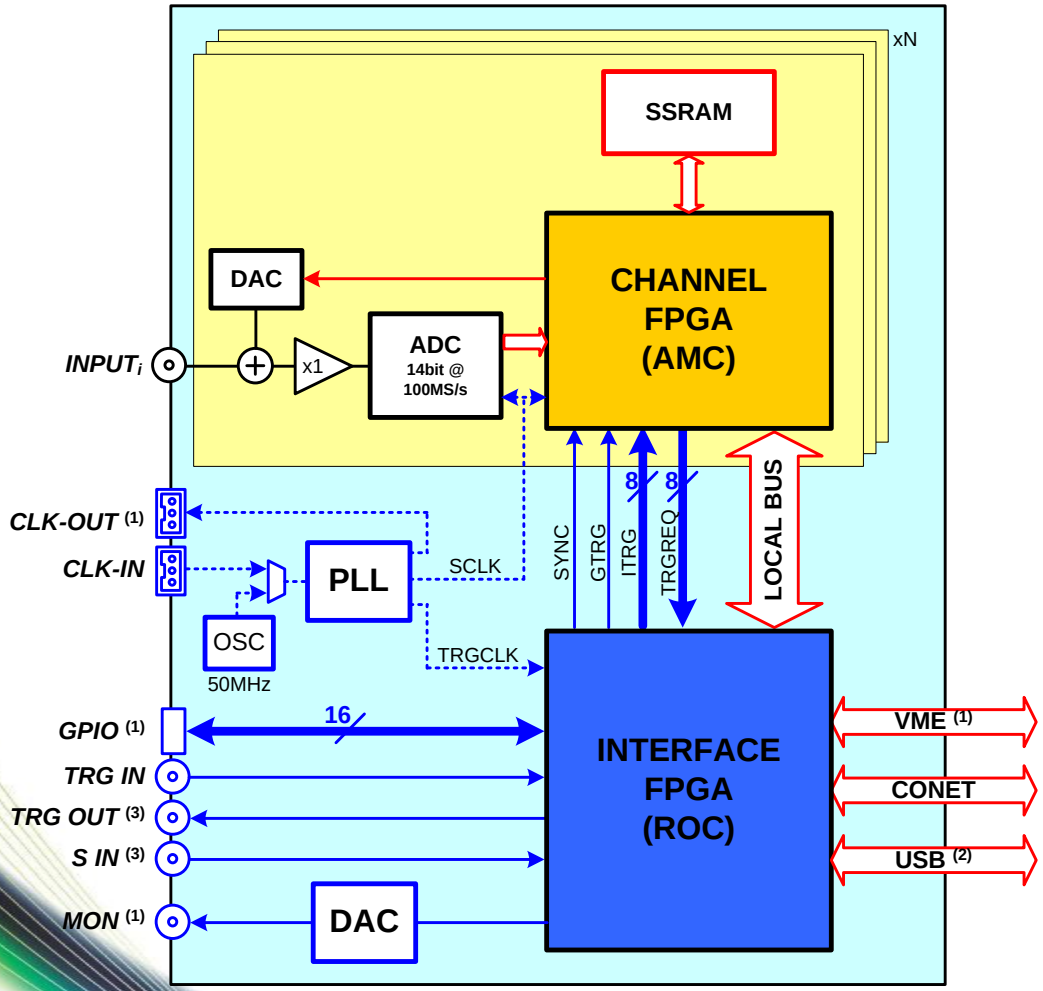
Architecture



(1) VME boards only
(2) Desktop/NIM boards only
(3) for Desktop/NIM baords, TRG-OUT = GPO, S-IN = GPI

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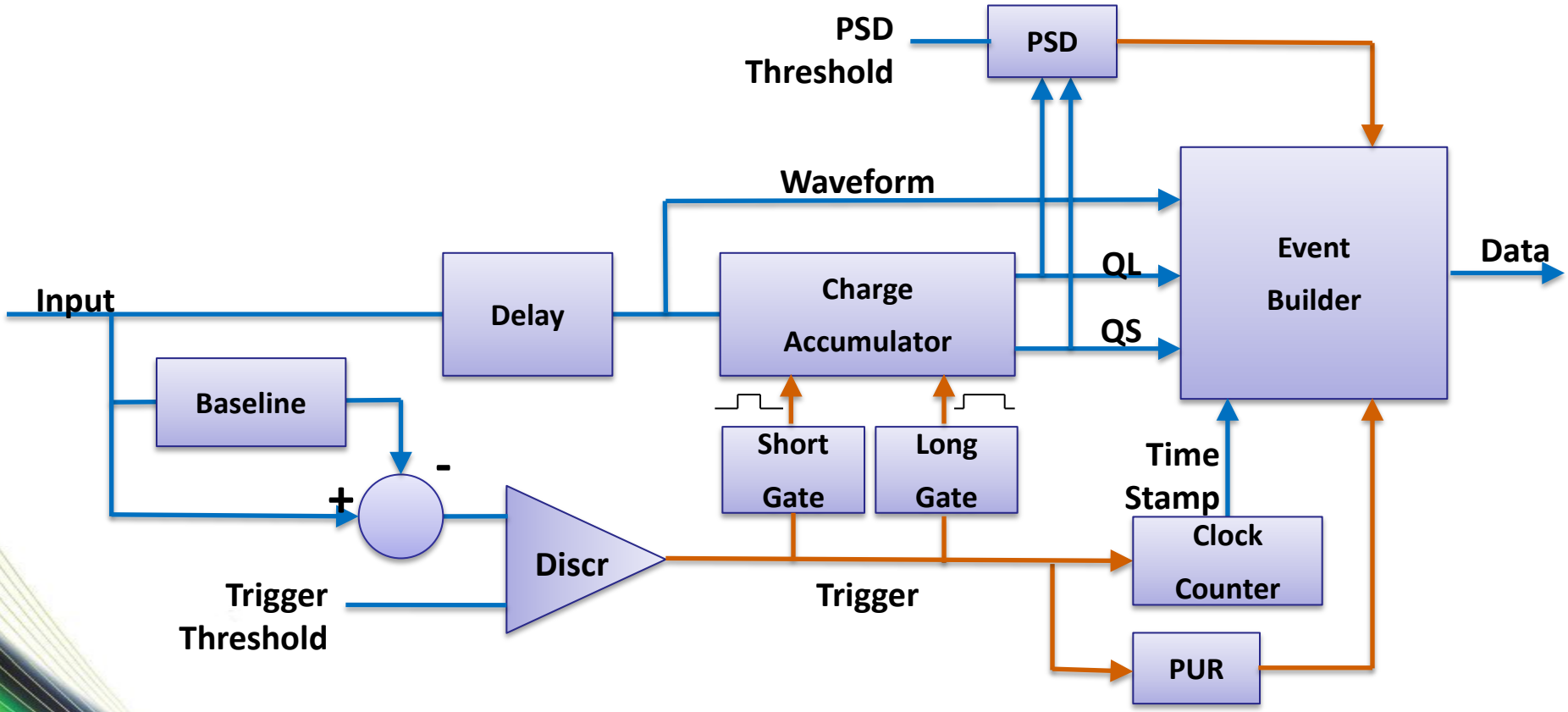
Pulse Shape Discrimination: Block Diagram



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Multi-board Synchronization: example 1

- **Requirements**: N boards with independent triggers (combination of the channel auto-triggers or external trigger).
- **Setup**: daisy chain of the connectors SIN-TRGOUT to propagate the start of run; TRGIN can be used for the external triggers
- **Start/Stop sequence**:
  1. Arm all boards to start with a logic pulse fed in SIN
  2. Send a SW Start (1) on the 1st board to start the run
  3. Send a SW Stop (1) on the 1st board to stop the run
- **Event alignment**: Busy signal (= memory almost full) propagated through LVDS I/Os up to the last board; global busy connected to the veto input of the 1st board; veto propagated in daisy chain (through LVDS I/Os) in order to stop all triggers

(1) run can also be started/stopped by an hardware signal going high/low and feeding the SIN input of the 1st board

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Multi-board Synchronization: example 2

- **Requirements**: N boards triggered by a global trigger = OR of all channel self-triggers (one channel triggers all)
- **Setup**: the TRGOUT of each board goes into an external OR logic, whose output goes back to the TRGIN of all boards (parallel fan-out)
- **Start/Stop sequence**:
  1. Arm all boards to start with the TRGIN edge
  2. Send a SW trigger on the 1st board to start the run (propagated through the external OR + fan-out and fed back into TRGINs)
  3. Self-triggers start to be ORed and acquire events in all boards
  4. Disarm acquisition board by board to stop the run
- **Event alignment**: Busy signal (= memory almost full) propagated through LVDS I/Os up to the last board; global busy connected to the veto input of the 1st board; veto propagated in daisy chain (through LVDS I/Os) in order to stop all triggers

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Multi-board Synchronization: example 3

- **Requirements**: N boards with individual self-triggers (1); coincidence and/or propagation on channel basis (each channel can be triggered/validated by a combination of any other)
- **Setup**: the individual TRGOUTs of each channel go into an external trigger logic (e.g. CAEN V1495) through the LVDS I/Os. The trigger logic generates the individual TRGINs of each channel and feeds them into the LVDS I/Os
- **Start/Stop sequence**:
  1. Arm all boards to start with SIN=1
  2. Send a SW Start (2) to the 1st board to start the run
  3. Send a SW Stop (2) on the 1st board to stop the run
- **Event alignment**: usually not necessary; can be managed by the external logic that uses the Busy of each board (on TRGOUT) to inhibit individual triggers

(1) Individual triggers available with DPP firmware only

(2) run can also be started/stopped by an hardware signal going high/low and feeding the SIN input of the 1st board

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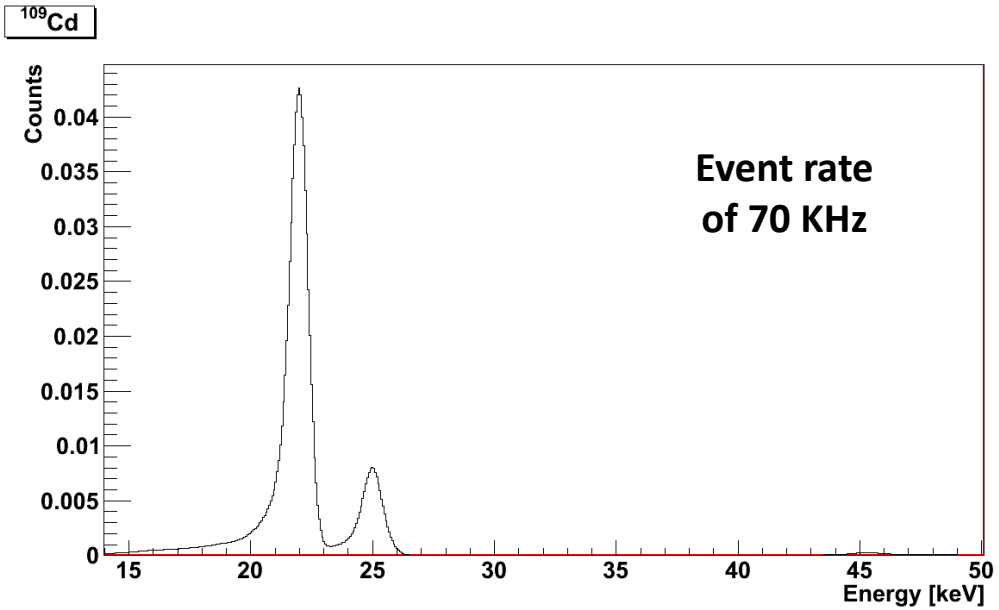
Test Results with CdTe

- Tests executed at University of Palermo on February 2011
  - Detector: CdTe from Amptek with embedded FET integrator
  - Rise Time = 140 ns, Decay Time = 100 μs
  - Source = ^{109}Cd, X-ray peaks at 22 and 25 KeV



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