High-speed building block implementations in the GBT project

Filip Tavernier

CERN

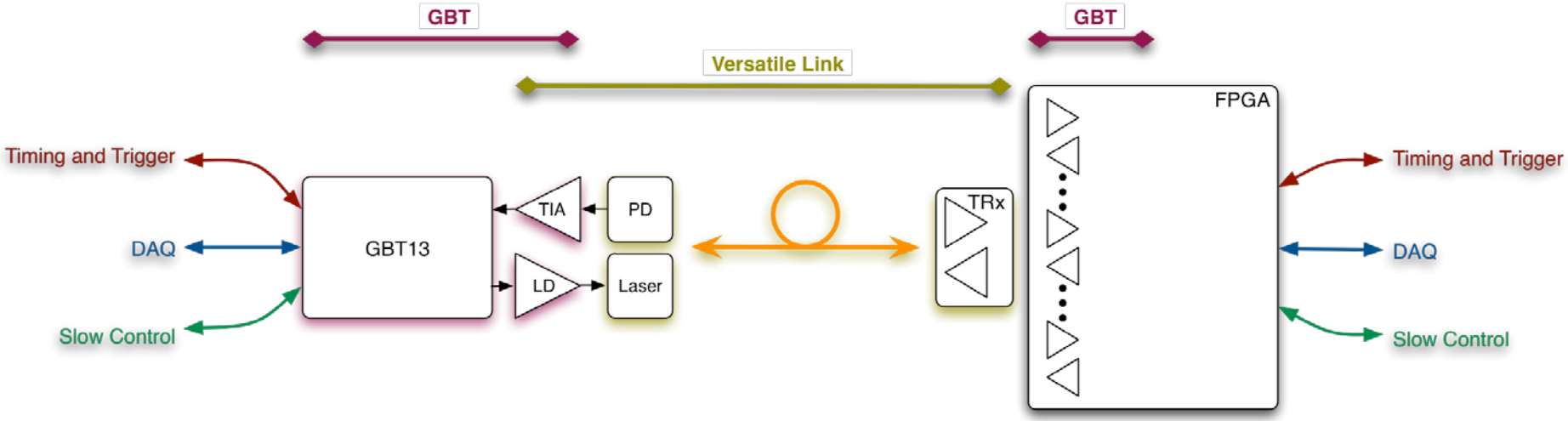
Outline

- GBT project overview
- *Basic PLL operation*
- *GBT ePLL*
- *GBT serializer*
- *GBT laser driver*

The GBT project

Development of a high-speed bidirectional optical link for the LHC experiments upgrade program:

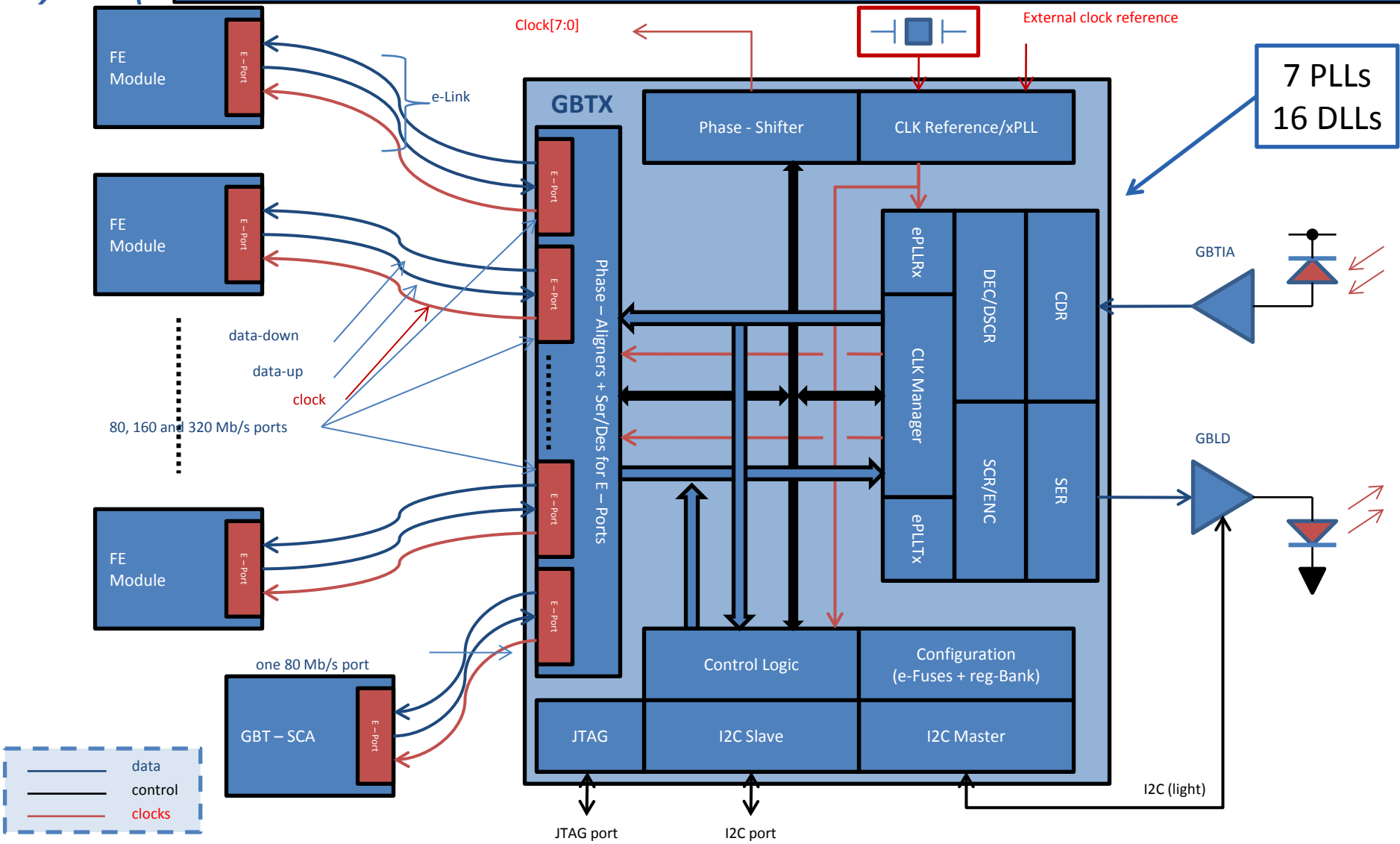
- Versatile link project: opto-electronics
- GBT project: ASIC design, especially for on-detector systems



On-Detector
Custom Electronics & Packaging
Radiation Hard

Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

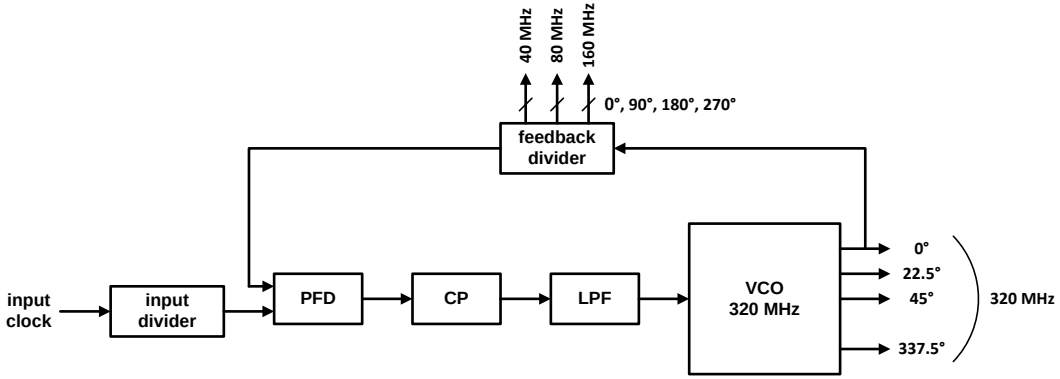
The GBT system



Outline

- *GBT project overview*
- Basic PLL operation
- *GBT ePLL*
- *GBT serializer*
- *GBT laser driver*

PLL principle



$$\frac{\varphi_{out}}{\varphi_{in}} = \frac{1}{M} \cdot \frac{K_D K_{VCO} F(s)}{s + \frac{K_D K_{VCO} F(s)}{N}}$$

M	input divider ratio
N	feedback divider ratio
K_D	PFD and charge pump gain [A/rad]
$F(s)$	loop filter gain [V/A]
K_{VCO}	VCO gain [Hz/V]

principle: equalize the phase of the generated clock to the phase of the input clock

→ PFD measures the phase error and steers the charge pump to bring the phase of the feedback clock towards that of the input clock

→ in steady-state, the phase (and frequency) of the clocks at the input of the PFD are equal

→ input divider enables the input clock frequency to be higher than that of the VCO clock

→ feedback divider enables the input clock frequency to be lower than that of the VCO clock

→ PLL is a feedback amplifier for phase (frequency), not for amplitude

→ can become unstable!

PLL transfer function

$$\frac{\varphi_{out}}{\varphi_{in}} = \frac{1}{M} \cdot \frac{K_D K_{VCO} F(s)}{s + \frac{K_D K_{VCO} F(s)}{N}}$$

$$= \frac{N}{M} \cdot \frac{\omega_n^2 + 2 \cdot s \cdot \zeta \omega_n}{s^2 + 2 \cdot s \cdot \zeta \omega_n + \omega_n^2}$$

order of the PLL?
→ VCO is an integrator for frequency
assuming a 1st order loop filter
→ 2nd order system

DC closed-loop gain

low-pass filter with 2 poles and 1 zero
→ -20 dB/decade in the limit
→ overshoot around the -3 dB point depends on damping ζ
→ -3 dB point depends on both ω_n and ζ
→ placement of -3 dB point defines the suppression of spurious signals

$$\omega_n = \sqrt{\frac{K_D K_{VCO}}{N C_{LF}}}$$

$$\zeta = \frac{R_{LF}}{2} \cdot \sqrt{\frac{K_D K_{VCO} C_{LF}}{N}} = \frac{R_{LF} C_{LF}}{2} \cdot \omega_n$$

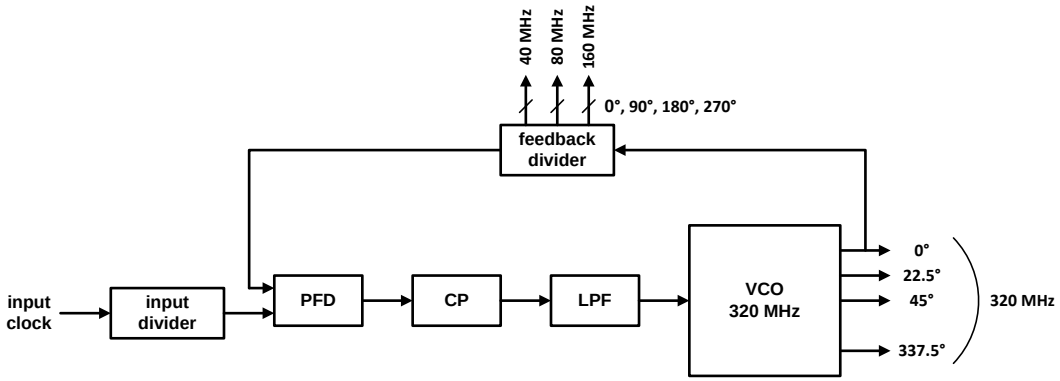
$$\omega_{-3dB} = \omega_n \cdot \sqrt{1 + 2 \cdot \zeta^2 + \sqrt{2 + 4 \cdot \zeta^2 + 4 \cdot \zeta^4}}$$

$$\begin{cases} \zeta = \sqrt{0.5} \longrightarrow \omega_{-3dB} = 2.06 \cdot \omega_n \\ \zeta = 1 \longrightarrow \omega_{-3dB} = 2.48 \cdot \omega_n \\ \zeta = 2 \longrightarrow \omega_{-3dB} = 4.25 \cdot \omega_n \end{cases}$$

Outline

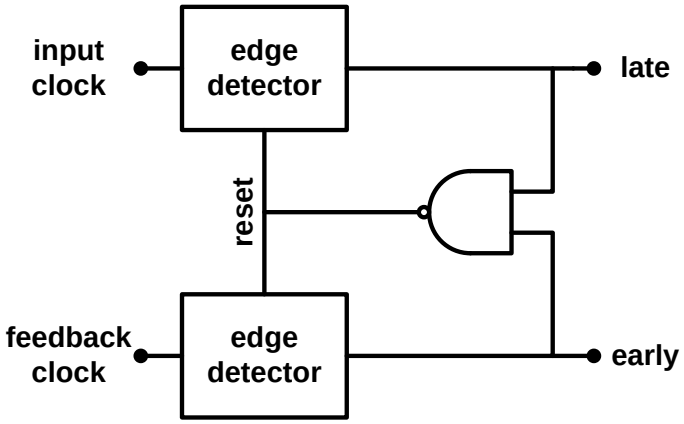
- *GBT project overview*
- *Basic PLL operation*
- GBT ePLL
- *GBT serializer*
- *GBT laser driver*

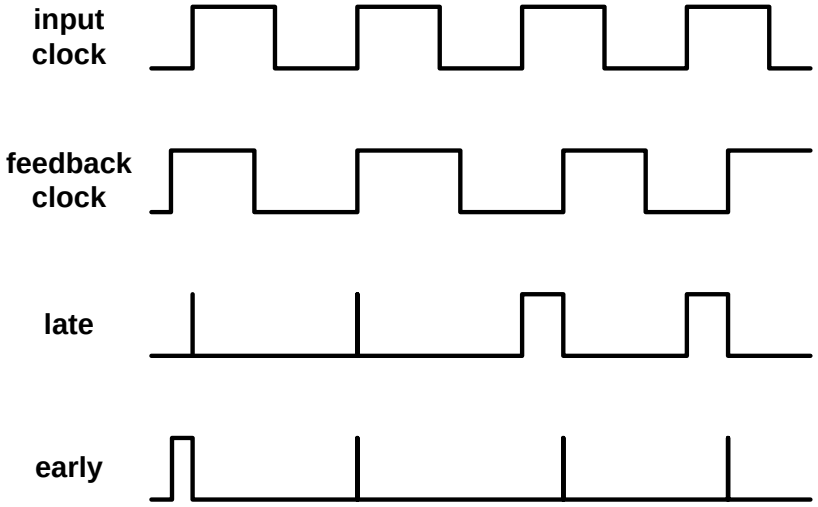
Design example: GBT ePLL



- **input divider:** programmable divider ratio so that the output is always 40 MHz
- **feedback divider:** fixed divider ratio of 4 because the VCO runs at 320 MHz
- **PFD:** determines the frequency and phase difference between the input clocks and outputs UP and DOWN signals, of which the duration depends linearly on the phase difference between the input clocks
- **CP:** charge pump with a 4-bit programmable output current to convert the UP and DOWN signals of the PFD to the current domain
- **LPF:** 1st order loop filter referred to the supply voltage because of the pMOS current sources in the VCO
- **VCO:** voltage-controlled ring-oscillator at 320 MHz with 16 output phases

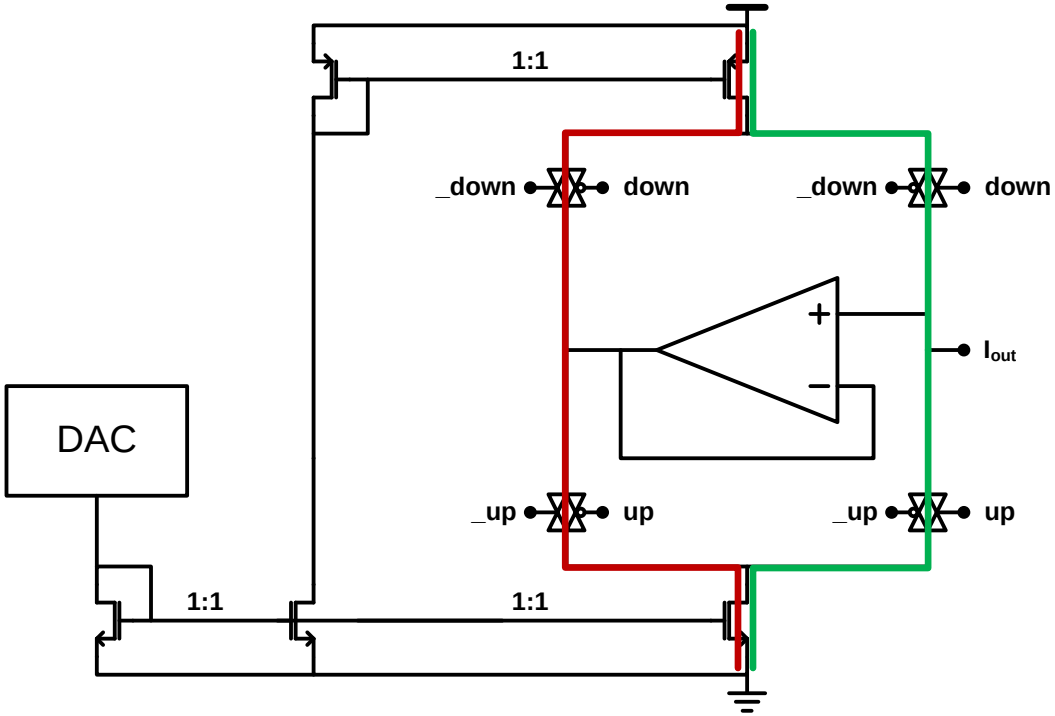
Phase-frequency detector





- linear relationship between the duration of the early/late pulses and the phase error
- PFD is sensitive to phase and frequency errors which leads to a PLL with a locking range that is basically limited by the VCO tuning range
- delay of the NOR gate results in the early/late pulses go high every clock cycle → '4' possible output states of the PFD
- 'translation' of signals taking into account the pMOS current source in the VCO
  - early → VCO is too fast → DOWN → source current into the loop filter
  - late → VCO is too slow → UP → sink current from the loop filter

Charge pump (1)



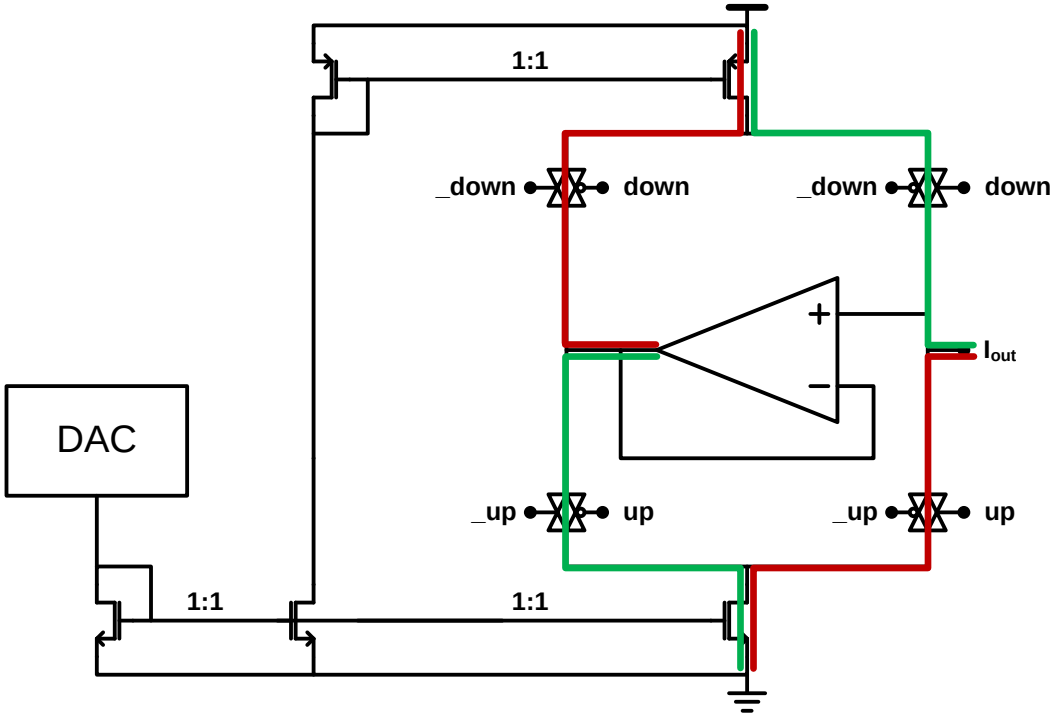
UP = low and DOWN = low

no current flows to the loop filter or in the unity-gain amplifier

UP = high and DOWN = high

no current flows to the loop filter **if sink and source currents are equal**!

Charge pump (2)



UP = high and DOWN = low

sink current flows out of the loop filter, source current flows into the amplifier

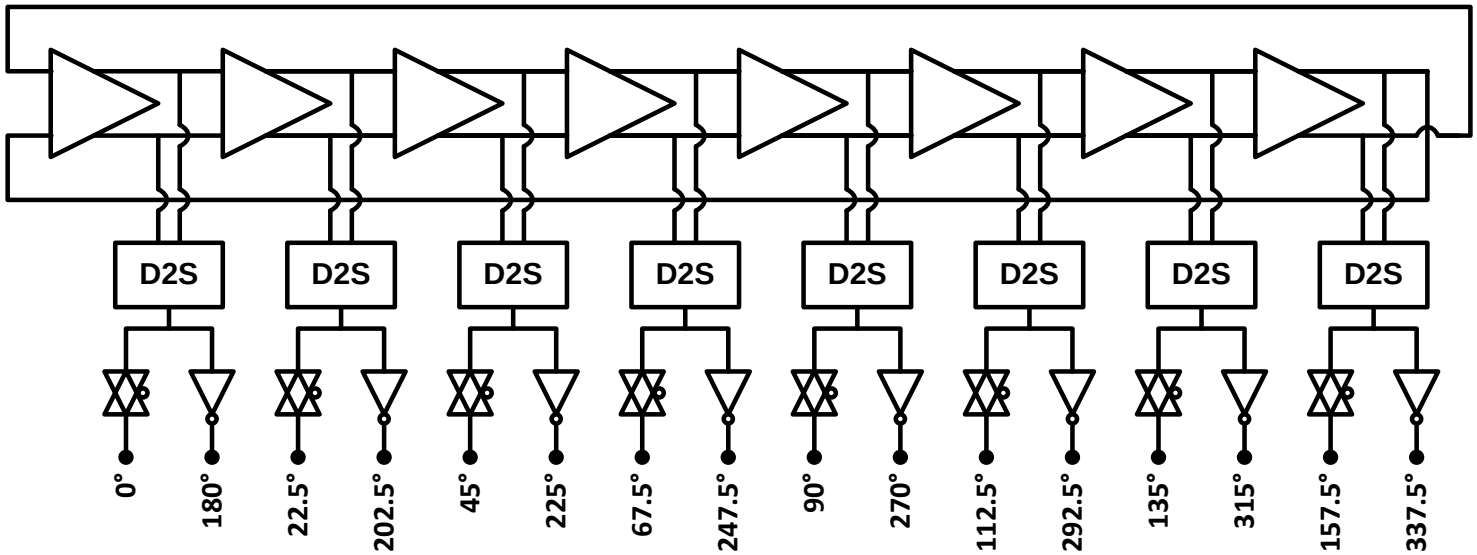
UP = low and DOWN = high

source current flows into the loop filter, sink current flows out of the amplifier

Charge pump non-idealities

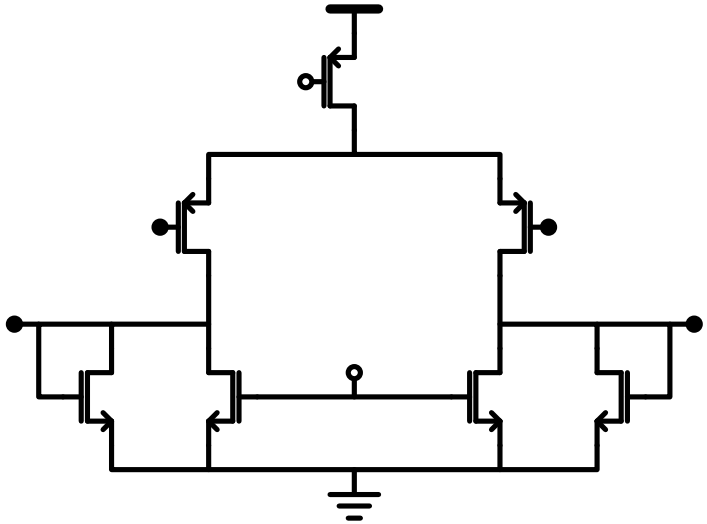
- unequal sink and source currents
  The loop filter is charged or discharged by the current difference when UP and DOWN are both high every clock cycle.
  → static phase error
  → **solution:** current sources with long length and consequently high output impedance
- parasitic capacitance at the drain of the current sources
  Charge sharing takes place every time one of the current sources is connected to the loop filter
  → static phase error
  → **solution:** unity-gain amplifier to equalize the drain voltage of the current sources to the control voltage

Voltage-controlled oscillator



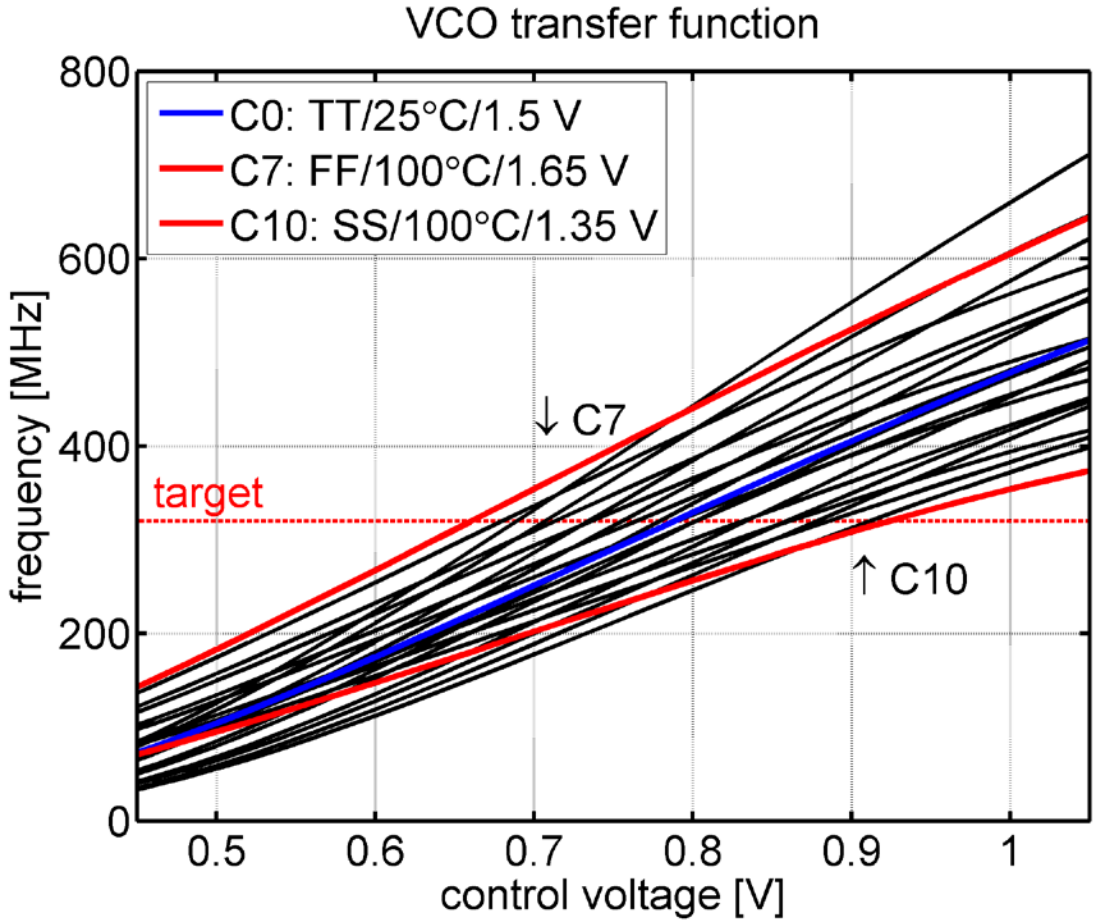
- 8-stage differential ring-oscillator
- 8 D2S converters to generate the full-swing output phases (0°, 22.5°, 45°, 67.5°, 90°, 112.5°, 135°, 157.5°) from the analog levels in between the delay stages
- inverters used to generate the other 8 phases to save the power of another 8 D2S converters
- transmission gates to equalize the phases generated by the D2S converters directly and the ones generated by the inverters

VCO – delay cell



- pMOS differential pair with pMOS current source → control voltage referred to the supply voltage
- input transistors biased with small overdrive voltage because of the relatively large cell delay of 195.3125 ps
- active load consisting of a current source and a diode to avoid the need for a common-mode feedback circuit and still have enough small-signal gain
- gate voltage of the nMOS current sources derived by means of a replica biasing circuit

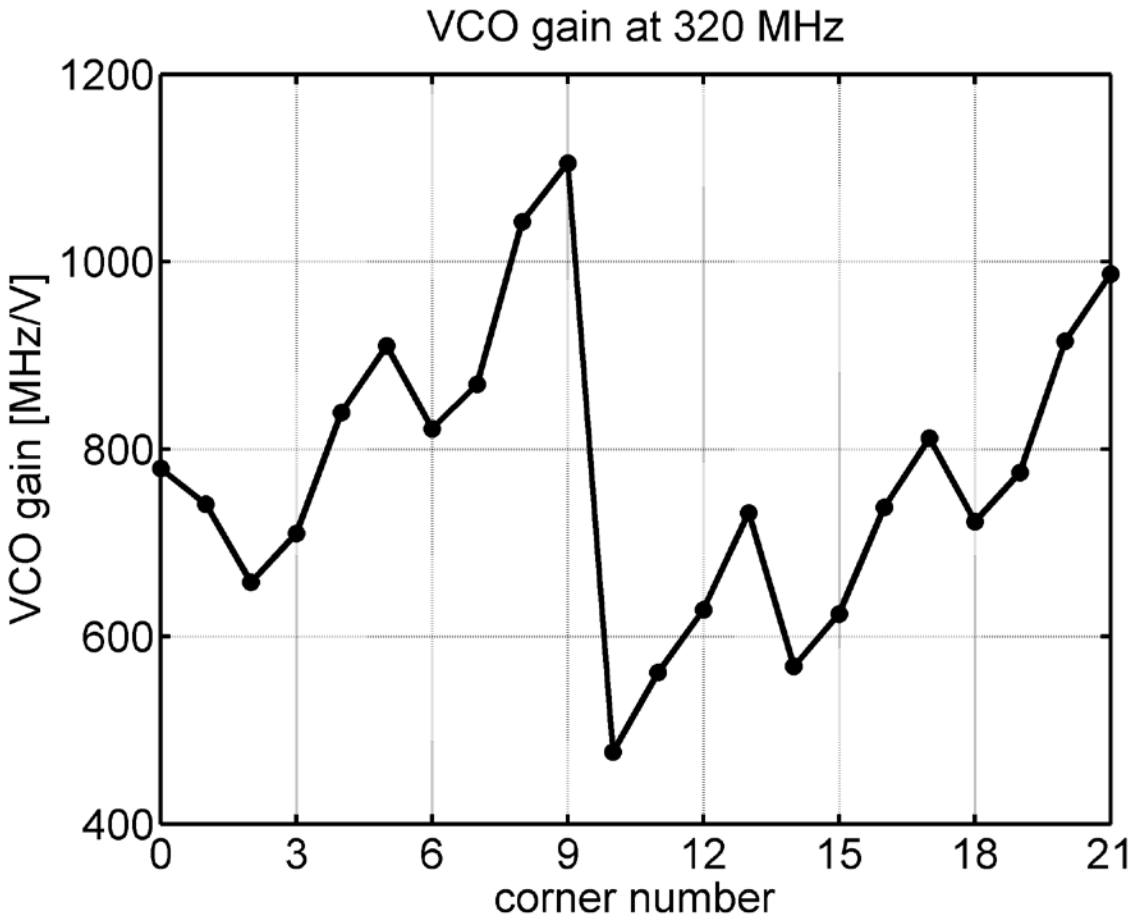
Transfer function of the VCO



control voltage referred to supply voltage!

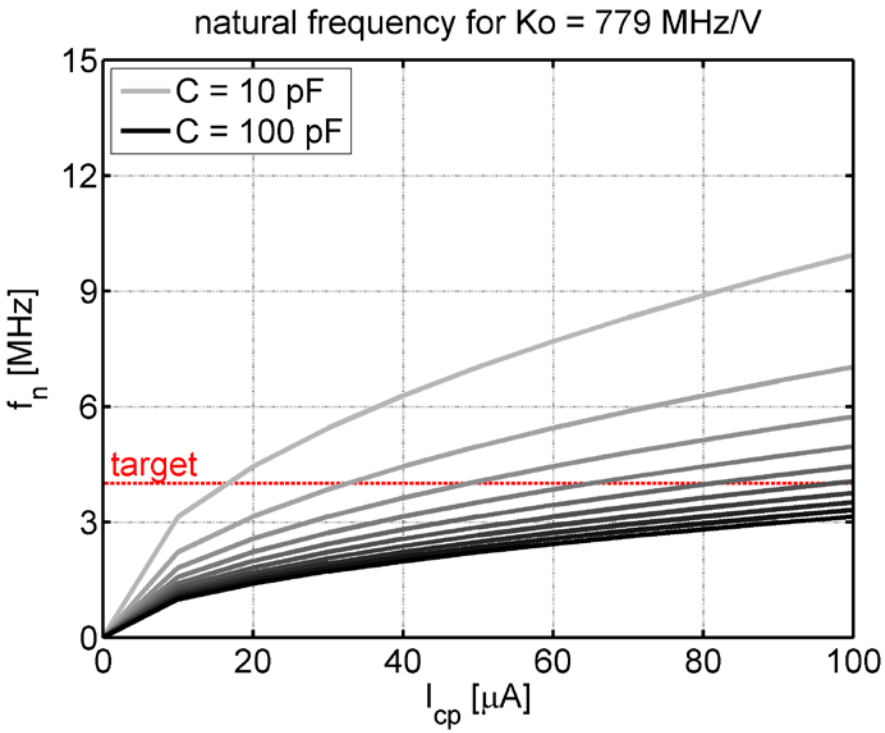
The target oscillation frequency of 320 MHz is obtained in every corner.
The control voltage in lock is between 0.66 V and 0.92 V.

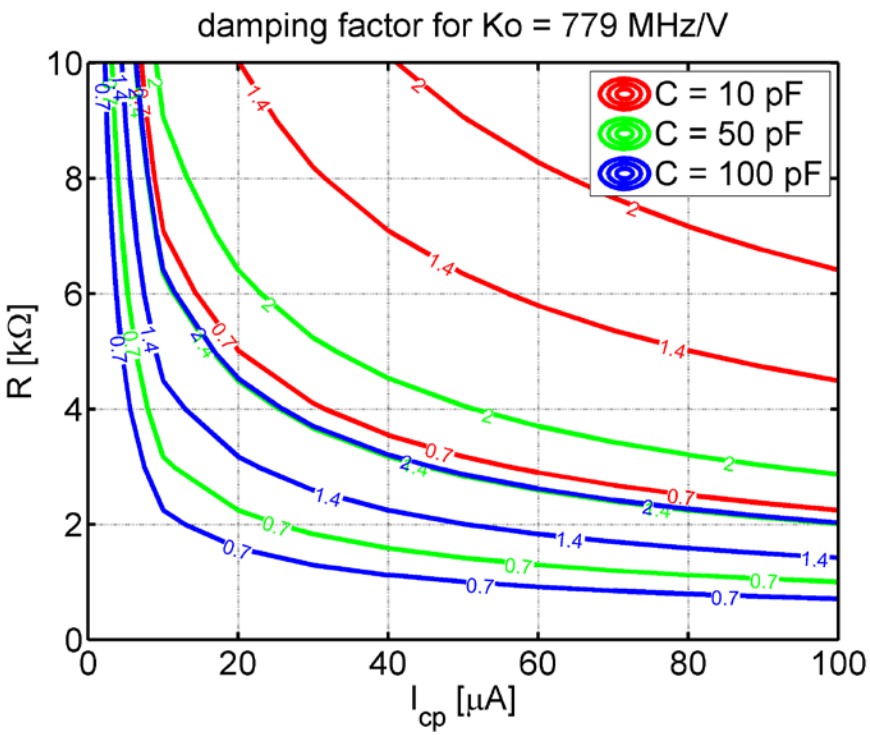
VCO gain at 320 MHz



The typical VCO gain is obtained in C0 (779 MHz/V), the minimal gain is seen in C10 (476 MHz/V) and the maximal in C9 (1106 MHz/V).

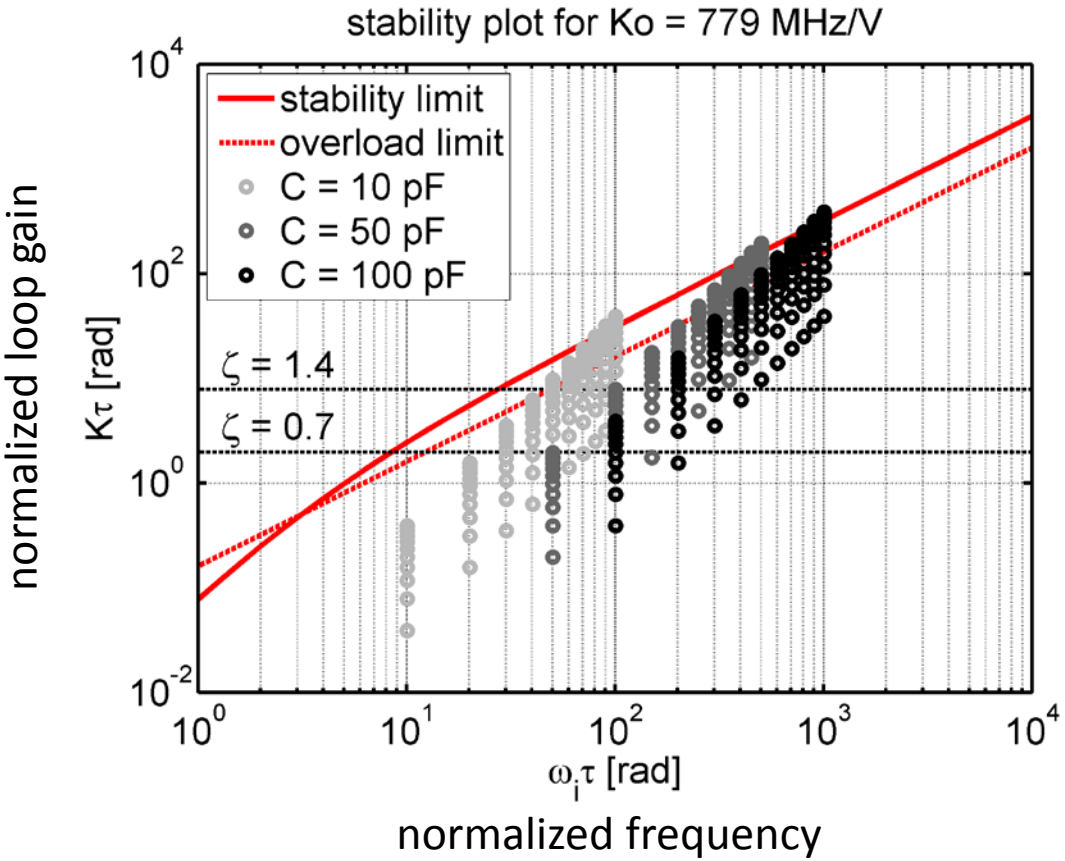
Natural frequency and damping factor with typical VCO gain





- The target natural frequency (4 MHz) is achievable for the smaller filter capacitances (10 pF → 60 pF) if the charge pump current is arbitrarily limited at 100 µA.
- The damping factor can be set to values within the range of interest ($\zeta \approx 1$) for the proposed filter resistance range.

Stability plot with typical VCO gain



PLL is not a continuous-time system, sampled with reference frequency

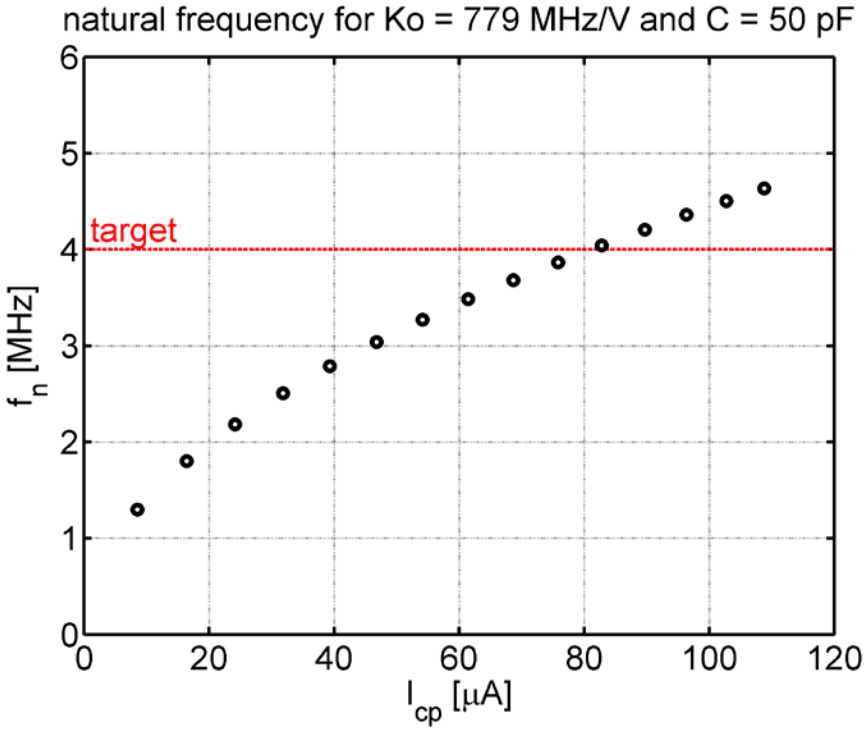
→ stability problems may arise because of the sampled nature

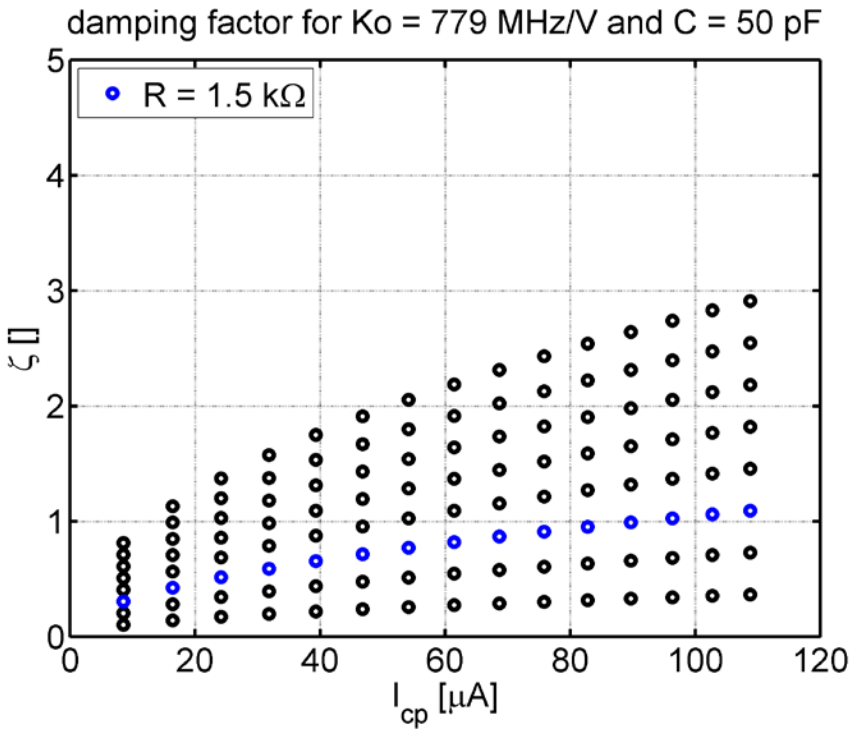
→ stability limit where on the poles of the loop exits the unit circle

Parameter choice

- 4 settable filter capacitances: C = 30 pF, 40pF, 50 pF or 70 pF
- 8 settable filter resistances covering the desired damping factor range (0.7-1.4): 0.5 kΩ → 8 kΩ in steps of 0.5 kΩ
- 15 settable charge pump currents with a range as discussed before: 8.5 µA, 16.4 µA, 24.2 µA, 31.8 µA, 39.4 µA, 46.8 µA, 54.2 µA, 61.5 µA, 68.7 µA, 75.8 µA, 82.8 µA, 89.7 µA, 96.3 µA, 102.7 µA, 108.8 µA

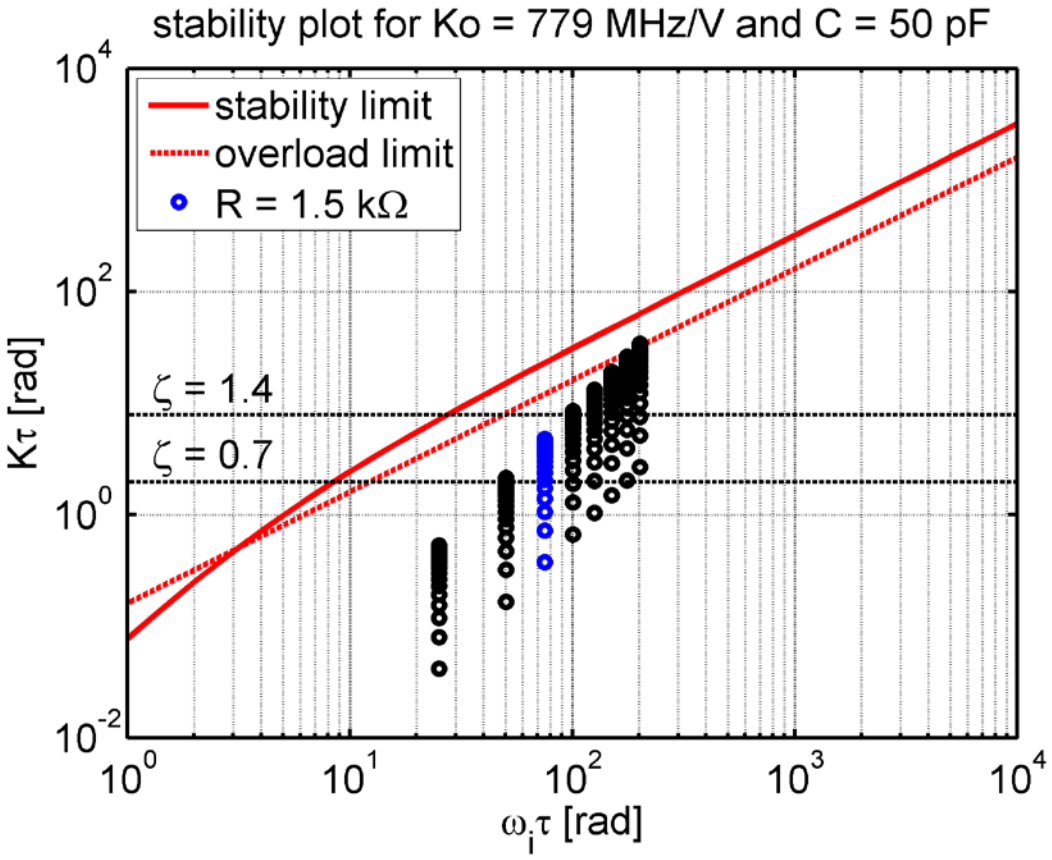
Settable operating points with typical VCO gain (C = 50 pF)





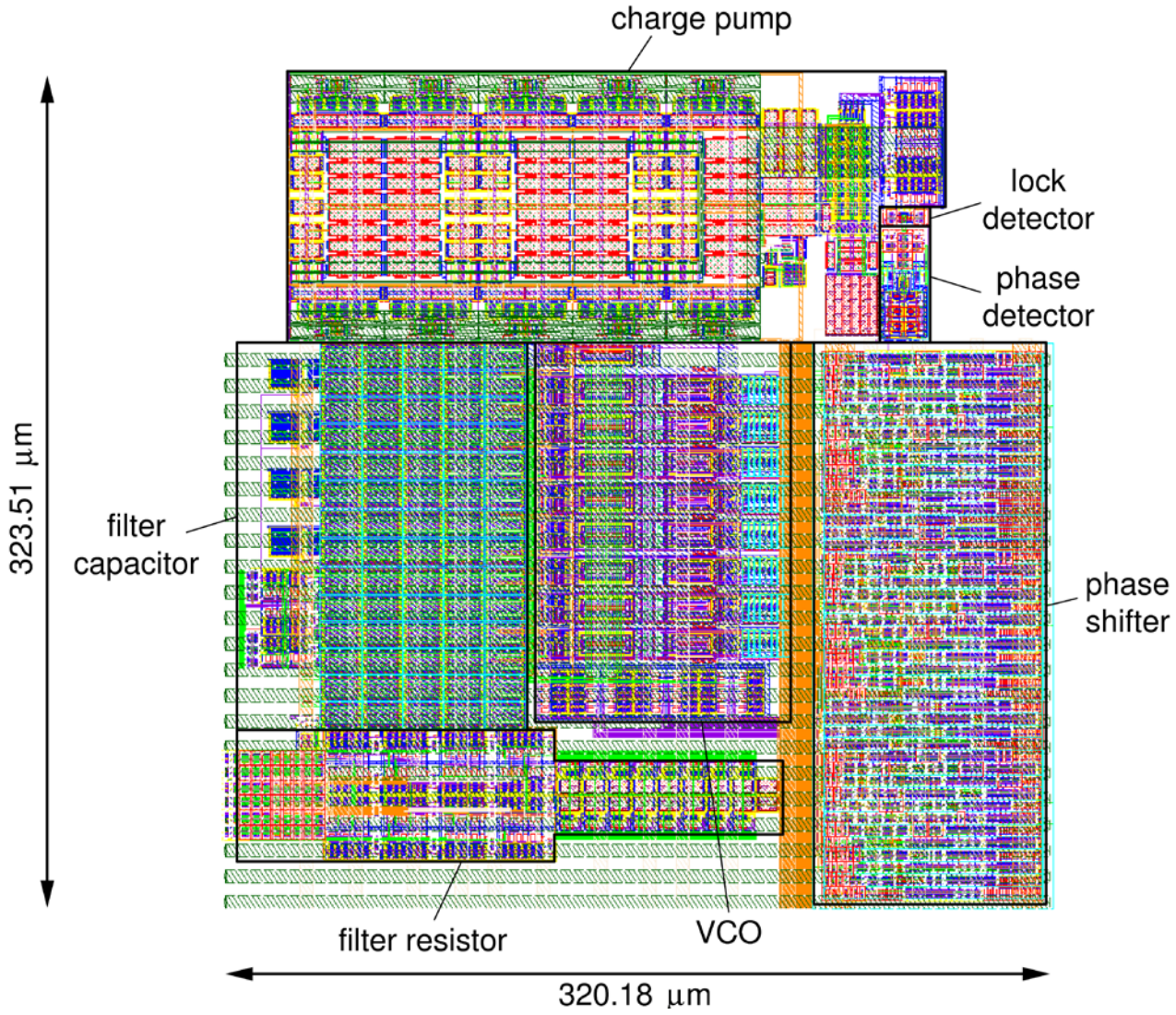
- The target natural frequency (4 MHz) is obtained for a charge pump current of 82.8 µA.
- The optimal damping factor at this charge pump current is reached for a filter resistance of 1.5 kΩ.

Stability of the settable operating points with typical VCO gain (C = 50 pF)

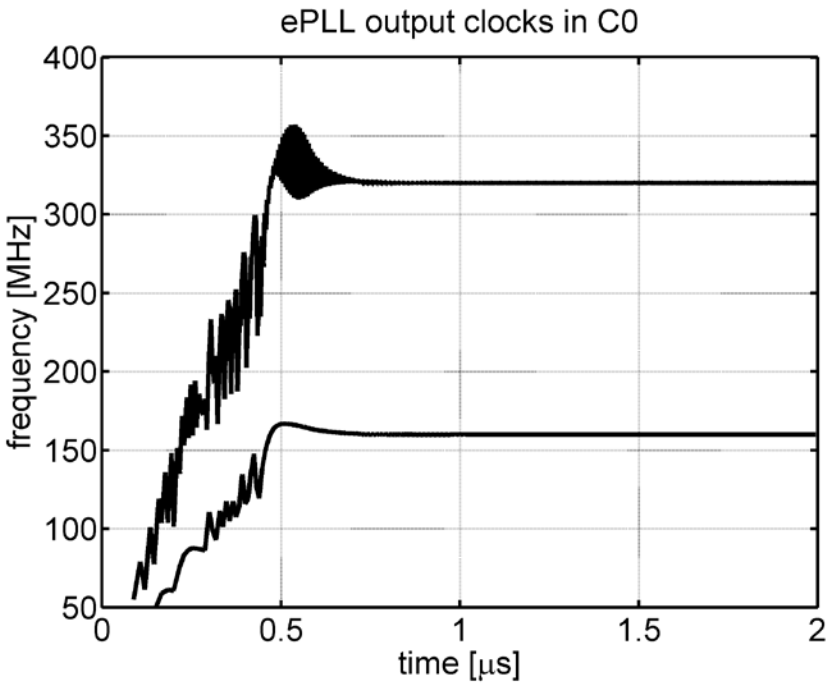


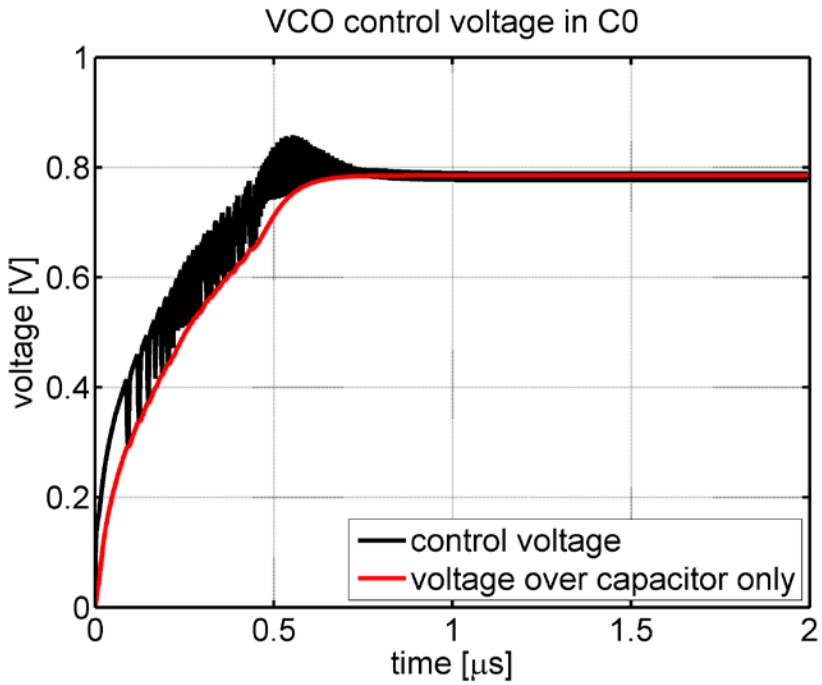
If the filter capacitance is fixed at 50 pF, stability is guaranteed in almost all settable operating points; especially the larger filter resistances can results in stability problems.

ePll core layout



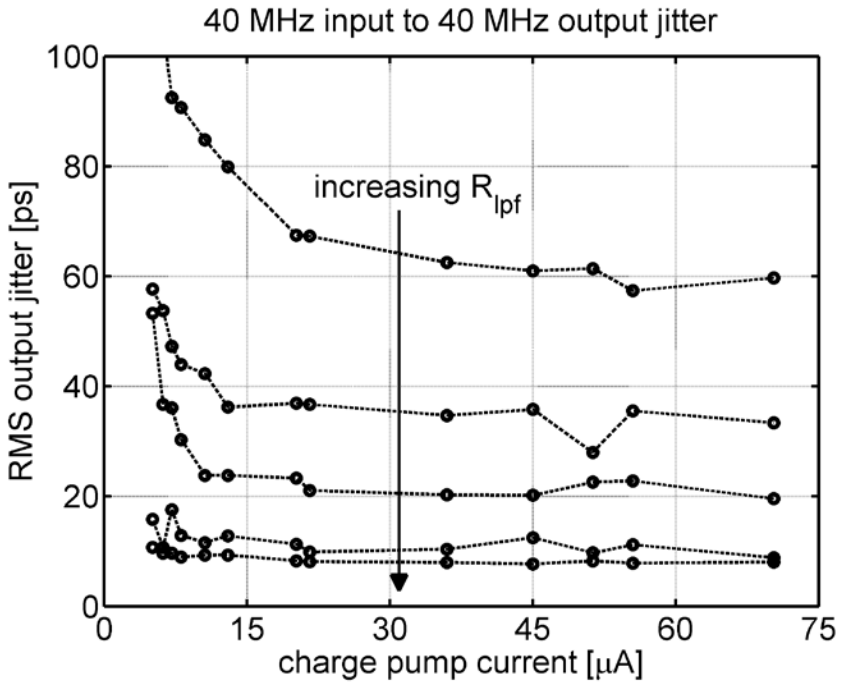
Simulation in C0 (typical VCO gain)

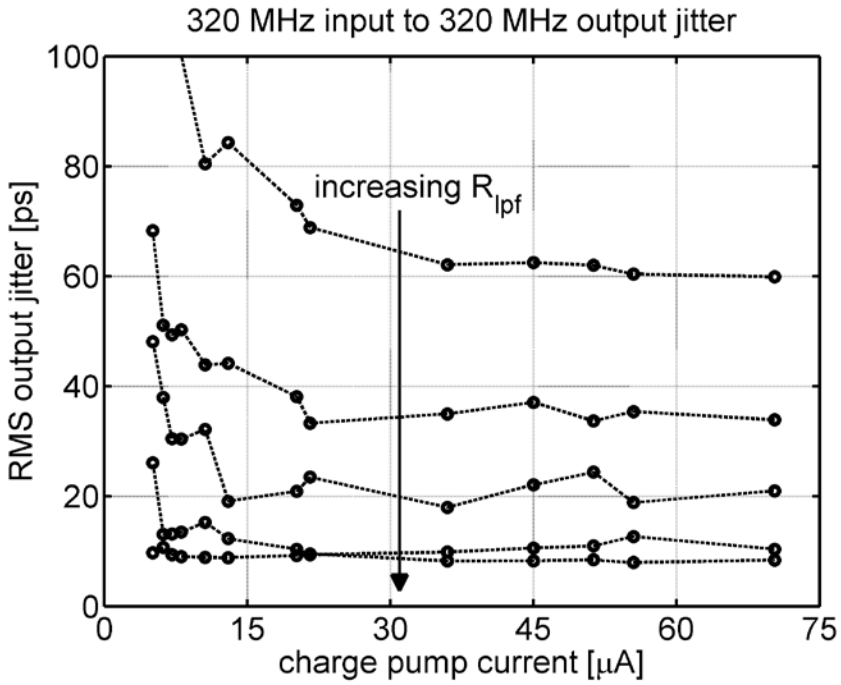




time until lock after reset: 750 ns

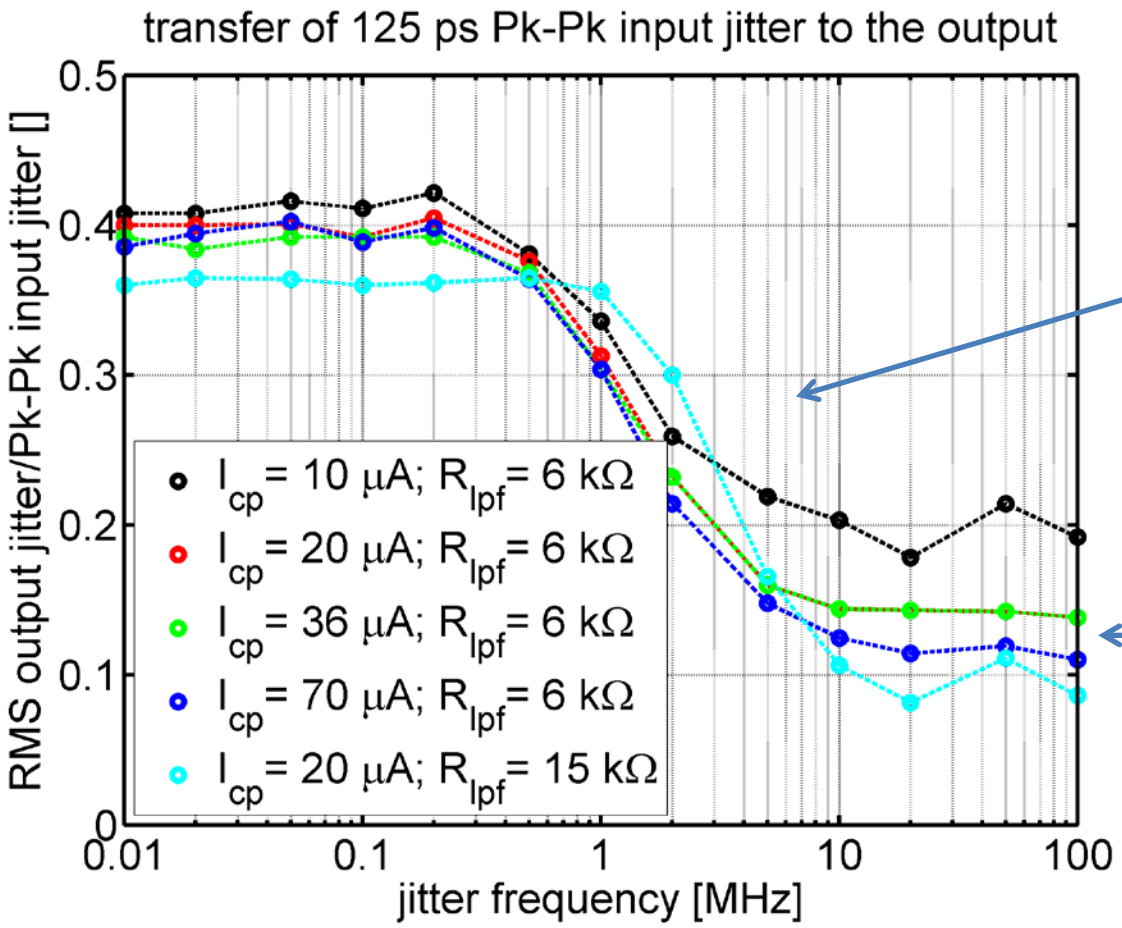
Measured output jitter





jitter values < 10 ps_{RMS} are possible

Measured jitter transfer



$$\frac{\varphi_{out}}{\varphi_{in}} = \frac{1}{M} \cdot \frac{K_D K_{VCO} F(s)}{s + \frac{K_D K_{VCO} F(s)}{N}}$$

$$= \frac{N}{M} \cdot \frac{\omega_n^2 + 2 \cdot s \cdot \zeta \omega_n}{s^2 + 2 \cdot s \cdot \zeta \omega_n + \omega_n^2}$$

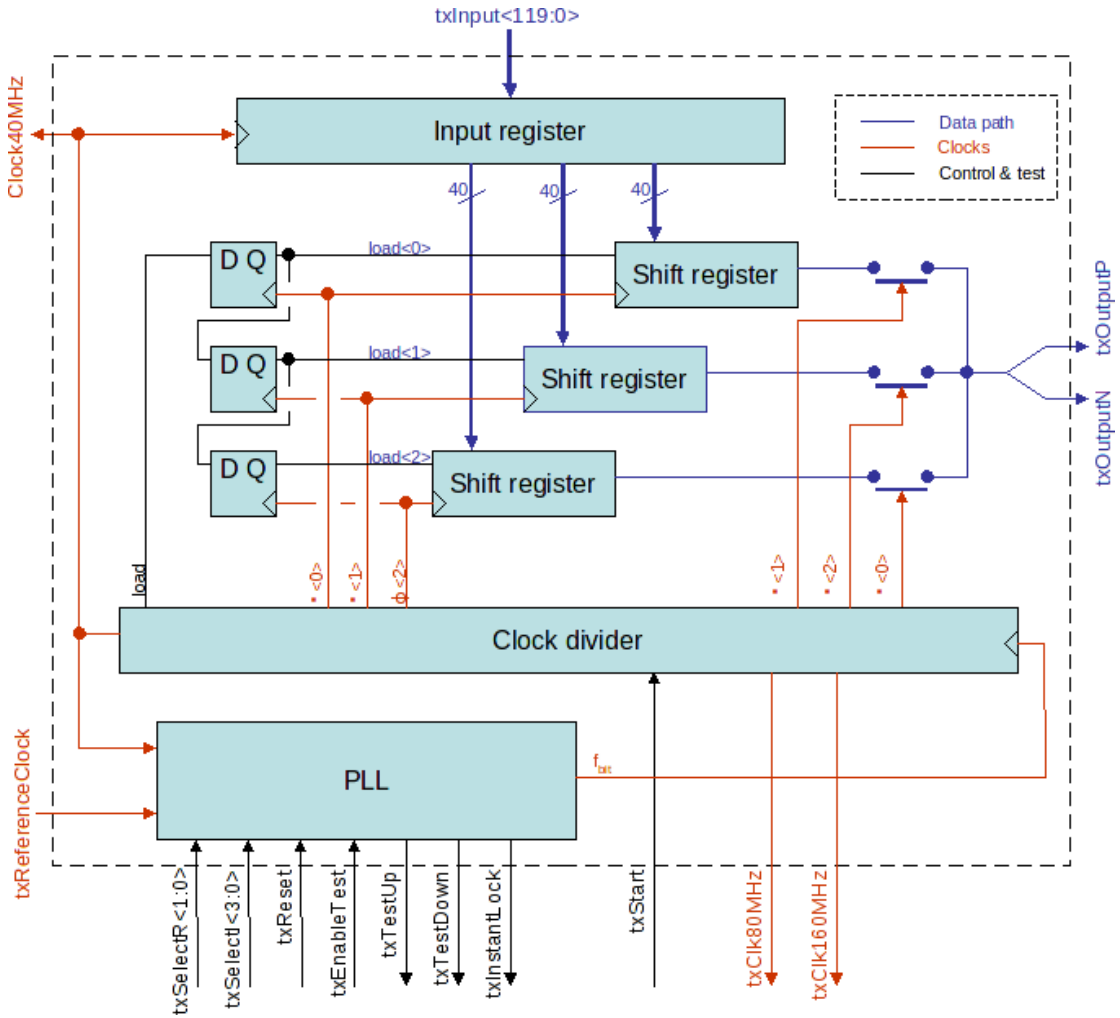
intrinsic noise of ePLL

jitter transfer = phase transfer!

Outline

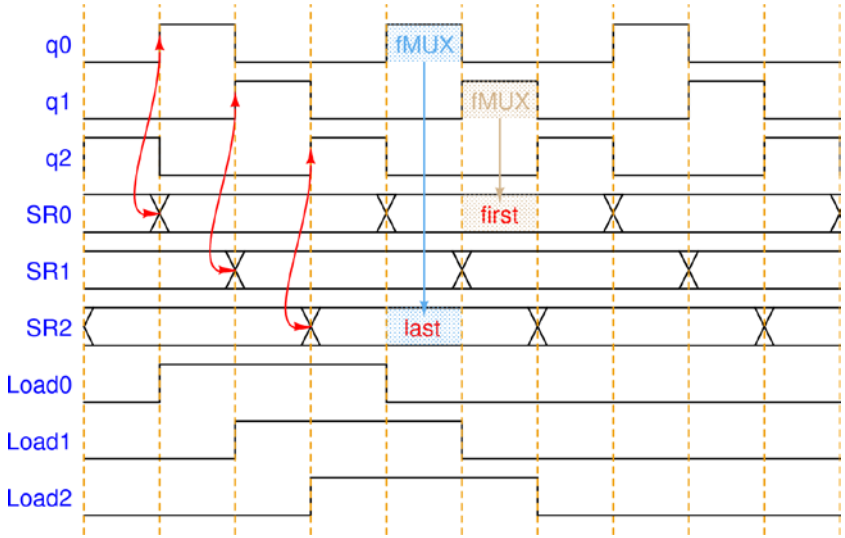
- *GBT project overview*
- *Basic PLL operation*
- *GBT ePLL*
- GBT serializer
- *GBT laser driver*

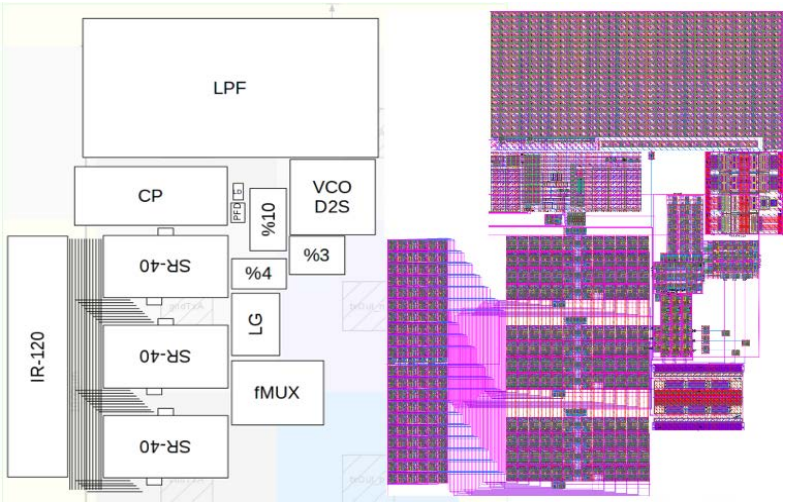
GBT serializer block diagram



- input: 120-bit word every 25 ns
- output: 4.8 Gbit/s serialized data
- PLL running at 4.8 GHz with a reference clock at 40 MHz
- 120-bit input register
- 3 40-bit shift registers clocked with 1.6 GHz clocks
- output multiplexer to combine the outputs of the 3 shift registers onto a single output
- only output multiplexer and PLL operate at full speed
- radiation-hard PLL
- triplicated clock divider
- data path is not radiation hard → FEC

Timing and layout





timing is critical for the correct operation!

→ make sure the data is correctly loaded in the shift registers before shifting out

→ make sure the output multiplexer selects a stable signal

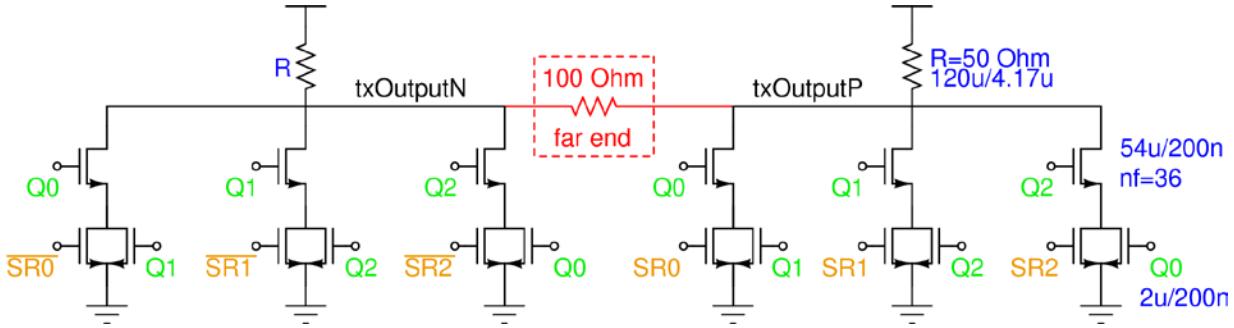
→ layout is a critical part of the design

→ symmetry

→ equal path lengths

→ equal loading

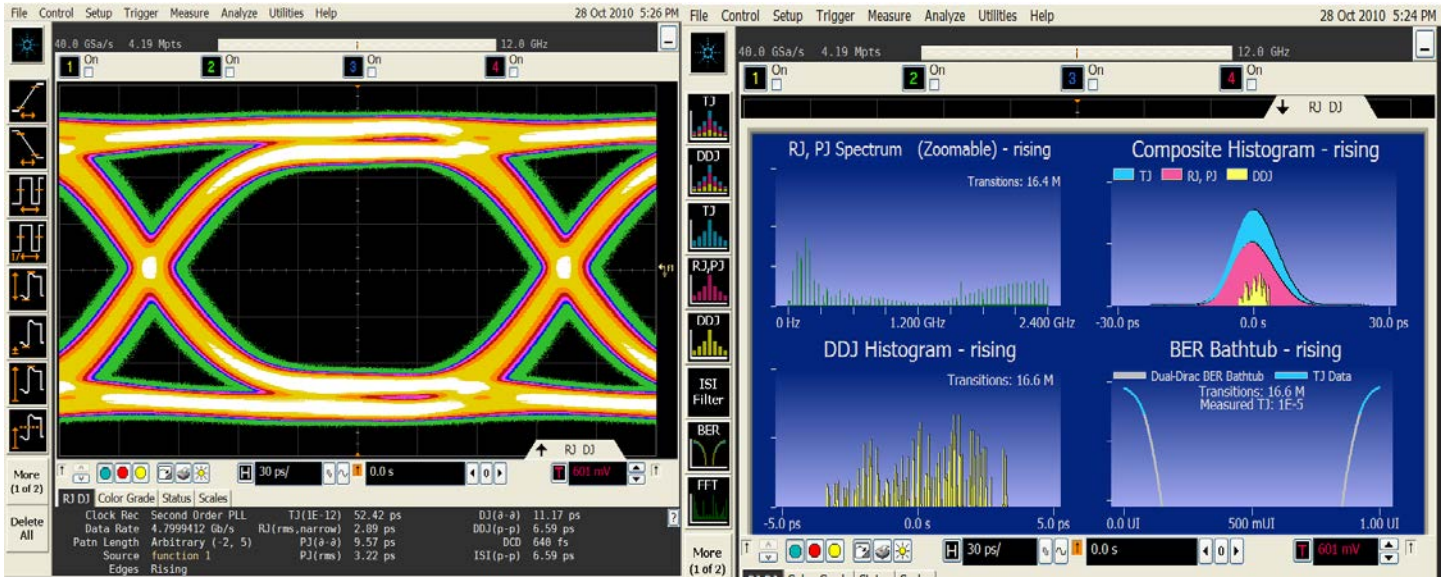
Output multiplexer



- fully differential structure
  → constant current drawn from the supply
  → no current spikes on the supply
- only nMOS transistors in the signal path → fast
- every internal node is pre-charged to ground
  → parasitic capacitance at the output nodes is independent on the SR signals
  → no pattern dependent jitter
- 50 Ω resistors as pull-up network instead of pMOS counterpart
  → intrinsic back termination
  → shift registers only need to drive (small) nMOS transistors

Measurement results

measurement at 4.8 Gbit/s with GBT frame



jitter decomposition:

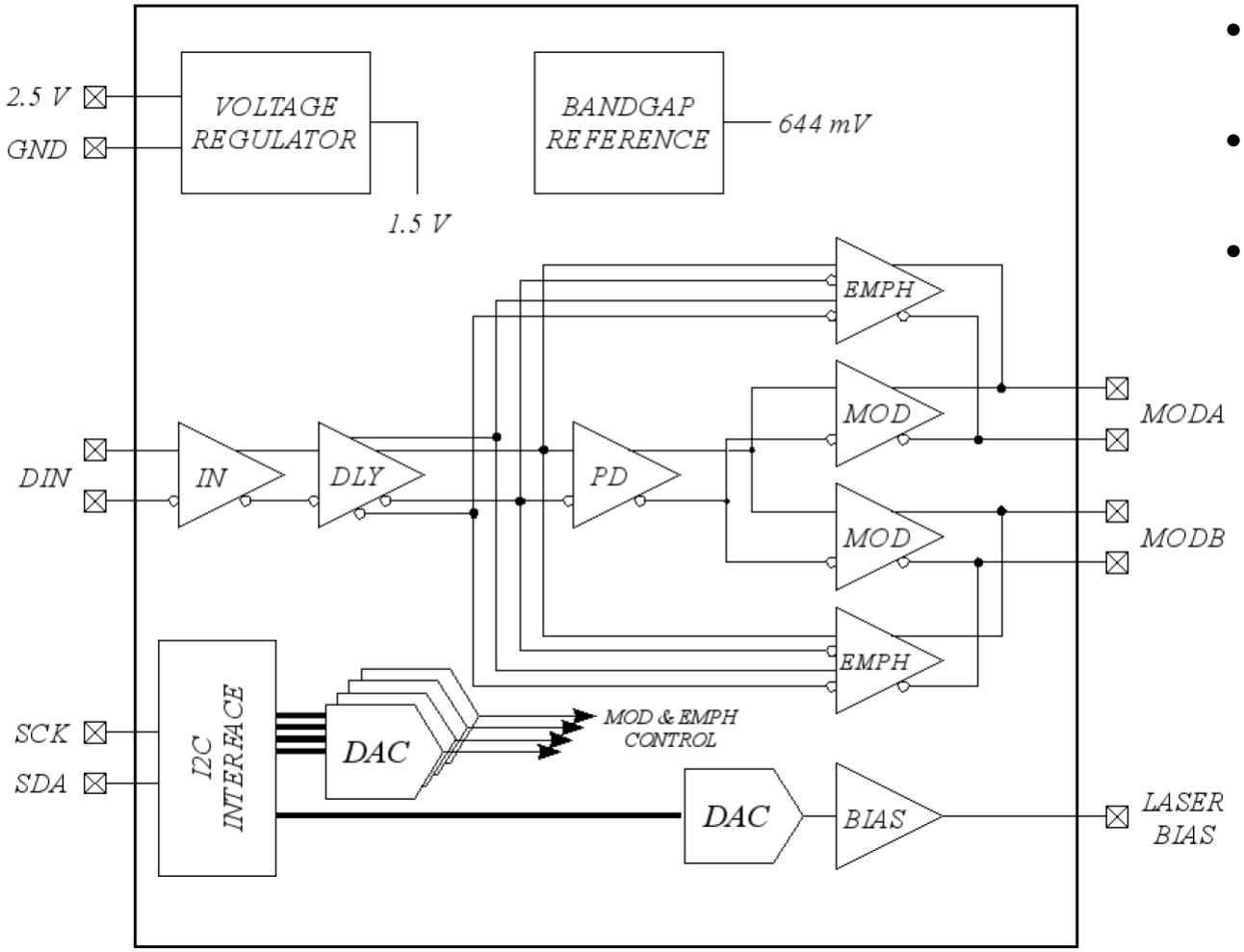
- random jitter
- periodic jitter
- deterministic jitter (duty-cycle distortion, DDJ, ISI)

Outline

- *GBT project overview*
- *Basic PLL operation*
- *GBT ePLL*
- *GBT serializer*
- GBT laser driver

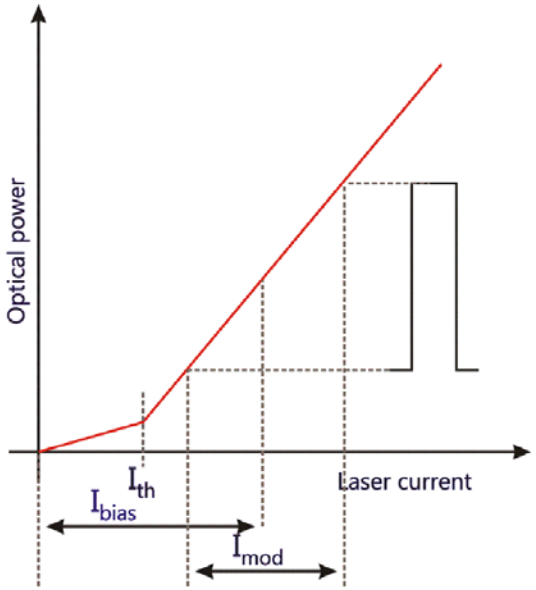
GBLD overview

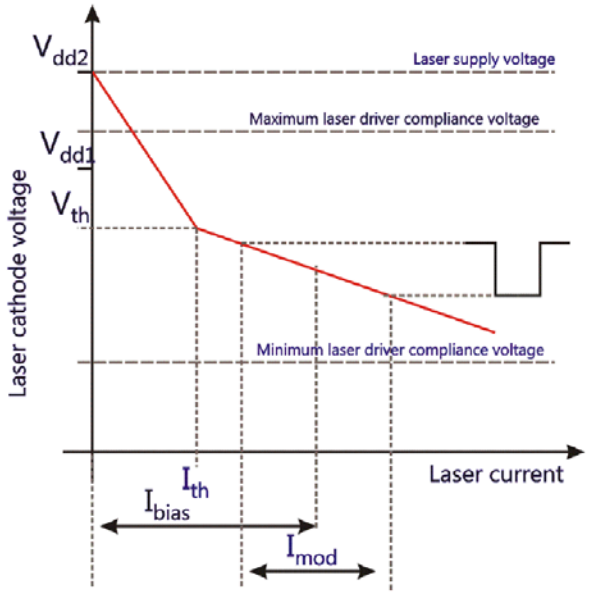
GBLD: 5 Gbit/s laser driver to drive VCSELs as well as edge-emitting lasers

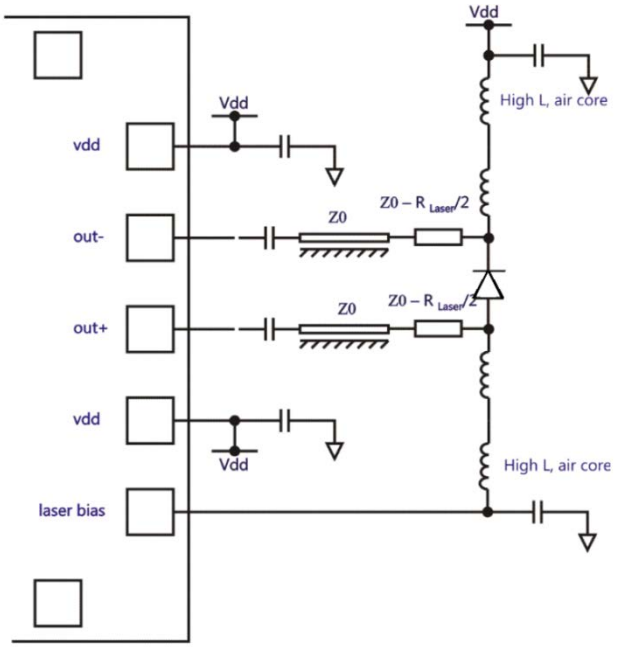


- programmable modulation current (2-24 mA)
- programmable emphasis current (±0-12 mA)
- programmable laser bias current (2-43 mA)

Laser bias and modulation



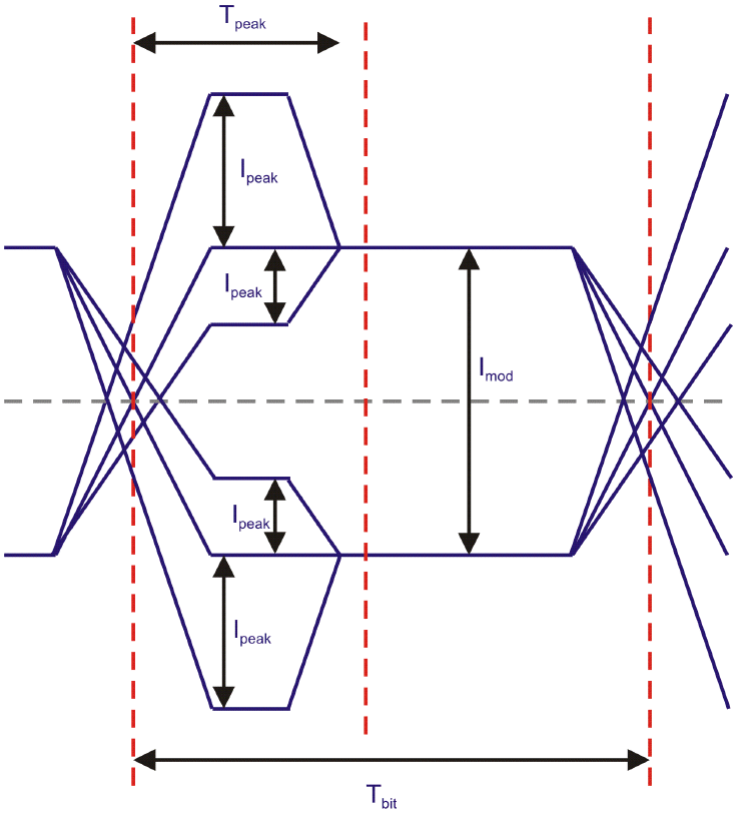




- minimal current always above threshold
- VCSEL: small bias and modulation current
- edge-emitting laser: large bias and modulation current
- large voltage drop over laser → laser bias circuit must be able to cope with this

- chokes for the bias current
- AC-coupling for modulation current
- matching resistors to match the laser dynamic impedance to the transmission line

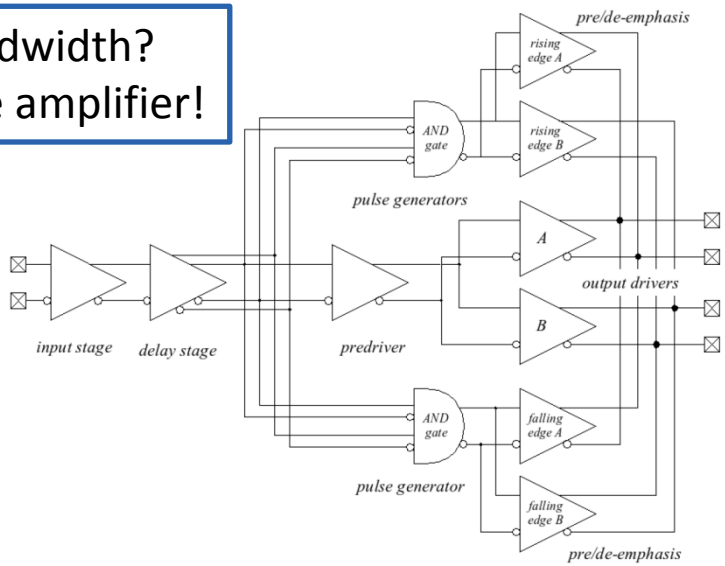
Pre-emphasis and de-emphasis

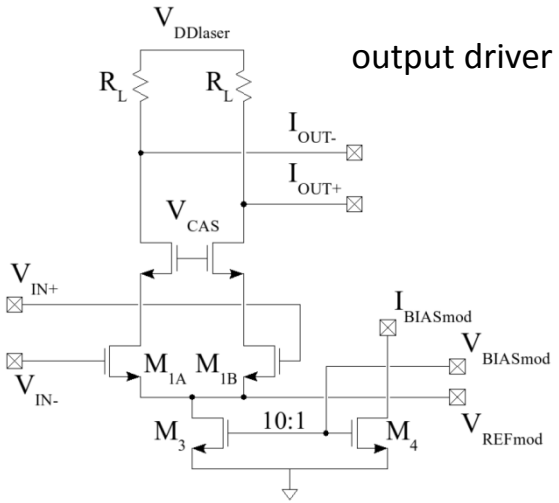


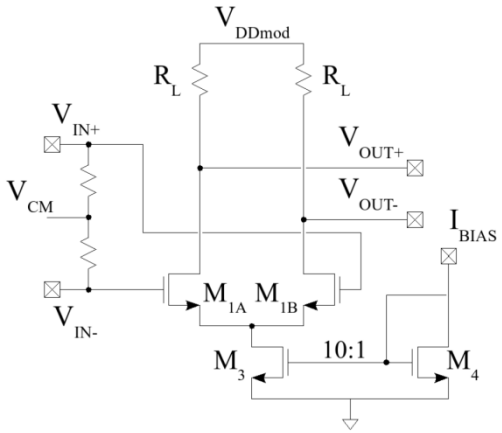
- pre-emphasis: reduce rise and fall time, compensate for unforeseen parasitic capacitances
- de-emphasis: increase rise and fall time, basically never used here
- emphasis duration generated by means of an on-chip delay line

The modulator

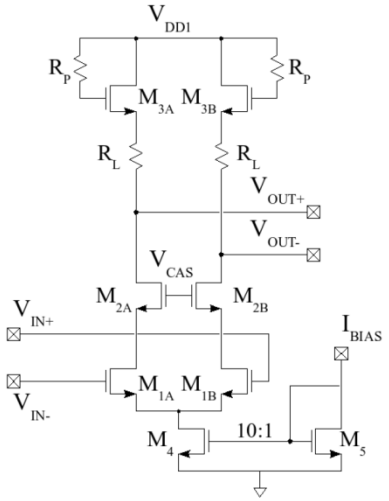
gain and bandwidth?
→ multistage amplifier!



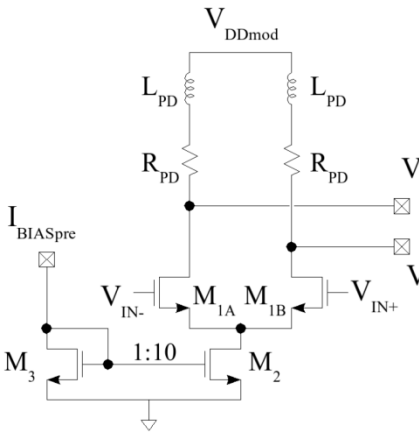




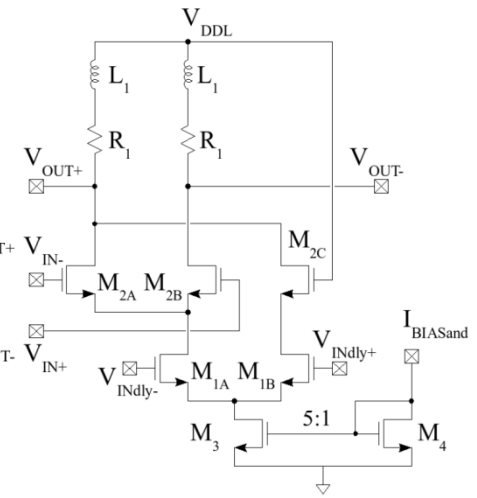
input stage



gain stage

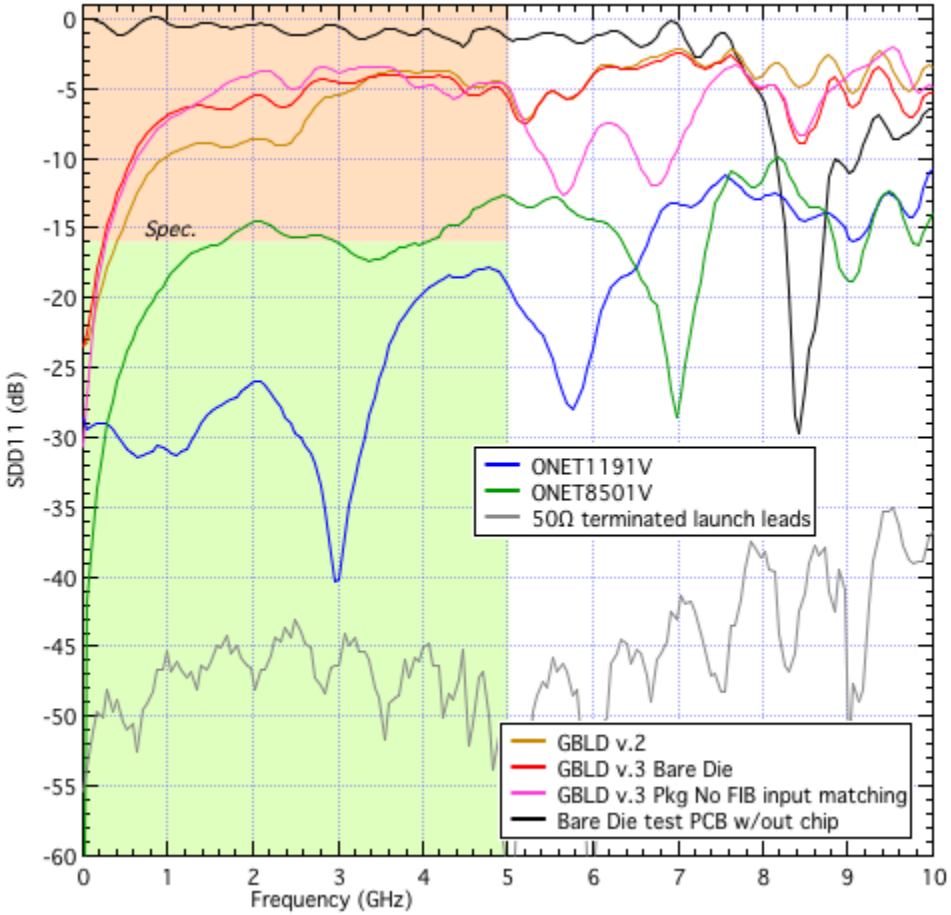


predriver



AND gate

Input return loss for the GBLD



$$RL = -20 \cdot \log\left(\frac{Z_L - Z_S}{Z_L + Z_S}\right)$$

on-chip termination resistor
is in parallel with a relatively large capacitance originating from the ESD devices and the input stage

↓

the termination becomes a short at high frequencies

↓

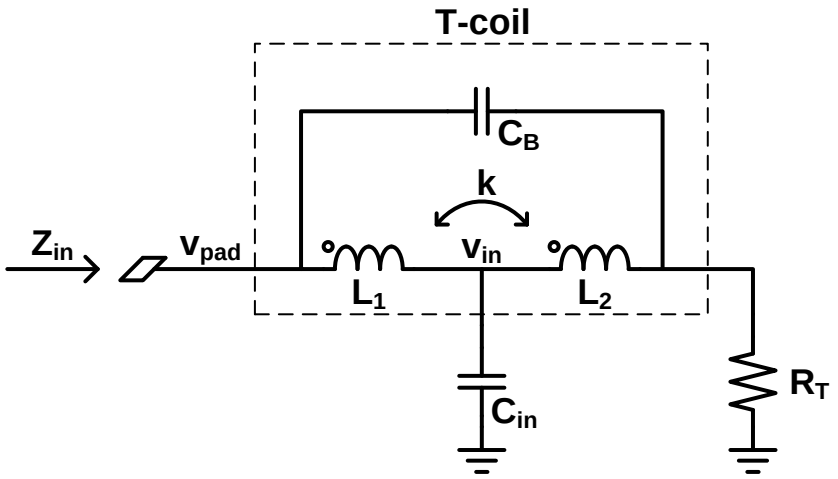
return loss does not fulfill the specification (> 16 dB)

↓

place a T-coil to separate the capacitance from the resistance

[S. Galal and B. Razavi, 'Broadband ESD Protection Circuits in CMOS Technology', *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2334-2340, December 2003]

The concept of a T-coil

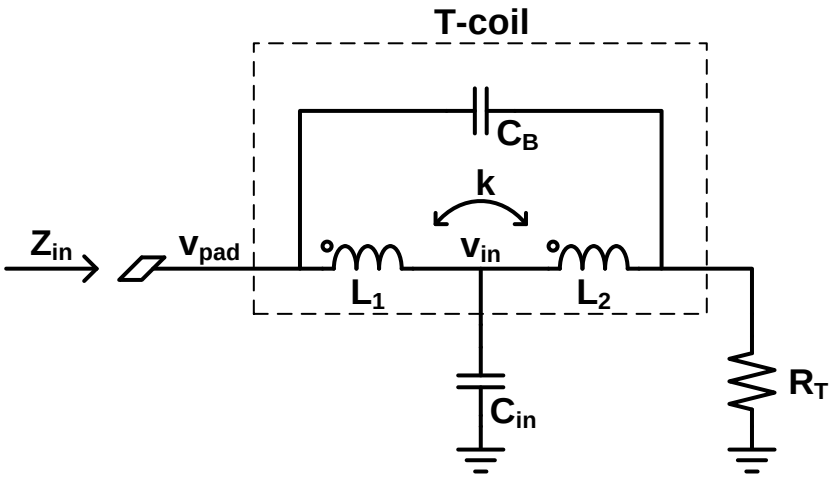


- At very low frequencies: $Z_{in} = R_T$ because the inductors act as a short
- At very high frequencies: $Z_{in} = R_T$ because C_B acts as a short
- By properly choosing L_1, L_2, k and C_B, $Z_{in} = R_T$ can be guaranteed for all intermediate frequencies.
- C_{in} (including the ESD capacitance) never influences the overall input impedance so that the return loss ideally is infinite.

T-coil input impedance

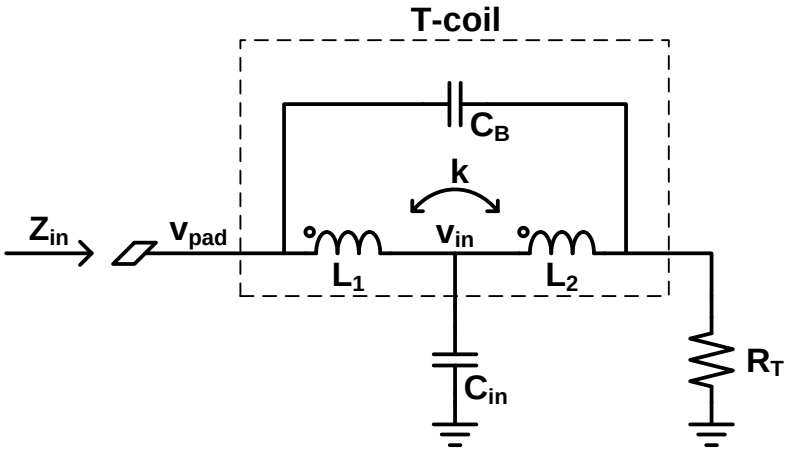
$$1+s\cdot\left(\frac{L_1+L_2+2k\sqrt{L_1L_2}}{R_T}\right)+s^2\cdot\left(C_B\left(L_1+L_2+2k\sqrt{L_1L_2}\right)+C_{in}L_1\right)$$

$$Z_{in}=R_T\cdot\frac{+s^3\cdot\frac{C_{in}L_1L_2}{R_T}\left(1-k^2\right)+s^4\cdot C_BC_{in}L_1L_2\left(1-k^2\right)}{1+s\cdot R_TC_{in}+s^2\cdot\left(C_B\left(L_1+L_2+2k\sqrt{L_1L_2}\right)+C_{in}L_2\right)+s^3\cdot R_TC_BC_{in}\left(L_1+L_2+2k\sqrt{L_1L_2}\right)+s^4\cdot C_BC_{in}L_1L_2\left(1-k^2\right)}$$



$$Z_{in}=R_T\Leftrightarrow\begin{cases}L_1=L_2\\ L_1=\dfrac{R_TC_{in}}{2\left(1+k\right)}\\ C_B=\dfrac{C_{in}}{4}\dfrac{1-k^2}{\left(1+k\right)^2}\end{cases}\rightarrow \text{choose } L_1 \text{ or } k$$

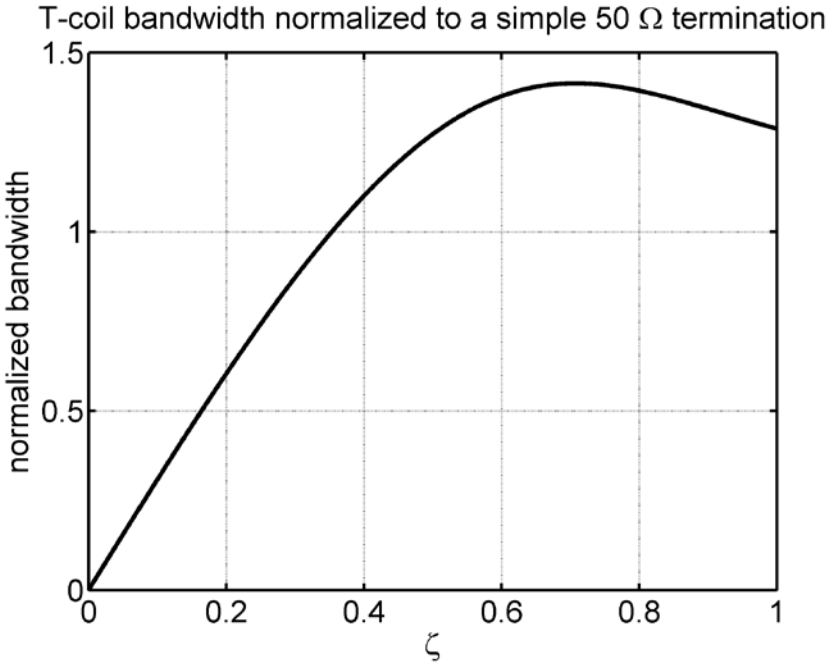
T-coil transfer function



$$\frac{v_{in}}{v_{pad}} = \frac{1}{1 + s \cdot \frac{R_T C_{in}}{2} + s^2 \cdot \frac{R_T^2 C_{in}^2}{4} \cdot \frac{1-k}{1+k}}$$

$$= \frac{\omega_n^2}{\omega_n^2 + 2\zeta\omega_n \cdot s + s^2}$$

$$\text{where} \begin{cases} \omega_n = \frac{2}{R_T C_{in}} \cdot \sqrt{\frac{1+k}{1-k}} \\ \zeta = \frac{1}{2} \cdot \sqrt{\frac{1+k}{1-k}} \end{cases}$$

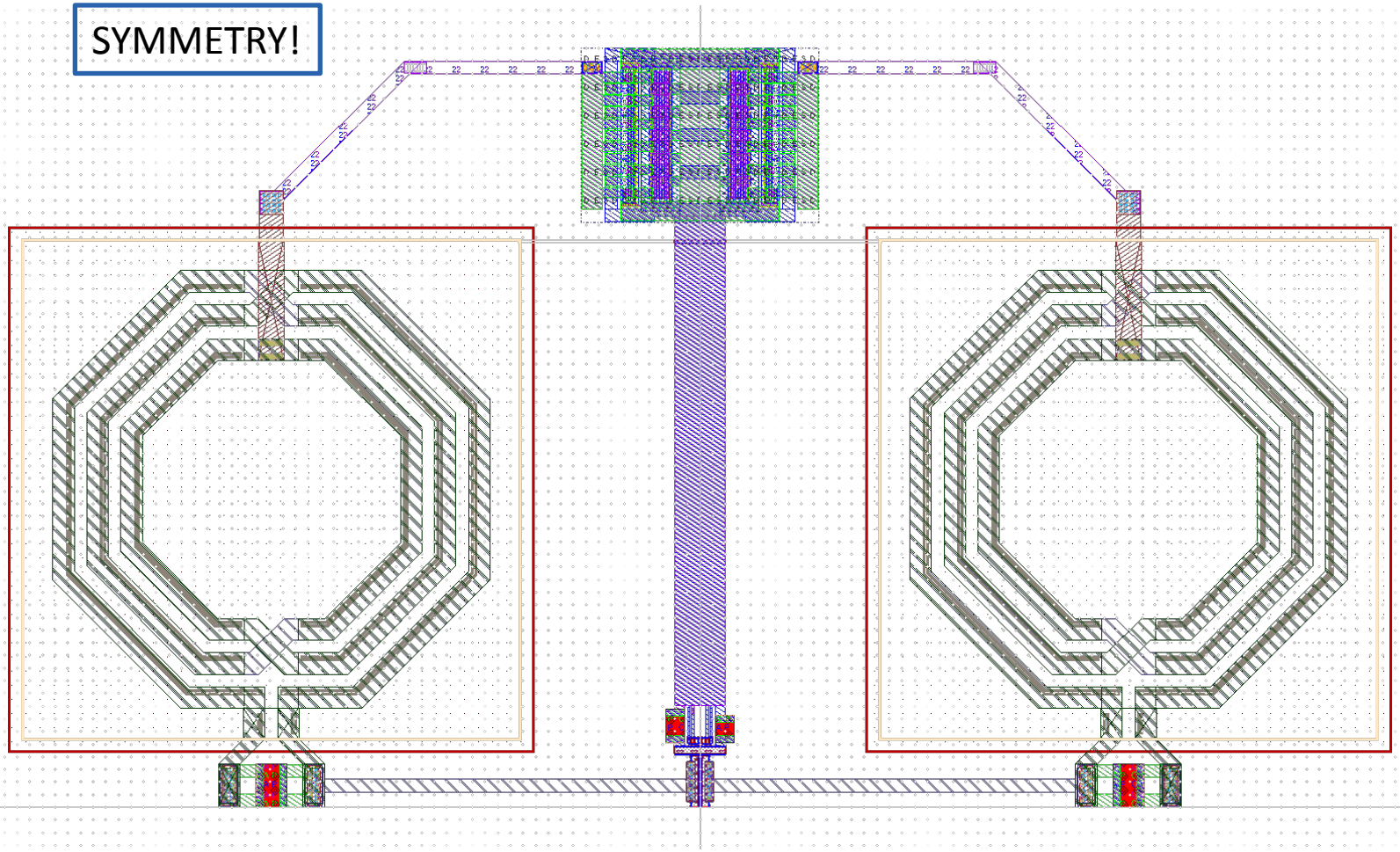


$\zeta = 0.7$ for maximum bandwidth

$\zeta = \frac{\sqrt{3}}{2} \approx 0.866$ for uniform group delay

Layout

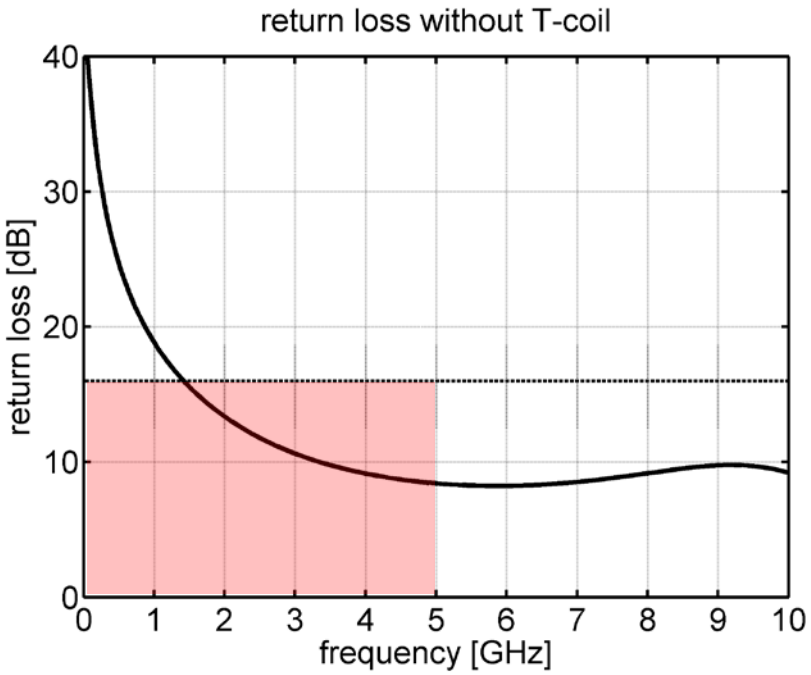
SYMMETRY!



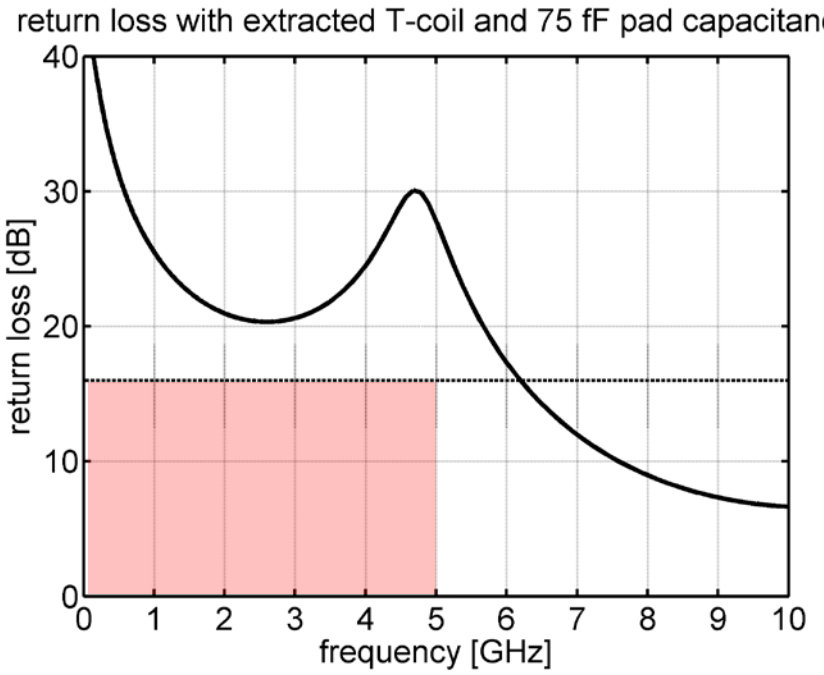
area = 550 µm x 300 µm

Return loss improvement simulation

before

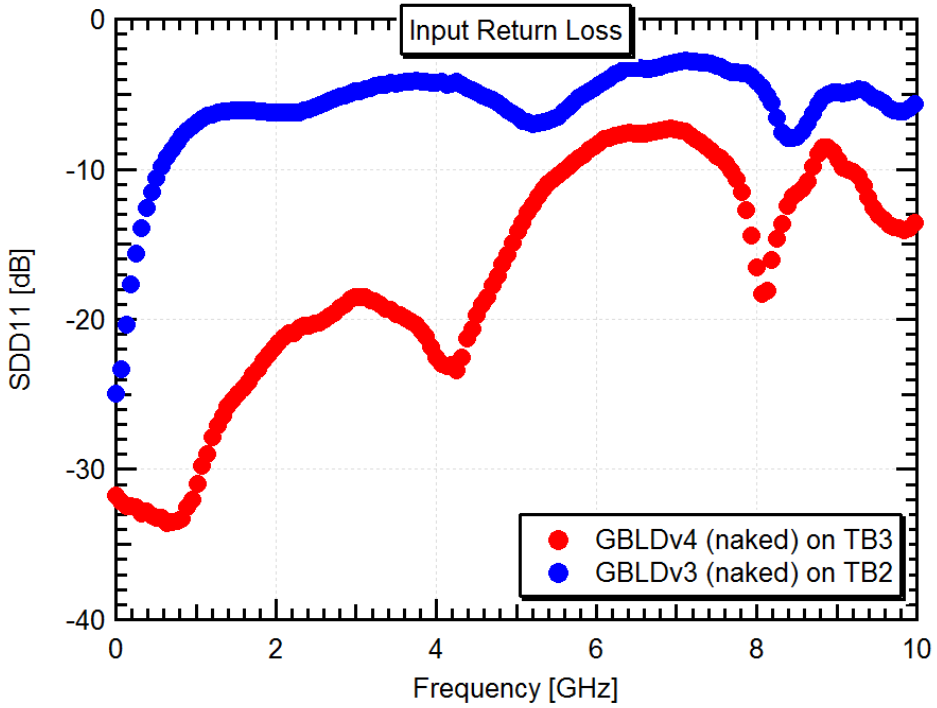


after



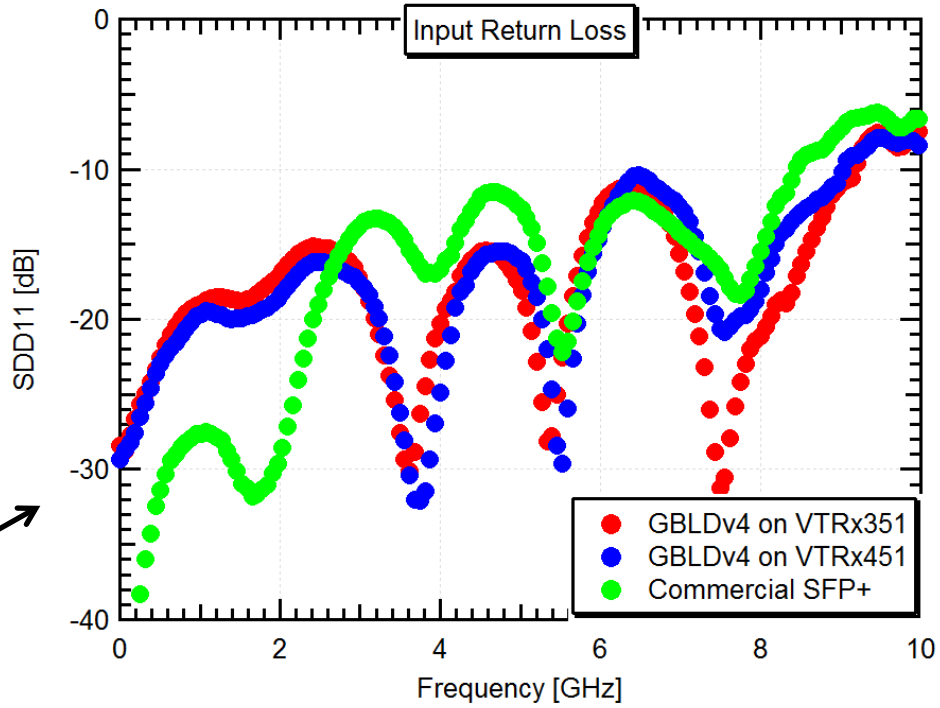
→ specification of 16 dB return loss cannot be met without a T-coil

Return loss measurements



compared with GBLD v3 on the testboard

compared with a commercial device on the VTRx



Acknowledgements

in alphabetical order:

- Özgür Çobanoğlu
- Gianni Mazza
- Paulo Moreira
- Karolina Poltorak
- Csaba Soos
- Jan Troska