Discriminator design

Angelo Rivetti
INFN-Sezione di Torino
rivetti@to.infn.it

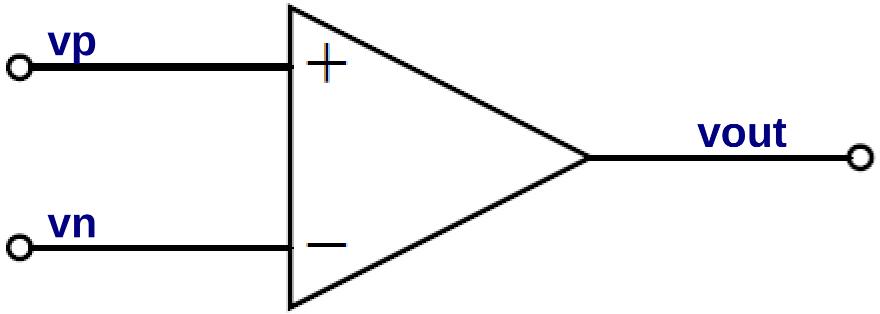
Comparator generals

- A comparator discriminates a good event against noise
- Comparators are particularly critical in timing systems

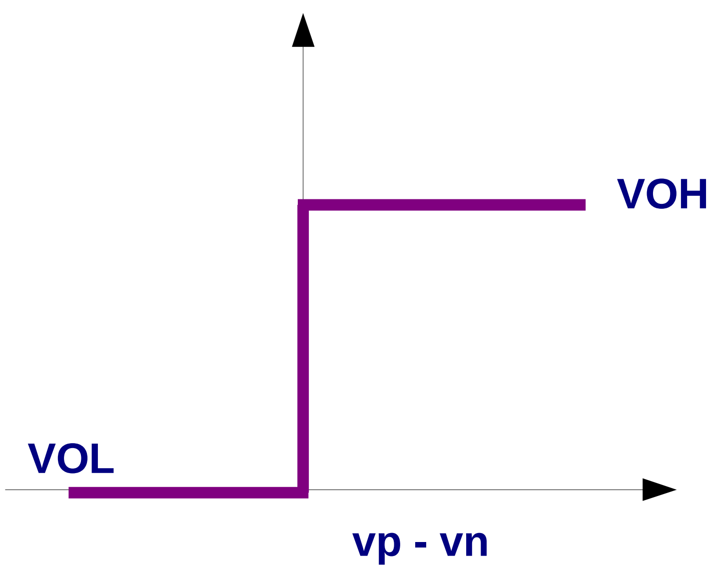
- Type of comparators:
  - General purpose, low power leading edge
  - Fast (multi-stage) leading edge
  - Latched comparators
  - Timing comparators
    - Zero crossing
    - Constant Fraction

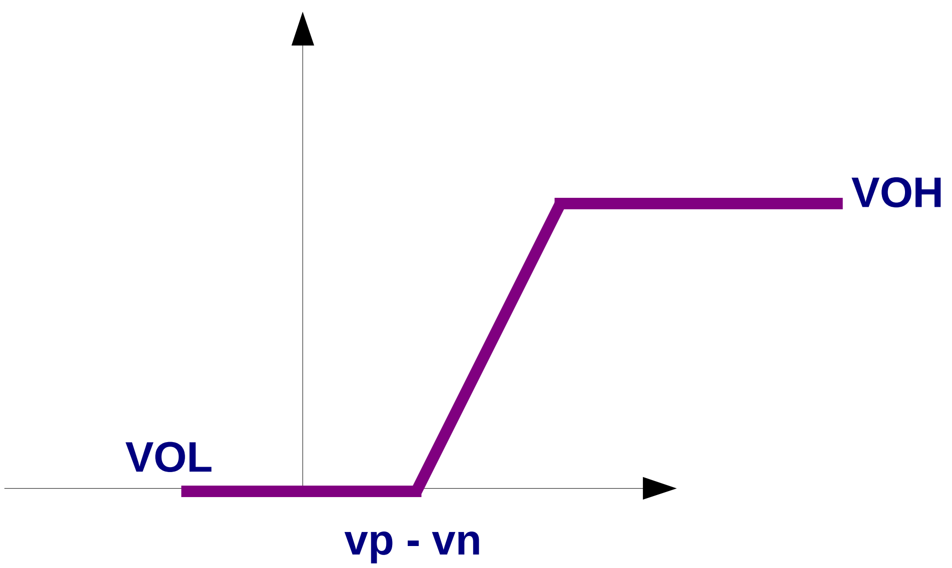
Leading edge discriminators

- High gain, open-loop, differential amplifiers.
- Essential elements also of the more complex zero-crossing and CFD discriminators.
- Should generate logic valid signal from a difference between the inputs as small as possible.

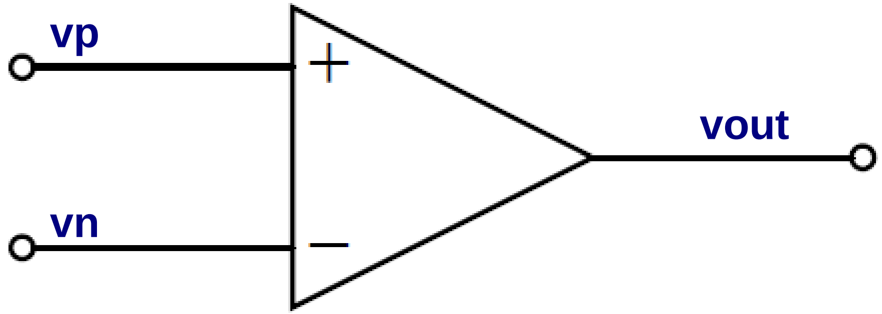


- Offset is due to transistor mismatch always affect discriminators (effective threshold change)
- Offset need to be corrected for. Very often this is achieved with Digital to Analog (DAC) converters.
- Propagation delay: time needed for the output to reach 50% measured with respect to the threshold crossing.





Discriminator propagation delay



$$A(s) = \frac{A_0}{(1 + s\tau_p)}$$

$$\frac{V_{OH} - V_{OL}}{2} = V_{in(min)} A_0 (1 - e^{-\frac{t_d}{\tau_p}})$$

$$V_{in(min)} = \frac{V_{OH} - V_{OL}}{A_0}$$

$$\frac{V_{OH} - V_{OL}}{2} = \frac{V_{OH} - V_{OL}}{A_0} A_0 (1 - e^{-\frac{t_d}{\tau_p}})$$

$$t_d = 0.693\tau_p$$

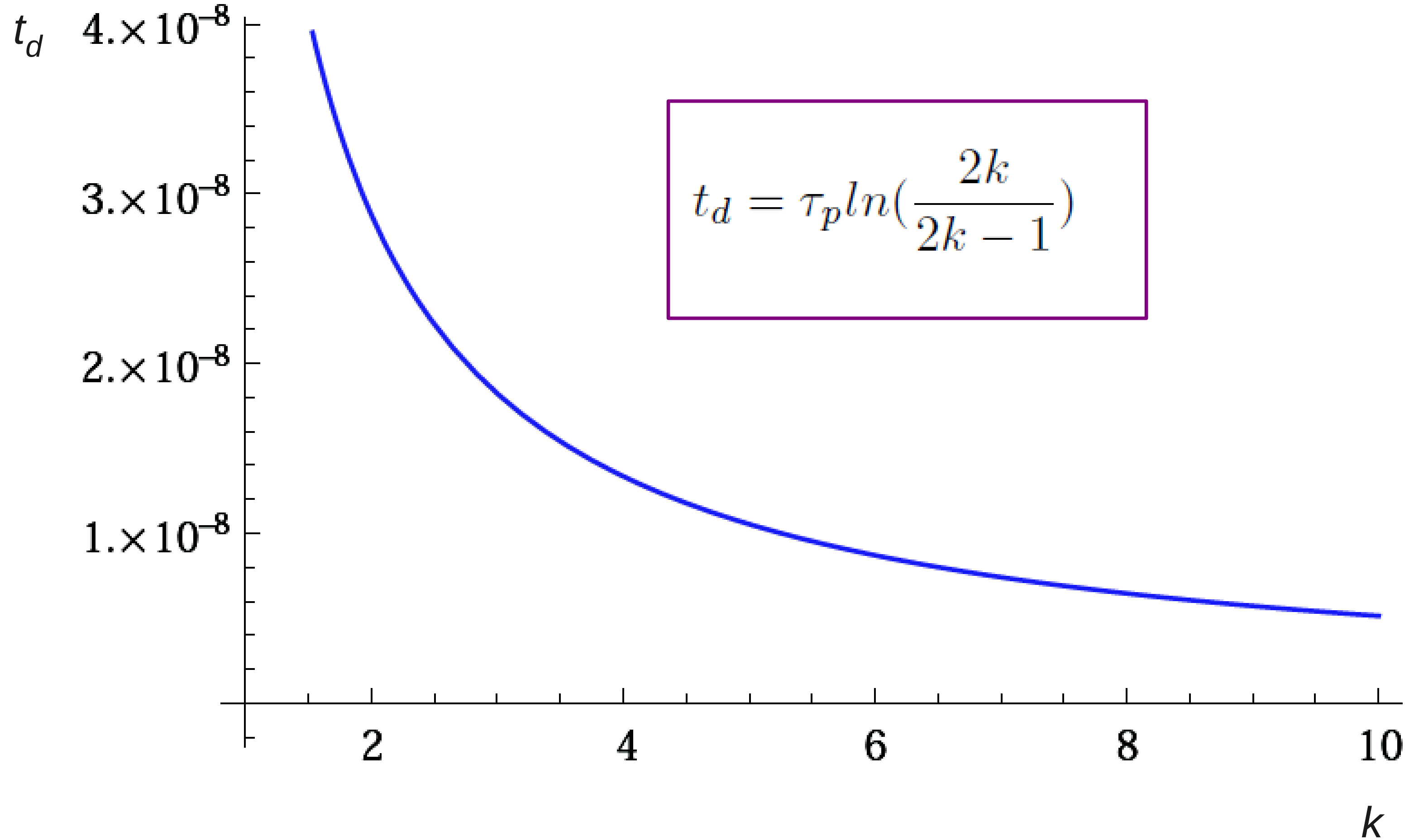
$$\frac{V_{OH} - V_{OL}}{2} = k V_{in(min)} A_0 (1 - e^{-\frac{t_d}{\tau_p}})$$

$$t_d = \tau_p ln(\frac{2k}{2k-1})$$

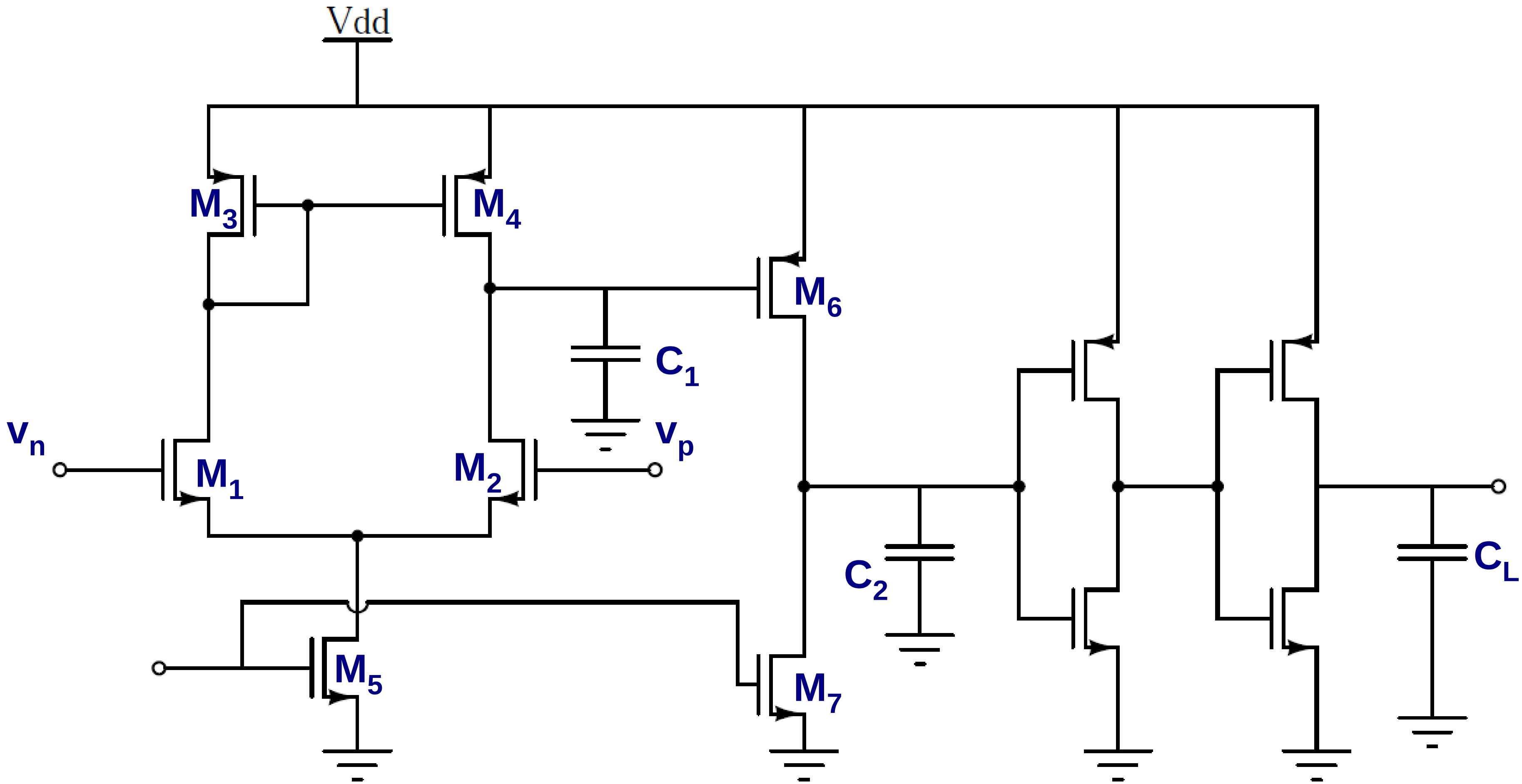
k=ratio between actual and minimum signal

Discriminator propagation delay

- Propagation delay versus the ratio between the actual and the minimum detectable signal for τ_P=100 ns.

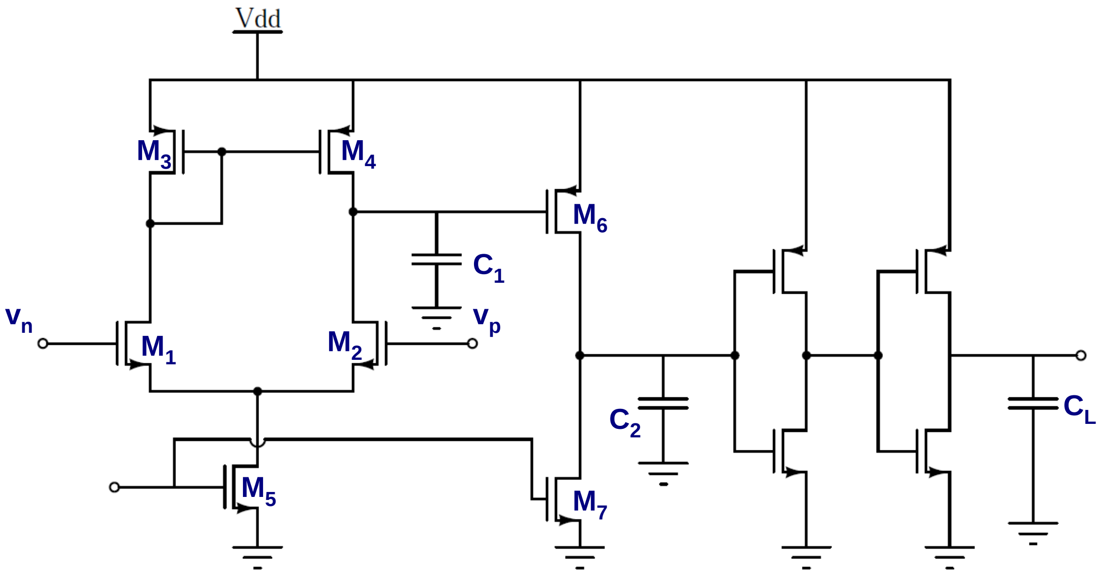


Two stage CMOS comparator



- **Compact design.**
- **A chain of inverters generates full swing digital output signals.**
- **Very popular when not very high speed is demanded.**
- **Several variants exist**

Two stage comp: small signal performance



$$\tau_1 = C_1 \frac{1}{g_{ds2} + g_{ds4}}$$

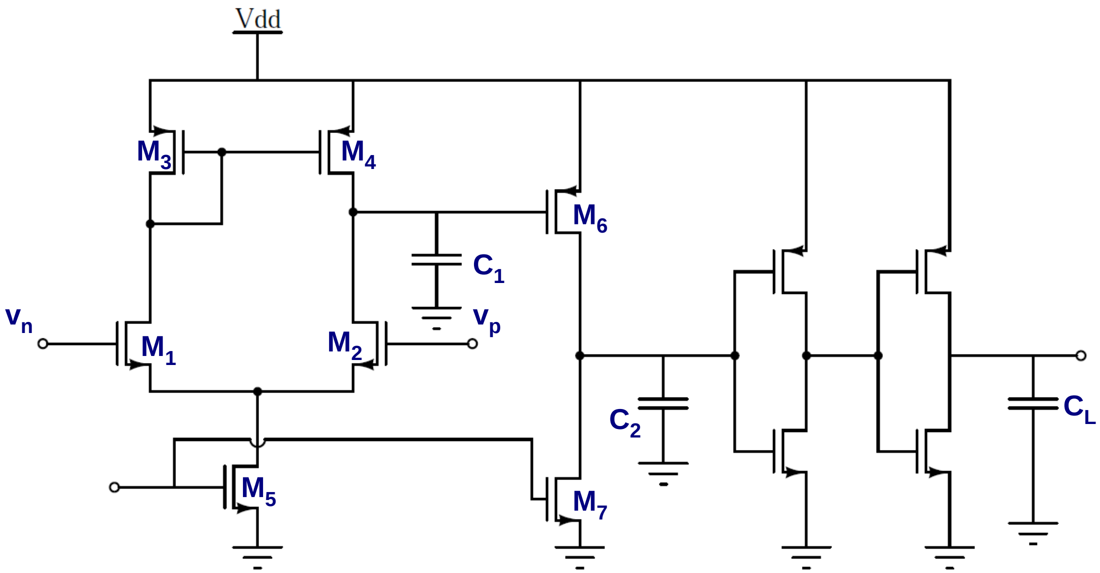
$$\tau_2 = C_2 \frac{1}{g_{ds6} + g_{ds7}}$$

$$A_0 = \left(\frac{g_{m1}}{g_{ds2} + g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6} + g_{ds7}}\right)$$

$$A(s) = \frac{A_0}{(1 + s\tau_1)(1 + s\tau_2)}$$

$$v_{out}(t) = A_0 V_{in}\left(1 - \frac{\tau_1 e^{-\frac{t}{\tau_1}}}{\tau_1 - \tau_2} + \frac{\tau_2 e^{-\frac{t}{\tau_2}}}{\tau_1 - \tau_2}\right)$$

Two stage comparator: slew rate limitation



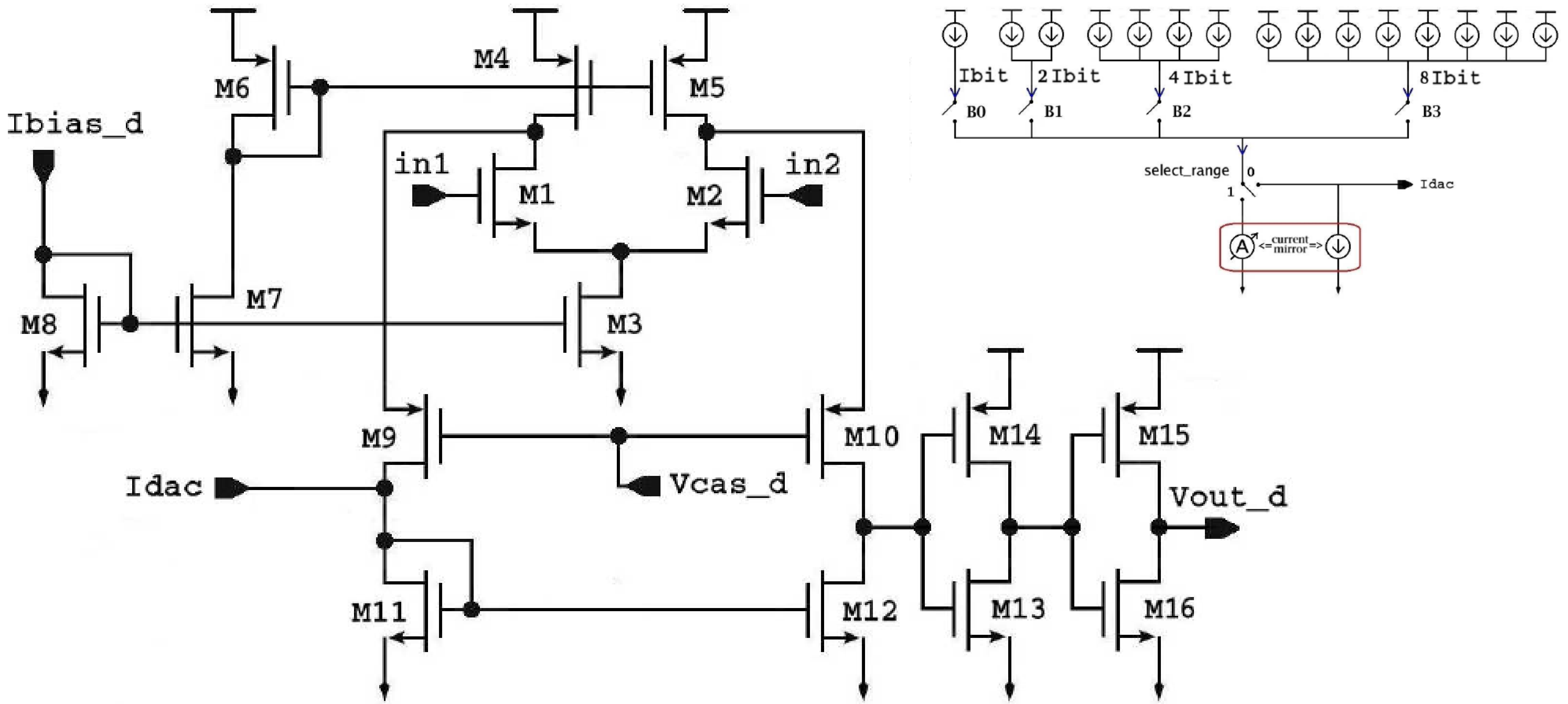
$$SR^+ = \frac{I_6 - I_7}{C_2}$$

$$SR^- = \frac{I_7}{C_2}$$

$$v_{out}(t) = A_0 V_{in}\left(1 - \frac{\tau_1 e^{-\frac{t}{\tau_1}}}{\tau_1 - \tau_2} + \frac{\tau_2 e^{-\frac{t}{\tau_2}}}{\tau_1 - \tau_2}\right)$$

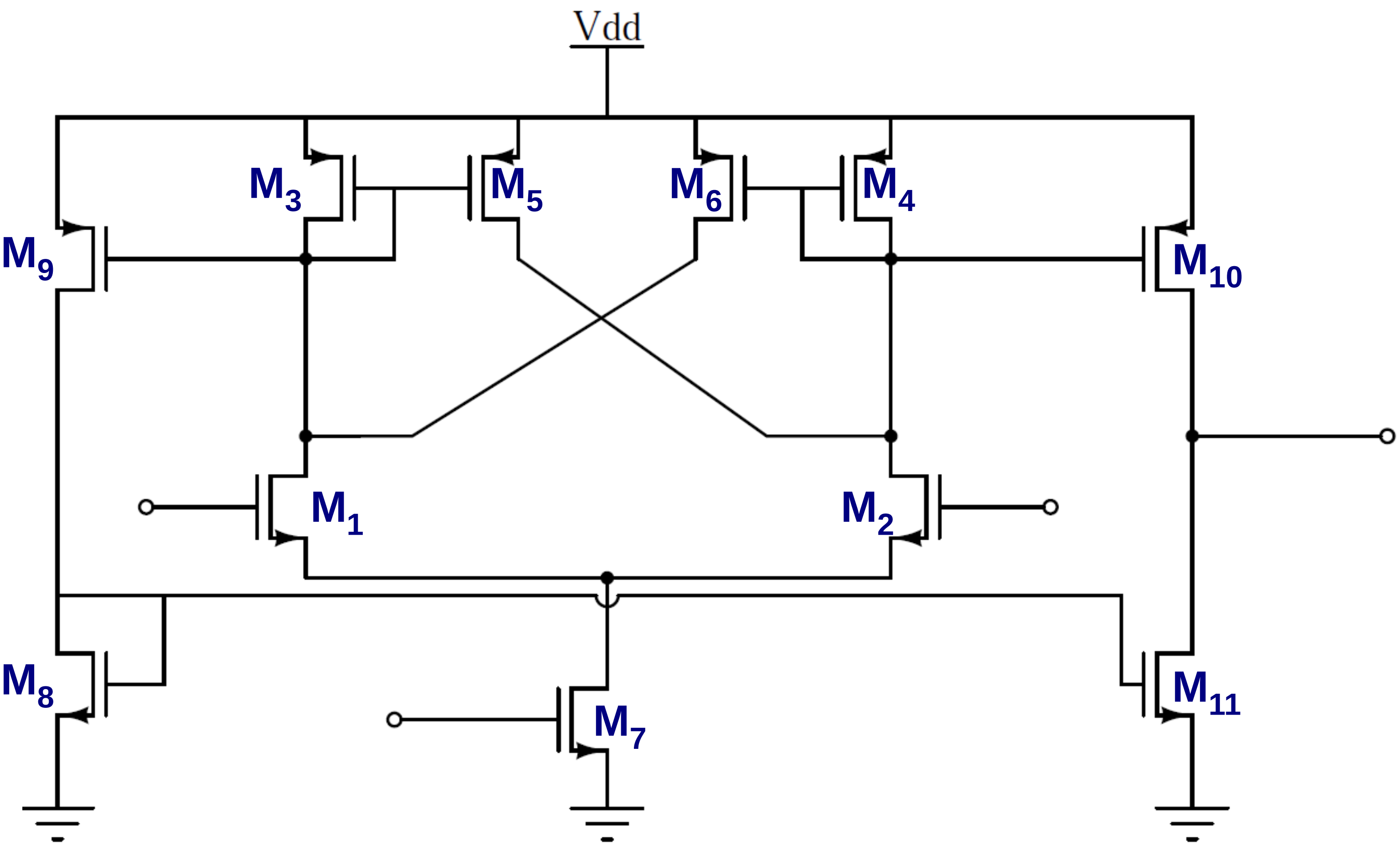
- **If the slope of the small signal step response exceeds the SR+ or SR-, the circuit becomes slew rate limited and the output is a ramp with the slope defined by SR^+ and SR^-**

Implementation example



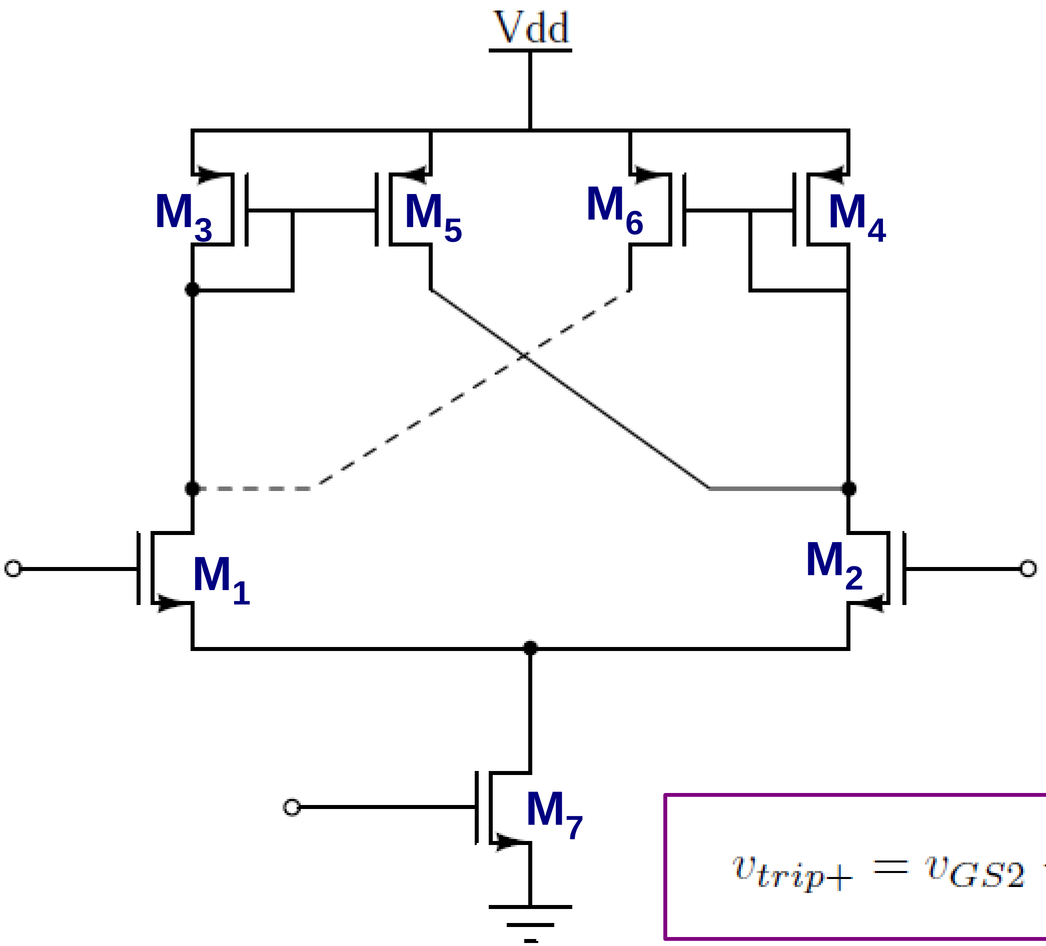
- The folding cascode topology allows to use only NMOS transistors where speed is critical
- Second stage is already an inverter.
- Current mode DAC to control the threshold.

Comparator with hysteresis



- Hysteresis implies a **positive feed-back** into the circuit.
- M5 and M6 provides the positive feed-back which is **regulated by sizing** M5 and M6 w.r.t M3 M4
- Hysteresis avoids **multiple bouncing** near the threshold point.

Trip point calculation



$$i_5 = \frac{(W/L)_5}{(W/L)_3}$$

$$i_2 = i_5 \qquad i_7 = i_2 + i_1$$

$$= i_1 = \frac{i_7}{1 + [(W/L)_5/(W/L)_3]}$$

$$v_{GS1} = \sqrt{(\frac{2i_1}{\beta_1})} + V_{TH1}$$

$$v_{trip+} = v_{GS2} - v_{GS1}$$

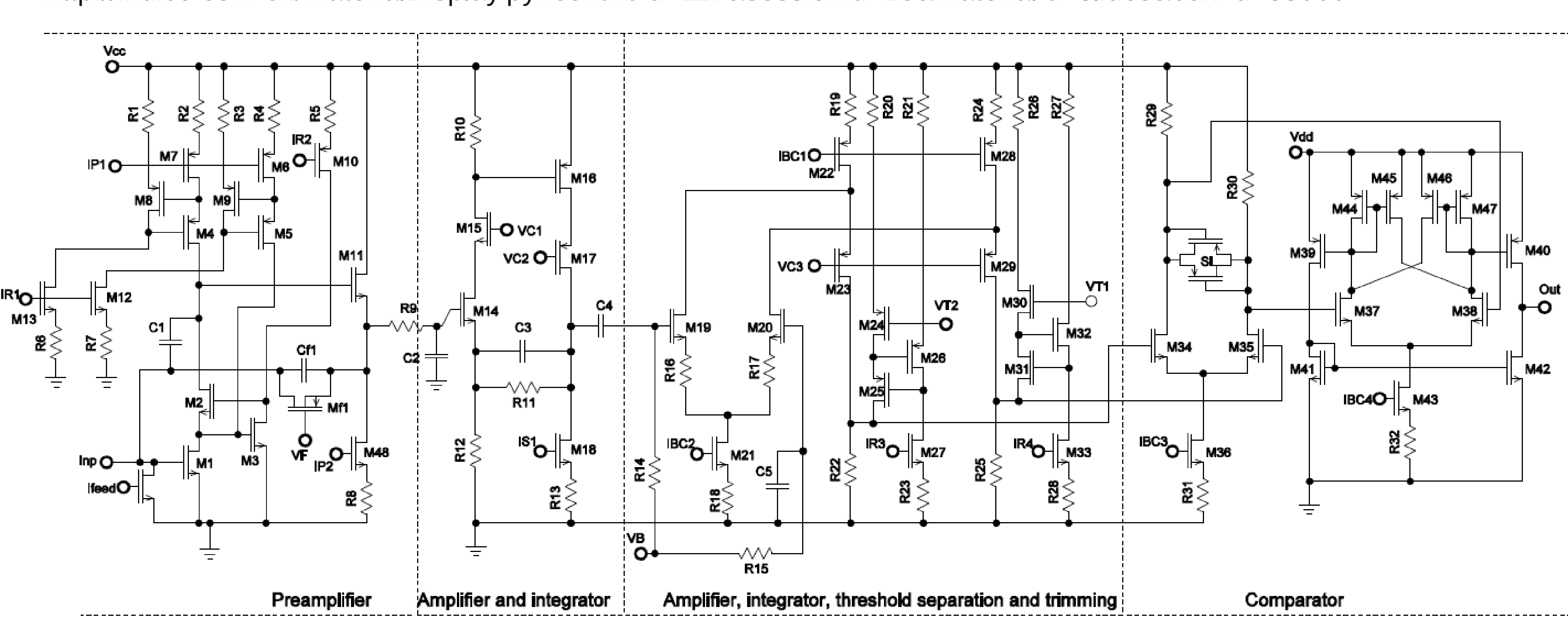
$$v_{GS2} = \sqrt{(\frac{2i_2}{\beta_2})} + V_{TH2}$$

- **Comparator flips when current in M5 and M2 are equal (signal on gate of M2 going upwards) or when the current in M1 and M6 are equal (signal on gate of M2 going downwards**

Multistage comparators

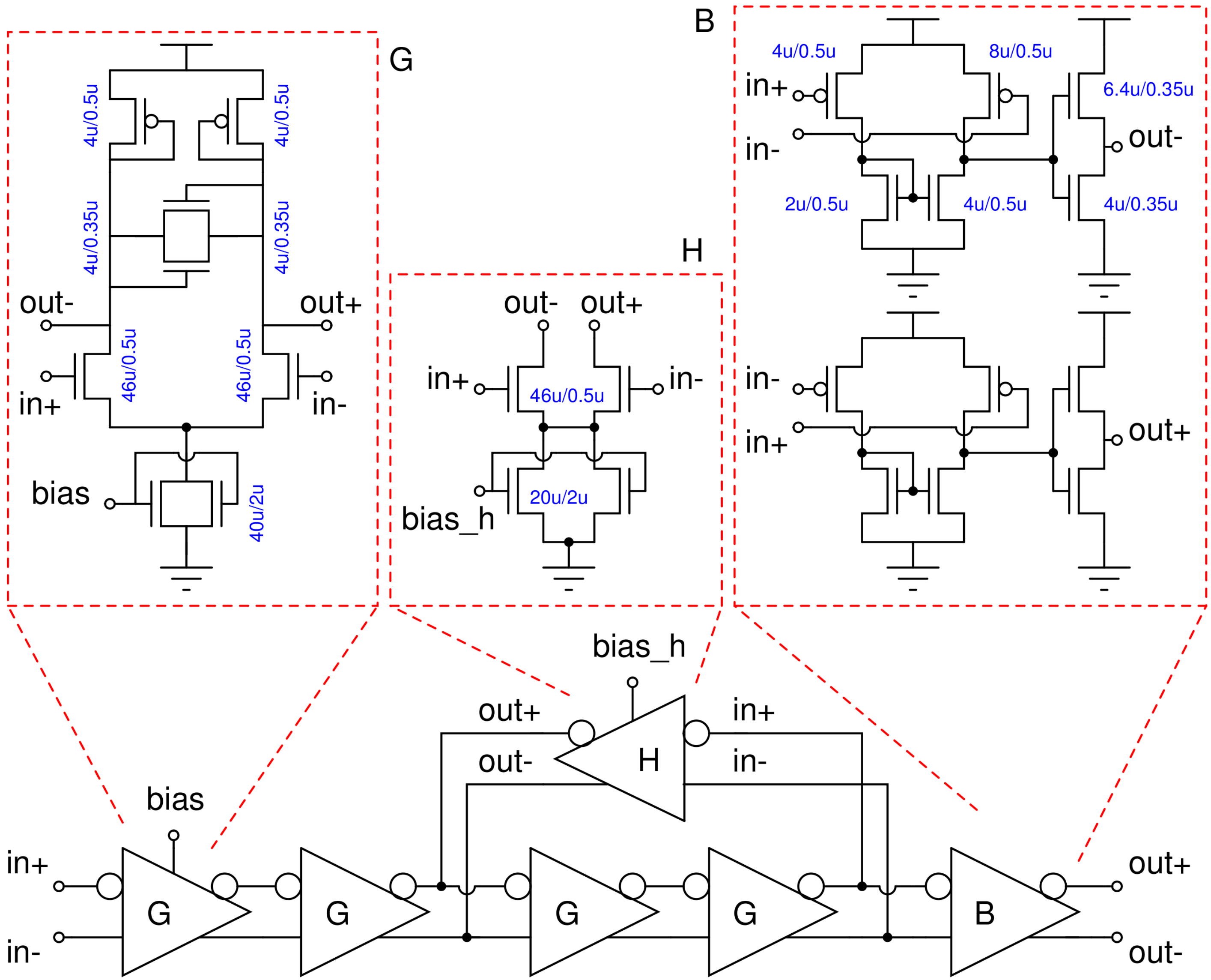
Jan Kaplon and Matt Noy (CERN) : “Front end electronics for silicon strip detectors in 90 nm CMOS technologies: advantages and challenges”, TWEPP 2010,

http://indico.cern.ch/materialDisplay.py?contribId=117&sessionId=15&materialId=slides&confId=83060



Preamplifier **Amp&integrator** **Amp, integrator, threshold, trimming** **Comparators**

Fast multistage comparators



- Very **fast comparators** are obtained by **cascading low-gain cells**. Full **CMOS levels** generated only in the **last stage**.

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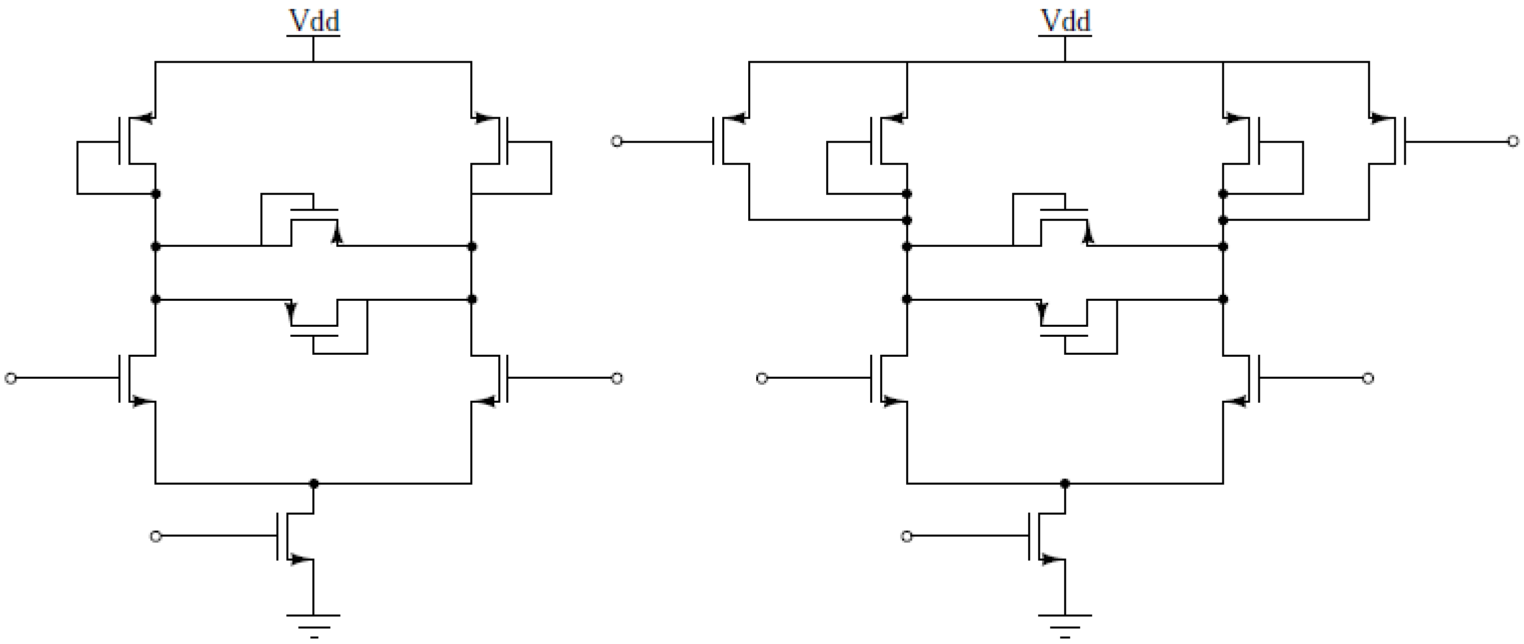
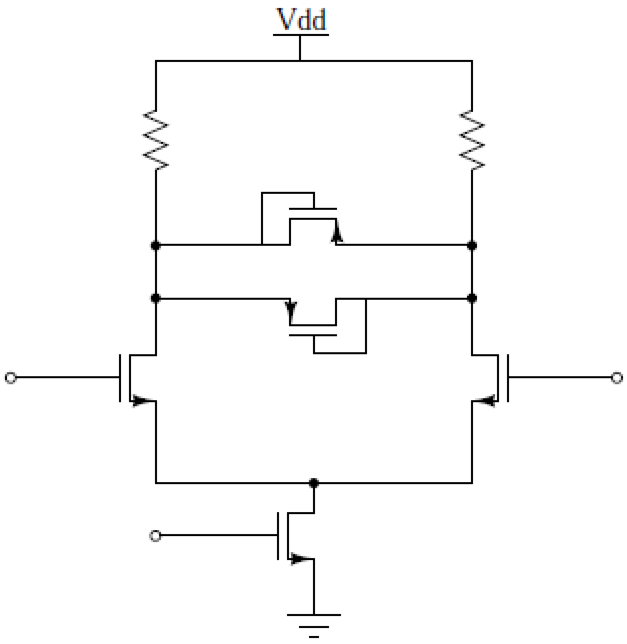
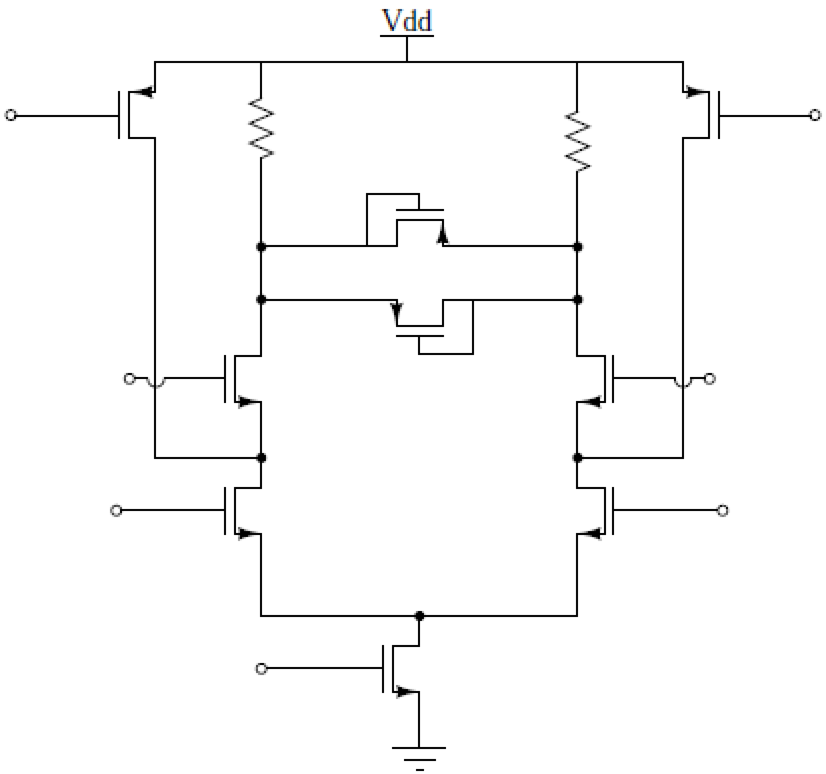
Gain cells in multi-stage comparators



- Differential cells with **diode connected** transistors as load.
- An extra **current source** can be added to **decouple** the equivalent impedance of the **load** from the **gm** of the differential input pair.
- **Diode connected** transistors among the **arms** of the diff pairs avoid **excessive swing** under **overdrive** condition that would slow the **recovery** of the circuit
- **PMOS** transistors could be used also in **triode** regionr.

Gain cell with resistive loads





- The **load** can be implemented also with **passive resistors**.
- In deep submicron technologies, these may offer **less parasitic** capacitance and give better speed.
- At low supply voltage (typical of modern CMOS technologies) look carefully at the **variation of bias points** with resistor change due to **process variations**.
- Cascoding can be applied to any of the cells.

How many stages?

$$A_0 = G^{1/n}$$

$$GBW = \frac{A_0}{\tau}$$

$$t = n\tau = \frac{nG^{1/n}}{GBW}$$

$$\frac{dt}{dn} = 0 = \frac{G^{1/n}(n - ln(G))}{nGBW} = 0$$

$$n = lnG \qquad A = e$$

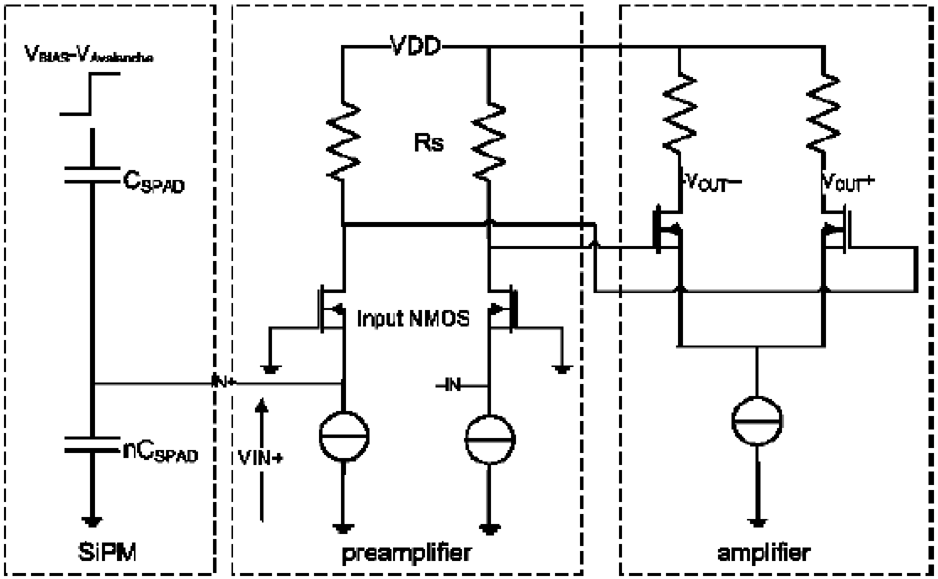
- **A_0 and GBW are the gain and gain-bandwidth product of the individual cell. G is the total gain of the full chain and n the number of stages.**
- **Example: gain of 2500 (necessary to resolve 0.5 mV to 1.2 V) number of stages=8**
- **High speed lead quickly to high power.**
- **Usually a compromise needs to be found.**

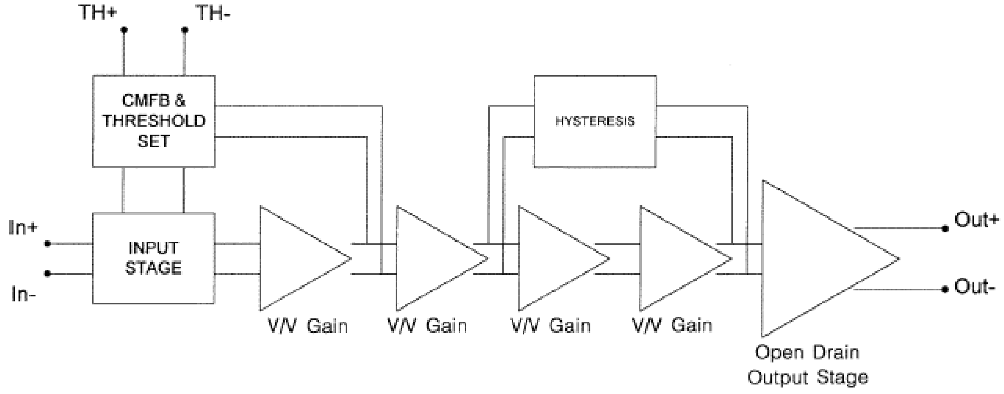
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 24, NO. 2, APRIL 1989

Design example of multi-stage comparator

F. Anghinolfi et al. "NINO, an Ultrafast Low-Power Front-End Amplifier Discriminator for the Time -of-Flight Detector in the ALICE Experiment", IEEE Trans. Nucl. Sci., vol. 51, n. 5 October 2004, pp. 1974-1978

Parameter	Value
Peaking time	1ns
Signal range	100fC-2pC
Noise (with detector)	< 5000 e- rms
Front edge time jitter	< 25ps rms
Power consumption	30 mW/ch
Discriminator threshold	10fC to 100fC
Differential Input impedance	40Ω< Zin < 75Ω
Output interface	LVDS

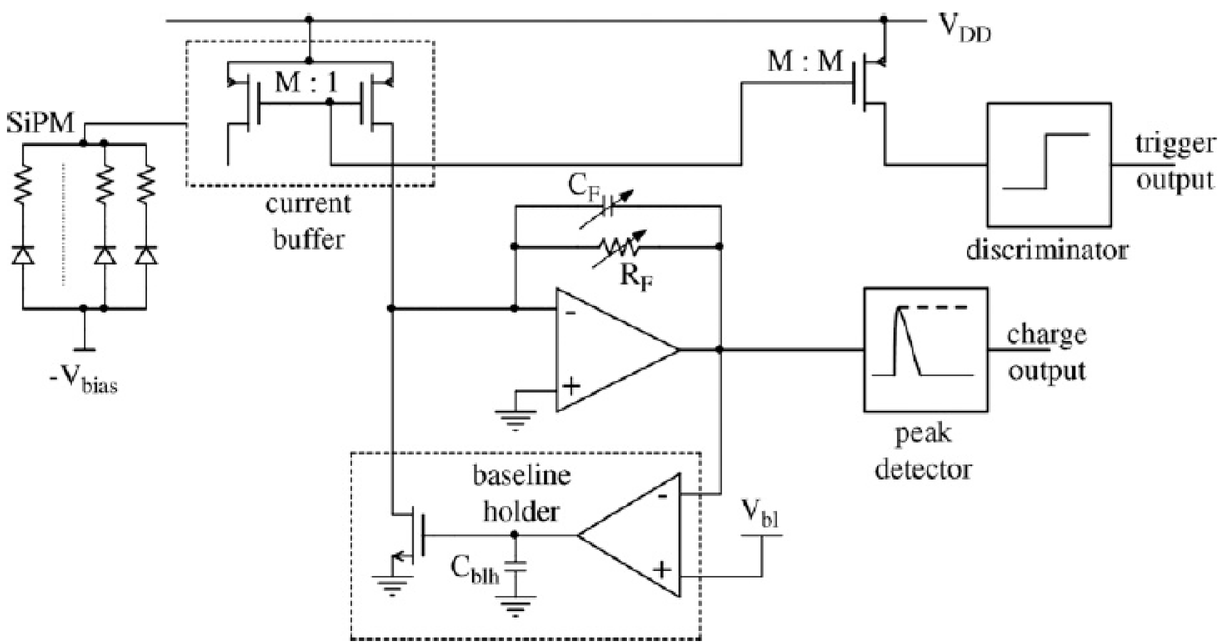


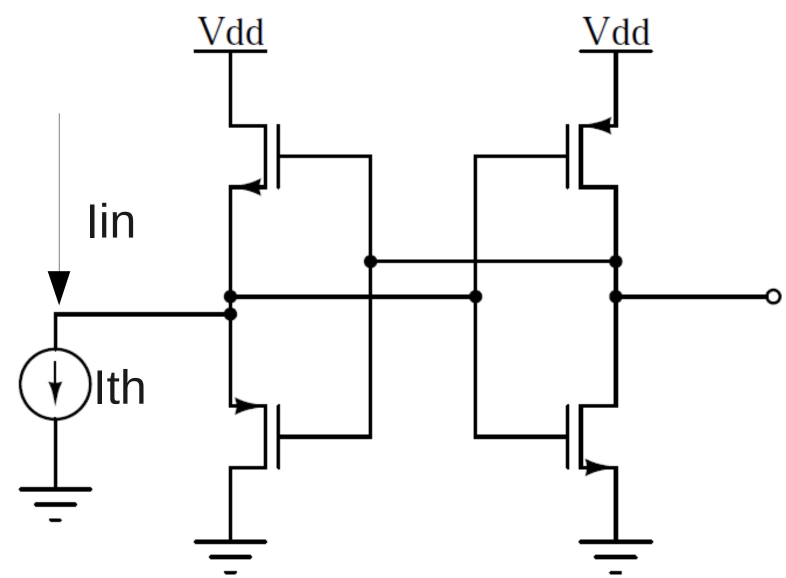


Technology: 0.25 µm CMOS

Current mode front-end and comparator

A. Argentieri, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.08.067

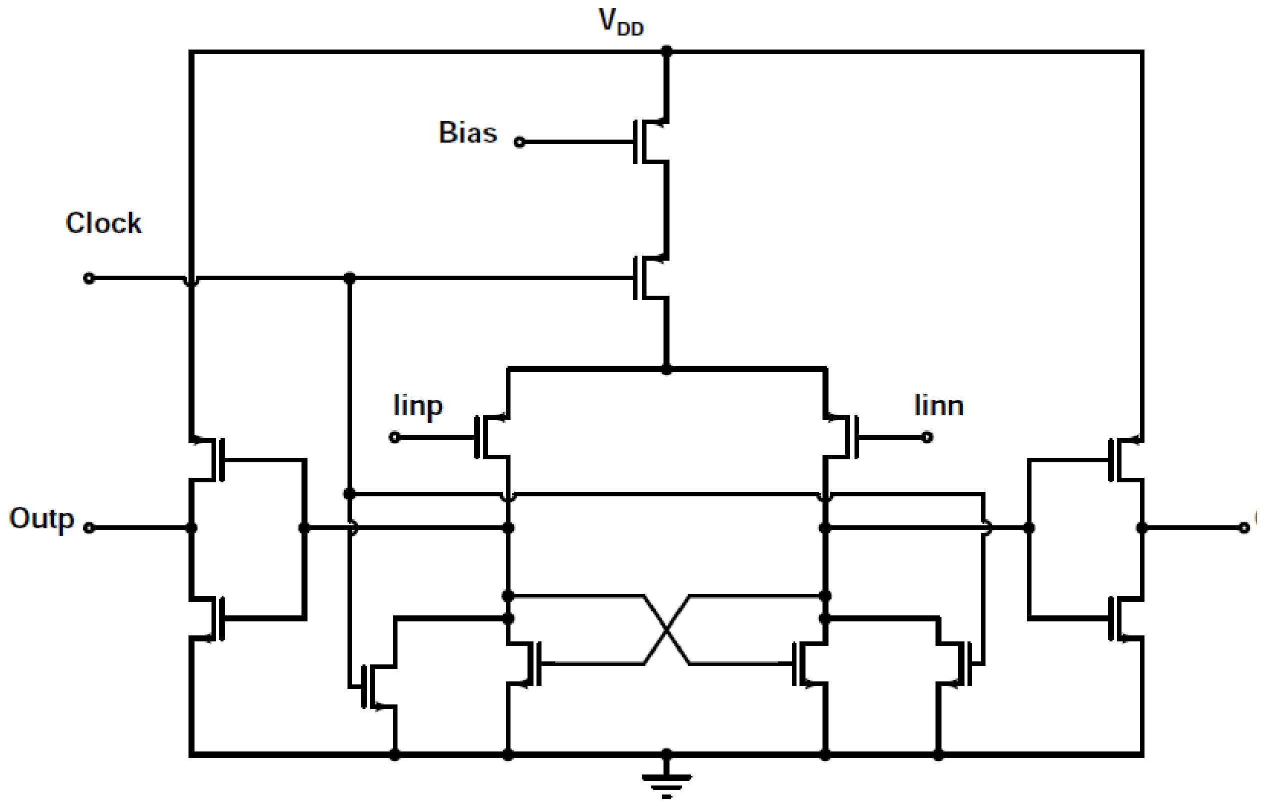




Current comparators:
E. Traff, “Novel Approach to High Speed CMOS Current Comparators”
Electronics Letters, 30th January 1992, vol. 28, n.3

A.T.K. Tang and C. Toumazou, “High Performance CMOS Current Comparator”
Electronics Letters, 6th January 1994, vol. 30, n.1

Discrete-time (latched) comparator



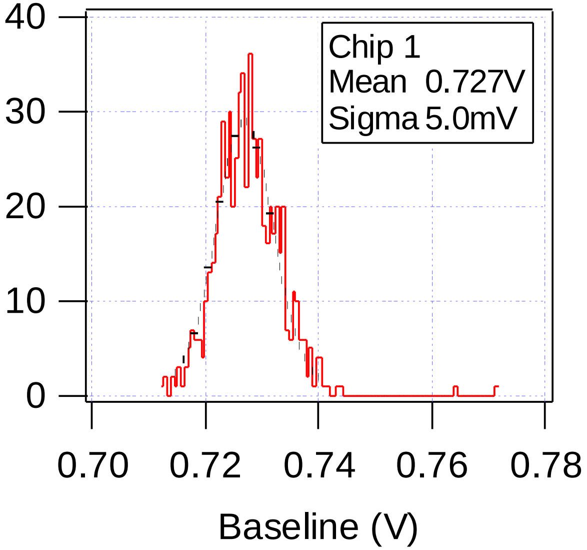
- Expoit positive feed-back to make a very fast decision.
- Very good sensitivity.
- The standard in ADC design
- Not often used in front-end as the time of arrival is not known and the switching noise can couple to the preamp.

Offset in comparators

- Mismatch between transistors in a differential pair originate offset: the effective threshold is different from the imposed one.
- Offest is random.
- Front-end ASIC are multi-channel systems: effective threshold will change from channel to channel
- If a single threshold value is used for all the threshold must be set so that the channel wit threshold does not fire on noise.
- Channels with higher effective threshold will suffer inefficiency.
- The threshold can be tuned on a channel by channel basis, introducing a digital to analog converter in every channel

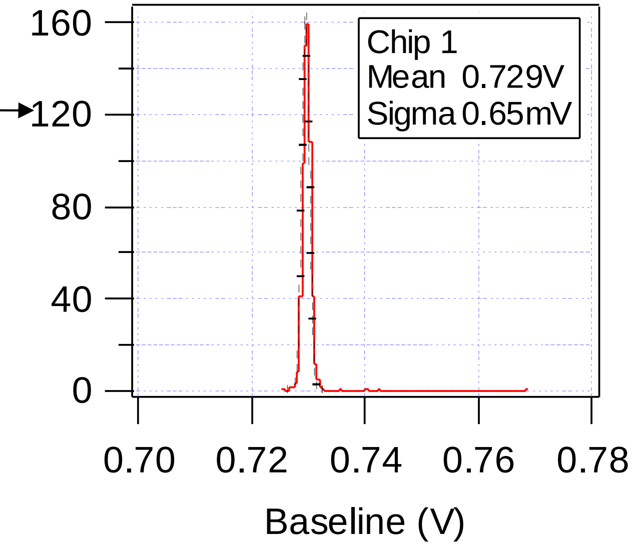
Example of threshold tuning

473 electrons rms

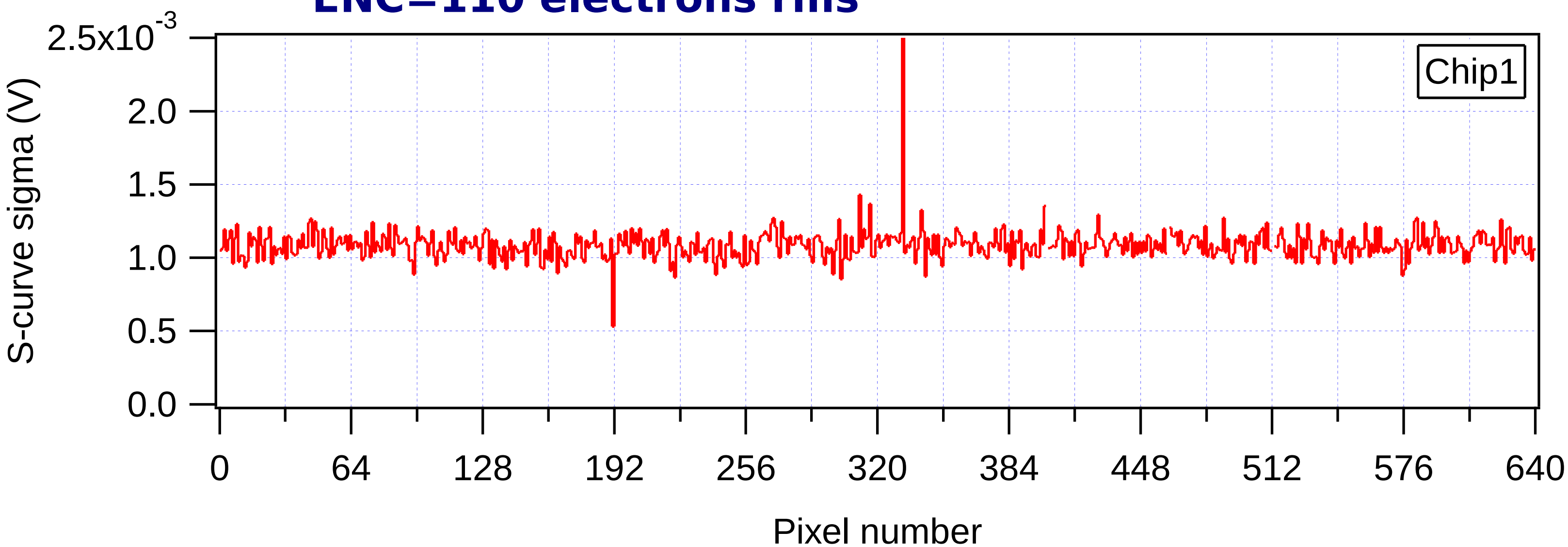


DAC correction

62 electrons rms



ENC=110 electrons rms



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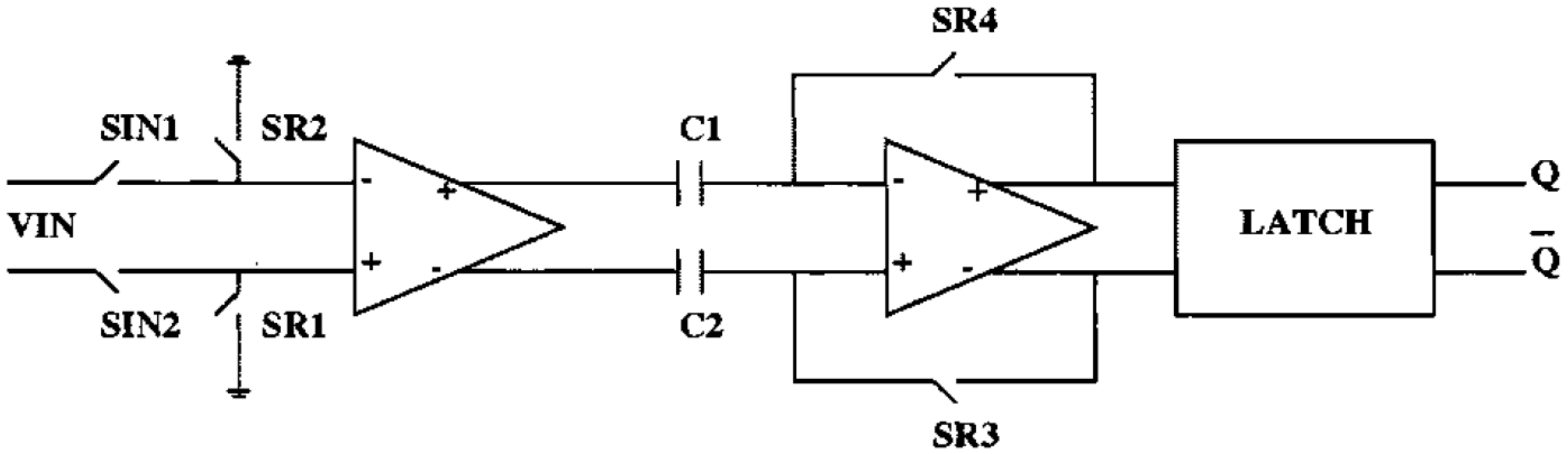
Autozeroing



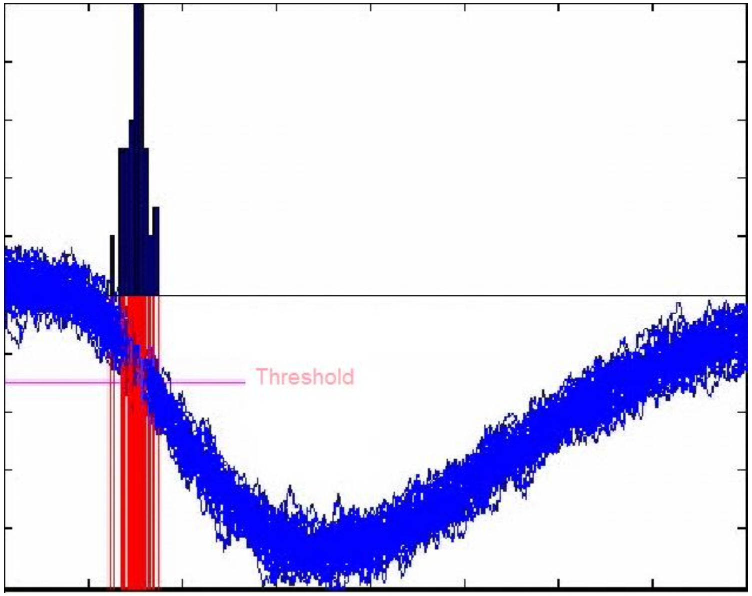
$$V_{\mathrm{OSR}} = \frac{\Delta Q}{A_{01} C} + \frac{V_{\mathrm{OSL}}}{A_{01} A_{02}} + \frac{V_{OSA2}}{A_{01}(1 + A_{02})}$$

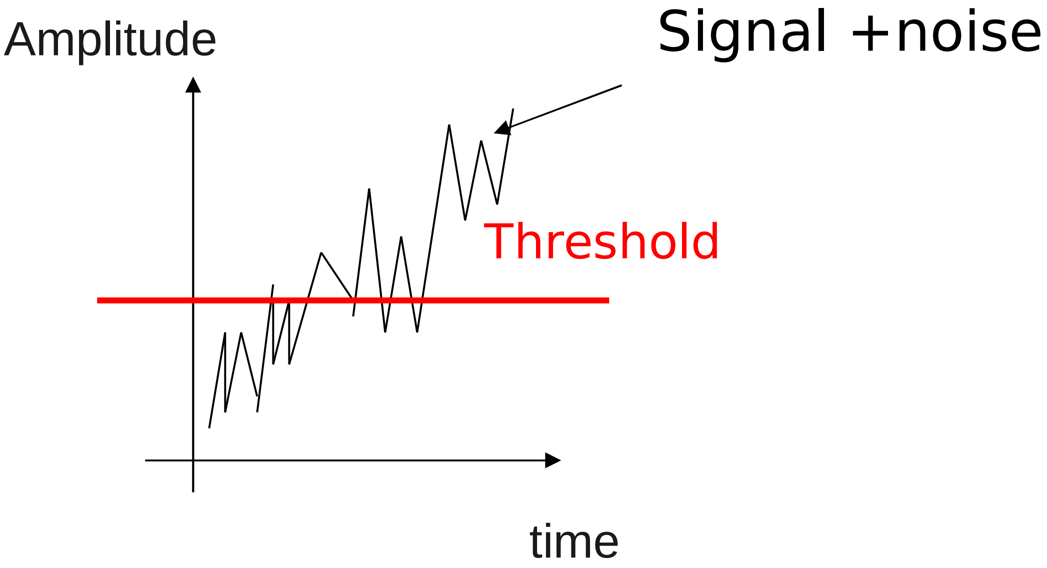
- **Offset can be suitable stored on capacitors and subtracted.**
- **Due to the leakage of the switches, the procedure must be repeated from time to time**
- **Very small residual offset can be achieved.**

- **Offset need to be studied with statistical simulations (Monte Carlo)**

Error in timing measurement: jitter

- Jitter is how noise before the discriminator appears in the time domain





JFG pictures...

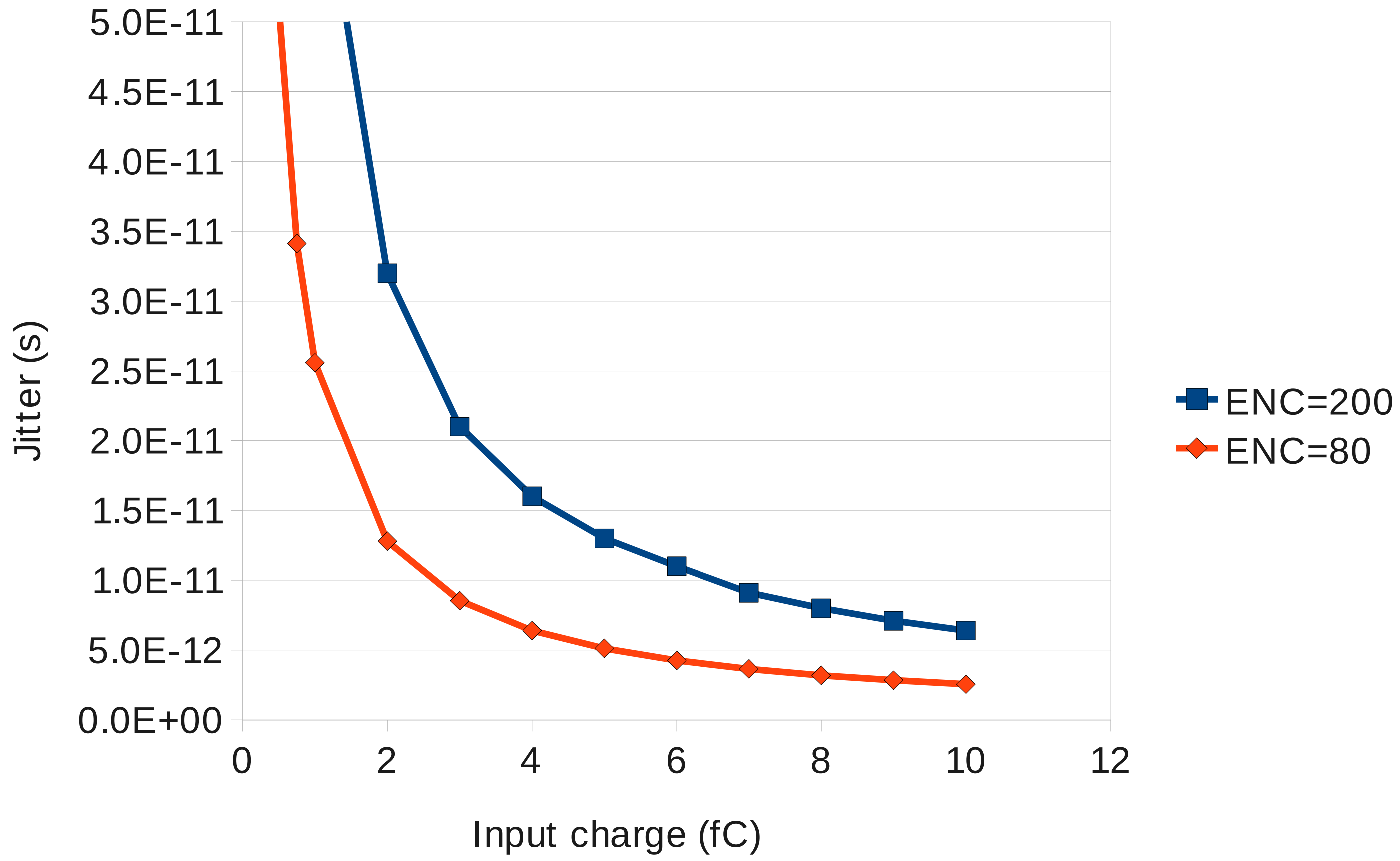
$$\sigma_t = \frac{\sigma_n}{\left(\frac{dV}{dt}\right)}$$

Proportional to the sqrt of the bandwidth (σ_n)

Proportional to the bandwidth ($\frac{dV}{dt}$)

Jitter vs signal amplitude

- **For a total signal rise time of 2 ns, a 10 ps resolution can be reached with a noise of 200 electrons and a signal of 6 fC or a signal of 2.5 fC and a noise of 80 electrons.**



$$\sigma_t = \frac{\sigma_v}{\frac{dV}{dt}}$$

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An important point

$$SNR = \frac{\sigma_n}{A_{peak}}$$

$$\sigma_t = \frac{\sigma_n}{\frac{dA}{dt}}$$

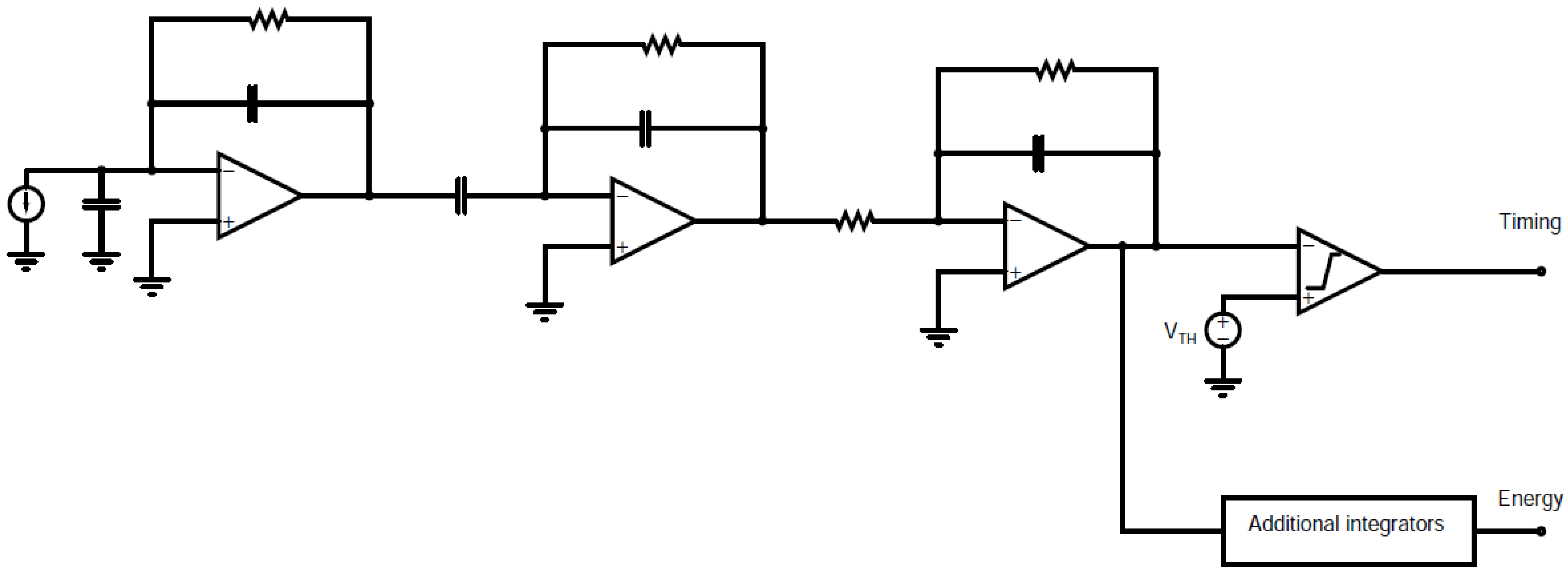
$$\sigma_n =\propto \sqrt{BW}$$

$$\frac{dA}{dt} =\propto BW$$

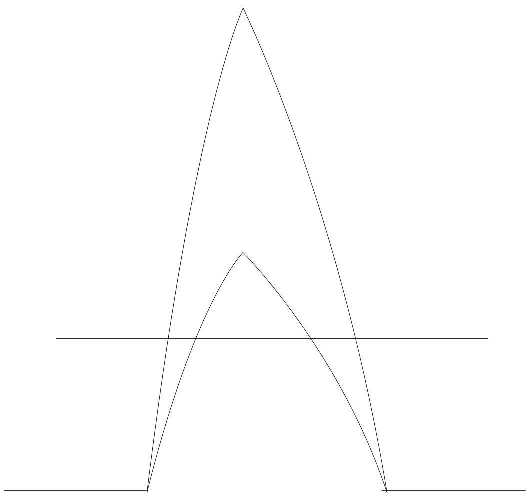
$$\sigma_t =\propto \frac{1}{\sqrt{BW}}$$

Timing system need to be fast!

Dual path system



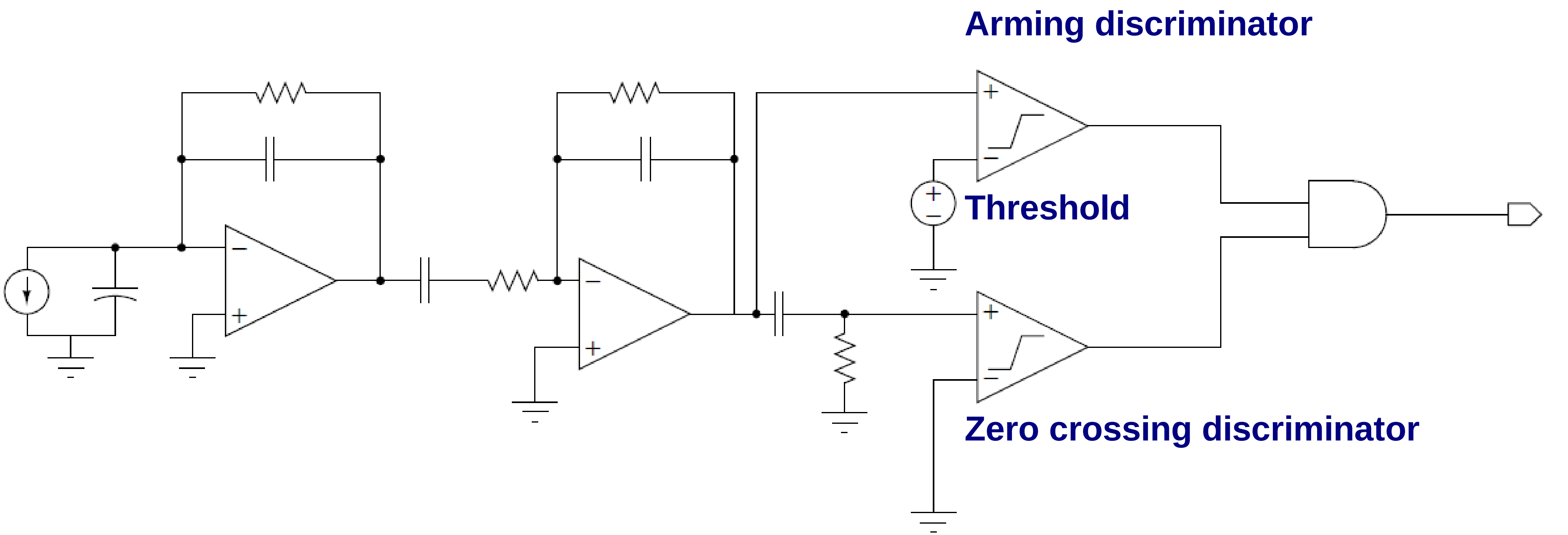
Time walk



Leading edge timing

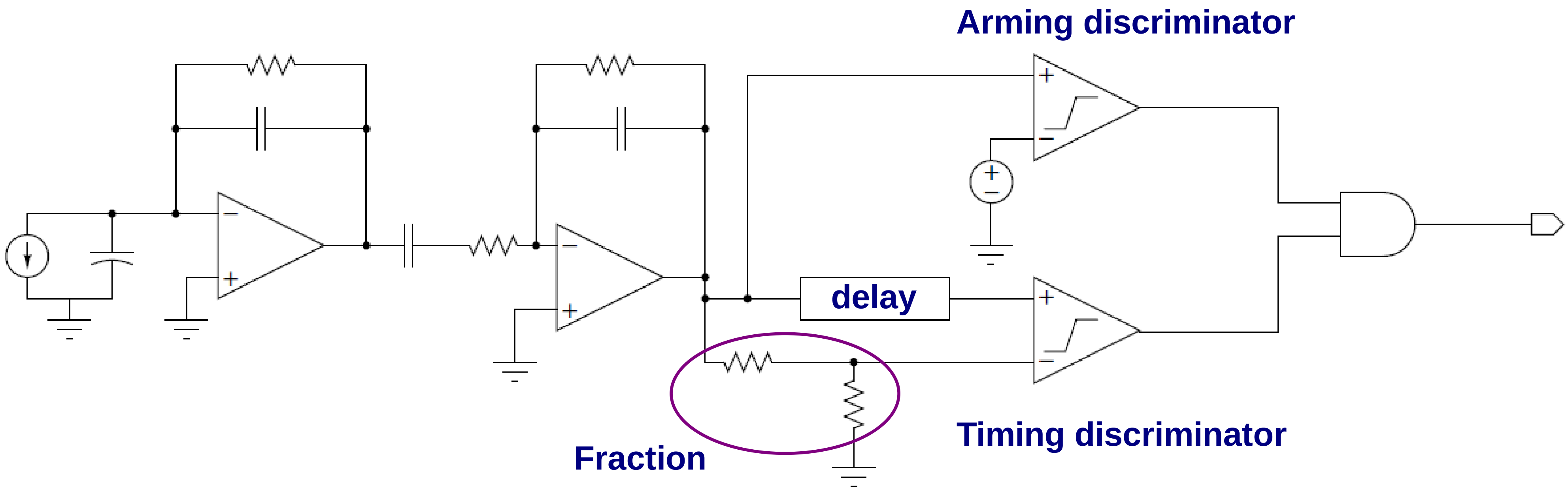
- Leading edge timing is affected by time-walk
- Signal with the same shape and different amplitude cross the threshold at different times.
- Time walk is a deterministic effect.
- It can be corrected by measuring the delay vs amplitude curve and registering also the signal amplitude.
- Time over Threshold is an effective way of registering the amplitude, as it re-uses the same hardware for time measurement (discriminator+TDC, no need for additional ADC).
- However calibration of the delay-vs-amplitude curve can be cumbersome.

Timing discriminators: zero crossing



- Operates on a **bipolar** signal.
- The **zero crossing** of the bipolar signal provides the timing.
- Needs to be **gated** to avoid continuous firing on **noise**.
- In IC with a large number of channels **gating** need to be implemented **carefully (avoid** the zcd generates **full swing digital** signals on noise).
- **Insensitive** to **time-walk**
- **Sensitive** to pulse **shape variations.**

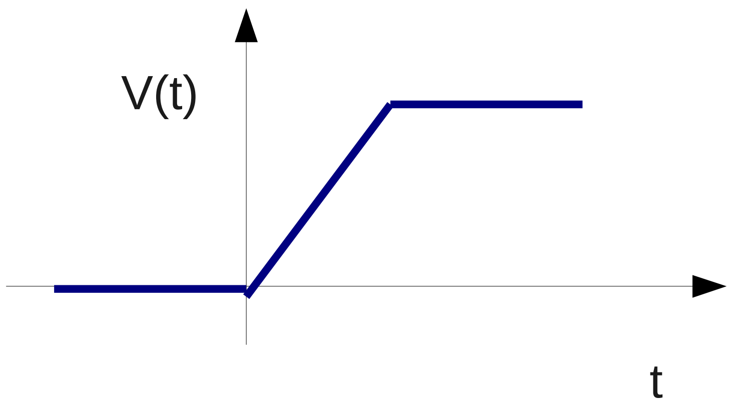
Timing discriminators: constant fraction



- Comparison between a **delayed copy** of the signal and an **attenuated** one.
- Detection of a **zero crossing** of a **bipolar waveform** (like in zero crossing).
- The key **difference** is how the **bipolar waveform** is **generated**.
- In IC, the **delay line** is often approximated with **RC filters**.
- **Insensitive** to amplitude variations.
- Can **reduce** significantly the sensitivity to **pulse shape variations** if properly optimized.
- **Precise timing** relies on **analog signal processing**. Can give very good performance, but not trivial to implement and a **lot of details** need to be watched out.

Timing discriminators: ideal constant fraction

$$V(t) = \frac{t}{t_r} V_0$$



$t_d > t_r$, amplitude compensation only

$$f V_0 = \frac{t - t_d}{t_r} V_0 \qquad t_{zc} = f t_r + t_d$$

$t_d > t_r$, amplitude and rise time compensation

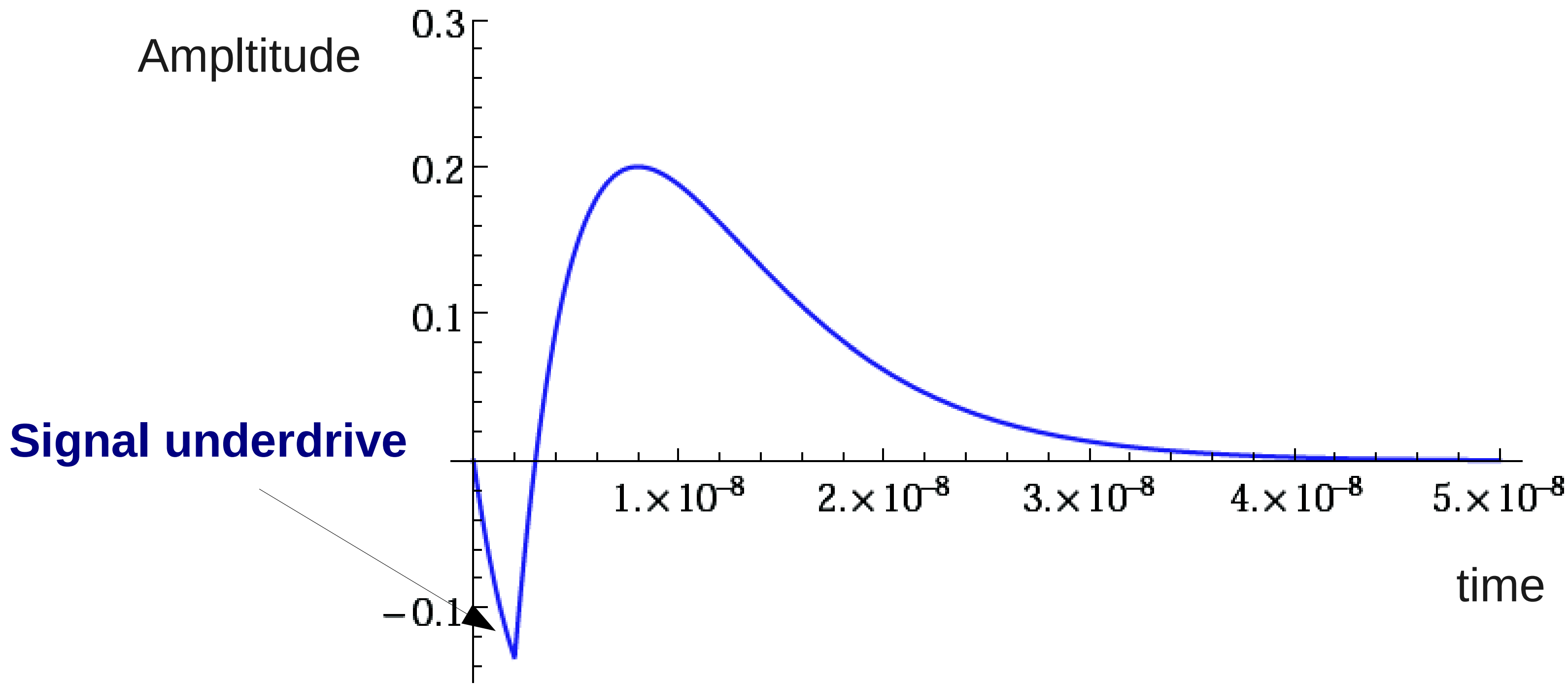
$$f \frac{t}{t_r} V_0 = \frac{t - t_d}{t_r} V_0 \qquad t_{zc} = \frac{t_d}{1 - f}$$

CFD timing withmore realistic signal

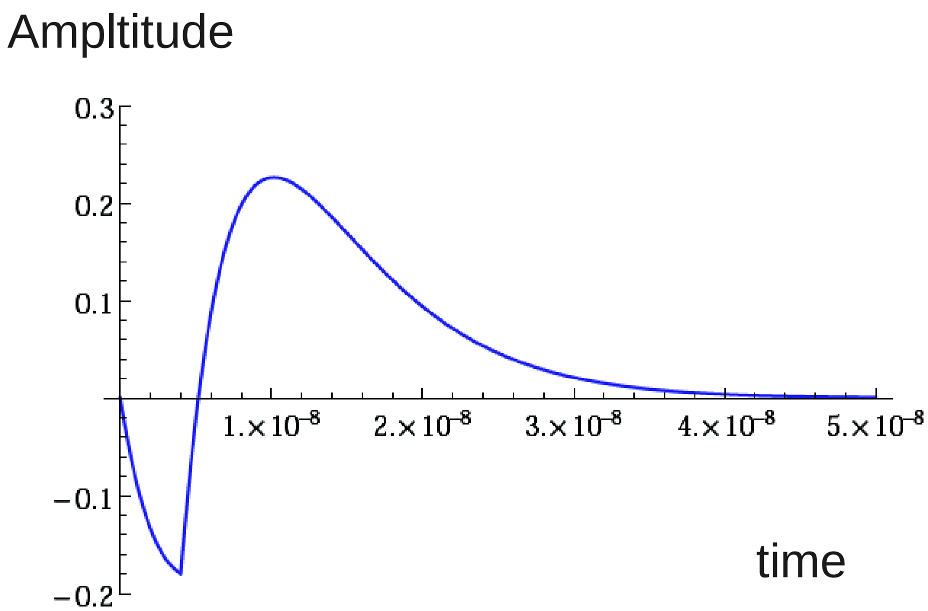
$$\frac{t-t_d}{\tau} e^{-\frac{t-t_d}{\tau}} - f\frac{t}{\tau} e^{-\frac{t}{\tau}}$$

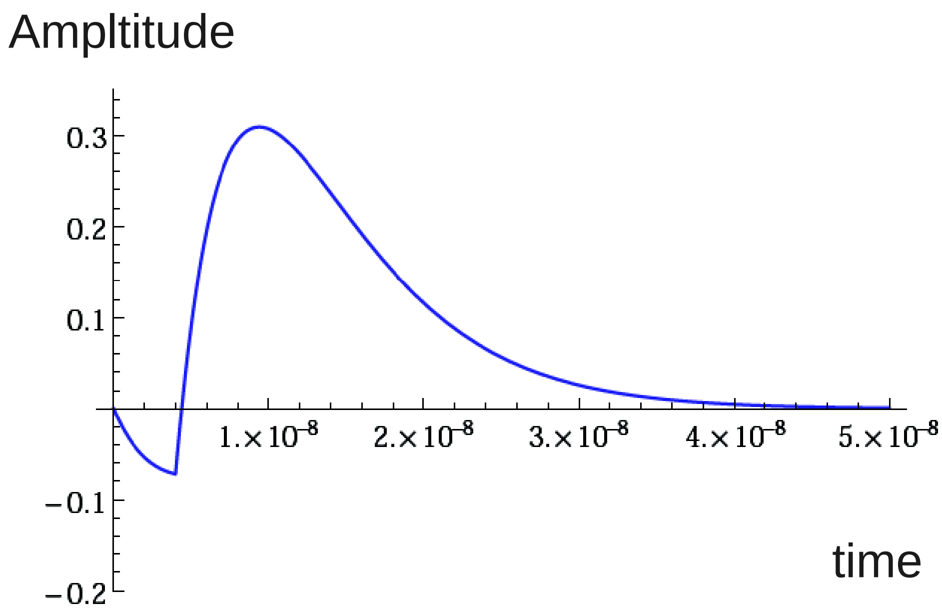
$$t_{zc} = \frac{t_d e^{t_d/\tau}}{e^{t_d/\tau} - f}$$

Waveform obtained from a CR-RC with 5 ns peaking time and a delay of 2ns.



Effect of delay and fraction



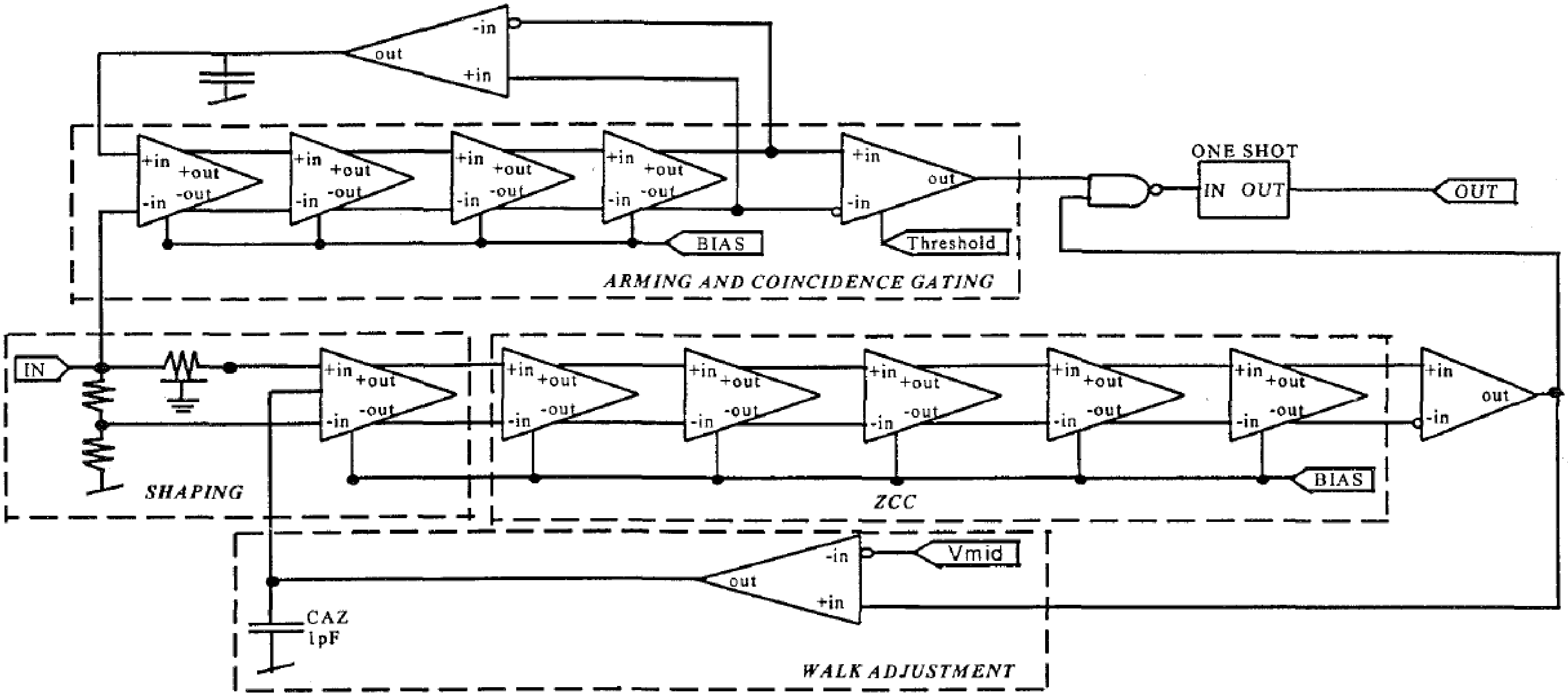


Obtained from CR-RC with 5 ns peaking time and a delay of 4ns, fraction = 0.5

Obtained from CR-RC with 5 ns peaking time and a delay of 4ns, fraction = 0.2

CFD with integrated delay line

M. L. Simpson, G. R. Young, R.G. Jackson and M. Xu, “A Monolithic, Constant Fraction Discriminator Using Distributed R-C Delay Line Shaping”, *IEEE Trans. Nucl. Sci.,* vol. 43, no. 3, June 1996, pp. 1695-1699.

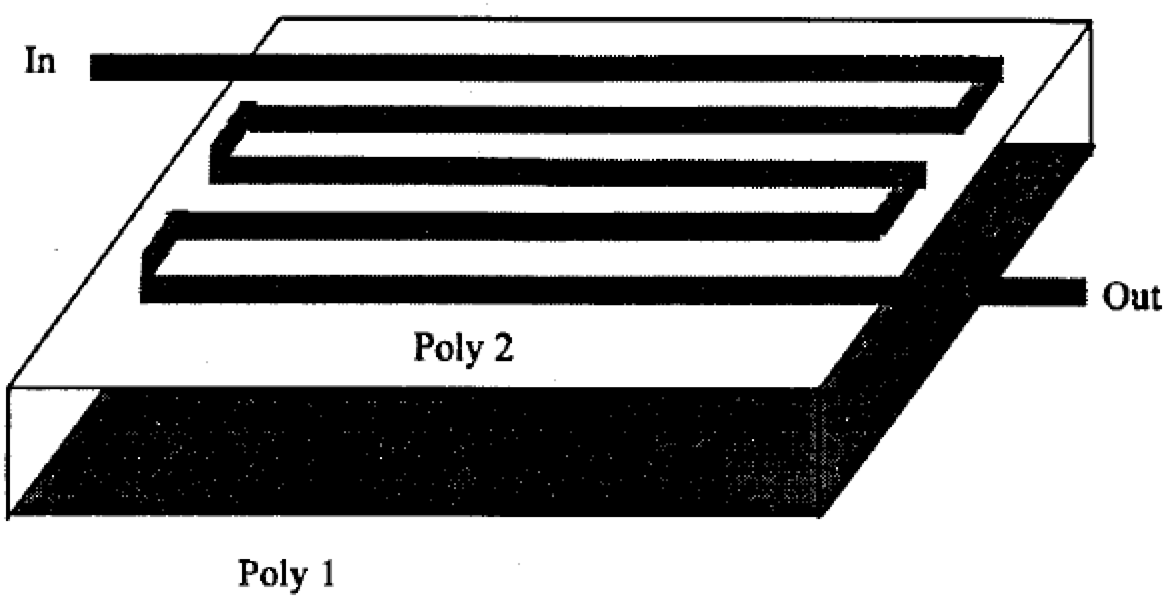


- **Comparators based on chain of large bandwidth, low gain cells.**
- **Automatic offset compensation with servo-loop.**
- **Fraction: resistive voltage divider**
- **Delay line: on silicon integrated delay line.**

Integrated delay line implementation

M. L. Simpson, G. R. Young, R.G. Jackson and M. Xu, "A Monolithic, Constant Fraction Discriminator Using Distributed R-C Delay Line Shaping", *IEEE Trans. Nucl. Sci.,* vol. 43, no. 3, June 1996, pp. 1695-1699.

Delay line area:
90 µm x 69.6 µm

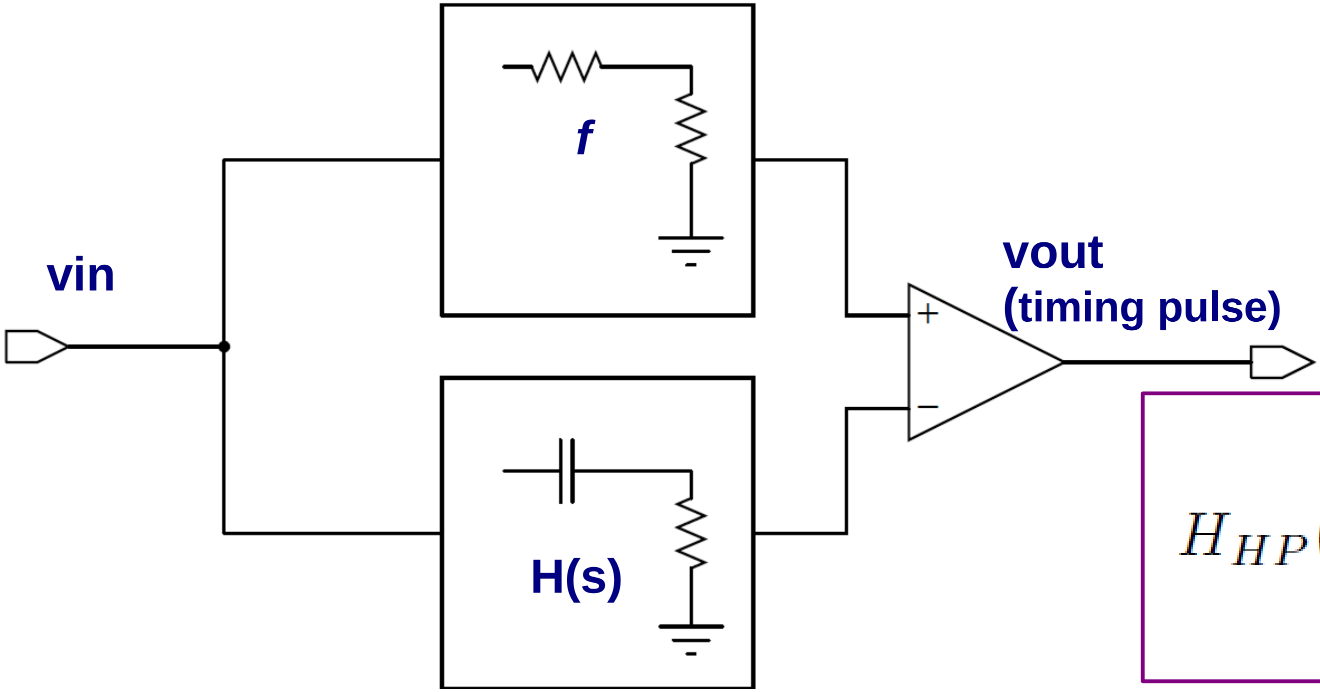


- **Delay line implemented as poly serpentine over a poly backplane.**
- **Today IC process may offer delay lines as a library component (so well modeled)**
- **Implementation of longer delay require considerable space (O(1 mm) for 4 ns delay.**
- **More common alternative: replace the delay line with a multi-pole RC filter.**

Lumped filters: single pole high-pass

C. H. Nowlin, "Low-noise lumped element timing filters with rise-time invariant cross-over time", Rev. Sci. Instr. 63 (4), April 1992, pp. 2322-2326.

David M. Binkley, "Performance of Non-Delay-Line Constant Fraction Discriminator Timing Circuit", *IEEE Trans. Nucl. Sci.,* vol. 41, no. 4, August 1994, pp. 1169-1175.

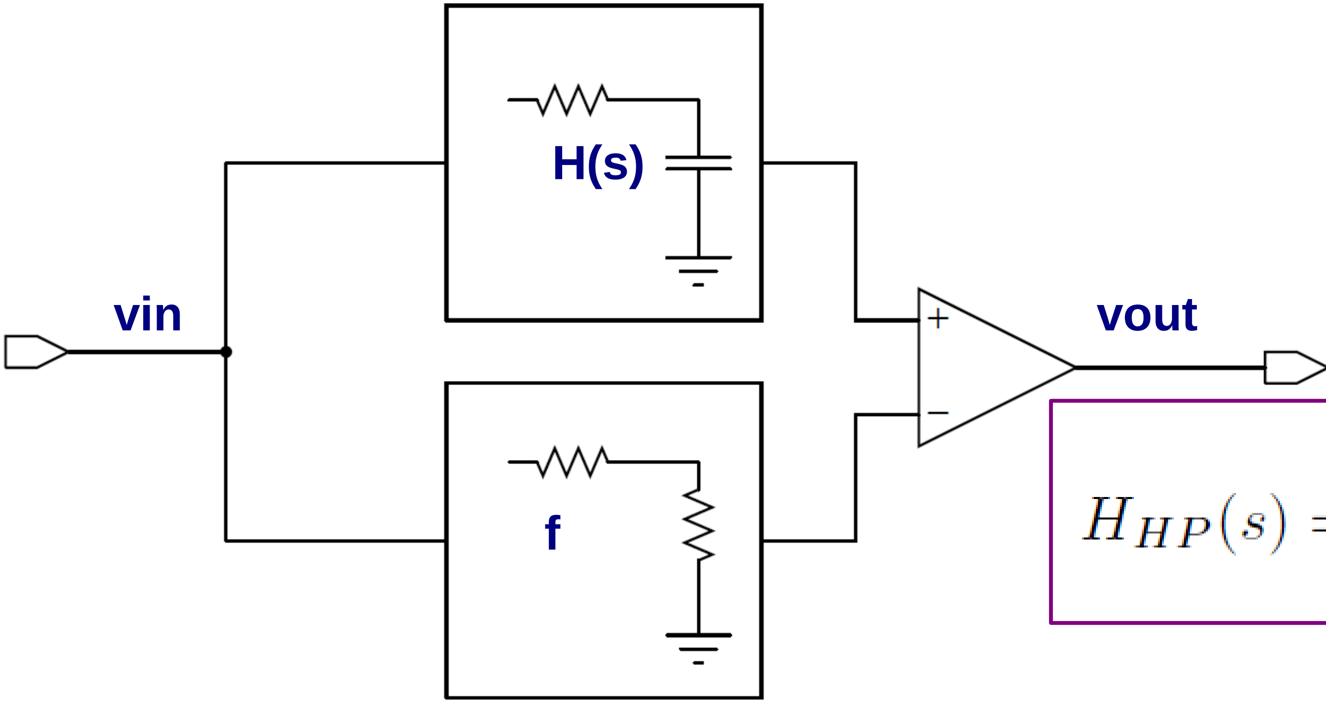


$$H_{HP}(s) = f\left(\frac{1 - s\tau_d\left(\frac{1-f}{f}\right)}{1 + s\tau_d}\right)$$

- **The zero in the transfer fucntion is necessary to provide the bipolar signal for timing.**
- **The discriminator provides amplitude compensation of time walk.**
- **Zero crossing is independent from input rise time only for inputs with linear rising edge and constant slope**

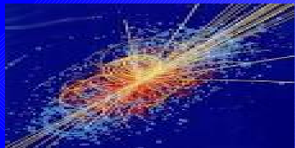
Lumped filters: single pole low-pass

David M. Binkley, “Performance of Non-Delay-Line Constant Fraction Discriminator Timing Circuit”, *IEEE Trans. Nucl. Sci.,* vol. 41, no. 4, August 1994, pp. 1169-1175.



$$H_{HP}(s) = (1-f)\left(\frac{1 - s\tau_d\left(\frac{f}{1-f}\right)}{1+s\tau_d}\right)$$

- **The zero in the transfer function is also provided even a low pass filter is used for the delay.**
- **The discriminator provides amplitude compensation of time walk.**
- **Zero crossing is independent from input rise time only for inputs with linear rising edge and constant slope**
- **The transfer function is identical to the one of the previous circuit if f=0.5. Otherwise it can be made identical by changing f in 1-f.**



Lumped filters: higher order low pass filters

David M. Binkley, "Performance of Non-Delay-Line Constant Fraction Discriminator Timing Circuit", *IEEE Trans. Nucl. Sci.*, vol. 41, no. 4, August 1994, pp. 1169-1175.

Circuit Configuration			Normalized Circuit Performance				
Topology	Delay (tau ea.)	Frac-tion	Under-drive	Over-drive	Zero-Cross Slope	Output Noise	Tim-ing Jitter
	$\frac{t_d}{t_{in}}$	(f)	$\frac{V_{und}}{V_{inpk}}$	$\frac{V_{ovr}}{V_{inpk}}$	$\frac{K_{zero}}{K_{inpk}}$	$\frac{\sigma_{vcf}}{\sigma_{vin}}$	$\frac{\sigma_{tcf}}{\sigma_{tin}}$
Delay Line	1.805	0.2	-0.167	0.8	0.8	0.987	1.234
Gaussian, 1-pole	1.770	0.5	-0.157	0.5	0.176	0.500	2.861
Gaussian, 2-pole	0.749	0.5	-0.201	0.5	0.245	0.611	2.492
Gaussian, 3-pole	0.477	0.5	-0.225	0.5	0.287	0.666	2.316
Gaussian, 4-pole	0.351	0.5	-0.242	0.5	0.318	0.701	2.204

Input signal is 1-pole lowpass-filtered step input with time-constant t_{in}.
Zero-crossing time (t_{cf}) is at $2t_{in}$.

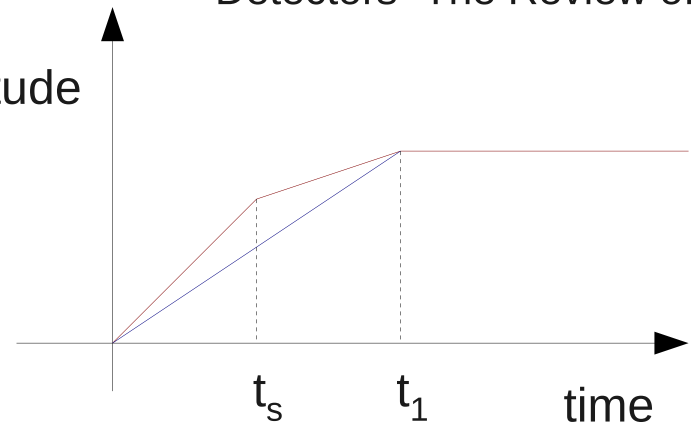
Circuit Configuration			Normalized Circuit Performance				
Topology	Delay (tau ea.)	Frac-tion	Under-drive	Over-drive	Zero-Cross Slope	Output Noise	Tim-ing Jitter
	$\frac{t_d}{t_{in}}$	(f)	$\frac{V_{und}}{V_{inpk}}$	$\frac{V_{ovr}}{V_{inpk}}$	$\frac{K_{zero}}{K_{inpk}}$	$\frac{\sigma_{vcf}}{\sigma_{vin}}$	$\frac{\sigma_{tcf}}{\sigma_{tin}}$
Delay Line	1.503	0.2	-0.126	0.8	0.852	0.994	1.109
Gaussian, 1-pole	1.325	0.5	-0.101	0.5	0.332	0.500	1.506
Gaussian, 2-pole	0.563	0.5	-0.131	0.5	0.446	0.600	1.344
Gaussian, 3-pole	0.360	0.5	-0.148	0.5	0.510	0.648	1.271
Gaussian, 4-pole	0.265	0.5	-0.159	0.5	0.551	0.677	1.228

Input signal is 2-pole lowpass-filtered step input with time-constant t_{in} ($t_{in}/\sqrt{2}$ each pole).
Zero-crossing time (t_{cf}) is at $2t_{in}$.

- **Lumped filters slow-down the signal decreasing its slope, leading to an increase in jitter.**
- **Increasing the order of the filter improves the slope to delay ratio.**
- **The jitter of a non-delay line CFD with a 4th order filter is only 11% above the one of the CFD with delay line.**
- **Fraction of 0.5 is optimal from the jitter point of view.**

ARC timing

Robert L. Chase "Pulse Timing System for Use with Gamma Rays on Ge(Li) Detectors" The Review of Scientific Instrumentation, vol. 39, no. 9, September 1968.



Linear rising edge, low pass filtered

$$V_{in} = K\tau[(t/\tau) - 1 + e^{-t/\tau}]$$

$t<t_1$

Timing signal for pulse with constant slope (blue curve)

$$V_{bp} = K\tau f[\frac{1}{f}(\frac{t-\tau_d}{\tau} - 1 + e^{-(t-\tau_d)/\tau}) - (t/\tau - 1 + e^{-t/\tau})]$$

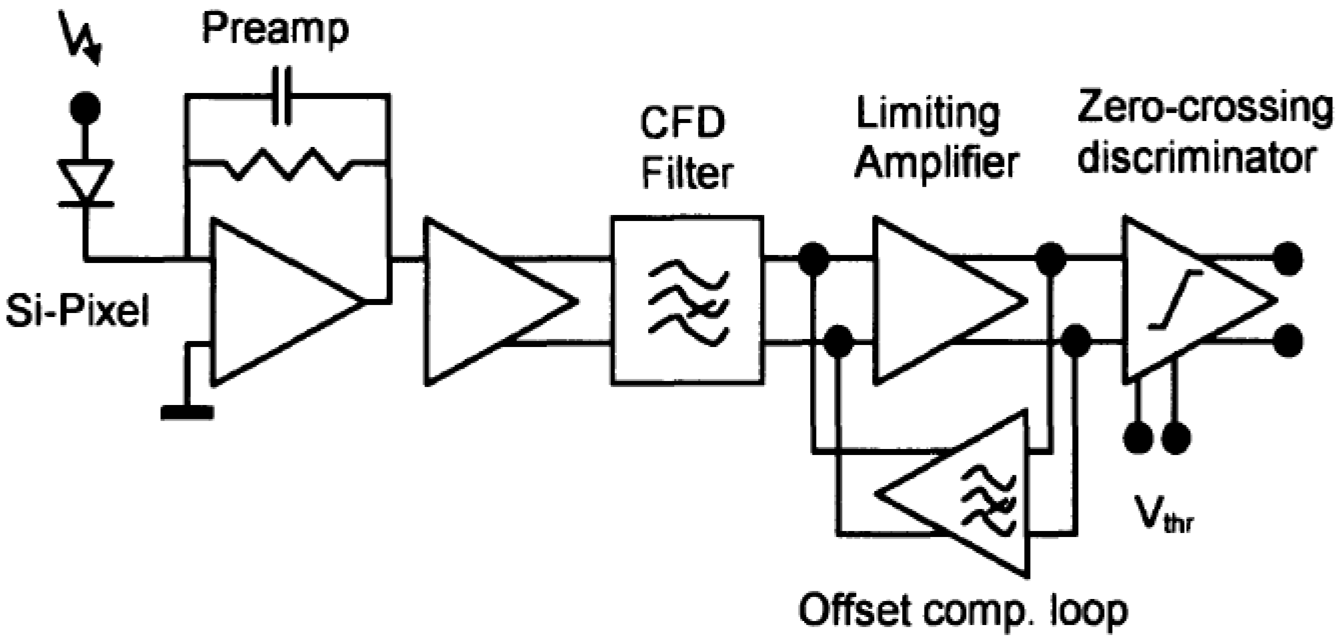
Timing signal for pulse with slope change at t_s (red curve)

$$V_{bp} = K\tau f[\frac{1}{f}(\frac{t-\tau_d}{\tau} - 1 + e^{-(t-\tau_d)/\tau}) - (t/\tau - 1 + e^{-t/\tau})] \; -$$

$$- \; V_{bp} = \frac{K\tau}{f}[f(\frac{t-\tau_d}{\tau} - 1 + e^{-(t-\tau_d)/\tau}) - (t/\tau - 1 + e^{-t/\tau})]$$

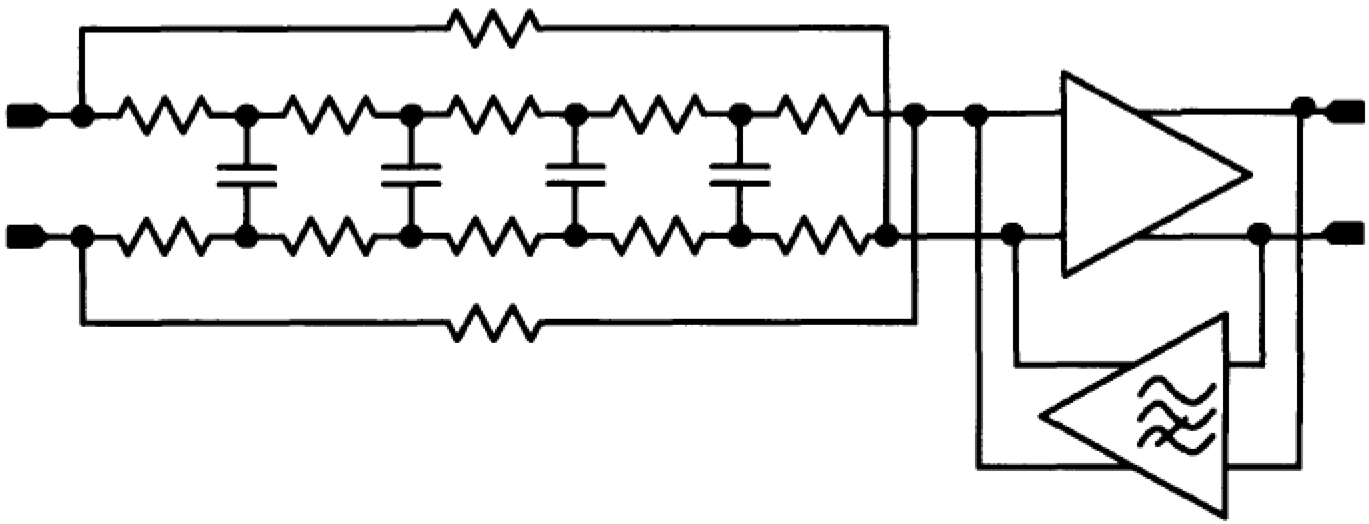
CFD design example (1)

S. Martoiu et al, "A Low-Power Front-End Prototype for Silicon Pixel Detectors with 100 ps Time Resolution"
2008 IEEE NSS Conference Record, N44-5



- **Technology: CMOS 0.13 µm, 1.2 V power supply.**
- **Dynamic range 10:1**
- **Voltage mode operation, fully differential topology**
- **Total area: 280 µm x 80 µm.**

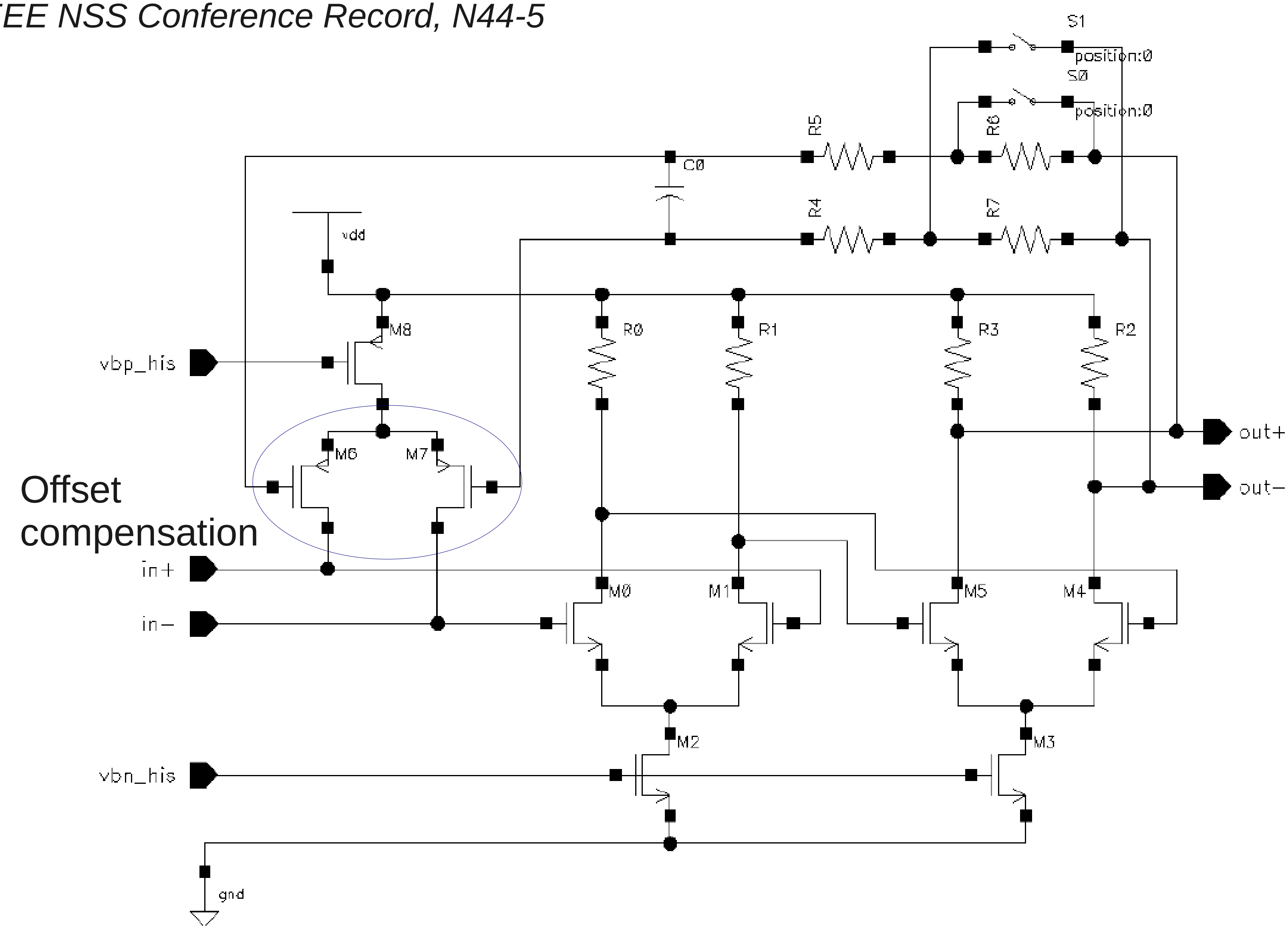
CFD design example (2)



- Technology: CMOS 0.13 µm, 1.2 V power supply.
- Dynamic range 10:1
- Voltage mode operation, fully differential topology
- Total area: 280 µm x 80 µm.

CFD design example (3)

S. Martoiu et al, “A Low-Power Front-End Prototype for Silicon Pixel Detectors with 100 ps Time Resolution”
2008 IEEE NSS Conference Record, N44-5



Post filter fast amplifier with resistive loads.

Discriminator summary

- Leading edge discriminators need correction for time walk.
- They are essentially part of the more complex zero crossing and constant fraction discriminator.
- Constant fraction discriminators with lumped delay lines may offer similar performance with respect with CFD employing true delay lines
- Filter of higher order (4th -5th) should be used to implement the delay line
- Post amplification after the filter is almost mandatory to properly drive the decision stages.
- Post amplification minimizes the impact of subsequent stages, but does not improve the noise to slope ratio (both signal and noise are amplified).
- CFD are still sensitive to pulse shape variations if the input pulse has not a linear rising edge.
- Minimization of sensitivity to pulse shape variations require several compromise.
- All CFD analysis assume linear circuits...Pulse distortion can significantly compromise timing.
- In order to have good final performance it is mandatory to have a realistic model of the input signal (including its shape and not only amplitude variations) and run very careful simulation with Monte Carlo analysis and process variations...