Timepix3 readout architecture

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CERN/TUCS (Uni. Of Turku)
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Workshop on Data driven front-end electronics for highly segmented radiation detectors
Torino, Italy

Outline

- Introduction and motivation
- Pixel matrix
- Periphery
- Design overview

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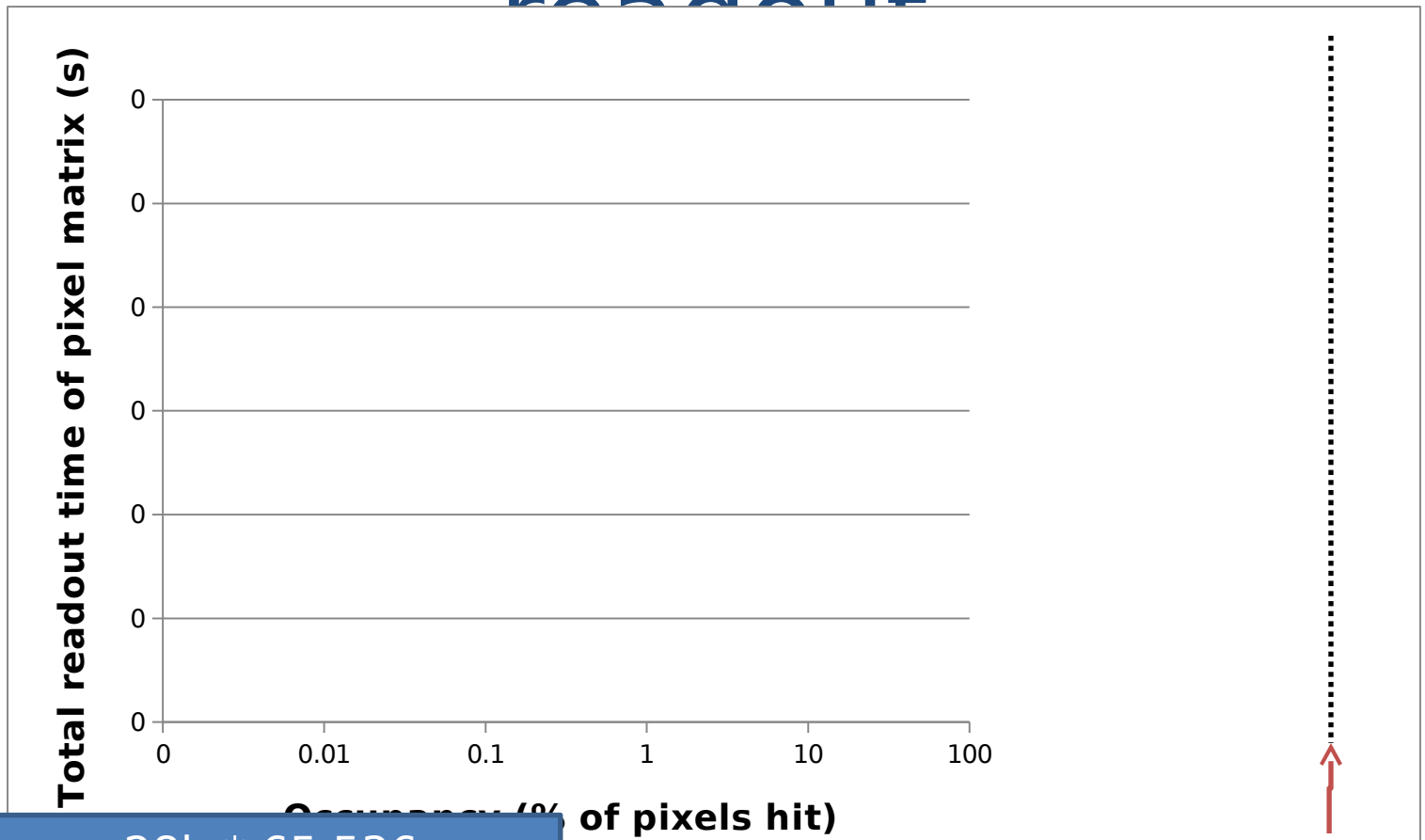
- **Introduction and motivation**
  - Pixel matrix
  - Periphery
  - Design overview

Timepix (2006) vs Timepix3 (2013)

	Timepix (250nm CMOS)	Timepix3 (130nm CMOS)
Acquisition modes	Charge (ToT)	Charge AND Time (ToA/ToT)
	Time (ToA)	Time (ToA only)
	Event counting	Event counting AND integral charge (PC & iToT)
Zero suppressed readout	NO	YES
Dead time per pixel	Readout time of one frame (> 300us)	ToT pulse width + 475ns (19 clocks @ 40MHz)
Min. timing resolution	10ns	1.562ns
On-chip Power pulsing	NO	YES
#Pixels	65,536 (256 x 256)	65,536 (256 x 256)
Pixel size	55 x 55 μm^2	55 x 55 μm^2

Motivation for sparse readout



Non-sparse: 28b * 65,536
Sparse: N * (28b+16b),
where N is number of pixels hit

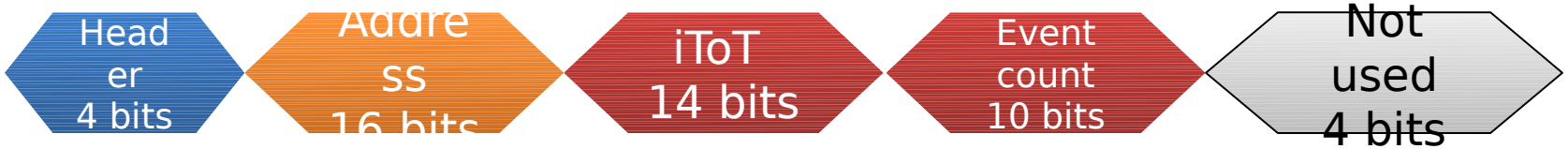
Break-even point
at ~ 63%

Three different data formats

ToA/ToT Mode:

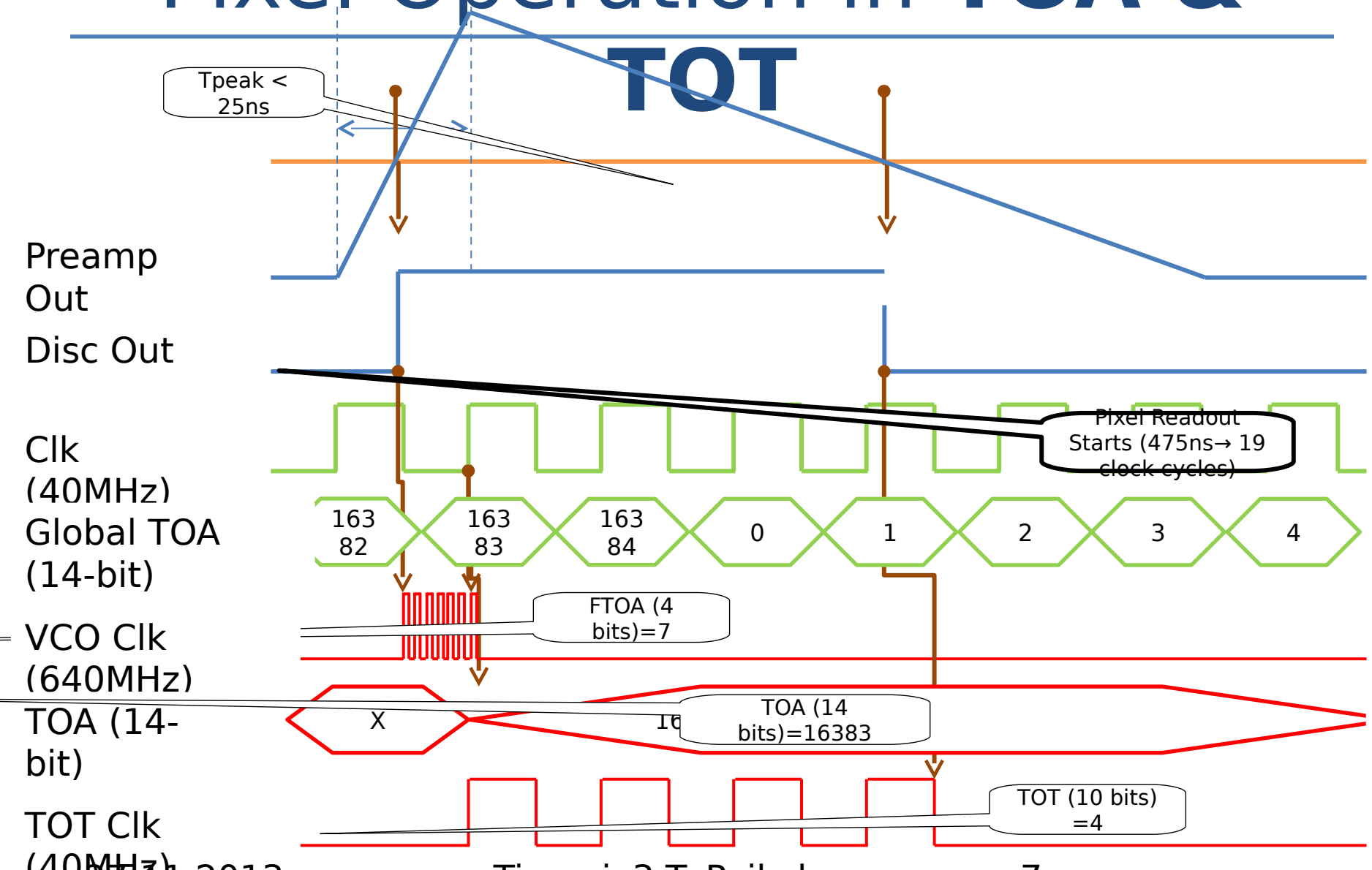
Only ToA mode:

Event counting mode:

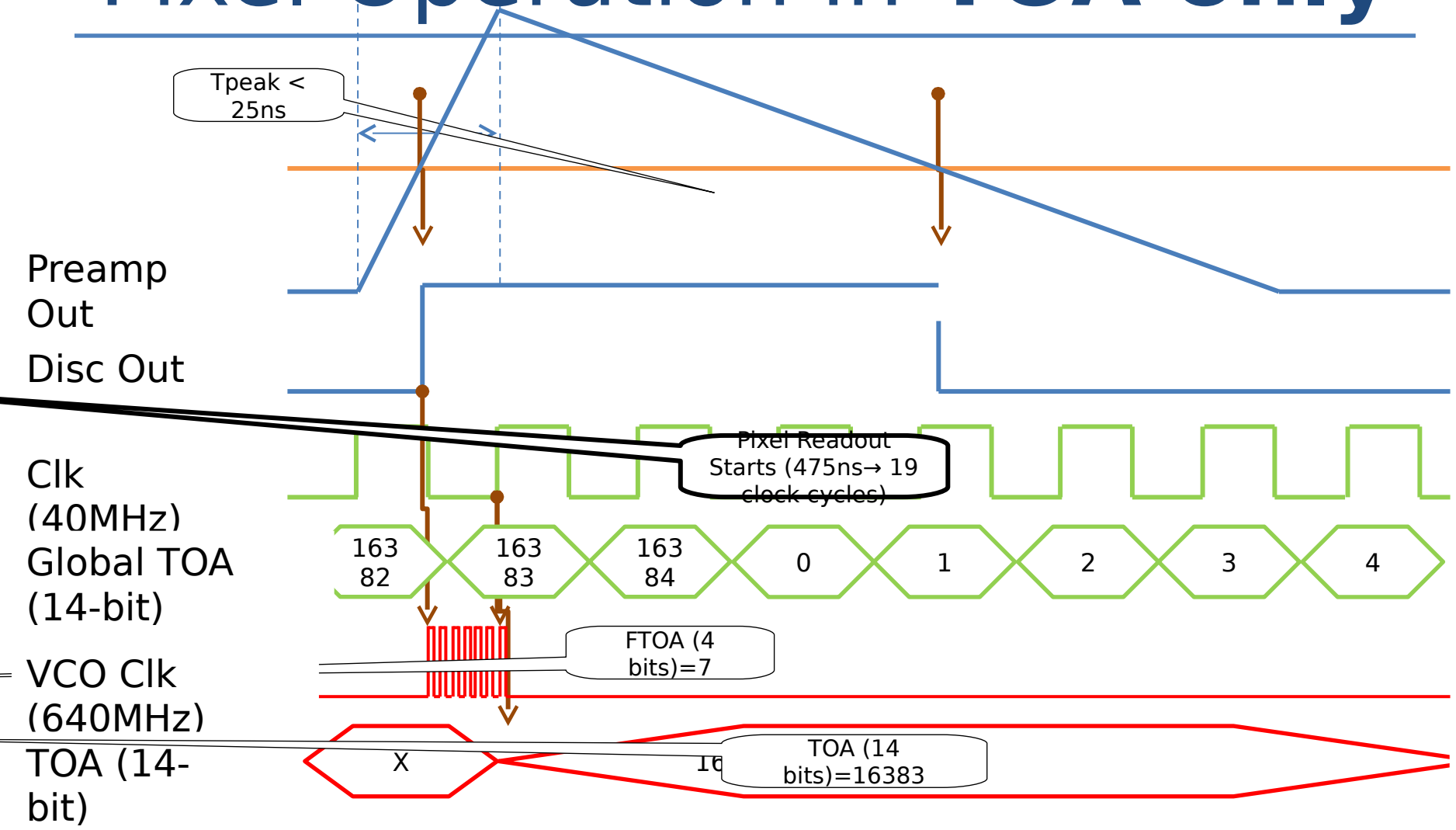


Fine time 4 bits can also be configured as 4-bit pile-up event counter.

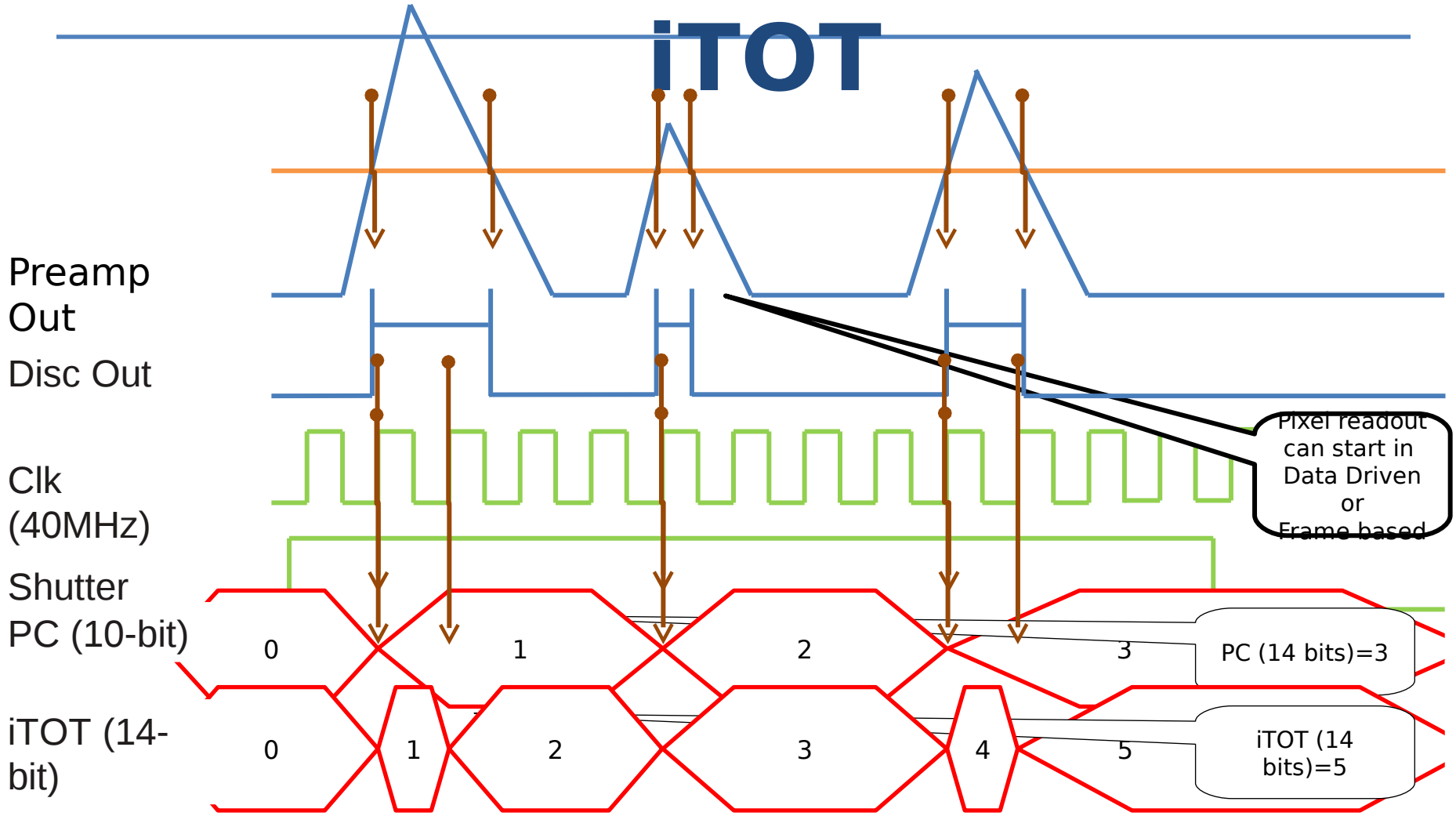
Pixel Operation in **TOA & TOT**



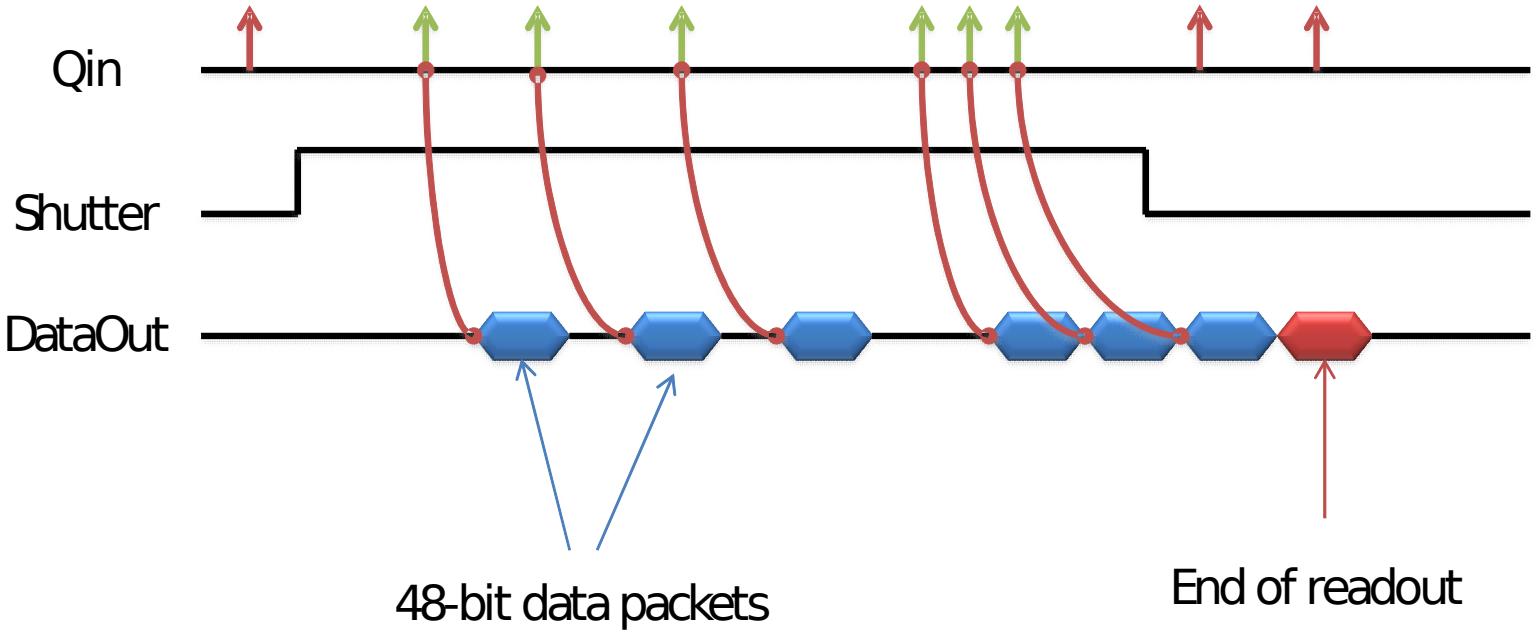
Pixel Operation in **TOA only**



Pixel Operation in **PC and iTOT**



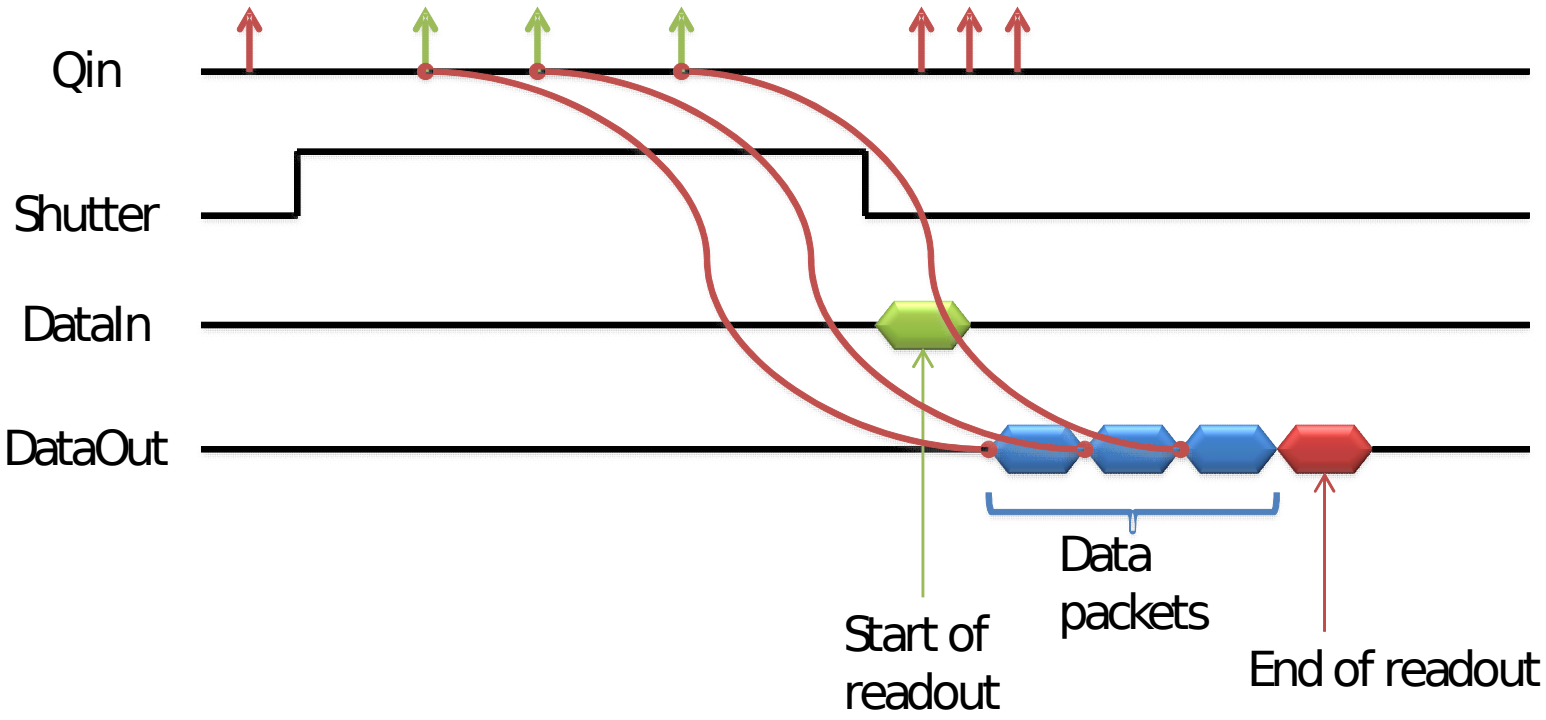
Data-driven readout mode



The main readout mode:

- Works without user interruption
- Shutter can be kept open indefinitely

Sequential readout mode



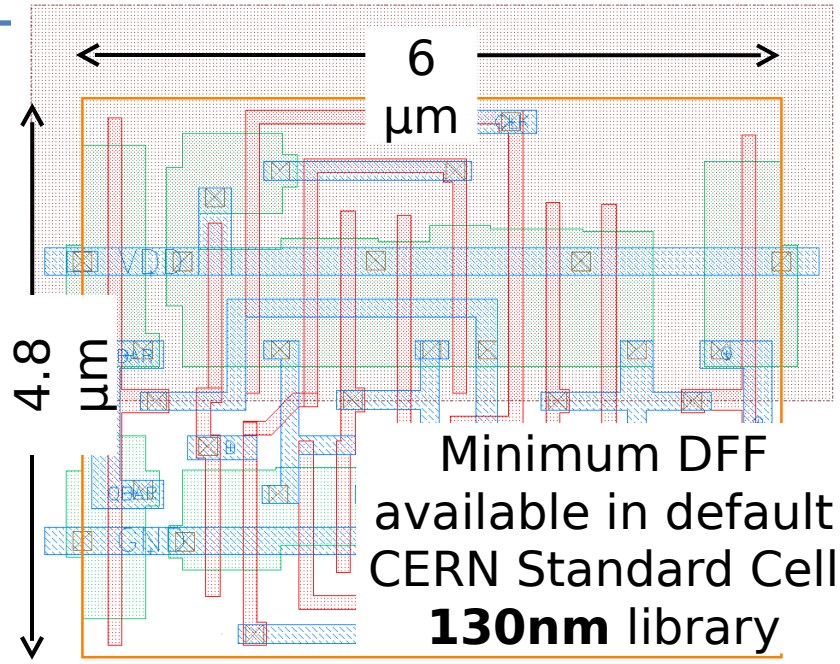
ode for testing purposes mainly.
t provides also fine-grain readout control.
ximum number of parallel columns read out specified using tokens.

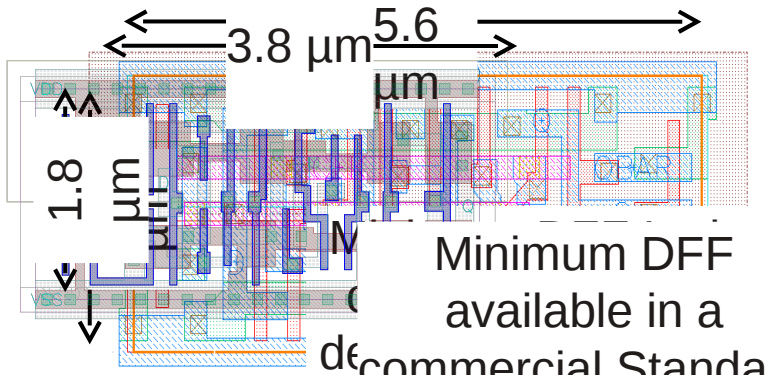
First design issues

- Avoid custom logic if possible (not explicitly stated…)
- Extremely area critical design: Commercial std cell library too big => build a new library
- General purpose chip: Many possibilities for the readout architecture => find a way to simulate different options
- Many feature requests => Try to converge to a number of most useful features
- Multi-site project => Repository needed

CERN HD Library

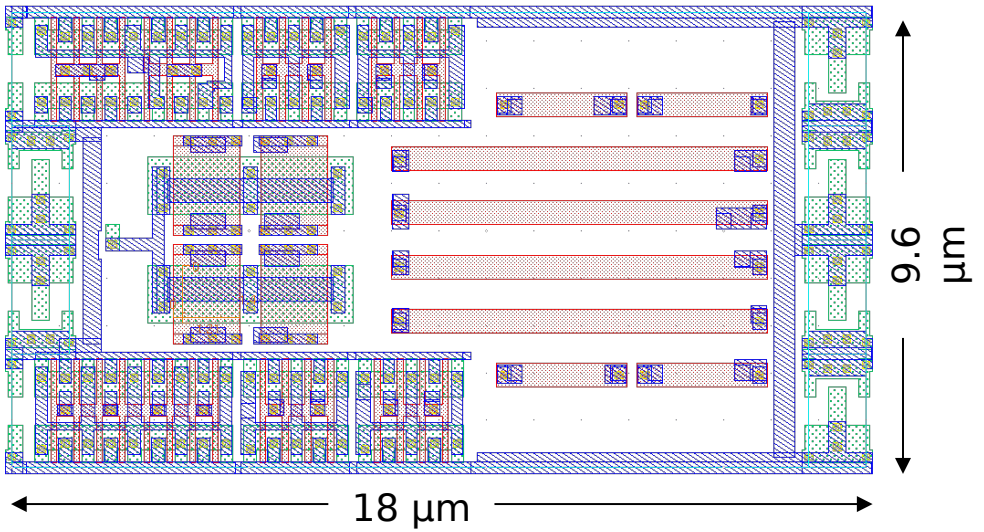
- Row Height is fixed to 2.4 µm
- Well Tap library
- Maximum frequency < ~600 MHz (@1.5V)
- Low power transistors
- ~50 cells are available in the library



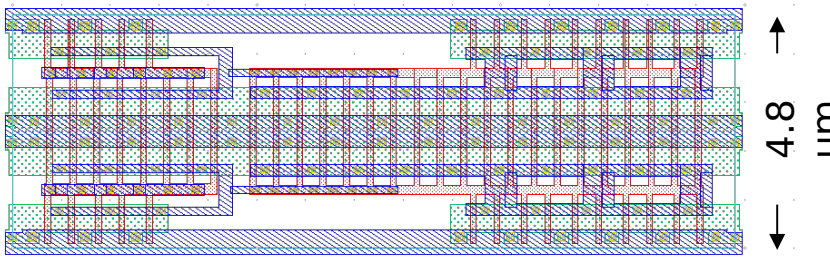


CERN HD Special cells

- Cells with non-standard row height are also possible to integrate:
  - Row height multiple (2.4 µm)
  - Pitch length multiple (0.4 µm)



VCO_4_VG



CLK_Q_RVT_XL

Outline

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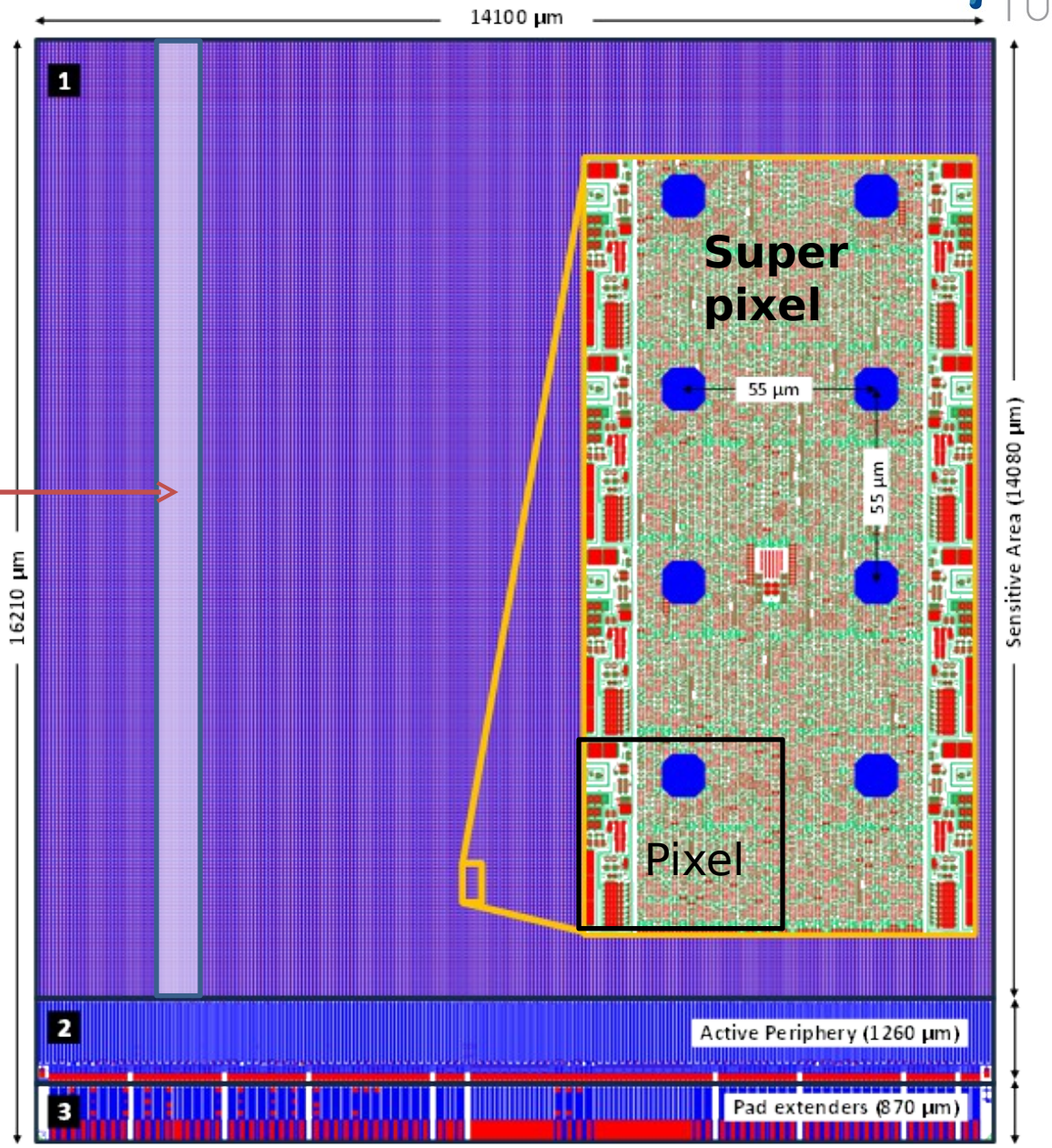
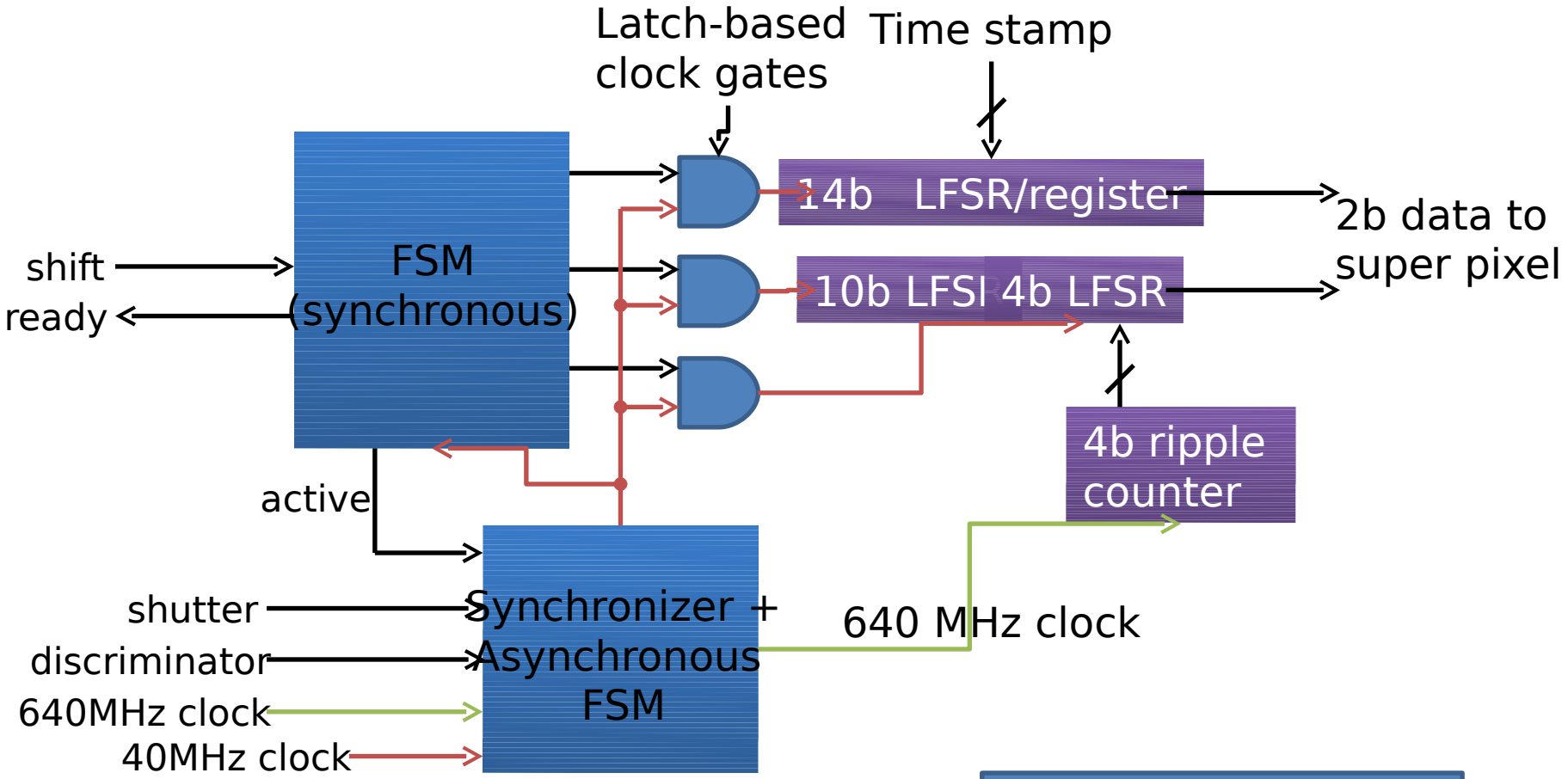
- **Pixel matrix**
- Periphery
- Design process

Pixel matrix floorplan

- Pixel 55x55um²
  (digital pixels not identical)
- 2x4 logical super pixel => double column
- Matrix physical building block: 4x super pixel (110x880um²)
- No on-chip



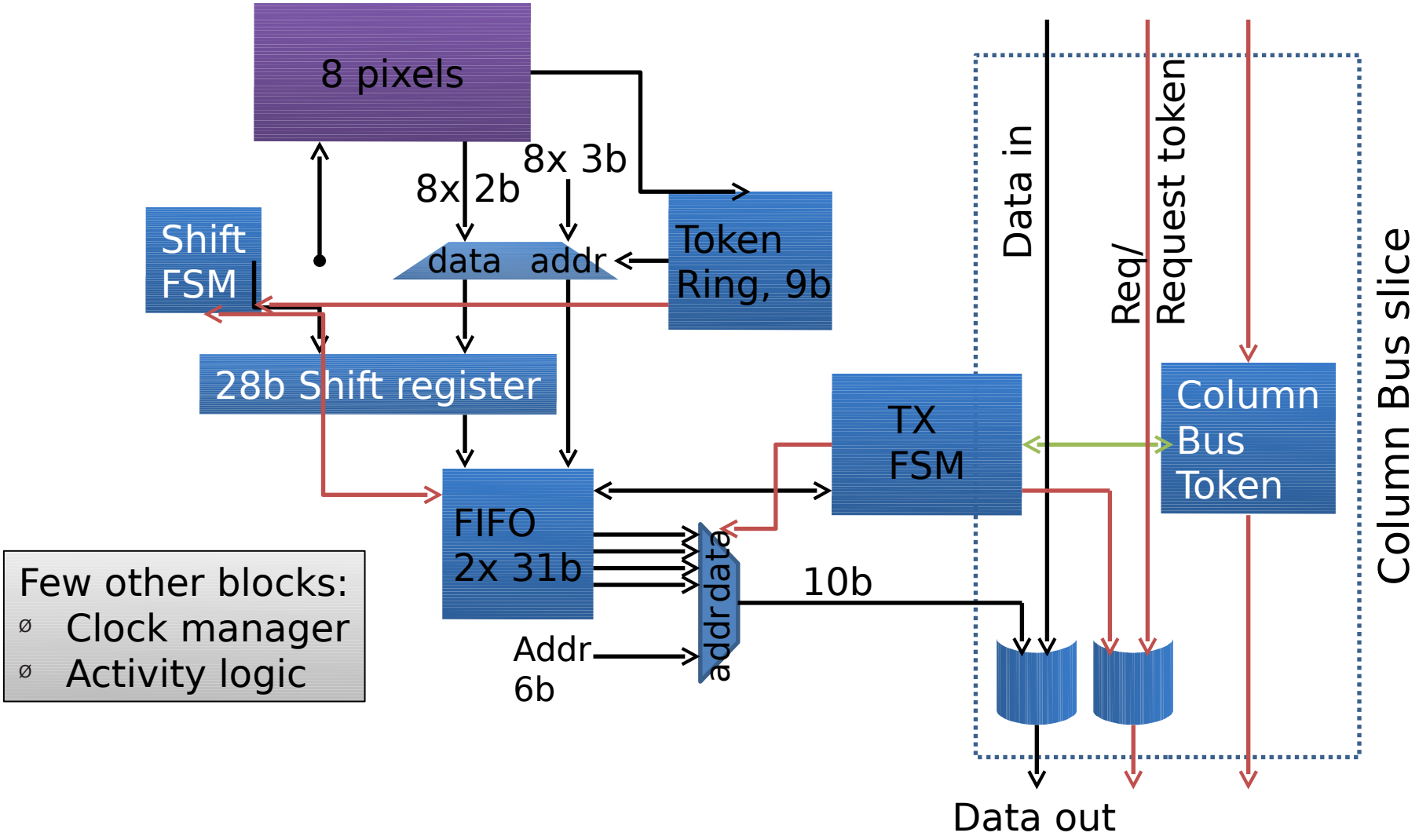
Digital pixel block diagram



Pixel design considerations

- Asynchronous FSM to gate the clock => power optimization, AFSM: 0.5 µW, 1 DFF 1µW
- Reset all counters by shifting => area saving by using DFF without reset (- longer reset)
- Latch-based clock gates for counters => glitch free clock + area and power savings
- Final optimizations: Test different FSM encodings, test different control signal polarities (using Verilog macros)

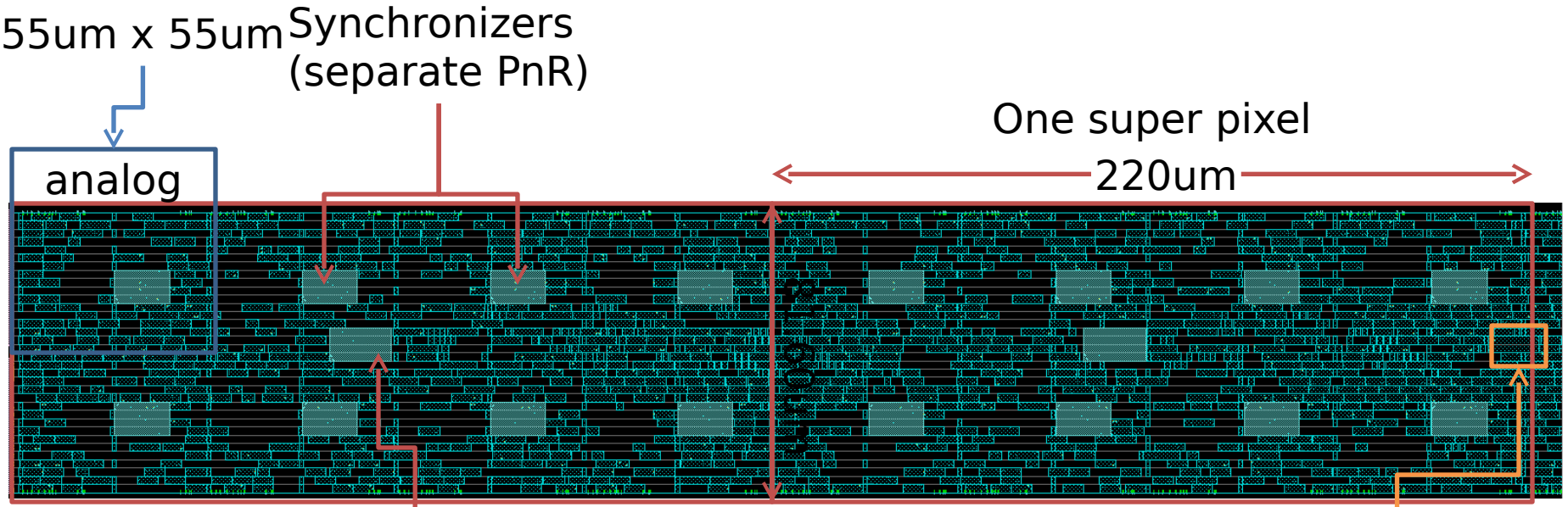
Super pixel block diagram



Super pixel design considerations

- Bring data from pixels at few nodes (2b) => less routing overhead (- more latency/dead-time)
- Latch-based clock gating => less dynamic power, area savings
- No muxes in FIFO input/output, “fall-through” architecture => area savings (- small latency)
- Asynchronous communication with EoC => simpler STA, robust against PVT (- more latency)
- Partly flattened design (RTL compiler) =>

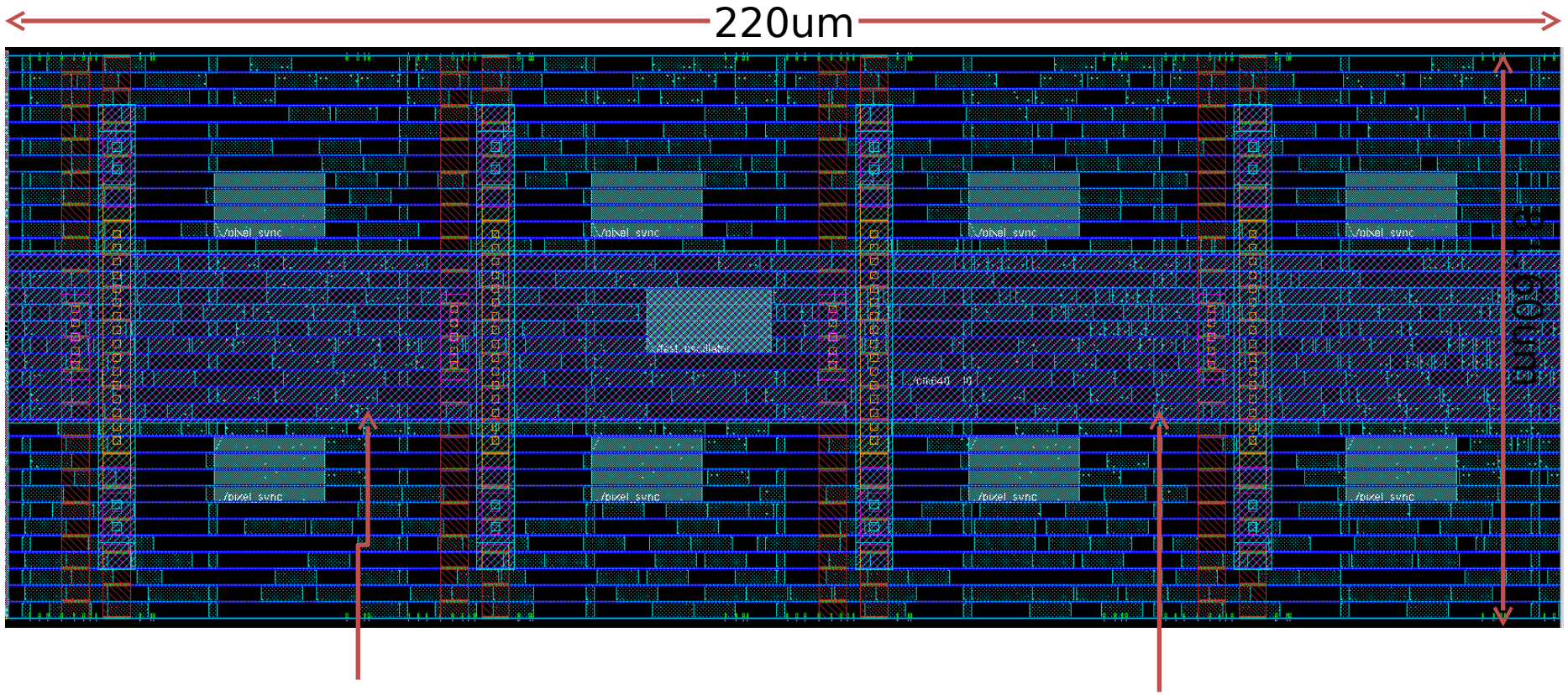
Super pixel floorplan



sical building block of matrix: 4x super pixel 81.60um x 880um

SP Power distribution

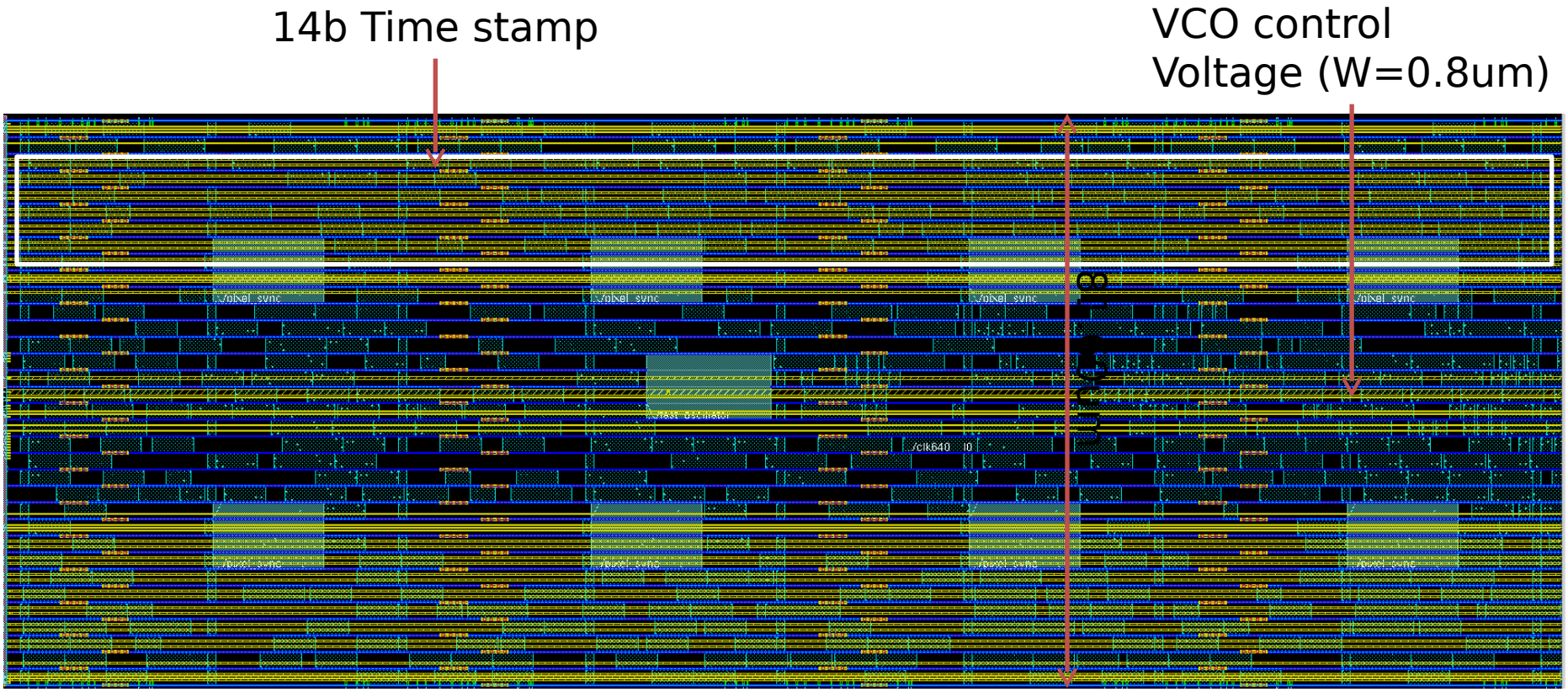
Digital power budget: 1 A / 128 columns = 7.8mA.
Peak current per column: 25mA (for a 100mV VDD drop)



VDD: MA (M8), W=25um, R= 3.94 Ω

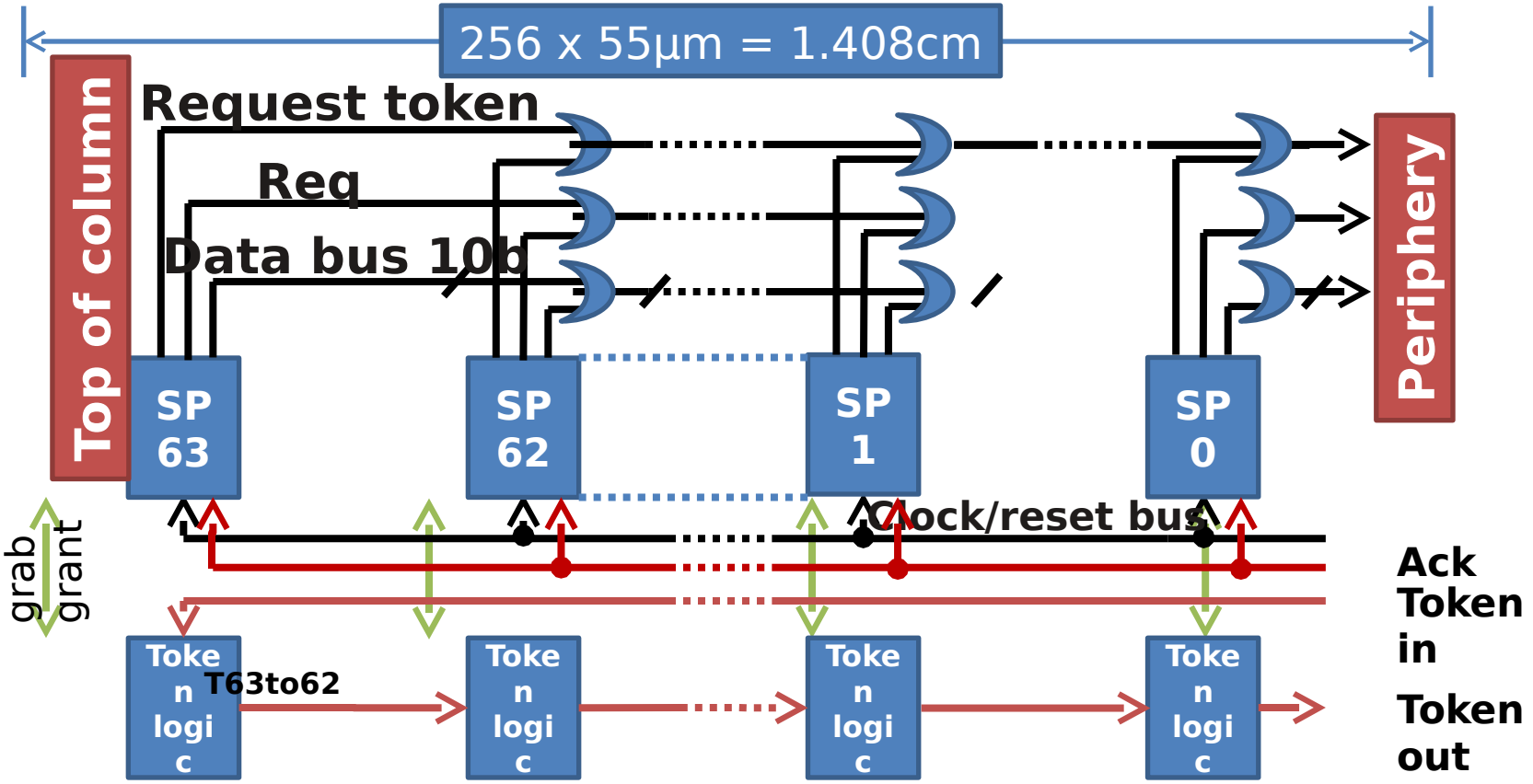
GND: E1 (M7), W=3.37 Ω

SP Global signal routing



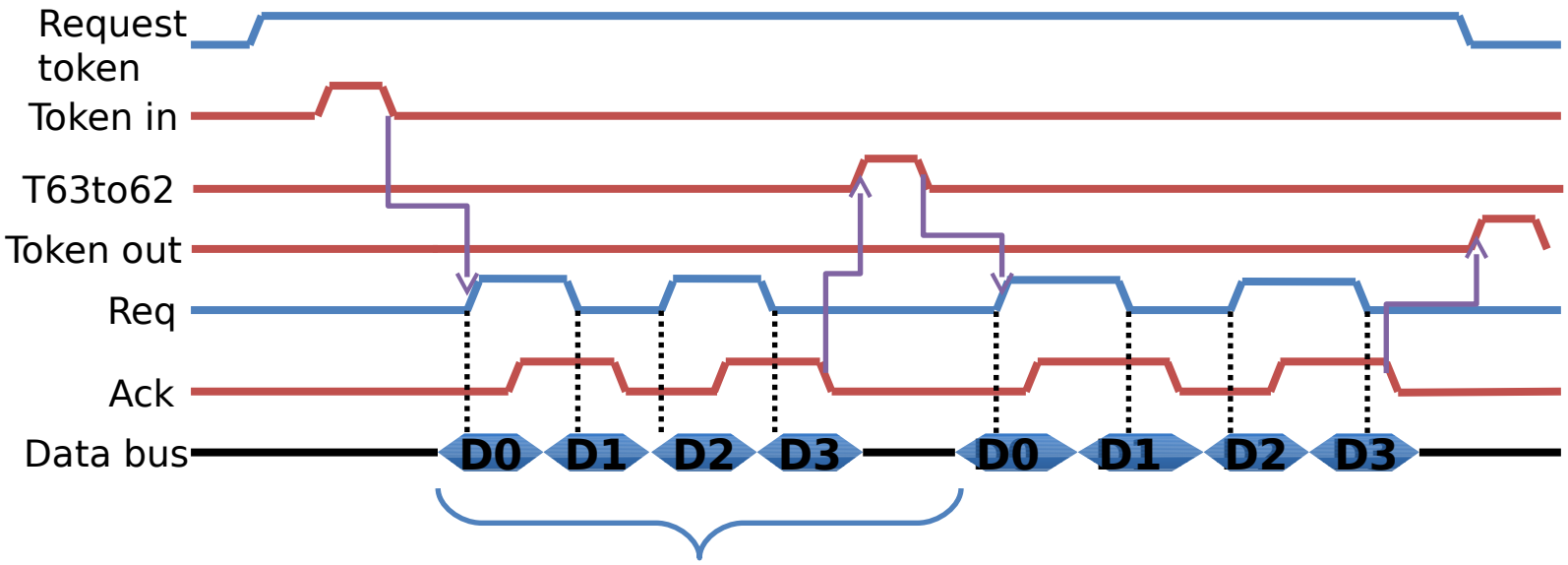
l lines driven from EoC (except clock):
l synchronous signals buffered using BUFFER_O.
sed BUFFER_D for non-timing critical signals.

Super pixel to EoC data transfer



Super pixel to EoC data transfer cont.

synchronous communication respect to the clock signal. The clock used only cally.

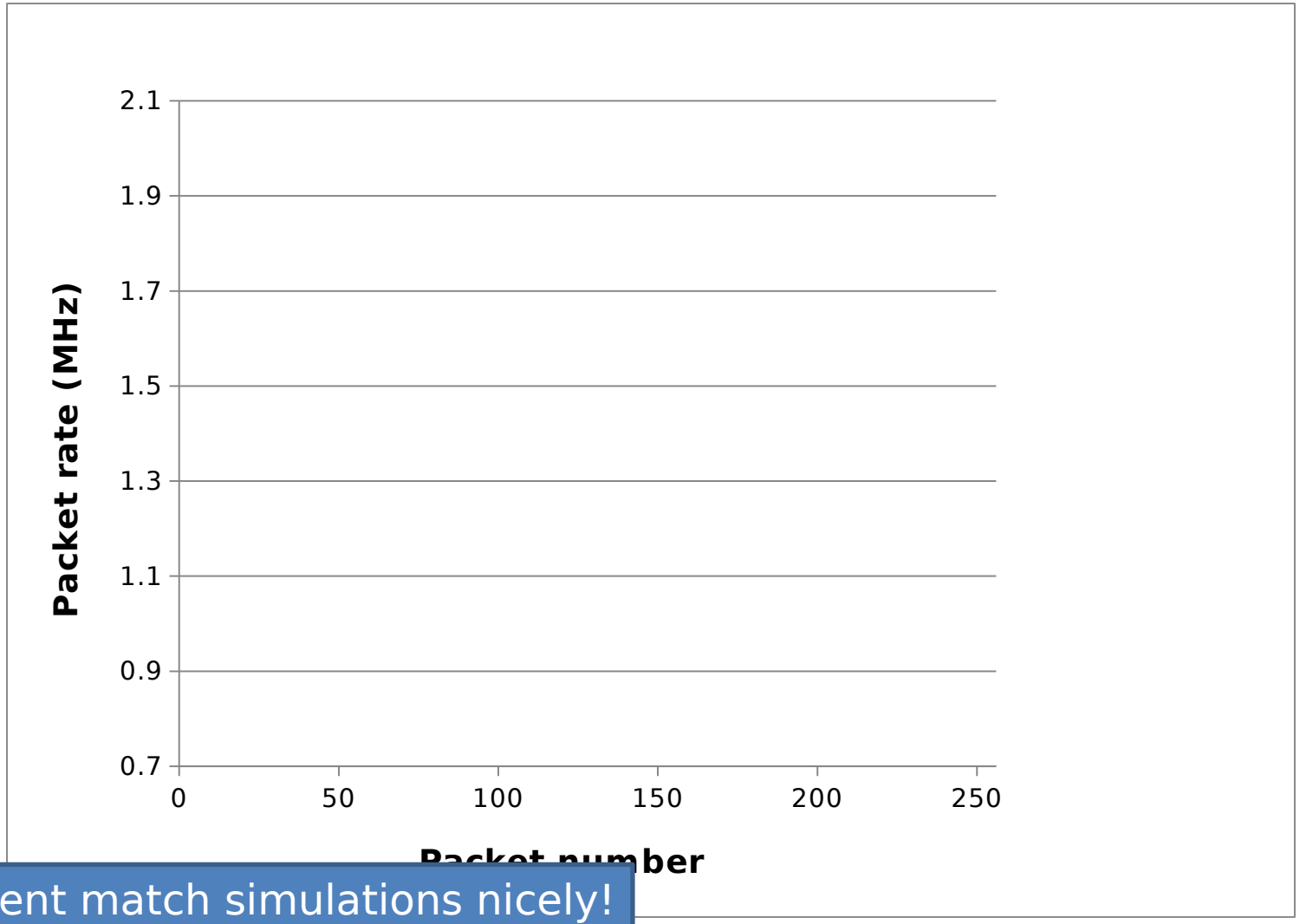


Packet period: 700ns - 2400ns*

Depends on SP address and column occupancy.

*Slow corner SS/1.4V/125C°

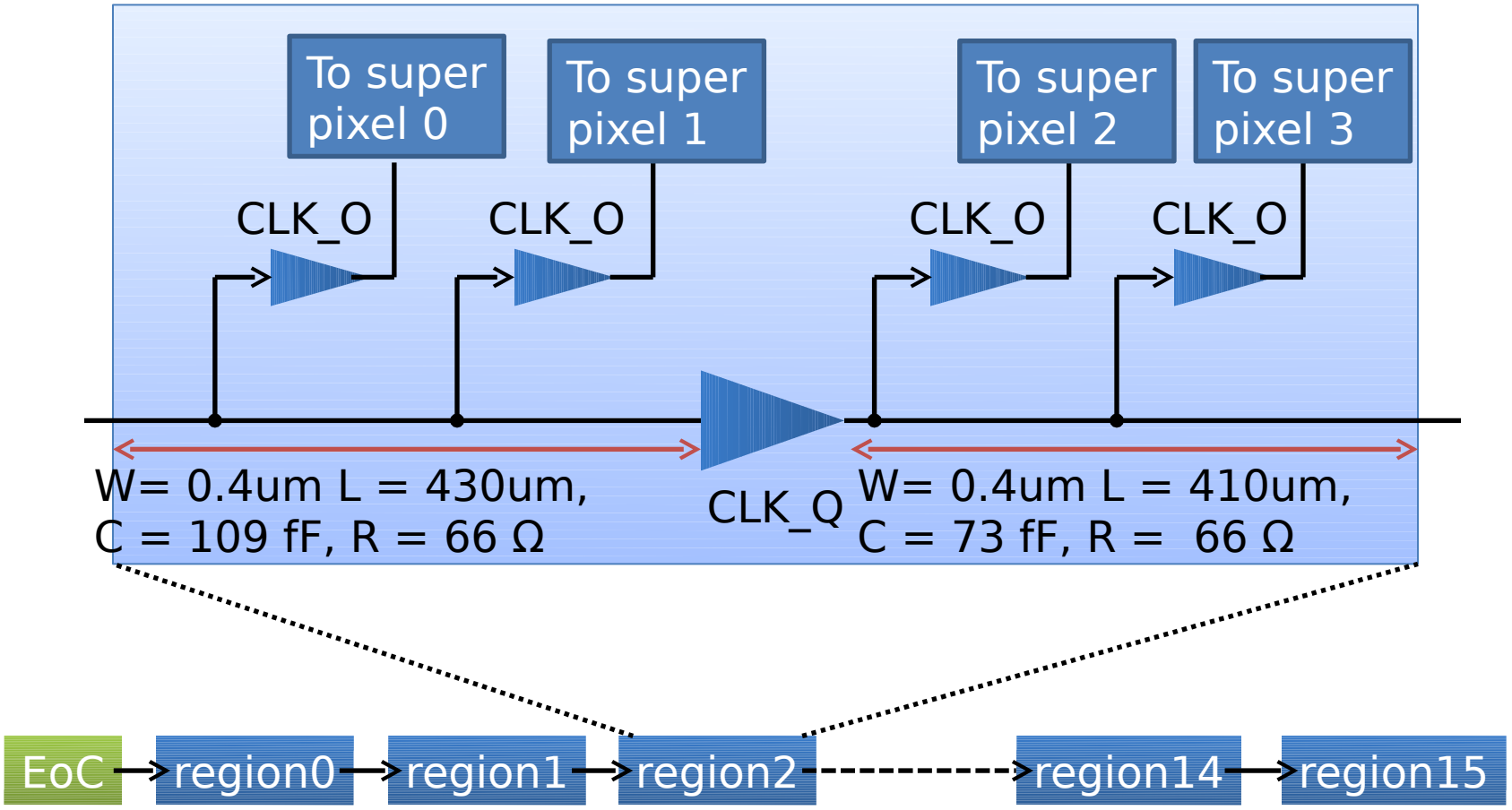
Packet rate in one column



easurement match simulations nicely!

Column clock distribution

- Clock tree split into 16 identical regions.

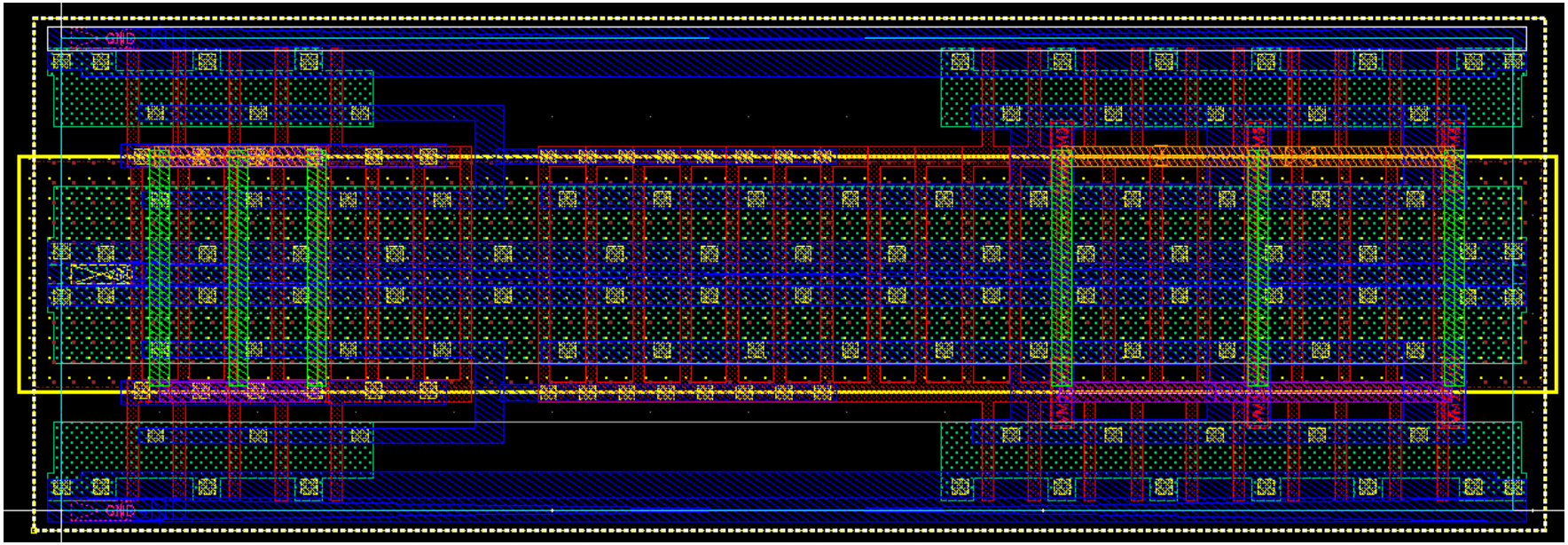


Clock buffer sizing

Regular Vt transistors used.

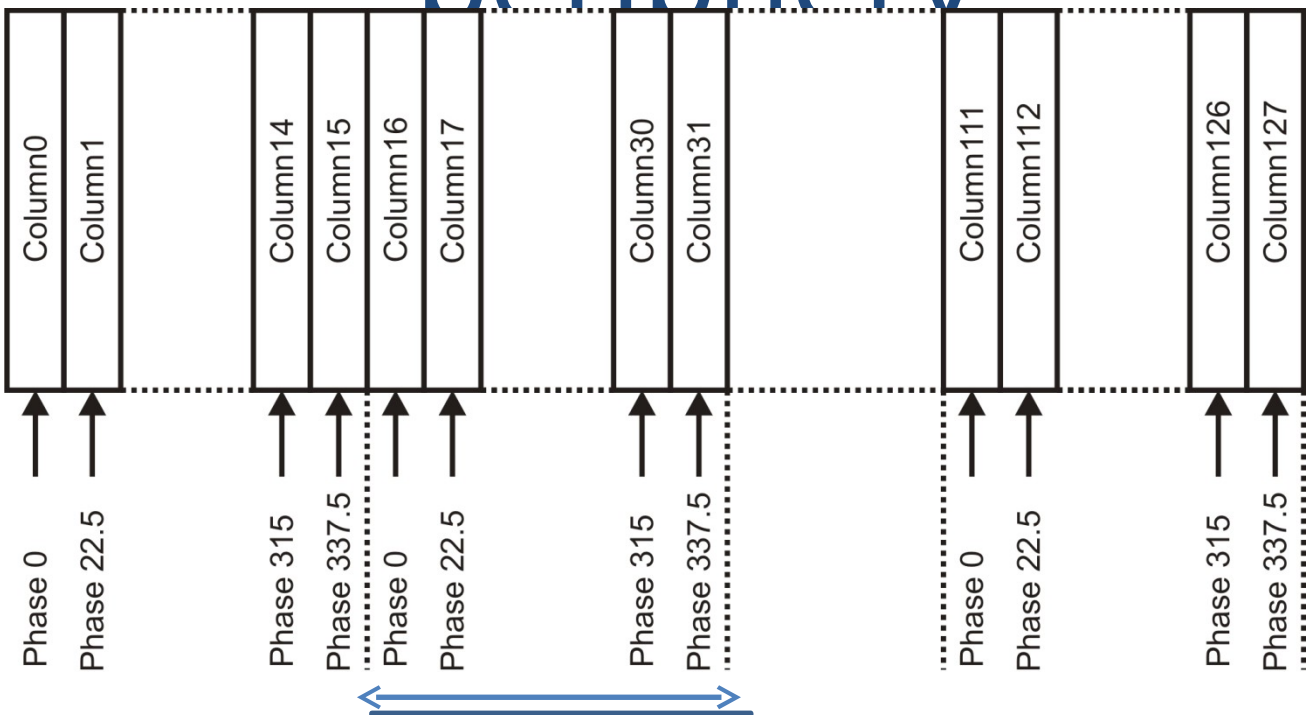
First stage:
3x PMOS: W=1.8um, L=0.12um
10x NMOS: W=0.57um, L=0.12um

Second stage:
20x PMOS: W=1.8um, L=0.12um
20x NMOS: W=1.8um, L=0.12um



Custom clock buffer CLK_Q layout (4.8um x 14.8um).

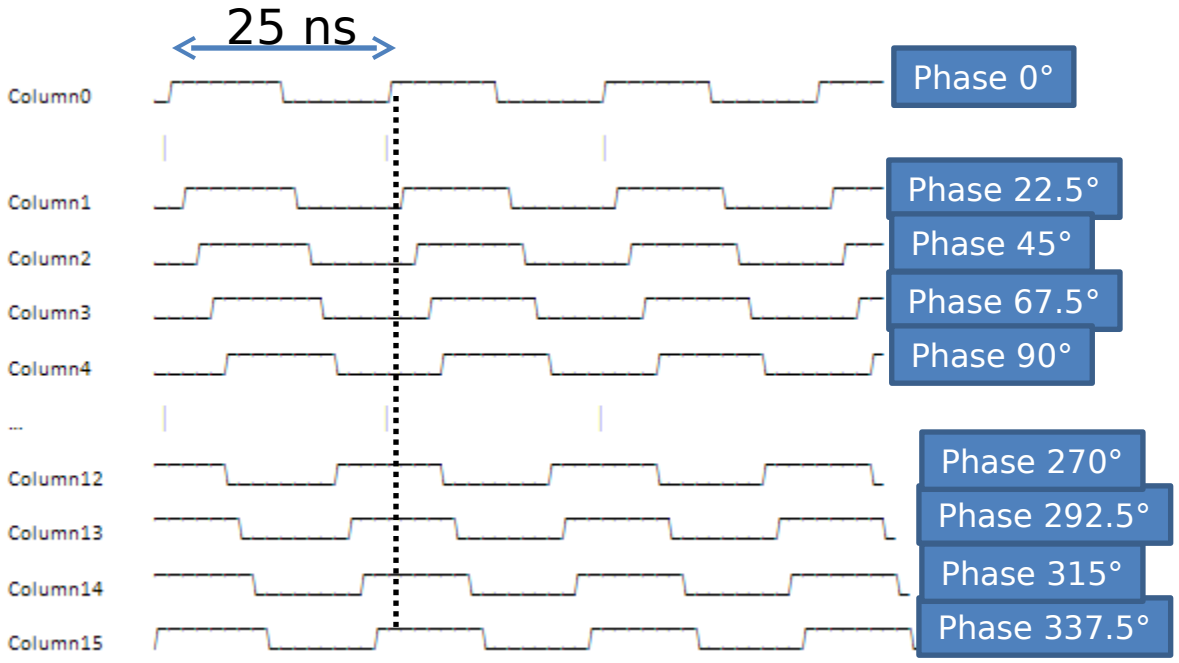
Clock Tree distribution in periphery



16 phases per 16 columns.

Routed in SoCE as a zero skew, fully balanced clock tree.

Phase-shifted clocks in 16 columns



Timing Diagram 1. 16 phase-shifted clocks in the periphery.

very 16th column has the same clock phase (configurable, lock phasing can be changed)

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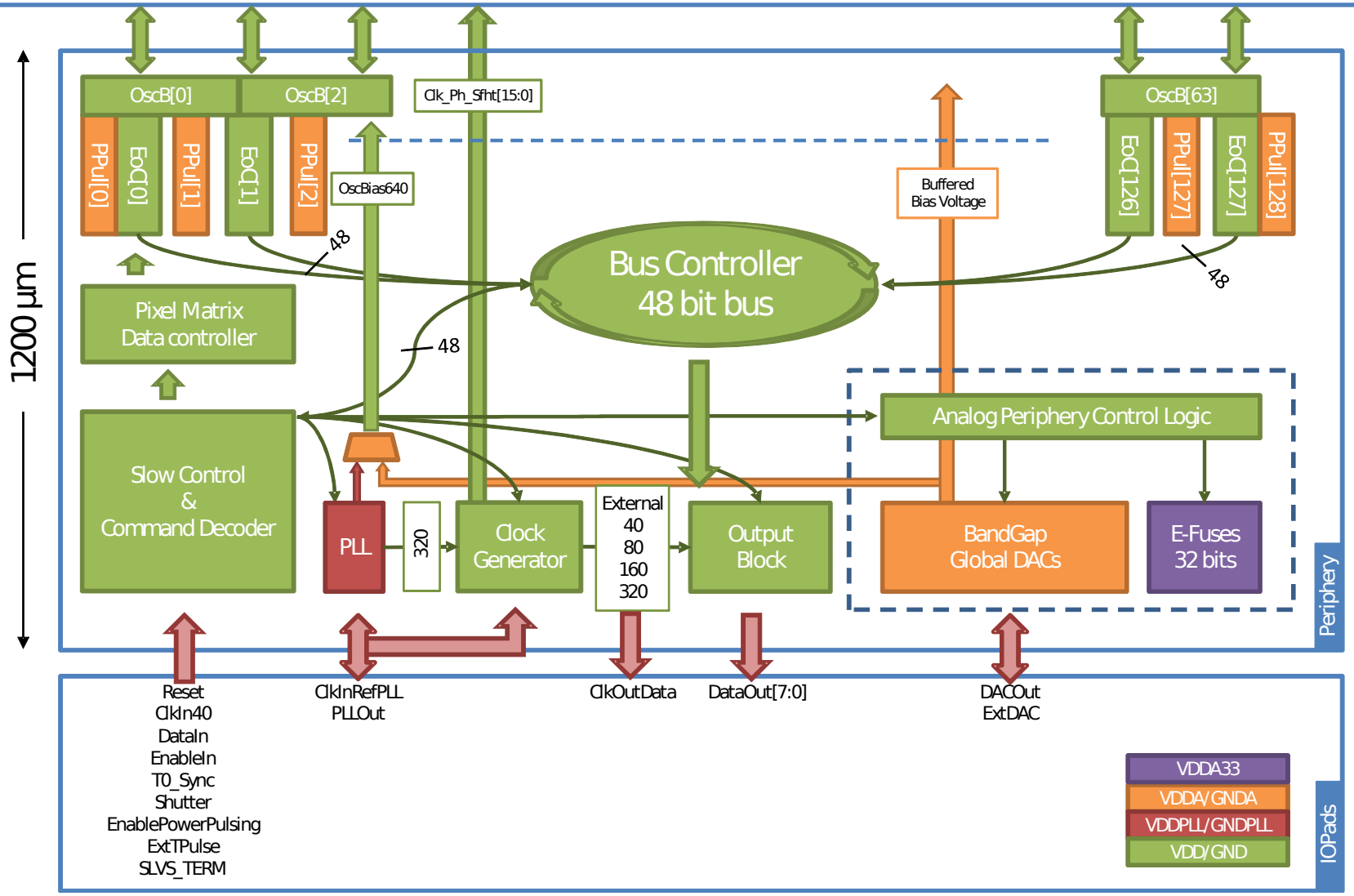
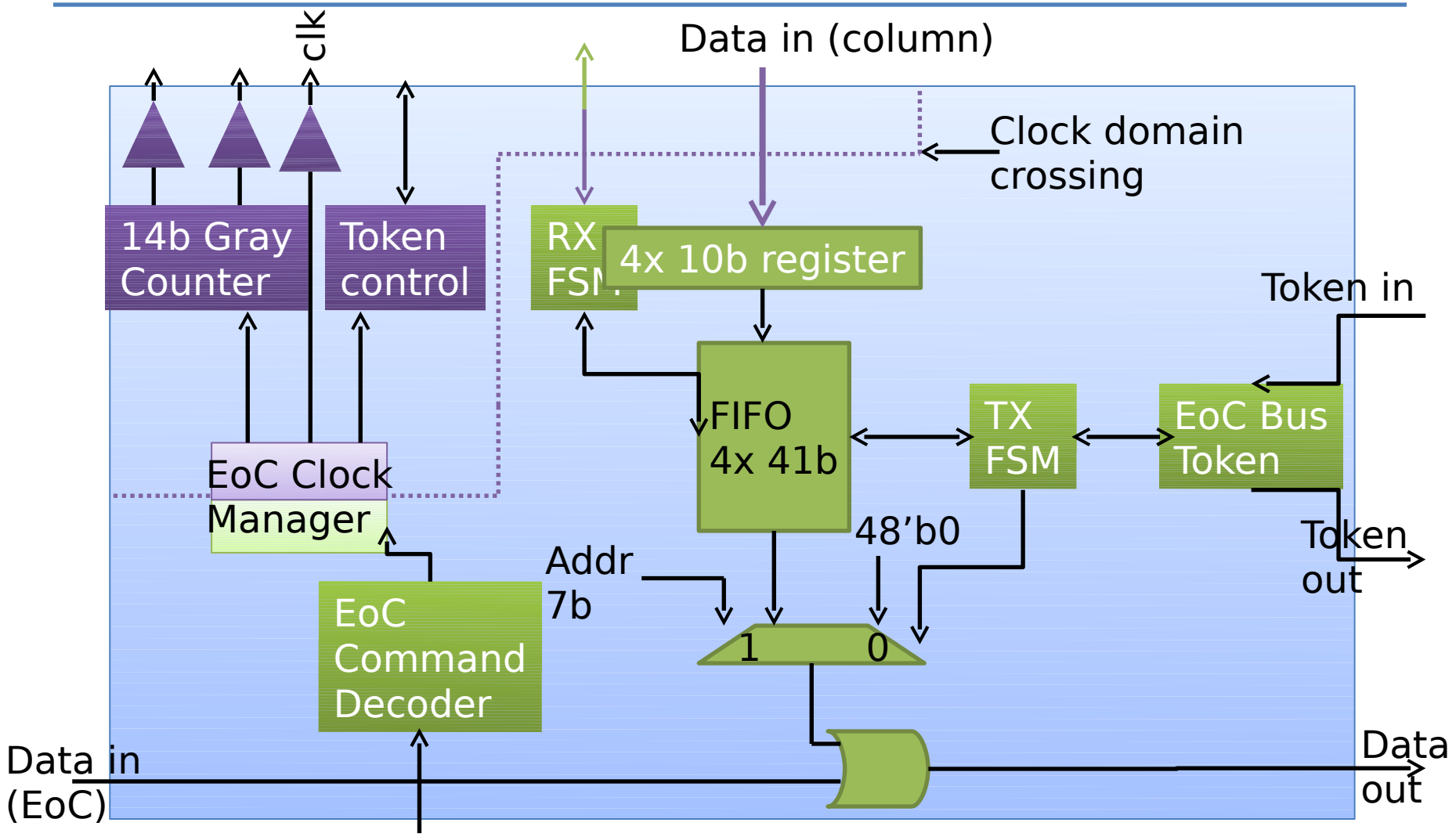
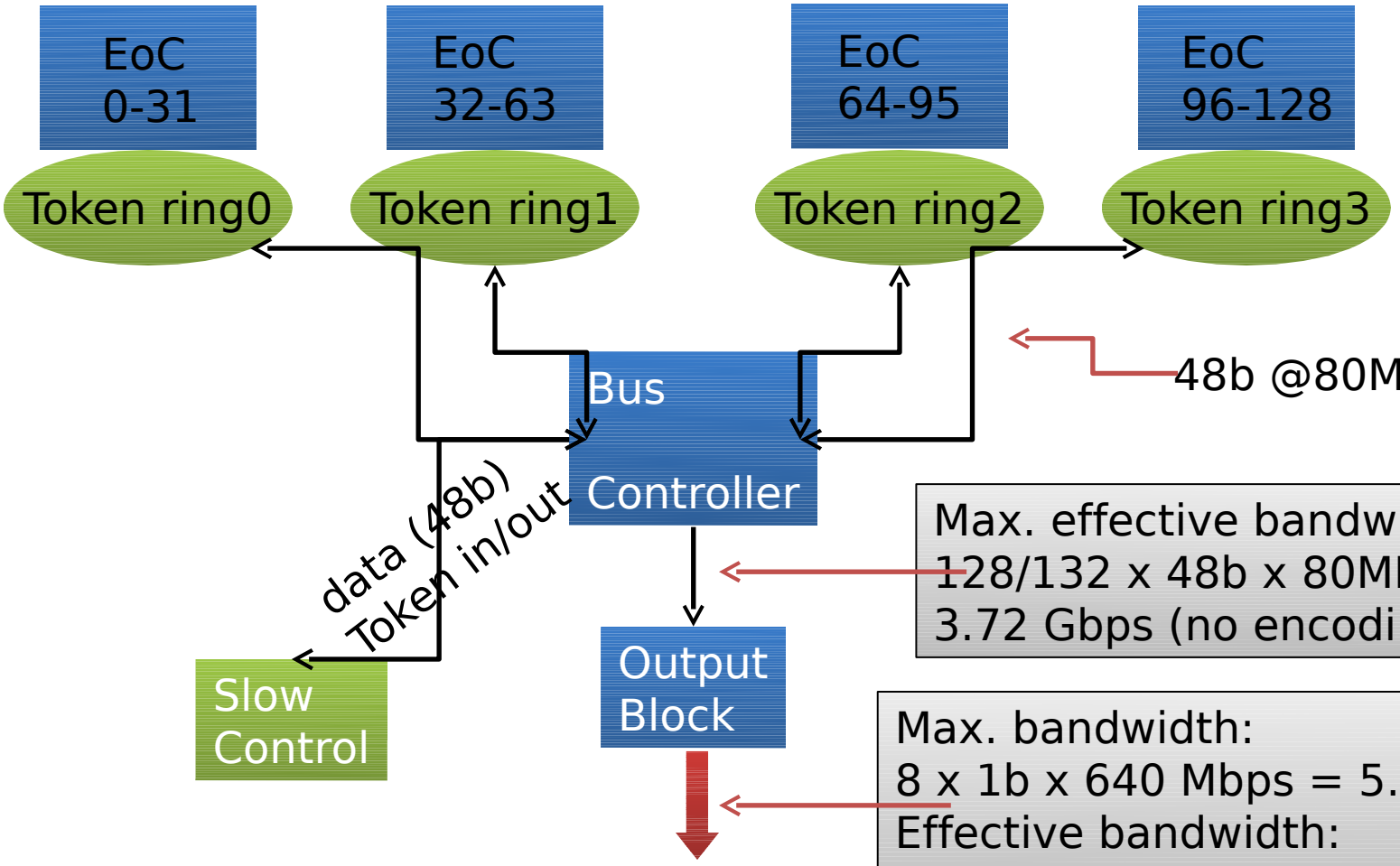
Periphery overview



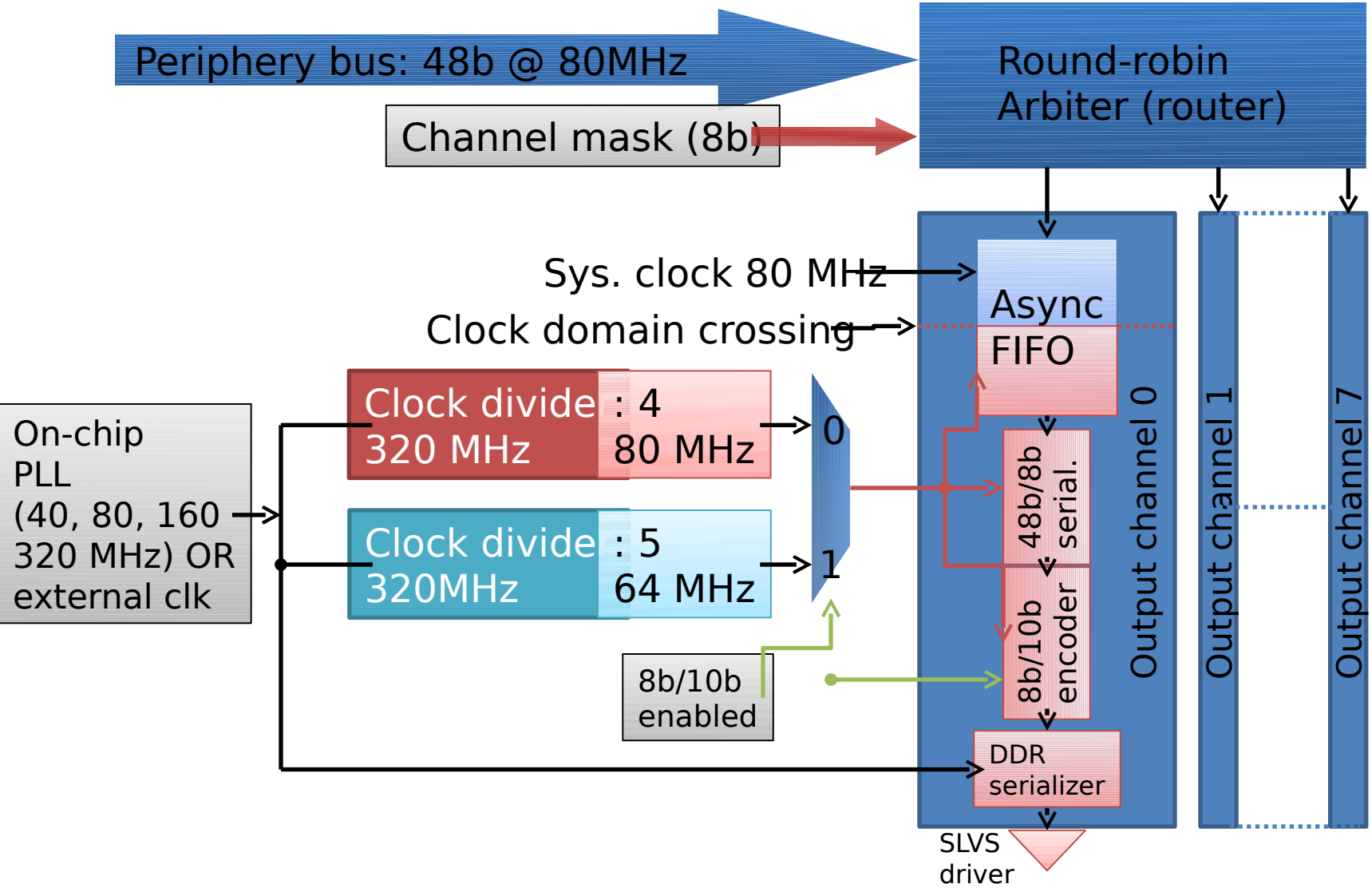
End-of-Column logic



Logical EoC bus structure



Output Block



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Design tools and languages

- RTL Design language: SystemVerilog
- RTL Synthesis: RTL Compiler 9.12
- Place n Route: SoC Encounter 9.12
- Simulation and verification: IUS 9.2, Open verification methodology (OVM), SystemVerilog
- Scripting: Perl (regression runs, code generation, netlist editing)
- Library characterization: ELC 9.12
- Repository: CLIOsoft

Timepix3 current status

- Readout architecture fully functional (some small “features” discovered)
- Simulations and measurements match very well
- Wafer probing will start in coming weeks
- First test beams planned for ~March 2014 with sensors on top of Timepix3

Thank you for your attention!

SPARE SLIDES

CERN High density (HD) 130nm library