Time-to-Digital Converter based on Time-Difference Amplifier (From single TDA to column-parallel TDC)

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Outline

- Introduction
- Time Difference Amplifier (TDA)
- Time-to-Digital Converter (TDC)
- Column-parallel TDC
- Conclusion

Application of TDC

- Jitter measurement
  - Timing requirement becomes higher
- Digital PLL
  - TDC performance influences the PLL jitter or spurious noise
- Time-of-Flight
  - 1ps resolution means 0.15mm range accuracy
- Bio-medical application
- High energy physics

Conventional TDC

Method	Reso.	Area
Inverter delay and counter	×	○
Vernier delay	○	×
Interpol.	○	×
Passive interpol.	△	○
Amp.	○	△

Our goal is to realize the higher resolution TDC employing an amp. with small area

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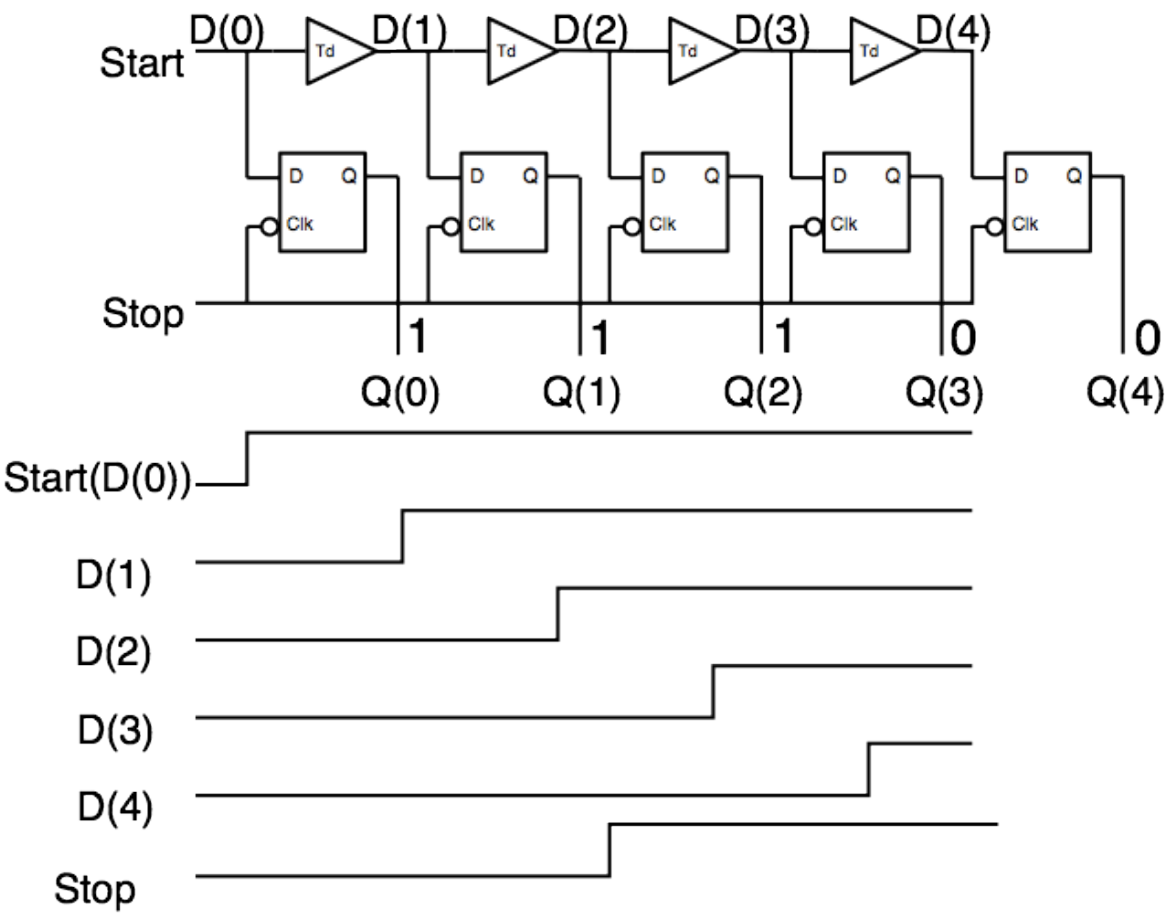
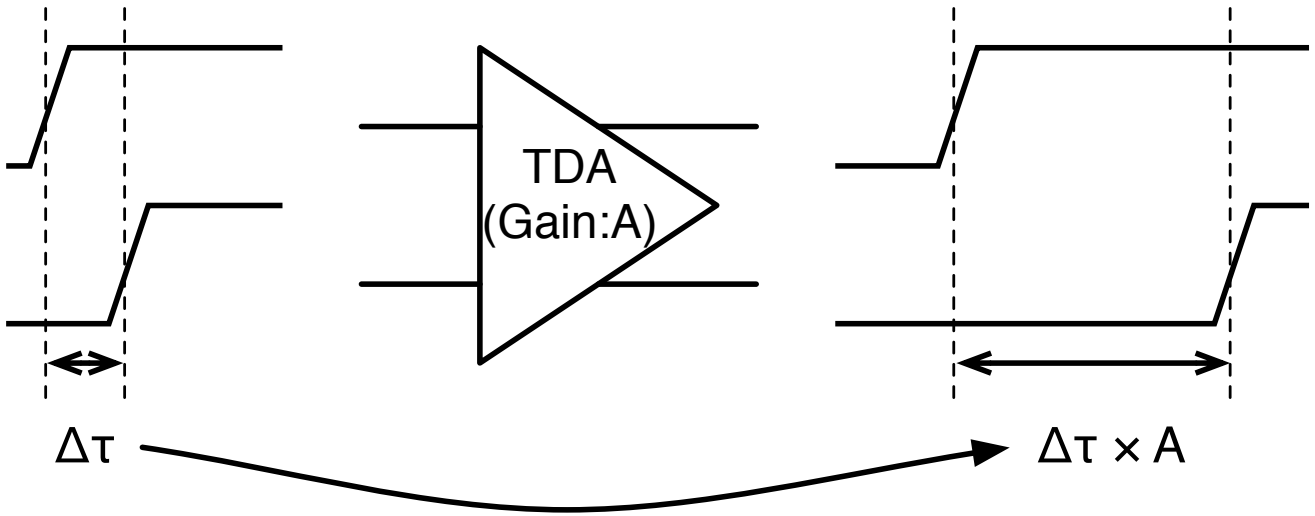
Time-to-Digital Converter



- A chain of buffers and flip-flops are often used
- As scaling of Tr., time resolution is higher
  - 180nm : about 30ps
  - 90nm : about 15ps
  - 65nm : about 10ps
- Minimum time resolution is limited by a buffer delay (gate delay)

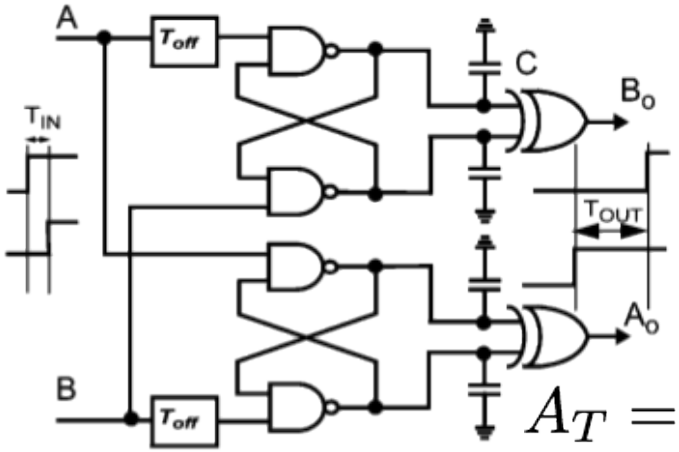
Time Difference Amplifier (TDA)



- Open-loop structure
  - simple structure, small area
  - Sensitive to process variation to result in gain mismatch
- Closed-loop structure
  - Complicated structure, large area
  - Strong to process variation

Conventional TDC using TDA

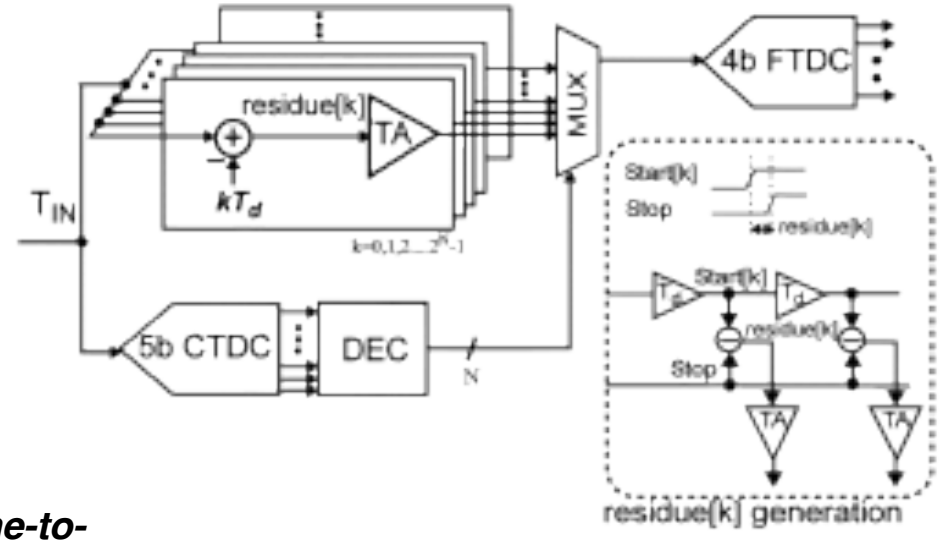
Time Amp.



$$A_T = \frac{2C}{g_m T_{off}}$$

M.Lee et al.,"A 9b,1.25ps Resolution Coarse-Fine Time-to-Digital Converter in90nm CMOS that Amplifies a Time Residue", JSSC 2008.

TDC



✓ **Advantage**

✓ **Drawback**

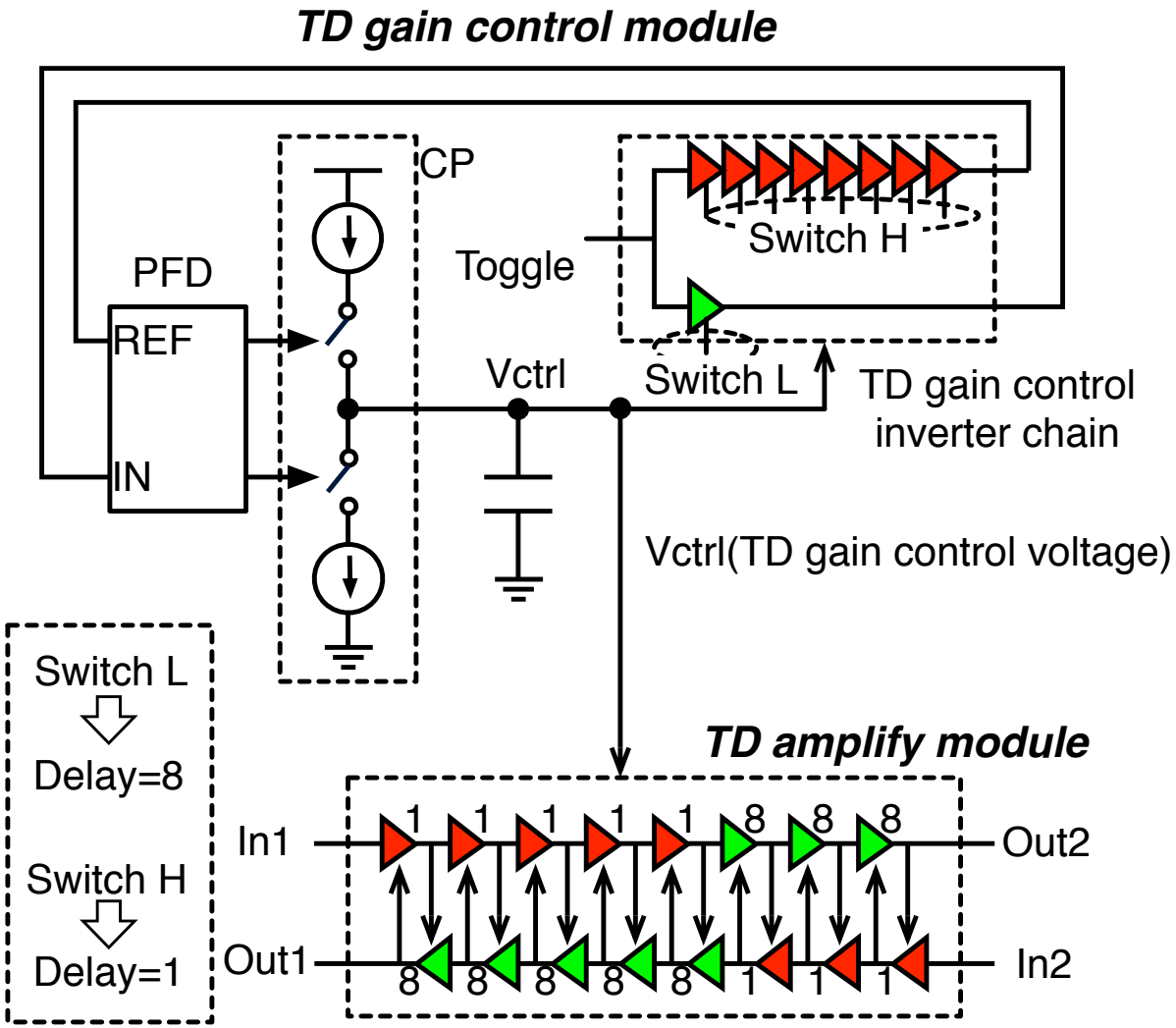
Open-loop

- ✓ High gain
- ✓ Simple structure
- ✓ Sensitive to PVT variation

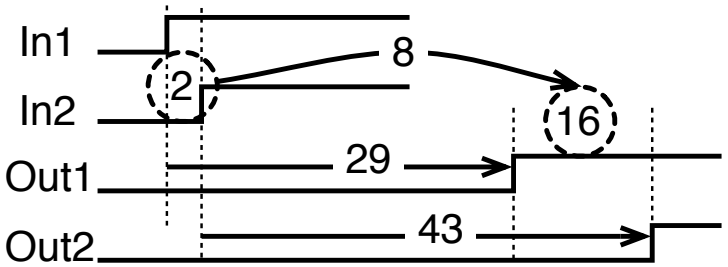
Closed-loop

- ✓ High resolution
- ✓ Redundancy
- ✓ Large area

TDA structure

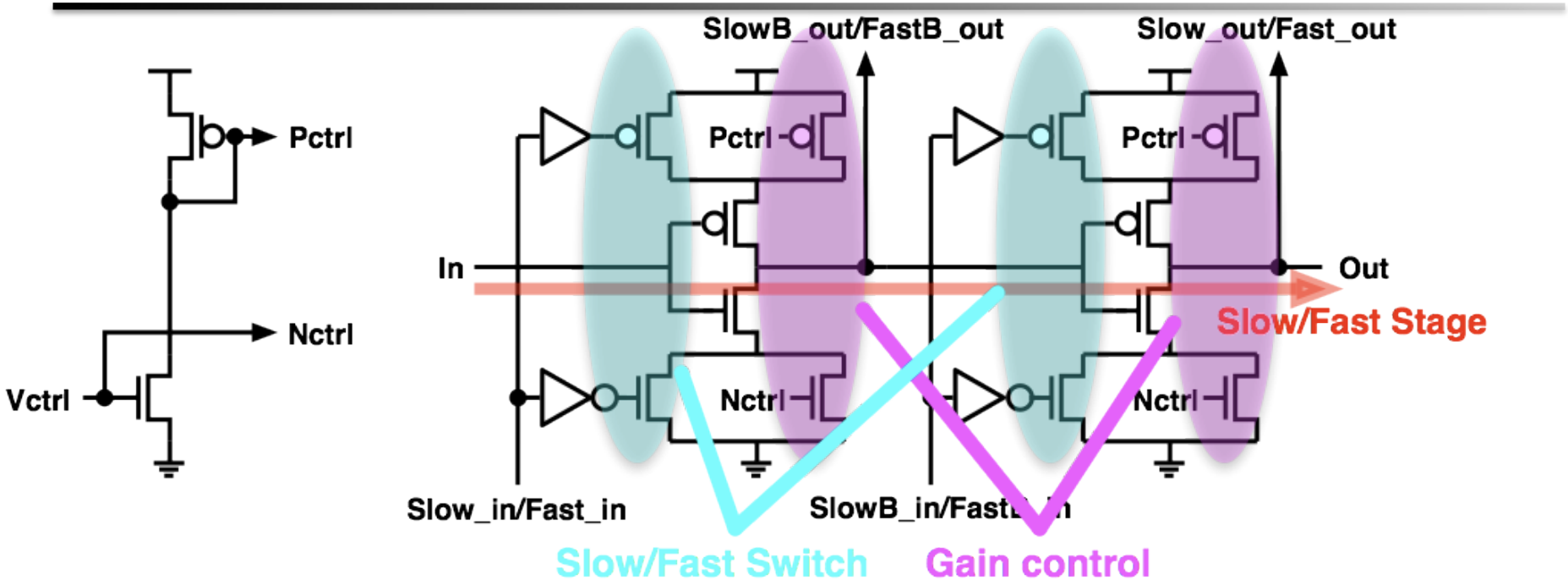


- Closed-loop gain control
- Gain control module
- Amplify module
- In this example, gain is 8

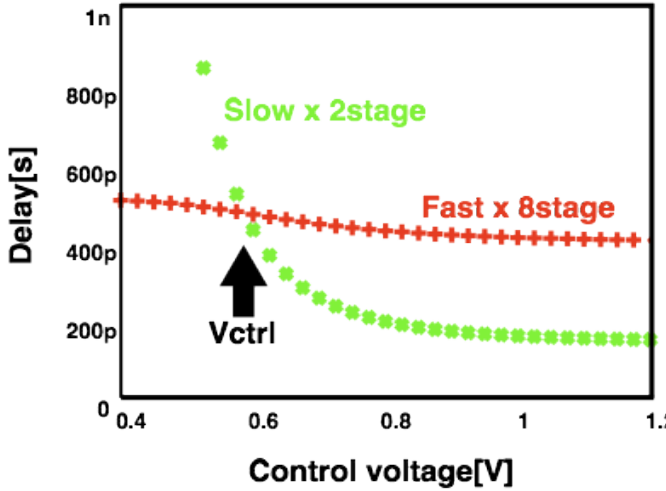


(T.Nakura, S.Mandai et al. VL 2009)

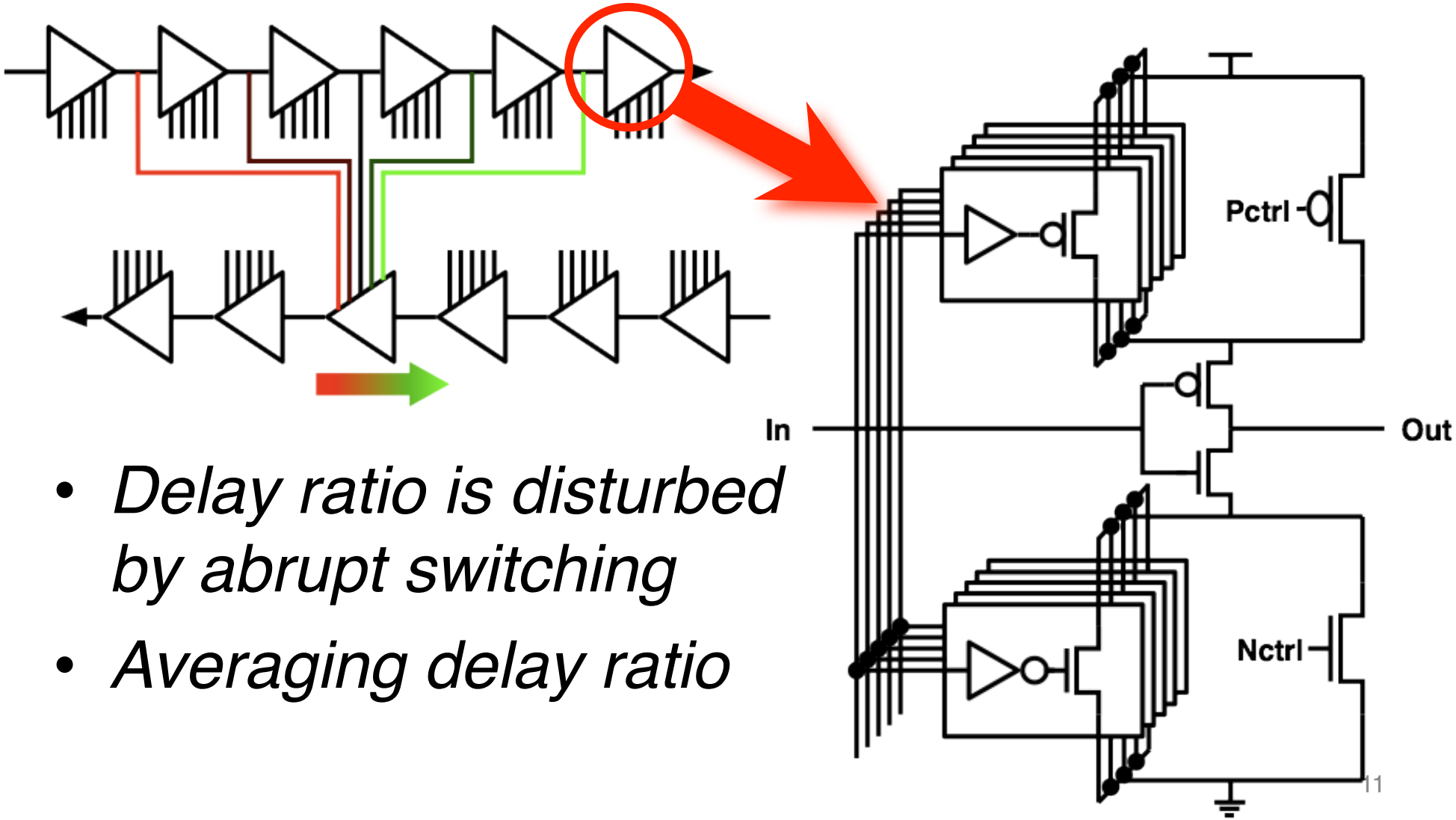
Variable Delay Cell



- *Fast/slow mode switches when left-Tr. is ON/OFF*
- *Delay is controlled by Vctrl for right-Tr.*

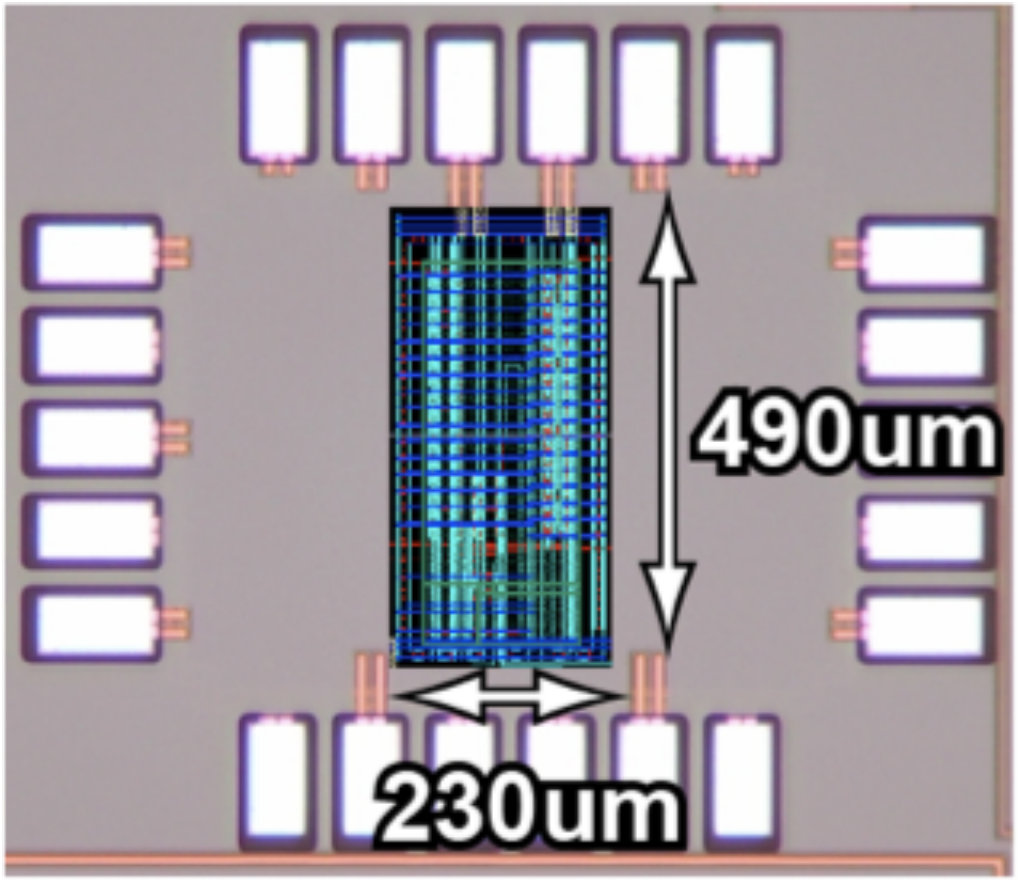


Soft switching



- *Delay ratio is disturbed by abrupt switching*
- *Averaging delay ratio*

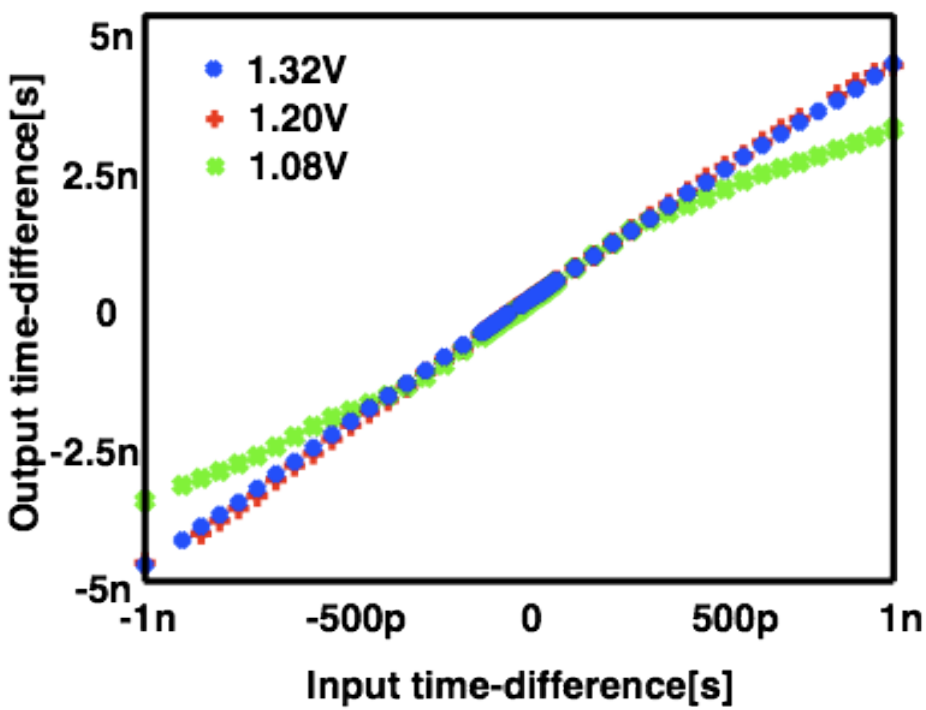
1st Chip Design of TDA

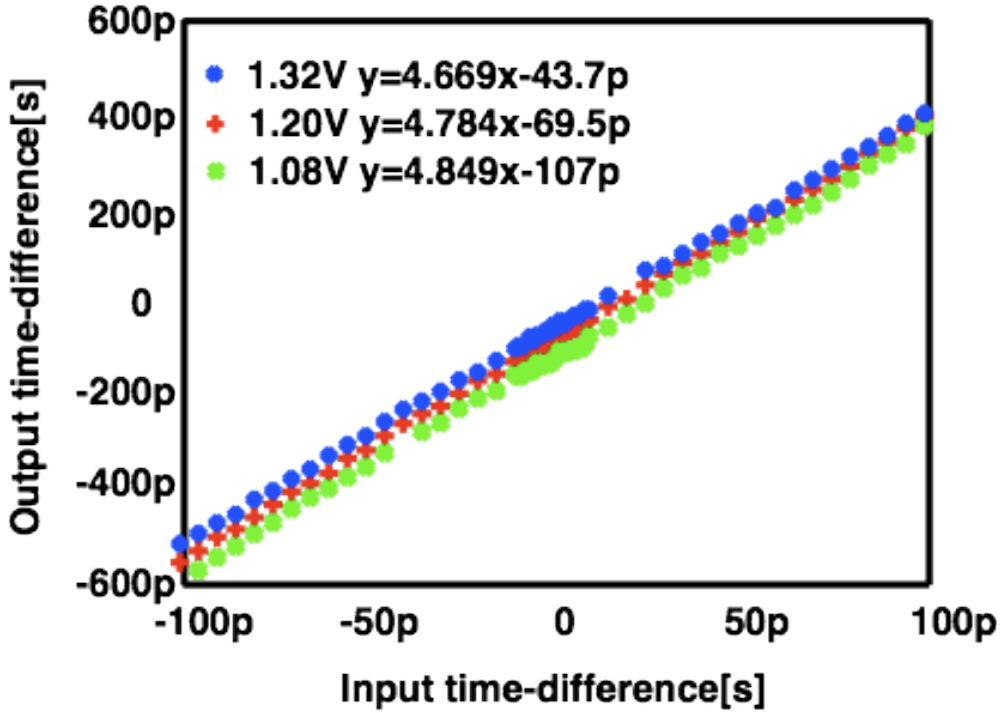


Process	65nm CMOS
Core Vdd	1.2V±10%
Temp.	Room temp.
Toggle freq.	5MHz
Gain	4.784±1.4%

(T.Nakura, S.Mandai et al., VLSI symp. 2009)

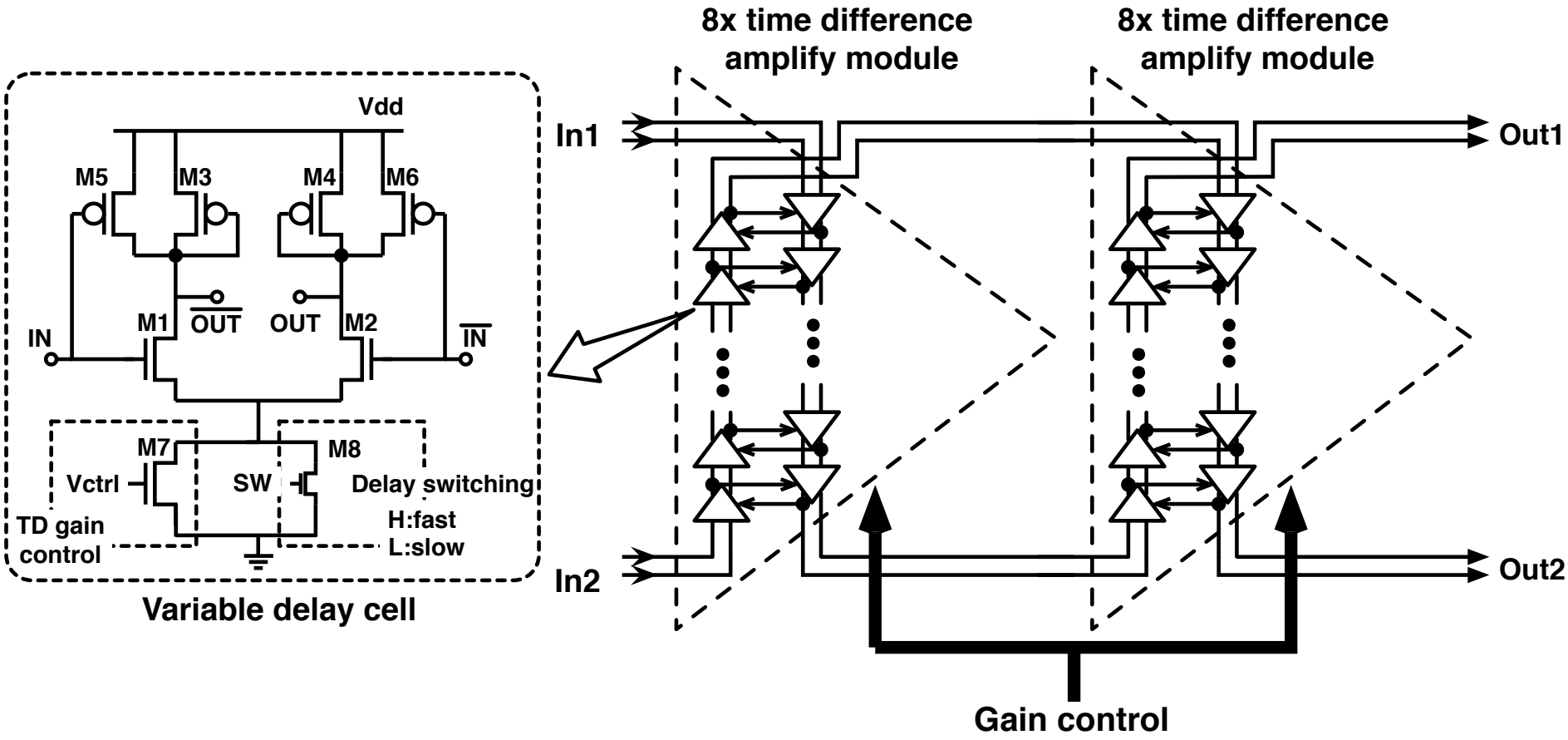
1st Chip Measurement Result





- *Gain is about 4, input linearity range is ±300ps*
- *Gain is acquired in only 1.4% fluctuation against ±10% power supply change*

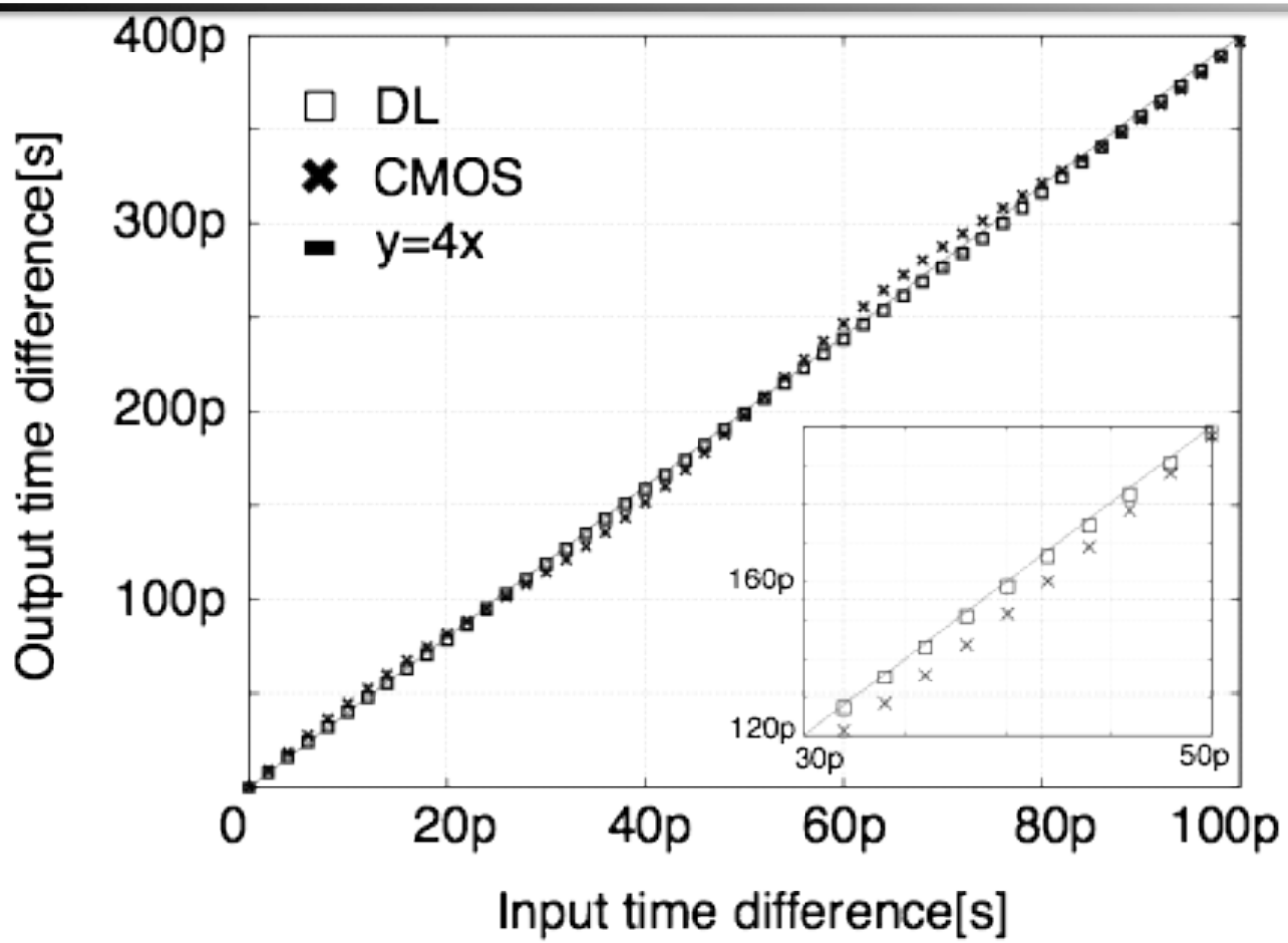
Cascaded TDA



(S.Mandai et al., ISOCC 2009)

By cascaded connection, gain become high
(In this case, a square)

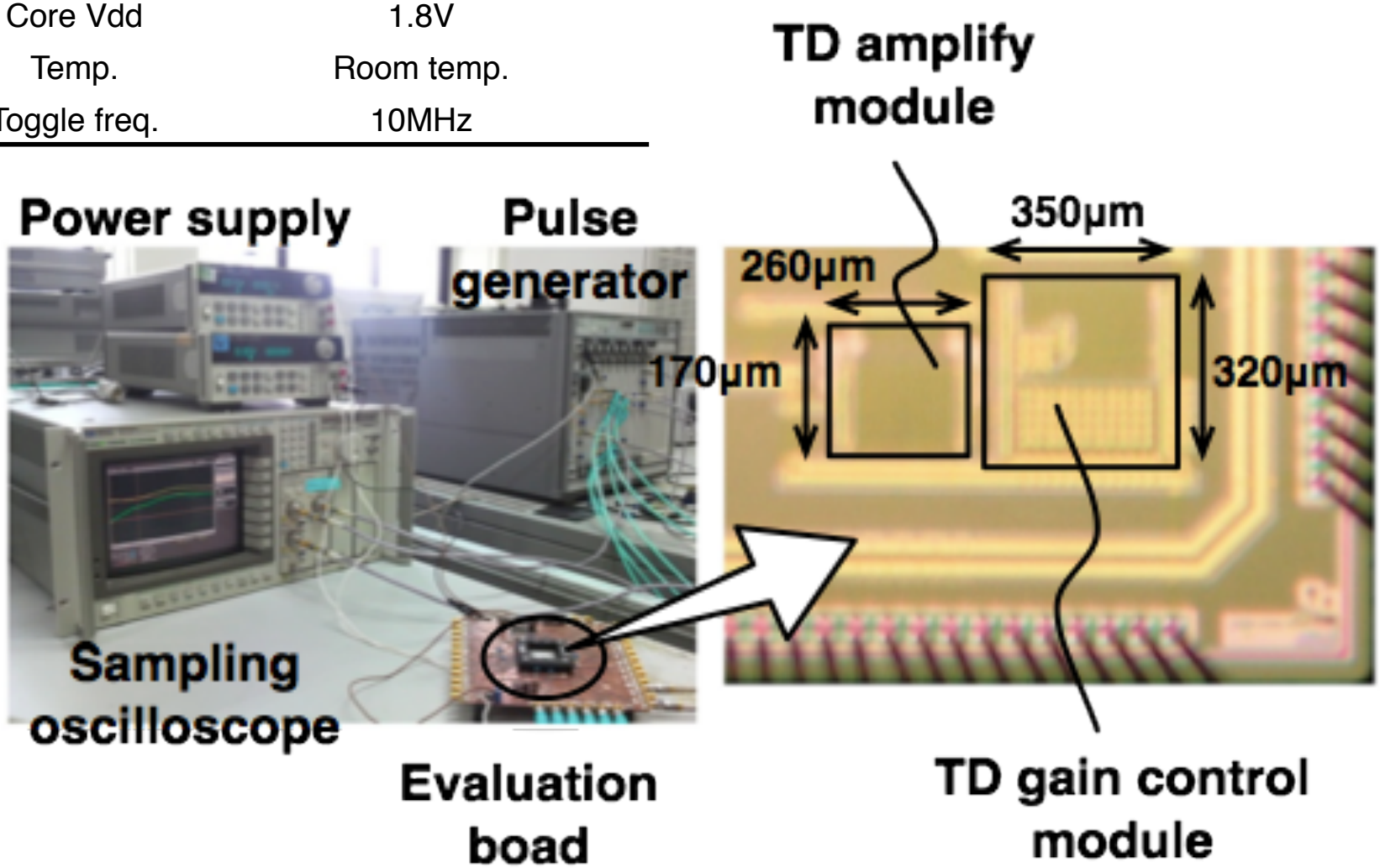
Comparison DL Cell and CMOS Logic Cell on Periodic Noise in Simulation



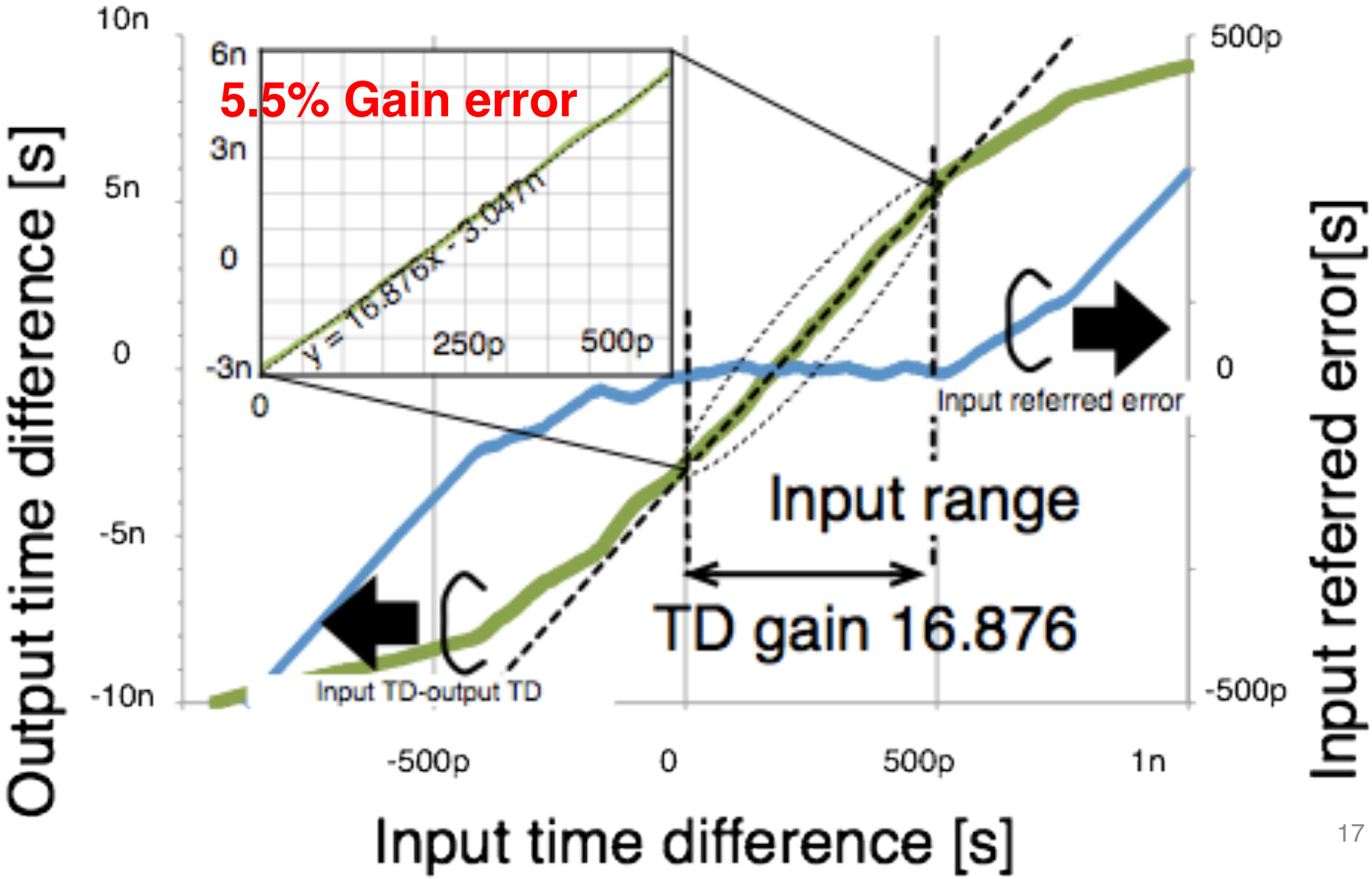
- *4x TDA simulation (Ideal: y=4x)*
- *Linearity is maintained in DL, periodic noise disappear*

2nd Chip Design

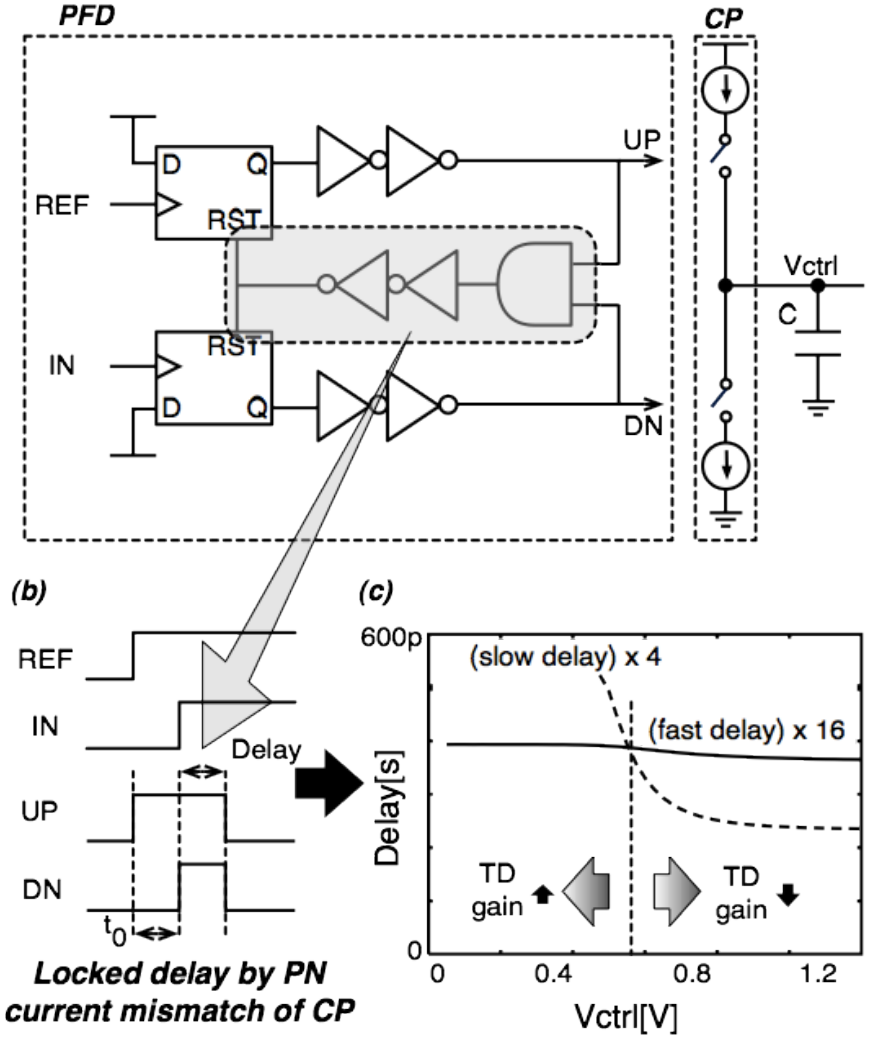
Process	0.18μm CMOS
Core Vdd	1.8V
Temp.	Room temp.
Toggle freq.	10MHz

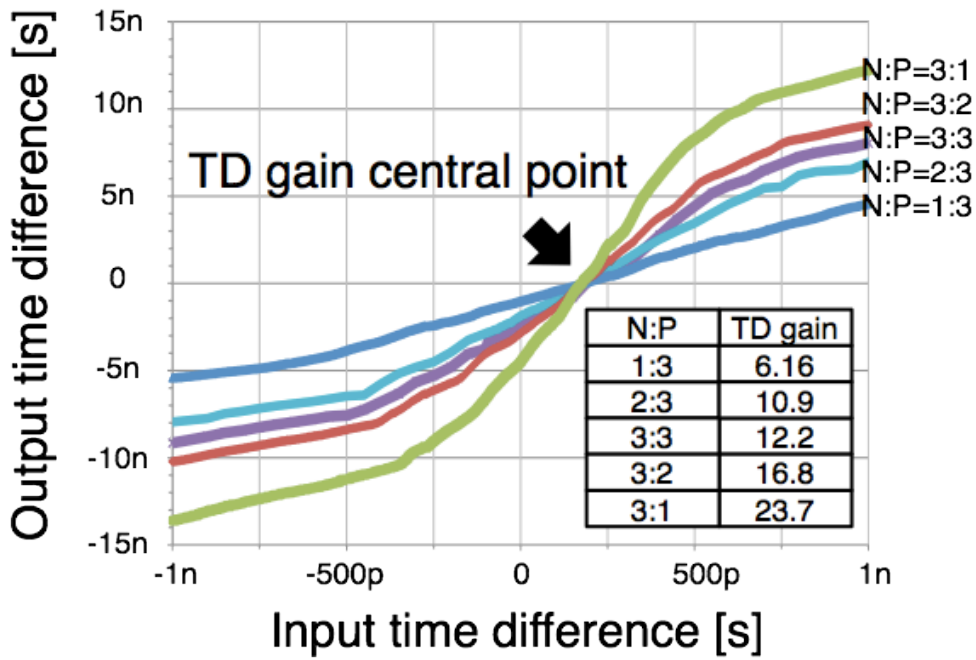


2nd Chip Measurement Results



TD Gain Offset





N:P	TD gain
1:3	6.16
2:3	10.9
3:3	12.2
3:2	16.8
3:1	23.7

- Current source mismatch of CP causes TD gain offset
- TD gain offset in each ratio of N, P current source of CP by measurement

Short summary

- I introduced TDA to realize high resolution TDC
  - Use closed-loop gain control
  - Cascade connection to realize high TD Gain
  - Employ differential logic delay cell for low noise
- I demonstrated measurement results
  - ±250ps input range
  - 5.5% TD gain offset (Ideal x16)
  - CP current source mismatch cause TD gain offset

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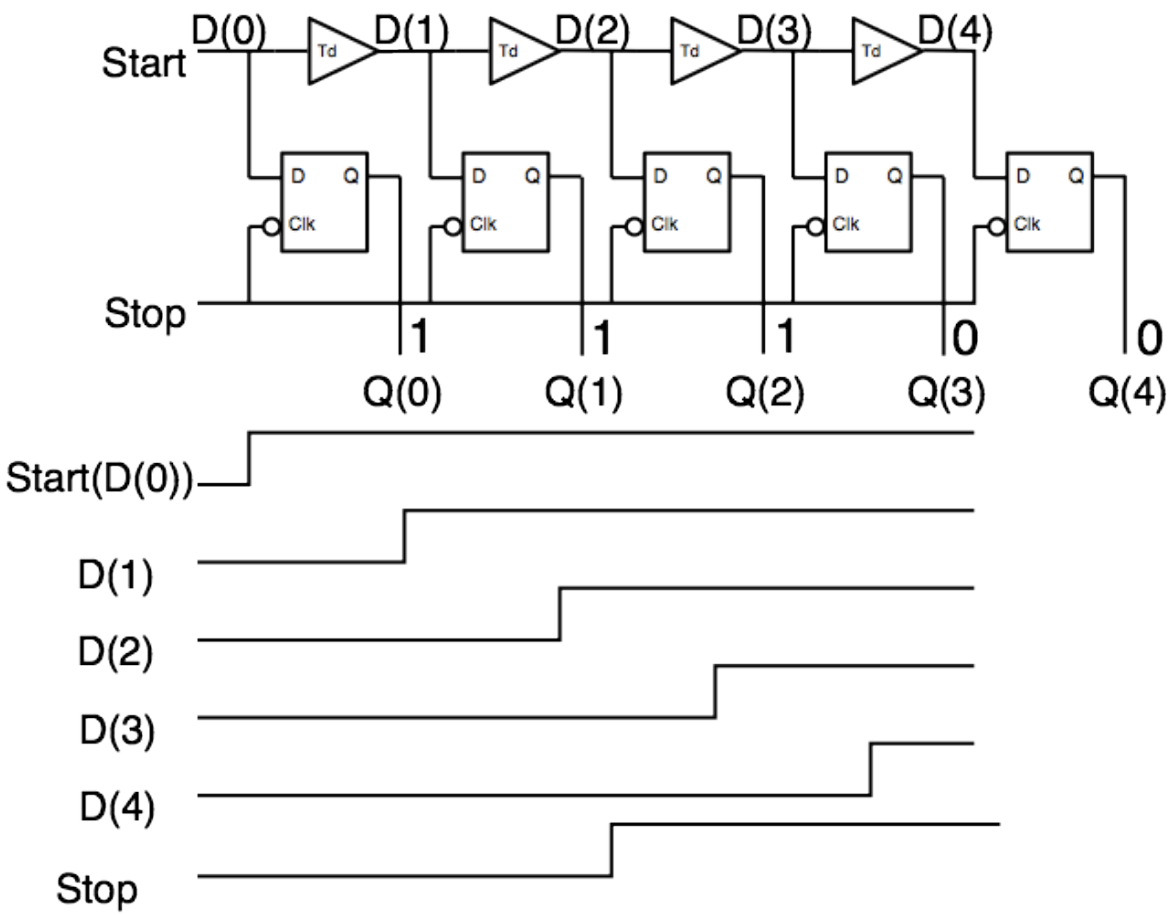
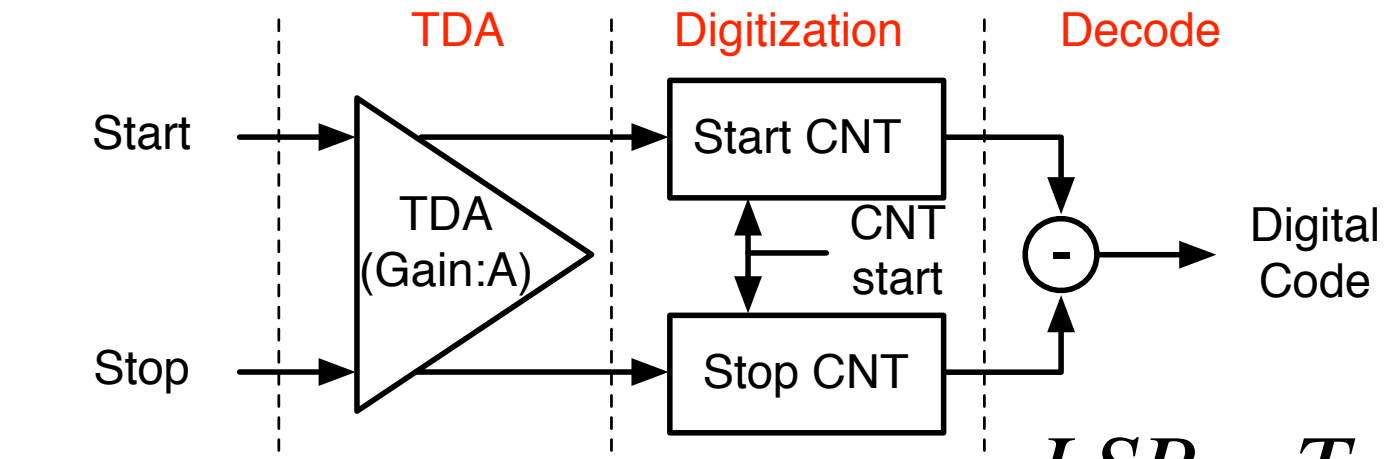
Time-to-Digital Converter

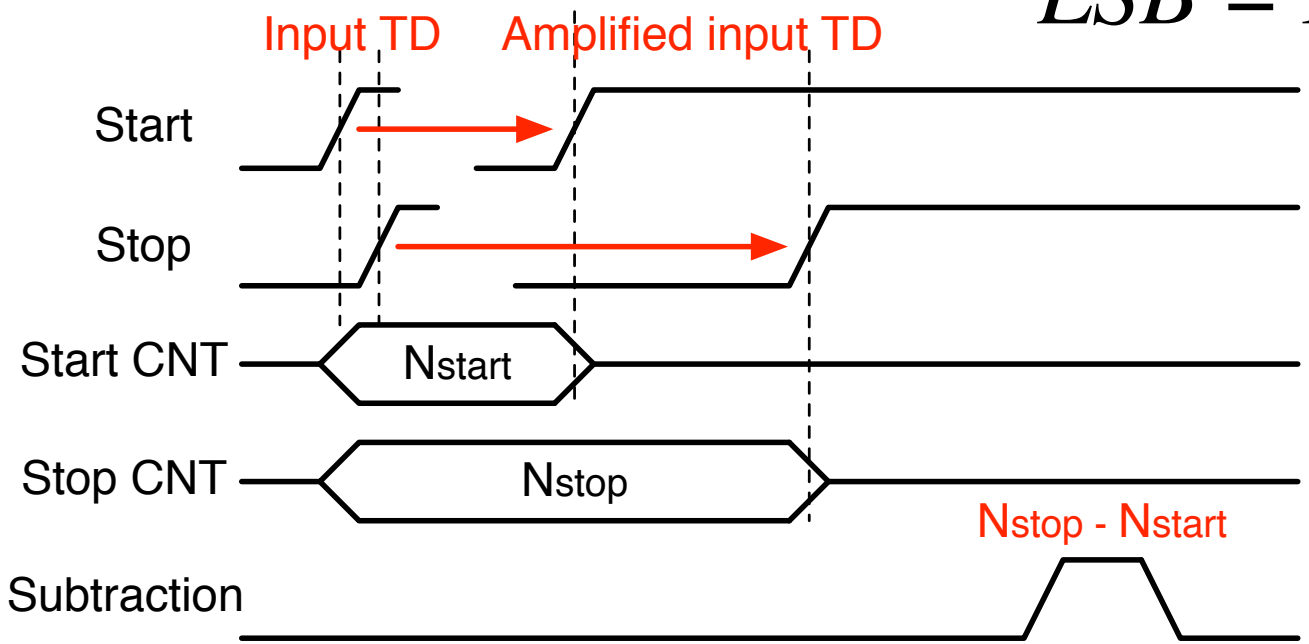


- A chain of buffers and flip-flops are often used
- As scaling of Tr., time resolution is higher
  - 180nm : about 30ps
  - 90nm : about 15ps
  - 65nm : about 10ps
- Minimum time resolution is limited by a buffer delay (gate delay)

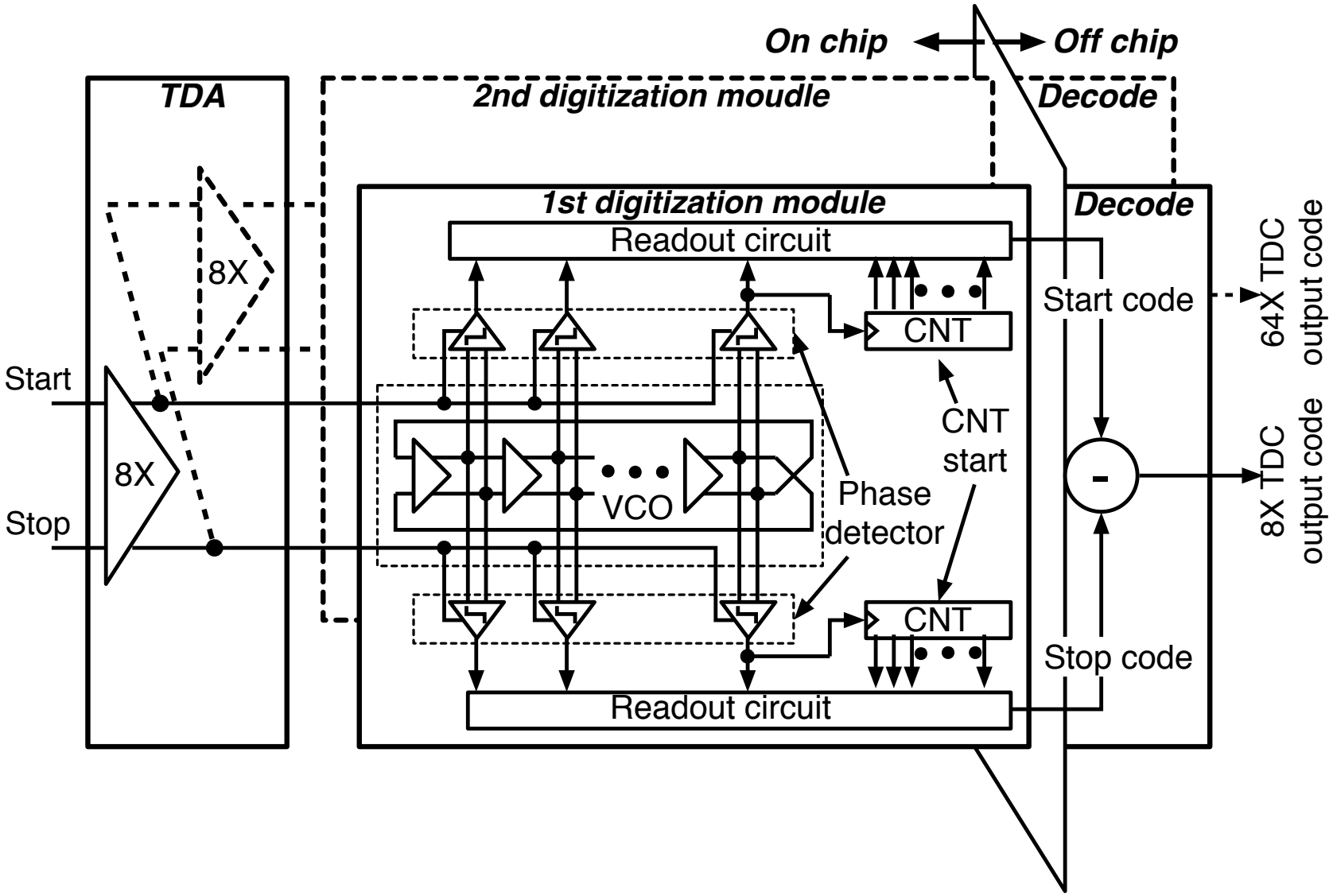
Concept of TDC



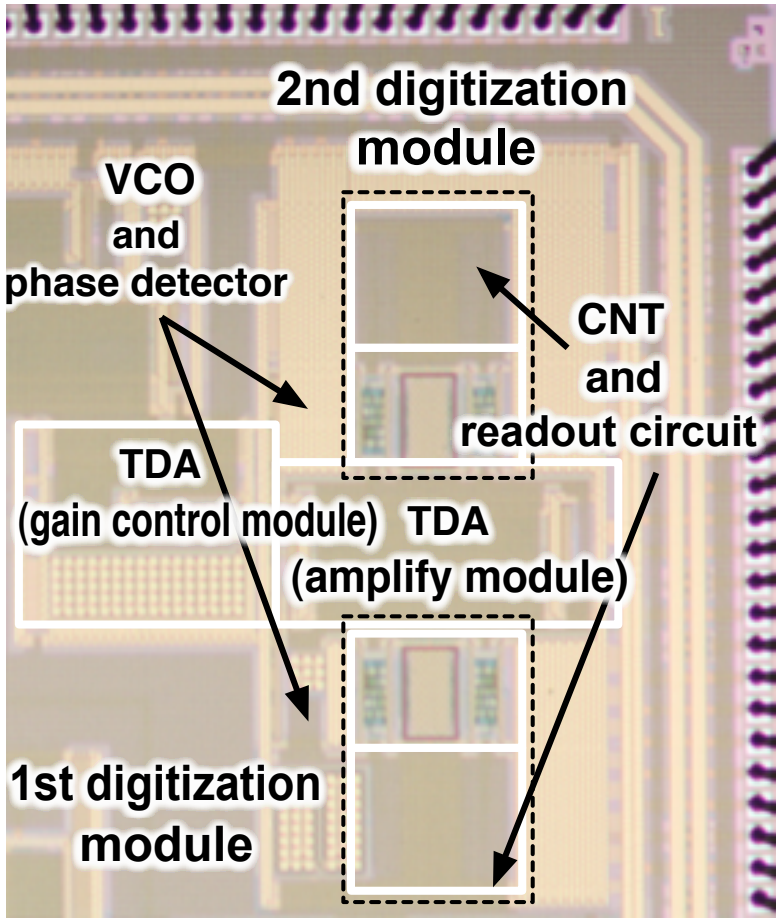
$$LSB = T_{gate} / Gain$$



TDC structure



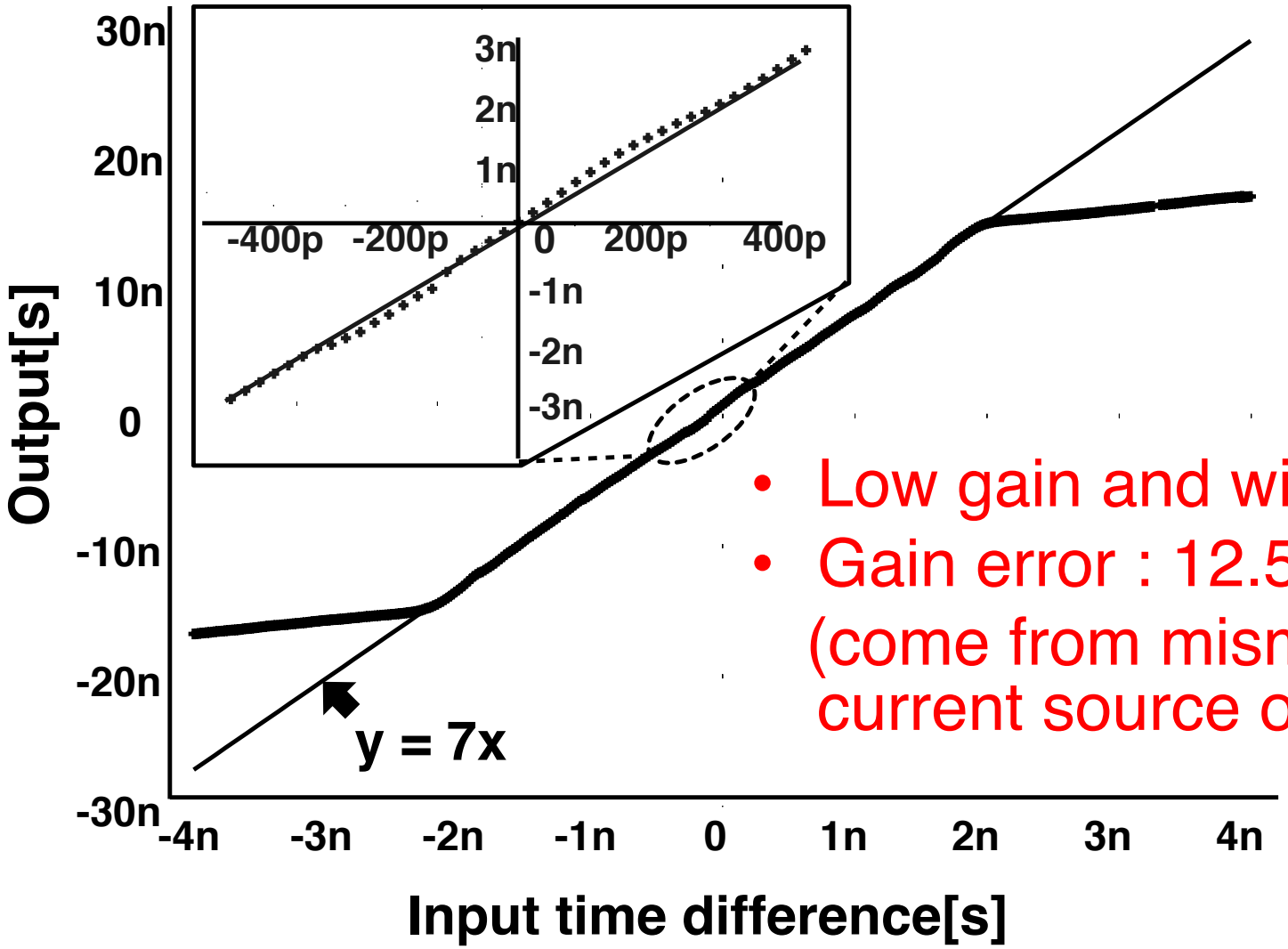
Chip implementation



Tech.	0.18um CMOS
Area	0.52mm^2
-TDA	0.343mm^2
-TDC	0.09mm^2 x2
Vdd	1.8V
Ref.	10MHz

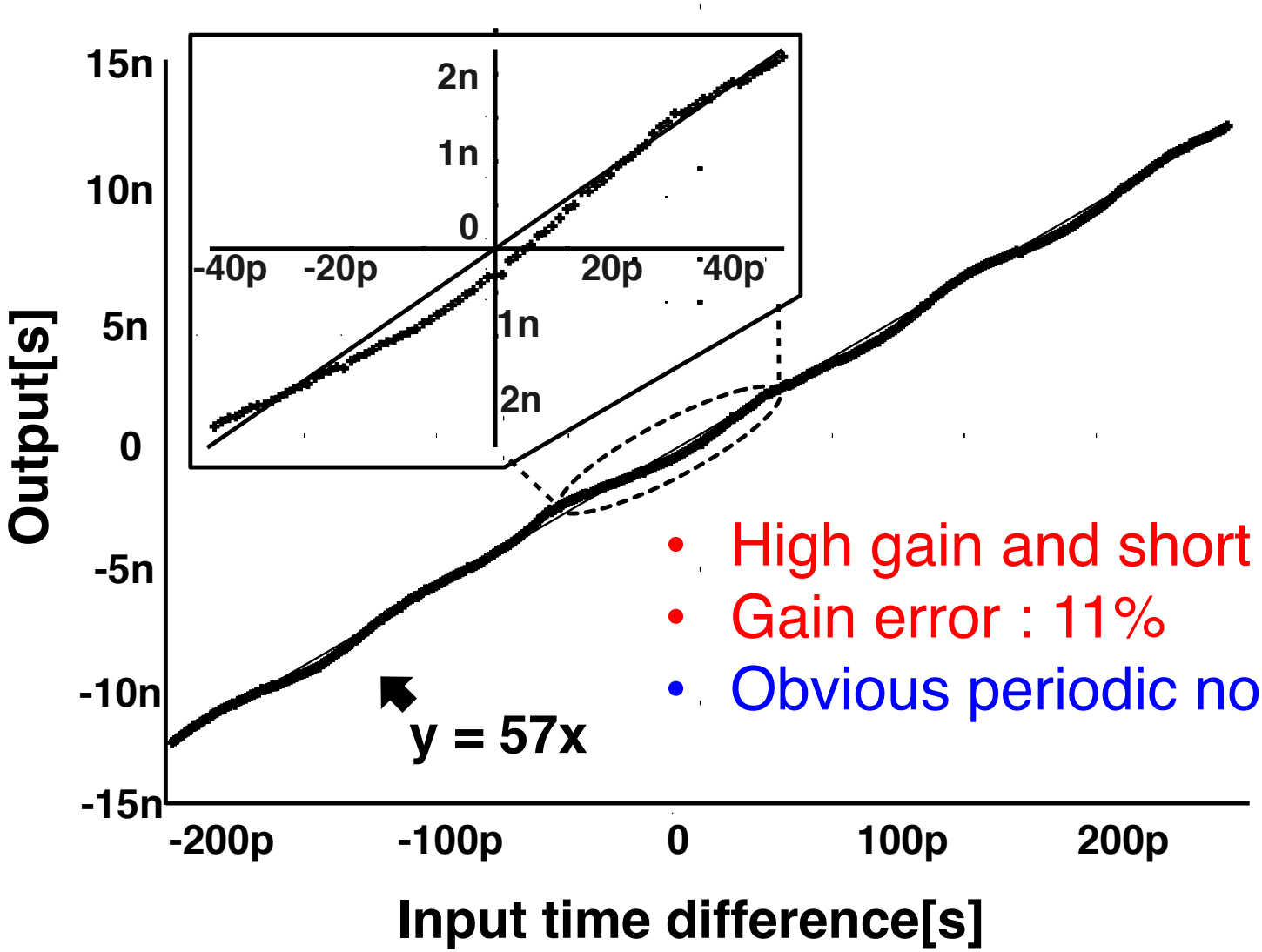
S. Mandai et al, ESSCIRC 2010

8X TDA measurement results



- Low gain and wide range
- Gain error : 12.5%
  (come from mismatch of current source of CP)

64X TDA measurement results

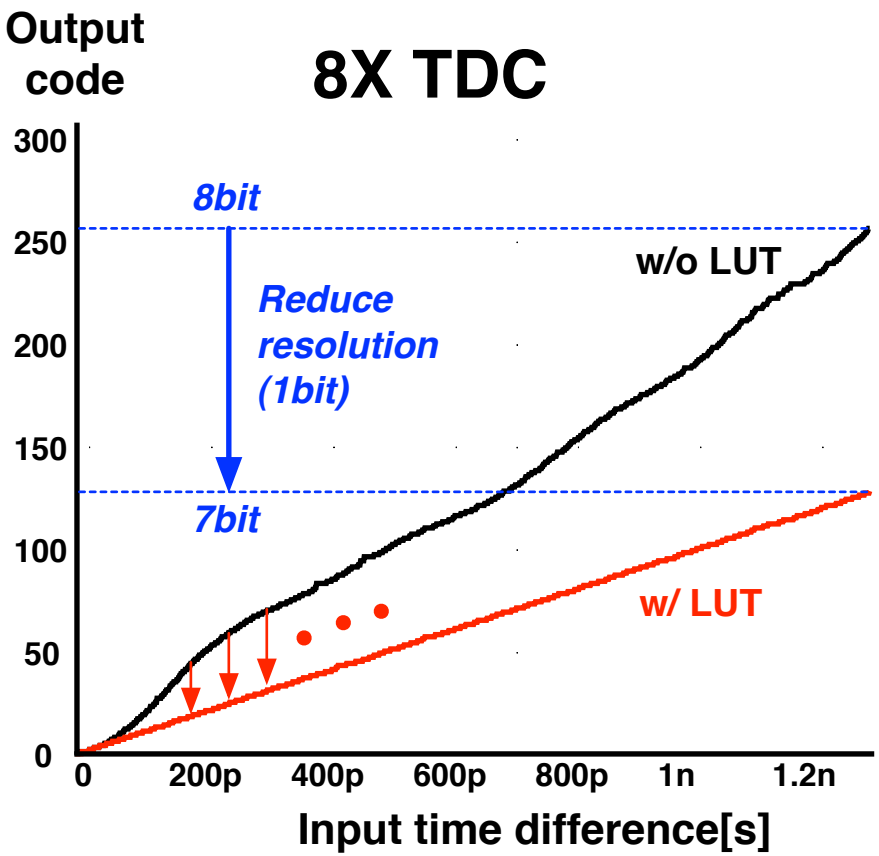


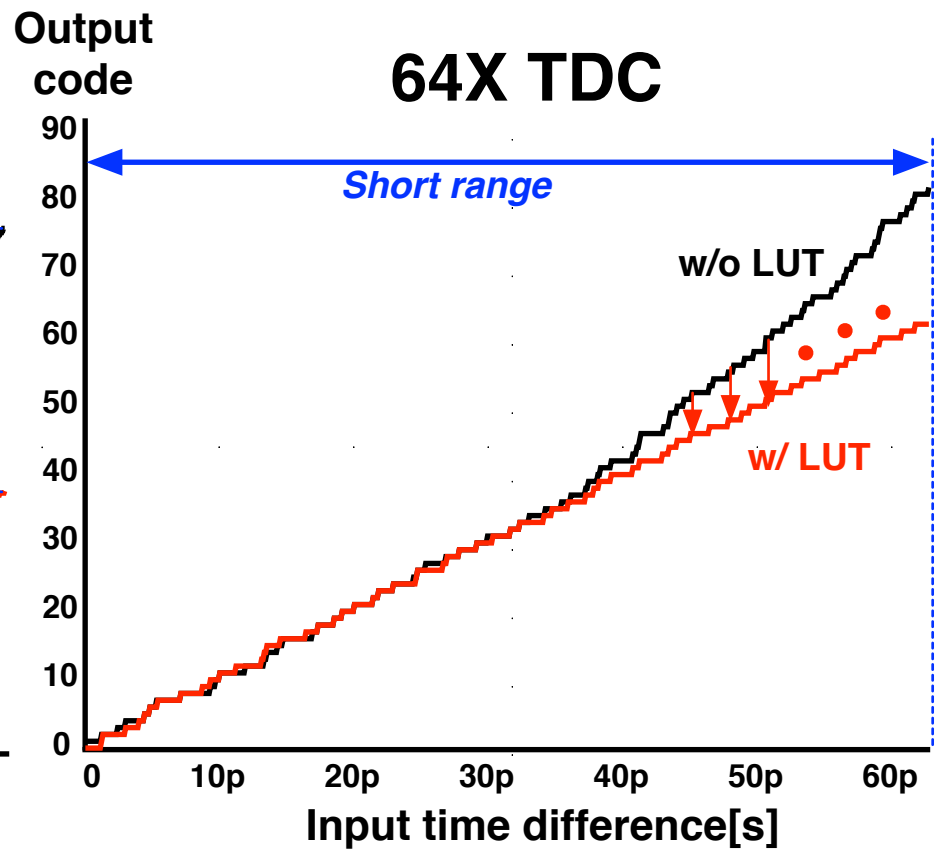
- High gain and short range
- Gain error : 11%
- Obvious periodic noise

TDA error effects the TDC

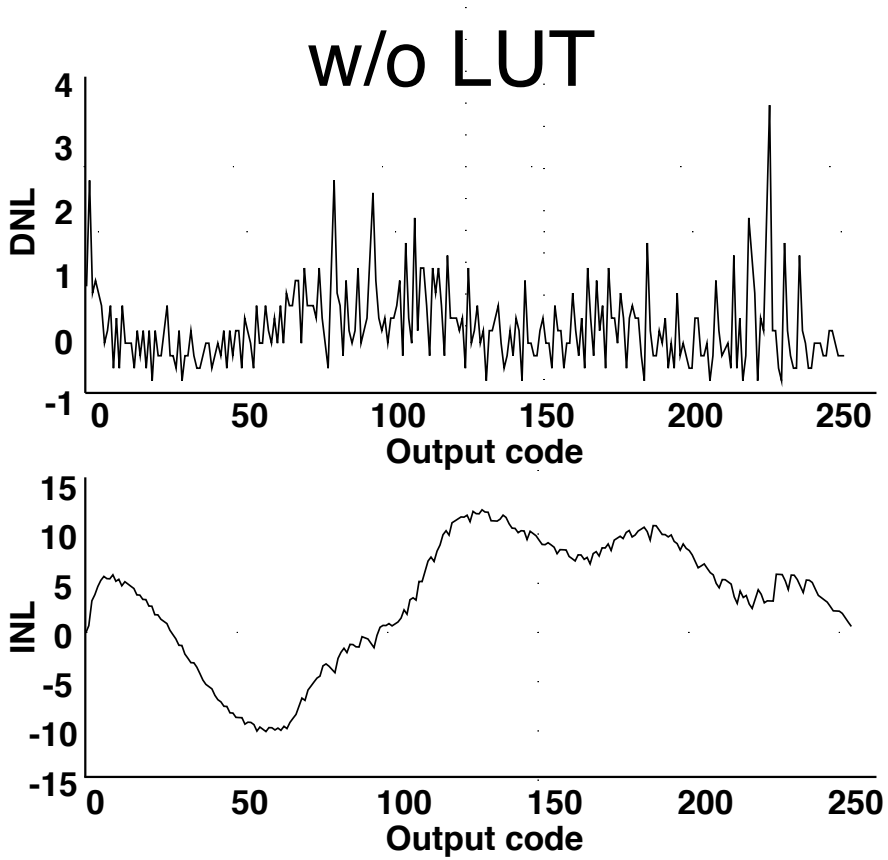
The periodic noise of TDAs can be observed in the measurement results of both TDCs

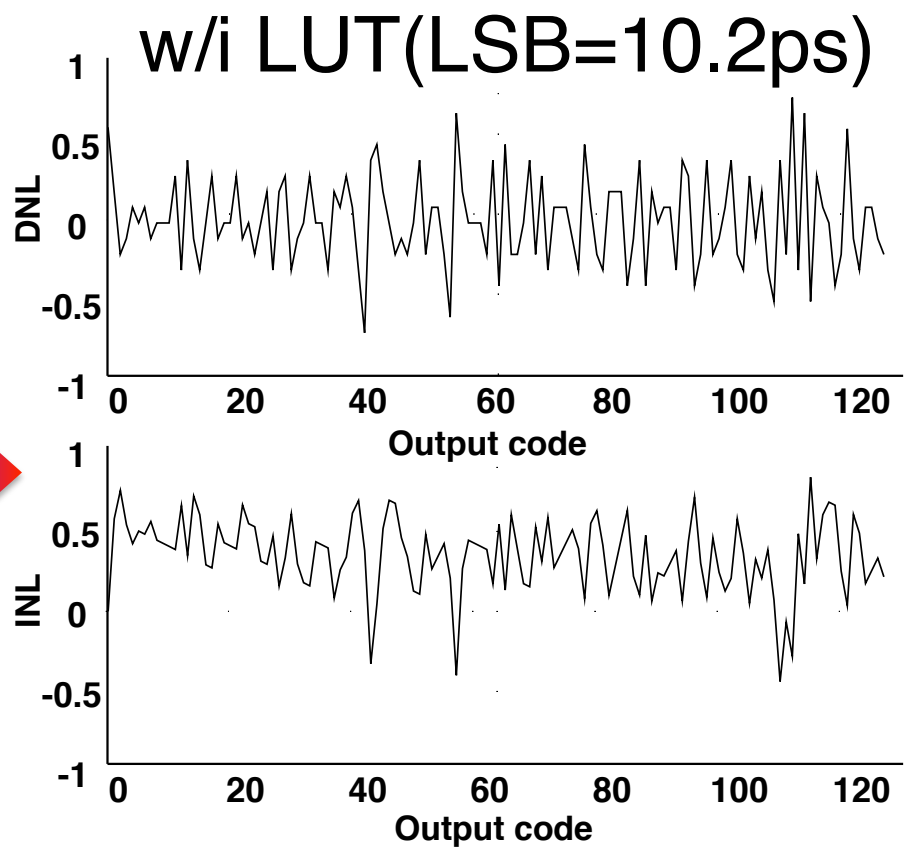
Compensate the non-linearity of the TDC by Look-up table (TDC)





DNL and INL(8X TDC)



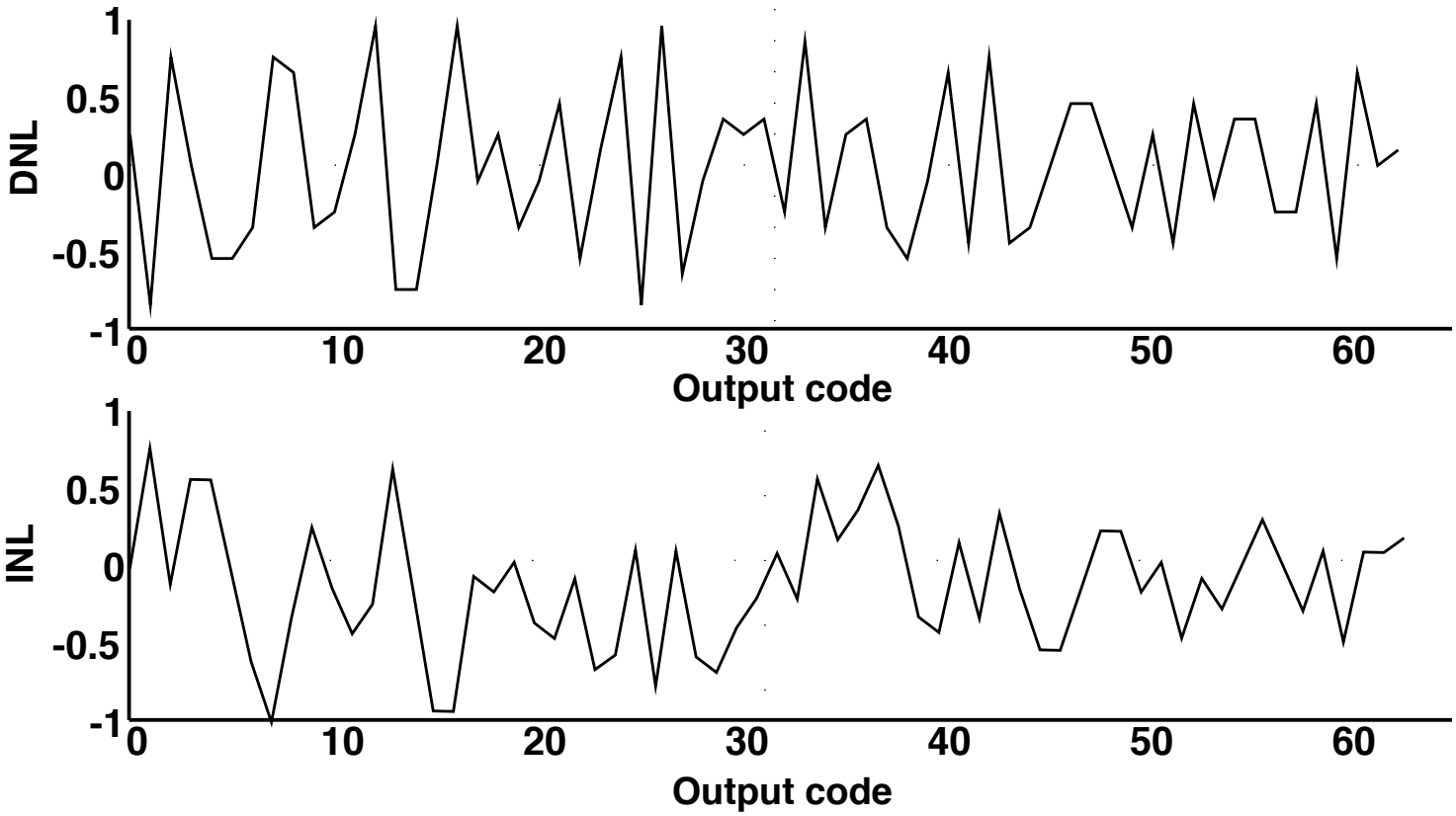


- DNL : +3.5/-0.8
- INL : +11.6/-9.3

- DNL : +0.8/-0.7
- INL : +0.8/-0.4

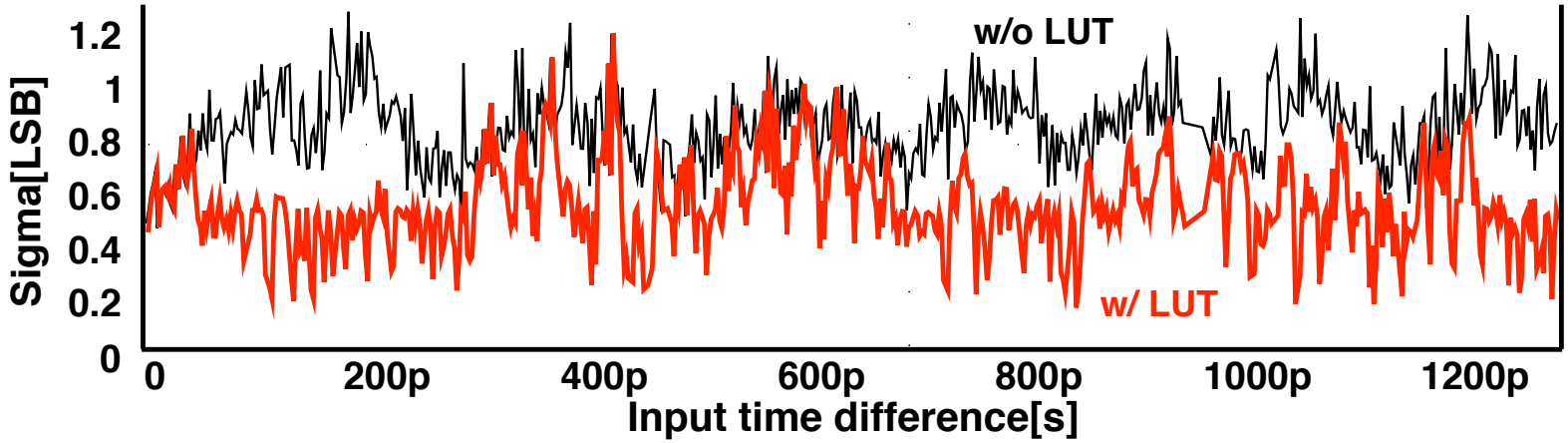
DNL and INL(64X TDC)

w/i LUT(LSB=1.0ps)

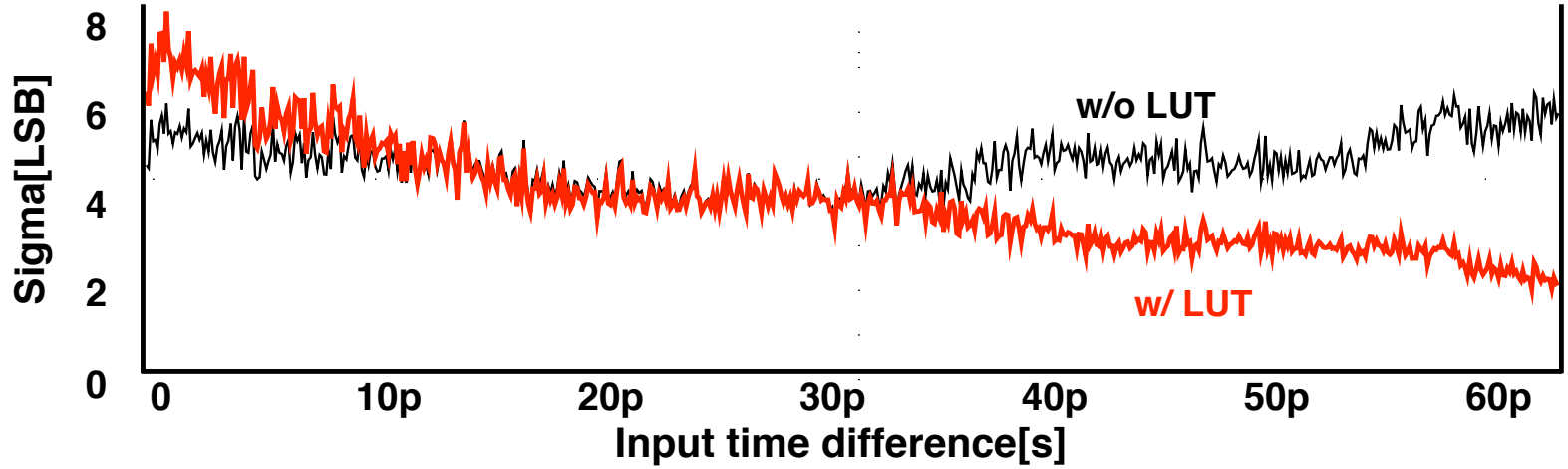


- DNL : +0.9/-0.9
- INL : +0.8/-1.0

Single shot precision



8X TDC



64X TDC

Comparison

Ref.	Method	Tech. (nm)	LSB (ps)	DNL	INL	bits	Area (mm^2)	Power*
[3]	Delayline	90	20.0	0.6	0.7	-	0.01	-
[4]	vernier	700	30.0	-	1.3	-	10	-
[5]	Pulse shrinking	350	68.0	-	-	-	0.03	-
[6]	Interpol.	350	1.22	-	-	28	-	606
[7]	Passiv interpol.	90	4.7	0.6	1.2	7	0.02	14
[8]	Amp.	90	1.25	0.8	3.0	9	0.6	300
this	**Single amp**	**180**	**10.2**	**+0.8/-0.7**	**+0.8/-0.4**	**7**	**0.52**	**3181**
	Cascade ampl.		**1.0**	**+0.9/-0.9**	**+0.8/-1.0**	**6**		

* Power is defined by P[mW]/(Vdd[V]^2 x f[GHz])

Reference

[3] R.B.Staszewski, S.Vemulapalli, P.Vallur et al.,”1.3 V 20 ps time-to-digital converter for Frequency Synthesis in 90-nm CMOS” IEEE Trans. on Circuits and Systems II, vol. 53, no. 3, pp.220-224, Mar. 2006.

[4] P.Dudek, S.Szczepanski, and J.V.Hatfield, ”A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line”, IEEE Trans. on Solid-State Circuits, Vol.35, No.2, Feb. 2000, pp.240-247.

[5] P.Chen, S.I.Liu, and J.Wu, ”A CMOS Pulse-Shrinking Delay Element For Time Interval Measurement”, IEEE Trans. on Circuits and Systems-I I, Vol. 47, No.9, Sep 2000, pp.954-958.

[6] A. Mantyniemi and T. Rhkone, and J. Kistamovaara, ”A CMOS Time-to-Digital Converter Based On a Cyclic Time Domain Successive Approximation Interpolation Method” IEEE JSSC, Vol.44, No.11,Nov. 2009.

[7] S.Henzler, S.Koeppe, W.Kamp et al., ”90nm 4.7ps-Resolution 0.7-LSB Single-Shot precision and 19pJ-per-Shot Local Passive Interpolation Time-to-Digital Converter with On-Chip Characterization”, IEEE ISSCC, 2008, pp. 548-635.

[8]M. Lee and Asad A. Abidi, ”A9b,1.25ps Resolution Coarse-Fine Time-to-Digital Converter in 90nm CMOS that Amplifies a Time Residue” IEEE JSSC, Vol.43, No.4,Apr. 2008.

Short summary

- We have designed the TDC based on the TDA with non-linearity calibration using a 0.18um CMOS process
- Two operation modes,
  - 8X TDC, 10.2ps LSB, 1.3ns input range
  - 64X TDC, 1.0ps LSB, 60ps input range
- The TDC can be applied to various applications such as PLL or jitter measurement.

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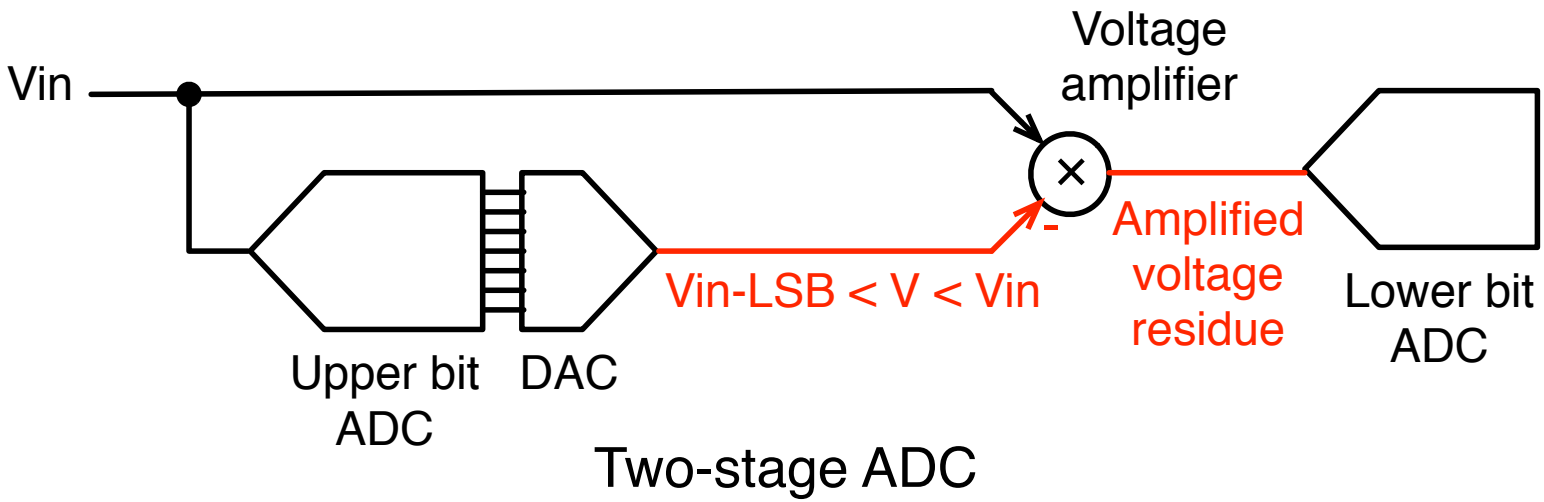
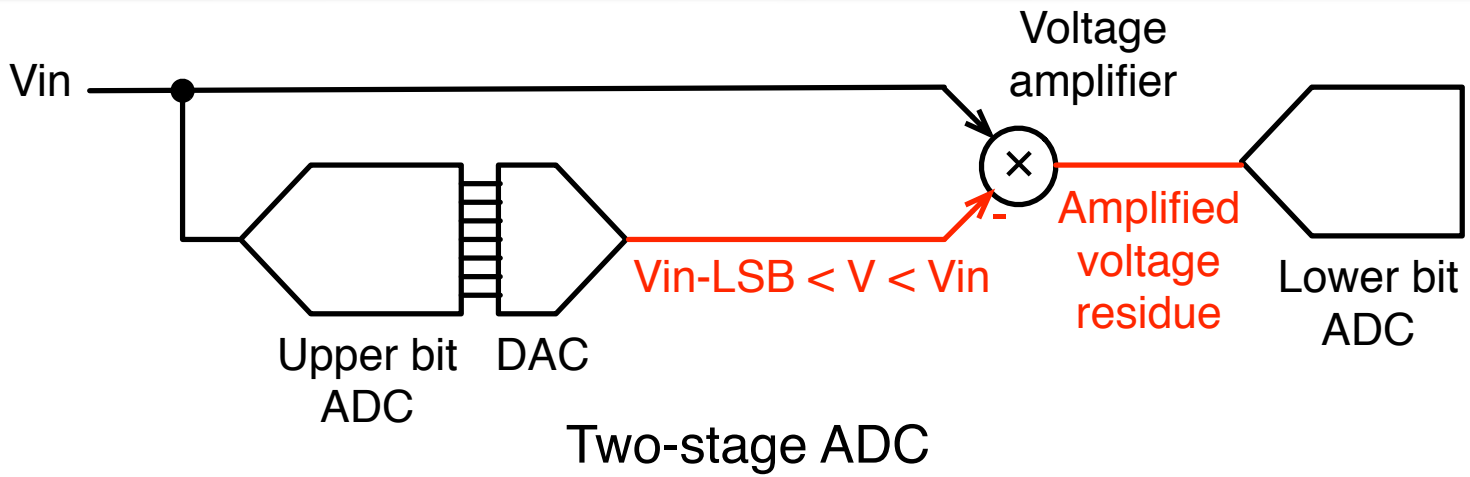
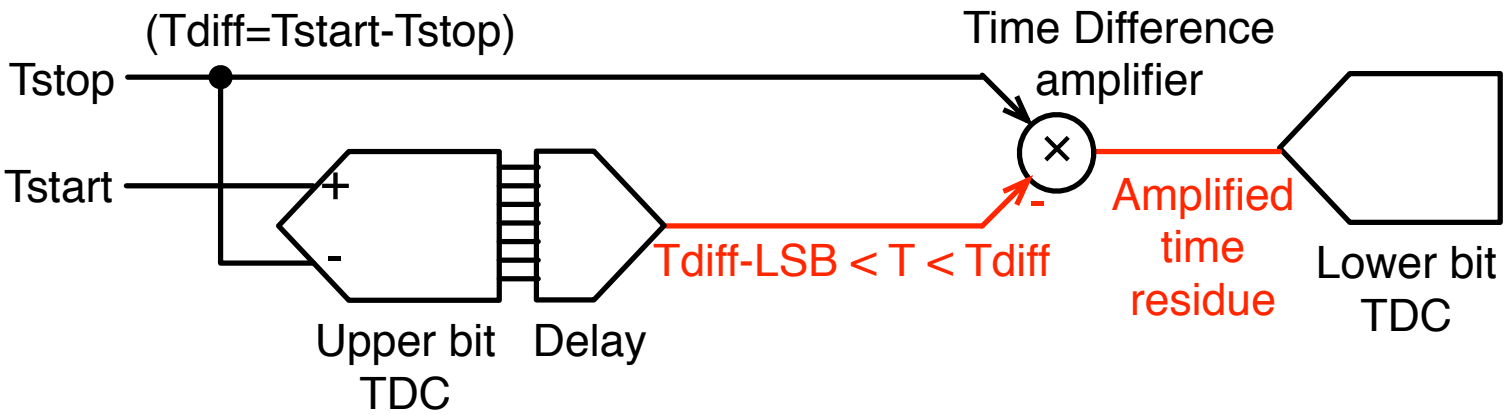
Concept of the proposed TDC



Concept of the proposed TDC



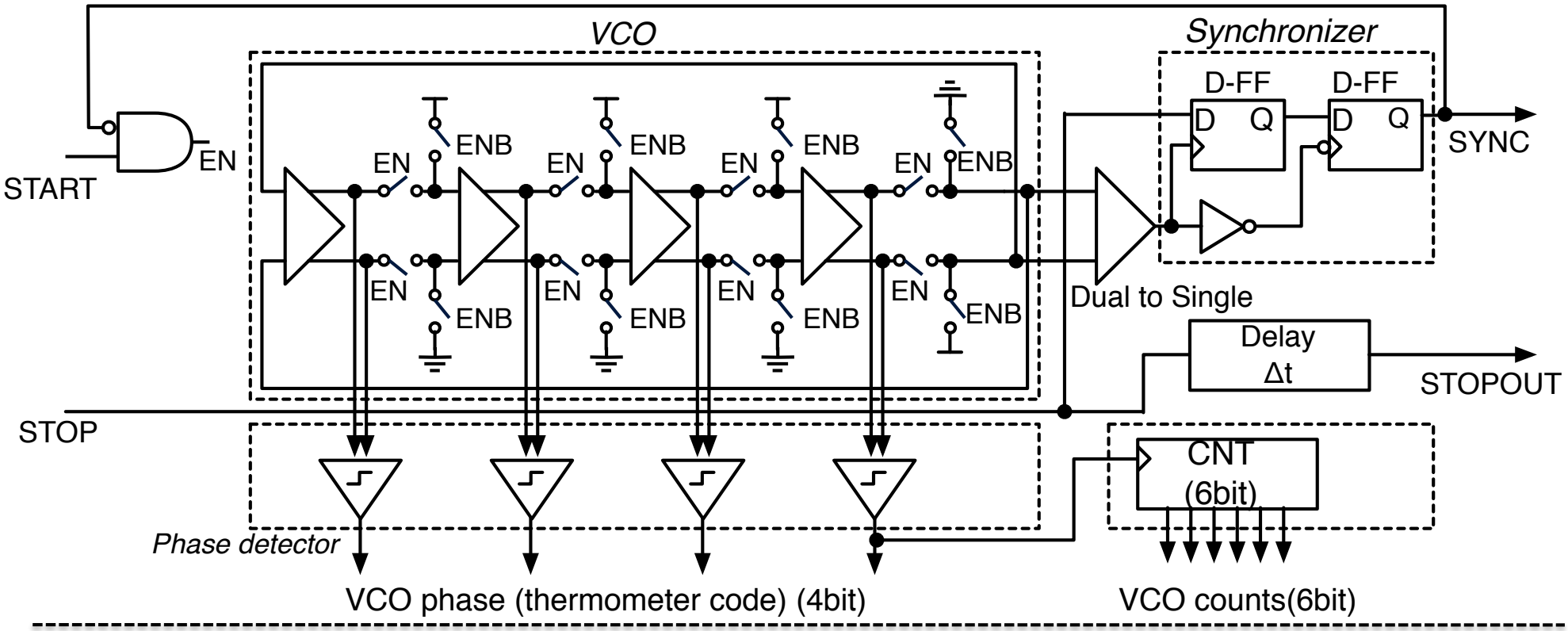
Two-stage ADC

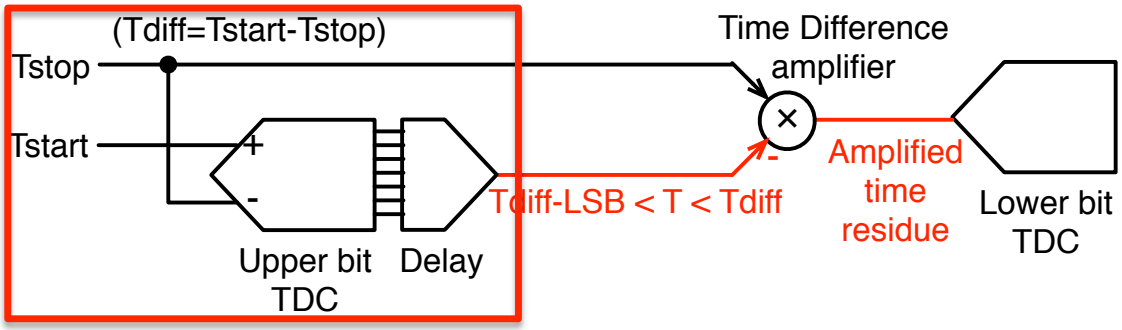


Two-stage TDC

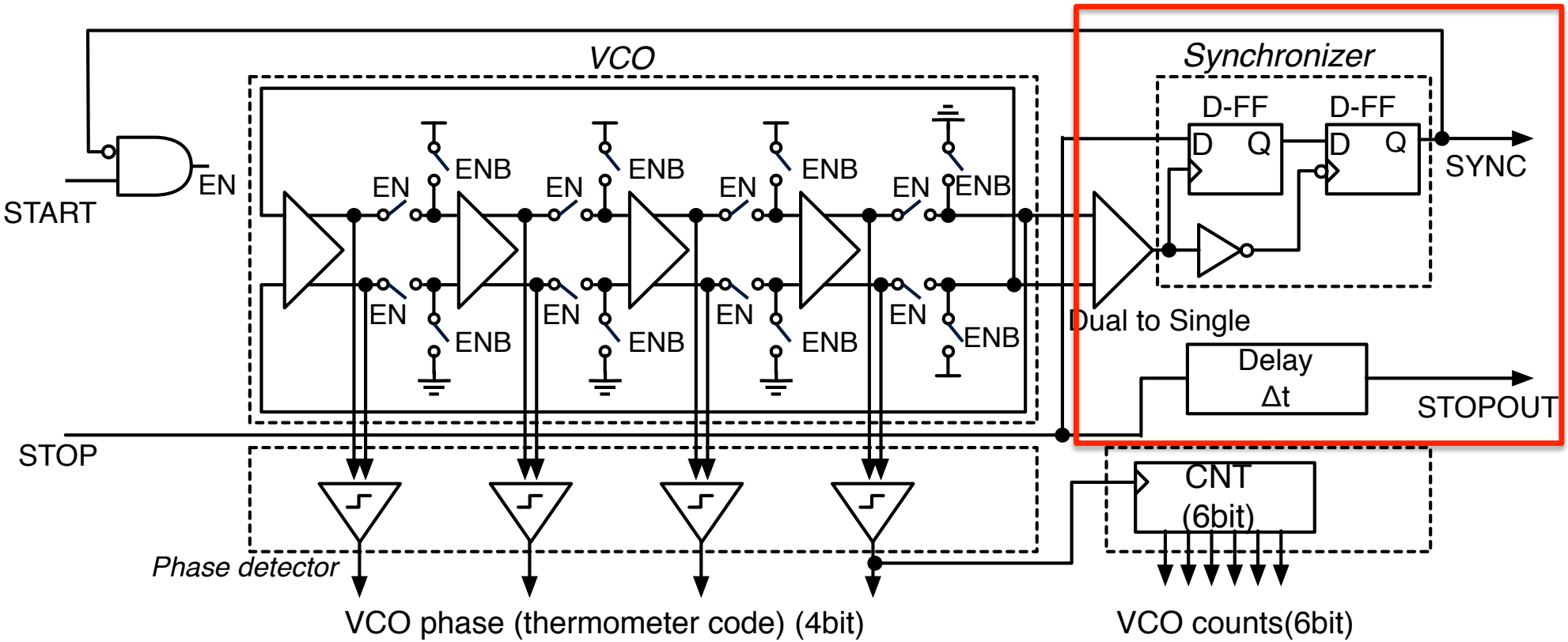
LSB will be improved by a factor equal to the gain of the TDA

Schematic of upper TDC and lower TDC



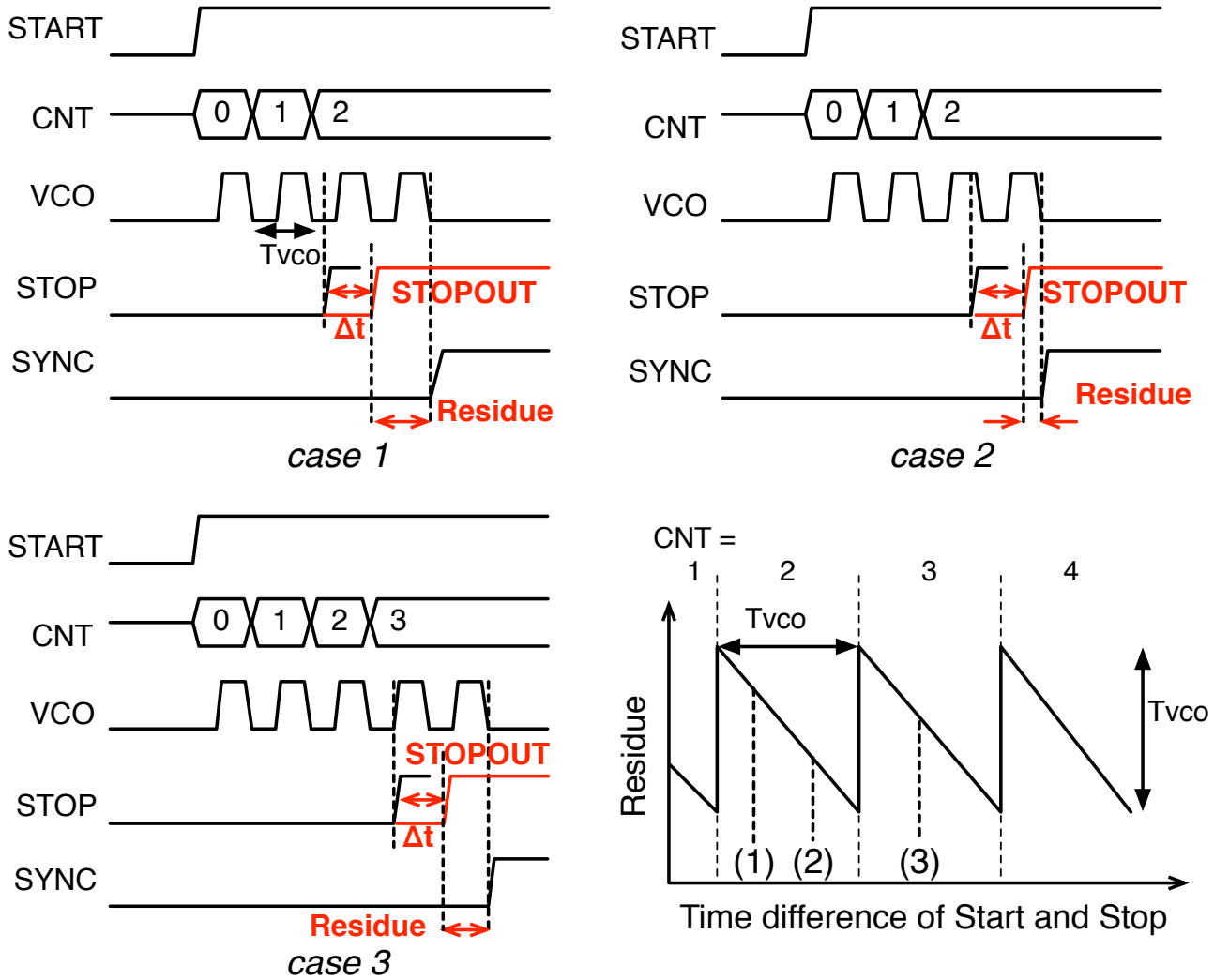


Schematic of upper TDC and lower TDC



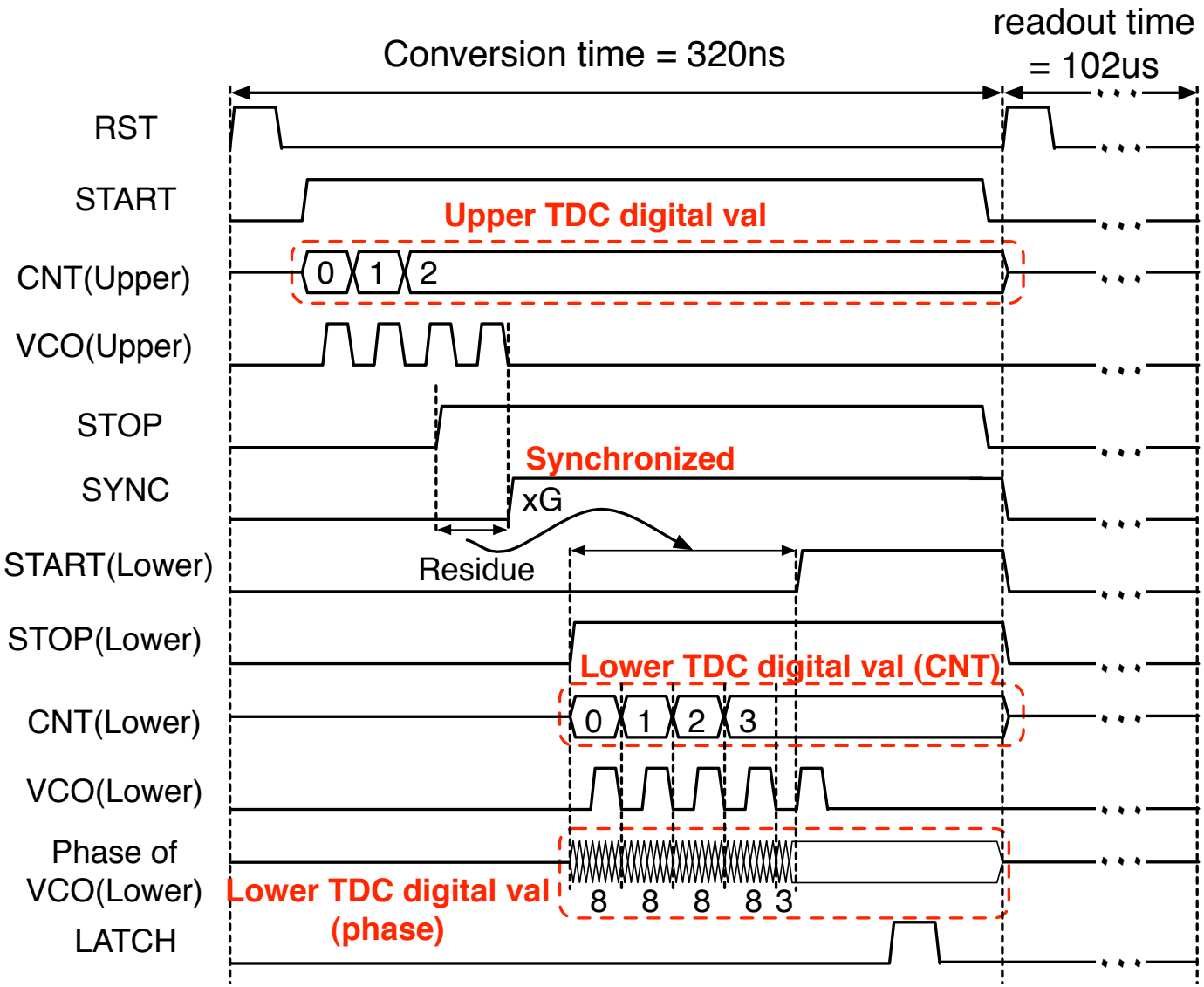
The lower TDC is identical except for Synchronizer and 5-bit counter instead of 6-bit counter

Residue calculation of upper TDC

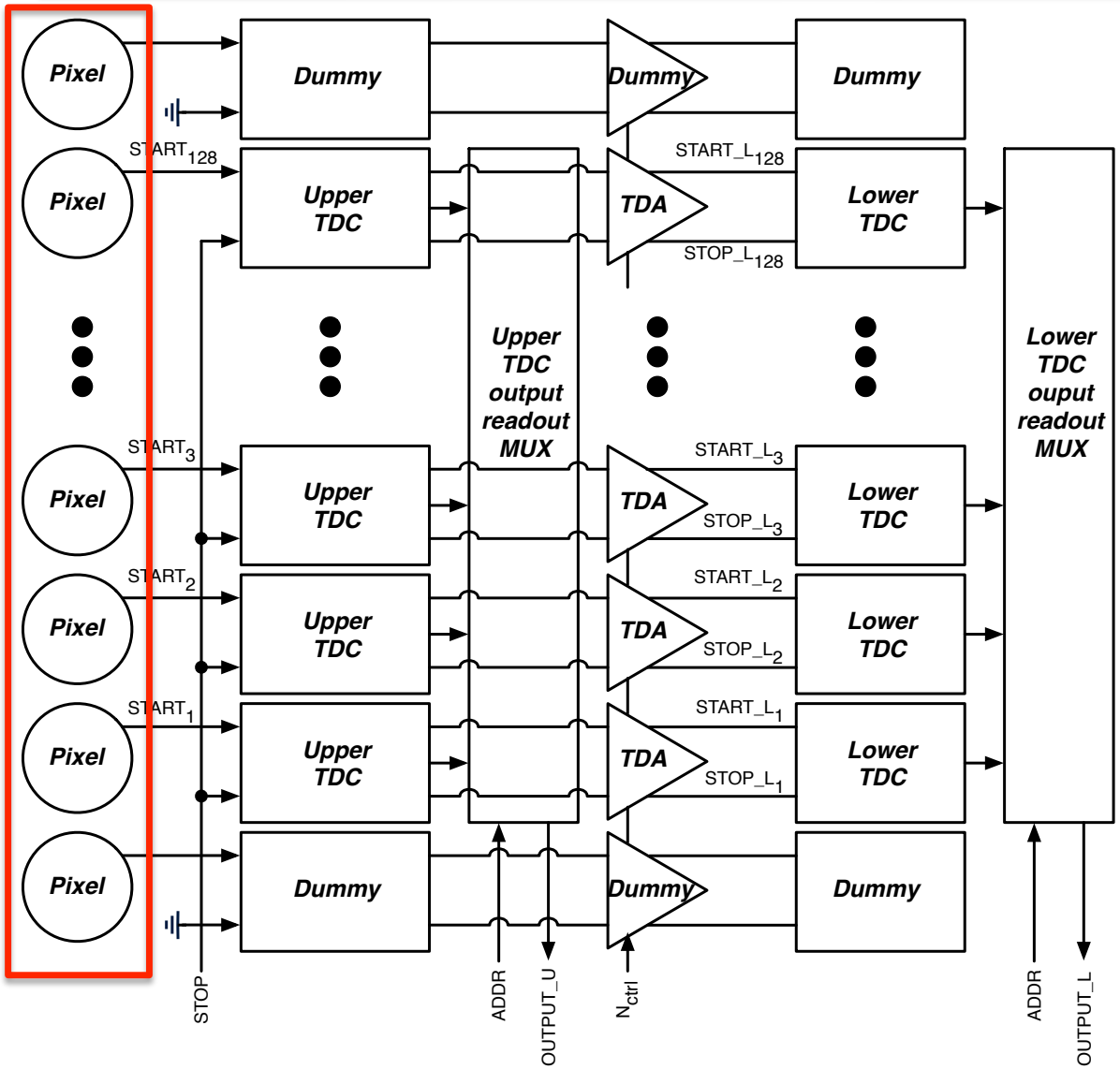


Δt is inserted to reduce the maximum value of the residue

Timing diagram

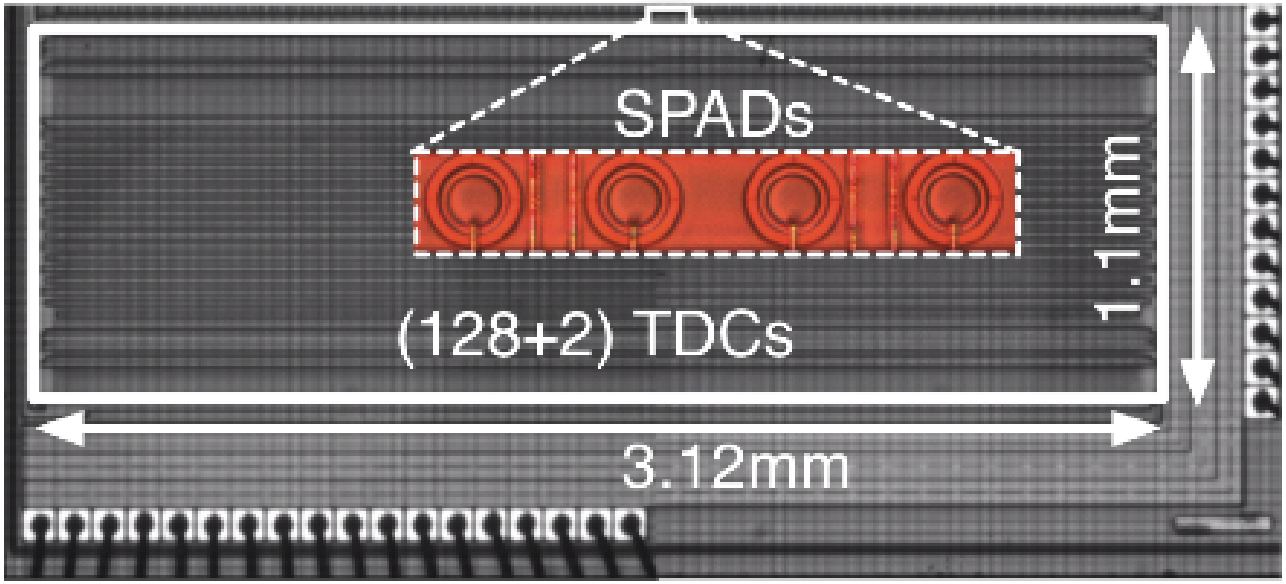


TDC array block diagram



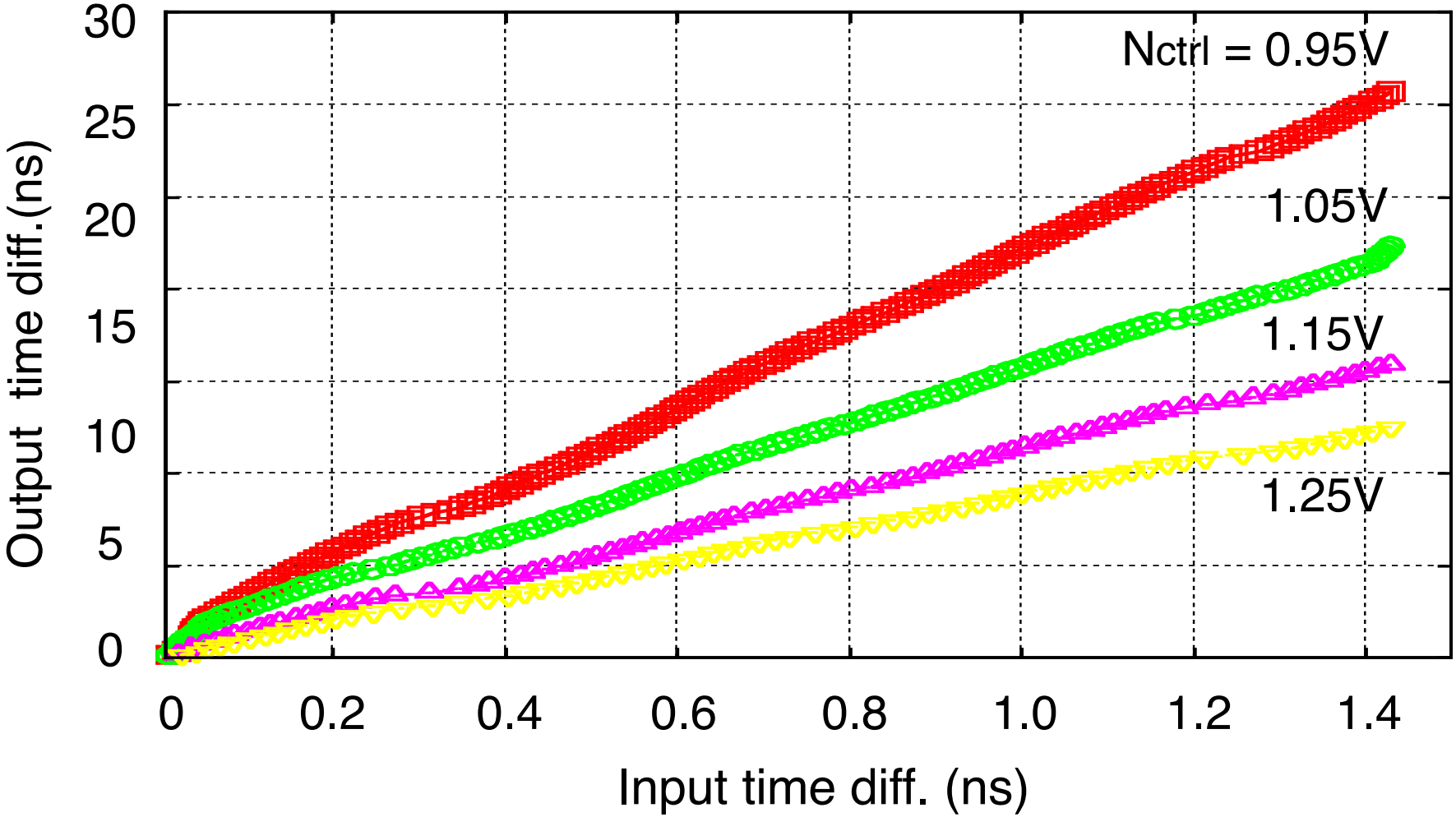
- 128+2 TDCs
- Each TDC has pixel circuit with single-photon avalanche diode (SPAD)
- Two kinds of inputs, SPAD and electrical test inputs
- SPAD generate a sharp pulse when a photon comes

Chip implementation



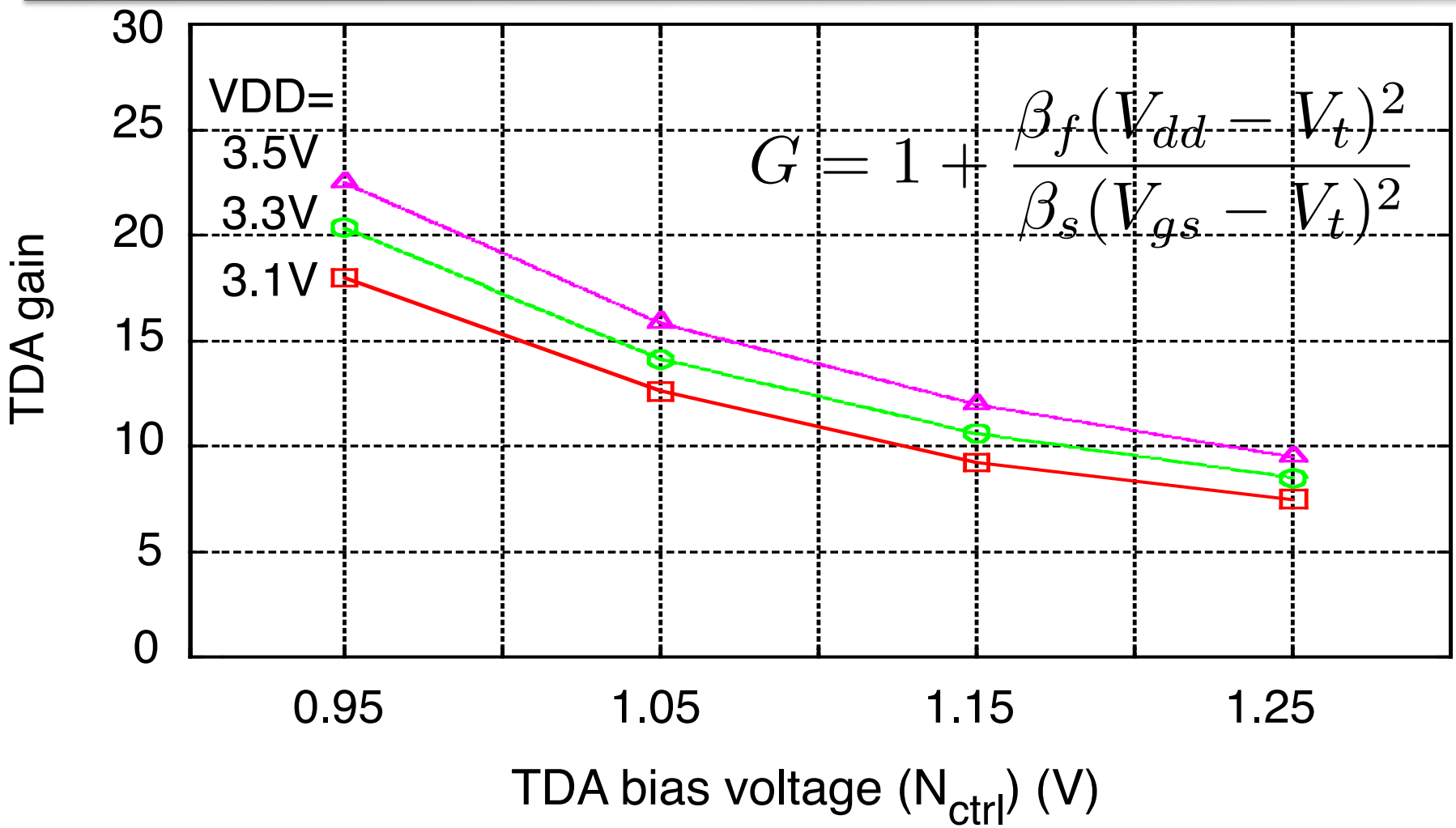
Tech.	0.35um HV CMOS	**Vdd**	3.3V
Area	3.12mm x 1.1mm	**SPAD**	C.Niclass, JSSC. 2008
-Upper & lower TDC	0.024 x 0.13mm	-Diameter	6um
-TDA	0.024mm x 0.55mm	**Pitch**	24um
-one TDC	0.01632mm^2	**# of TDC**	128+2(dummy)

TDA measurement results (by density test)



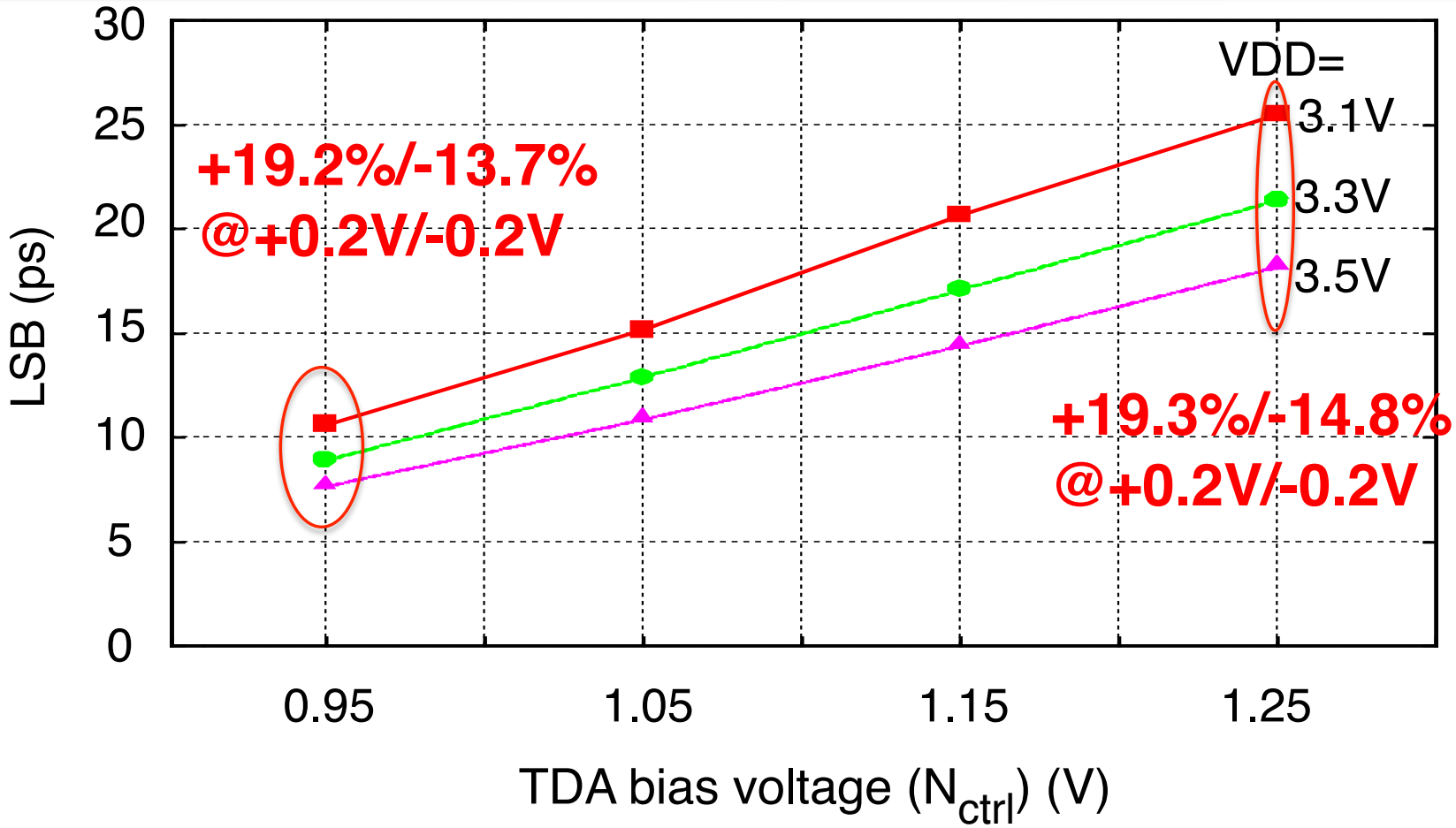
Gain is controller by Nctrl

TDA gain variation by power supply fluctuation



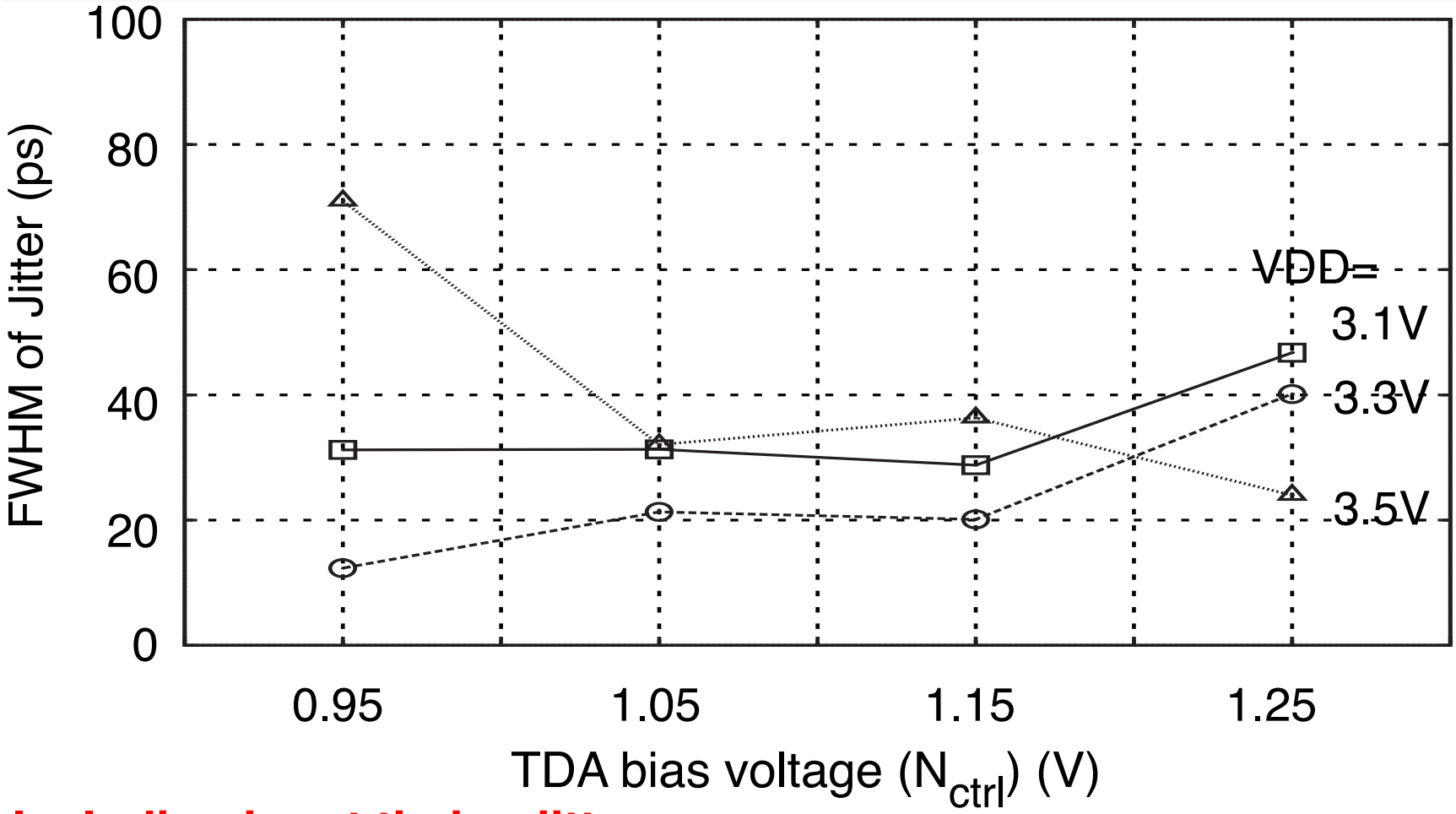
Power supply fluctuation cause TDA gain fluctuation but this effects is removed by using CML logic delay cell structure

LSB change by power fluctuation



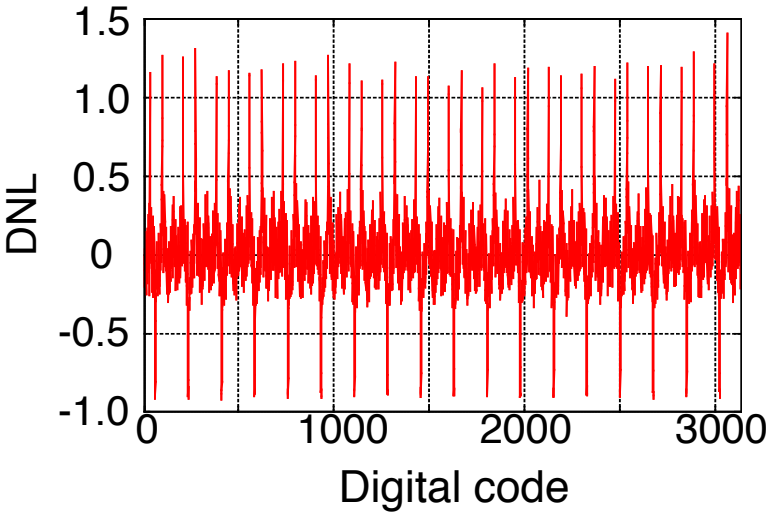
TDA gain and VCO frequency will be lower as the power supply decrease => LSB degrades

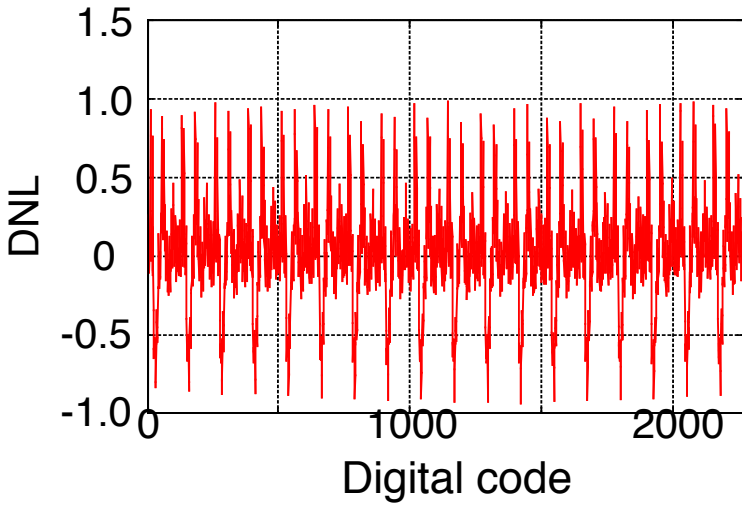
TDC Timing jitter change by power supply fluctuation

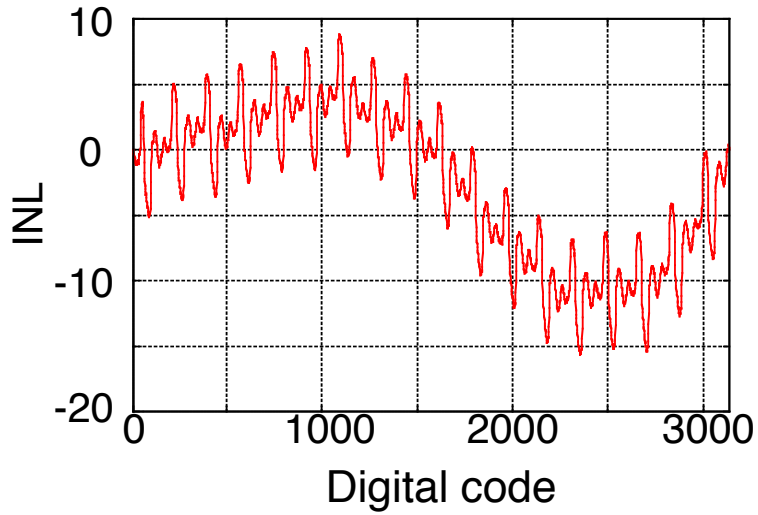


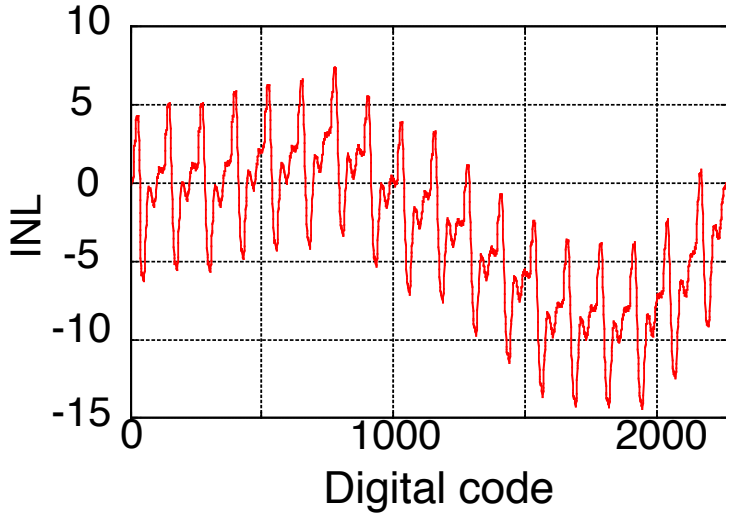
- **Including input timing jitter**
- **difficult to maintain same input jitter => ~30ps**
- **This is equivalent to a single shot accuracy of TDC**

DNL and INL





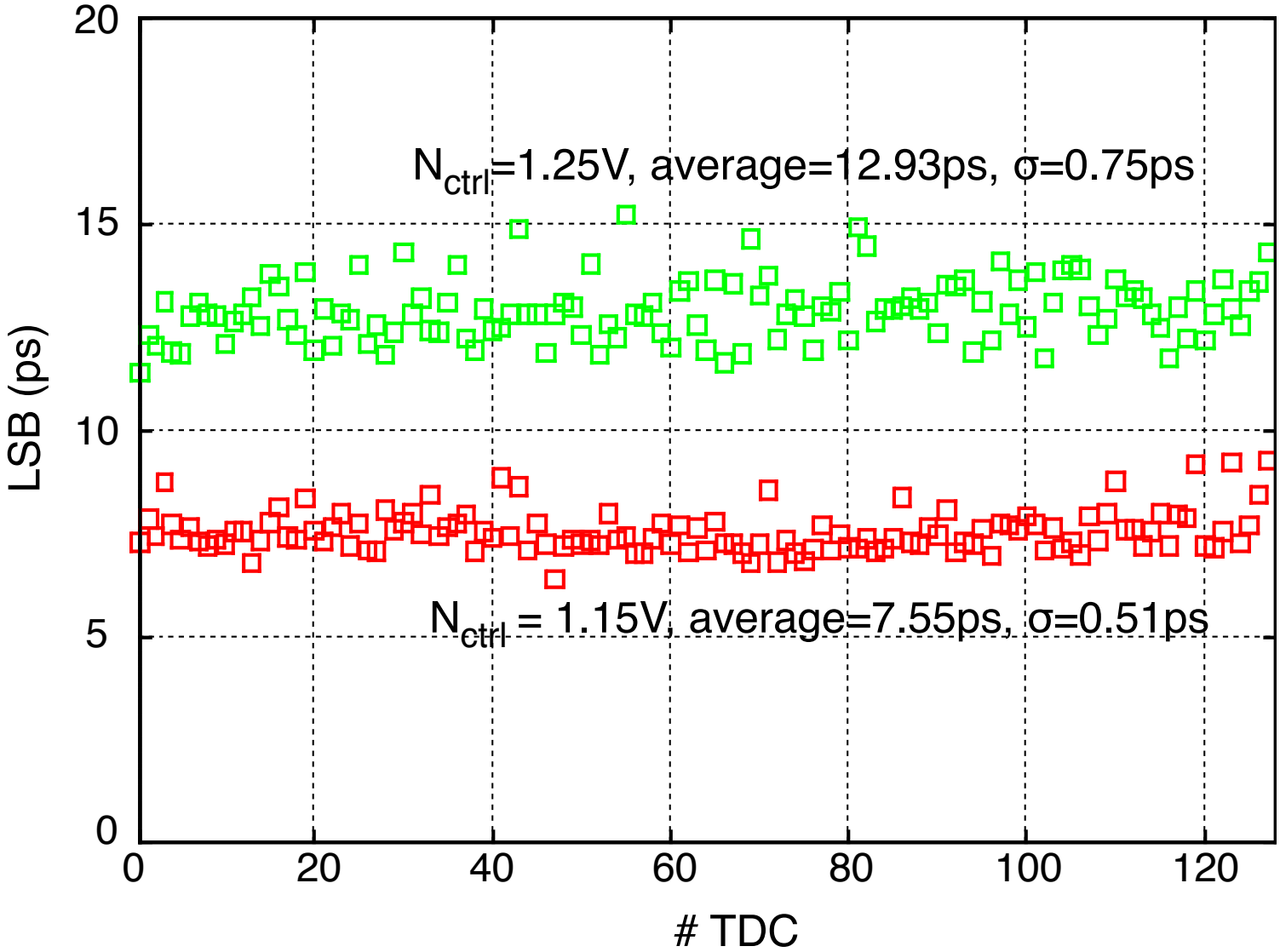




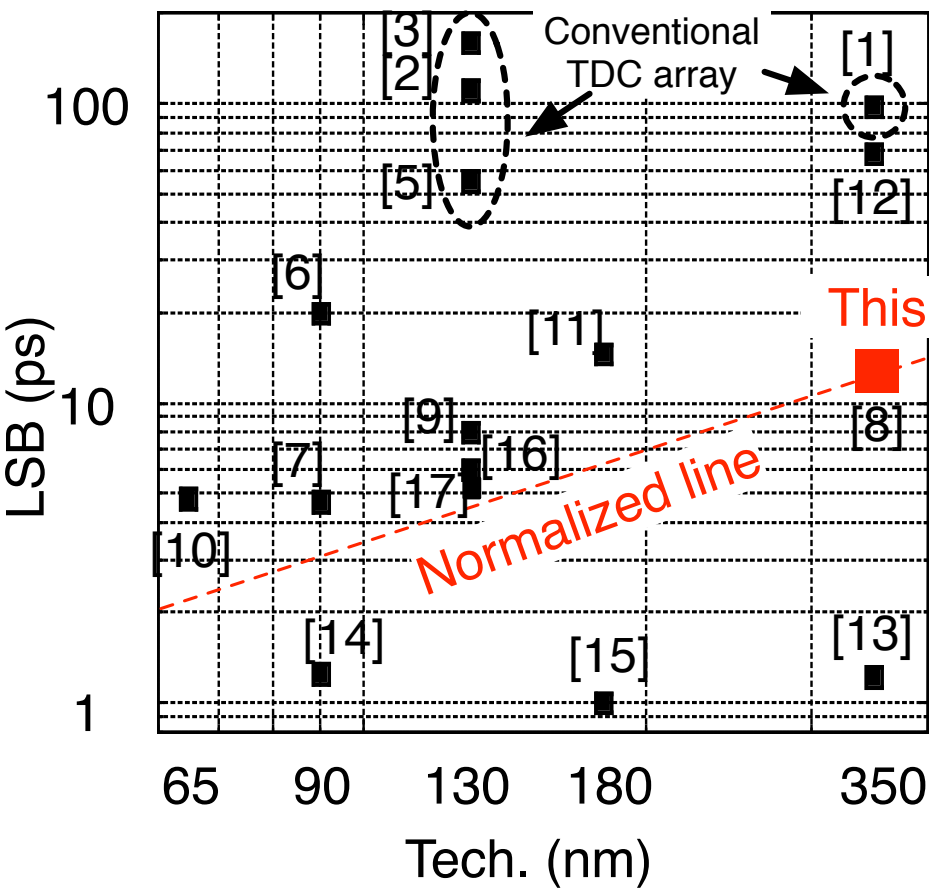
N_{ctrl}=0.95V, LSB=8.9ps

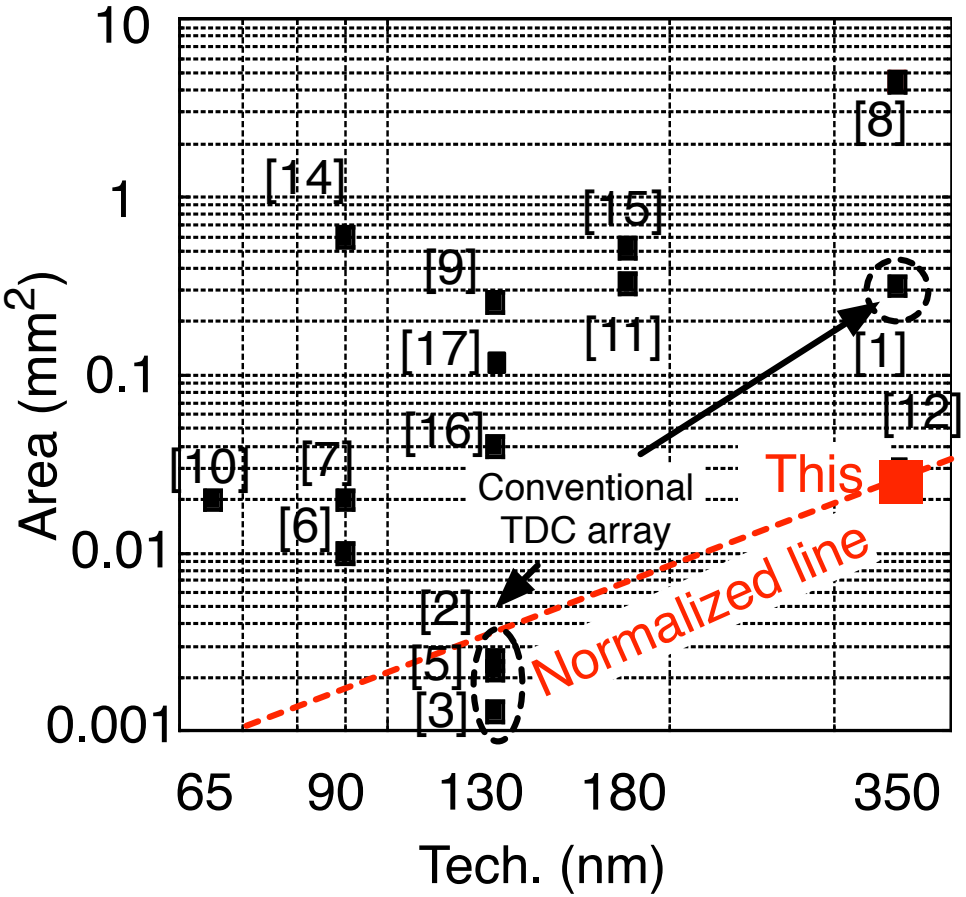
N_{ctrl}=1.05V, LSB=12.9ps

LSB variation in 128 TDC array



Comparison





Power : 2.37mW / TDC

Sampling rate : 3.125 MHz (without readout)

Dynamic range : 11.6bit@8.9ps LSB, 11.1bit@12.9ps LSB

Reference

[1] C. Niclass et al., “A 128x128 Single-Photon Image Sensor with Column- level 10-bit Time-to-Digital Converter Array,” IEEE JSSC Vol. 43, no 12, pp. 2977-2989, Dec. 2008.

[2] M. Gersbach et al., “A Parallel 32x32 Time-to-Digital Converter Array Fabricated in a 130nm Imaging CMOS Technology,” IEEE ESSCIRC, pp. 196-199, Sep. 2009.

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[4] J. Richardson et al., “A 32x32 50ps Resolution 10 bit Time to Digital Converter Array in 130nm CMOS for Time Correlated Imaging,” IEEE CICC, pp. 77-80, Sep. 2009.

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[14] M. Lee and Asad A. Abidi, “A9b, 1.25ps Resolution Coarse-Fine Time- to-Digital Converter in 90nm CMOS that Amplifies a Time Residue” IEEE JSSC, Vol.43, No.4, Apr. 2008.

[15] S. Mandai et al., “Time-to-Digital Converter Based on Time Difference Amplifier with Non-Linearity Calibration,” IEEE ESSCIRC, pp. 266- 269,Sep. 2010,

[16] M.Z. Straayer et al., “A Multi-Path Gated Ring Oscillator TDC With First-Order Noise Shaping, ”IEEE JSSC, vol. 44, no. 4, pp. 1089-1098, Apr. 2009.

[17] Y. Cao, et al., “A 1.7mW 11b 1-1-1 MASH ΔΣ Time-to-Digital Converter,” IEEE ISSCC, 2011, pp.480-482.

Summary

Parameter	Value
Tech.	0.35um HV CMOS
Area	3.12mm x 1.1mm
-Upper & lower TDC	0.024 x 0.13mm
-TDA	0.024mm x 0.55mm
-one TDC	0.01632mm^2
Pitch	24um
Gain of TDA	21.625 @ 0.95V TDA bias voltage
LSB	8.9ps @ 0.95V TDA bias voltage
Input range	28ns (until 88ns is possible)
Sampling rate	3.125MHz (without readout)
Power	2.37W/TDC

Short summary

- 128 Column-parallel TDC based on time difference amplification is proposed
- Time difference amplifier and TDC characterization is shown
- Small area and accurate time resolution are realized
  - Future Digital Silicon Photo Multiplier (D-SiPM)
- Application using the TDC array will be constructed in the near future

Conclusions

- Closed-loop structure time-difference-amplifier (TDA) is demonstrated
- High gain is realized by cascading TDAs
- High gain TDA is utilized for the fine resolution TDC
- 128 column-parallel TDC based on TDA is proposed

Acknowledgement

- These works are researched in Univ. of Tokyo and TU Delft
- This study partially has been carried out through the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.
  - Prof. Ikeda Makoto
  - Prof. Toru Nakura
  - Prof. Kunihiro Asada
- The research leading to these results has received funding from the European Union Seventh Framework Programme under Grant Agreement n◦256984 (EndoTOFPET-US).
- I also would like to thank
  - Prof. Edoardo Charbon
  - Dr. Yuki Maruyama,
  - Dr. Hyung-June Yoon,
  - Dr. Matthew Fishburn,
  - Chockalingam Veerappans
- The authors are also grateful to Xilinx, Inc. for FPGA donations.

Appendix

TDA characterization

Gain

$$G = \frac{T_s}{T_f} = \frac{I_s + I_f}{I_s}$$

T_f and T_s are delay of fast delay cell and slow delay cell
I_f and I_s are sat. current of fast delay cell and slow delay cell

$$I_f = \frac{\beta_f}{2}(V_{dd} - V_t)^2$$

$$I_s = \frac{\beta_s}{2}(V_{gs} - V_t)^2$$

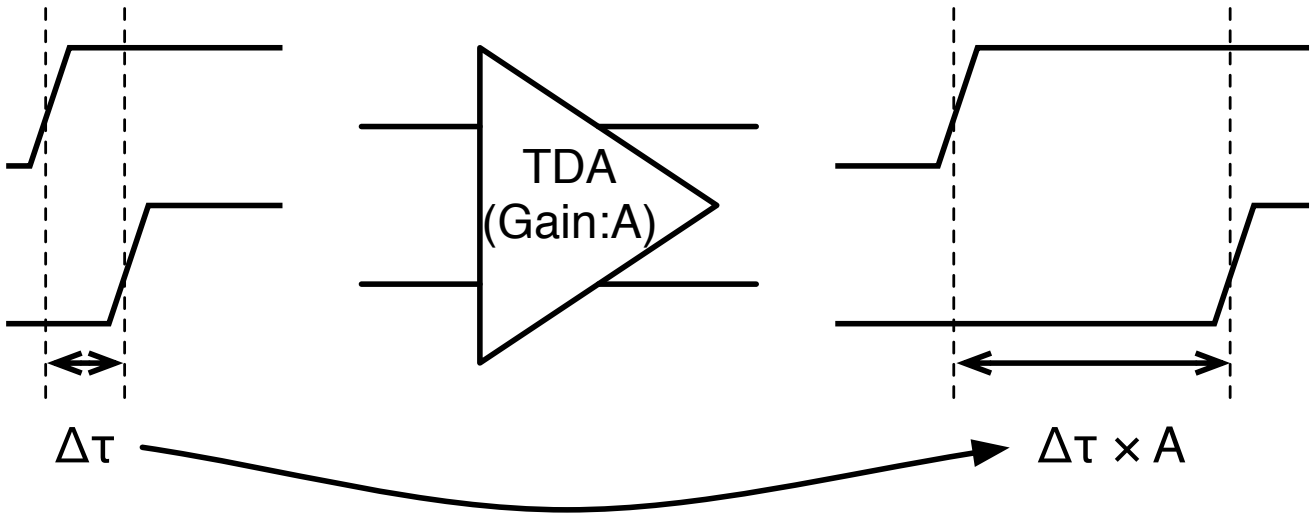
$$\Rightarrow \quad G = 1 + \frac{\beta_f (V_{dd} - V_t)^2}{\beta_s (V_{gs} - V_t)^2}$$

Input range

$$T_{range} = T_f * N$$

N is the number of delay cells in a chain

Time Difference Amplifier (TDA)



- Open-loop structure
  - simple structure, small area
  - Sensitive to process variation to result in gain mismatch
- Closed-loop structure
  - Complicated structure, large area
  - Strong to process variation

Power and temperature effect

Power fluctuation

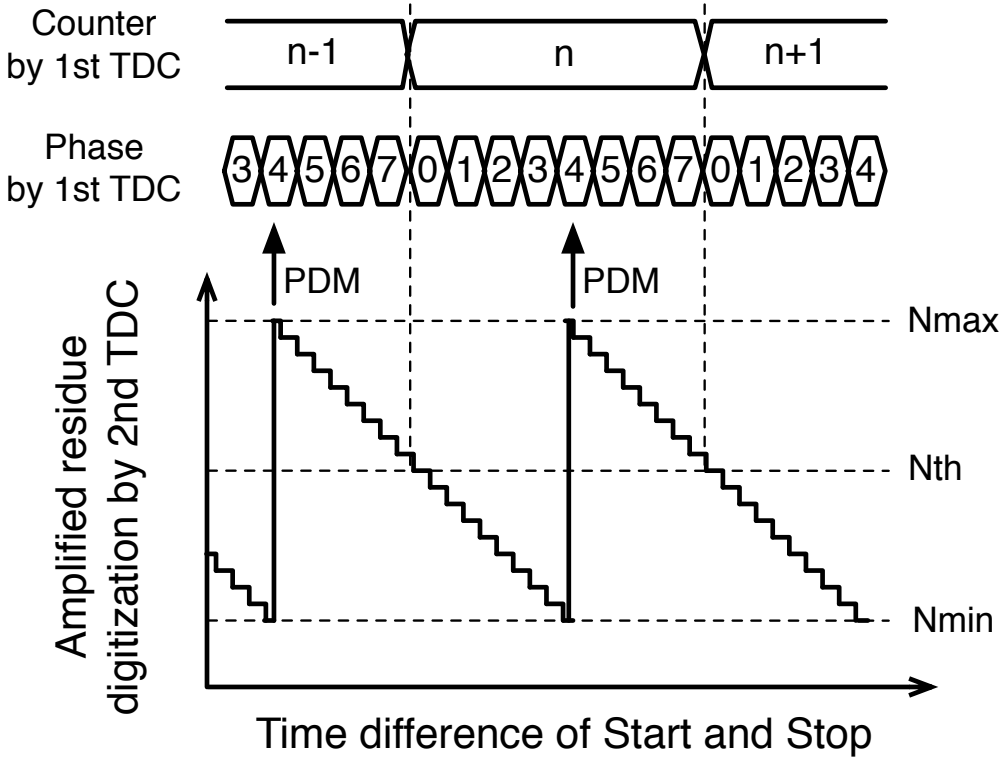
$$G(T) = 1 + \frac{\beta_f (V_{dd} + \Delta V - V_t)^2}{\beta_s (V_{gs} - V_t)^2}$$

Power fluctuation

$$G(T) = 1 + \frac{\beta_f(T)(V_{dd} - (V_{t0} + \alpha v_t \Delta T))^2}{\beta_s(T)(V_{gs} - (V_{t0} + \alpha v_t \Delta T))^2}$$

av_t : temperature coefficient (< 0)

Calculation of final digital codes



TDA gain

$$G = \frac{N_{max} - N_{min}}{8}$$

LSB

$$LSB_{total} = \frac{1}{f_{vco} \times (N_{max} - N_{min})}$$

Row 2nd TDC digital code

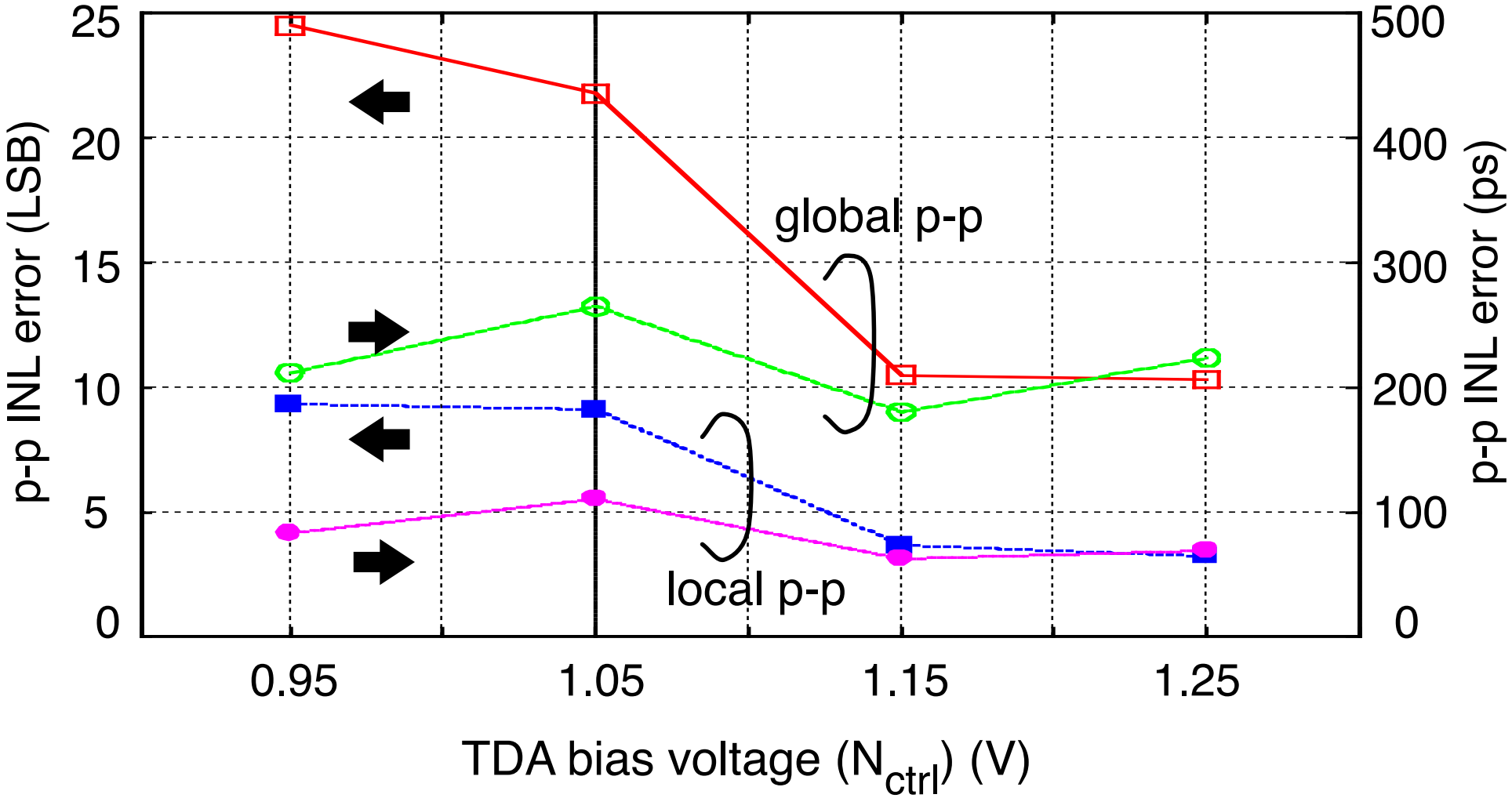
$$D_{2nd} = 8 \times C_{2nd} + P_{2nd}$$

To calculate final digital code

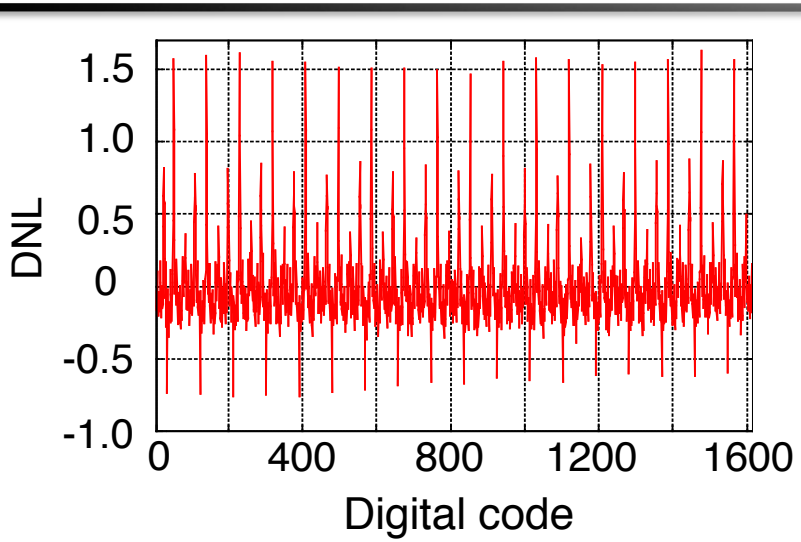
$$D_{2nd\_mod} = \begin{cases} Nmax - D_{2nd} + (Nth - Nmin + 1) & (P_{1st} > PDM - 1 \ \& \ D_{2nd} > Nth) \\ Nth - D_{2nd} & (\text{else}) \end{cases}$$

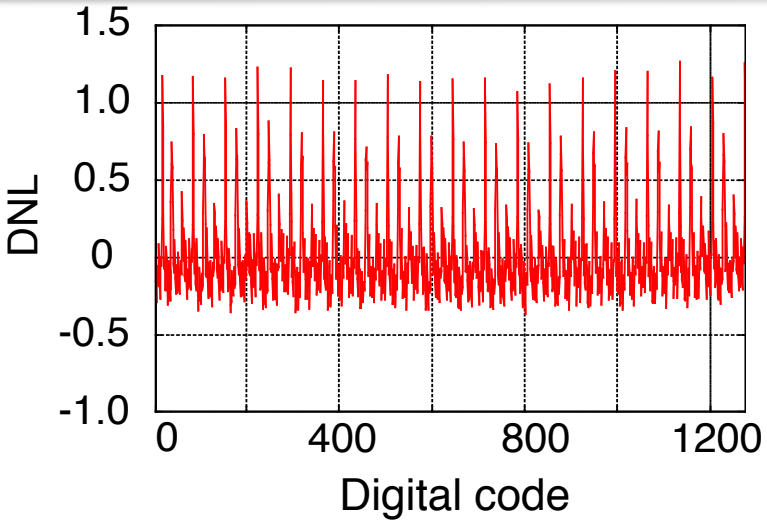
$$D_{total} = C_{1st} \times (Nmax - Nmin) + D_{2nd\_mod}$$

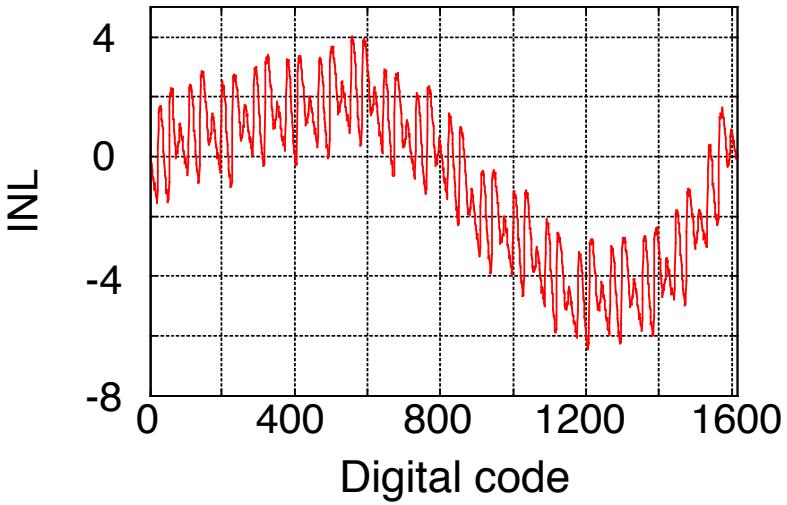
INL change by N_{ctrl}

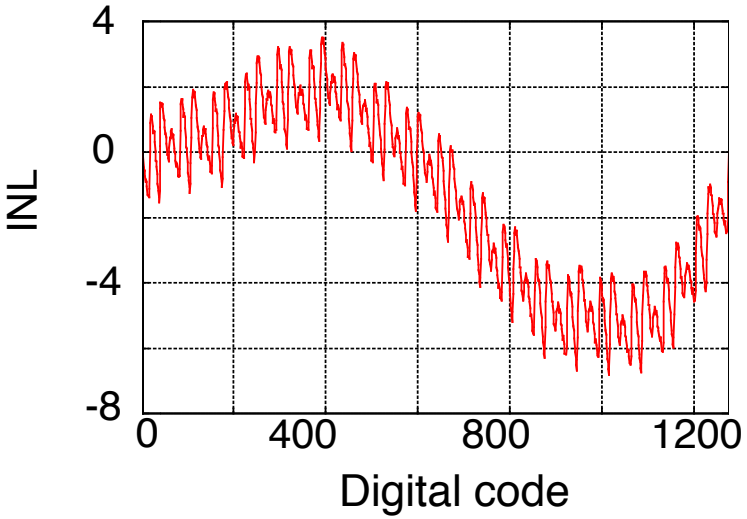


DNL and INL





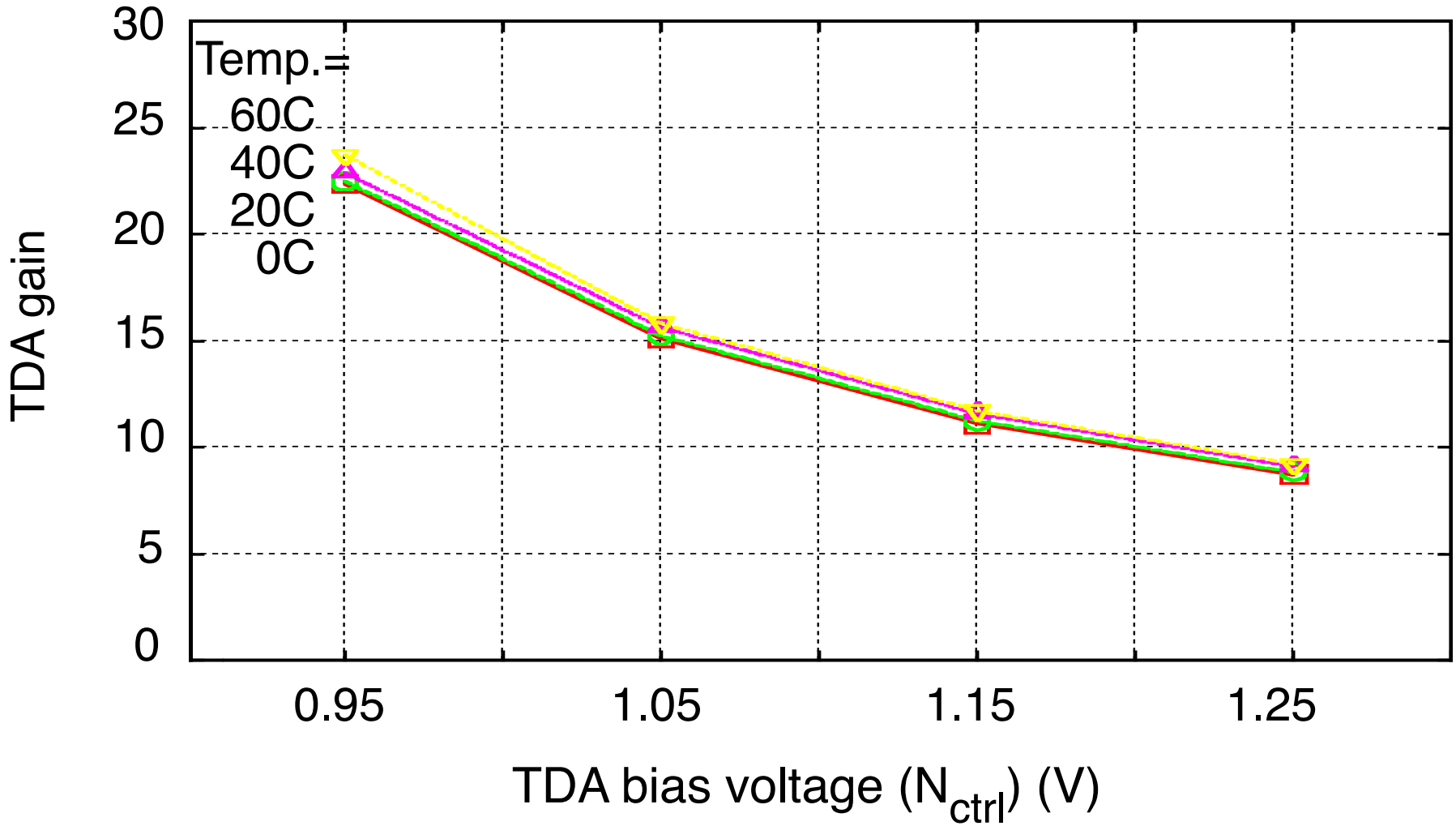




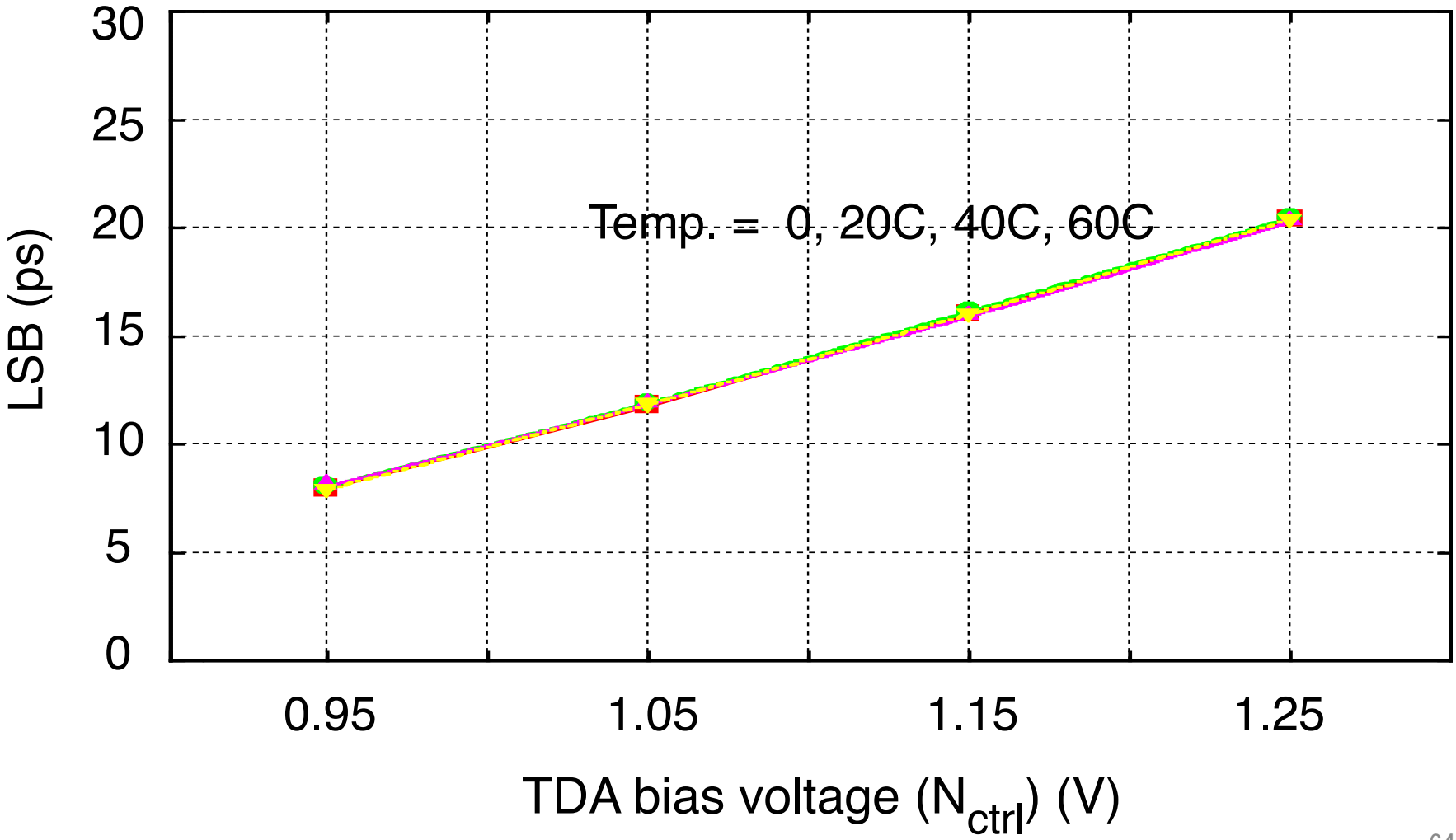
N_{ctrl}=1.15V, LSB=17.1ps

N_{ctrl}=1.25V, LSB=21.4ps

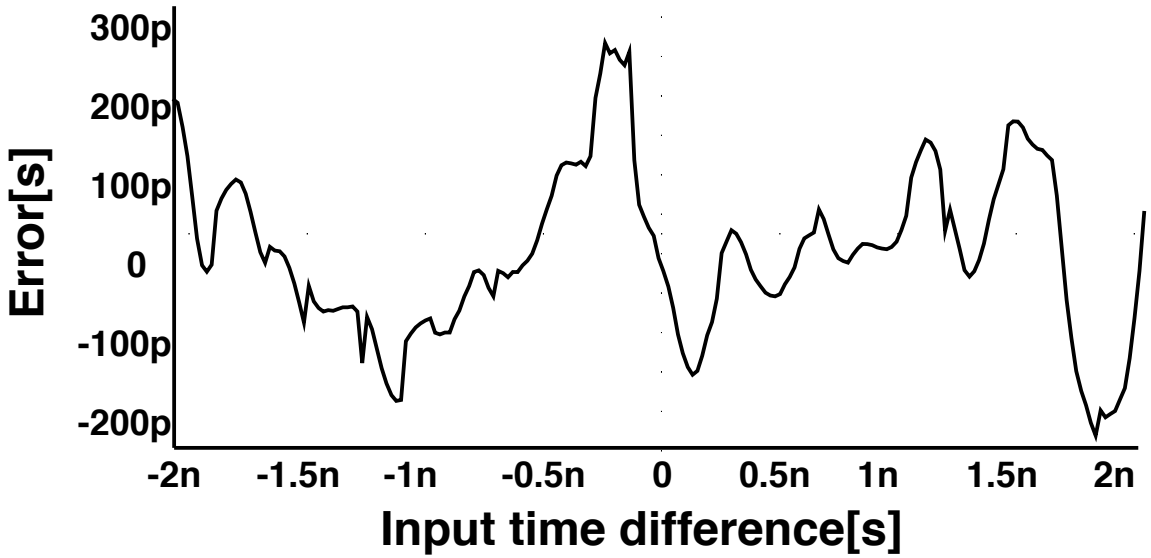
TDA gain variation by temperature fluctuation

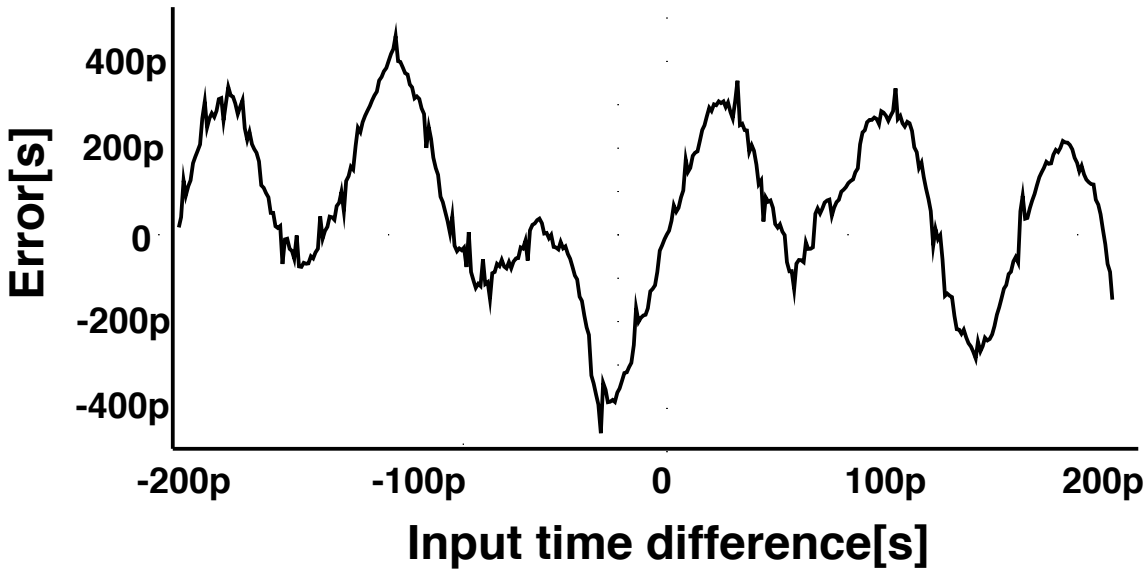


LSB change by temperature fluctuation

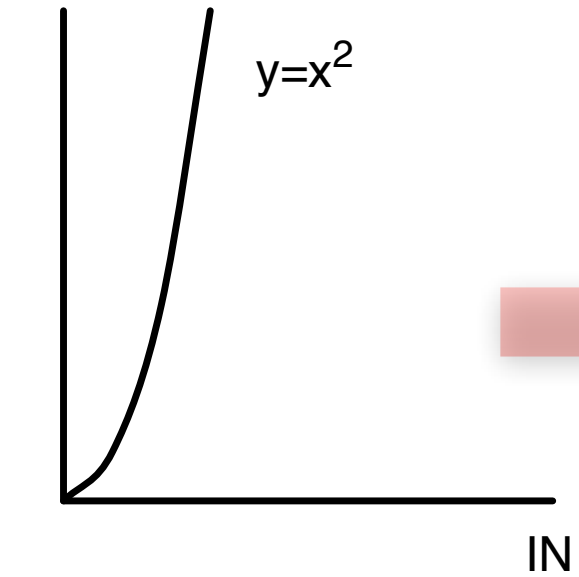


Error of TDA


300p
200p
100p
0
-100p
-200p
Error[s]
-2n
-1.5n
-1n
-0.5n
0
0.5n
1n
1.5n
2n
Input time difference[s]


400p
200p
0
-200p
-400p
Error[s]
-200p
-100p
0
100p
200p
Input time difference[s]

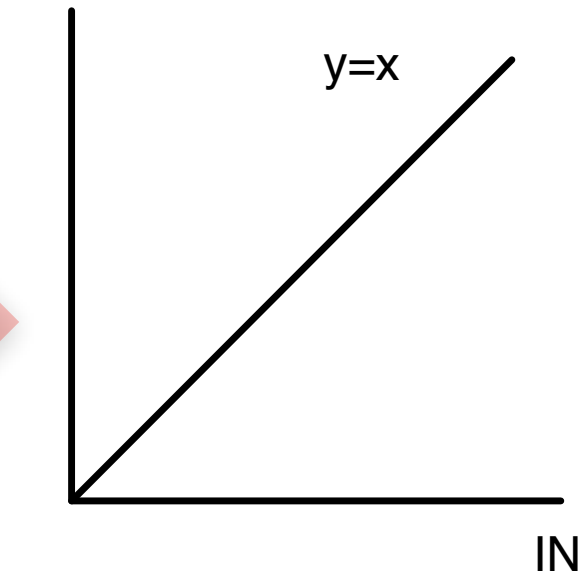
Calibration technique



Raw data
(Before LUT)

LUT

Before	After
0	0
1	1
2	1
3	1
4	2
5	2
6	2
7	2
8	2
9	3
10	3
11	3
…	…



Modified data
(After LUT)

Acknowledgement

- These works are researched in Univ. of Tokyo and TU Delft
- This study partially has been carried out through the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.
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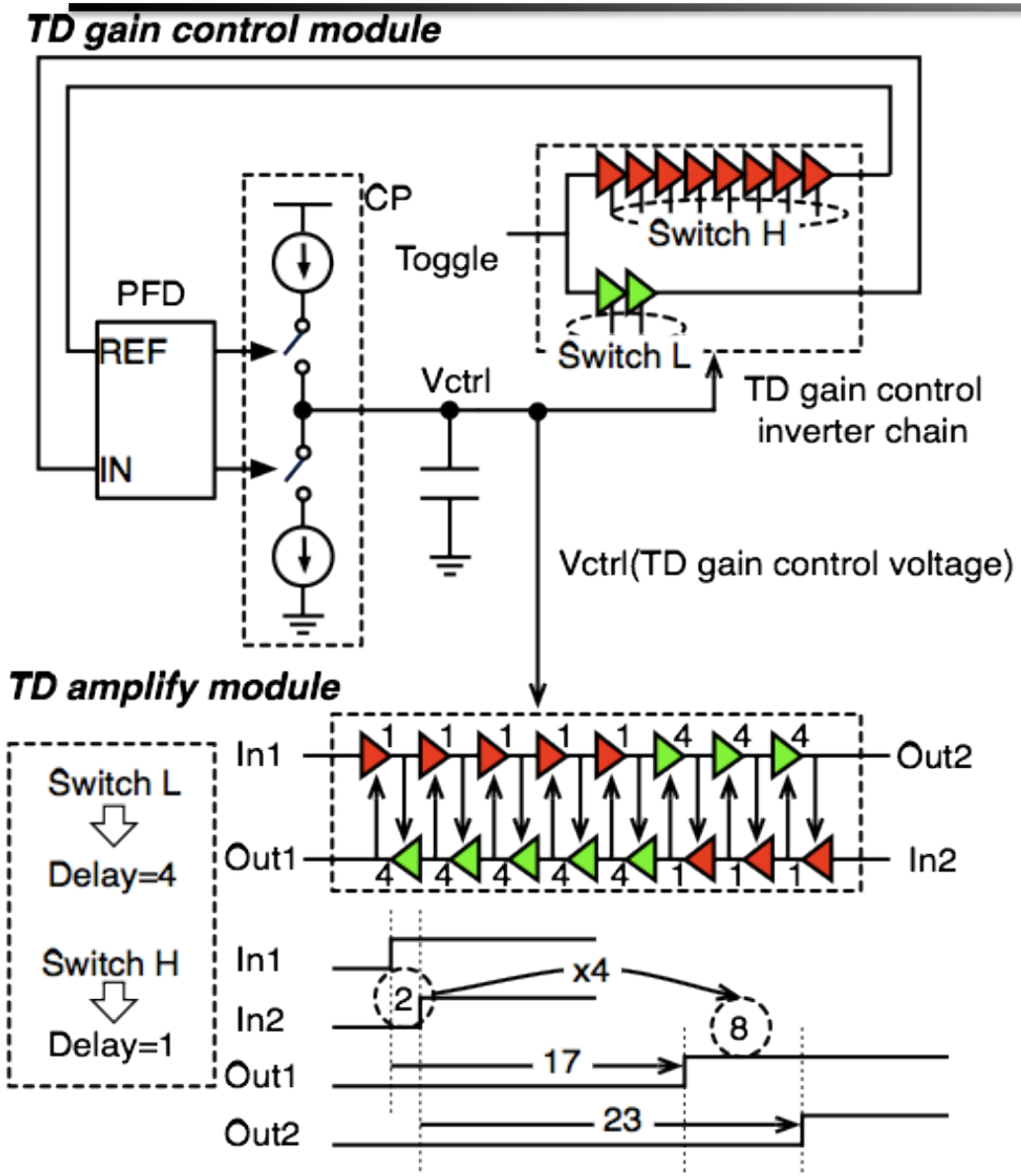
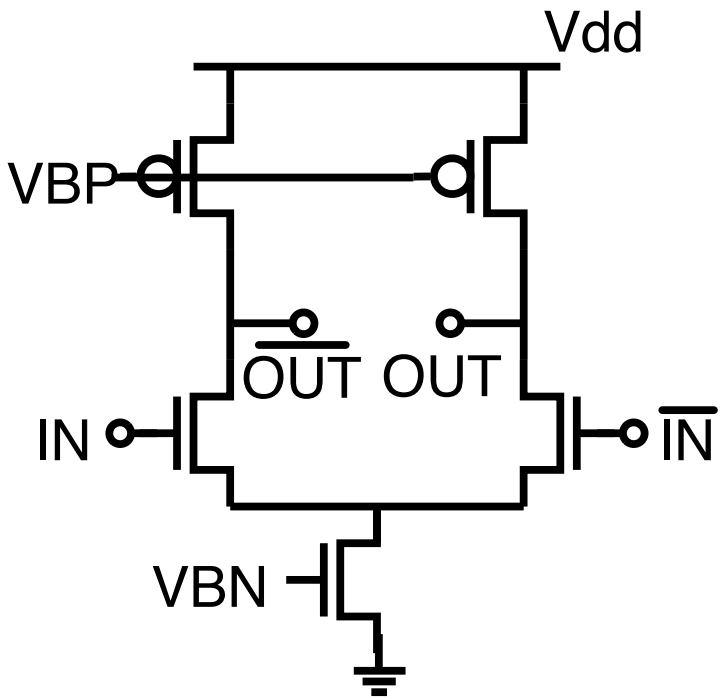
Time Difference Amplifier using Closed Loop Structure



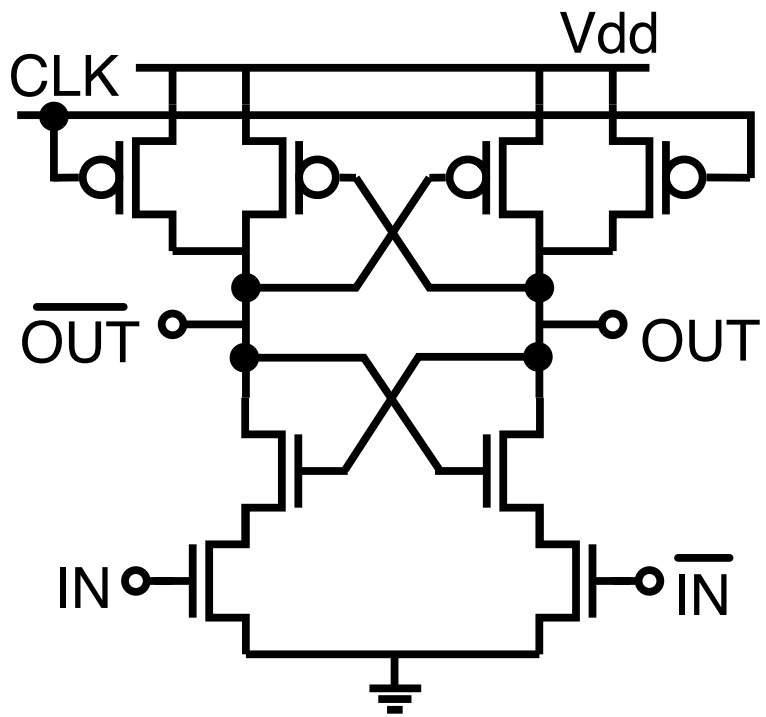
- **Closed loop gain control**
- **TD gain control module**
  - like DLL structure
  - decide gain
  - gain is 4 now
- **TD amplify module**
  - time difference is amplified
- **Strong to PVT variation**

※TD = Time Difference

Each component



Differential inverter



Comparator