Introduction to Time-to-Digital Converters

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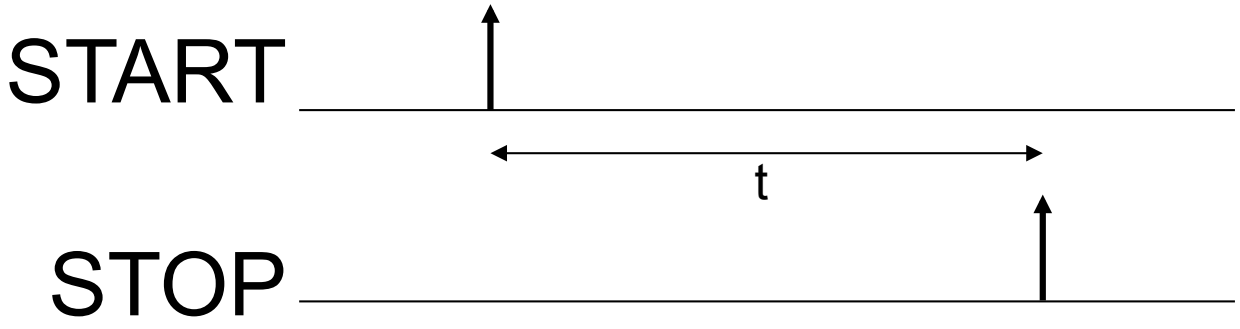
Outline

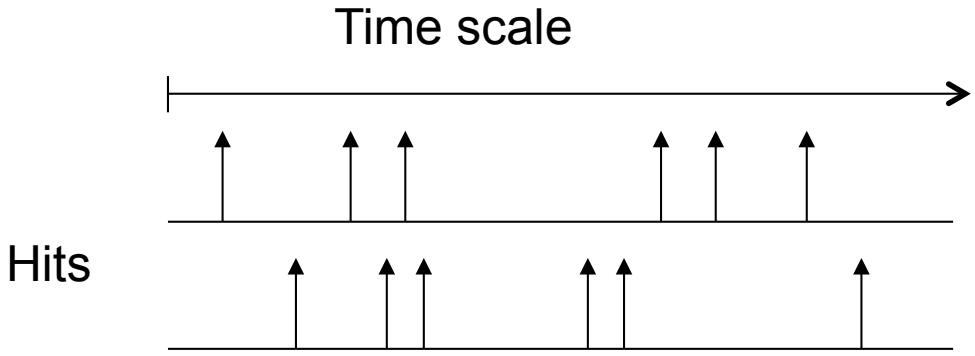
- TDC Basics
- Architectures
- Case Study
- ASIC vs. FPGA
- Conclusions

TDC Basics

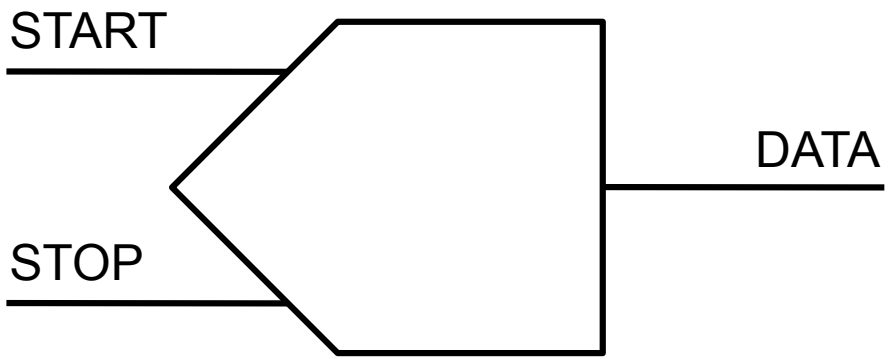
TDC Objective



But, in most cases:



TDC Symbol



Basic Definitions

- Bin size or resolution – τ (sec)
  - Minimum distance between time events that can be resolved
- Range (sec)
  - Maximum time difference that can be measured
- Conversion rate (MS/sec)
- Latency (sec)
- Non-linearities (LSB)
  - Differential non-linearity (DNL)
  - Integral non-linearity (INL)
- Single-shot accuracy (sec)

DNL / INL definition

DNL: Differential Non-Linearity

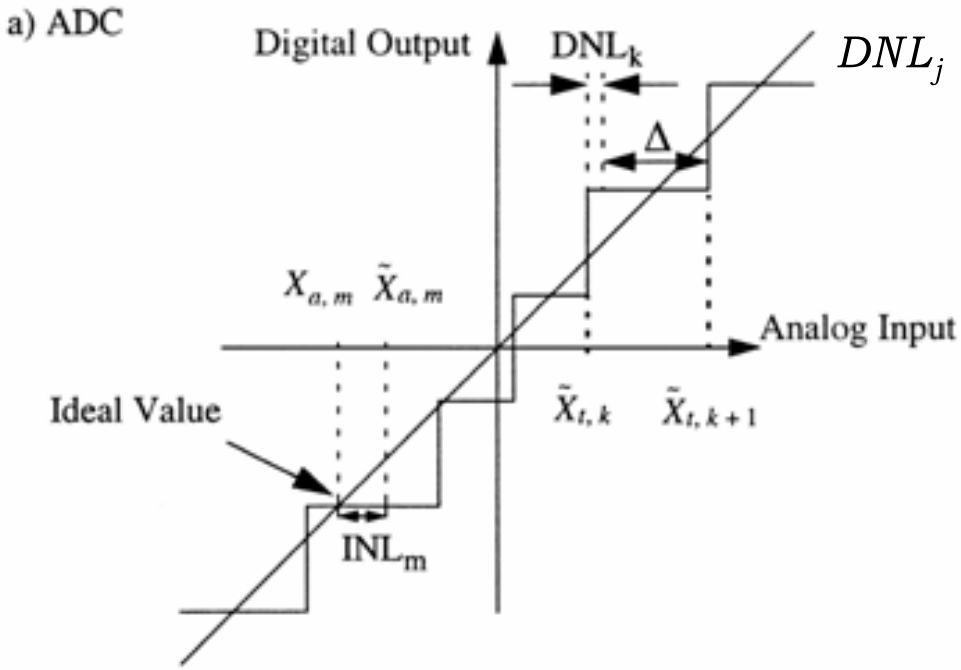
INL: Integrated Non-Linearity

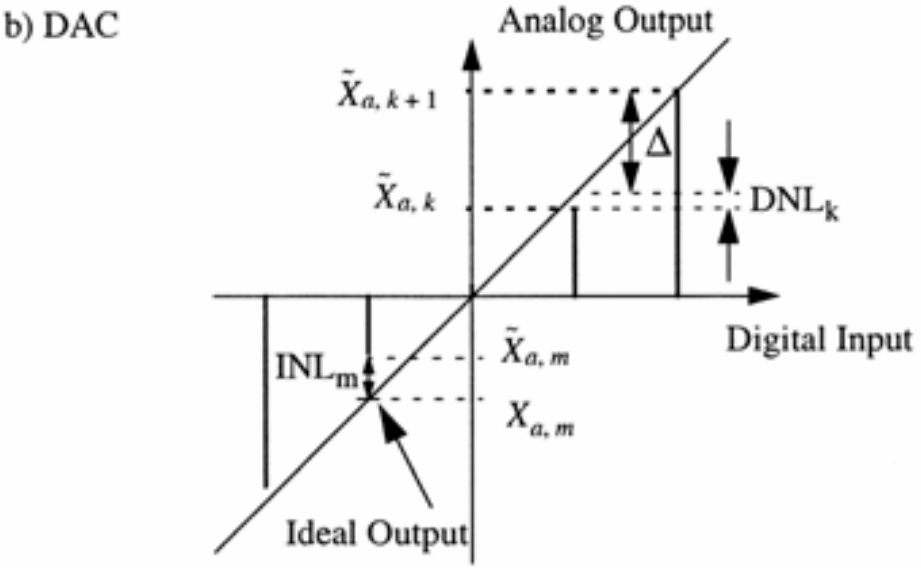
$$DNL_j \equiv \frac{Width_{ACTUAL,j} - Width_{IDEAL}}{Width_{IDEAL}}$$

$$INL_j \equiv Transf\,erf\,unction_{ACTUAL,j} - Transf\,erf\,uction_{IDEAL,j}$$

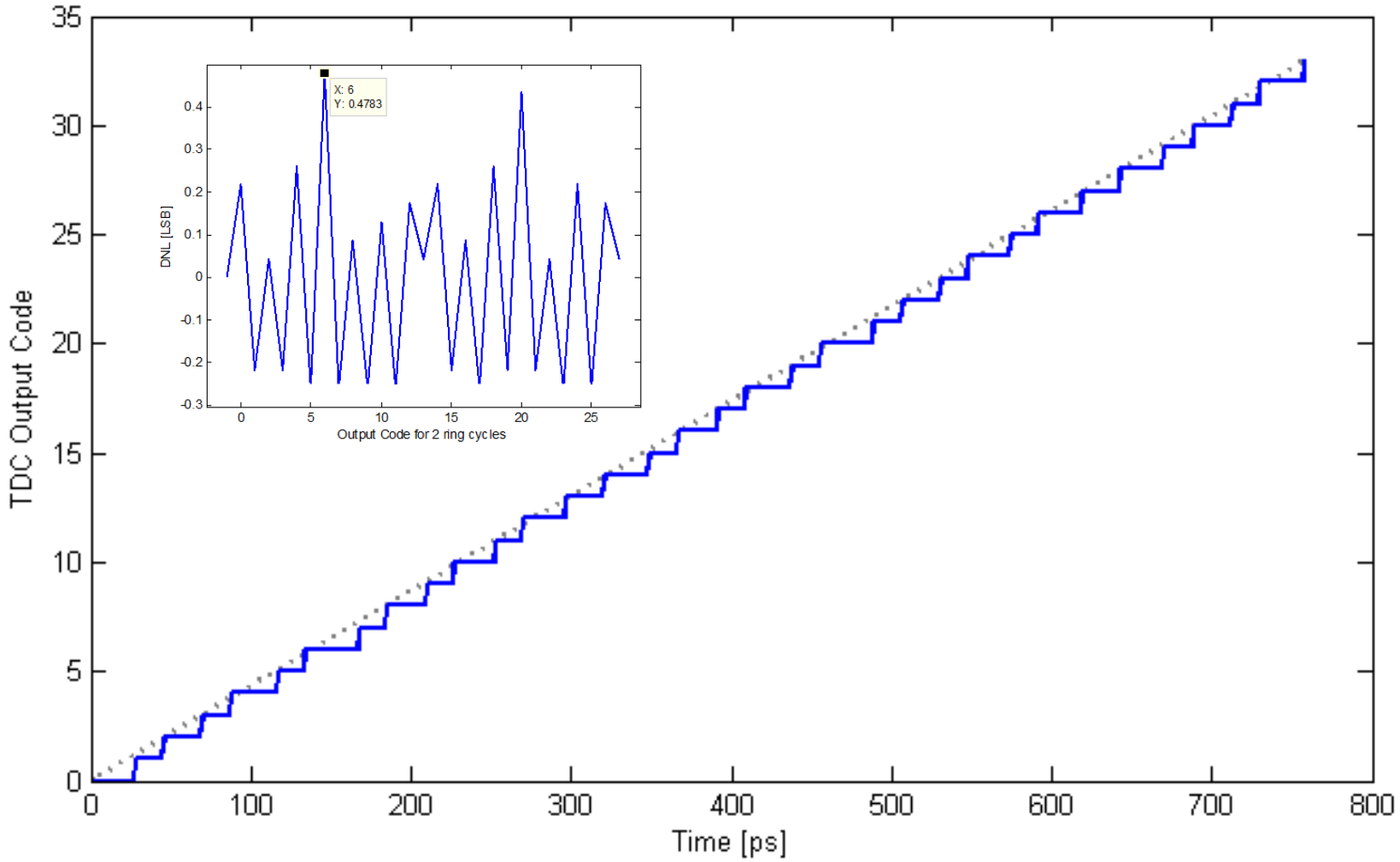
$$INL_j = \sum_{k=0}^{k=j} DNL_k$$

$$DNL_j = INL_{j+1} - INL_j$$



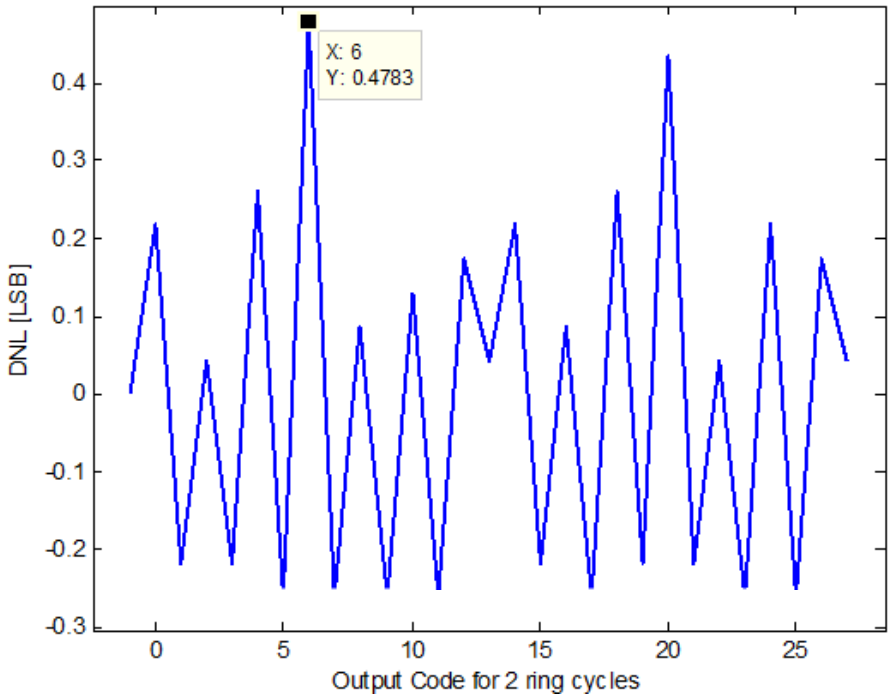


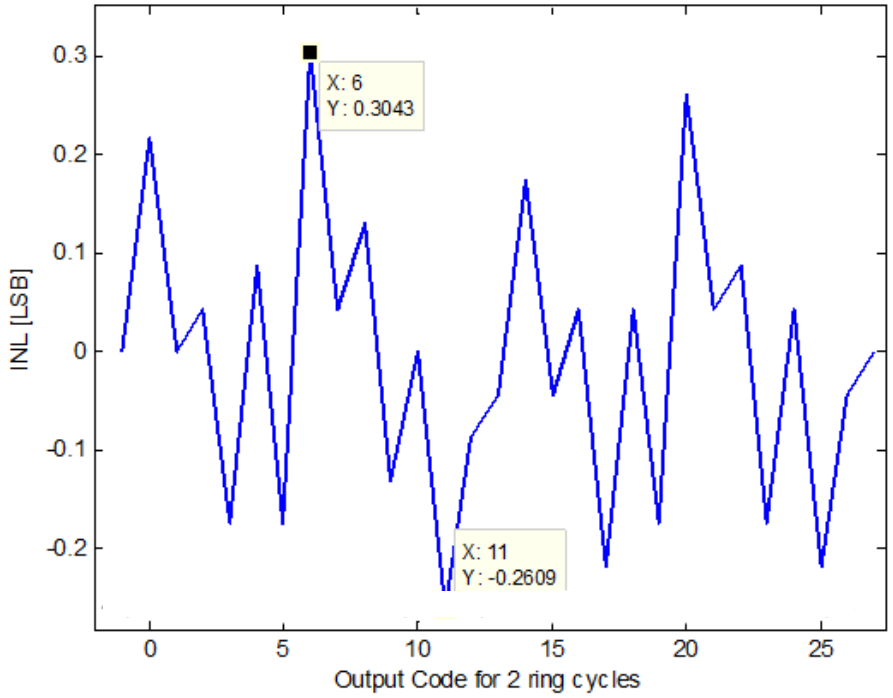
TDC Non-Idealities



DNL, INL

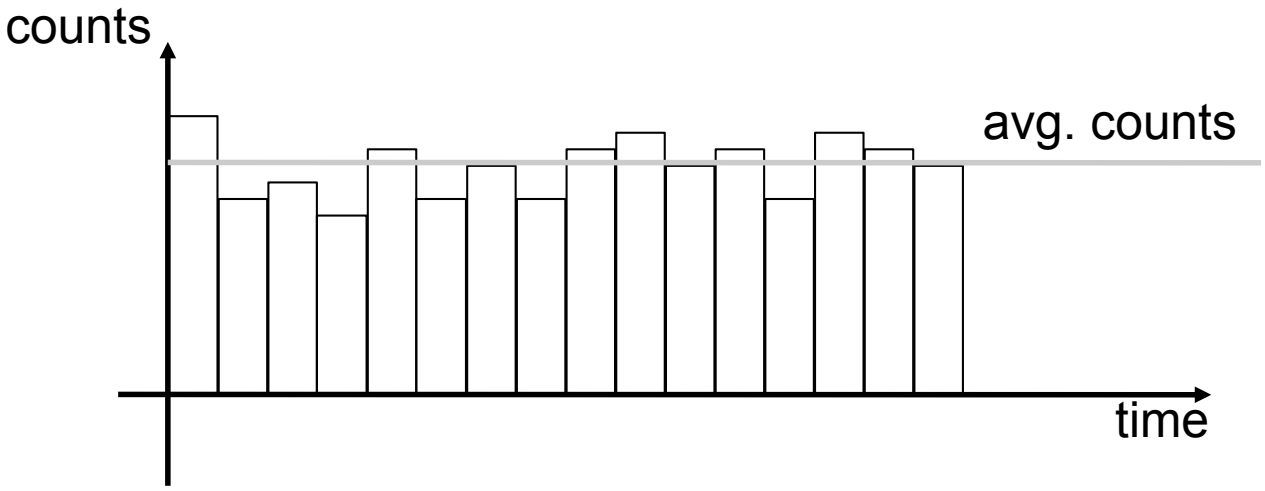
- Integral non-ideality (INL) is the integral of DNL
- Depending upon definition, starts and ends at 0





How to Measure: Density Test

- Poisson distributed uniform START generator
- Measure statistics of TDC measurements per bin
- Normalize to average counts, differences are DNL points

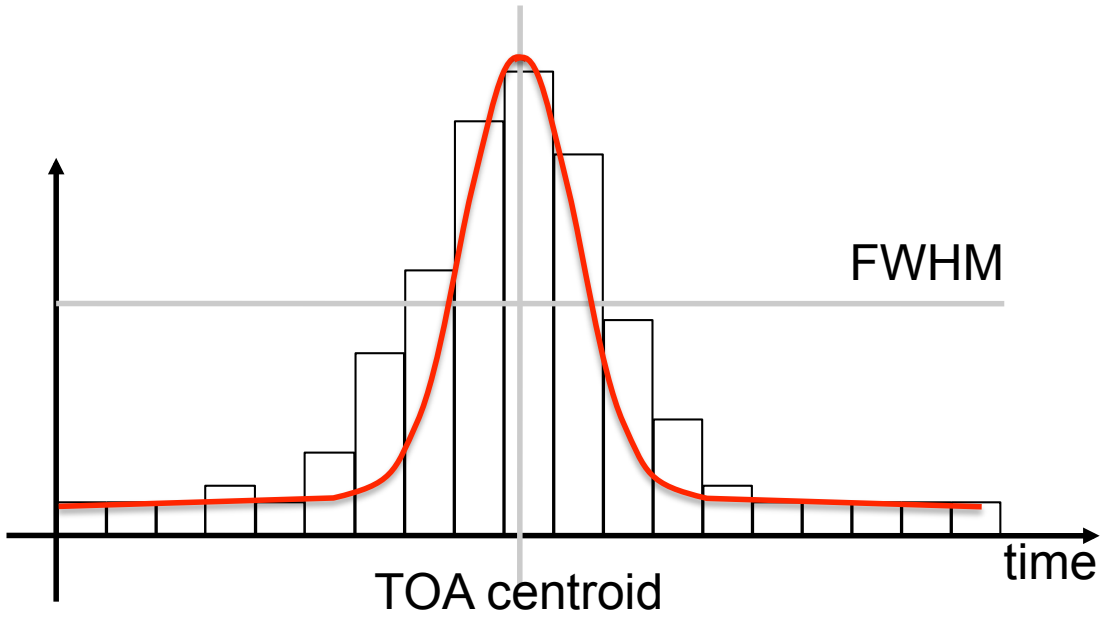


Input Non-Idealities

- Signals are non-Dirac
  - Non-zero rise time
  - Non-zero width
- START-STOP sequence is not regular
- Signals have jitter in
  - Time
  - Amplitude
- Temperature
- Supply variations

Single-Shot Accuracy (SSA)

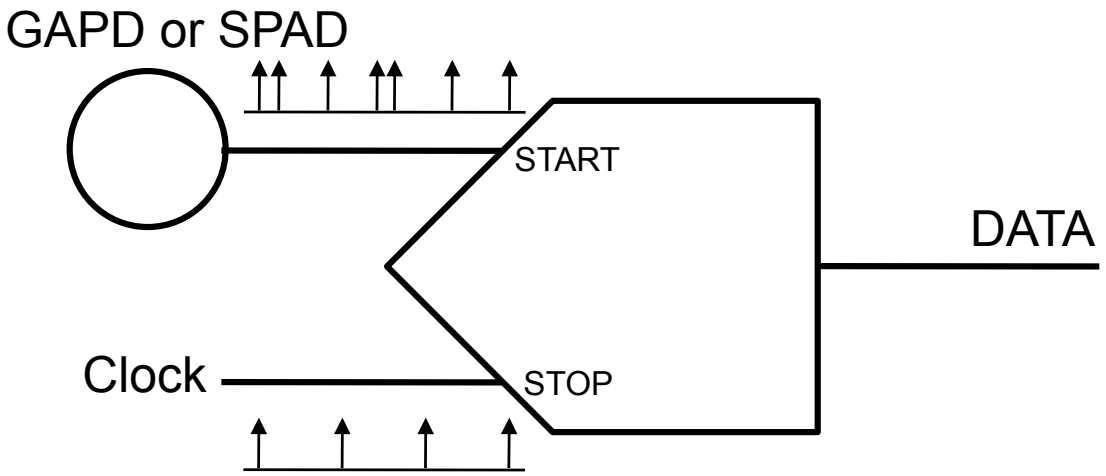
- Repeat measurement of single time-of-arrival and construct histogram
- Derive statistics by Gaussian fitting and calculation of FWHM or σ or 3σ.



Optical Tests

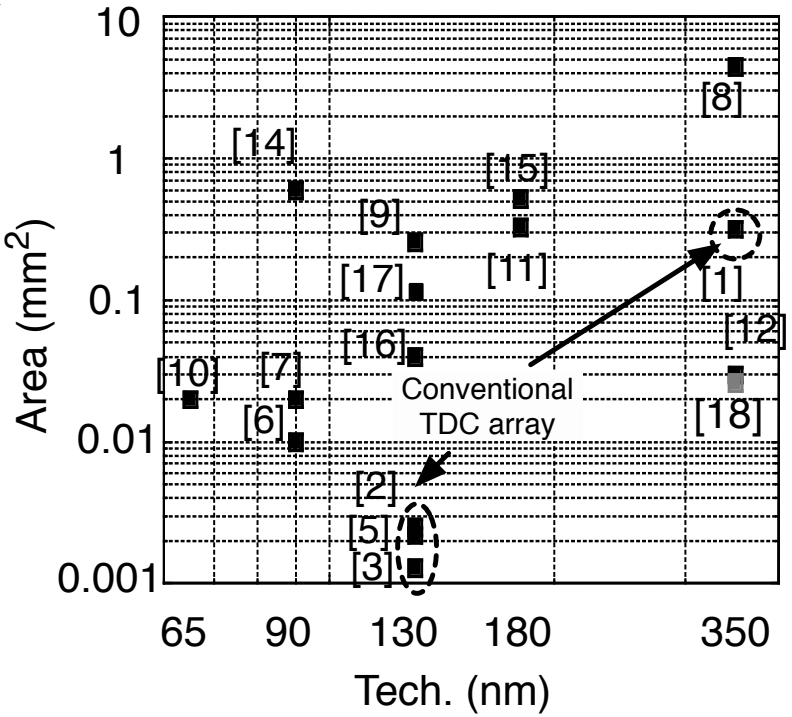
- Density test: free running SPAD
- Single-shot experiment:
  - Histogram Δt_i, $i=[1 \ldots N]$

  (time-correlated single-photon counting – TCSPC)



Figures of Merit

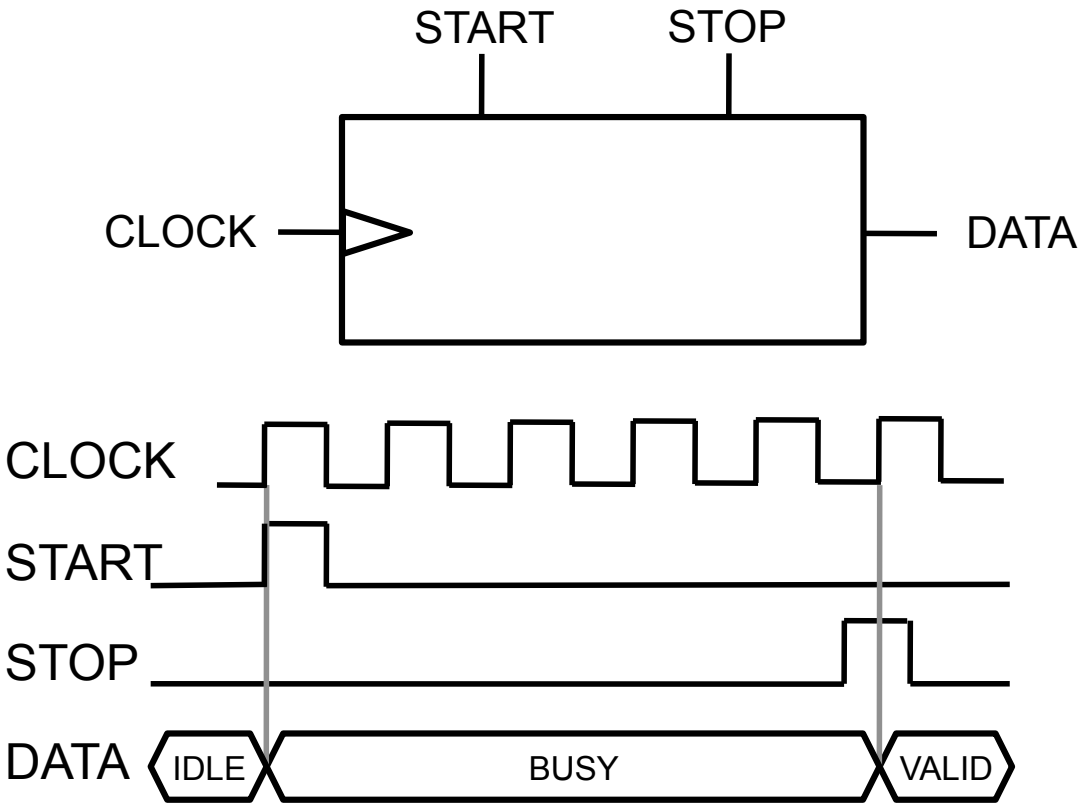
- Power, resolution, DNL/INL, SSA, area
- Temperature stability
- Cross-talk



Architectures

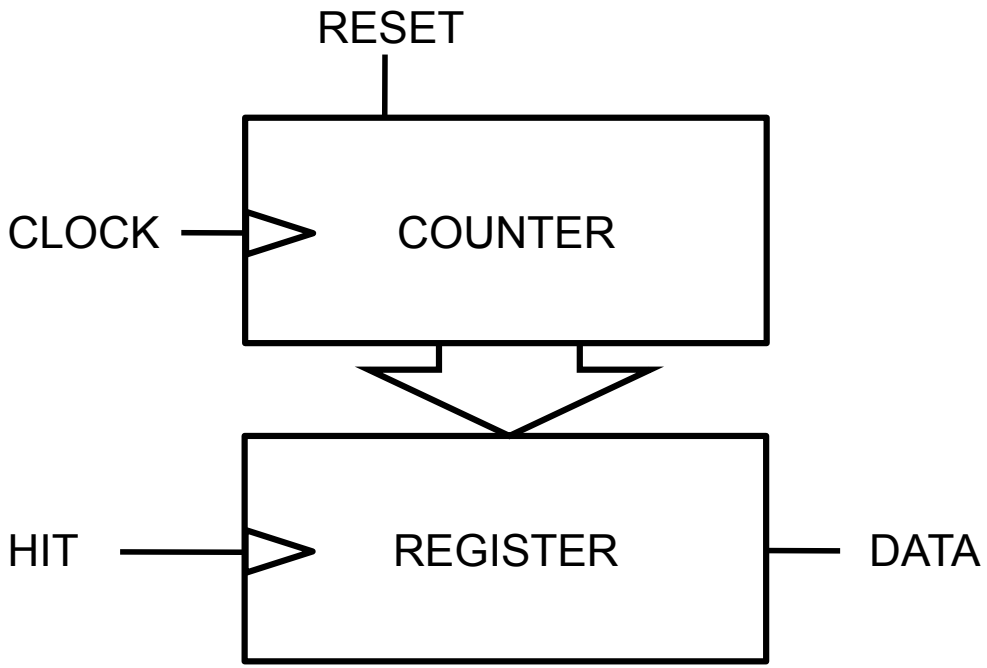
The Simplest: A Counter

- Resolution: $\tau = 1/f_{\text{clock}}$
- Conversion rate = 1/latency



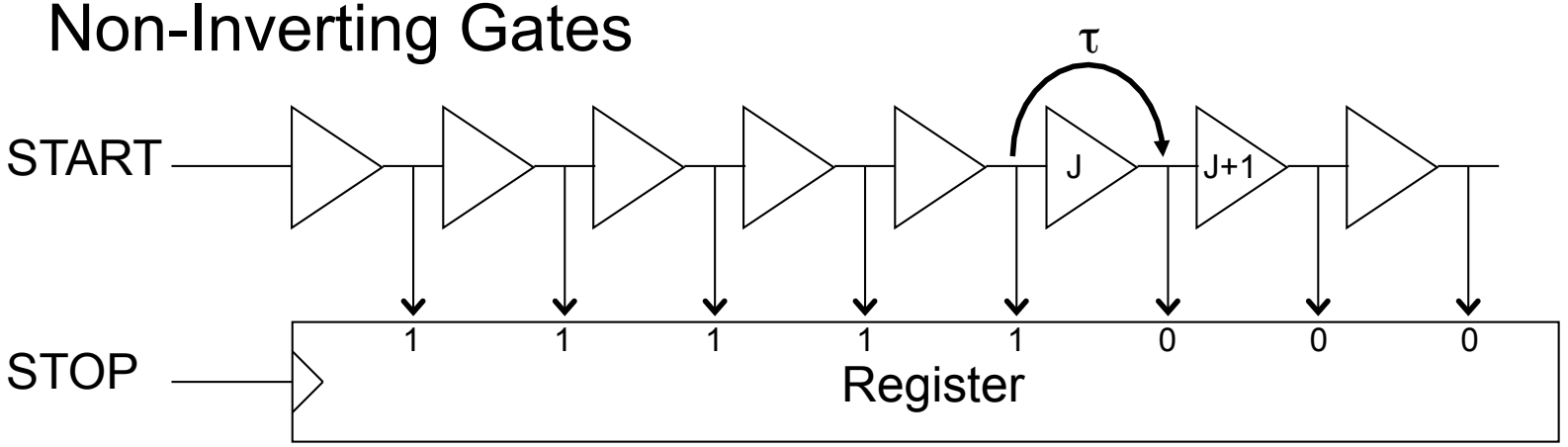
Counter – Register

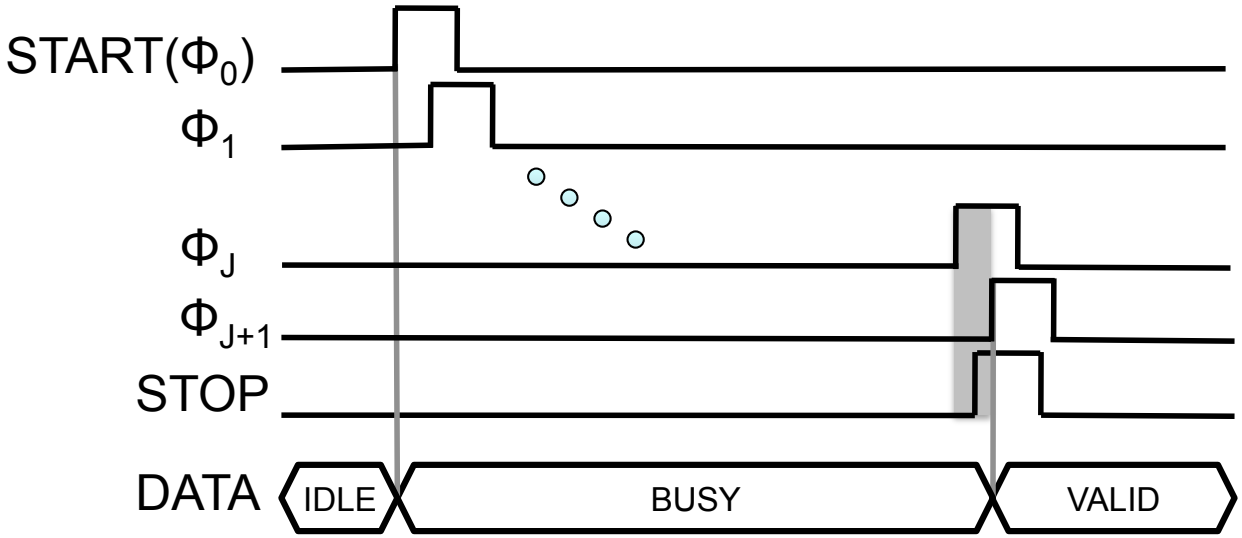
- Advantage: fast counter can be shared among many HIT lines
- Fast registers easier to build



Delay Chain

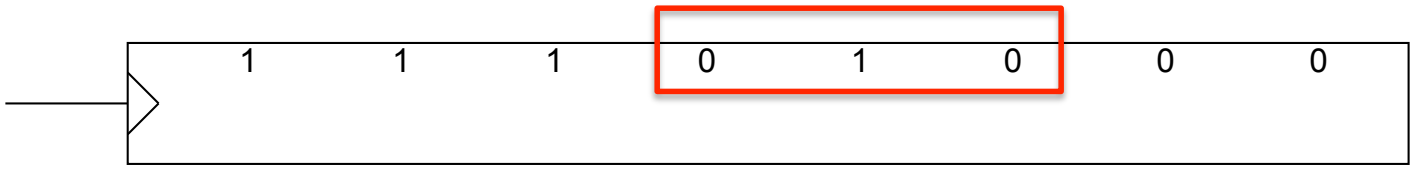
- Non-Inverting Gates



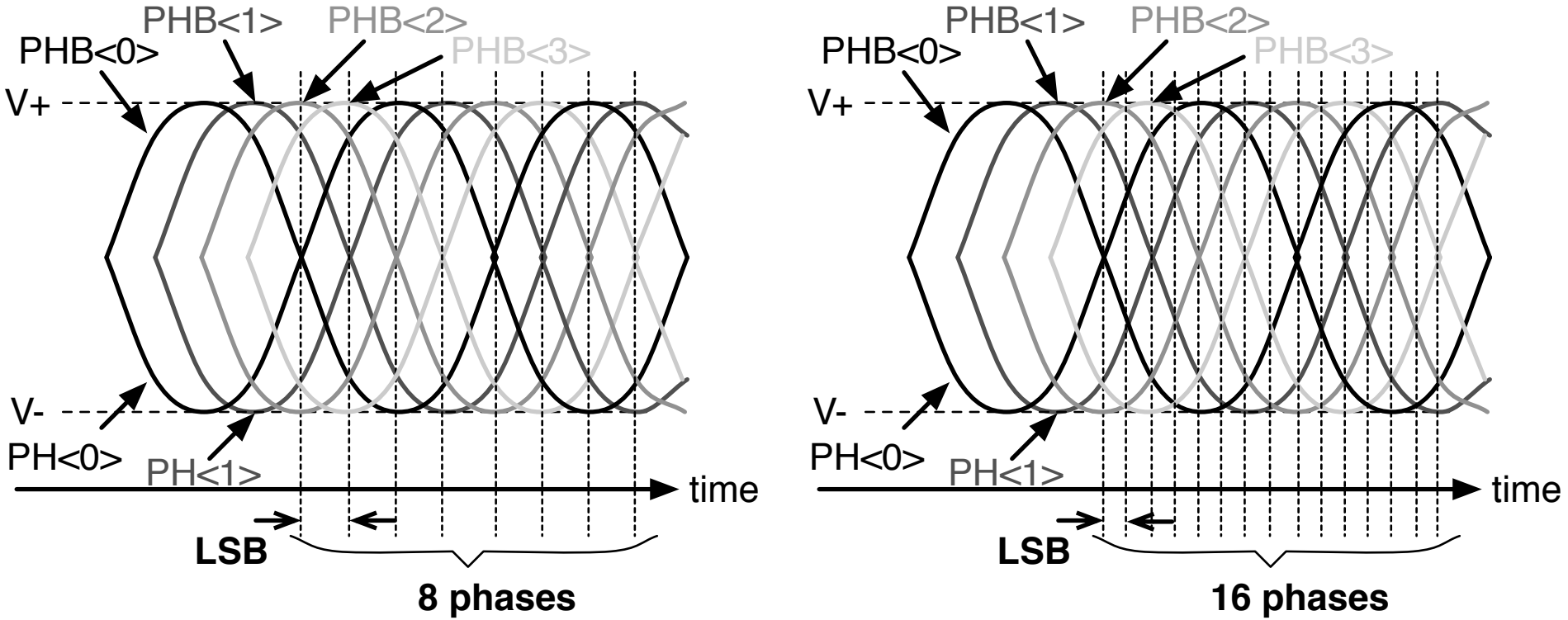


Delay Chain

- Resolution: τ = delay element
- Conversion rate = 1/latency
- Latency = $N \times \tau$
- Need a thermometer decoder: $N \rightarrow \log_2(N)$
- Issues: metastability, bubbles



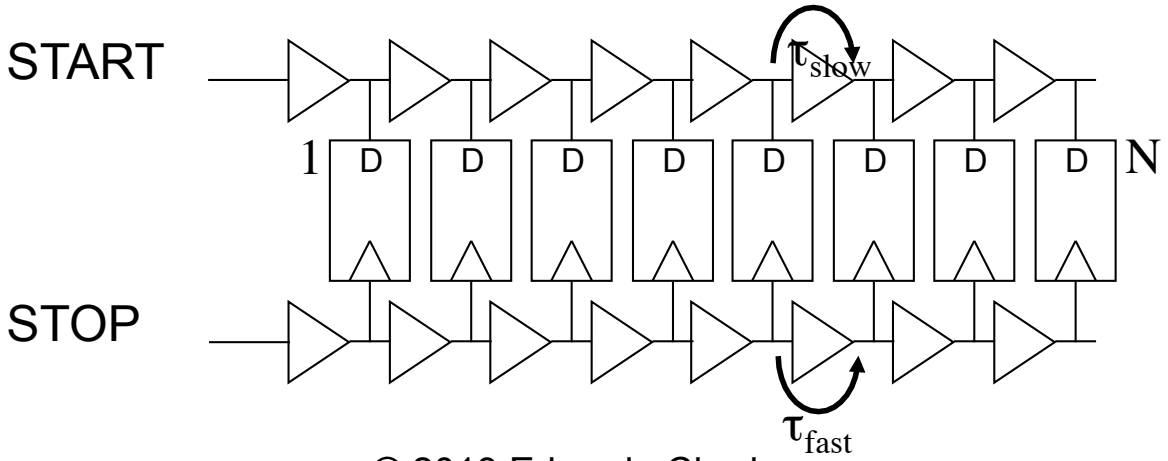
Phase Interpolator



- DLL, Passive component, Different threshold, Different offset for comparators
- Require area to achieve high resolution
- Can combine with other techniques easily

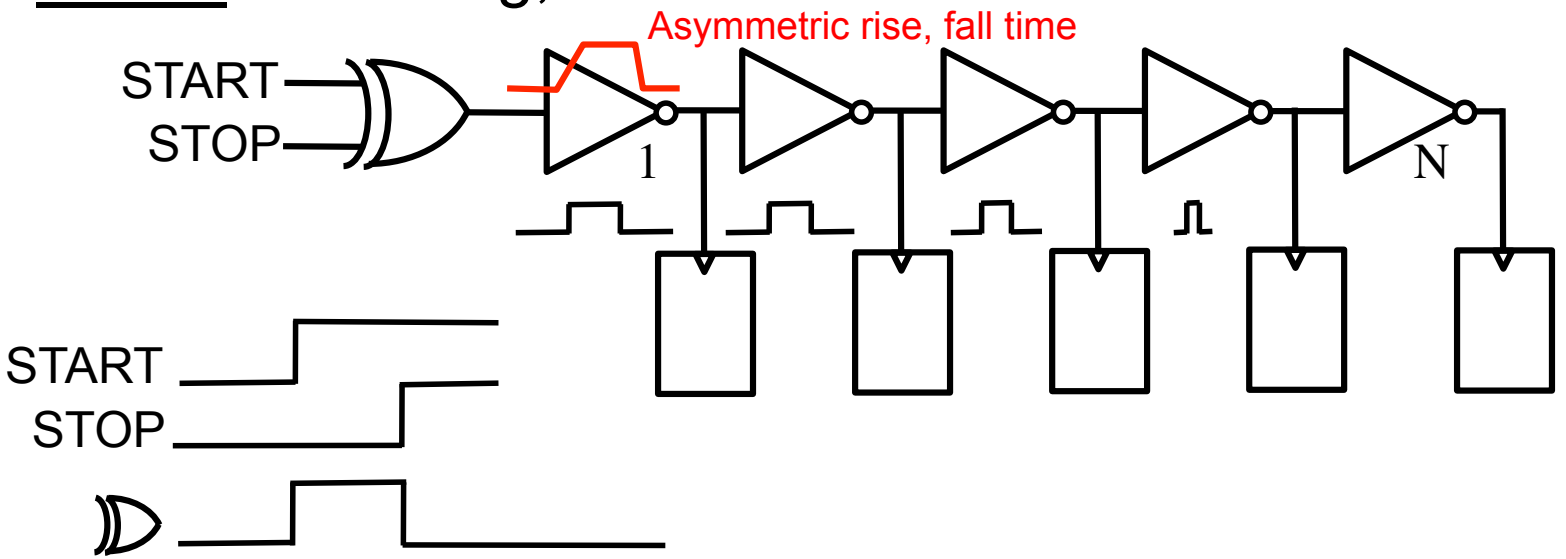
Vernier Lines

- Resolution: $\tau = \tau_{slow} - \tau_{fast}$
- Conversion rate = 1/latency
- Latency = $N \times \tau_{slow}$
- Need a thermometer decoder: $N \rightarrow \log_2(N)$
- Issues: metastability, matching, **big area, slow conversion rate**



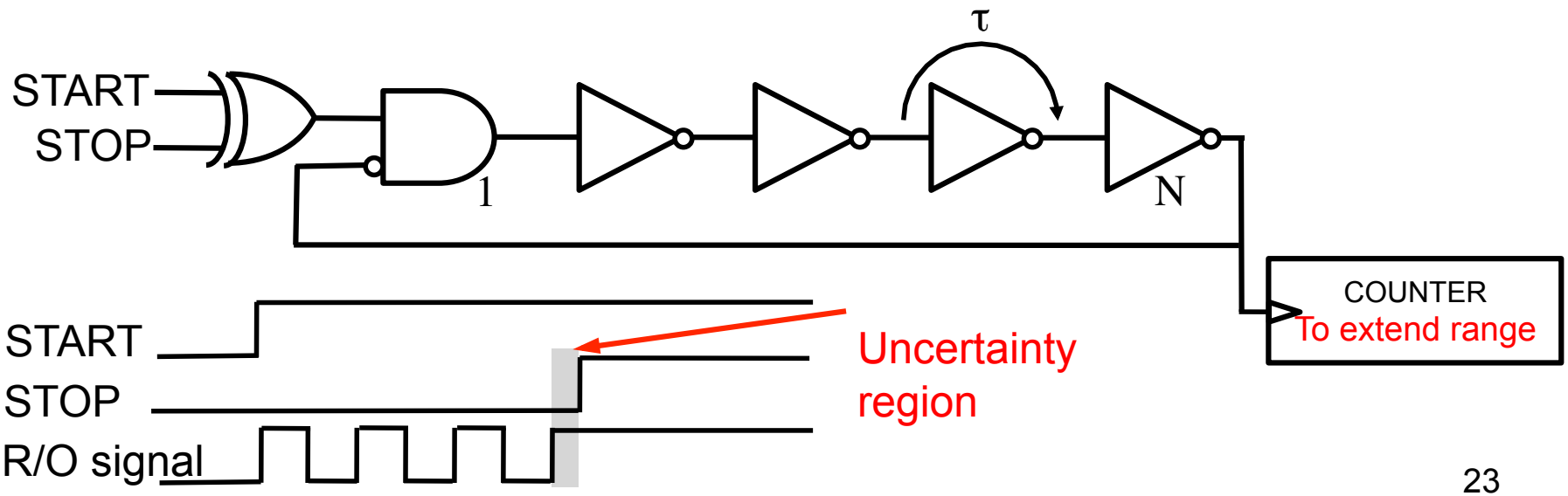
Pulse Shrinking

- Resolution: $\tau = \tau_{rise} - \tau_{fall}$
- Conversion rate = 1/latency
- Latency = $N \times \tau_{slow}$
- Need a thermometer decoder: $N \rightarrow \log_2(N)$
- Issues: matching, **slow conversion rate**



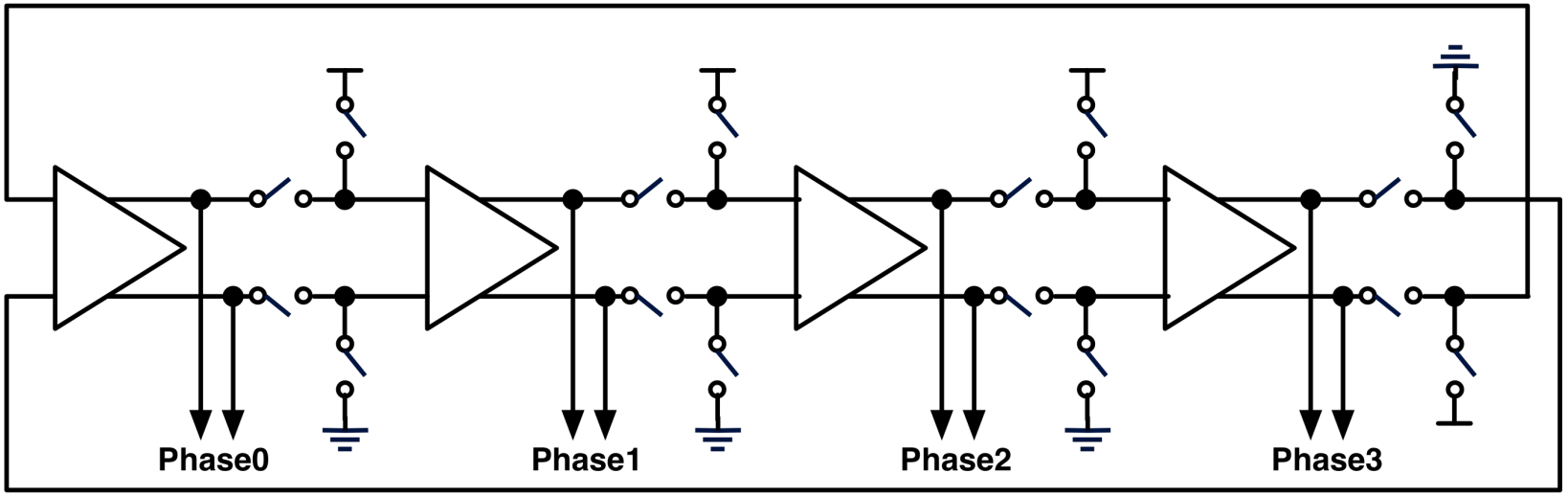
Ring Oscillators

- Resolution: τ = delay element
- Conversion rate = 1/latency
- Latency = $N \times \tau$
- Need a thermometer decoder: $N \rightarrow \log_2(N)$
- Issues: metastability, matching, asymmetric load



Actual Implementation

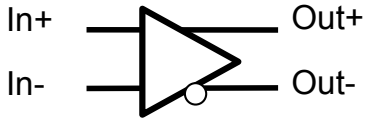
- Fully differential
- Partial propagation readout
  - lower oscillation frequency or higher resolution
  - Rise times and fall times doubles resolution
- Invariant load to improve linearity

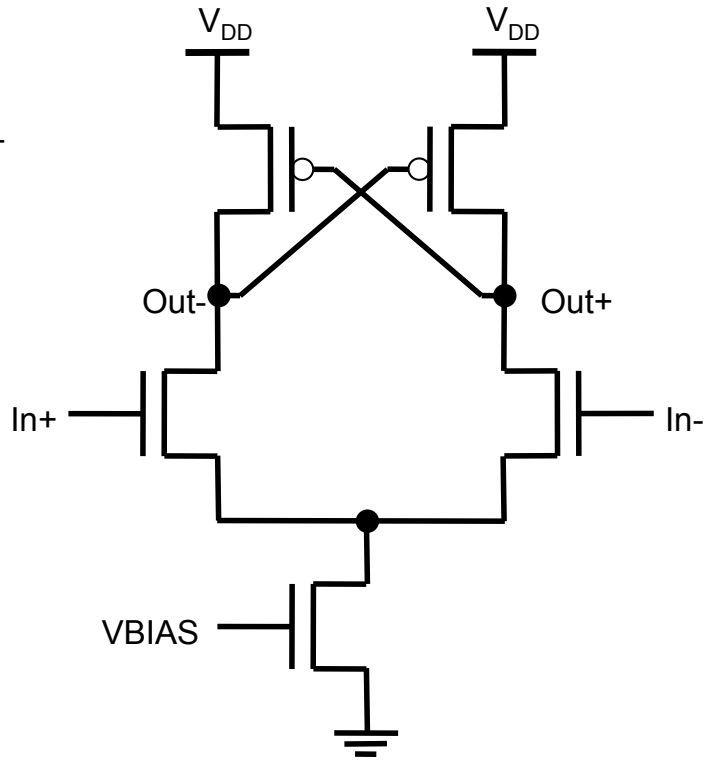


Mandai and Charbon, ESSCIRC11

Delay Element Implementation

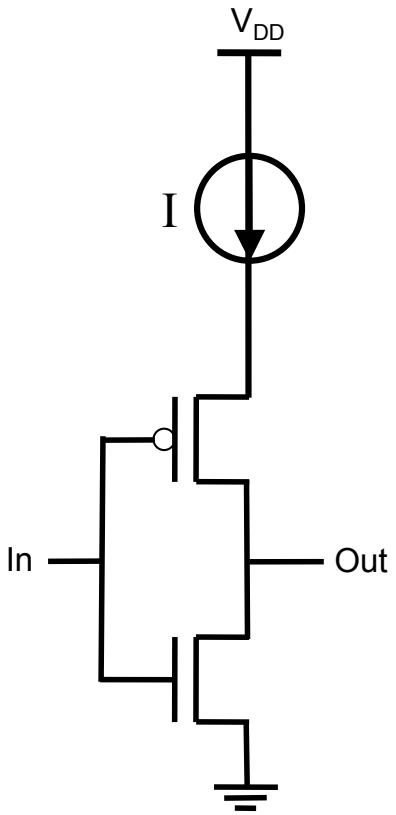
- Uniform rise/fall time
- Bias control used for feedback
- Positive feedback for speed





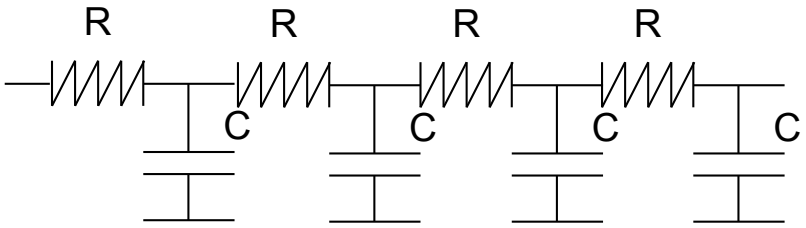
Asymmetric Rise/Fall Time

- E.g. inverter starved cell
- Rise time =V_{DD}• C_{load}/I
- Fall time: inverter delay

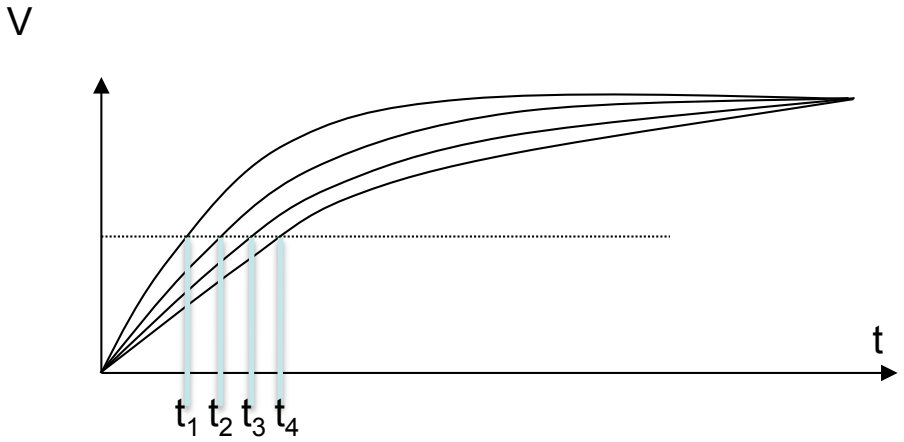


Semi-Digital TDCs

- Determine time difference based on propagation through an RC line

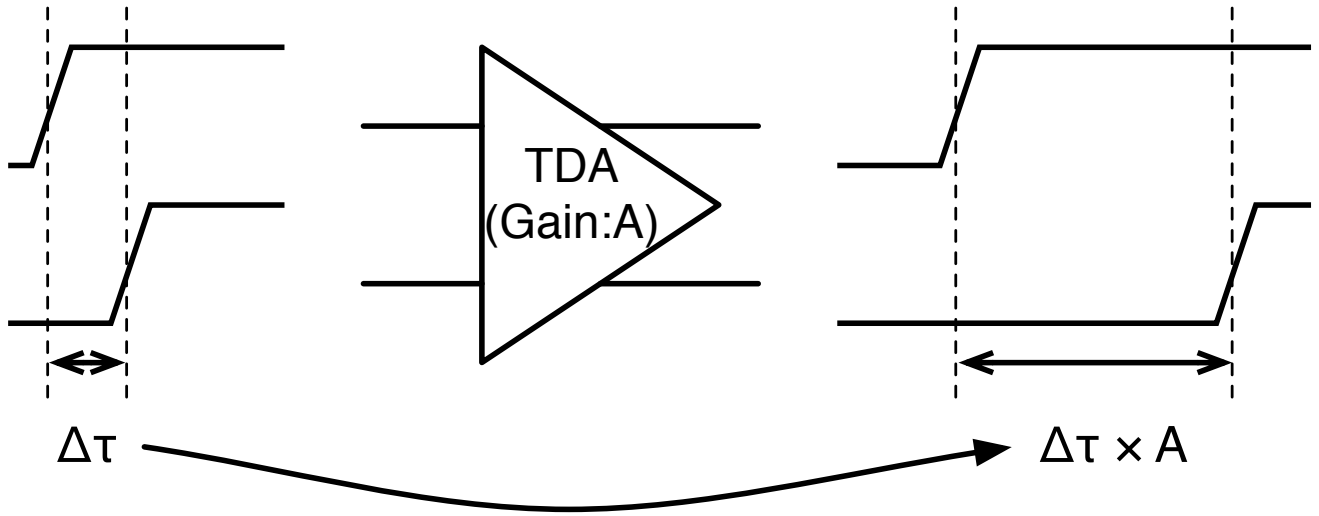


RC delay chain



Time Difference Amplifier (TDA)

- Time differences are multiplied as in successive approximation ADCs
- Issues: gain stability, jitter



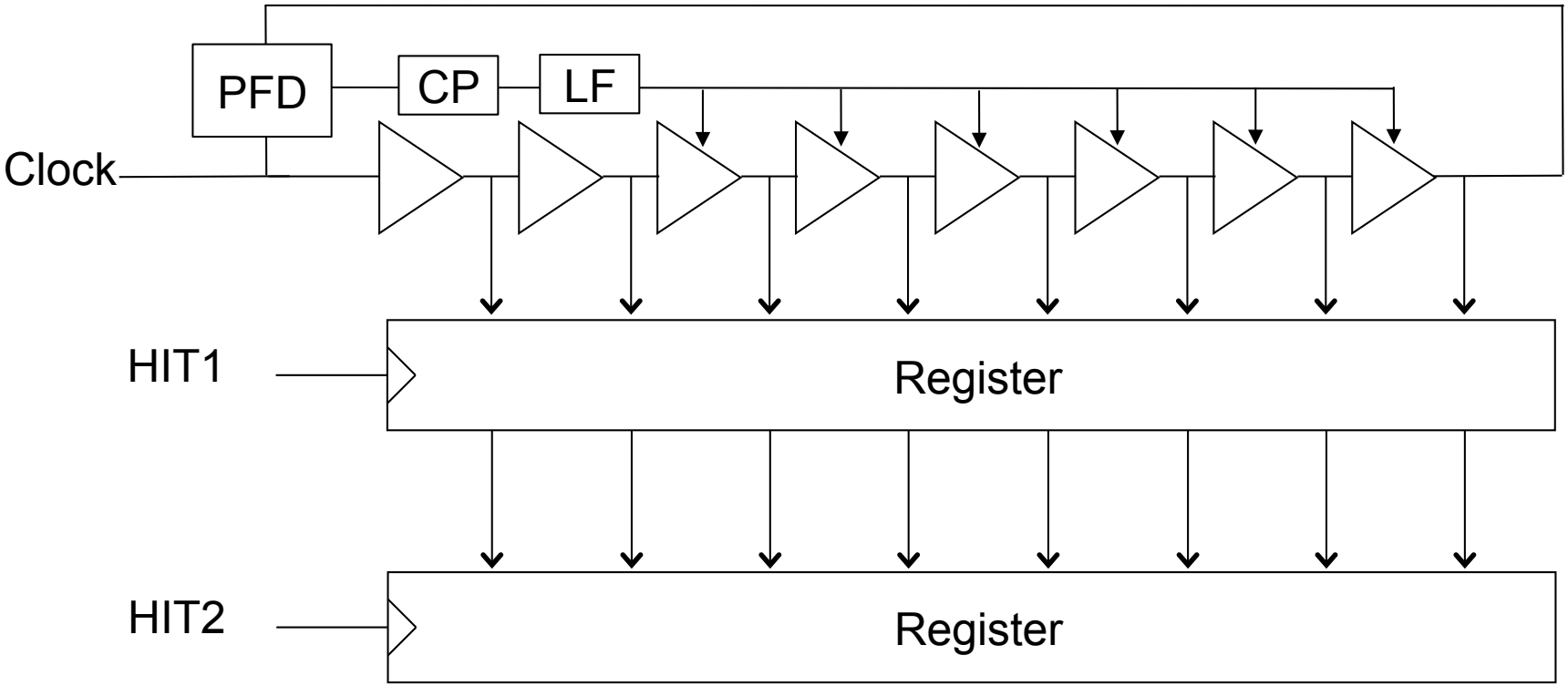
Other Composite TDCs

- Counter + Phase Interpolator + Vernier
  Niclass *et al.*, JSSC08
- Ring Oscillators + Counters
  Veerappan *et al.*, ISSCC11
- Ring Oscillators + TDA
  Mandai and Charbon , ESSCIRC11

… and many more

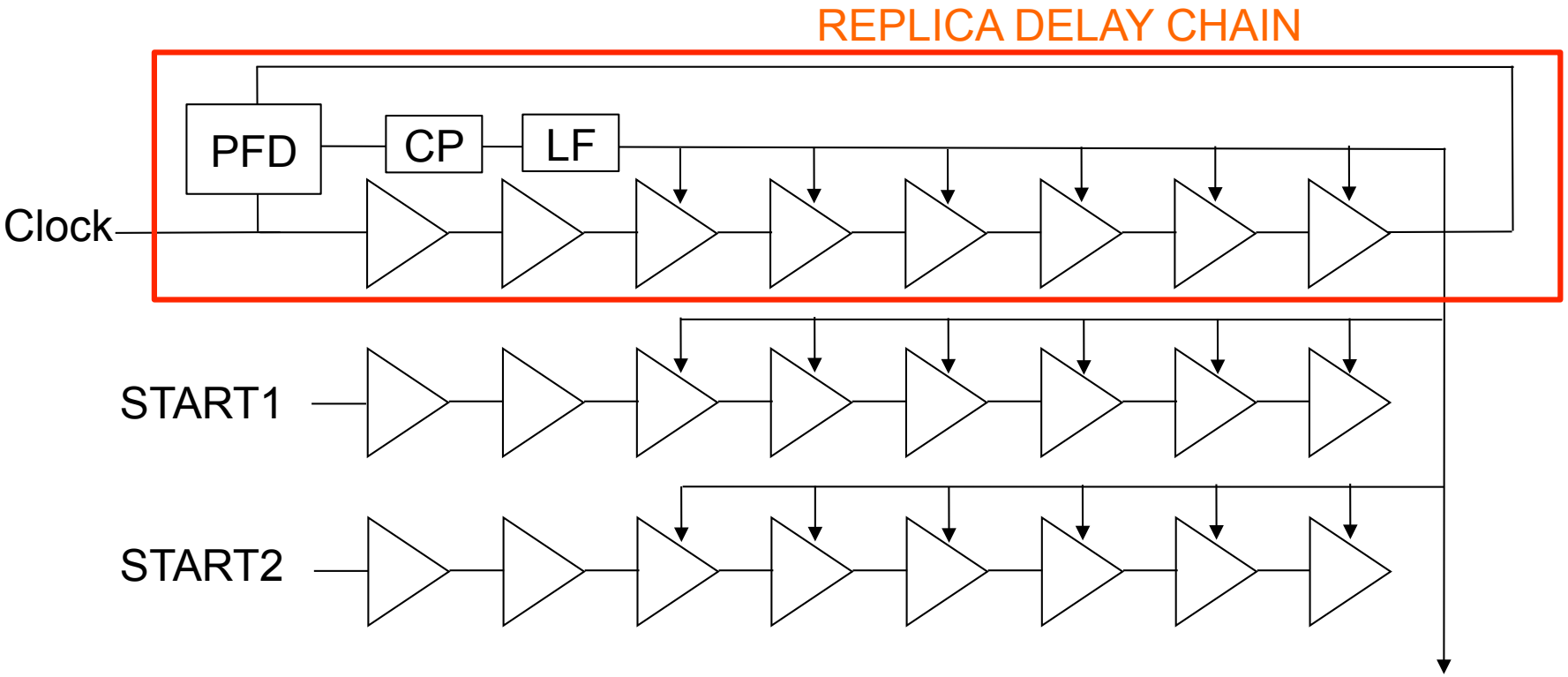
Stabilization Techniques

- Process, Voltage supply, Temperature (PVT) variations eliminated using a delay locked-loop (DLL) in clock phase generation

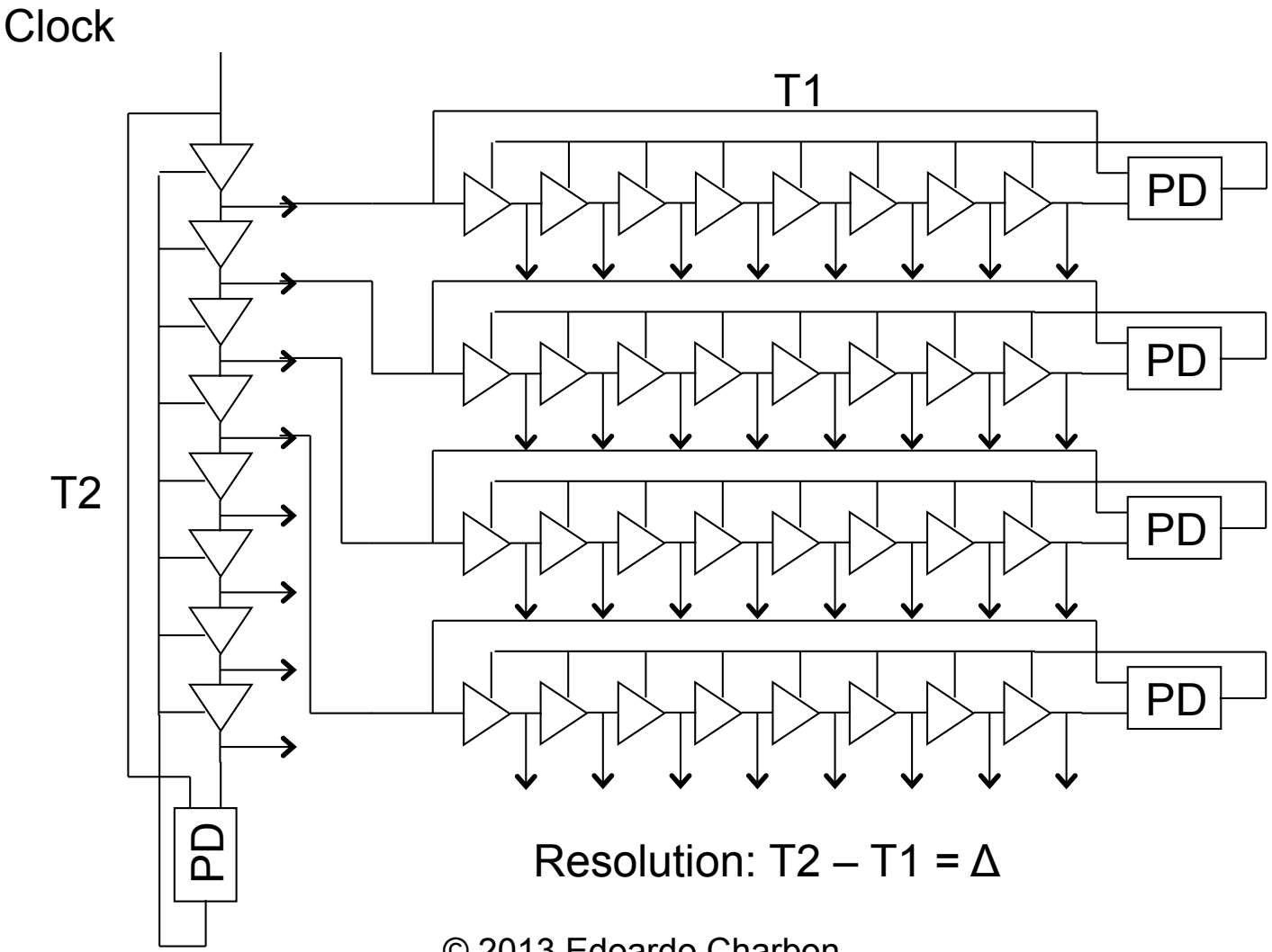


PVT Stabilization in Phase Interpolators

- DLL running in parallel as a replica of delay chain
- Distribute bias to all delay chains

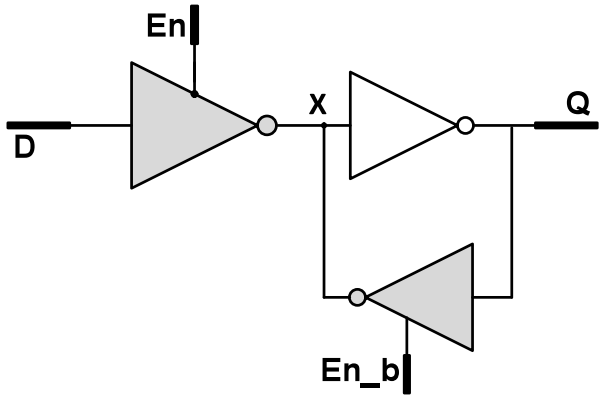


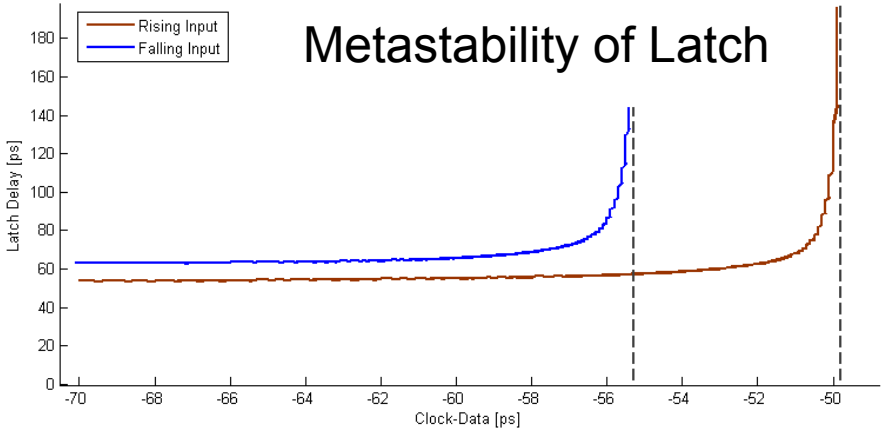
Nested Stabilization Loops

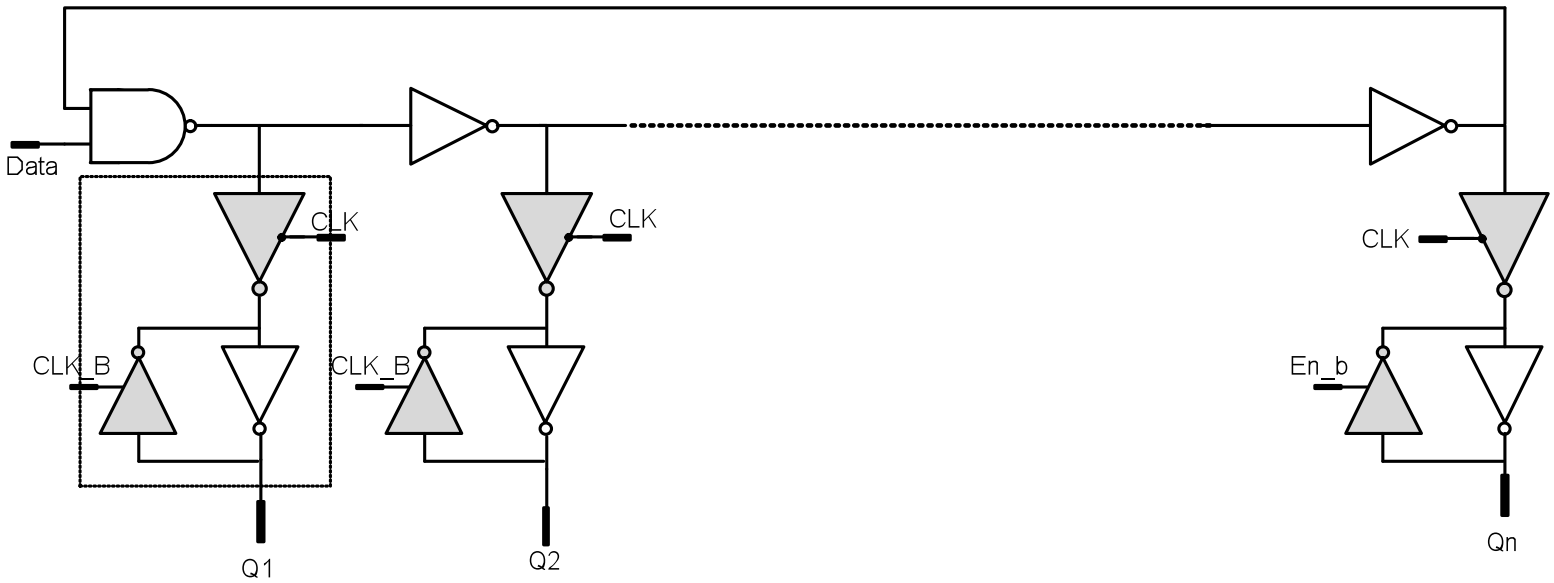


Resolution: T2 – T1 = Δ

Metastability in Ring Oscillators







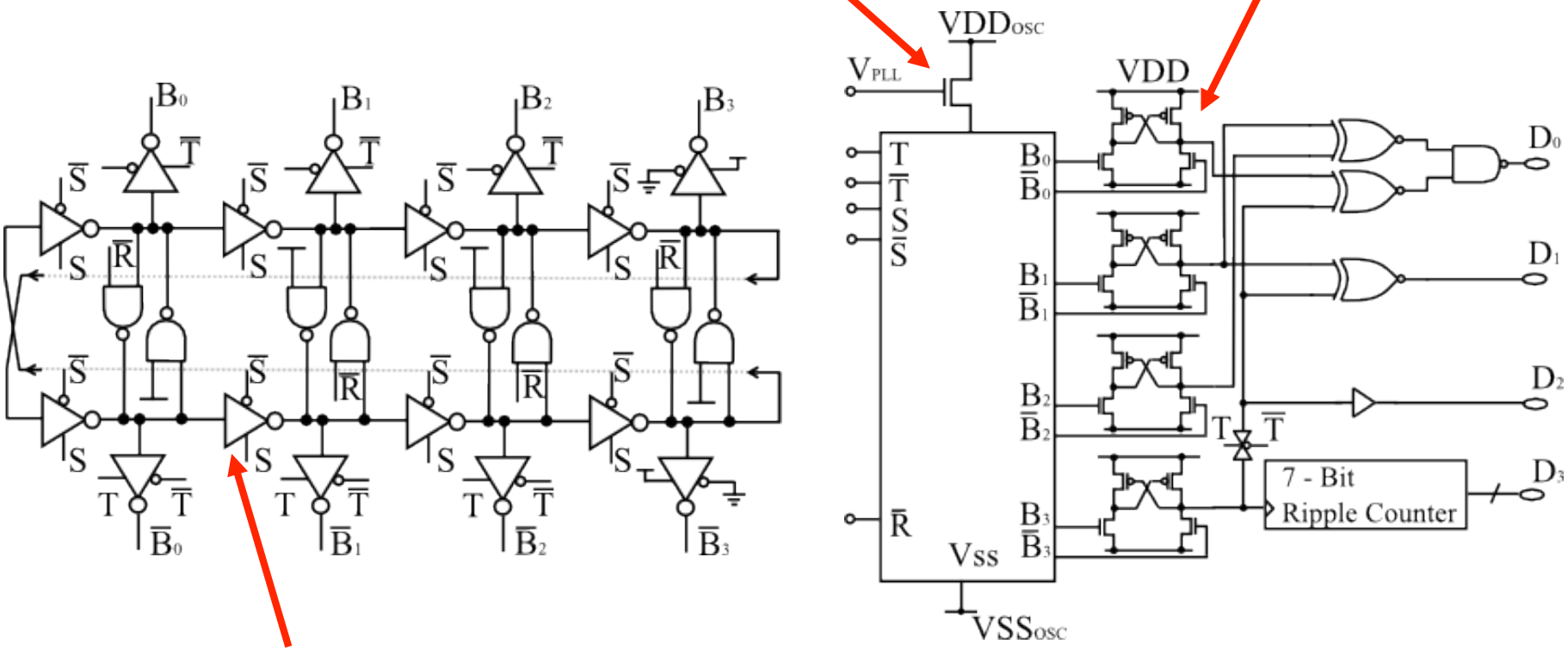
Case Study

An Array of 20,480 TDCs

- **Massive array** of pixels comprising
  - single-photon avalanche diode (SPAD)
  - TDC (ring oscillator type)
  - Memory
- Readout
  - Frame rate: 1us
  - Fully digital

TDC Implementation

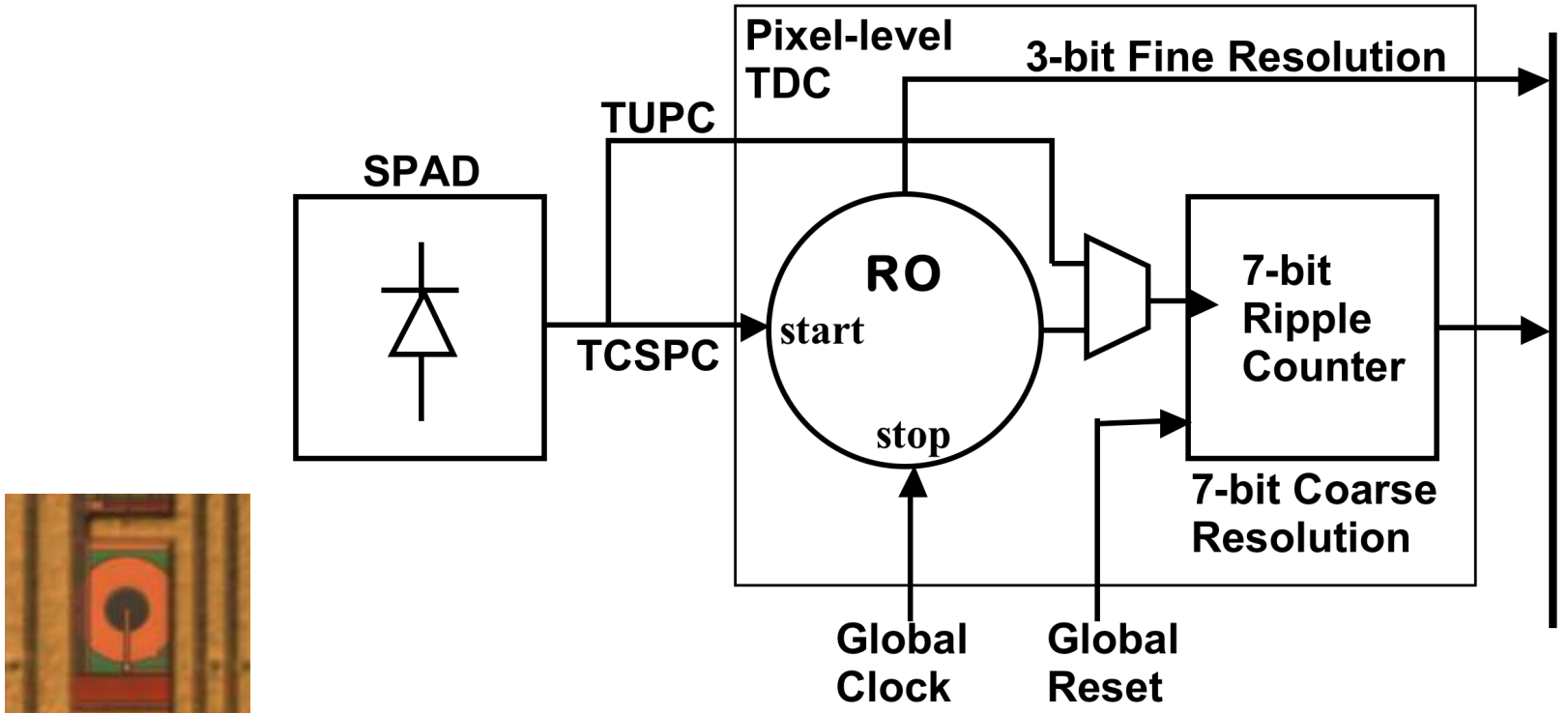
Analog techniques allow greater architecture flexibility

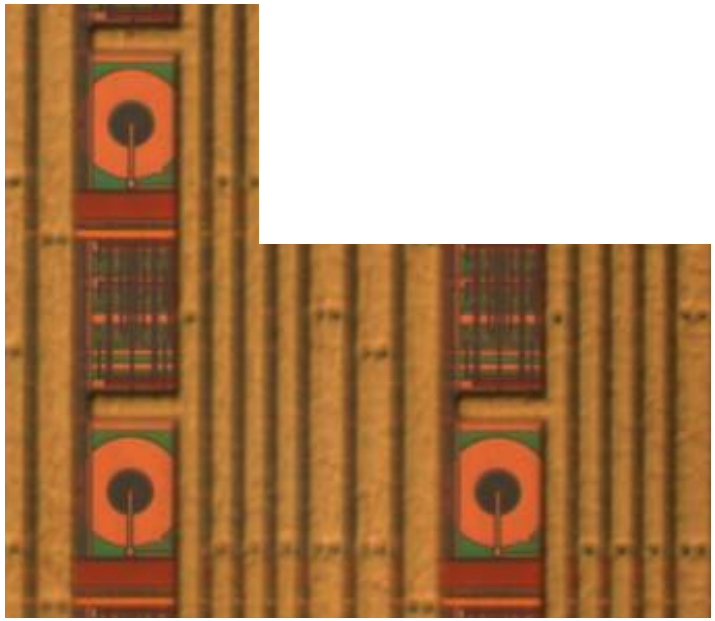


Single-gate delay means less power, faster transitions

C. Veerappan, J. Richardson, R. Walker, D.-U. Li, M. W. Fishburn, Y. Maruyama, D. Stoppa, F. Borghetti, M. Gersbach, R.K. Henderson, E. Charbon, *ISSCC2011*

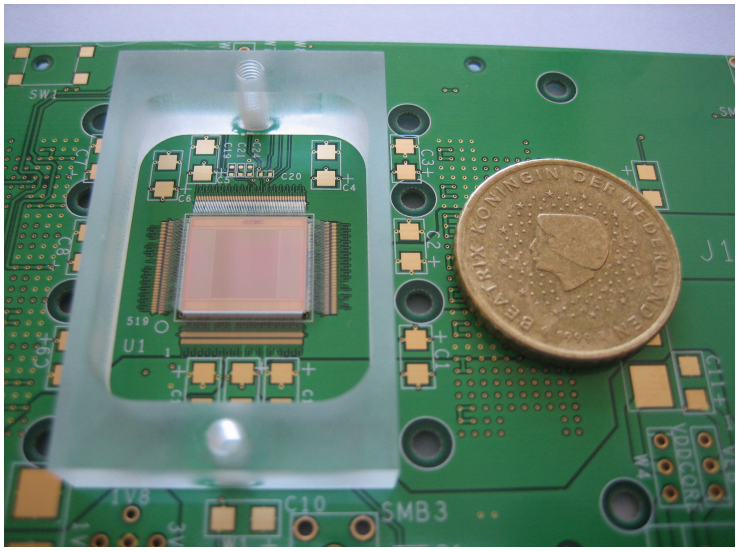
The MEGAFRAME Pixel

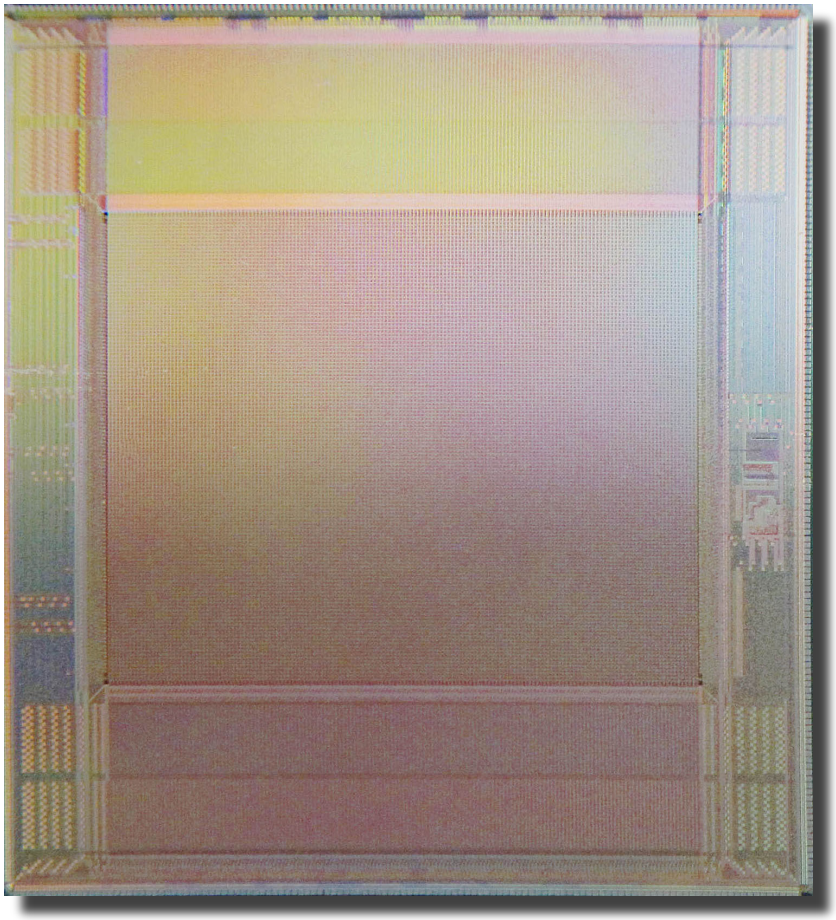




The MEGAFRAME Chip

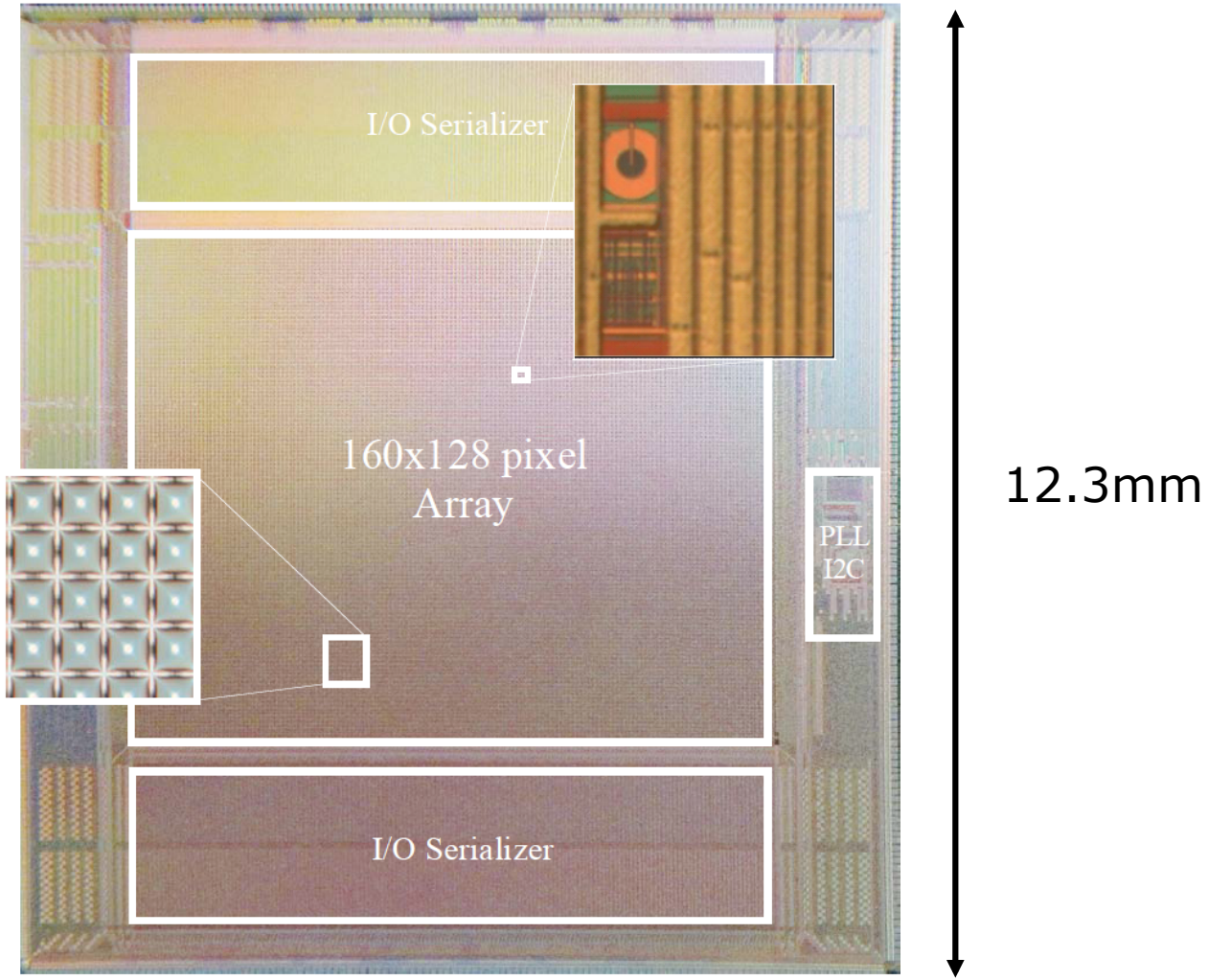
- Format: 160x128 pixels
- Timing resolution: 55ps
- Impulse resp. fun.: 140ps
- DCR (median): 50Hz
- R/O speed: 250kfps
- Size: 11.0 x 12.3 mm^2





TDC
Ring oscillator (3 bits) + counter (7 bits)
= 10 bits

The Megaframe-128 Chip



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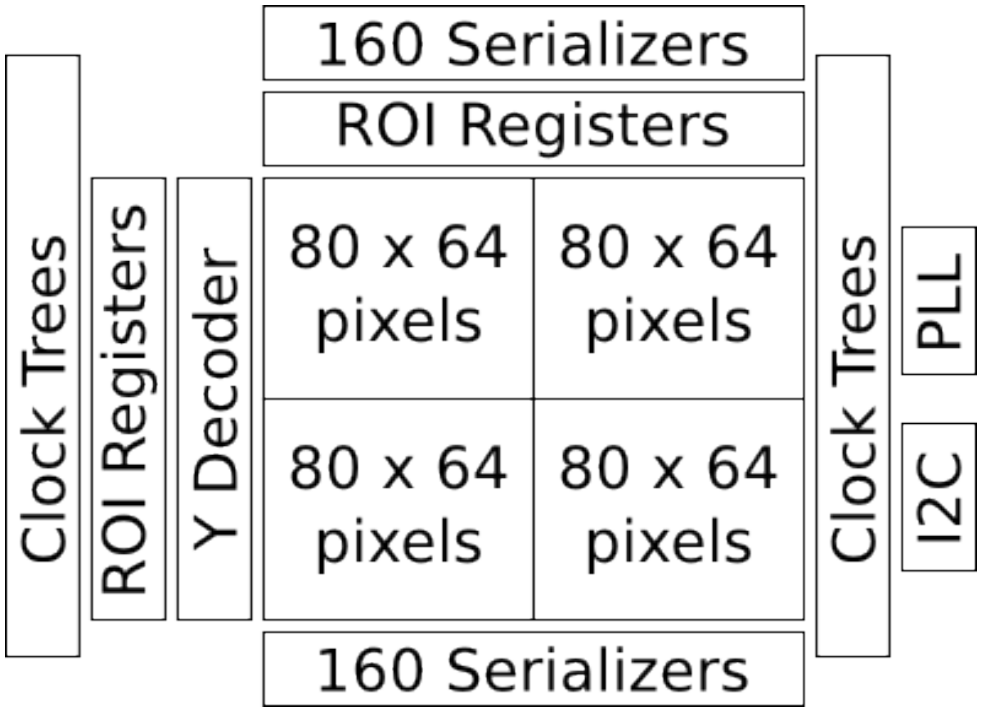
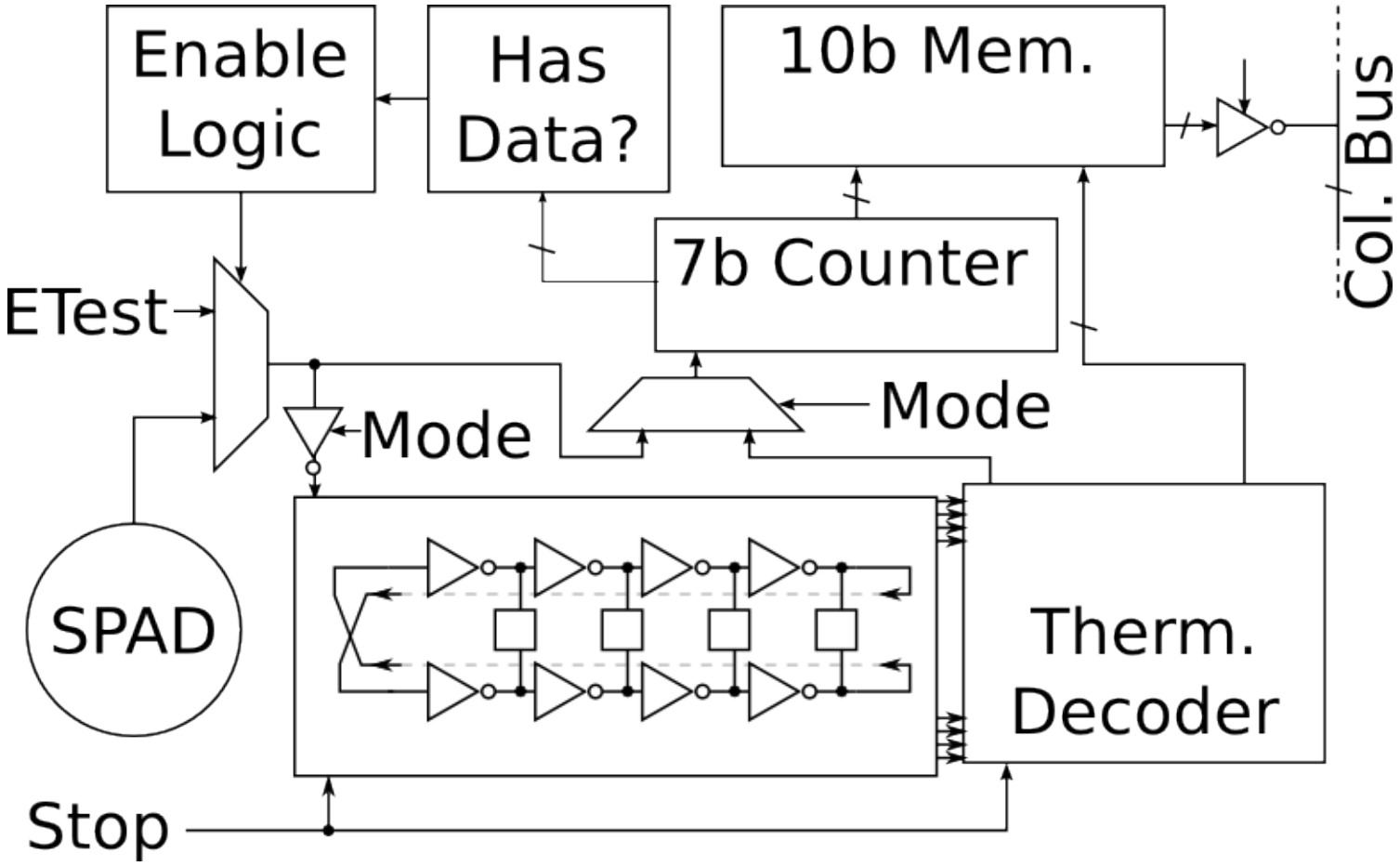
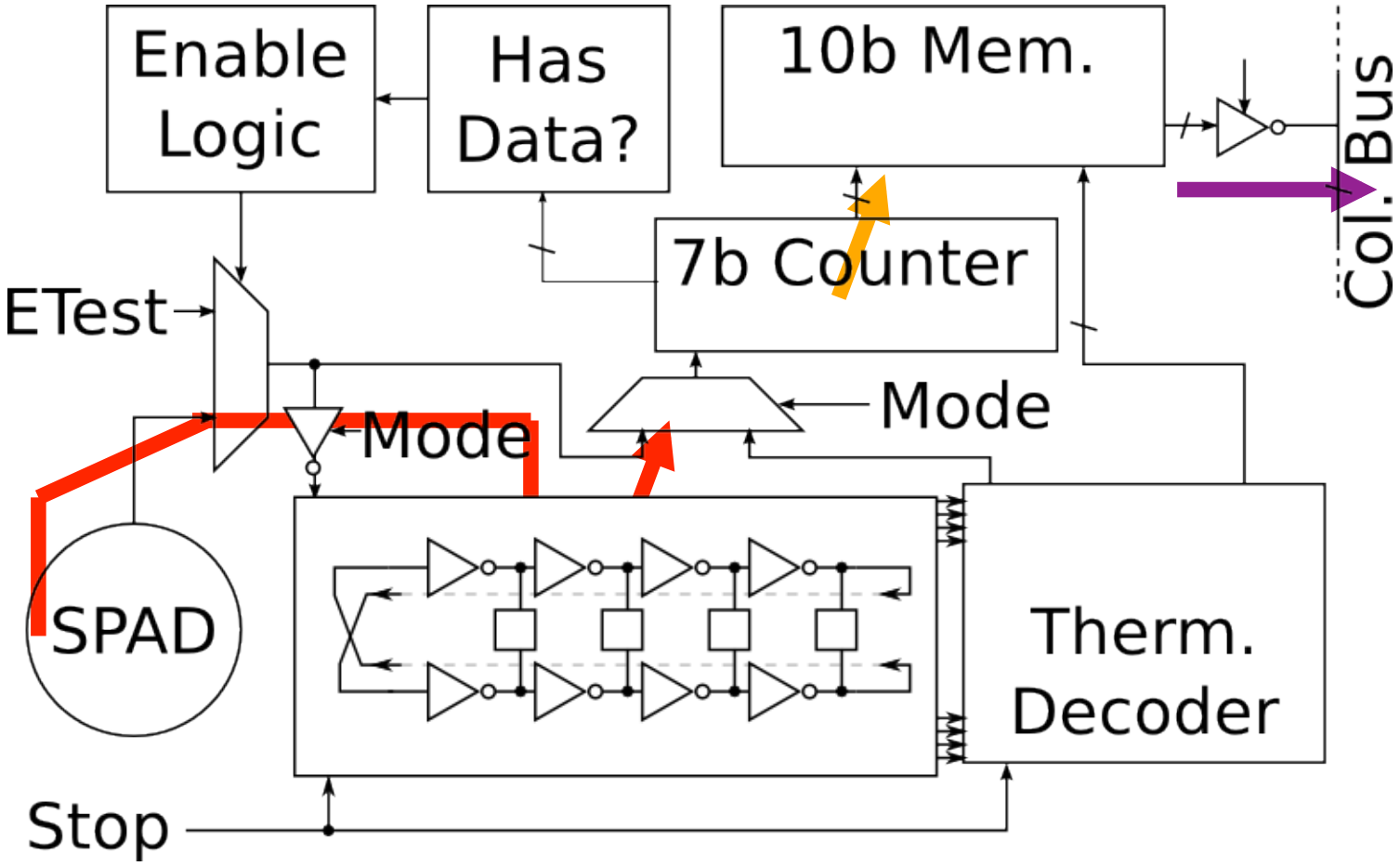
Imager Block Diagram



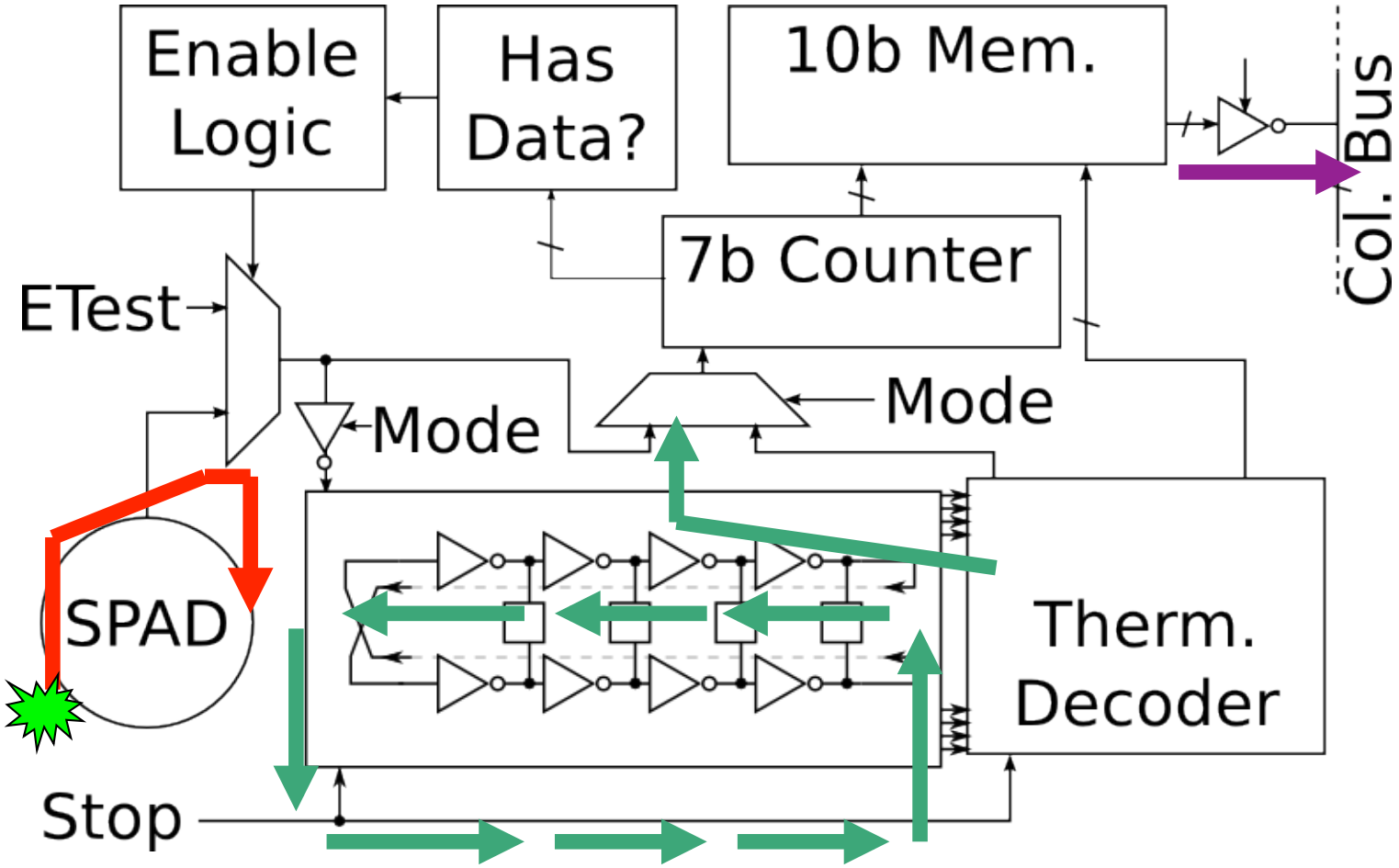
Pixel Architecture



Photon Counting

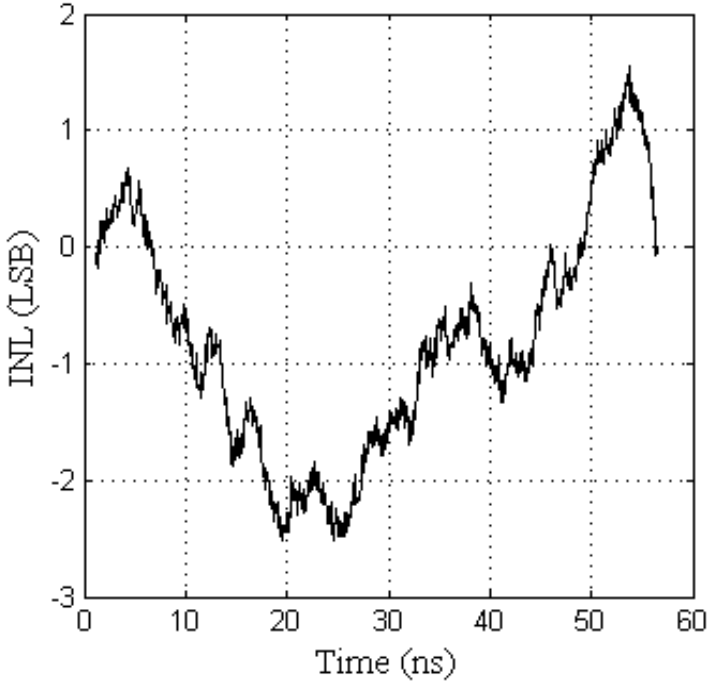


Photon Time-of-Arrival

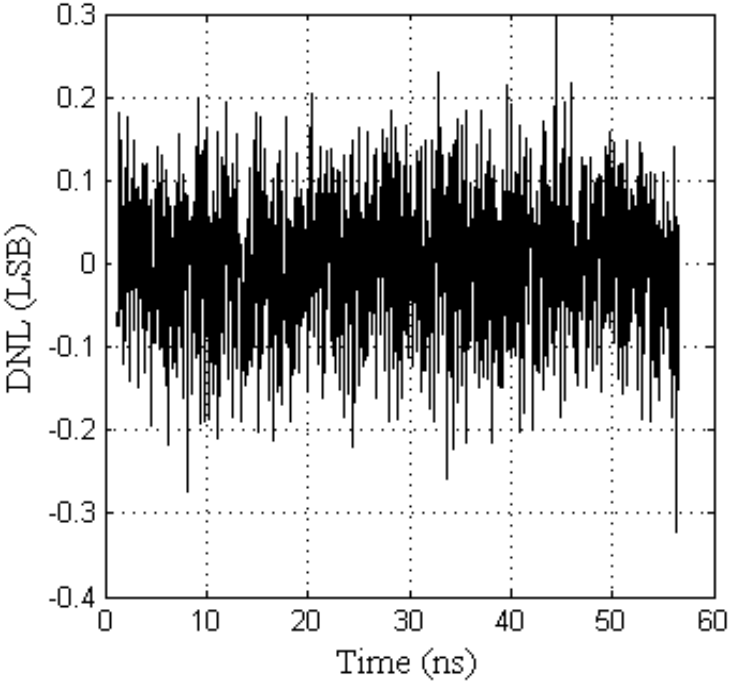


TDC Characterization

INL



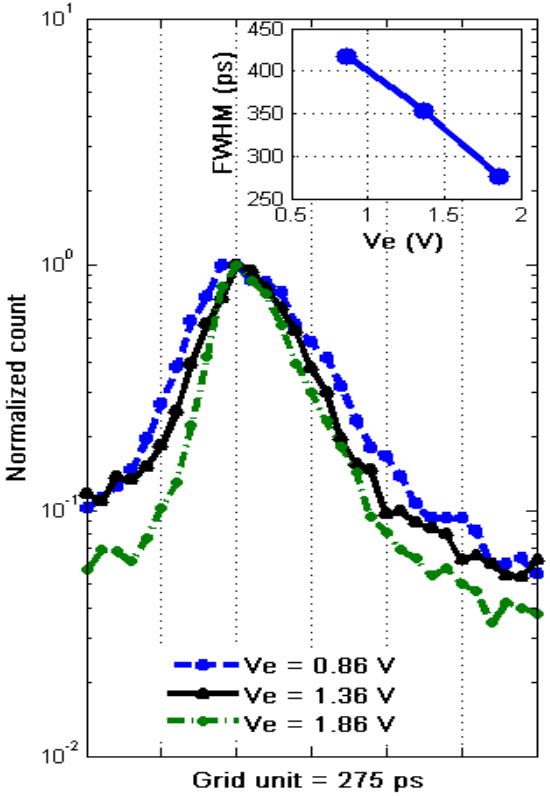
DNL



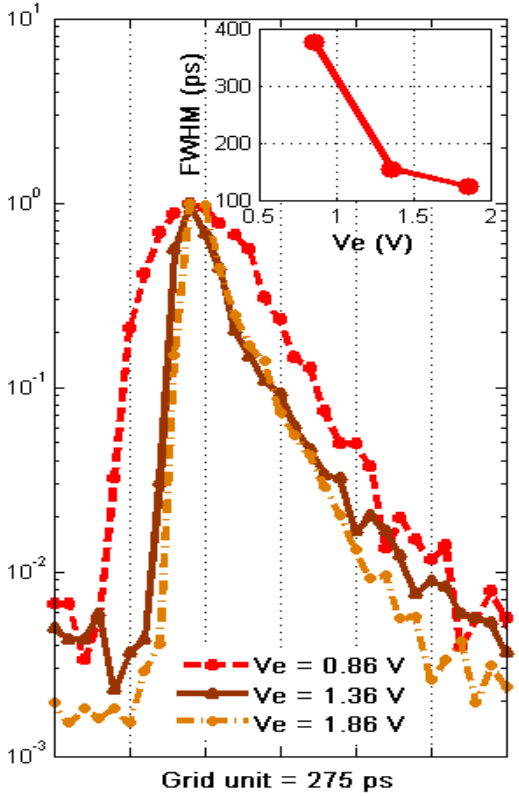
55ps resolution, 55ns range

System-level Timing

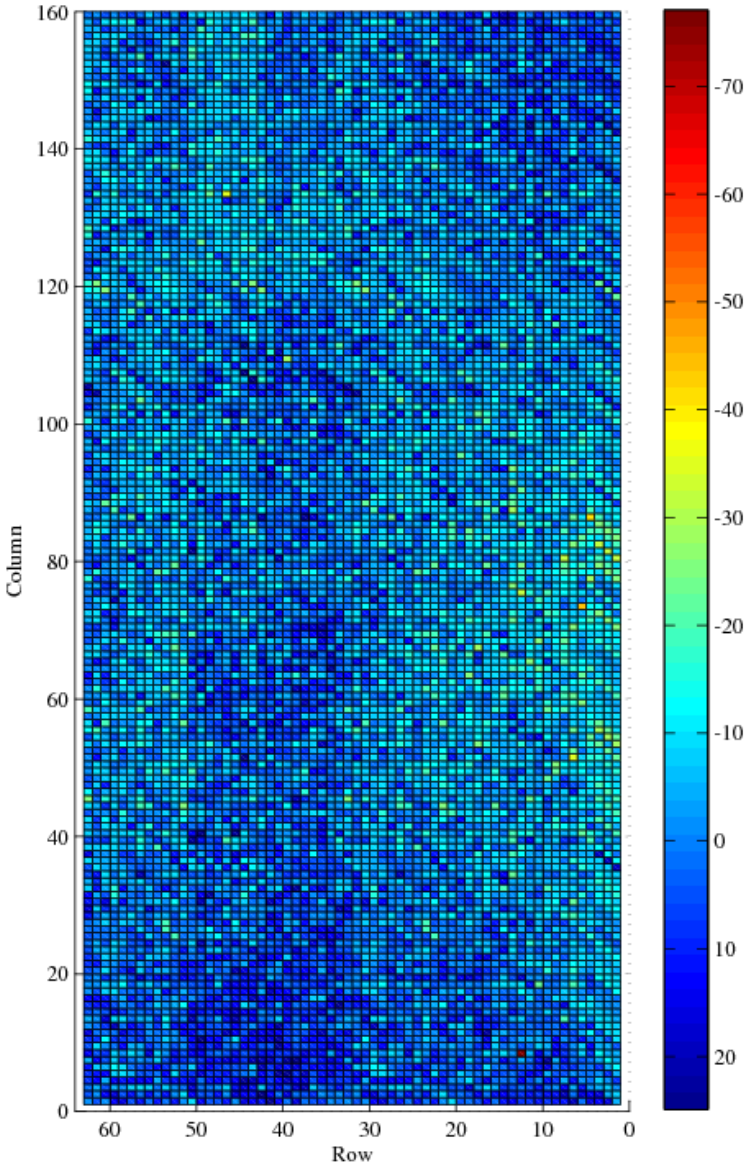
Blue laser

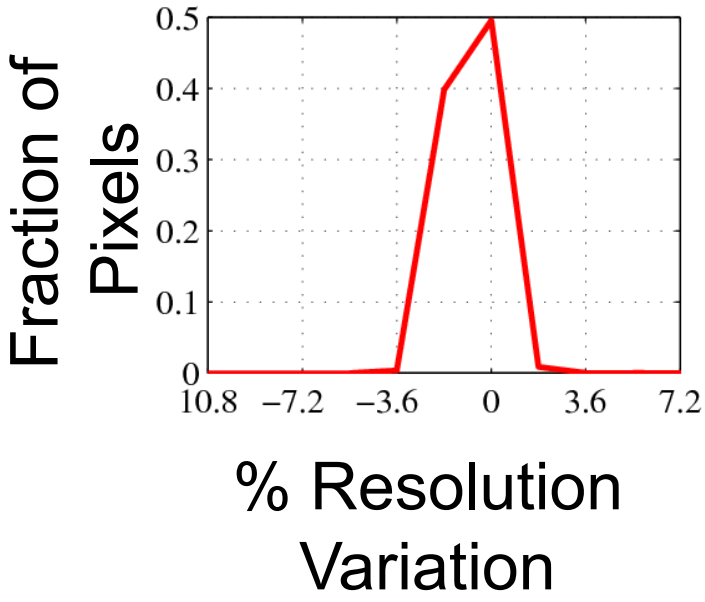


Red laser

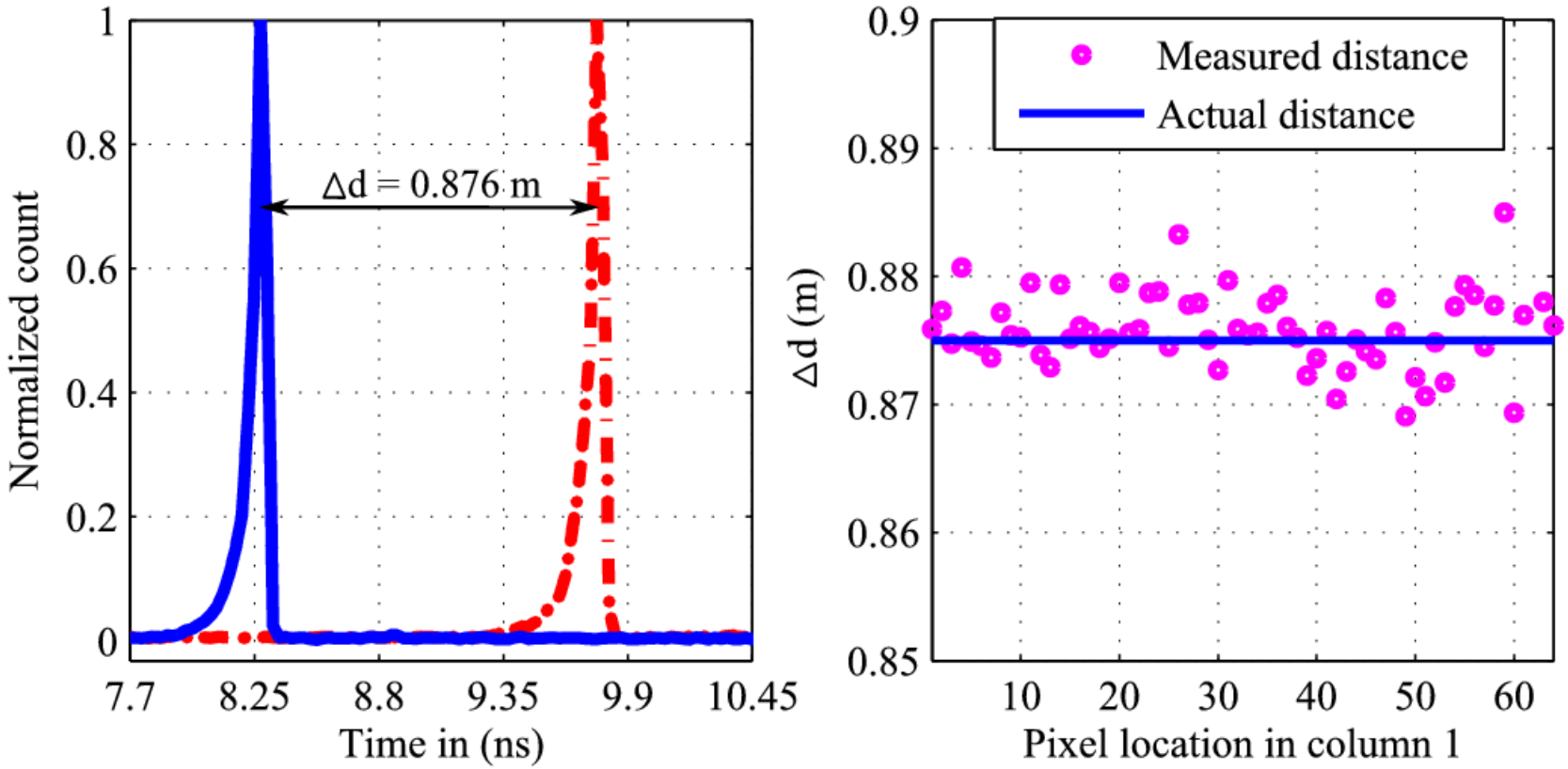


LSB Uniformity





Optical Burst Detection



Using MEGAFRAME

- Optical rangefinder on-pixel (3D camera)
- Fluorescence lifetime imaging microscopy (FLIM)
- Fluorescence Correlation Spectroscopy (FCS)
- Detection of a scintillation shower upon gamma photon detection in PET

ASIC vs. FPGA

FPGA vs. discrete ASIC

- An application-specific integrated circuit (ASIC) is a chip with static circuitry optimized for one task

- A field-programmable gate array (FPGA) is a chip whose configuration, specified by a hardware description language, can be changed many times

General Comparison

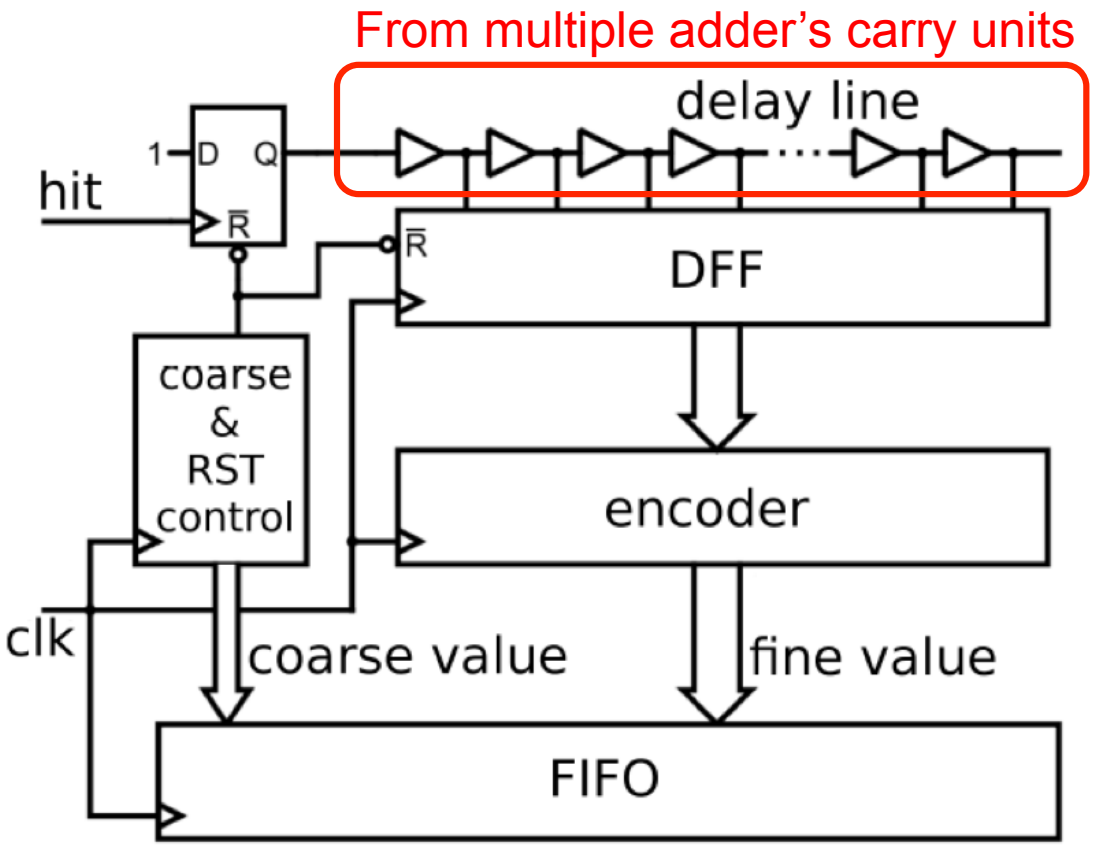
FPGA

- Fast Development Time
- Reconfigurable
  - Lower fault risk
  - Iterate design
- Low non-recurring costs
  - Development
  - Testing

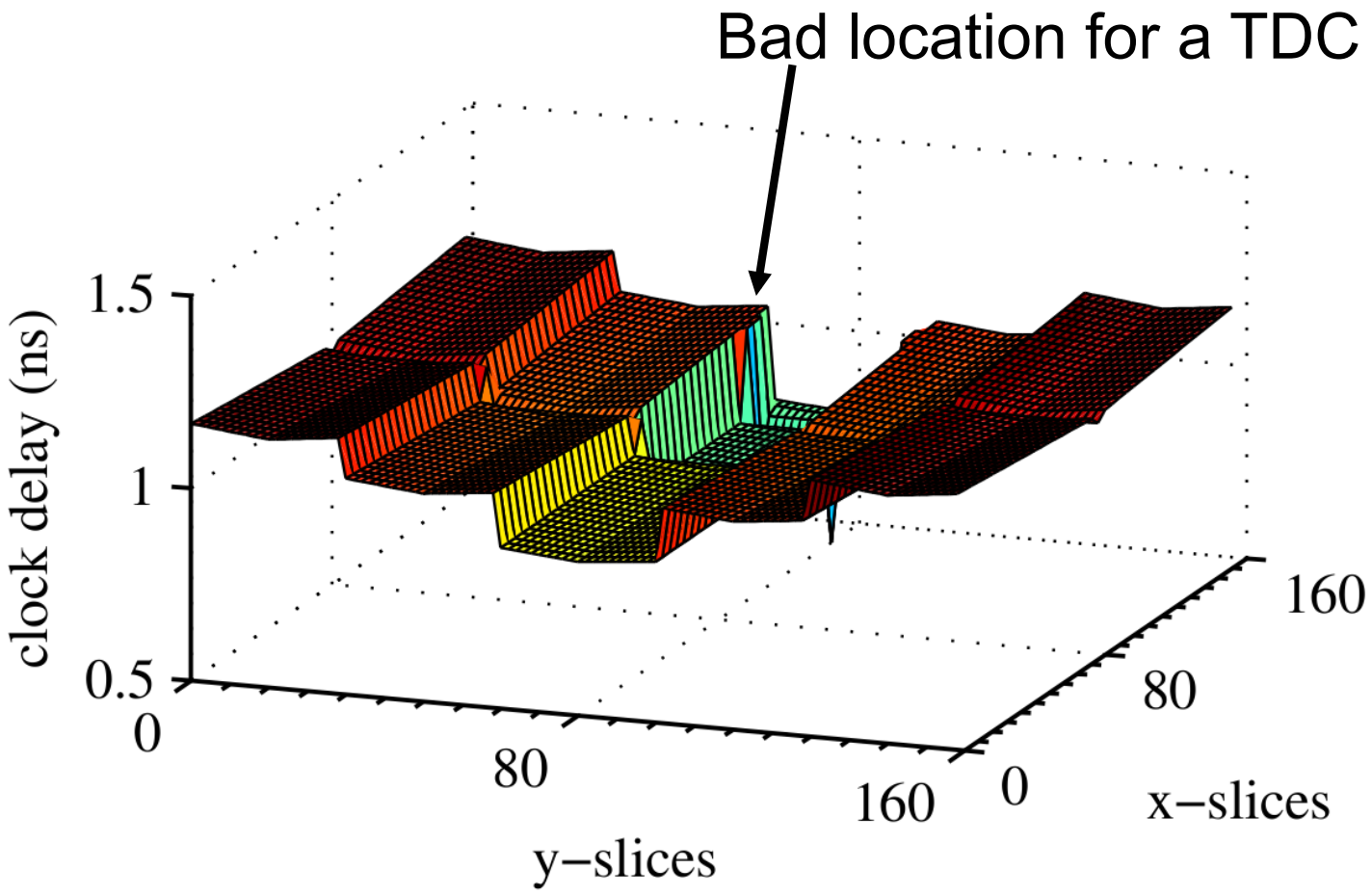
ASIC

- Lower power
- Faster operation
- Smaller footprint
- Better integration
- More flexibility
- Low unit costs
  - High-volume applications

How to Build a Delay Chain

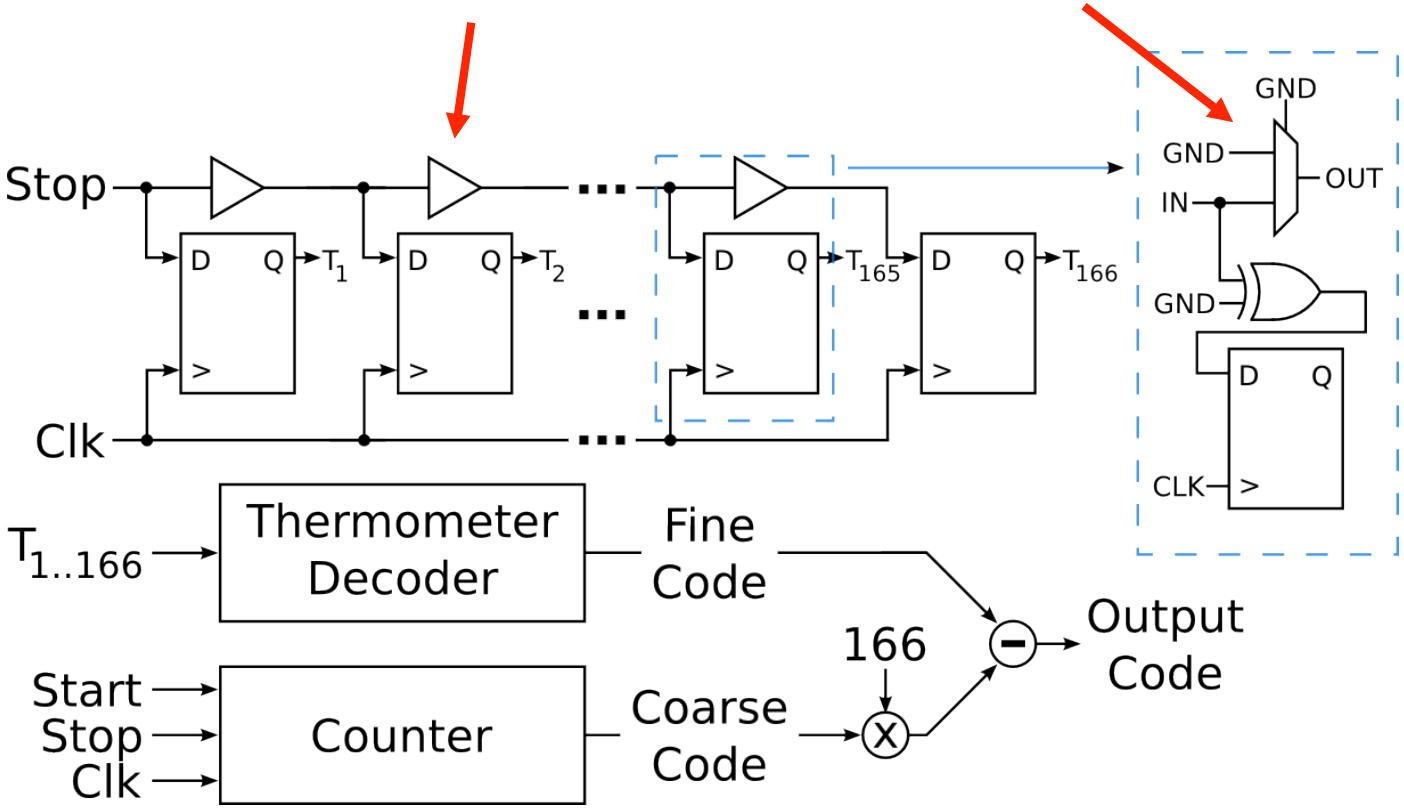


FPGA Caveats: Clock Regions



Example FPGA Architecture

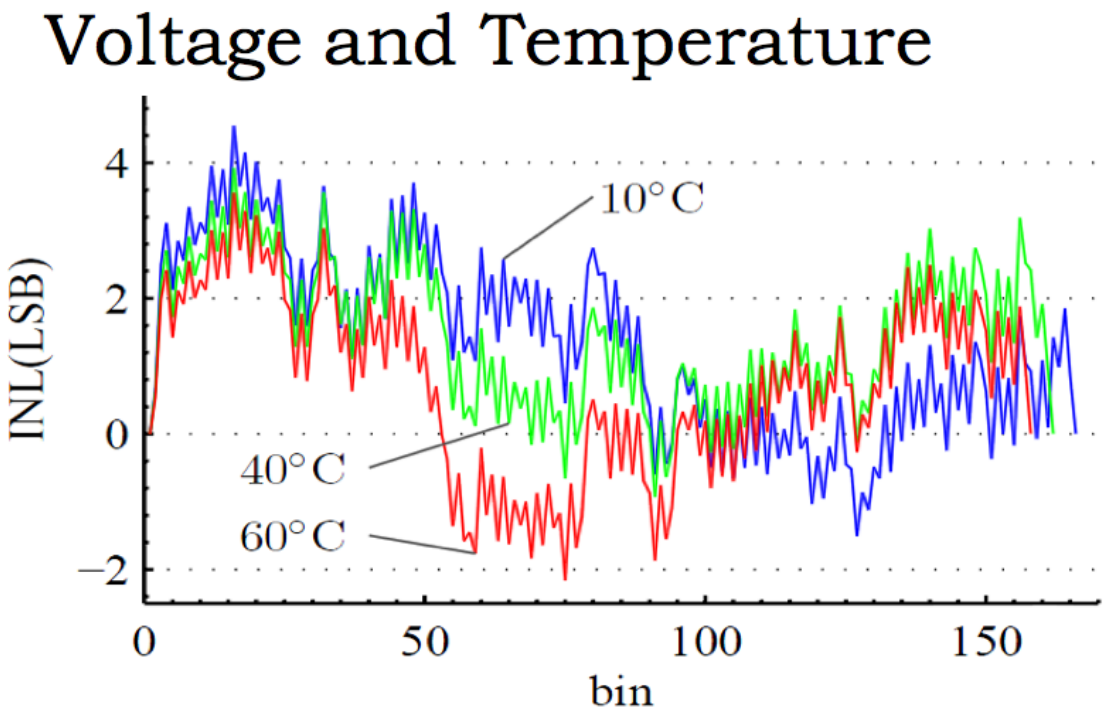
Only digital techniques available with existing cells



Virtex-6 FPGA TDC

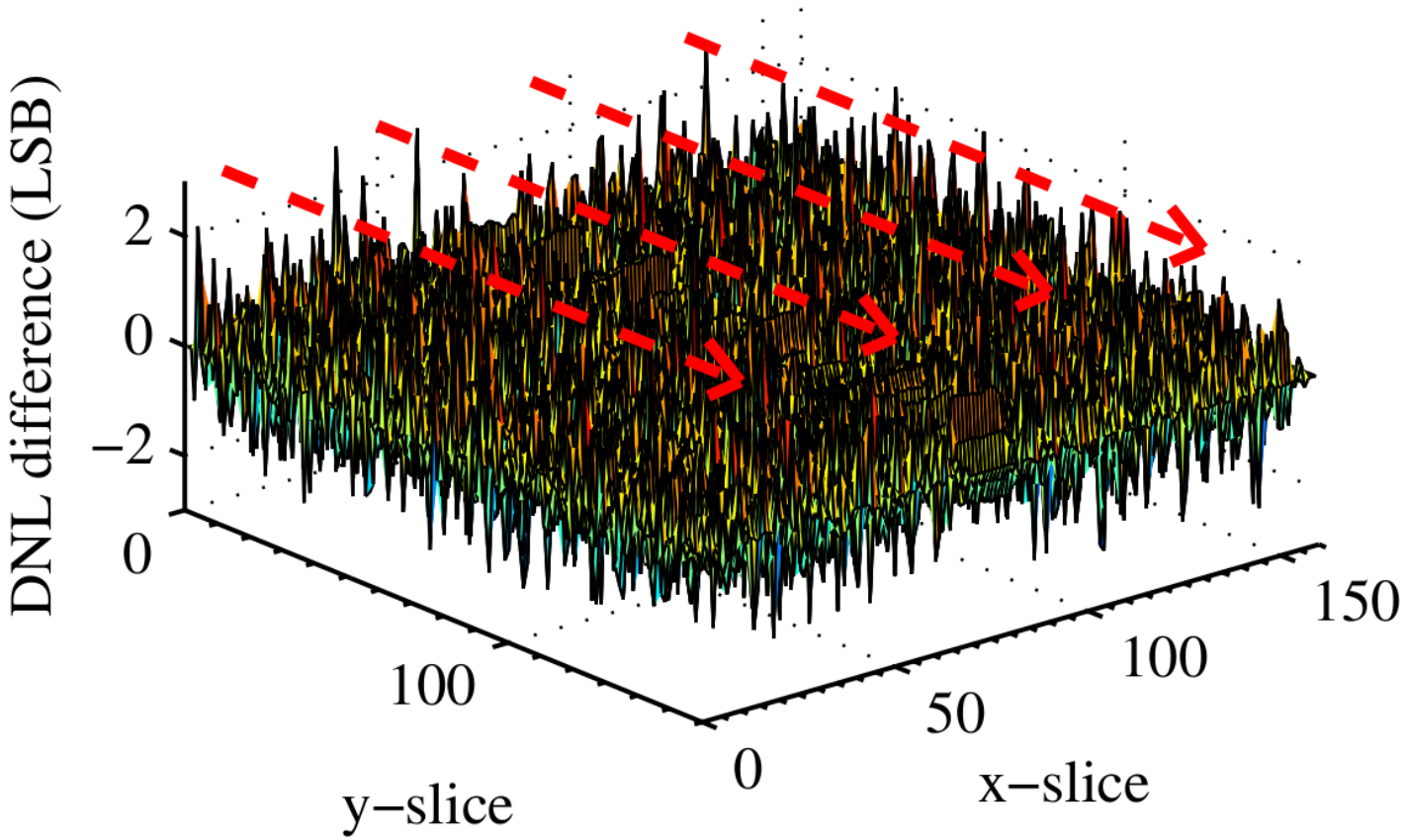
Implementation #1 (design on Virtex-6)				
	Min	Typ	Max	Unit
Clock frequency		200		MHz
Standard uncertainty	7.38		14.24	ps
Resolution		9.8		ps
DNL	-1		6.2	LSB
INL	-2.1		13.7	LSB
Throughput		100		MSample/s
Implementation #2 (improved timing)				
Clock frequency		600		MHz
Standard uncertainty	7.38		14.24	ps
Resolution		9.8		ps
DNL	-1		1.5	LSB
INL	-2.8		4.1	LSB
Throughput		300		MSample/s
Implementation #3 (improved position)				
Clock frequency		600		MHz
Standard uncertainty	7.38		14.24	ps
Resolution		9.8		ps
DNL	-1		1.5	LSB
INL	-2.25		1.61	LSB
Throughput		300		MSample/s

Temperature Dependence

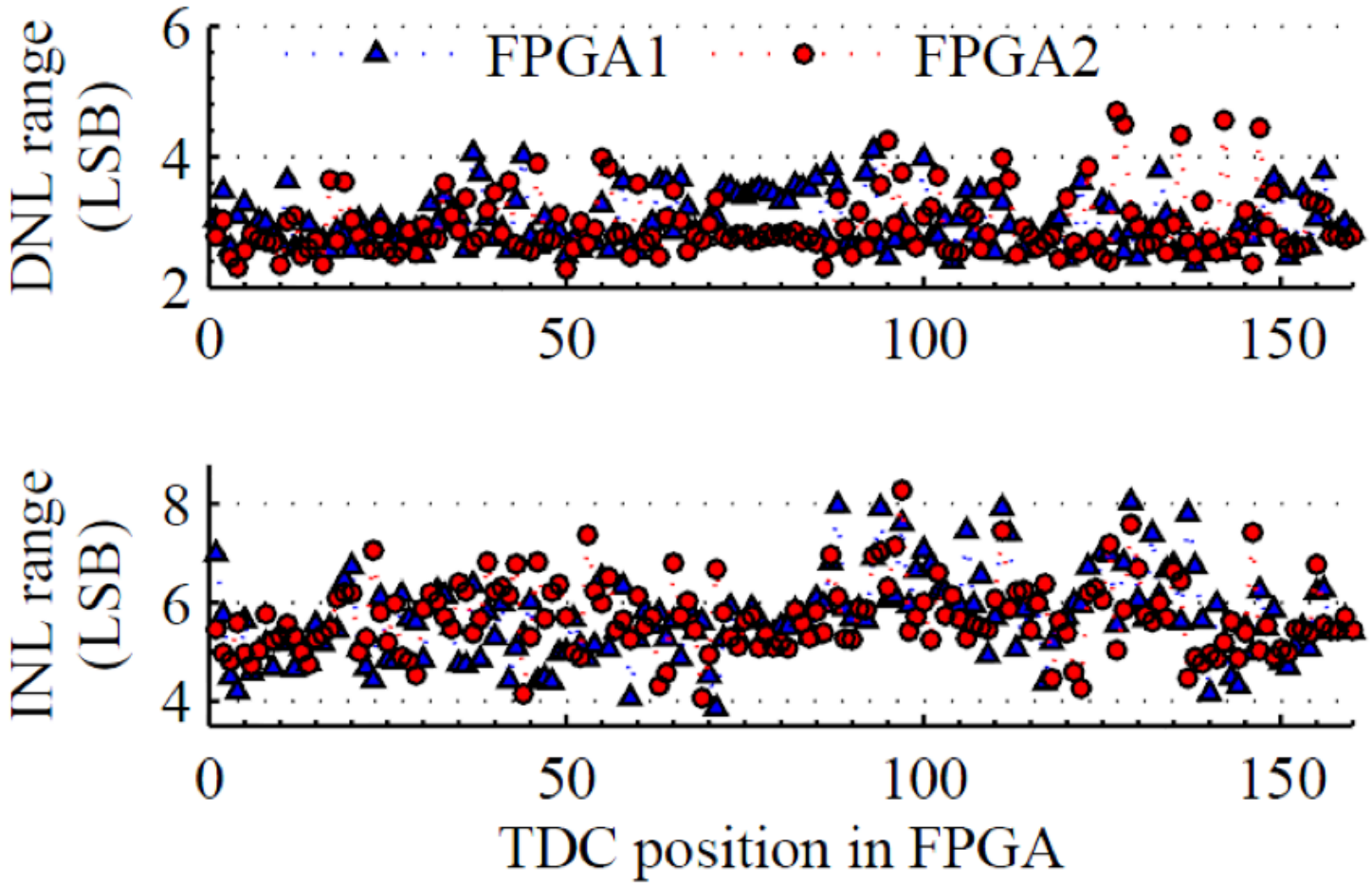


Color	Temp.	Res.(ps)	μ(V)	σ(mV)
	$10°C$	9.8	1.0096	2.9
	$40°C$	10.22	1.0034	1.9
	$60°C$	10.48	0.9993	3.2

Location, Location, Location



Chip-to-chip Variation



TDC Comparison

FPGA

- Best time uncertainty: 20ps
- Usage examples
  - High-energy physics
  - OpenPET

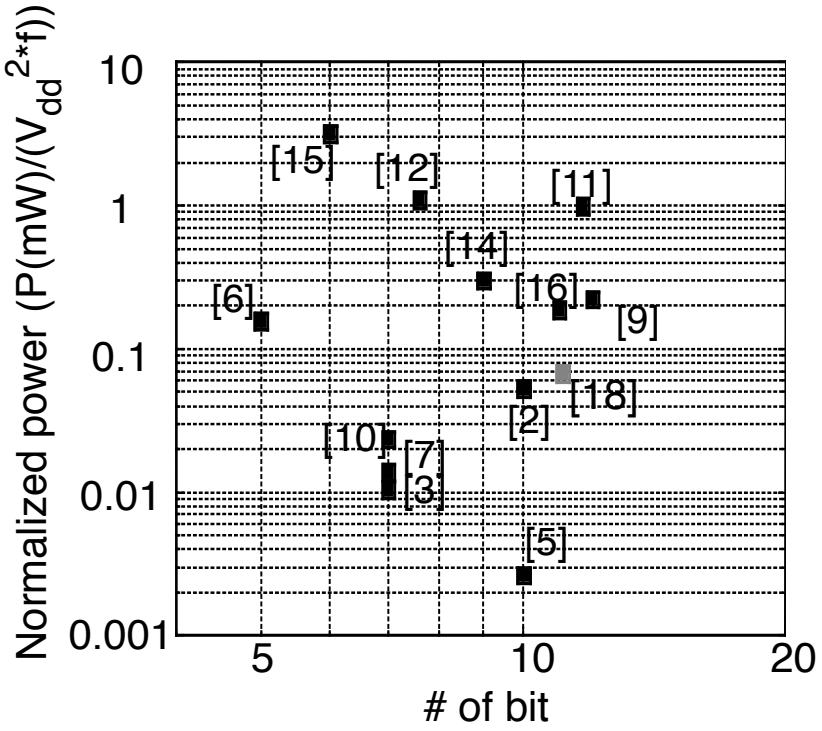
ASIC

- Best time uncertainty: <1ps
- Examples
  - Time-correlated imaging
  - Frequency synthesizers for RF

FPGA- or ASIC-based TDC?

- Consider an FPGA-based TDC if your application:
  - Is low-volume
  - Doesn’t require <20ps time uncertainty
  - Is sensitive to development time, or is being created in iterations
  - Is open source (FPGA-based TDCs are code-based)

State-of-the-art



Conclusions

- TDCs have experienced significant growth for many applications from microscopy to 3D vision, from ADPLLs to spectroscopy
- ASICs vs. FPGAs: problems and solutions are different
- Case study showed some trade-offs
- Perspectives show there is more to come

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Perspectives

How To Compare and Choose

- Use in final system
  - Can one actually use effectively very high time resolution in large systems (detectors)
  - Calibration - stability
  - Distribution of timing reference (start signal or reference clock)
  - Other features: data buffering, triggering, readout, test, radiation, etc.
- Merits

Merits (Jorgen Christiansen)

- Resolution
  - Bin size
  - Effective resolution (RMS, INL, DNL)
- Dynamic range
- Stability
  - Use of external reference
  - Drift (e.g. temperature)
  - Jitter
  - Noise
- Integration issues:
  - Digital/analog
  - Noise / power supply sensitivity
  - Sensitivity to matching of active elements
  - Required IC area
  - Common timing block/ per channel
  - Interference of noisy digital circuits