AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Part I: ADC fundamentals
Part II: SAR ADCdesign and tests

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Part I: ADC fundamentals

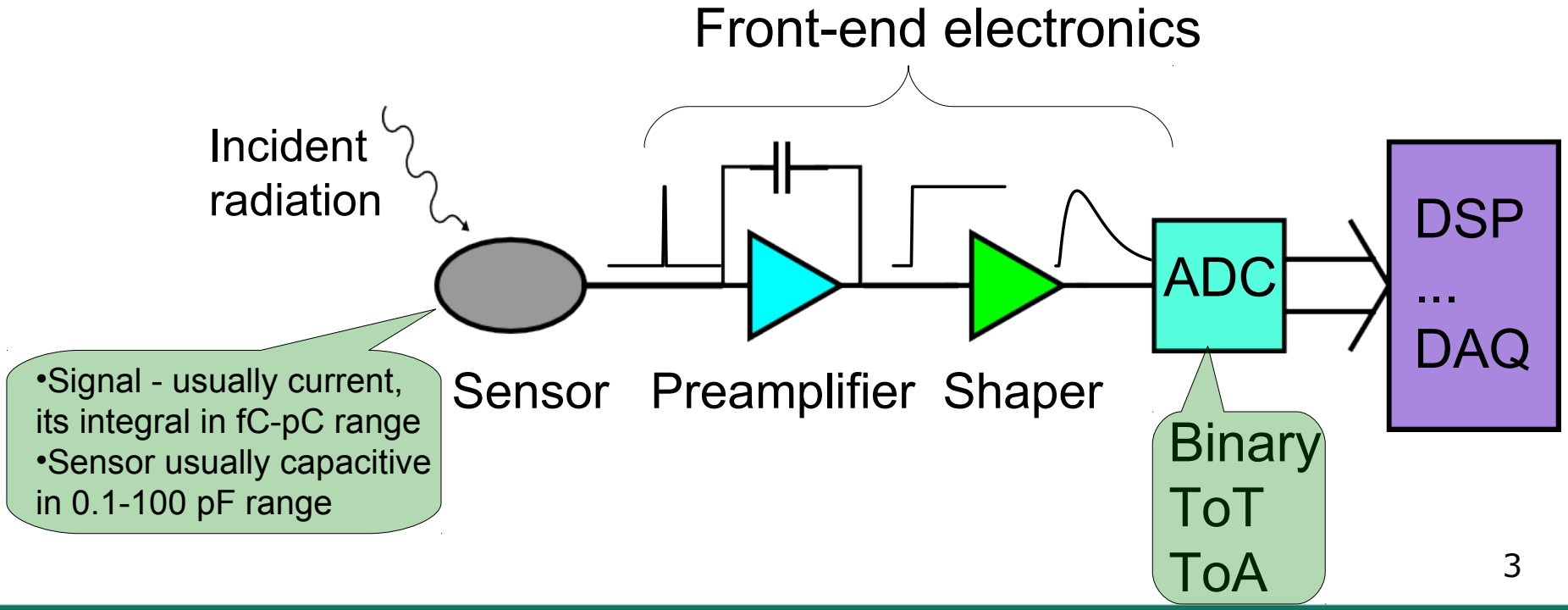
- Introduction
- ADC fundamentals of operation
- ADC errors
- ADC testing
- ADC architectures
- ADC State of Art
- Examples of multichannel ADC in HEP and commercial

➢ Many references to source articles are given throughout the presentation

Introduction
Readout electronics in HEP experiments

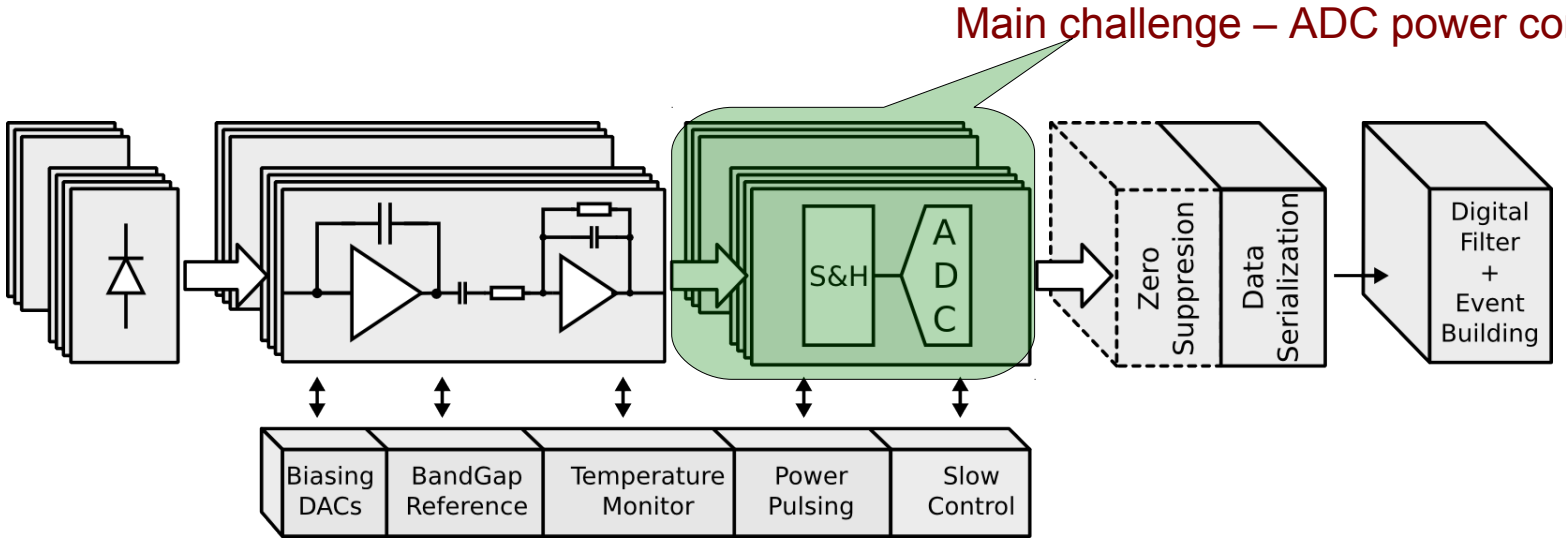
Readout electronics processes signals from sensors to measure:

- energy released by radiation ► amplitude measurements
- time of signal occurrence ► timing measurements
- position where the radiation hits the sensor ► tracking, imaging



Introduction
Motivation for low power ADC design

In older detector readout systems analog signals were sent out from the front-end ASIC and conversion was done externally by commercial ADC. This was because ADC power consumption was too high to place ADC in each readout channel. Of course the system performance was limited.



Multichannel readout system(ASIC) with efficient(DIGITAL) signal processing needs fast low-power ADC in each channel

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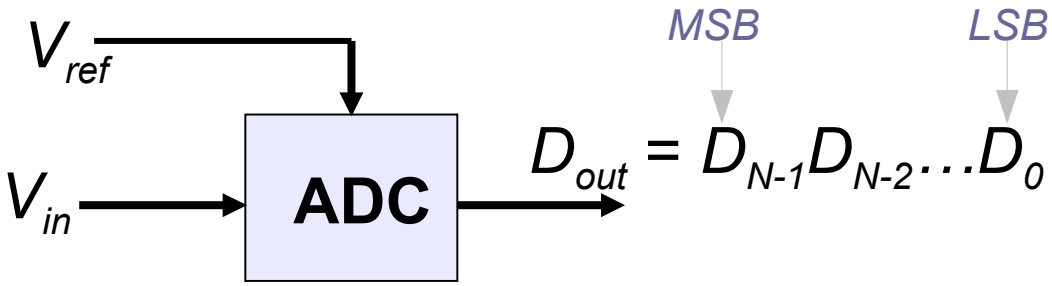
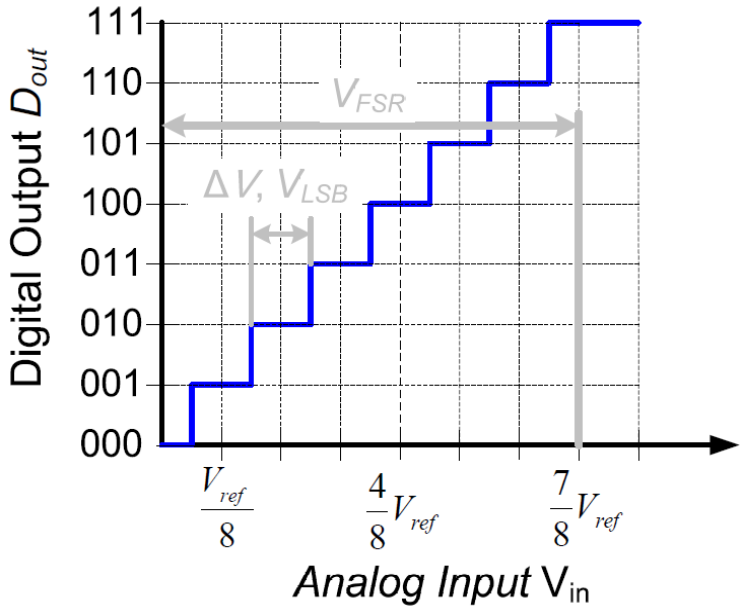
ADC fundamentals



- **Resolution N:** number of bits used to represent in discrete way an analog signal
  - 6 Bit = 2^6 = 64 quantization levels,
  - 10 Bit = 2^{10} = 1024 quantization levels
- **Reference voltage V_{ref}:** Sets the input range. Analog input signal V_{in} is related to digital output signal D_{out} through V_{ref} with:

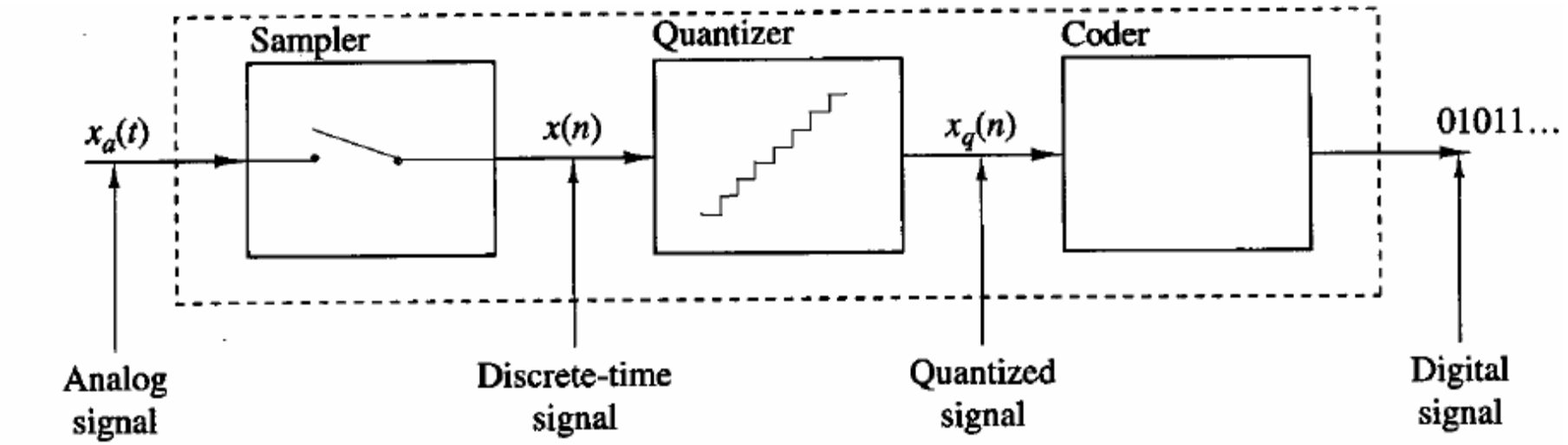
$$V_{in} = V_{ref} \cdot (D_{N-1}2^{-1} + D_{N-2}2^{-2} + \ldots + D_0 2^{-N})$$

  - Example: N = 3 Bit, V_{ref} = 1V, D_{out} = '011'
    => V_{in} = 1V · (2^{-2}+2^{-3})=1V · (0.25+0.125)=0.375V



ADC blocks&operations

- Sampler – samples the analog signal at discrete time intervals
- Quantizer approximates the sampled analog voltage to one of 2^N discrete levels
- Encoder – encodes the measurement in a convenient format



ADC operation fundamentals
Time discretization

Shannon Sampling Theorem: The sampling frequency should be at least twice the maximum frequency of the signal. If a continuous-time signal contains no frequencies higher than:

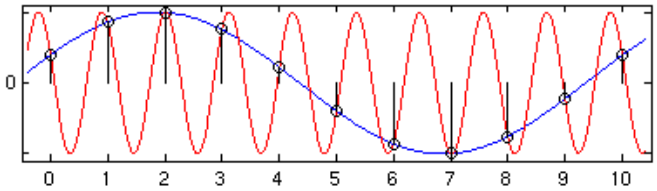
$$f_{max} < f_{sample} / 2 \qquad (f_{sample}/2: \text{Nyquist frequency})$$

,it can be completely determined by collected discrete samples.

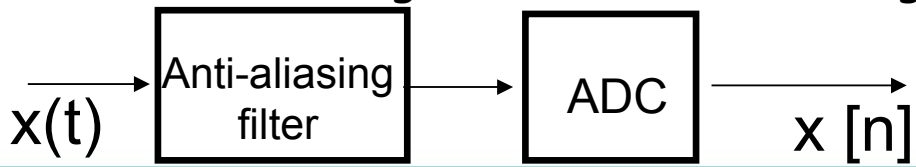
Example: Humans hear audio signals 20 Hz – 20 Khz. Audio CDs sample at 44.1 KHz

Aliasing: spurious low frequencies introduced by low sampling.

- Signals beyond $f_{sample}/2$ are aliased to below $f_{sample}/2$



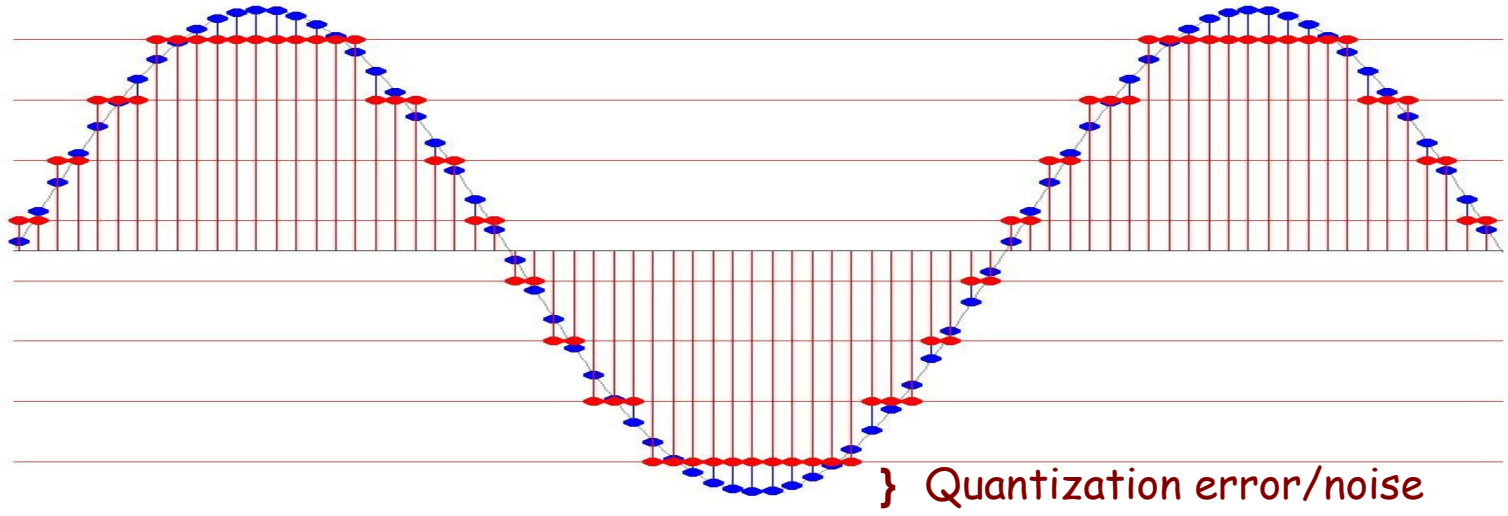
- Use anti-aliasing filter to avoid aliasing effects



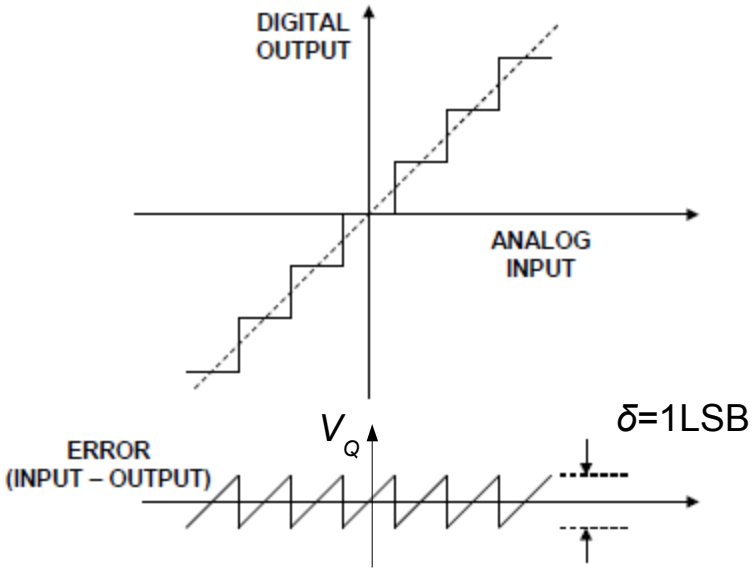
ADC operation fundamentals
Amplitude discretization

- 1 bit → 2 possible values (comparator in binary systems)
- 8 bits → 256 possible values
- 10 bits → 1024 possible values

  : :
- N bits → 2^N possible values



Amplitude discretization for ideal ADC
Quantization error/noise



For N-bit converter $\delta = V_{FSR}/2^N$

- Noise energy:

$$V_{Q(RMS)} = \sqrt{\frac{1}{\delta}\int_{-\delta/2}^{\delta/2} V_Q^2 dV_Q} = \sqrt{\frac{\delta^2}{12}}$$

- Signal energy:

$$V_{in(RMS)} = \frac{\delta \cdot 2^N}{2\sqrt{2}}$$

- SNR for ideal ADC:

$$SNR = 20\log\left(\frac{V_{in(RMS)}}{V_{Q(RMS)}}\right)$$

$$SNR = 20\log\left(2^N \cdot \sqrt{\frac{3}{2}}\right)$$

$$SNR = 6.02 \times N + 1.76[dB]$$

or

$$N = \frac{SNR[dB] - 1.76}{6.02}$$

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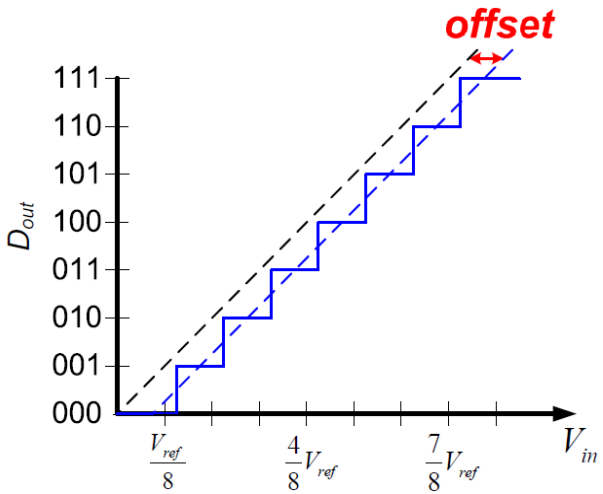
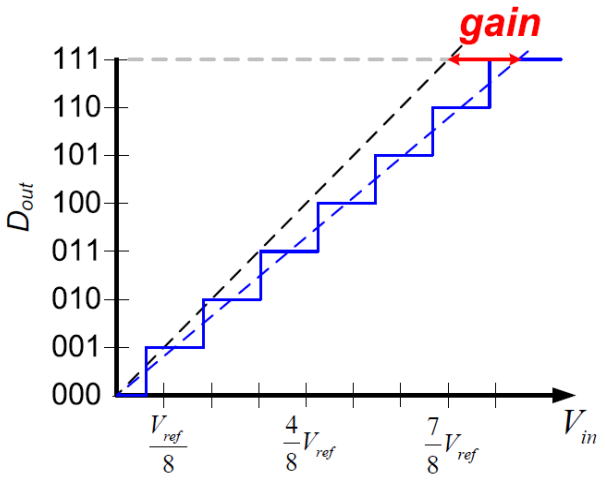
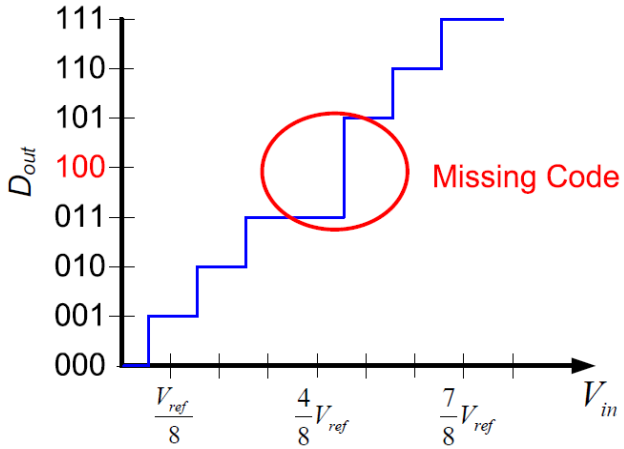
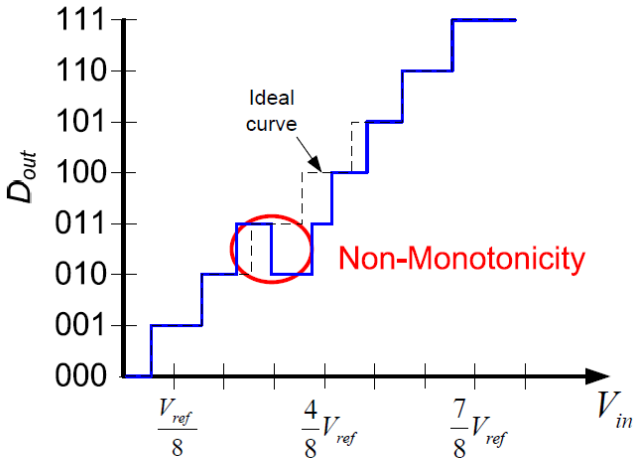
ADC errors

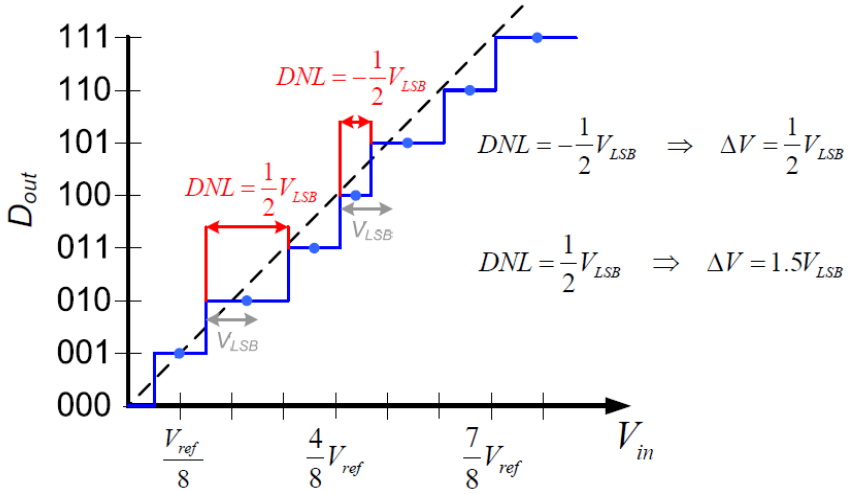

offset
111
110
101
100
011
010
001
000
D_{out}
$\frac{V_{ref}}{8}$
$\frac{4}{8}V_{ref}$
$\frac{7}{8}V_{ref}$
V_{in}

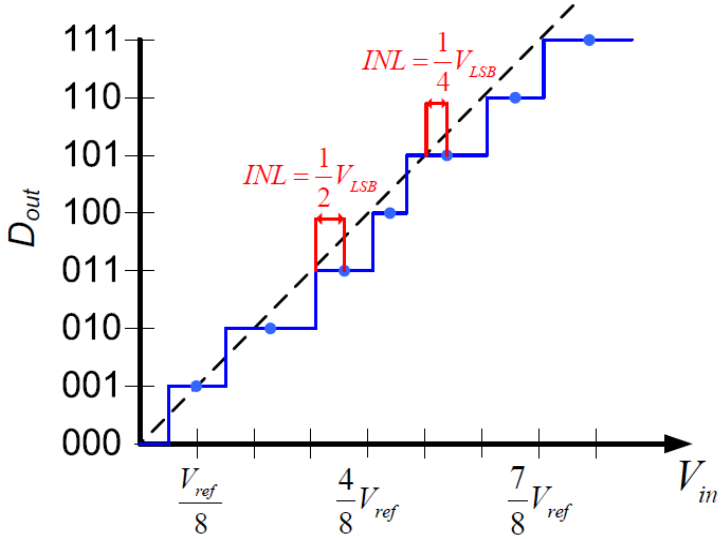

gain
111
110
101
100
011
010
001
000
D_{out}
$\frac{V_{ref}}{8}$
$\frac{4}{8}V_{ref}$
$\frac{7}{8}V_{ref}$
V_{in}


111
110
101
100
011
010
001
000
D_{out}
Missing Code
$\frac{V_{ref}}{8}$
$\frac{4}{8}V_{ref}$
$\frac{7}{8}V_{ref}$
V_{in}


111
110
101
100
011
010
001
000
D_{out}
Ideal
curve
Non-Monotonicity
$\frac{V_{ref}}{8}$
$\frac{4}{8}V_{ref}$
$\frac{7}{8}V_{ref}$
V_{in}

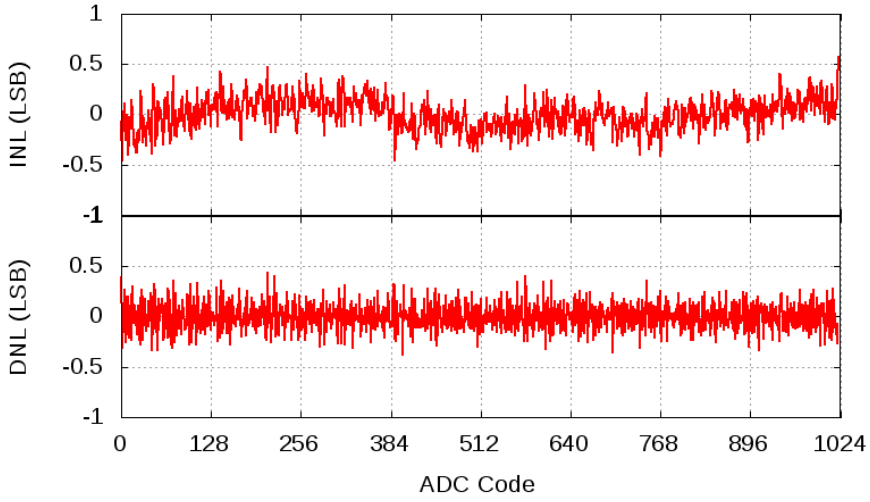
ADC errors
Static NonLinearity errors





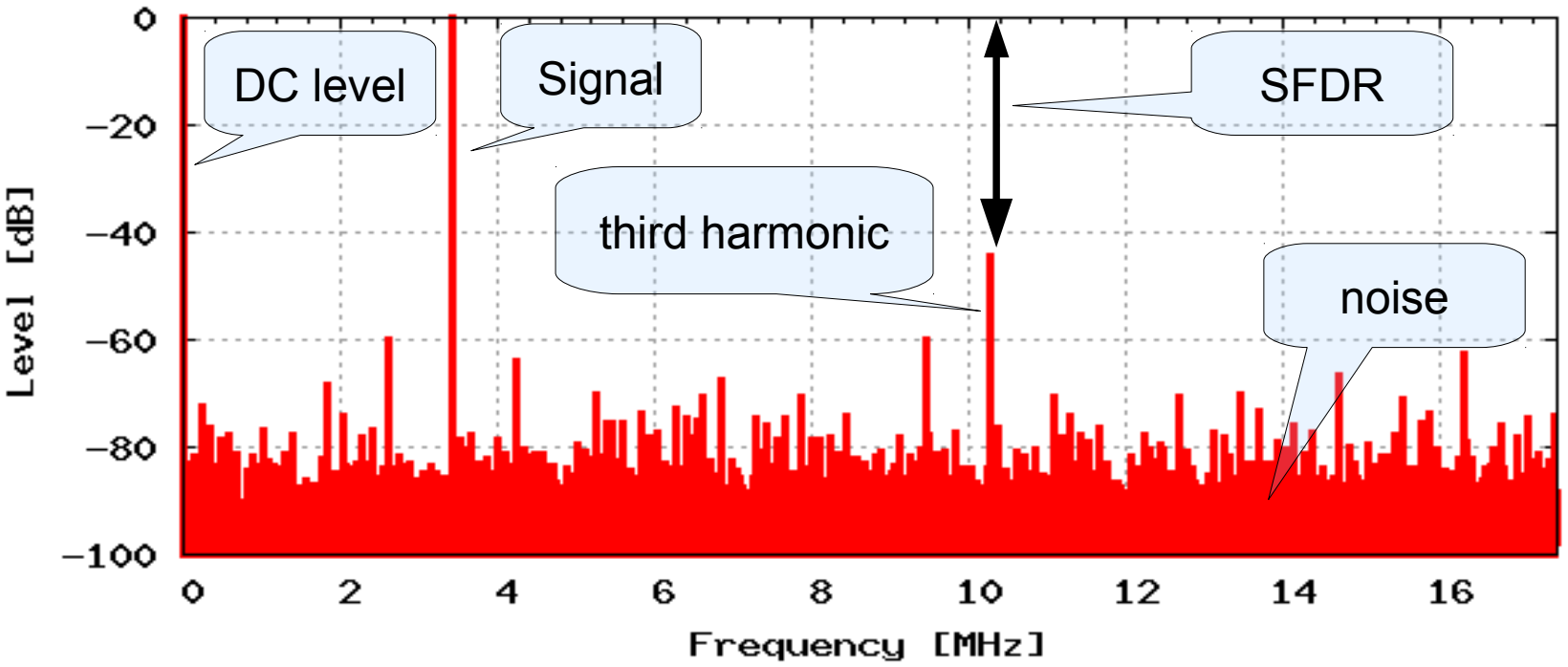
- **DNL** - Differential NonLinearity - the difference between an actual step width and the ideal step width
- **INL** - Integral NonLinearity - deviation of an actual transfer function from a straight line (integrated DNL)

Example of INL/DNL for 10-bit ADC



ADC dynamic
Dynamic errors

- Single tone, full scale sine wave applied to input of the ADC
- Fourier Transform computed from the collected digital samples



- **SNHR –** Signal to Non Harmonic Ratio
- **THD** – Total Harmonic Distortions
- **SFDR** – Spurious Free Dynamic Range
- **SINAD/SNDR –** Signal to Noise and Distortions

ADC errors
Calculation of dynamic errors

From DFT histogram collected with single tone sine input all dynamic parameters (usually expressed in dB) can be calculated:

$$SNHR = 20\log_{10}\sqrt{\frac{X_{sine}^2}{\sum_{k=1,\,k\neq sine\,,\,k\neq harmonics}^{N/2} X_k^2}}$$

$$-THD = 20\log_{10}\sqrt{\frac{X_{sine}^2}{\sum_{k=harmonics}^{10} X_k^2}}$$

$$SINAD/SNDR = 20\log_{10}\sqrt{\frac{X_{sine}^2}{\sum_{k=1,k\neq sine}^{N/2} X_k^2}}$$

$$SFDR = 20\log_{10}\sqrt{\frac{X_{sine}^2}{X_{highest\ spur}^2}}$$

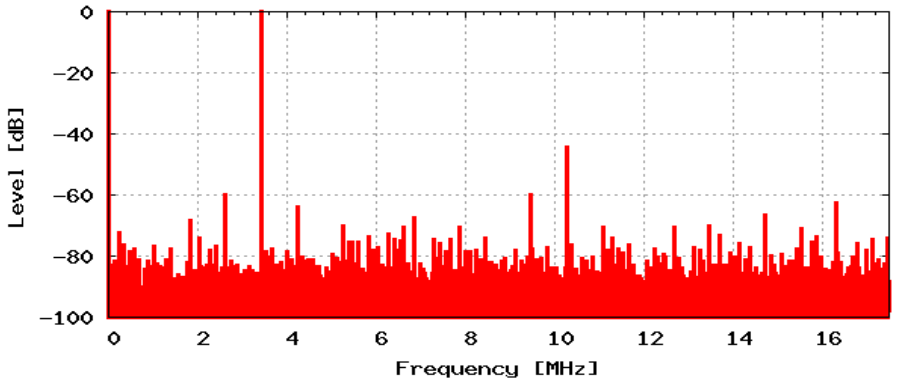
Real ADC Resolution

For ideal ADC with NO harmonic distortion and NO noise only quantization error/noise exists and so its resolution:

$$N = \frac{SNR[dB] - 1.76}{6.02}$$

For realistic ADC the Effective Number Of Bits – ENOB – can be measured/calculated

$$ENOB = \frac{SINAD[dB] - 1.76}{6.02}$$



Aperture jitter
Resolution vs aperture jitter error

$$V_{IN}(t) = V_A \times \sin(2\pi \times f_{IN} \times t)$$

$$\frac{dV_{IN}(t)}{dt} = 2\pi \times f_{IN} \times V_A \times \cos(2\pi \times f_{IN} \times t)$$

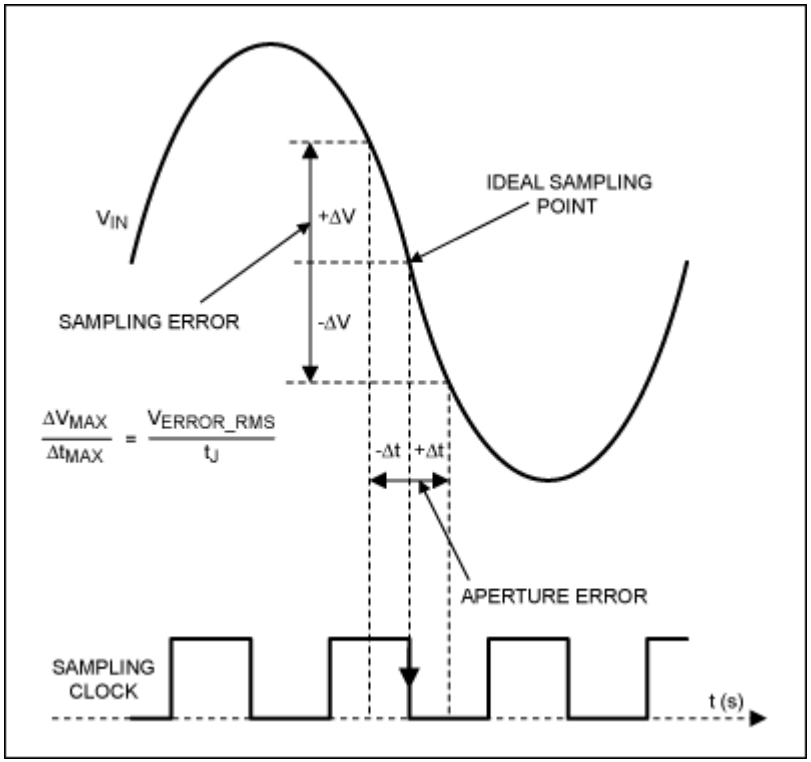
$$\left.\frac{dV_{IN}(t)}{dt}\right|_{RMS} = \frac{2\pi \times f_{IN} \times V_A}{\sqrt{2}}$$

$$\frac{V_{ERROR\_RMS}}{t_J} = \frac{2\pi \times f_{IN} \times V_A}{\sqrt{2}}$$

t_J -time jitter

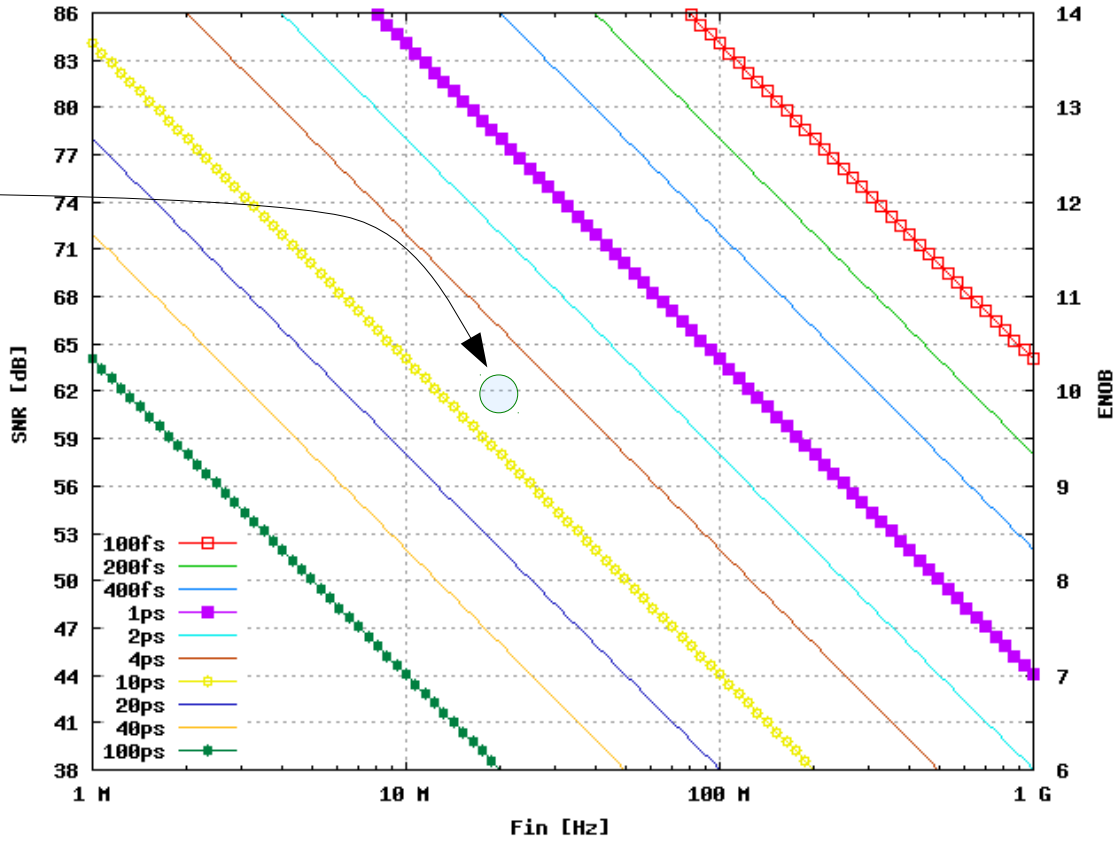
$$V_{ERROR\_RMS} = \frac{2\pi \times f_{IN} \times V_A \times t_J}{\sqrt{2}}$$

$$SNR = 20\log_{10}\left[\frac{V_{IN\_RMS}}{V_{ERROR\_RMS}}\right] = 20\log_{10}\left[\frac{V_A/\sqrt{2}}{2\pi \times f_{IN} \times V_A \times t_J/\sqrt{2}}\right]$$



Aperture jitter
Resolution vs aperture jitter error

For 10-bit ADC sampling at 40 MHz a Nyquist rate (20MHz) signal the aperture jitter error should be significantly less than 10ps to obtain full 10-bit resolution



Aperture jitter worsens the ENOB and so need to be minimized according to the required resolution.

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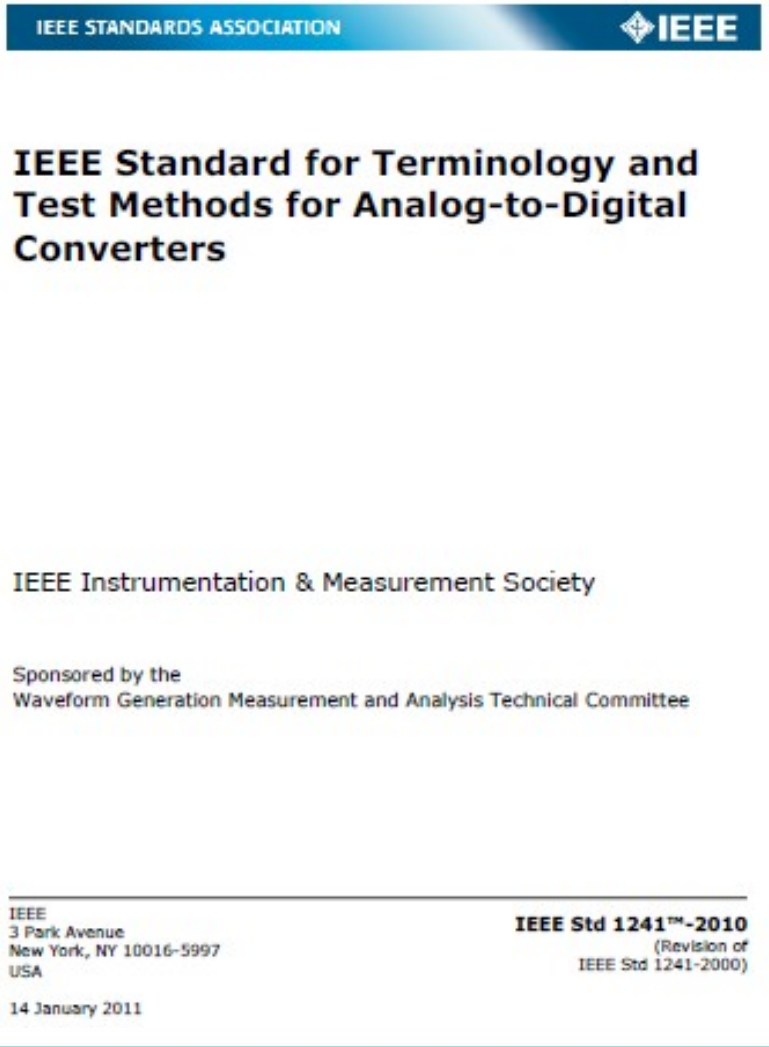
ADC testing

If you have any doubt on ADC test procedure or formula needed, please consult
The IEEE Standard 1241



IEEE STANDARDS ASSOCIATION IEEE

IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

IEEE Instrumentation & Measurement Society

Sponsored by the
Waveform Generation Measurement and Analysis Technical Committee

IEEE
3 Park Avenue
New York, NY 10016-5997
USA

14 January 2011

IEEE Std 1241™-2010
(Revision of
IEEE Std 1241-2000)

ADC testing
Static linearity errors DNL/INL

Linearity errors measurements are usually done using histogram (code density) method. In this method a well defined input signal with uniform probability density function (like ramp) is applied to the ADC input and the histogram with number of occurrences h(k) of each ADC code is done.
From this histogram the DNL is calculated for all codes (except the first and last):

$$DNL(k) = \frac{h(k)_{ACTUAL}}{h(k)_{THEORETICAL}} - 1$$

INL is simply the integral of DNL values

$$DNL(n) = \sum_{k=1}^{n} DNL(k)$$

ADC testing
Theory of dynamic measurements

Input signal S_i

ADC transfer function T_{ADC}

Output data $O_D = S_i \cdot T_{ADC}$

Discrete Fourier Transform (DFT) of output data

$$F(x_n):\ X_k = \sum_{i=0}^{N} x_n \exp\left(\frac{-i2\pi kn}{N}\right)$$

$$F(O_D) = F(S_i \cdot T_{ADC}) = F(S_i) \otimes F(T_{ADC})$$

$$S_i = \sin(kf_{base}) \ \Rightarrow \ F(\sin(kf_{base})) = \delta_k$$

$$f_{base} = \frac{f_{sample}}{N}$$

$$F(S_i) \otimes F(T_{ADC}) = \delta_k \otimes F(T_{ADC}) = F(T_{ADC})$$

Very important !

(otherwise a leak to whole spectrum appears)

If input signal is pure sine wave with frequency equal to the one of DFT fundamental frequencies, deconvolution is straightforward since DFT of input signal is Kronecker delta

ADC testing
Theory of dynamic measurements

DFT of ADC transfer function → spectrum for given sampling frequency and input sine frequency

$$F(T_{ADC}) = f(f_{sample}, f_{sine})$$

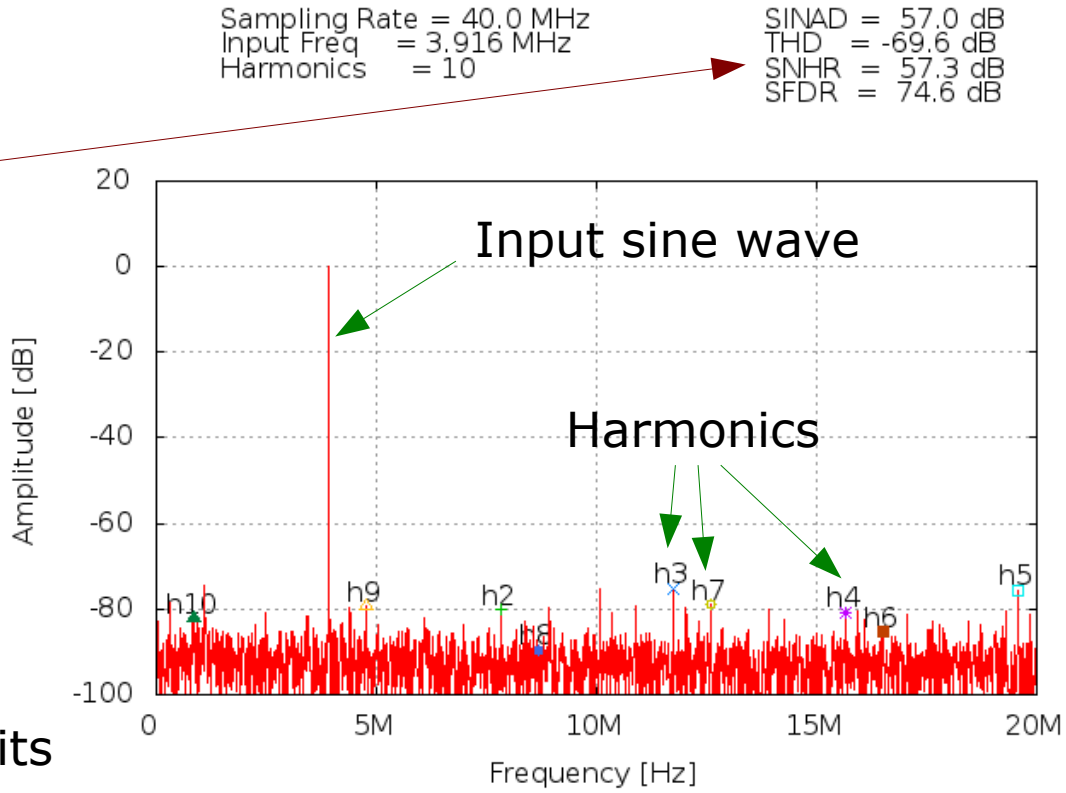
Dynamic metrics calculated from obtained DFT, i.e.:

- **SINAD** – signal to noise and distortion (harmonics) ratio

$$SINAD = 20\log_{10}\sqrt{\frac{X_{sine}^2}{\sum_{k=1,k\neq sine}^{N/2} X_k^2}}$$

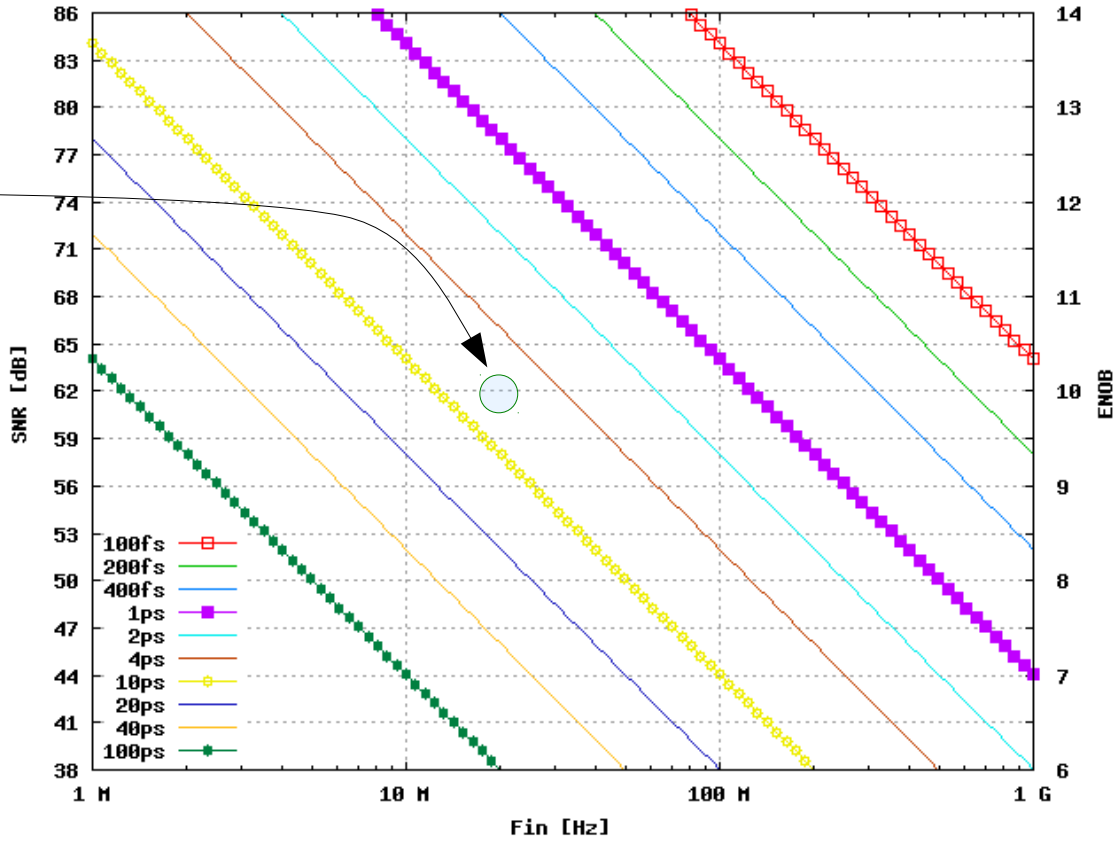
- **ENOB** – effective number of bits

$$ENOB = \frac{SINAD - 1.76}{6.02}$$



ADC testing
Resolution vs sampling clock jitter

For 10-bit ADC sampling at 40 MHz a Nyquist rate (20MHz) signal the phase jitter of sampling clock should be significantly less than 10ps to obtain full 10-bit resolution



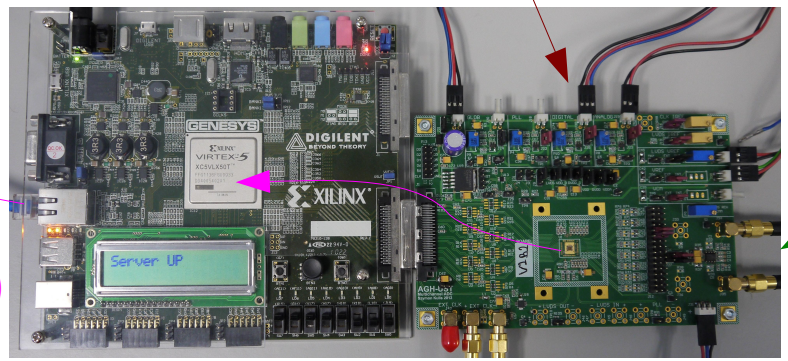
Phase jitter of sampling clock affects the ADC resolution in the same way as ADC aperture jitter. A low jitter generator is needed for ADC testing.

ADC testing
Measurements setup

DFT and data analysis – custom software

Power supply

Differential function generator – Agilent 81160A

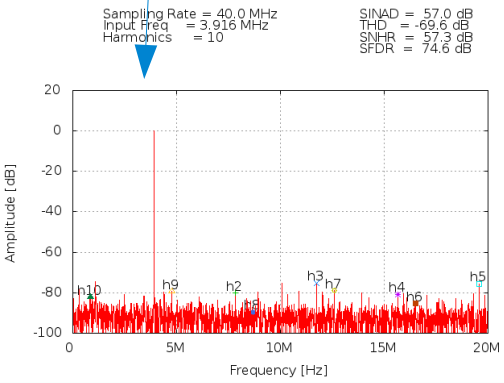


Input sine

Sample clock

Results

Sampled data (**low bitrate**)



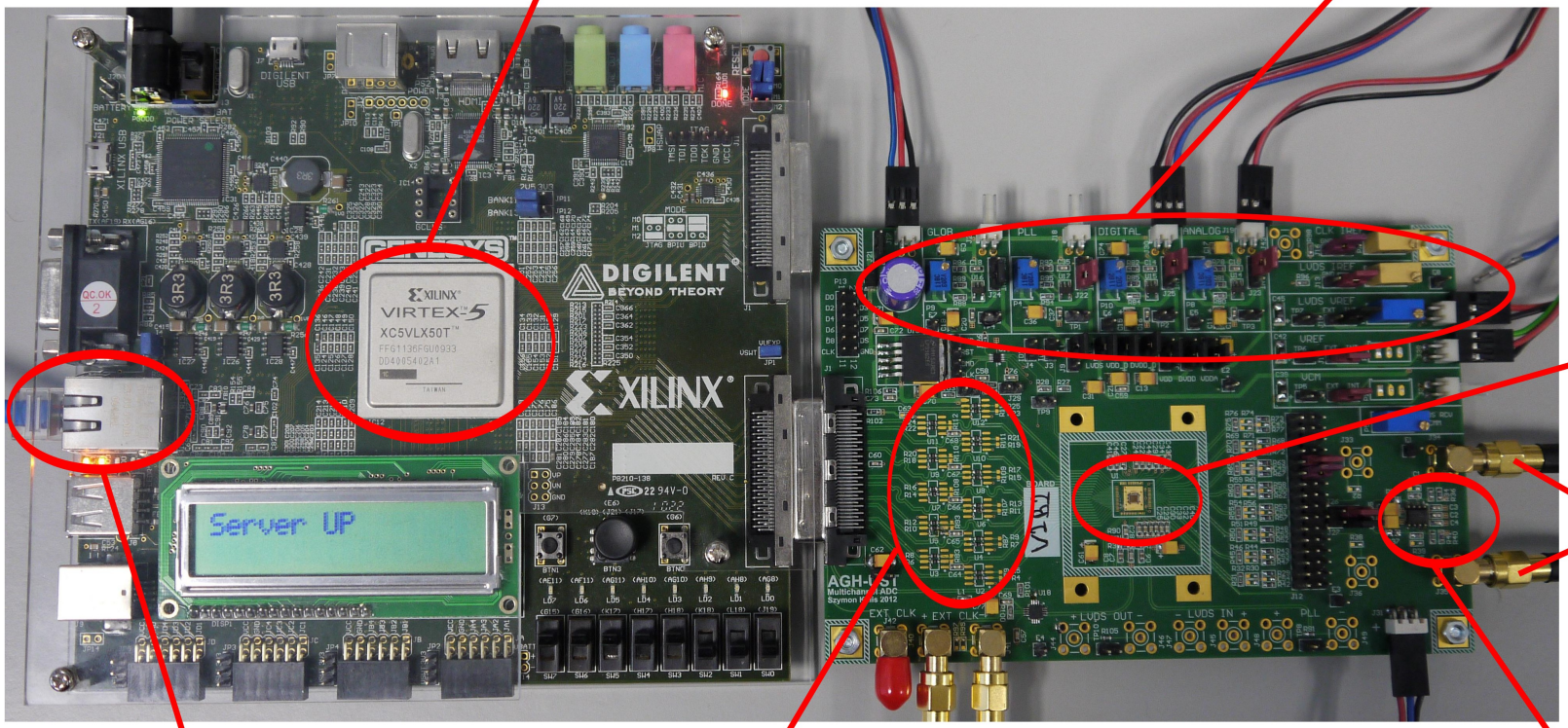
Sampled data (**high bitrate**)

DAQ – receive fast transmission from ADC (up to 500Mb/s), store the assumed amount of data (ie. 4096 samples) and sends to PC via Ethernet for offline analysis.

ADC testing
Measurement setup – main board

DAQ (VIRTEX-5 FPGA)

ADC bias and power supply



10b SAR ADC

Input sine

PC data link (Ethernet)

ADC output data - parallel or serial (SLVS)

Input differential low pass filter

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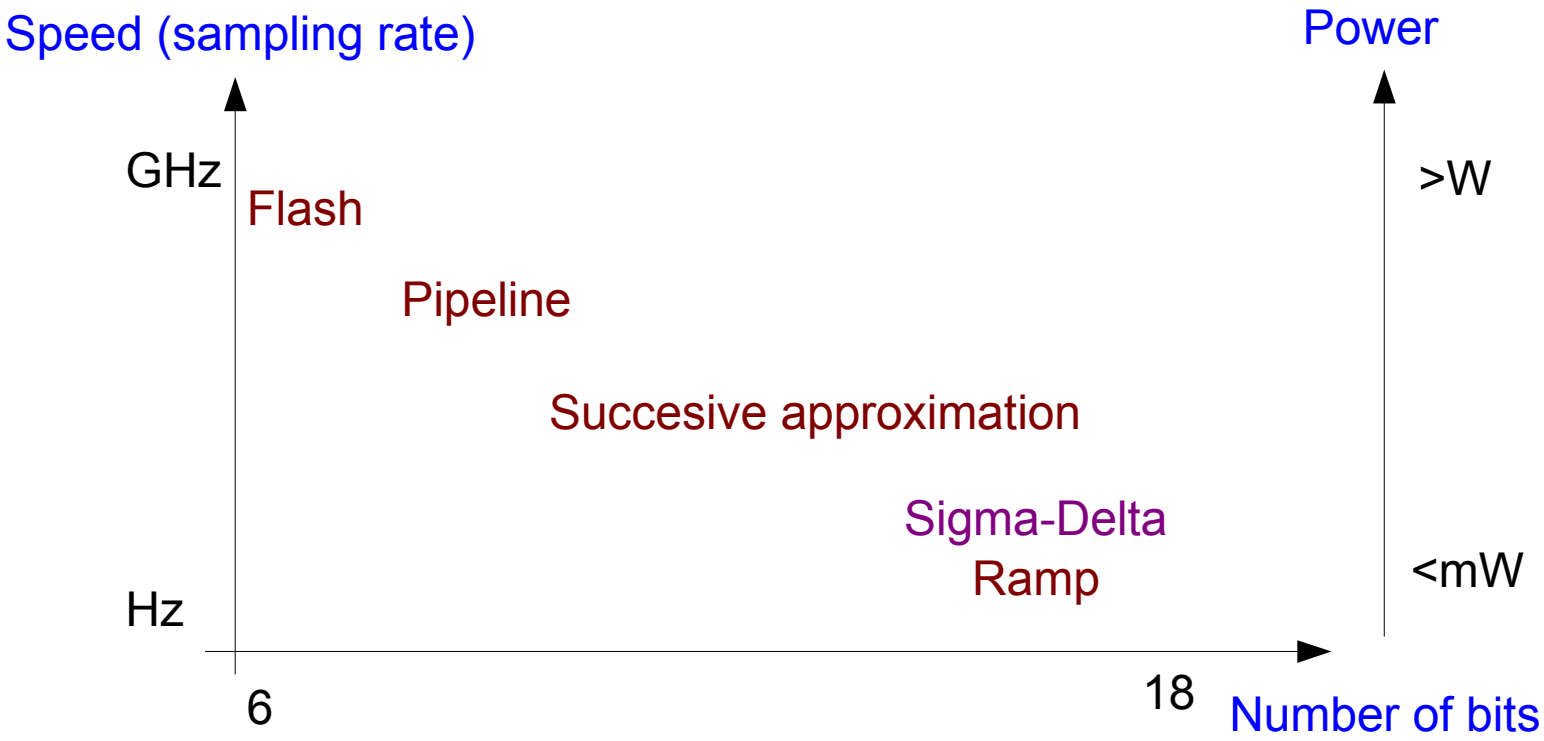
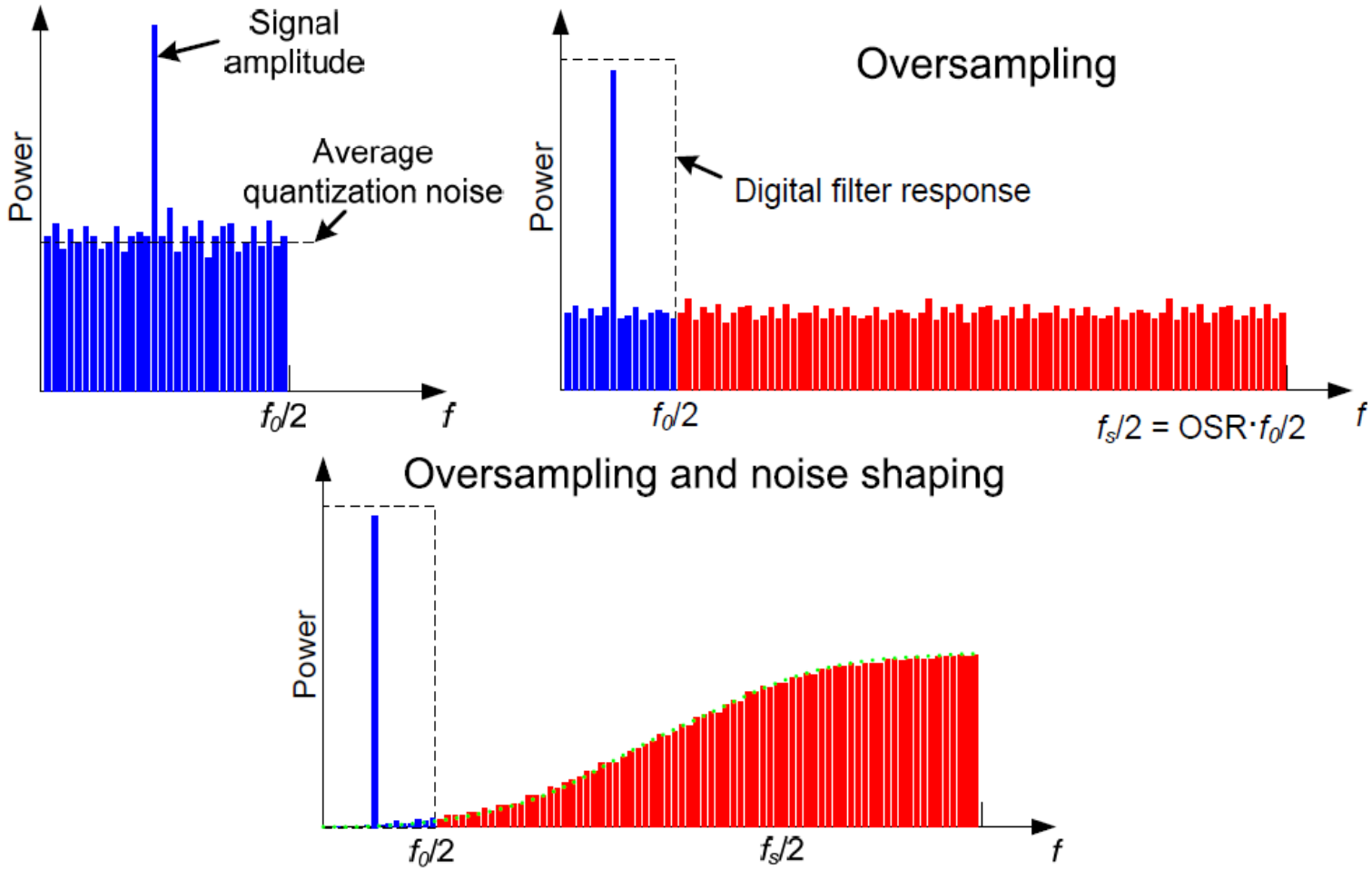
ADC architectures



Nyquist rate ADCs ($f_{signal}^{max} \sim 0.5\, f_{sample}$): Flash, Pipeline, SAR, Ramp, etc...

Oversampling ADCs ($f_{signal}^{max} << 0.5\, f_{sample}$): Sigma-Delta

ADC architectures
Sigma-Delta



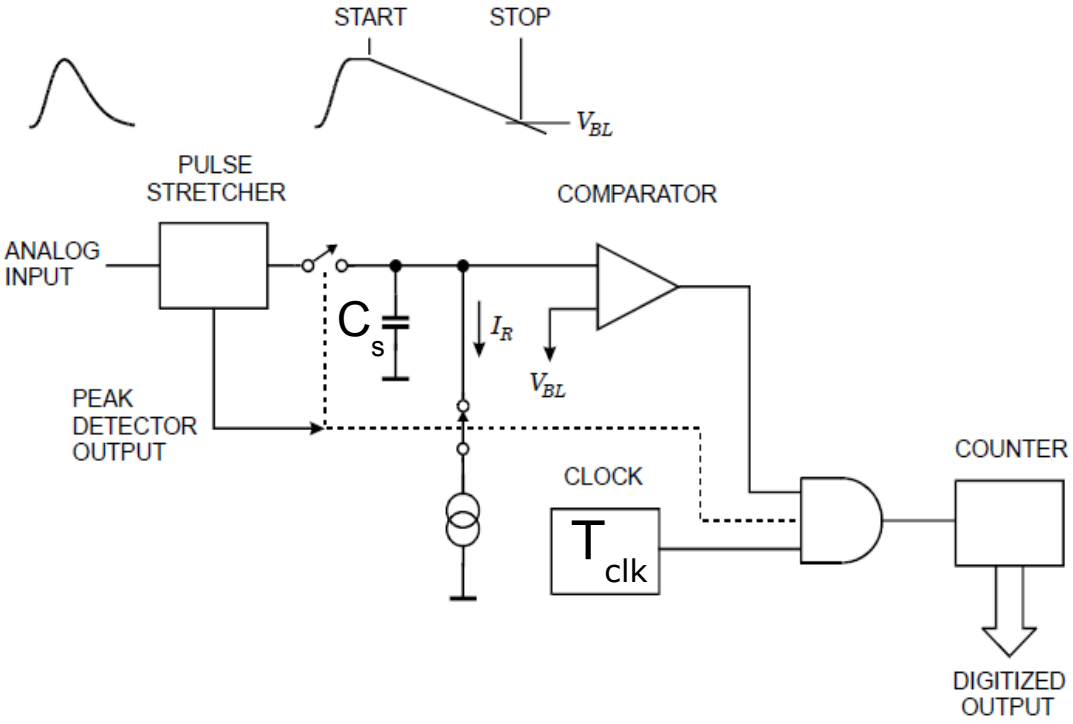
Thanks to Oversampling and Noise Shaping lowest noise (highest resolution >20-bit) can be obtained in Sigma-Delta converters

ADC architectures
Slow (ramp) Wilkinson ADC

Wilkinson ADC is often used in detector readout

When sampling capacitance C_s is charged:

- Stretcher disconnected
- Current source switched on and counter started
- Constant current discharging
- Counter stopped when comparator indicates that voltage on the capacitor reached the baseline



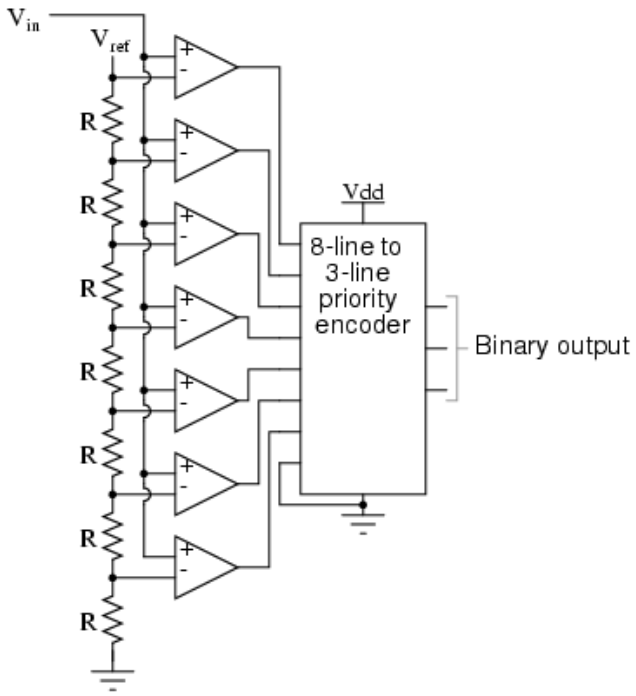
Advantages: high resolution, linearity, low power

Drawback: slow conversion $T_{conv} \sim T_{clk} * 2^{N\text{-bit}}$

ADC architectures
Fast ADC - Flash

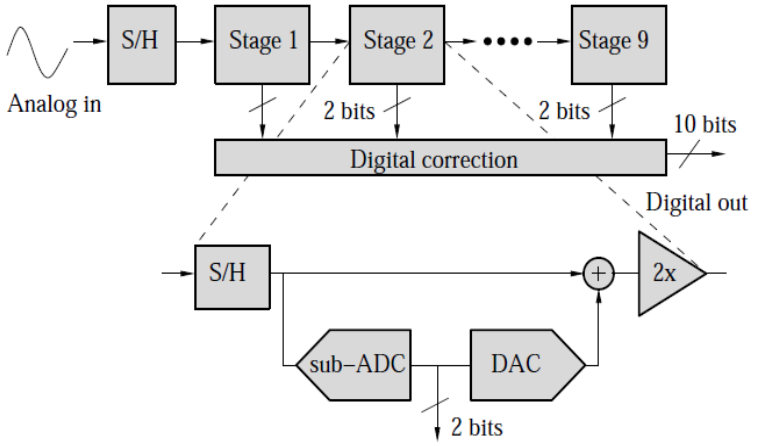
- Flash Architecture
  - Output rate = Clock rate
  - For N-bits need ~2^N comparators&resistors
    - High power consumption
    - Large area
  - Good for low resolution systems (< ~6 bit)

3-bit Flash ADC example

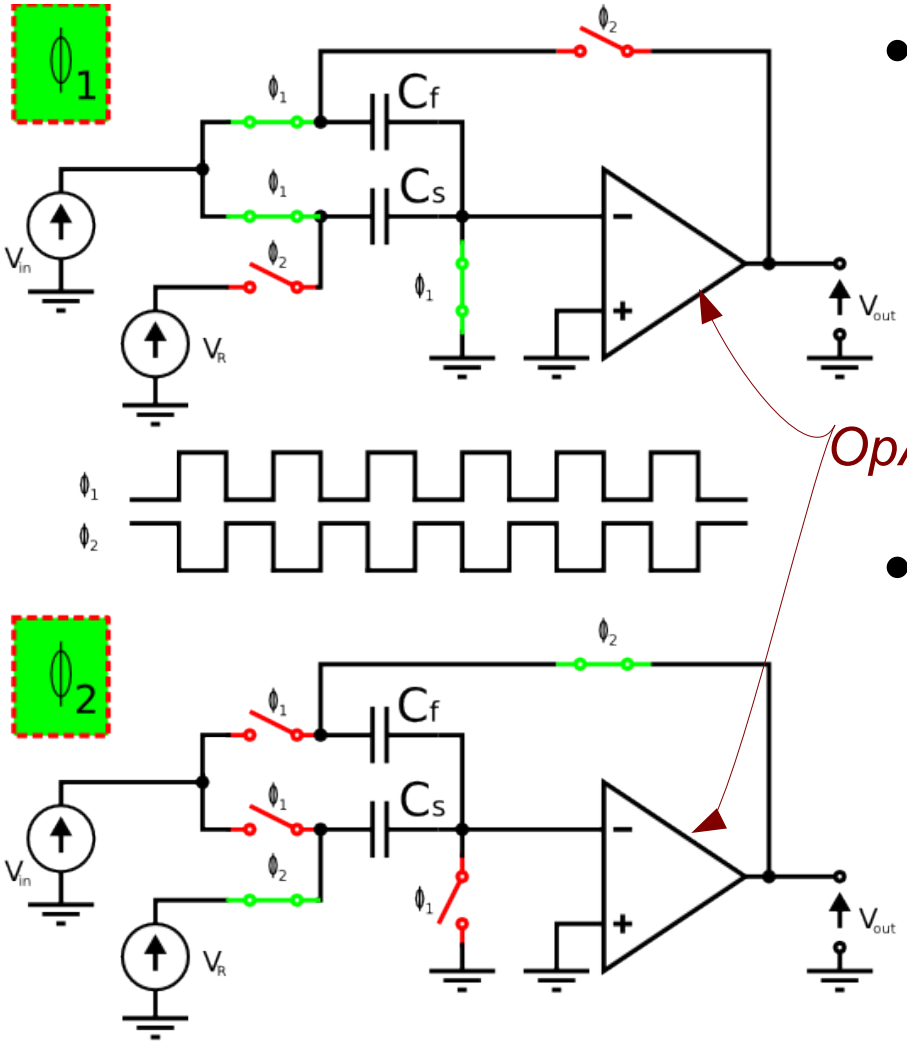


ADC architectures
Fast ADC - Pipeline

- Pipeline architecture
  - Output rate = Clock rate (latency time)
  - For N-bit resolution ~N same pipeline stages (often more than 1-bit per stage is converted) are working concurrently
    - Medium power consumption
    - Medium size
  - Usually up to ~12-bits resolution
  - Very popular architecture (also in HEP detector readouts)



ADC architectures
Fast ADC – Pipeline stage operation



- phase ϕ1 : sample & hold

$$V_{cf} = V_{cs} = V_{in}$$

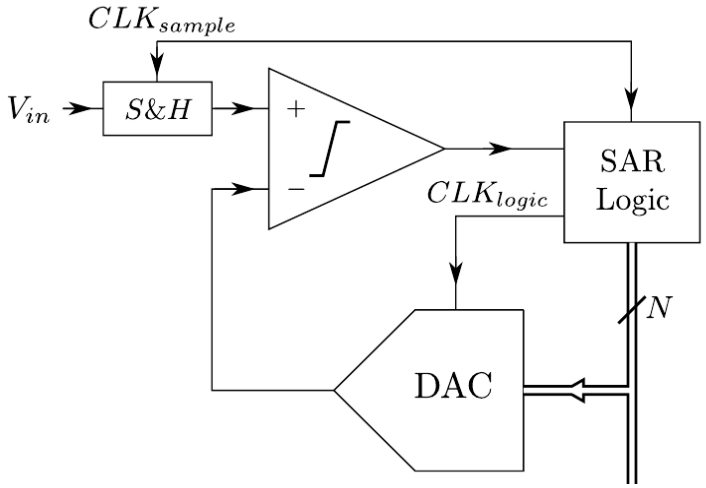
OpAmp- Main power

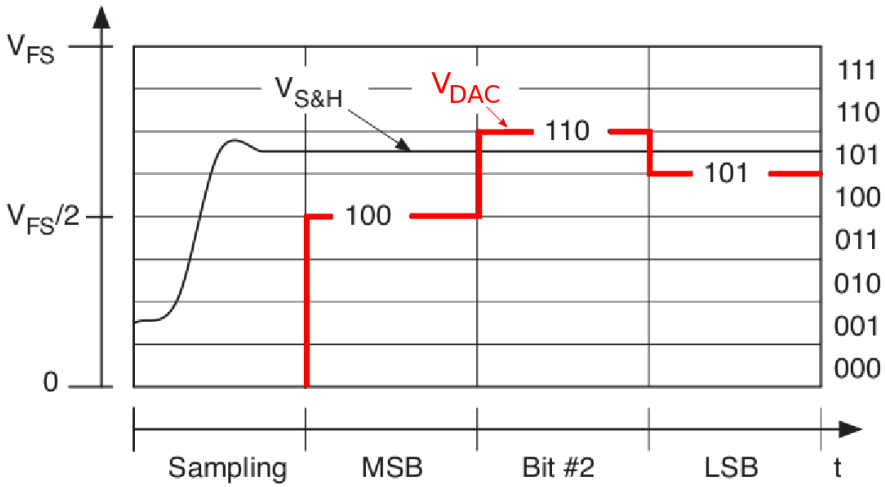
- phase ϕ2 : add & multiply

$$V_{out} \simeq V_{in}\left(1 + \frac{C_s}{C_f}\right) - V_R\left(\frac{C_s}{C_f}\right)$$

ADC architectures
Medium speed ADC – SAR (Succesive Approximation Register) ADC

- SAR architecture
  - Output rate ~ Clock rate/N
  - For N-bits only one stage
    - Very low power
    - Very small area
  - Usually up to ~12-bits
  - In modern CMOS <200nm
    - f_{sample} ~100MS/s possible
    - ultra low power, like ~1mW at 50MS/s for 10-bit ADC possible





Will be discussed in next lecture...

Part I: ADC fundamentals

- Introduction
- ADC fundamentals of operation
- ADC errors
- ADC testing
- ADC architectures
- **ADC State of Art**
- Examples of multichannel ADC in HEP and commercial

How to compare ADC performance ? "Classic" Walden FOM

- Various features/parameters are important in ADC design/applications: effective resolution (ENOB), power, sampling frequency, area, etc... and can be used to create the "Figure Of Merit" (FOM) for ADC
- The first and most commonly used in various publications is the so called Walden FOM:

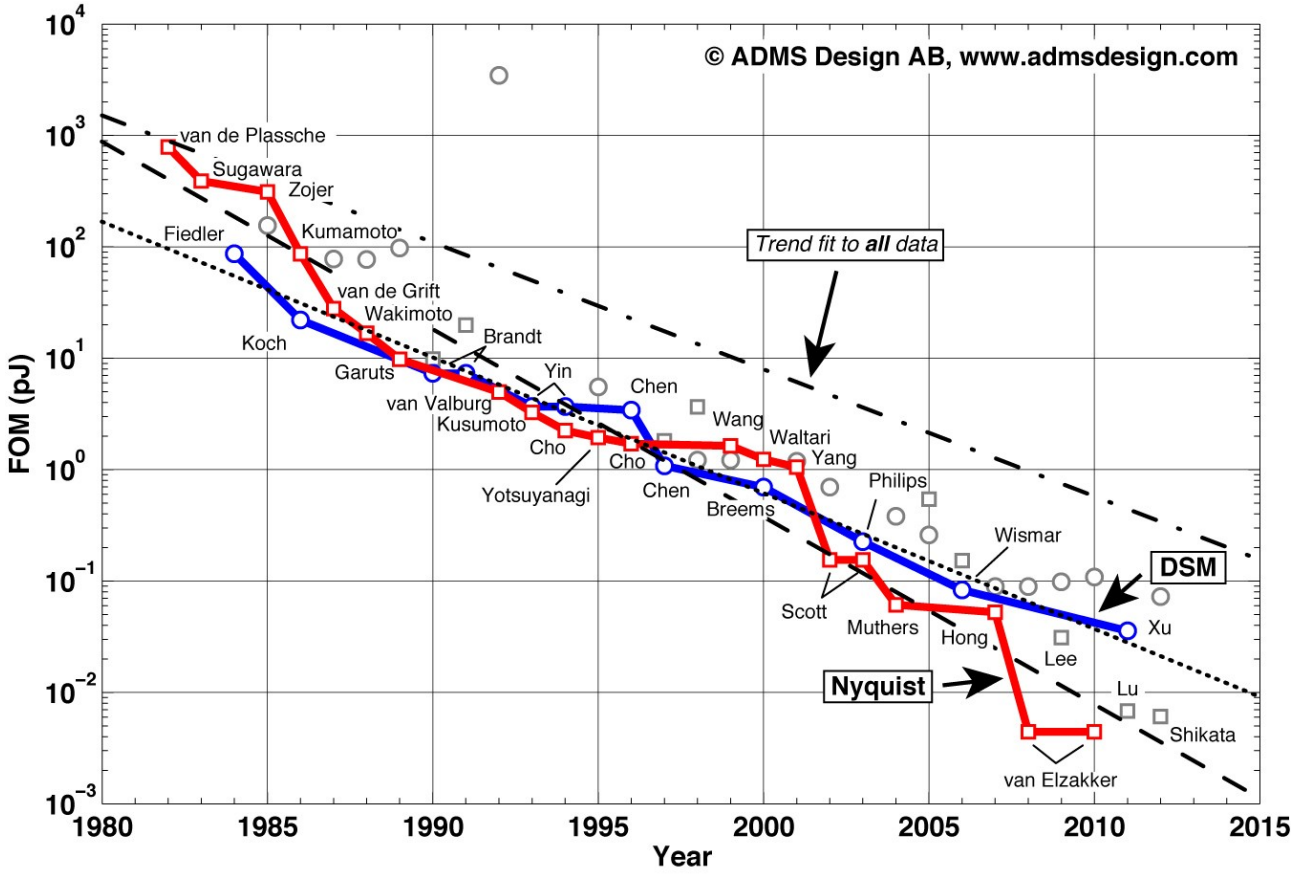
$$FOM = \frac{Power}{f_{sample} * 2^{ENOB}} [J/conv.]$$

- Since it is not "perfect" (does not account for all features), there are also other FOMs, but this one is most commonly used

R. H. Walden, "Analog-to-digital converter technology comparison," in Proc. of GaAs IC Symp., pp. 228–231, Oct., 1994.
R. H. Walden, "Analog-to-digital converter survey and analysis," IEEE J. Selected Areas in Communications, no. 4, pp. 539–550, Apr. 1999.

ADC State of Art
Walden FOM evolution in time

$$FOM = \frac{Power}{f_{sample} * 2^{ENOB}} [J/conv.]$$

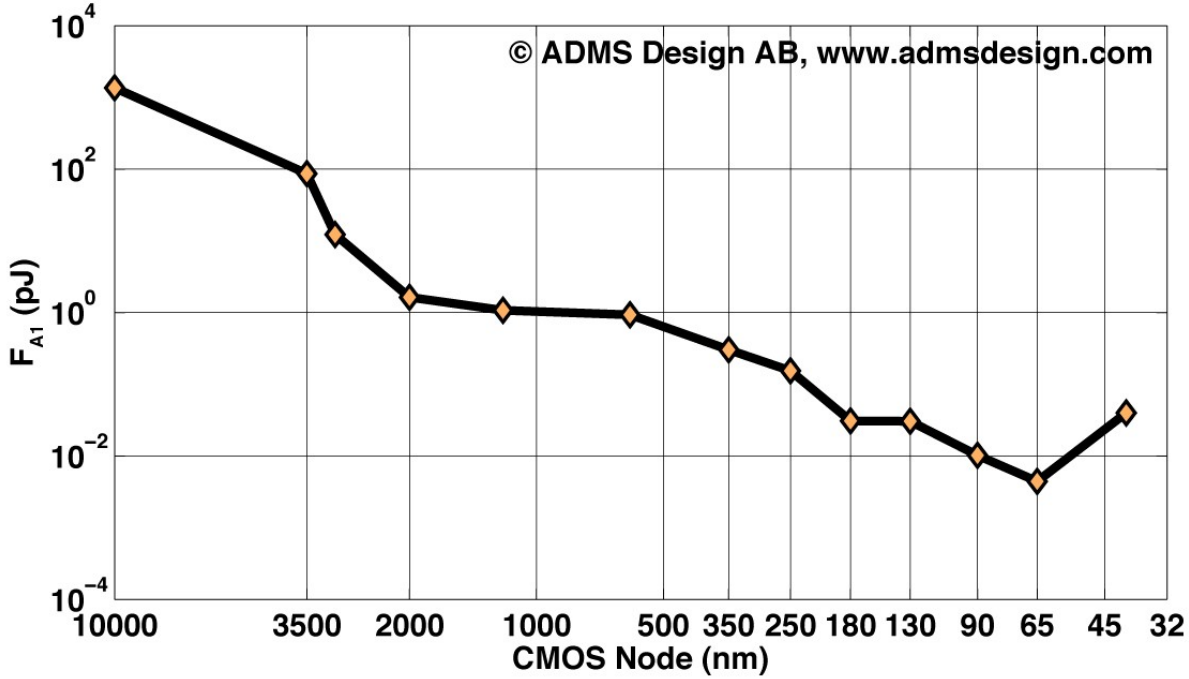


Nyquist ADCs improve roughly 2 times every 1.8 year. From ~2000 Nyquist rate ADCs broke away from the trend and improve faster...

http://converterpassion.wordpress.com/2012/08/21/adc-performance-evolution-walden-figure-of-merit-fom/

ADC State of Art
Walden FOM vs CMOS scaling

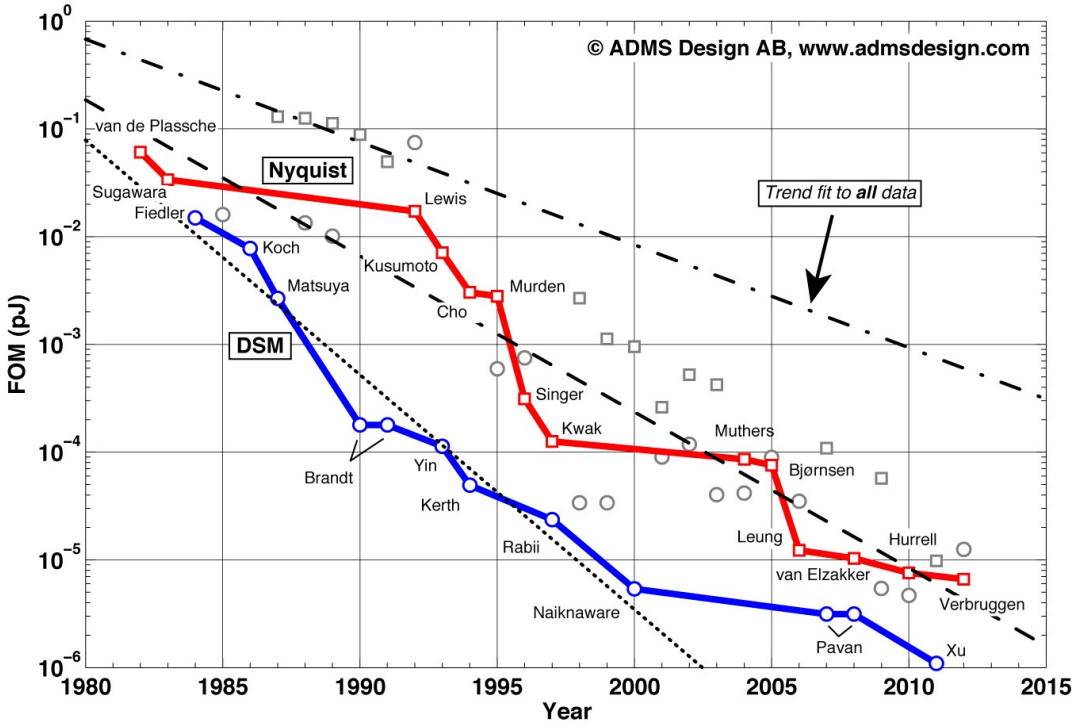
$$FOM = \frac{Power}{f_{sample} * 2^{ENOB}} [J/conv.]$$



FOM improves by roughly 100 time with a tenfold CMOS scaling.
Main factor – decreasing power supply.

B. E. Jonsson, "On CMOS scaling and A/D-converter performance," Proc. of NORCHIP, Tampere, Finland, pp. 1–4, Nov. 2010

"Thermal FOM"

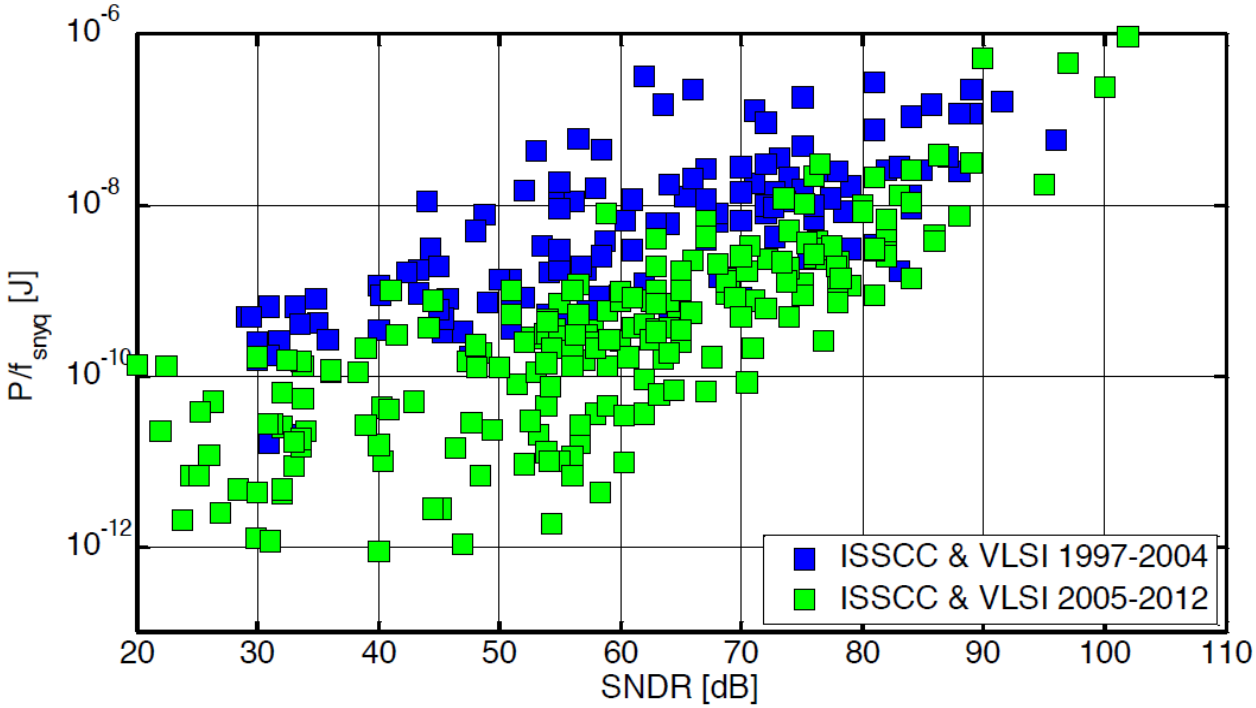


For high resolution ADCs,whose resolution is limited by thermal noise, the "Thermal" FOM_{Th} is used for comparison:

$$FOM_{Th} = \frac{Power}{f_{sample} * 2^{2*ENOB}} [J/conv.]$$

A. M. A. Ali, C. Dillon, R. Sneed, A. S. Morgan, S. Bardsley, J. Kornblum, and L. Wu, "A 14-bit 125 MS/s IF/RF sampling pipelined ADC with 100 dB SFDR and 50 fs jitter," IEEE J. Solid-State Circuits, Vol. 41, pp. 1846–1855, Aug, 2006

ADC State of Art
Murmann Figure of Merit



Since there is no theoretical reason to have power exactly doubled at each additional bit of resolution Murmann prefers to show the plot of of Power/f_{sample} versus "resolution" (SNDR)

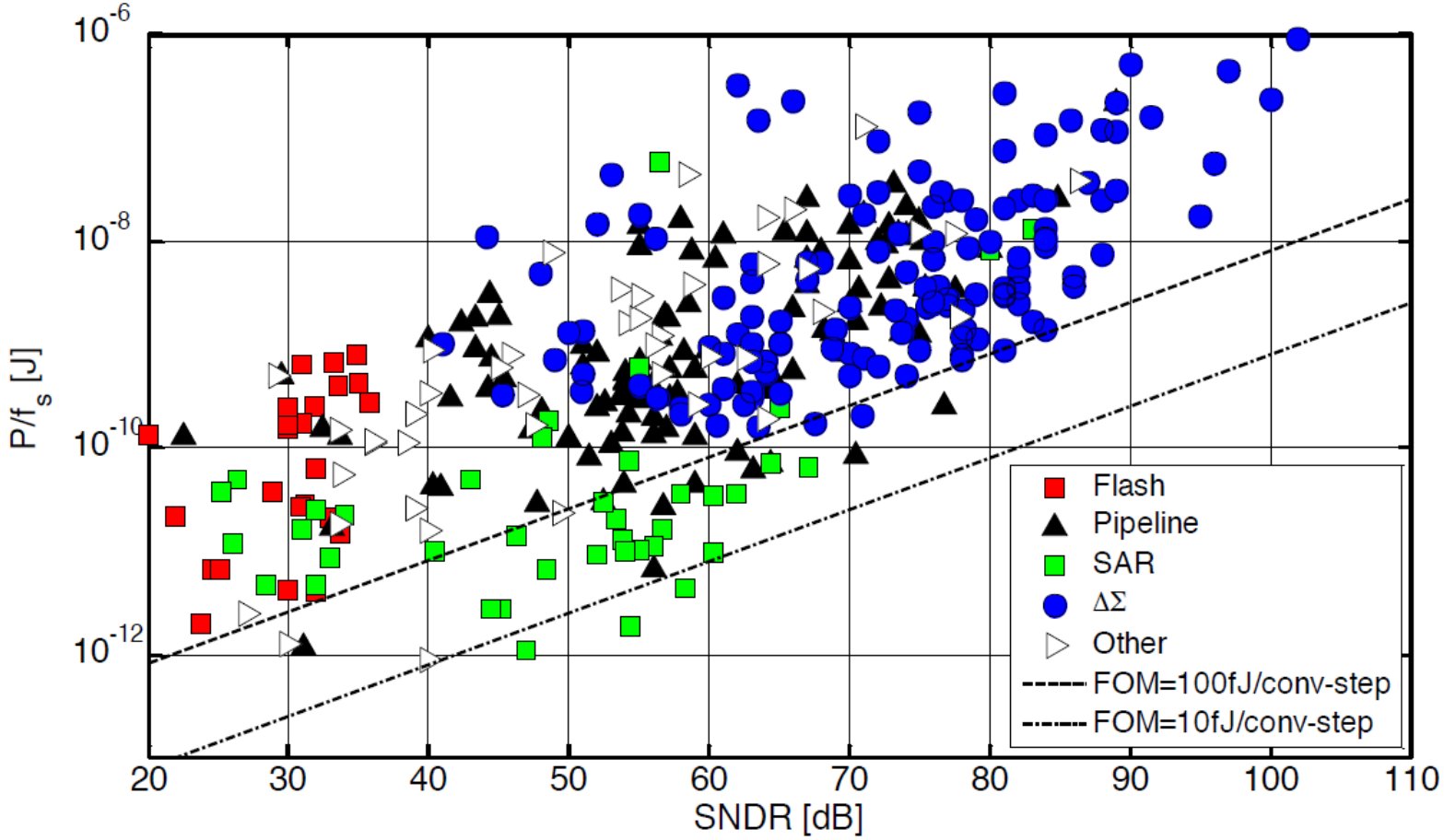
$$ENOB = \frac{SNDR[dB] - 1.76}{6.02}$$

A huge performance improvement has been obtained in the last ~10 years.

A nice feature of Murmann ADC survey is the fact that it is constantly updated on his webpage:

B. Murmann, "ADC Performance Survey 1997-2013", http://www.stanford.edu/~murmann/adcsurvey.html

ADC State of Art
Murmann Figure of Merit - architectures



Most of the best ADCs (FOM<100fJ/conv.) are SARs designed within last 10 years

B. Murmann, "ADC Performance Survey 1997-2013", http://www.stanford.edu/~murmann/adcsurvey.html

Part I: ADC fundamentals

- Introduction
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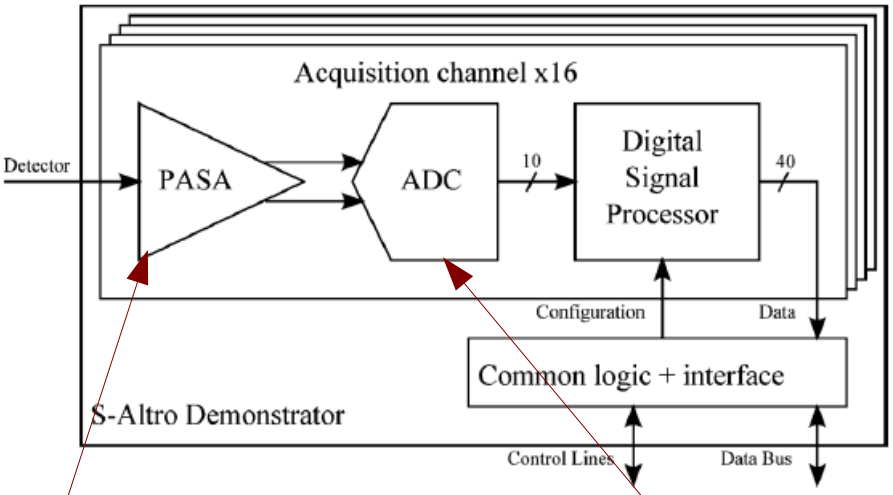
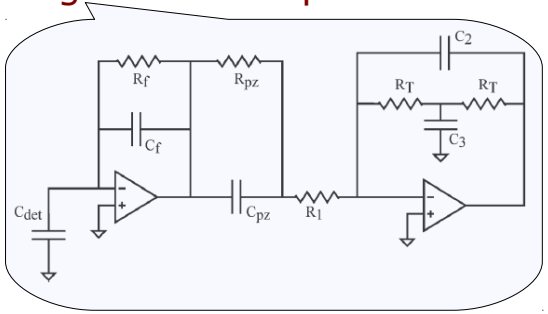
- **Examples of multichannel ADC in HEP and commercial**

S-ALTRO Demonstrator ASIC
Project at CERN in 130 nm CMOS

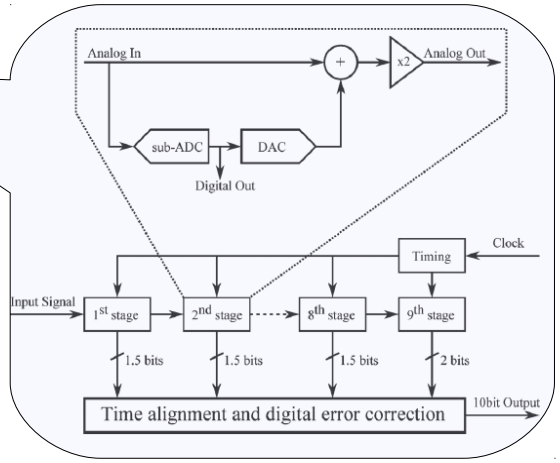


Supply voltage	1.5 V core, 2.5 V pads
Programmable gain	12, 15, 19 or 27 mV/fC
Programmable peaking time	30, 60, 90 or 120 ns
Shaper type	CR-(RC)^4
Programmable signal polarity	Positive or negative
Linearity	±5% up to 150 fC
Detector capacitance	4-20 pF
ENC	<1000 e$^-$ @ 12 pF
Cross-talk	<1%
Number of bits	10
Sampling frequency	10-40 MHz
Readout frequency	max 80 MHz
Power consumption	<50 mW/channel
Area	<4 mm^2/channel

Front-end with
semi-gaussian shaper

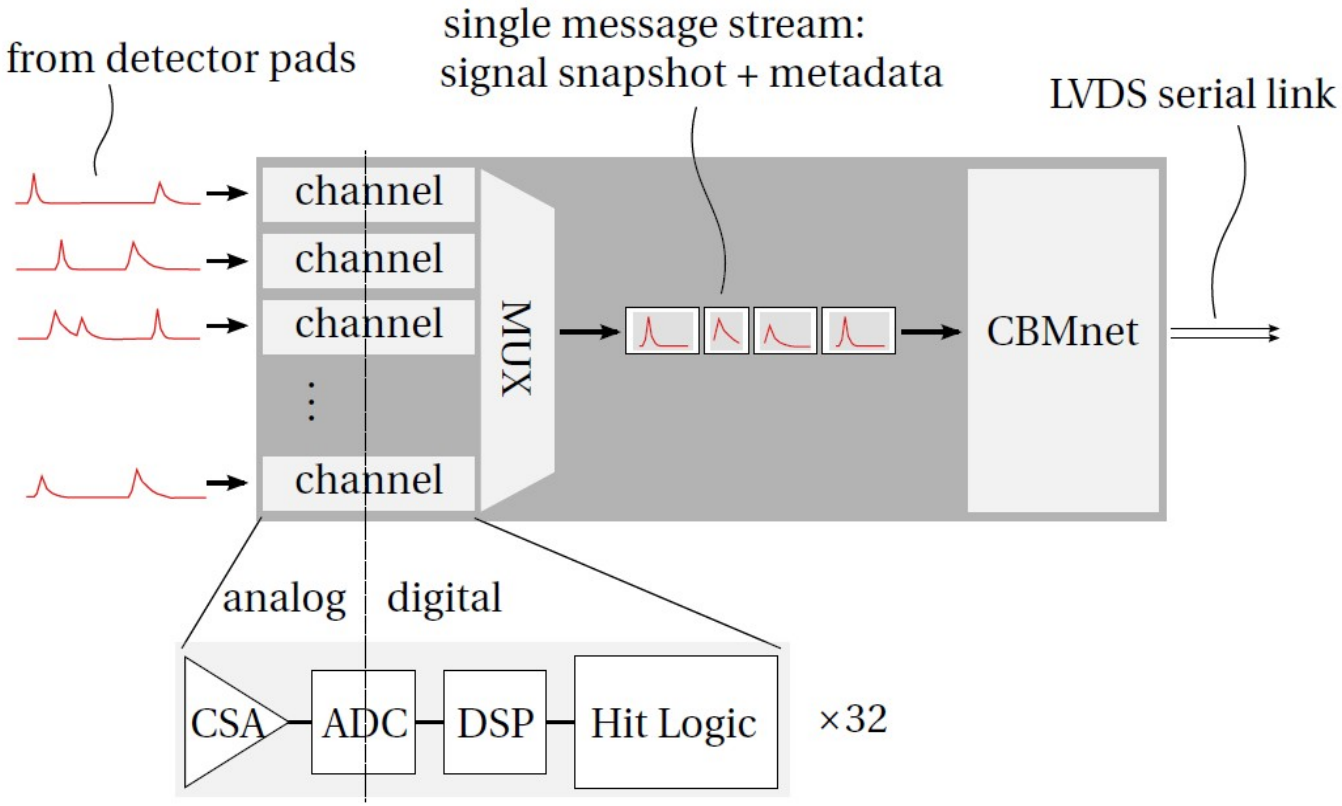


10-bit pipeline ADC
ADC consumes ~33 mW !!
FOM ~ 1.5pJ/conv.



P. Aspell, M.De Gaspari, H. Franca, E. Garcia, L. Musa "A Super-Altro 16: A Front-End System on Chip for DSP Based Readout of Gasous Detectors", IEEE Trans. On Nucl. Science vol. 60, April 2013 pp. 1289-1295

SPADIC: Self-triggered Pulse Amplification and Digitization ASIC
for TRD readout at CBM (FAIR)



CMOS UMC 180nm

Front-end

- Preamplifier
- Semi-gaussian shaper
- Tpeak 80ns
- Power 4-8 mW
- ENC~800e@30pF

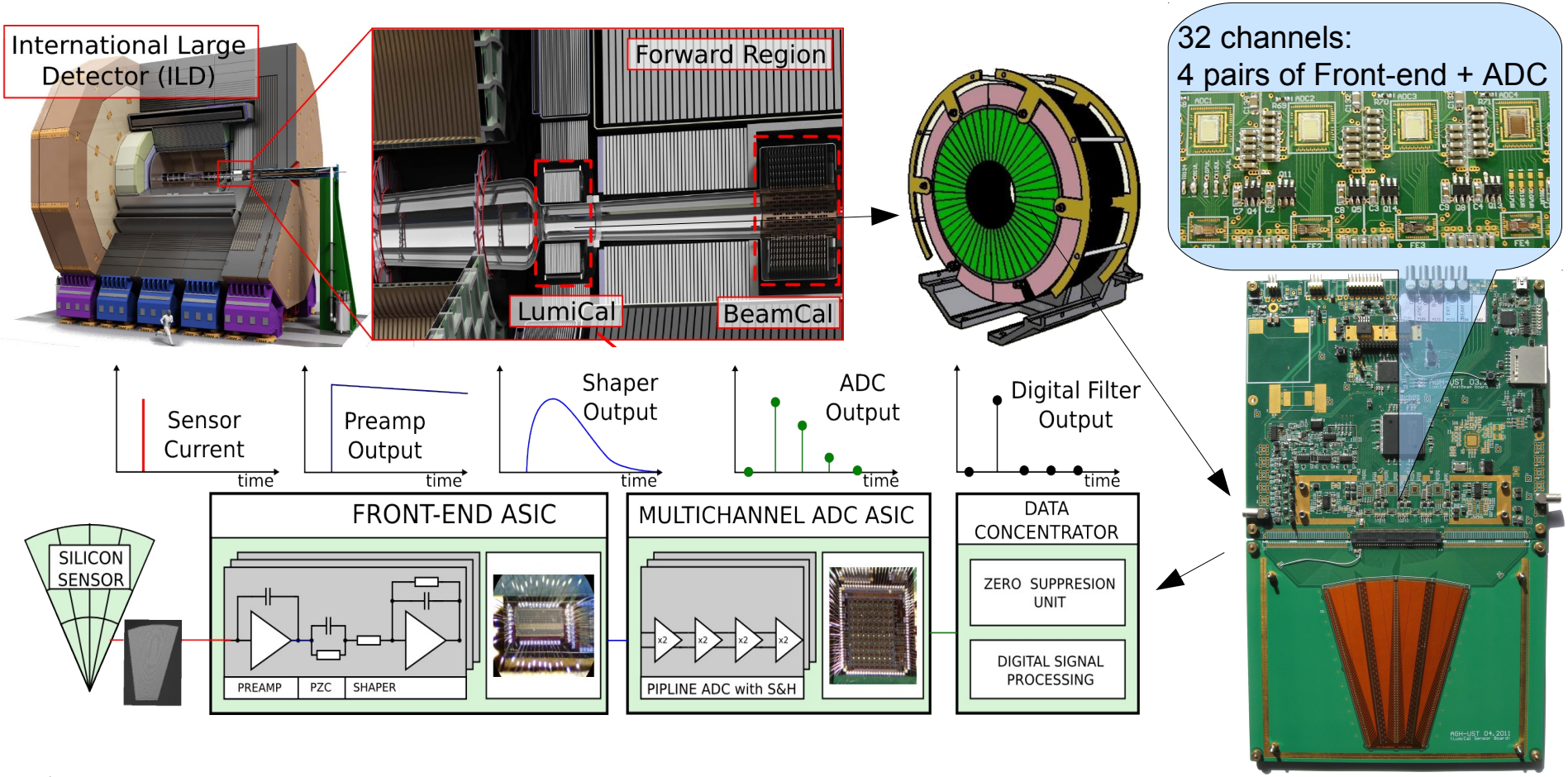
9-bit Pipeline ADC

- f_{sample} 25MHz
- ENOB ~8 bits
- Power cons. 4.8mW
- FOM ~ 0.75 pJ/conv.

T. Armbruster, P. Fischer, M. Krieger, I. Peric "SPADIC – Self-triggered charge pulse processing ASIC", TWEPP2013 23-27 September 2013, Perugia Italy

Readout of LumiCal - Luminosity calorimeter for future International Linear Collider (ILC)

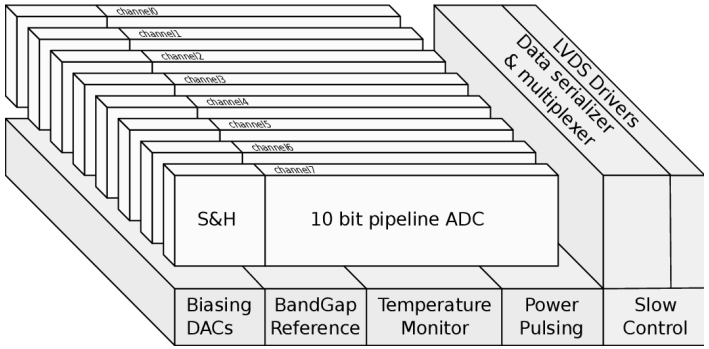
LumiCal detector will contain 30 layers of sandwitch Si-W calorimeter ~200 000 channels

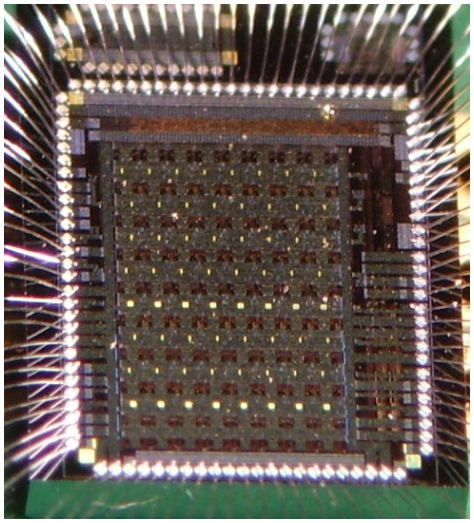


1st Prototypes of 8-channel front-end and ADC ASICs were designed and produced in AMS 0.35um CMOS. 32-channel readout module was built.

Multichannel digitizer ASIC for LumiCal readout

- **Main features:**
  - 8 channels of 10-bit pipeline fully differential ADC
  - Technology AMS 0.35um
  - Layout with 200um ADC pitch
  - Multimode digital multiplexer/serializer:
    - Test mode: single channnel output (max fsmp ~50 Msps)
    - Parallel mode (~250MHz): one data link per channel (max fsmp ~ 25 MSps)
    - Serial mode (~250MHz): one data link per all channels (max fsmp ~ 3 MSps)
  - High speed LVDS interface (~1GHz)
  - Power pulsing
  - BandGap reference and Temperature sensor
  - Various DACs
  - Power consumption 1.2mW/channel/MHz
  - ENOB ~ 9.7, FOM ~ 1.4 pJ/conv.

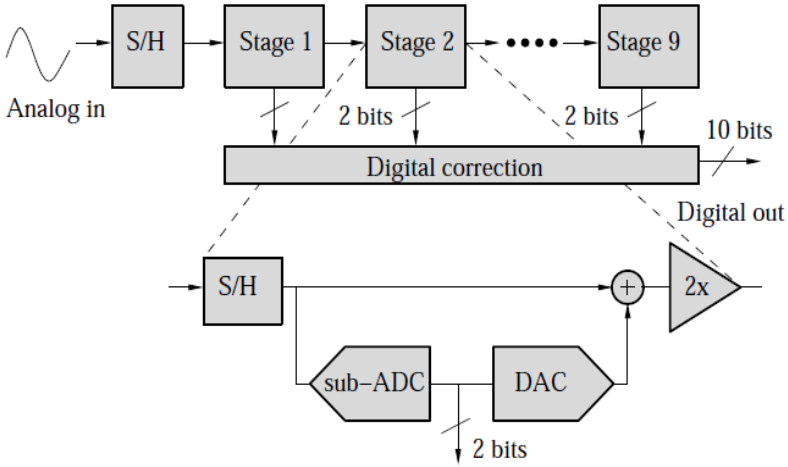


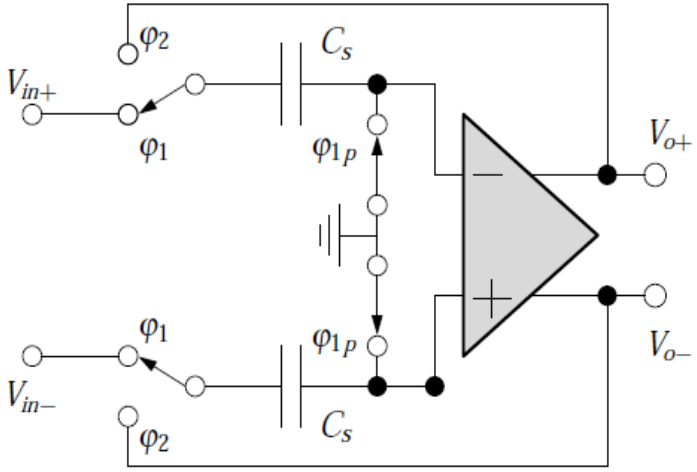


2.6mm x 3.2mm

M. Idzik, K. Swientek, T. Fiutowski, Sz. Kulis, D. Przyborowski "A 10-bit multichannel digitizer ASIC for detectors in particle physics experiments", IEEE Trans. Nucl. Sci. v.59 p.294-302 2012

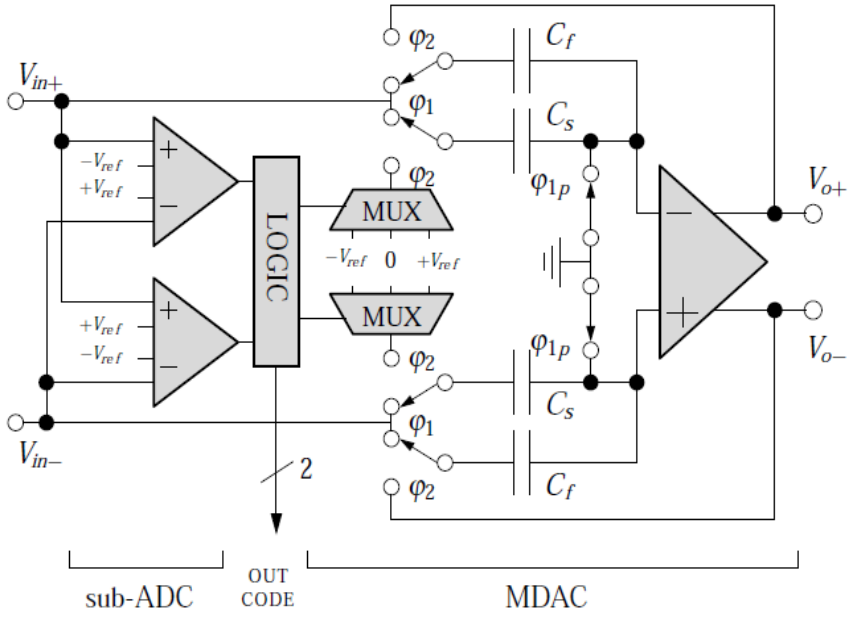
Multichannel digitizer ASIC
10-bit pipeline ADC





S/H stage

- High throughput - conversion rate = clock rate
- 1.5 bit per stage - redundancy reduces comparator requirements
- Fully differential architecture

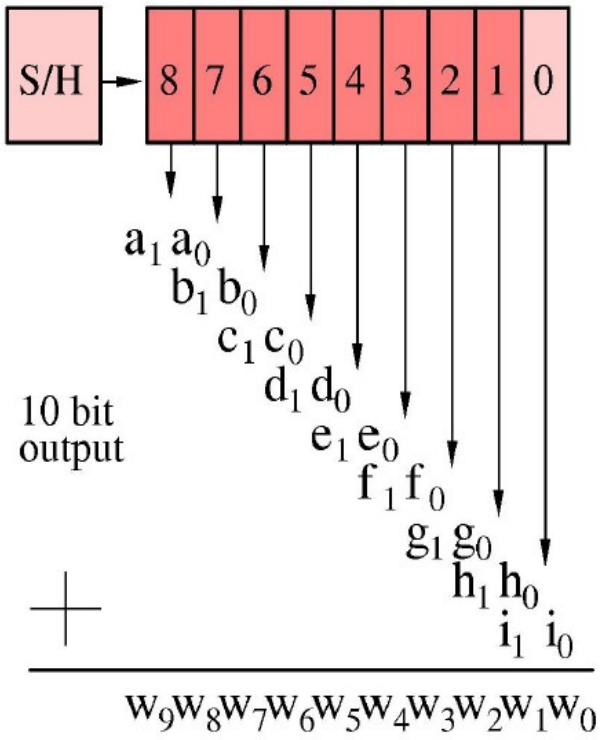


1.5 bit pipeline stage

Pipeline ADC – digital correction

• Digital part, including digital correction block is described in Verilog, synthesized automatically with RC Compiler (Cadence), and implemented using SoC Encounter (Cadence)

Digital correction

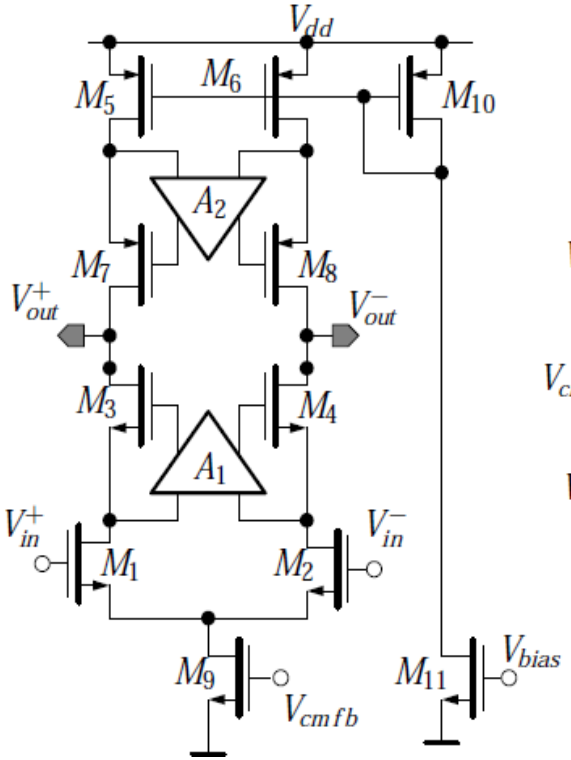


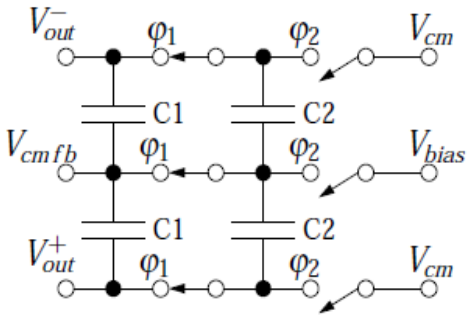
- Denote stage output as $s_i = \{0, 1, 2\}$
- Then digital correction is

$$w = \sum_{i=0}^{8} 2^i s_i$$

Pipeline ADC – analog blocks

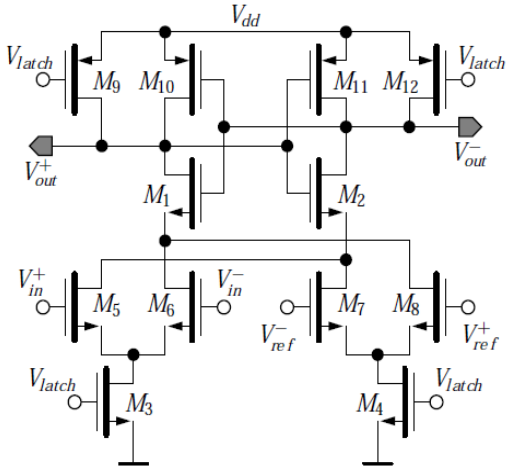
- Fully differential amplifier+CMFB





High gain amplifier needed for precise Multiplication by 2

- Dynamic latch comparator

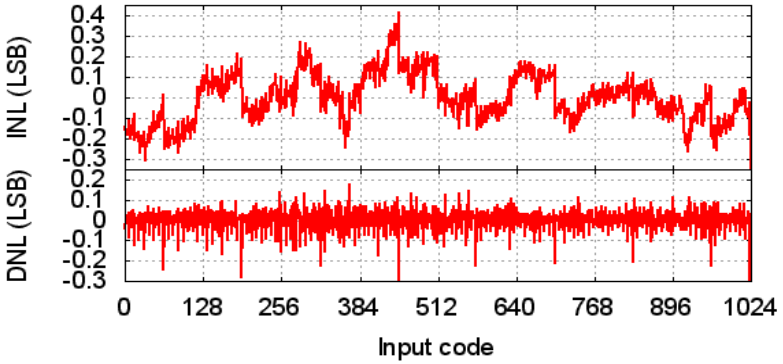


Simple low precision comparator good enough (because of 1.5 bit per stage redundancy)

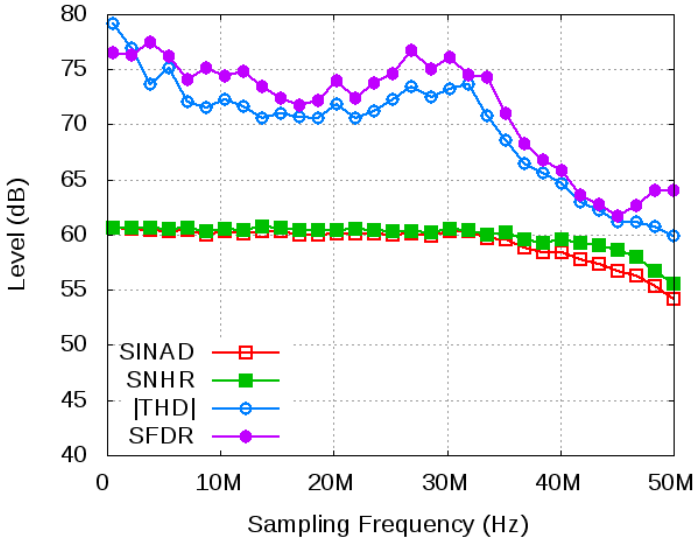
Multichannel digitizer ASIC
Performance measurements

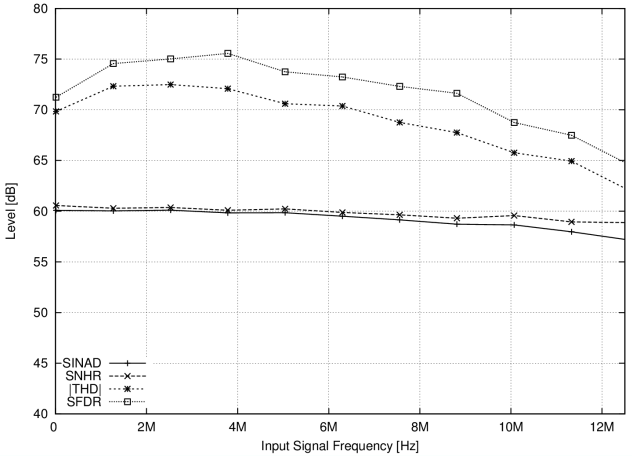
- Performance
  - ENOB=9.7 up to 25 Ms/s (8 channels)
  - INL<0.68, DNL<0.62
  - Sampling rate up to ~25MS/s (multichannel) or up to ~50MS/s (single channel)
  - Power scales linearly with sampling rate ~1.2mW/channel/MHz (without power pulsing)

Static measurements



Dynamic measurements





"Fast" Multichannel 10-bit pipeline ADCs Commercial and research solutions

These ADCs have FOM ~ 1-2 pJ/conv. Means 1-2 orders of magnitude worse than the best published designs.

A lot can be done...

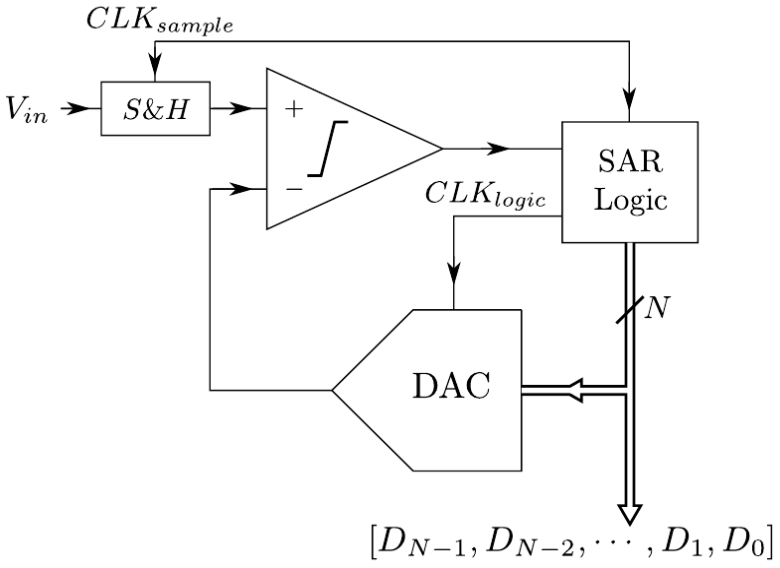
Parameter	Our work*	K. Kavani et al ESSCIRC 2002	AD9212 AnalogDevices	ADS5287 TexasInstruments	MAX1434 Maxim
Nr of channels	8	8	8	8	8
Architecture	10-bit pipeline	10-bit pipeline	10-bit pipeline	10-bit pipeline	10-bit pipeline
Serialization	Per channel & per chip	Per chip	Per channel	Per channel	Per channel
Technology	0.35 µm CMOS	0.25 µm CMOS	-	CMOS	BiCMOS
Supply	3.3 V	2.5 V	1.8 V	3.3/1.8 V (A/D)	1.8 V
Max. f_{sample}	25MS/s	20MS/s	65MS/s	65MS/s	50MS/s
Input range	2Vpp	-	2 Vpp	2 Vpp	1.4 Vpp
Power/channel	~1.2mW/MS/s plus I/O (<15%)	41mW@20MS/s	100mW@65MS/s 68mW@40MS/s	74mW@65MS/s 46mW@30MS/s	96mW@50MS/s
Area	8.2 mm^2	4mm^2	9x9mm^2 (package)	9x9mm^2 (package)	14x14mm^2 (package)
INL	<0.68LSB	-	<0.5LSB	<1LSB	<1LSB
DNL	<0.62LSB	-	<0.4LSB	<0.55LSB	<0.5LSB
SINAD	~60.3dB	54.3dB	>=60dB	>=60.4dB	>=60dB
T_{power_ON}	<=10Tclk (~µs)	-	375µs	-	100ms

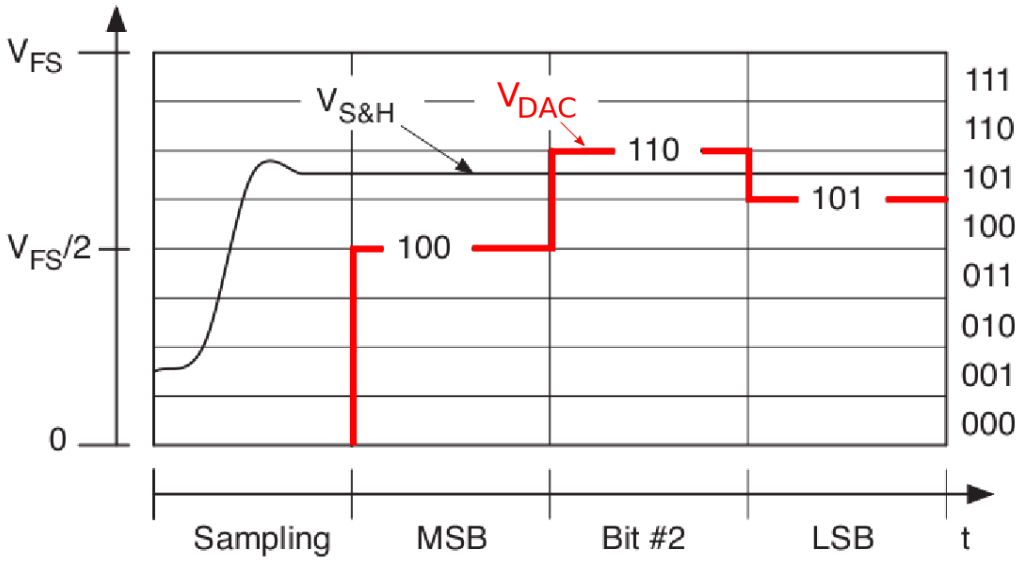
** M. Idzik, K. Swientek, T. Fiutowski, Sz. Kulis, D. Przyborowski "A 10-bit multichannel digitizer ASIC for detectors in particle physics experiments", IEEE Trans. Nucl. Sci. v.59 p.294-302 2012*

Part II: SAR ADC design and tests

- SAR ADC design
  - Fundamentals
  - DAC Switching energy
  - Other aspects - DAC capacitance, splitted DAC, asynchronous logic, dynamic comparator&logic, bootstrapped switch
- SALT project in IBM CMOS 130 nm
- LumiCal readout in IBM CMOS 130 nm
- Multichannel ADC aspects: PLL, sampling pulse, I/O SLVS, Single-to-Differential converter
- Summary

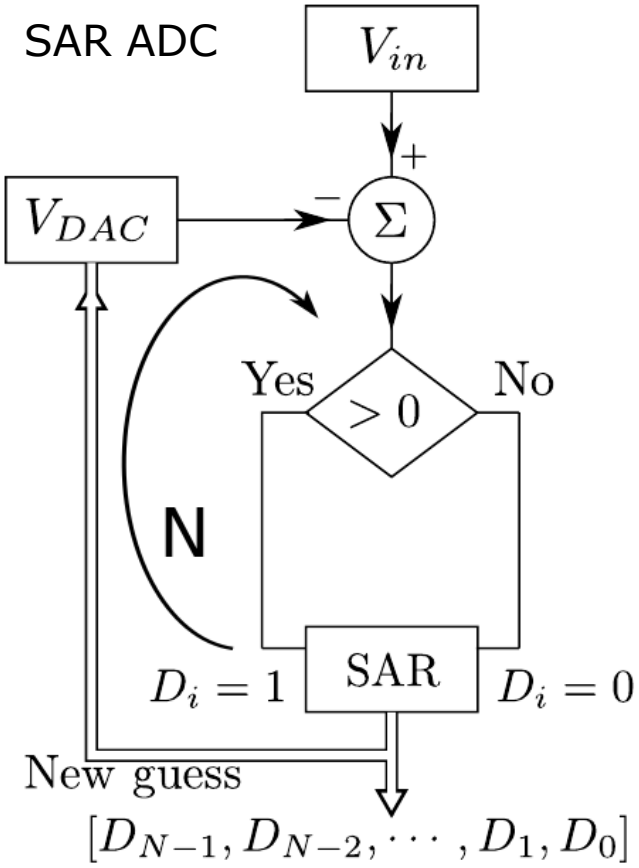
SAR architecture
Fundamentals of operation





- Comparison between sampled input voltage and reference DAC output voltage
- Comparison result → change reference DAC output voltage closer to input sample
- Each consecutive voltage change is half of the previous one
- Operation is repeated N times for N-bit ADC

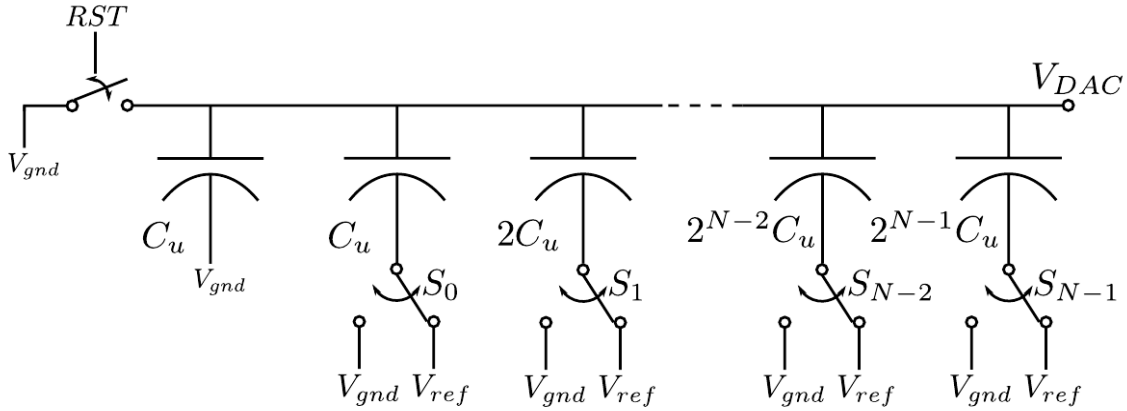
SAR architecture
Advantages and disadvantages



+ Power and area-efficient architecture – ***same circuitry is used in loop N-times***

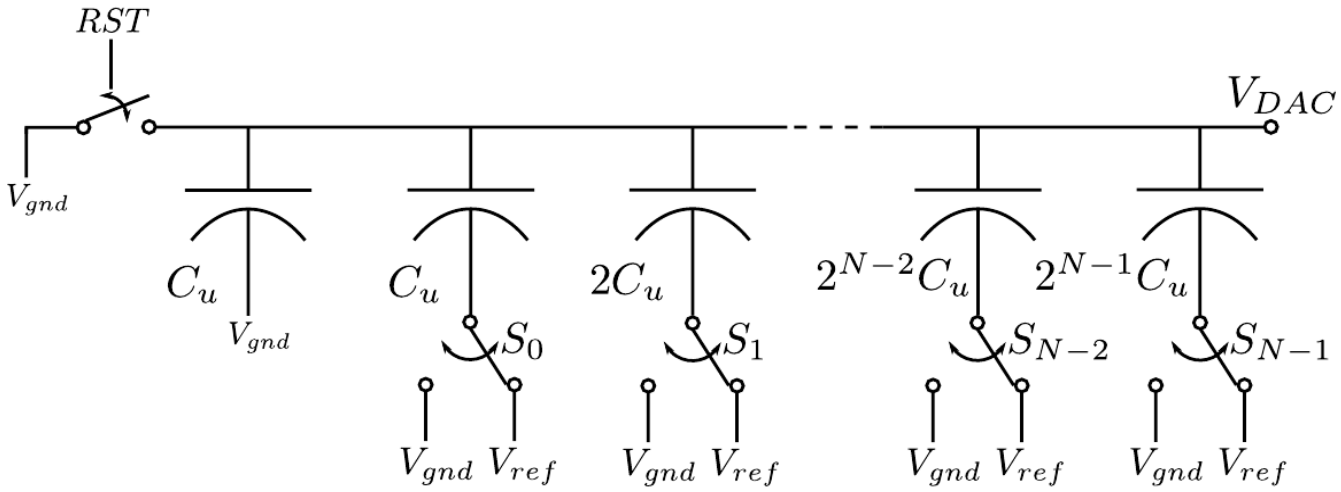
+ SAR ADC contains: single comparator, two DACs (differential) and SAR logic – ***fits well to modern digital CMOS technologies***

+ DAC network is usually capacitive - ***no static power, serves also as S/H circuit***



– Limited sampling rates – ***but with modern CMOS technology (~100nm) above 100MSps 10-bit ADCs are reported***

SAR architecture: Operation of charge scaling DAC



1) Reference voltage setting - charge scaling DAC:
   1) Bottom side of MSB (S_{N-1}) capacitor switched to V_{ref}, all others to V_{gnd} → $V_{DAC} = ½V_{ref}$
   2) Next switching depends on comparison result
      - $V_{DAC} = ¾V_{ref}$ if $V_{DAC} < V_{in}$
      - $V_{DAC} = ¼V_{ref}$ if $V_{DAC} > V_{in}$

Part II: SAR ADC design and tests

- SAR ADC design
  - Fundamentals
  - **DAC Switching energy**
  - Other aspects - DAC capacitance, splitted DAC, asynchronous logic, dynamic comparator&logic, bootstrapped switch
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- LumiCal readout in IBM CMOS 130 nm
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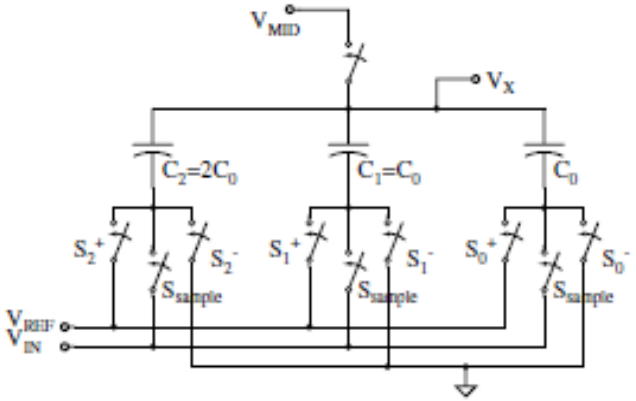
Switching energy – principle
2-bit capacitor array example



Energy drawn from Vref:

$E=V_{ref} * \Delta Q$

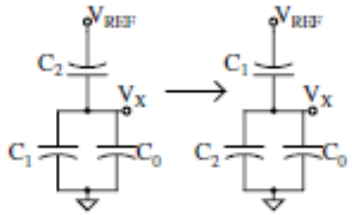
"up" transition – S_i short to V_{ref}

"down" transition - S_i short to gnd

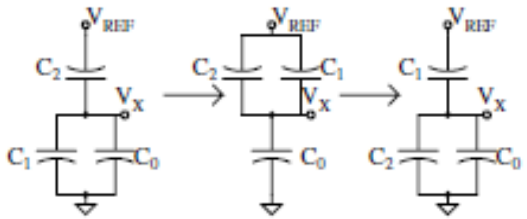
1. S_2 "up" transition: $E=C_0V^2_{ref}$

2A. If $V_{in}>V_{ref}/2$ S_1 "up" transition: $E=C_0V^2_{ref}/4$

2B. If $V_{in}<V_{ref}/2$ S_1 "down" transition:



Conventional switching:
$E=5C_0V^2_{ref}/4$



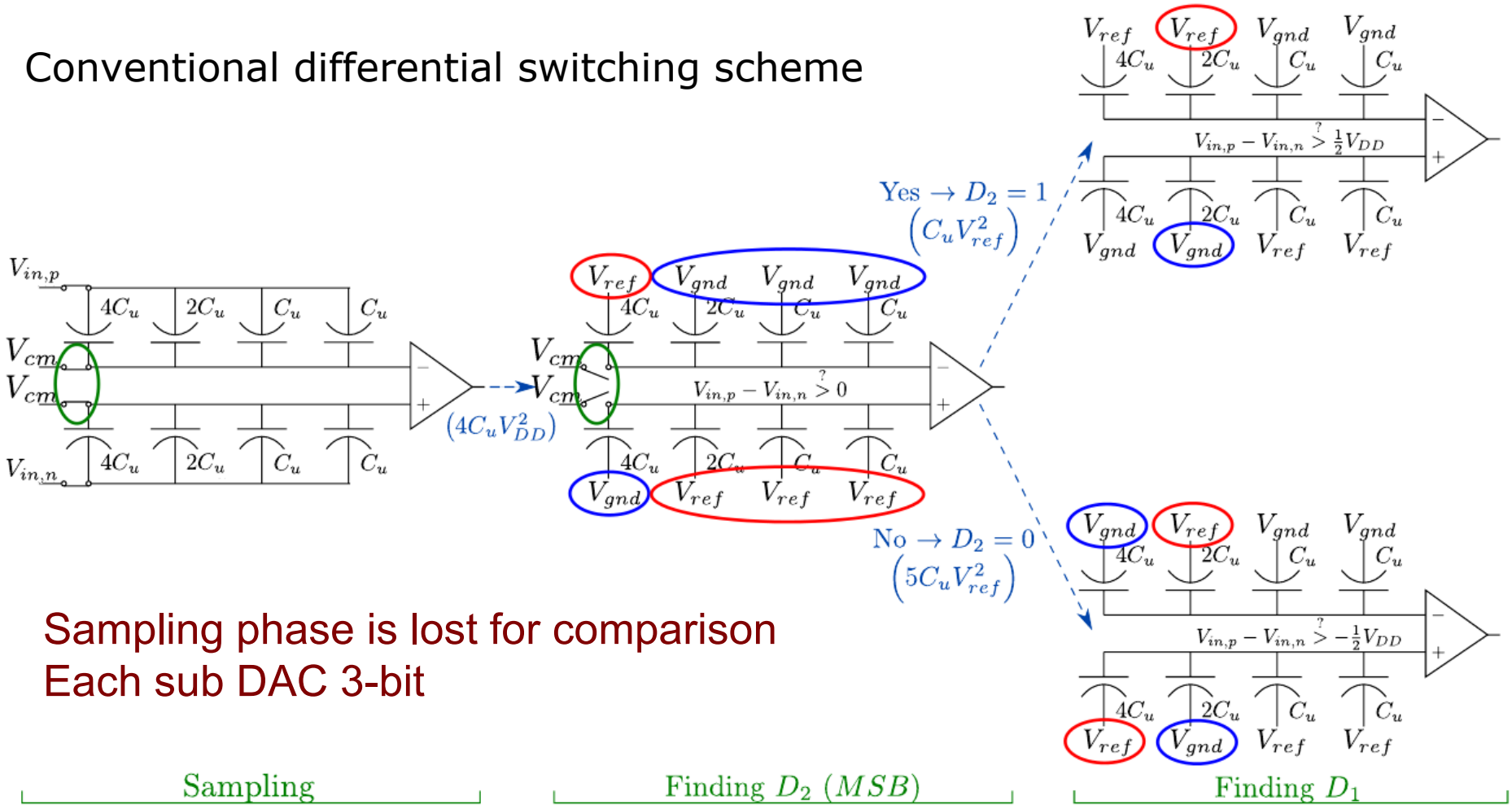
2 step switching:
$E=3C_0V^2_{ref}/4$

"down" transitions consume a lot of power...
Switching scheme can be optimized to save power in "down" transitions !

B. P. Ginsburg, A.P.Chandrakasan "An Energy-Efficient Charge Recycling Approach for SAR Converter With Capacitive DAC", IEEE Int. Symp. On Circuits and Systems, May 2005 pp. 184-187

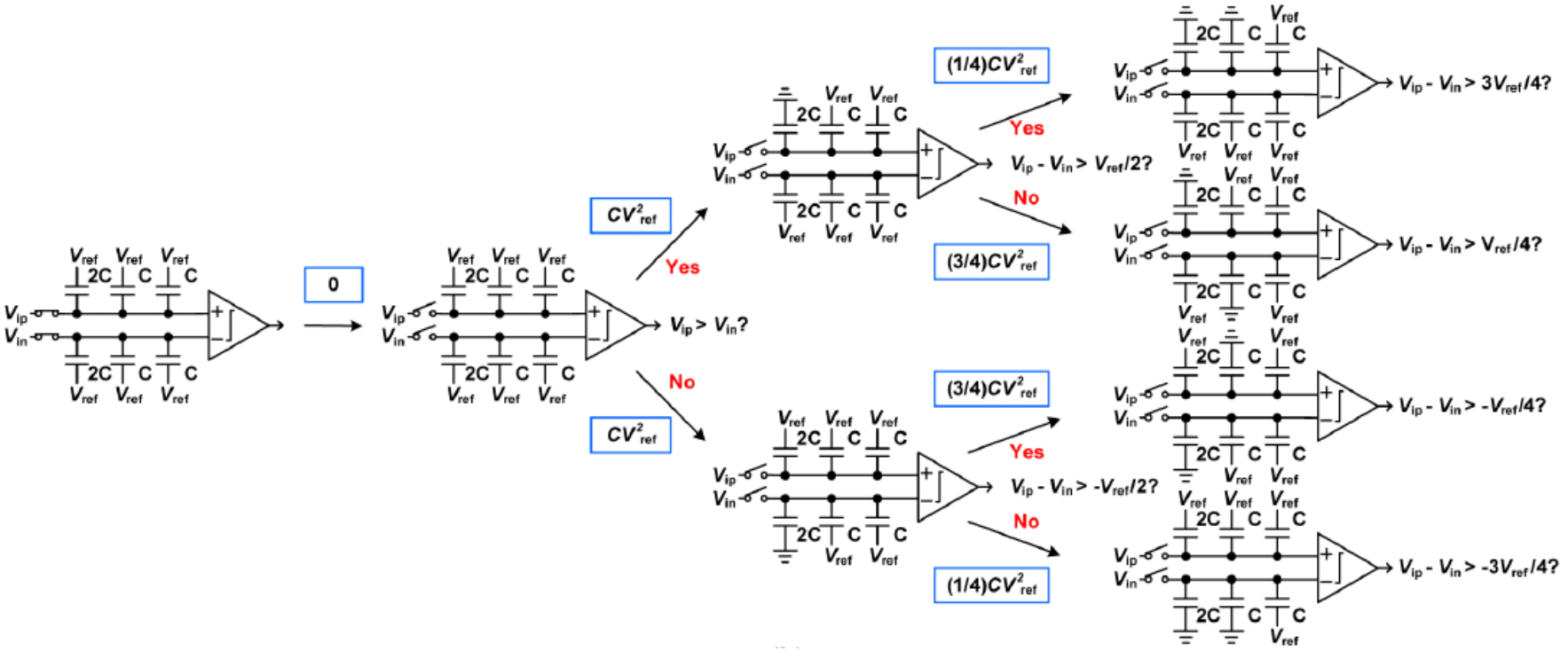
Conventional DAC in SAR ADC
Switching scheme and energy consumption
3-bit SAR ADC example

Conventional differential switching scheme



Sampling phase is lost for comparison
Each sub DAC 3-bit

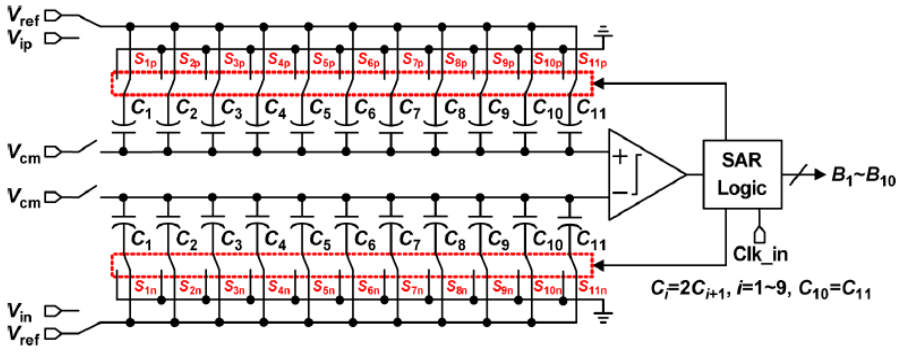
Switching energy – more efficient configurations
Set and down 3-bit SAR ADC example



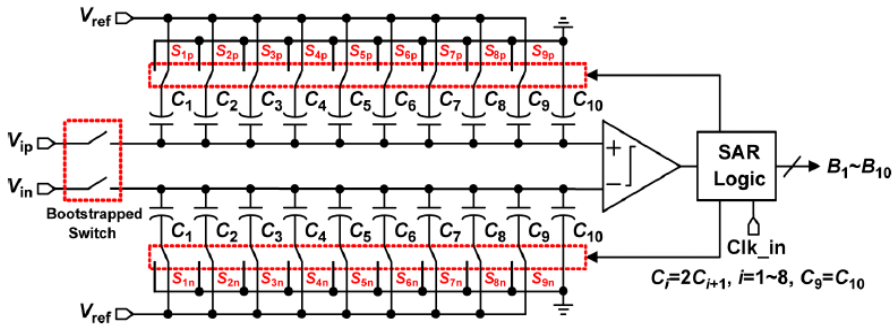
- 1st comparison after sampling ! (before any switching in DAC)
- Each sub DAC 2-bit !
- Switching energy ~81% less than conventional SAR ADC

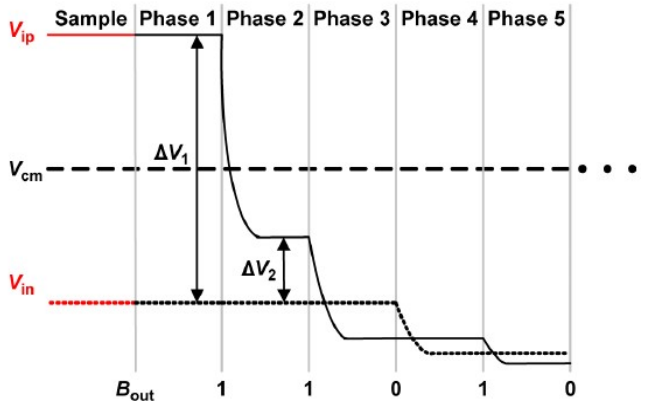
Switching energy – more efficient configurations
Set and down vs conventional

Conventional 10-bit SAR



Set and down 10-bit SAR





Set and down SAR ADC:

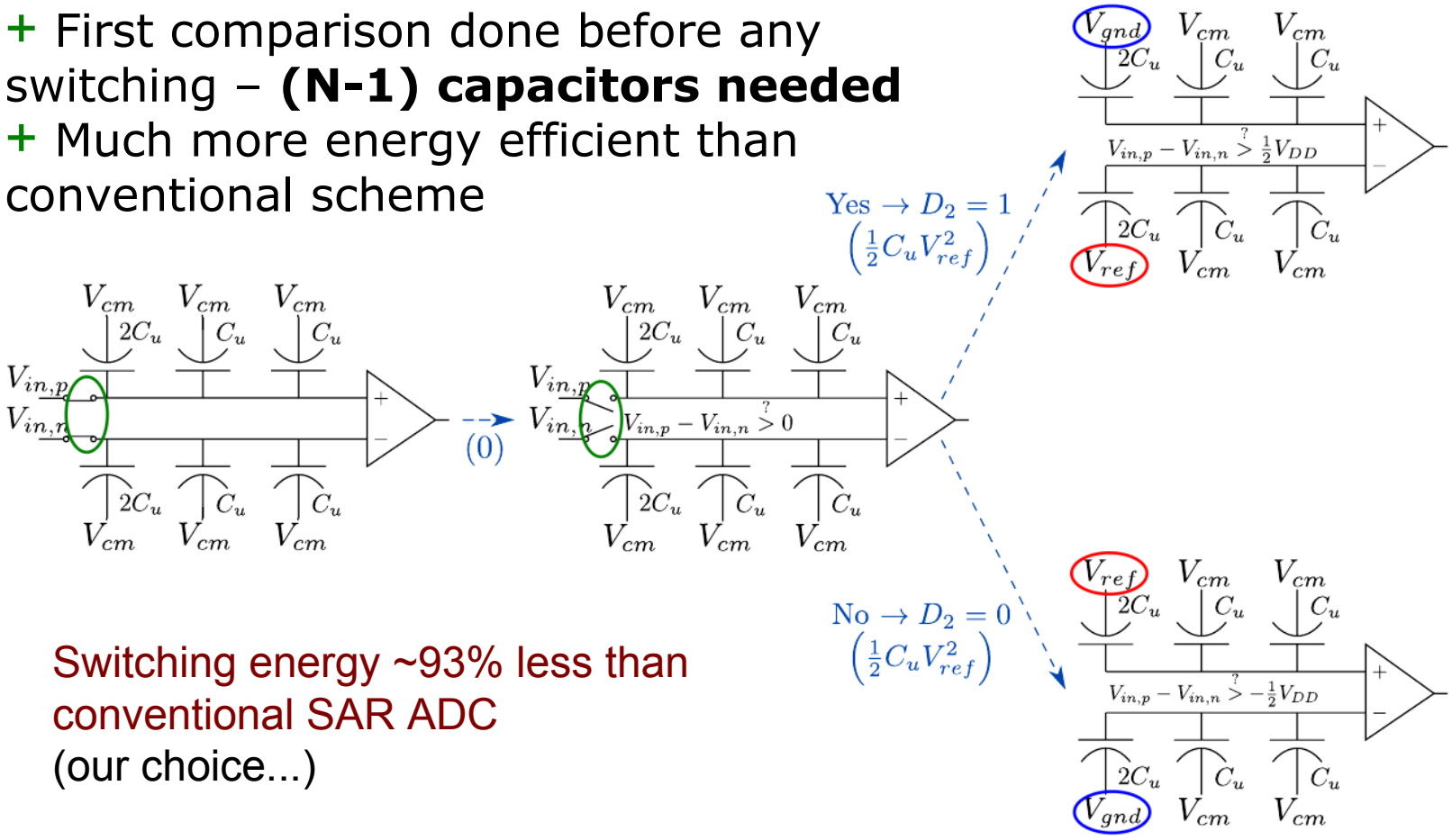
- pair of MSB capacitors less
- V_{in} sampled on top plate
- 1st comparsion done before any switching

Ch. Ch. Liu, S-J. Chang, G-Y.Huang, Y-Z. Lin "A 10-bit 50MS/s SAR ADC with a monotonic capacitor switching procedure", IEEE Journal of Solid-State Circuits v.45 pp. 731-740, April 2010

Variable common mode...

DAC in SAR ADC
Merged Capacitor Switching (MCS) scheme

+ First comparison done before any switching – **(N-1) capacitors needed**
+ Much more energy efficient than conventional scheme



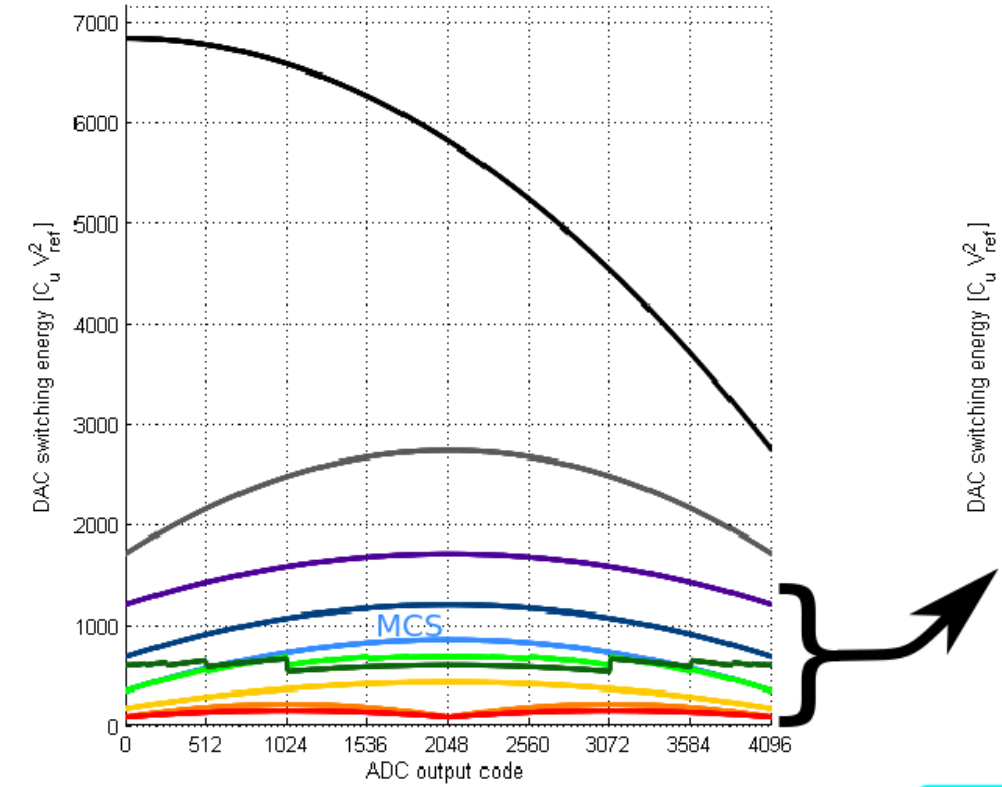
Switching energy ~93% less than conventional SAR ADC
(our choice...)

V. Hariprasath, J. Guerber, S-H. Lee, U-K. Moon "Merged capacitor switching based SAR ADC with highest switching energy-efficiency", Electronics Letterss v.46 No.9 April 2010

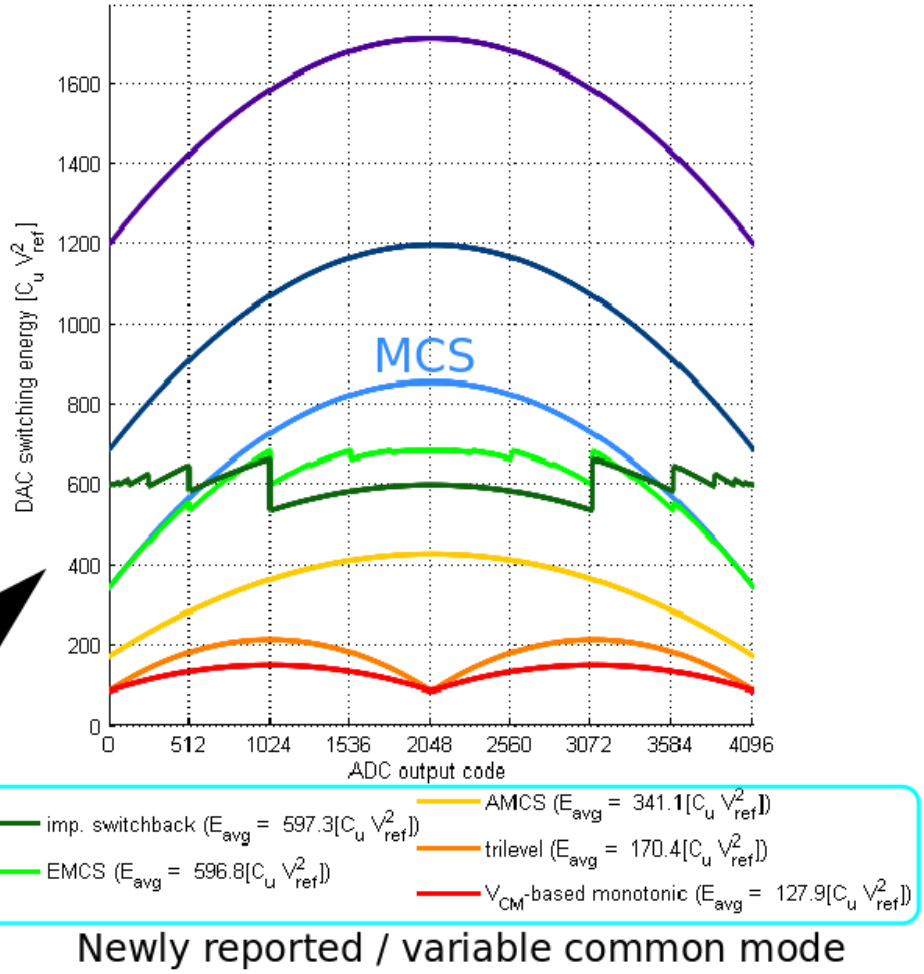
DAC switching energy in SAR ADC
Various SAR configurations

- With CMOS technology scaling digital power consumption is decreasing rapidly - so minimizing analog power (DAC, comparator) is of main interest
- Huge progress has been obtained in the last ~10 years in optimizing capacitive DAC configurations and their switching schemes
- Various DAC switching configurations were proposed
  - **Conventional (100% power consumption)**
  - 2 step switching (~10% power saving)
  - Charge sharing (~24% power saving)
  - Split capacitor (~37% power saving)
  - Energy saving (~56% power saving)
  - Set and down (~81% power saving)
  - Vcm-based (~87% power saving)
  - **Merge Capacitor Switching (MCS) (~93% power saving)**
  - During the last year some new were proposed (up to ~98% power saving)

DAC switching energy in SAR ADC
Comparison of various configurations...



Choosen scheme



Newly reported / variable common mode

Part II: SAR ADC design and tests

- SAR ADC design
  - Fundamentals
  - DAC Switching energy
  - **Other aspects - DAC capacitance, splitted DAC, asynchronous logic, dynamic comparator&logic, bootstrapped switch**
- SALT project in IBM CMOS 130 nm
- LumiCal readout in IBM CMOS 130 nm
- Multichannel ADC aspects: PLL, sampling pulse, I/O SLVS, Single-to-Differential converter
- Summary

DAC in SAR ADC
Capacitors noise area and matching

Noise

- Thermal switch noise of sampling circuit – kT/C

$$\frac{kT}{C} < \frac{\sigma^2}{12}, \sigma = \frac{V_{ref}}{2^N}$$

$$C > 12\,kT\left(\frac{2^N}{V_{ref}}\right)^2$$

- For V_{ref}=1 V:

N=6 bits	C >	0.2 fF
N=8 bits	C >	3.3 fF
N=10 bits	C >	52.0 fF
N=12 bits	C >	830.0 fF

Thermal noise is negligible for low/medium resolution

Area

Capacitance density in CMOS 130nm:

- VNCAP M1-M2 ~0.4fF/um^2
- MIMCAP ~2fF/um^2

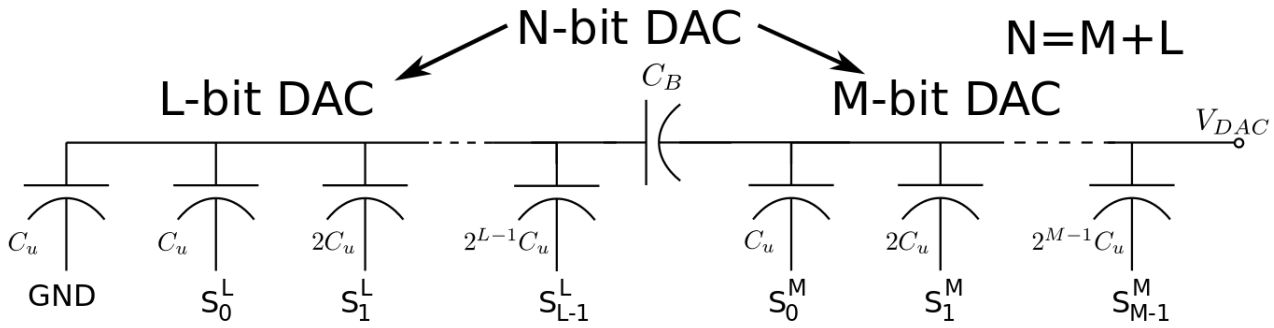
Matching

Mismatch (%) at 3σ:

- VNCAP 10x20 μm^2 (~80fF): ~5%
- MIMCAP 6x7 μm^2 (~80fF): ~0.7%
- MOM – no model exist, matching unknown...

For considered technology MIMCAP has higher density and better matching, but a problem of C_{min} appears...

DAC in SAR ADC
Splitted DAC configuration
Example for 10-bit SAR ADC



- N-bit DAC splitted into two DACs connected via series unit capacitor

M	L	C_u [fF]	C_{DAC} [pF]	No. of C_u	~Area [μm²]
9	0	5.66 → 30	15.33	512	7079
8	1	11.29 → 30	7.65	257	3553
7	2	22.5 → 30	3.81	131	1811
6	**3**	**44.64**	**2.81**	**71**	**1461**
5	4	87.87	2.72	47	1903
4	5	170.07	2.55	47	3684
3	6	317.47	2.22	71	10388
2	7	544.24	1.63	131	32857
1	8	725.65	0.73	257	85947

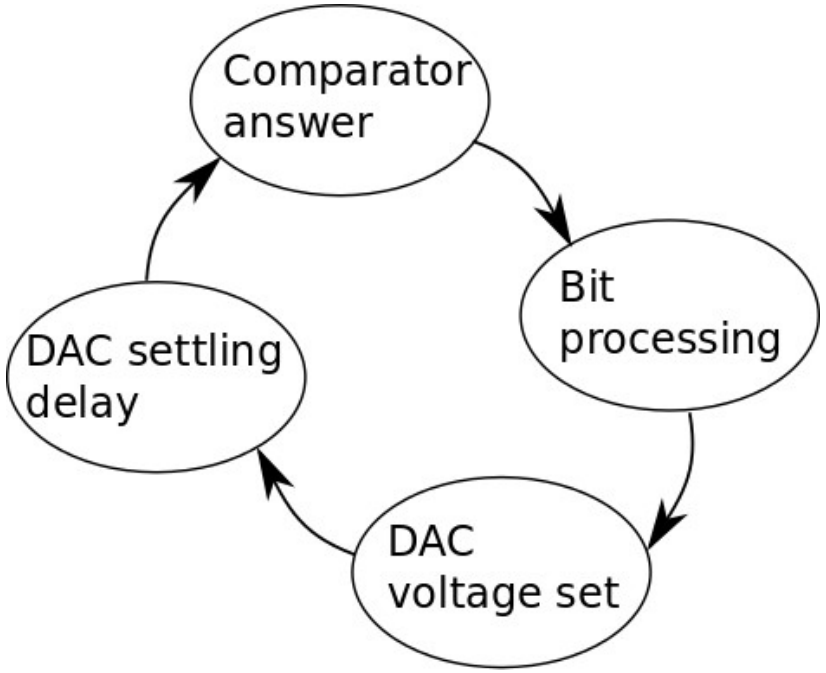
- **C_u** – minimal unit capacitance ensuring 3σ matching within 0.5LSB
Assume technology limit
C_u=30fF

$$C_u = \frac{9}{2\sqrt{2}} 2^{2L} \left(2^M - 1\right) K_\sigma^2 K_C$$

$$K_\sigma = 4.12 \frac{\%}{\mu m} \qquad K_C = 2.05\,\mu m$$

Design of SAR ADC
Asynchronous logic – no fast clock distribution

- To operate at 40MS/s 10-bit ADC has to convert single bit in approximately 2ns
- Each bit conversion require at least two clock cycles – generation and distribution of 1GHz clock is needed for synchronous operation
- Asynchronous logic → data flow releases actions in sequence



+ No fast clock distribution needed – a lot of power saved

+ Single slope of sampling signal starts the conversion → ADC can operate in **asynchronous mode**

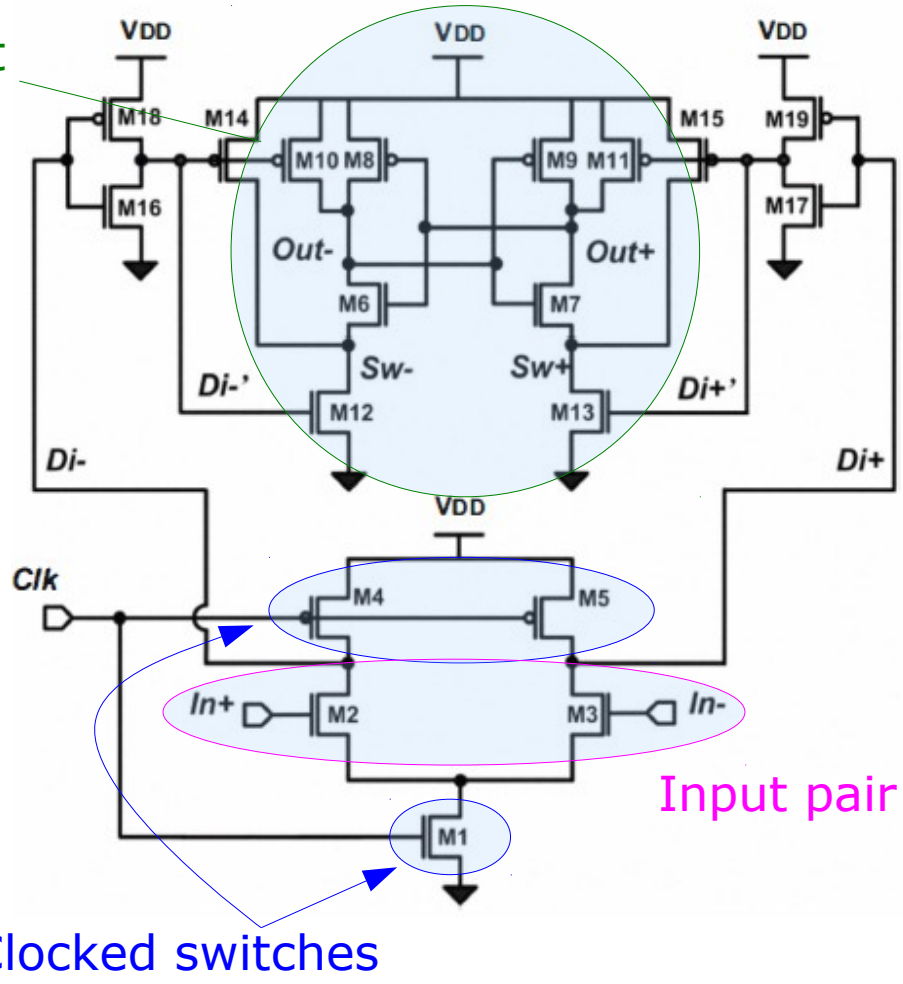
Design of SAR ADC
Dynamic comparator

Dynamic comparator

- Comparison performed on rising edge of clock signal
- Reset (low clock level) needed before next comparison

Pros and cons:

+ No direct path current
+ Low power consumption
– Dead time needed for reset



H.J. Jeon, Y-B. Kim, M. Choi "Offset voltage analysis of dynamic latched comparator", IEEE 54th Int. Midwest Symp. On Circuits and Systems, 2011

Design of SAR ADC
Dynamic logic – idea of operation

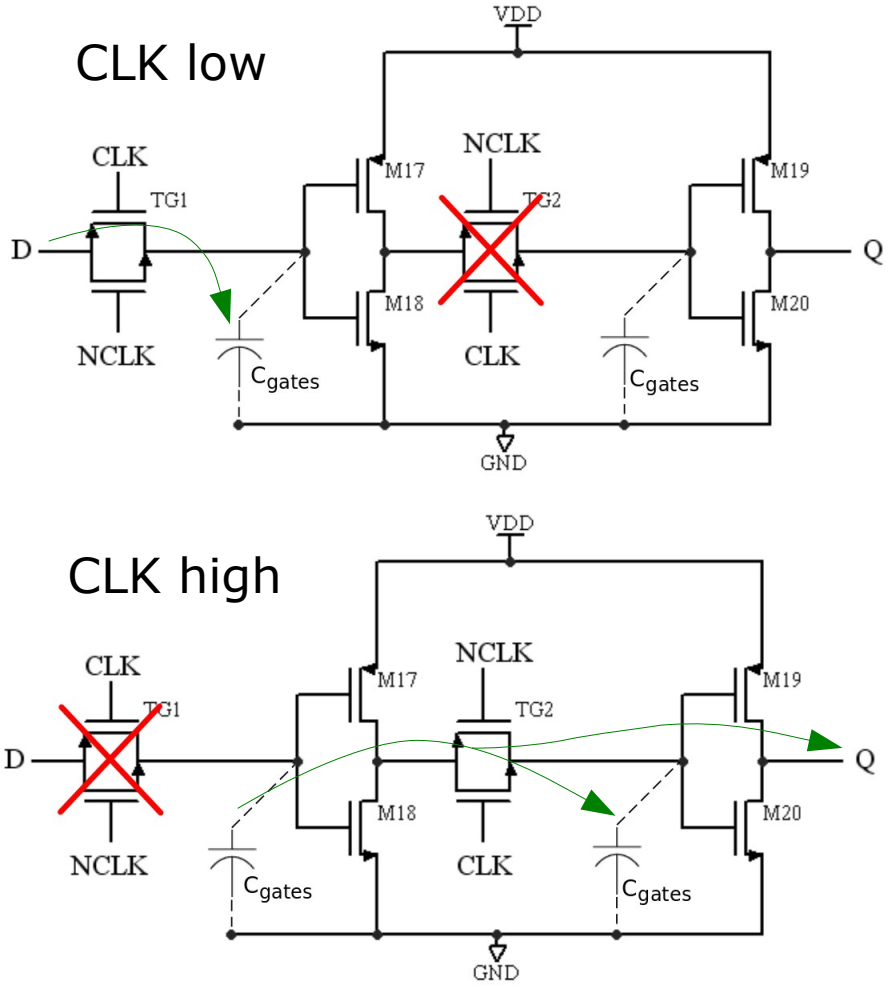
Dynamic D-type flip-flop:

- Bit (voltage level) stored on inverter gate capacitance

\+ Very fast - only two small transistor gates need to be recharged on each clock slope

– Clock needs to run continuously (or static reset is needed)

– Manual layout



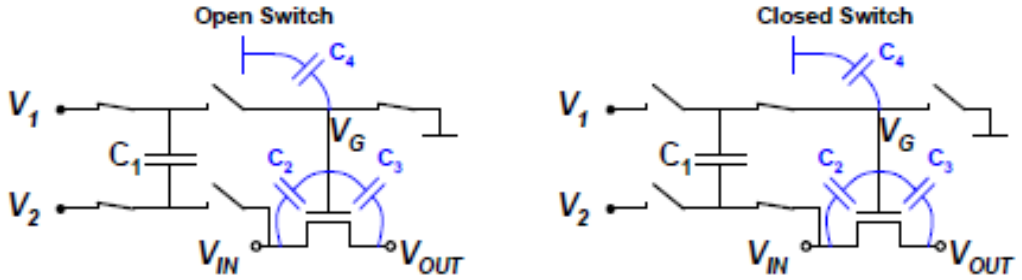
Flip-flop architecture	Signal propagation time [ps]	Power consumption [μW/clk cycle]
Static	155	2.62
Dynamic	**50**	**2.58**

Dynamic flip-flop is 3 times faster

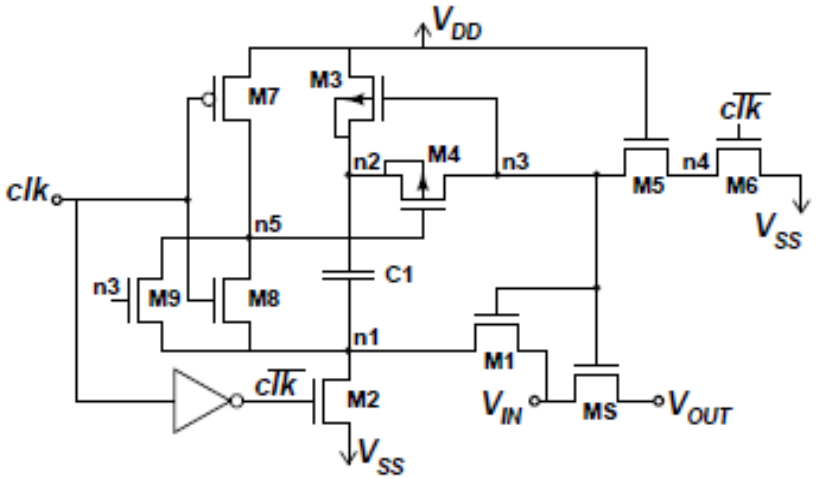
Design of SAR ADC
Bootstrapped S/H switch

How to minimize signal distortion during sampling phase ?

Idea



Implementation

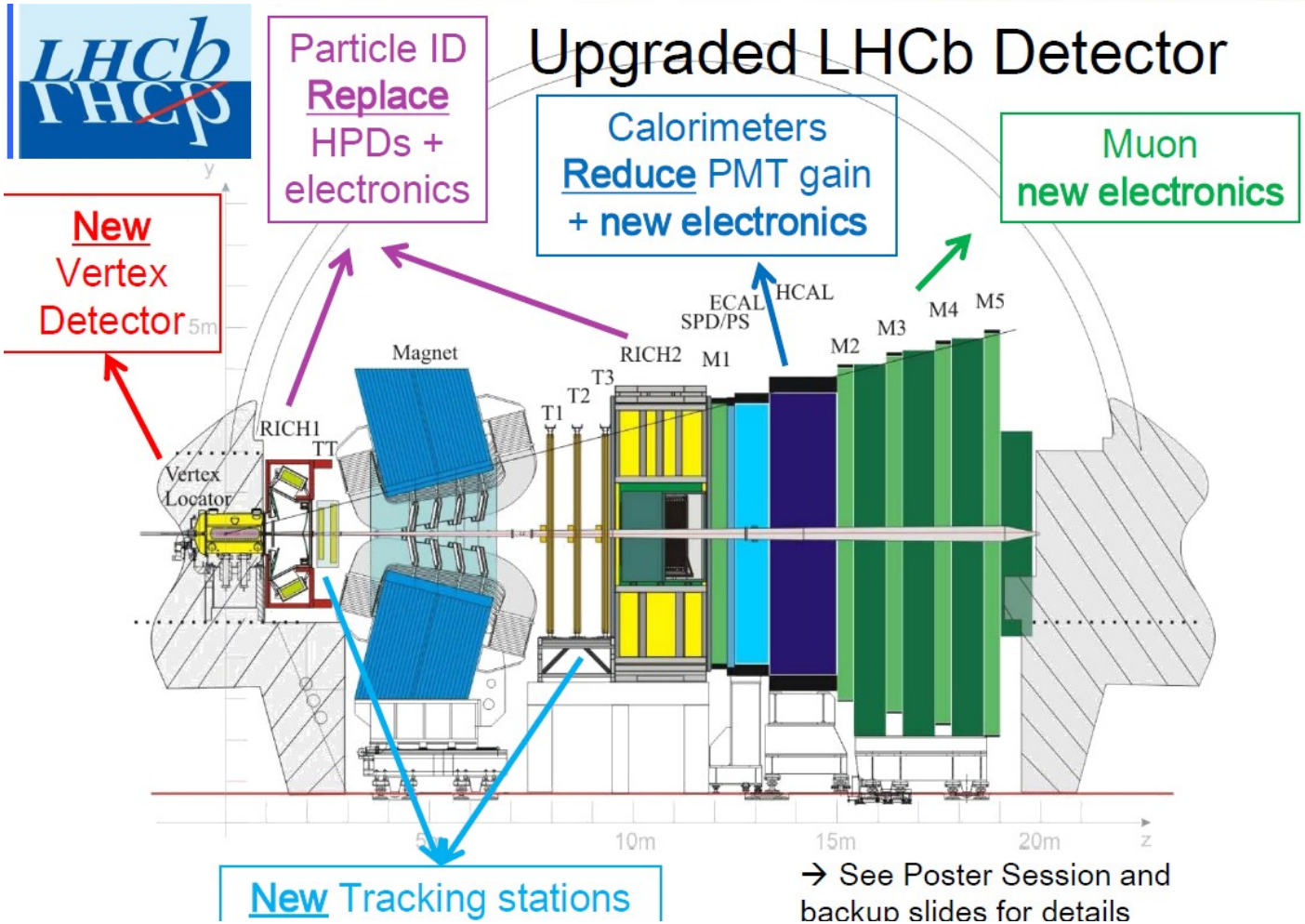


M. Dessouky, A. Kaiser, "Input switch configuration for rail-to-rail operation of switched opamp circuits",Electronics Letters vol. 35 no. 1 pp. 8-10 January 1999

Part II: SAR ADC design and tests

- SAR ADC design
  - Fundamentals
  - DAC Switching energy
  - Other aspects - DAC capacitance, splitted DAC, asynchronous logic, dynamic comparator&logic, bootstrapped switch
- **SALT project in IBM CMOS 130 nm**
- LumiCal readout in IBM CMOS 130 nm
- Multichannel ADC aspects: PLL, sampling pulse, I/O SLVS, Single-to-Differential converter
- Summary

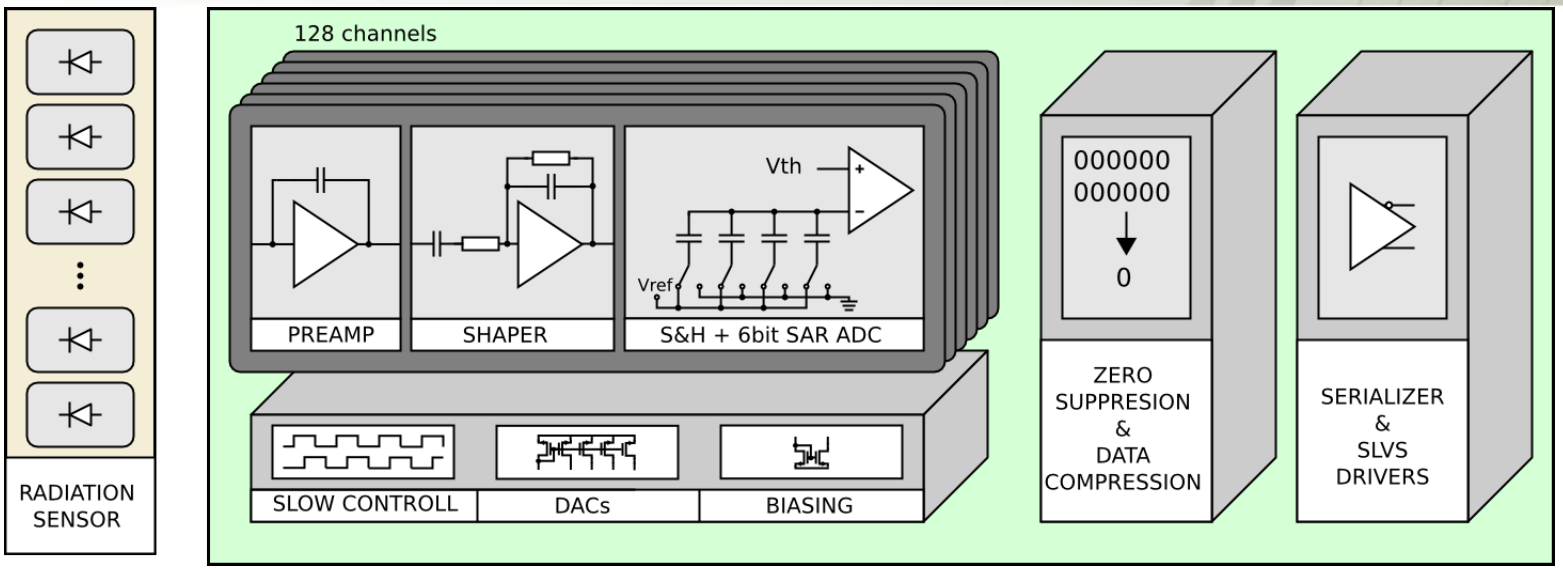
LHCb Tracker System Upgrade



- To increase trigger rate from 1MHz to 40MHz new readout electronics needed in LHCb Tracking System
- Silicon Upstream Tracker (old TT) will need ~0.5 million readout channels

F. Alessio "Trigger-less readout architecture for the upgrade of the LHCb experiment at CERN", TWEPP2013 23-27 September 2013, Perugia Italy

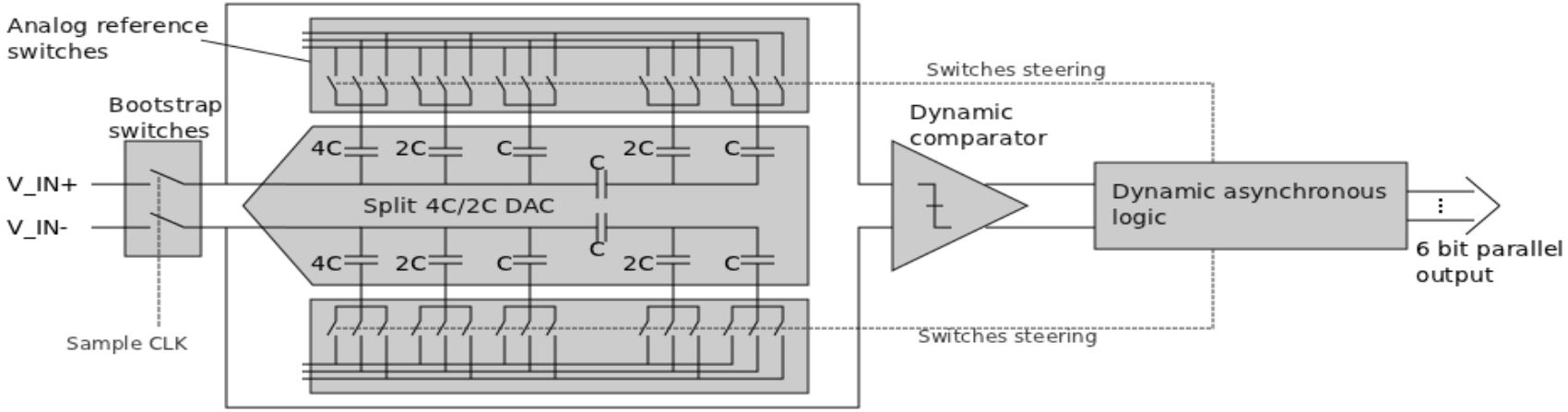
SALT- readout ASIC for LHCb silicon strips



- Complex System on Chip (SoC) ASIC
  - 128 channels
  - Preamplifier-shaper, 6-bit ADC, zero supp., serialization, fast data transmissiion
  - Pitch ~40um
- CMOS IBM 130 nm technology

K. Świentek, M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, T. Szumlak "SALT – new silicon strip readout chip for the LHCb Upgrade", TWEPP2013 23-27 September 2013, Perugia Italy

6-bit SAR ADC
Architecture&Design considerations



Architecture of 6-bit ADC

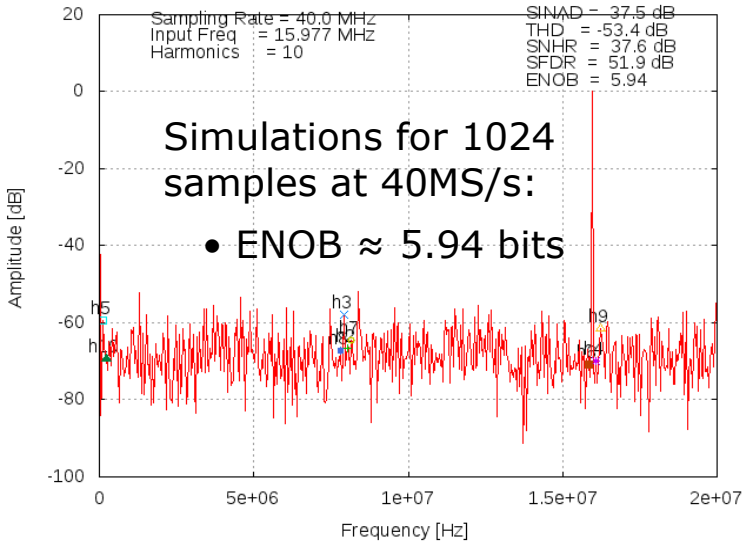
- Differential segmented/split DAC with MCS switching scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption, power pulsing for free***
- Asynchronous logic – no clock tree – ***power saving, allows asynchronous sampling***
- Dynamic SAR logic – ***much faster than conventional static logic***

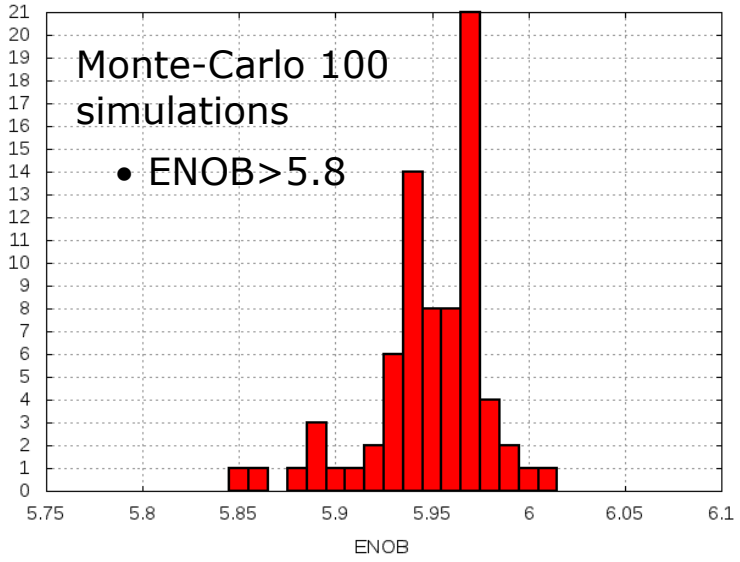
Design consideration:

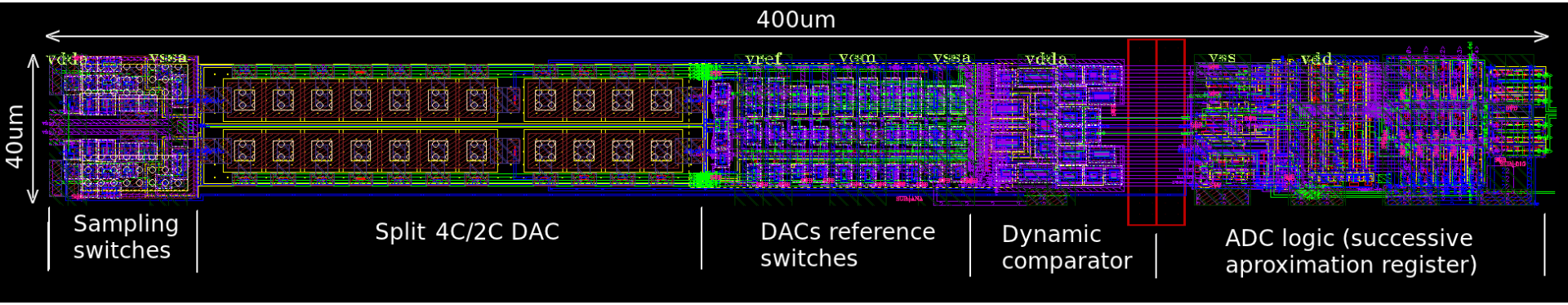
- Variable sampling frequency (up to ~90 MS/s) and power consumption
- Power consumption ~0.3 mW at 40 MS/s
- 40 µm pitch, ready for multichannel integration

K. Świentek, M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, T. Szumlak "SALT – new silicon strip readout chip for the LHCb Upgrade", TWEPP2013 23-27 September 2013, Perugia Italy

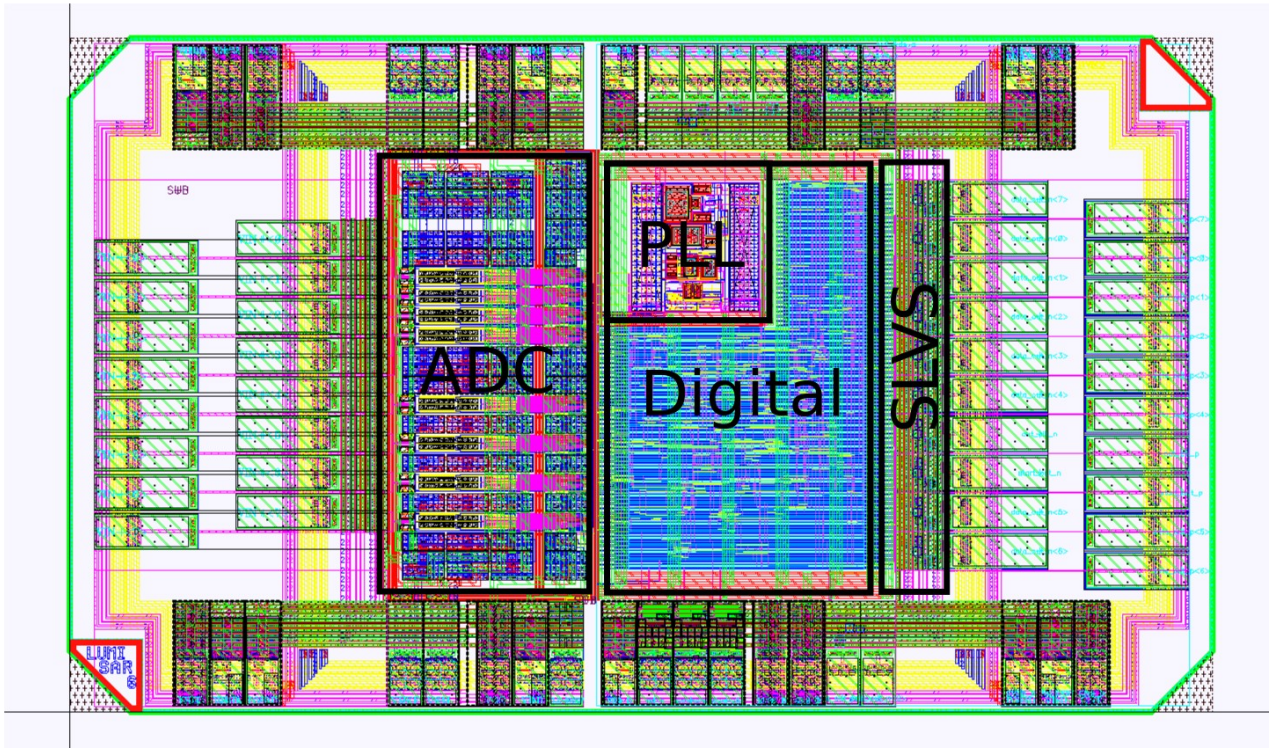
6-bit SAR ADC
Post-layout simulations







6-bit SAR ADC
Prototype ASIC integration



2340um x 1380um

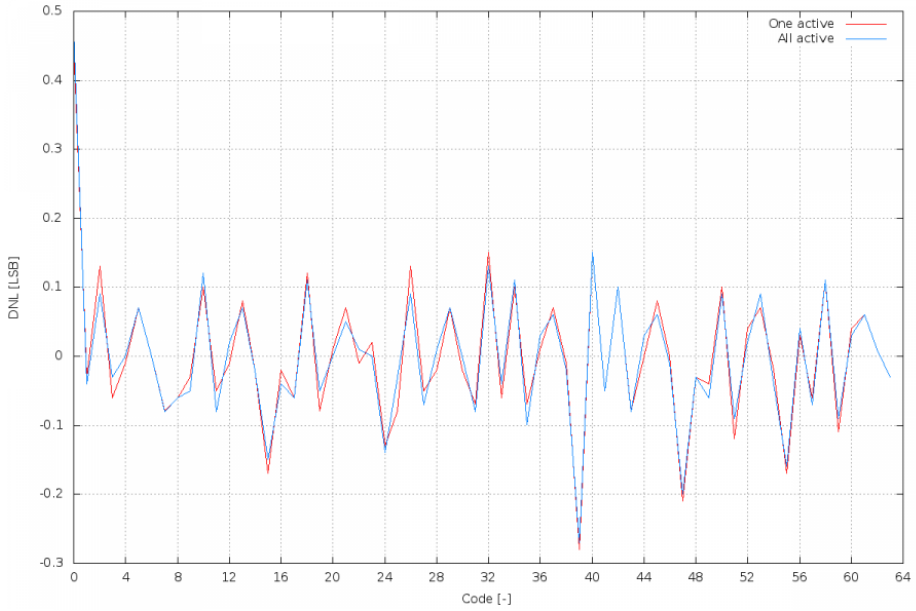
ADC prototype contains:

- 8 channels of 6-bit SAR ADC in 40um pitch
- Multiplexing&Serialization circuitry
- PLL prototype (discussed later...)
- SLVS I/O circuitry (discussed later...)
- Staggered pads

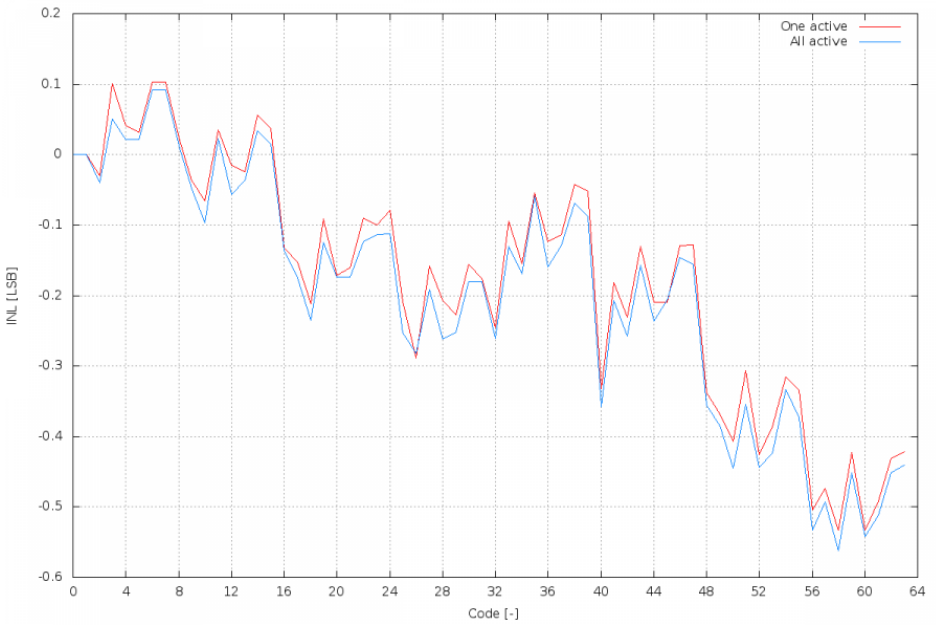
Prototypes were fabricated in 2012. Development of FPGA based test setup has taken long time. First part of measurements has been completed in October 2013

6-bit SAR ADC
Static tests – linearity

DNL@50MHz



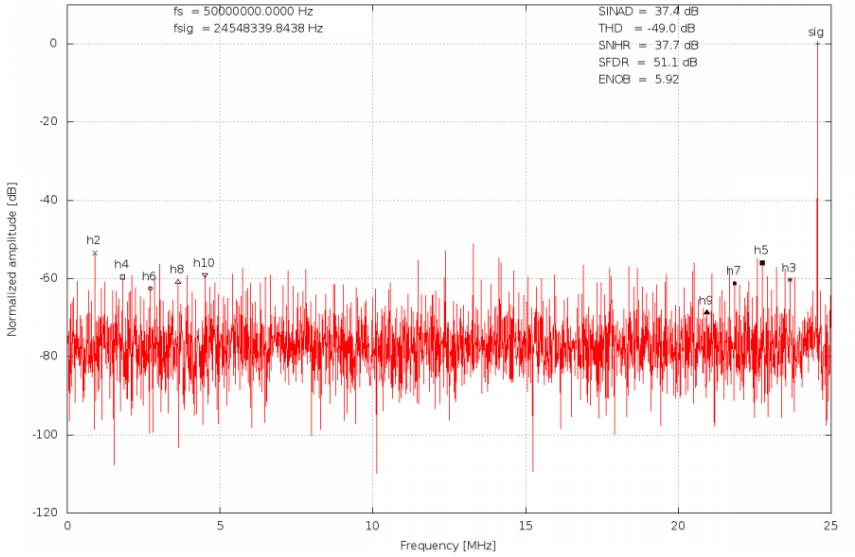
INL@50MHz



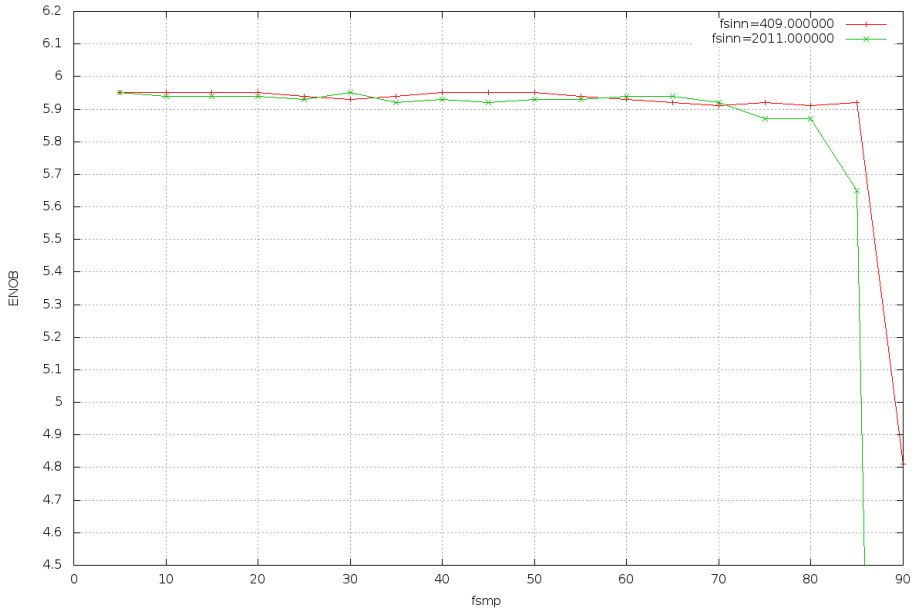
First measurements show that ADC is working very well. At 50MHz sampling frequency good linearity INL, DNL < 0.5 is seen.

6-bit SAR ADC
Dynamic tests – ENOB effective resolution

Example Fourier spectra @50MHz sampling



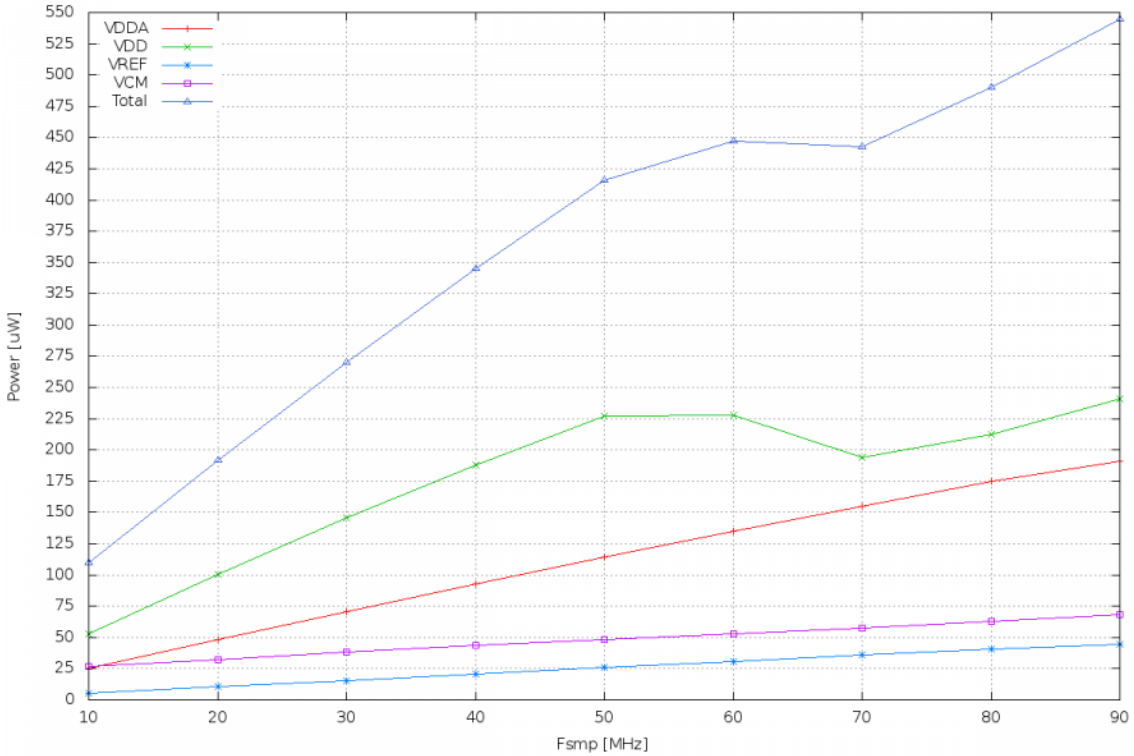
Scan vs sampling frequency



Measurements show very good dynamic behaviour. The measured ENOB is between 5.7 – 5.9 bits. The ADC works well for sampling frequencies beyond 80 MHz.

6-bit SAR - test results
Power consumption

Example power measurements vs sampling frequency



The 6-bit ADC sampling at 40MHz consumes much less than the front-end !

FOM ~ 150 fJ/conv

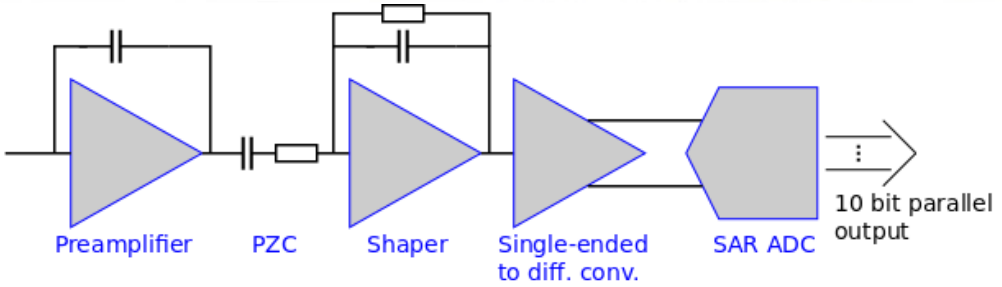
At 40 MHz sampling the total power consumption is around 350uW.

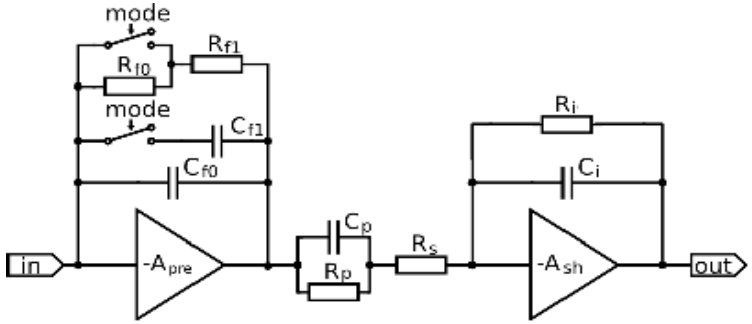
Part II: SAR ADC design and tests

- SAR ADC design
  - Fundamentals
  - DAC Switching energy
  - Other aspects - DAC capacitance, splitted DAC, asynchronous logic, dynamic comparator&logic, bootstrapped switch
- SALT project in IBM CMOS 130 nm
- **LumiCal readout in IBM CMOS 130 nm**
- Multichannel ADC aspects: PLL, sampling pulse, I/O SLVS, Single-to-Differential converter
- Summary

New readout electronics for luminosity calorimeter in IBM CMOS 130 nm Design and technology comparison

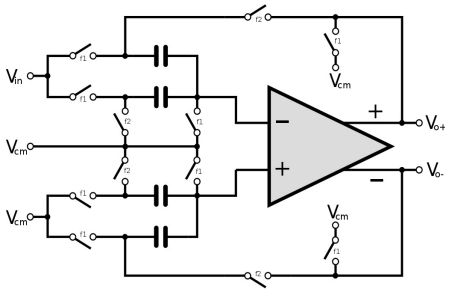
New readout in 130 nm has very similar architecture to existing one in 0.35um but should consume much less power and be radiation resistant





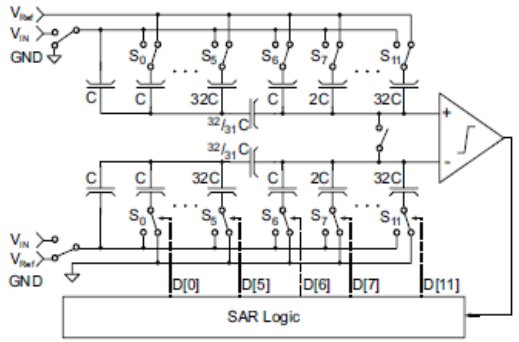
Front-end specs:

- Cdet ≈ 5 ÷ 50pF
- 1st order shaper (Tpeak ≈ 50 ns)
- Variable gain, two modes:
  - calibration: MIP sensitivity
  - physics: Q_{in} up to ~6 pC
- Power pulsing
- Peak power cons. **~1.5 mW**/channel (in AMS 0.35um it was **~9mW**)



Single-to-Diff specs:

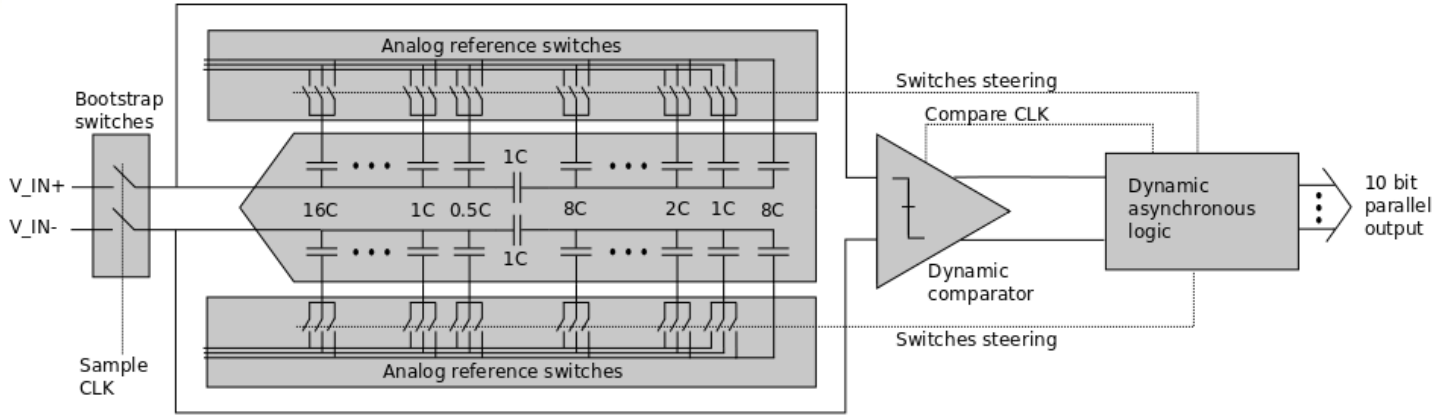
- Max freq. > 40MHz
- Power pulsing
- Peak power ~ 0.5mW



ADC specs:

- 10-bit resolution
- Architecture: SAR ADC
- Max frequency > 40 MHz
- Power pulsing
- Peak power ~ 1 mW @40MHz (in AMS 0.35u mit would be > 40mW)

Design of SAR ADC
Chosen architecture of 10-bit SAR ADC



Architecture of 10-bit ADC

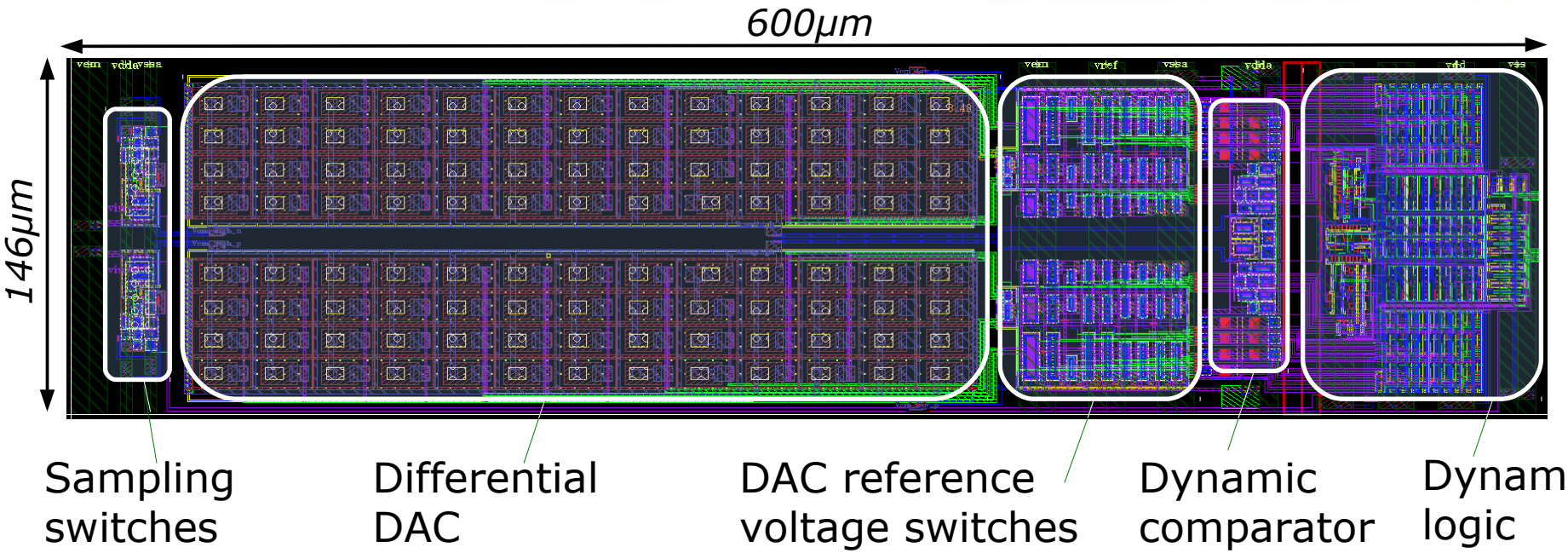
- Differential segmented/split DAC with MCS switching scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption, power pulsing for free***
- Asynchronous logic – no clock tree – ***power saving, allows asynchronous sampling***
- Dynamic SAR logic – ***much faster than conventional static logic***
- Bootstrapped sampling switch – ***improves linearity***

Design consideration:

- Variable sampling frequency (up to ~50 MS/s) and power consumption
- Power consumption ~1 mW at 40 MS/s
- 146 µm pitch, ready for multichannel integration

J. Moron, M. Firlej, T. Fiutowski, M. Idzik, Sz. Kulis, K. Swientek. "Development of variable sampling rate low power 10-bit SAR ADC in IBM 130 nm technology", TWEPP2013 23-27 September 2013, Perugia Italy

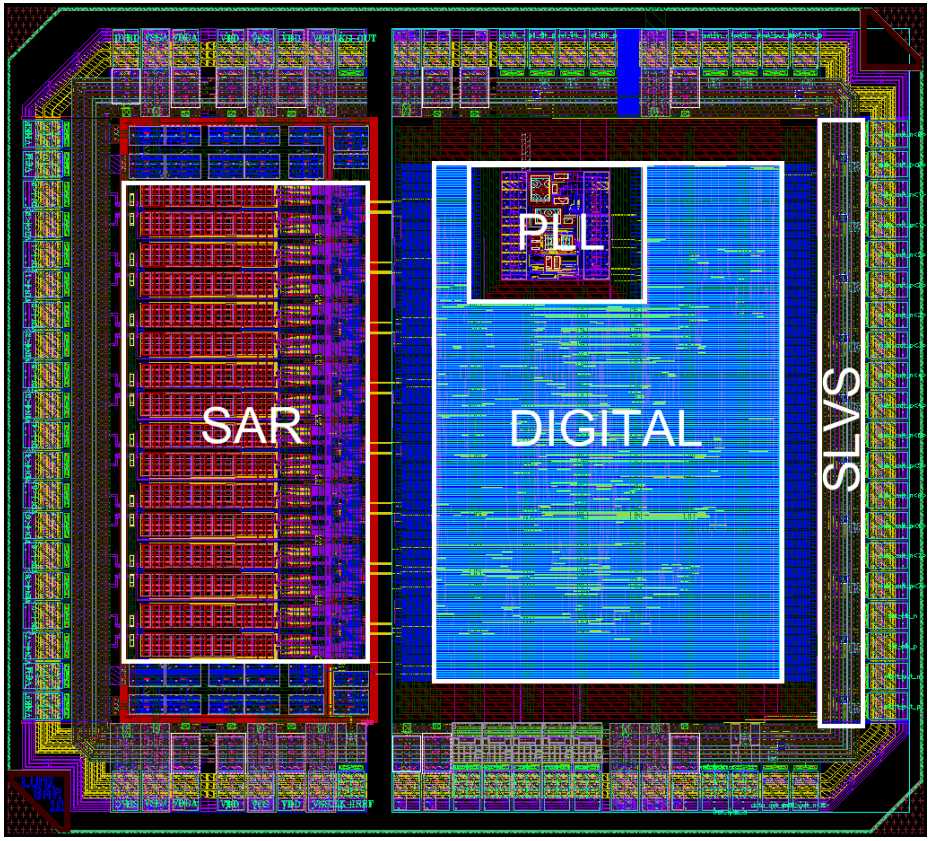
Design of 10-bit SAR in IBM 130nm



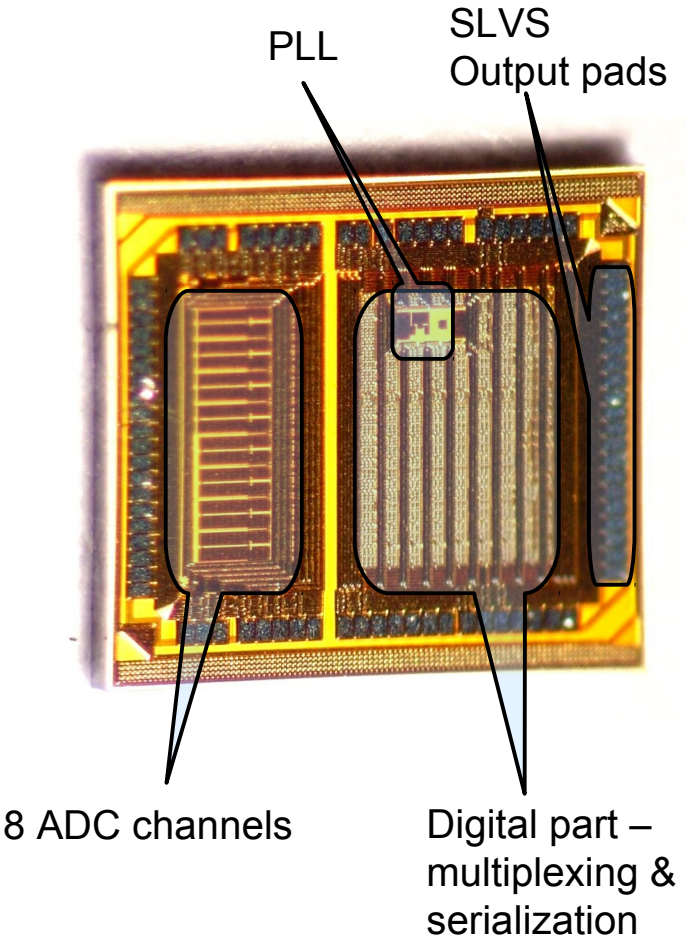
Main features of ADC in IBM 130 nm

- Simulated ENOB ≈ 9.5-9.7 bits
- Maximum sampling rate ~50 MS/s
- Power consumption ≈ 1-1.4mW @ 40 MS/s
- No dummy capacitors in DAC network!

8 channel 10-bit SAR ADC in IBM 130 nm

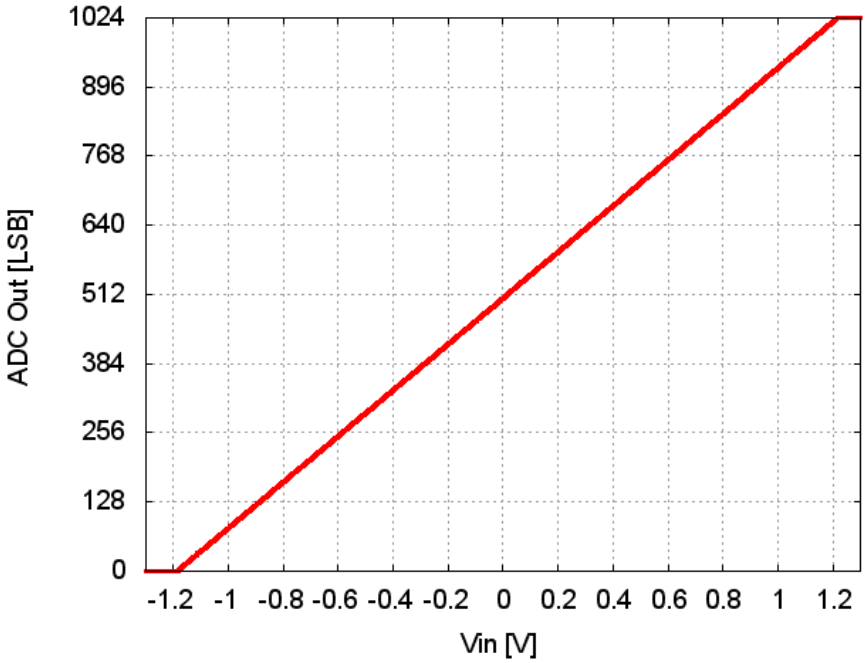


2200um x 2000um

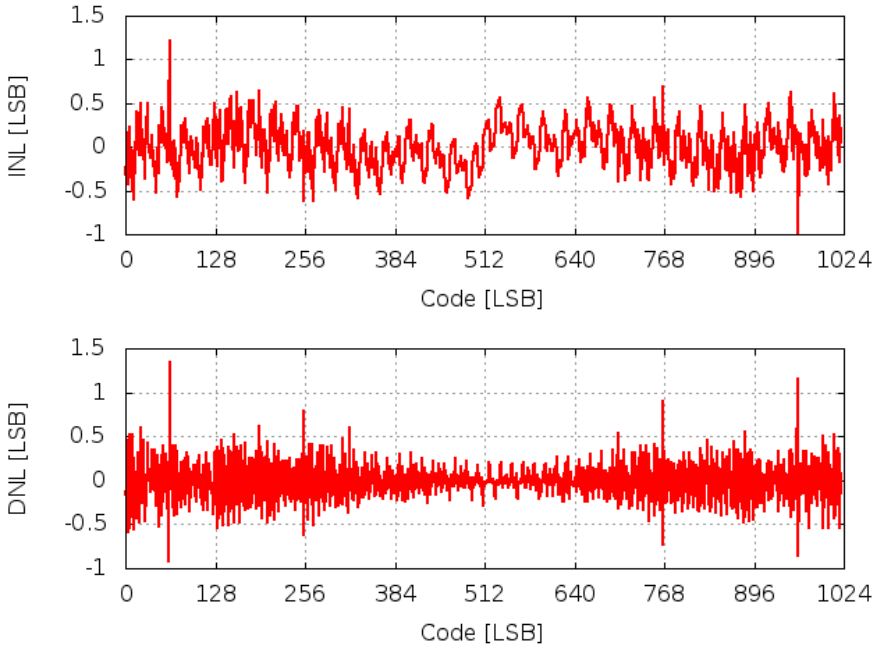


Measurements results
10-bit SAR ADC - Static measurements

Transfer function



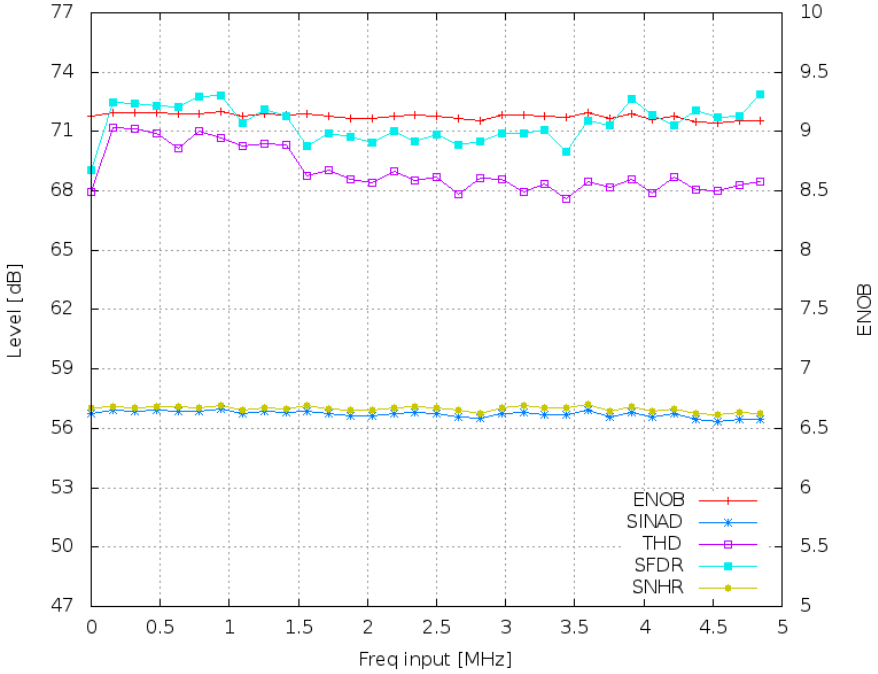
INL/DNL measurements

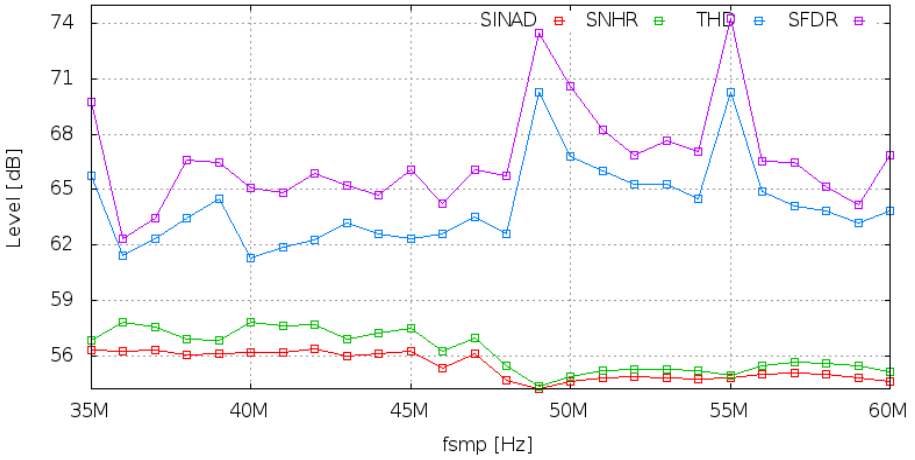


- ADC is alive and works in the whole input signal range
- There are some codes with worse linearity (some improvements in DAC layout are needed)

Measurements results: Dynamic measurements

Dynamic measurements @10MHz

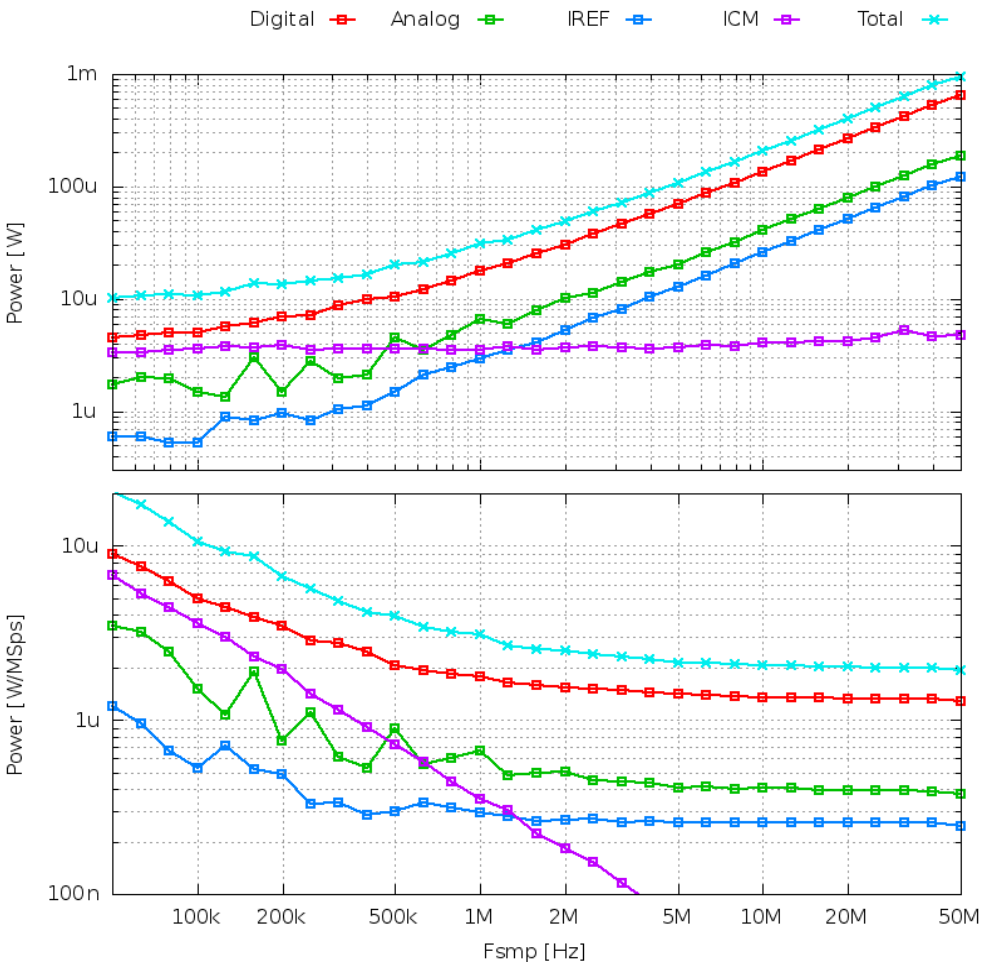




ENOB~9.2 up to Nyquist input frequency for f_{sample} ~20MHz

ADC works for f_{sample} up to about 60MHz, but above 20 MHz ENOB start to decrease. Problem with jitter found..., will be fixed in next submission.

Measurements results of 10-bit SAR ADC
Power consumption

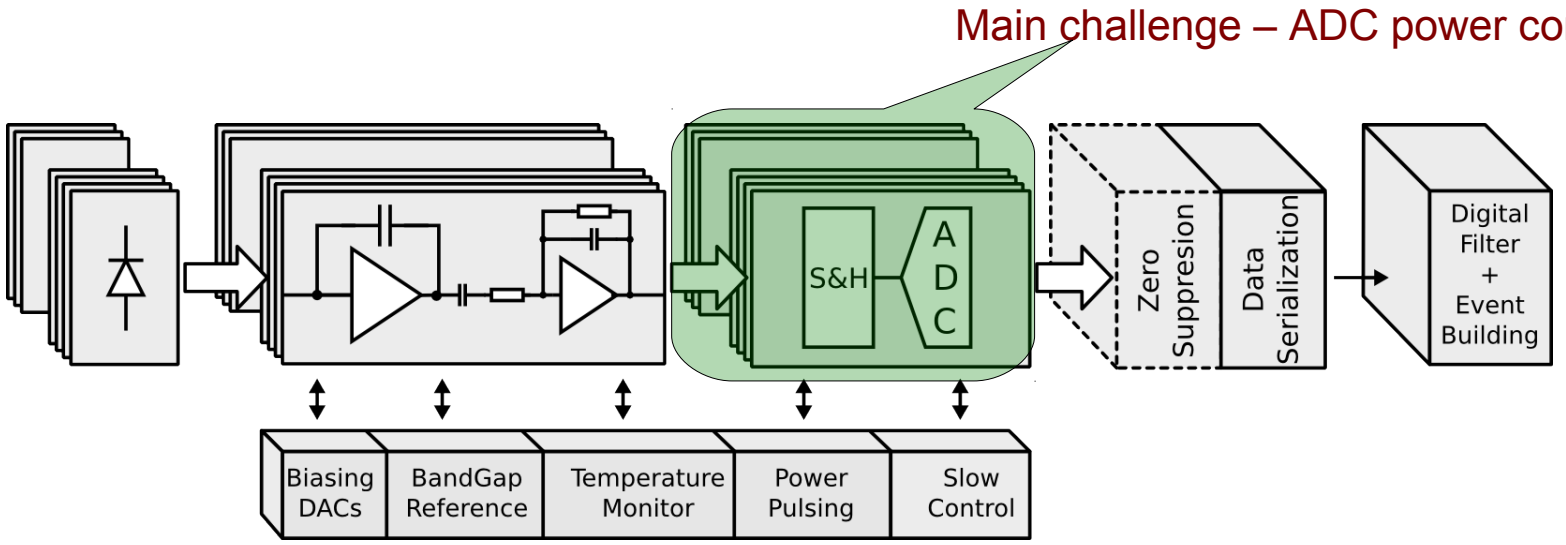


- Power consumption **~ 1 mW** per channel at 40 MS/s (**40 times less than pipeline ADC in AMS 0.35um**)
- 10-bit ADC sampling at 40MHz consumes less than the front-end !
- FOM ~ 50fJ/conv.

Part II: SAR ADC design and tests

- SAR ADC design
  - Fundamentals
  - DAC Switching energy
  - Other aspects - DAC capacitance, splitted DAC, asynchronous logic, dynamic comparator&logic, bootstrapped switch
- SALT project in IBM CMOS 130 nm
- LumiCal readout in IBM CMOS 130 nm
- **Multichannel ADC aspects: PLL, sampling pulse, I/O SLVS, Single-to-Differential converter**
- Summary

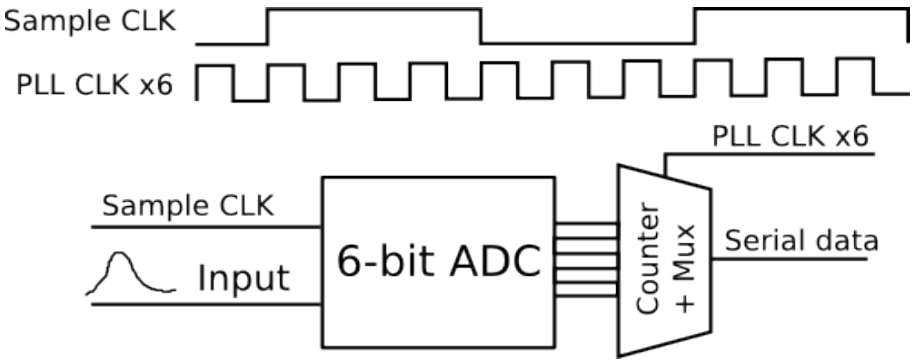
Multichannel ADC aspects



Multichannnel readout with ADC conversion becomes real SoC (System on Chip) and needs peripheral circuits:

- PLL/DLL for data multiplexing&serialization, DACs , Slow control eg. SPI or I2C, voltage reference (bandgap), temperature sensor (PTAT), I/O circuits like LVDS/SLVS, DSP, etc...

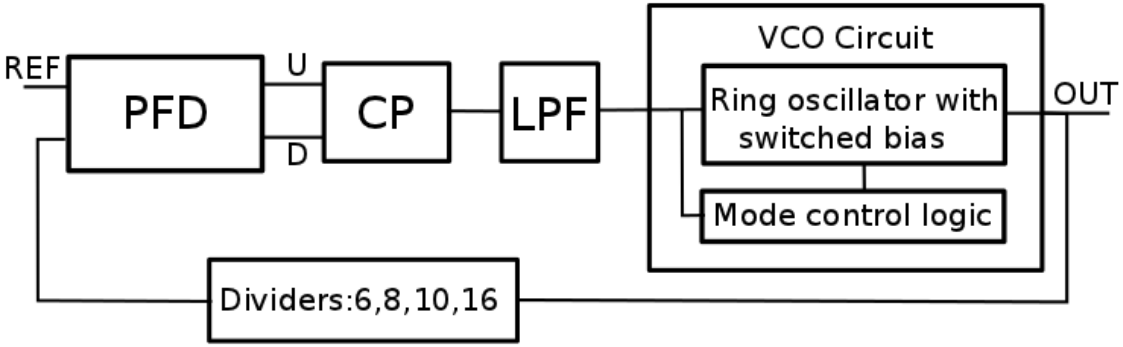
Multichannel ADC aspects
Phase-Locked Loop (PLL) - key block for high speed clock generation and data serialization

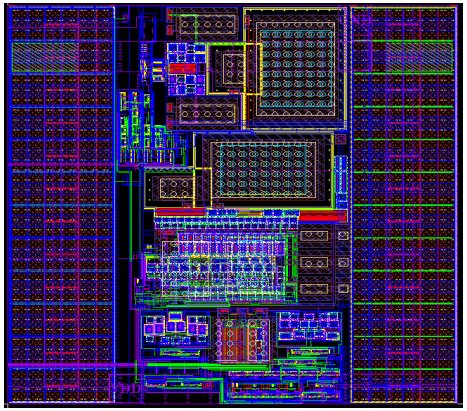


Example PLL needed to multiply sampling CLK frequency by 6

- Flexible PLL needed for data serialization in future readouts
  - different division factors needed for 6(10)-bit ADCs and maybe also for different numbers of ADC channels
  - variable frequency PLL needed for different sampling rate ADC
- Low power consumption is default requirement

Multichannel ADC aspects PLL design in IBM 130 nm





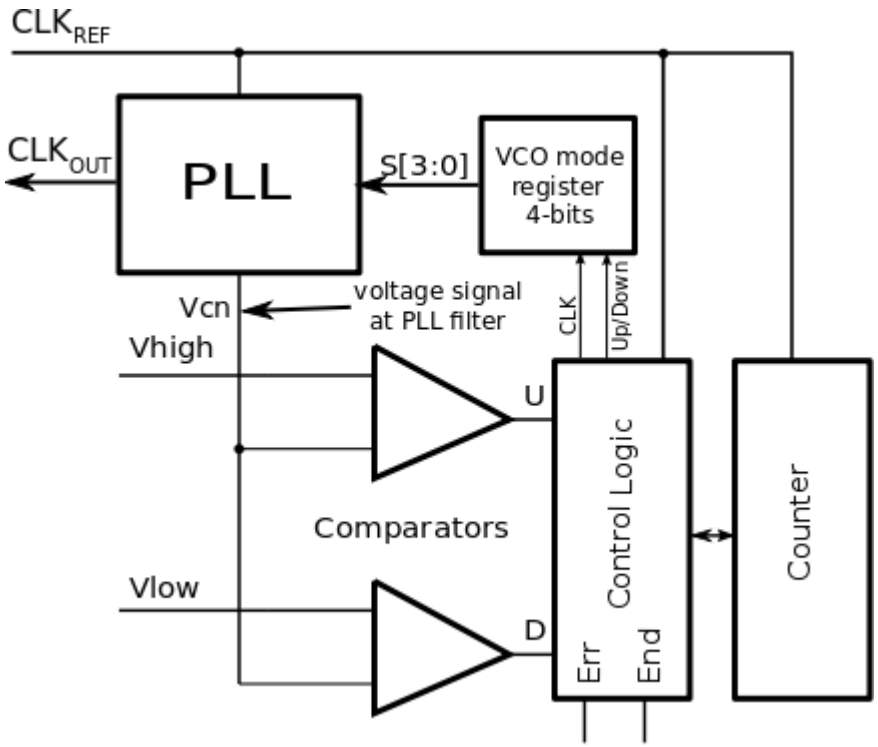
300 x 300 um

PLL features:

- General purpose PLL block
- Very wide output frequency range (10MHz – 3.5GHz)
- 16 VCO modes - Automatically (or manually) changed
- Jitter 15-70 ps (to be improved...)
- Power consumption ~0.6mW@1GHz
- Different loop division factors: 6,8,10 and 16

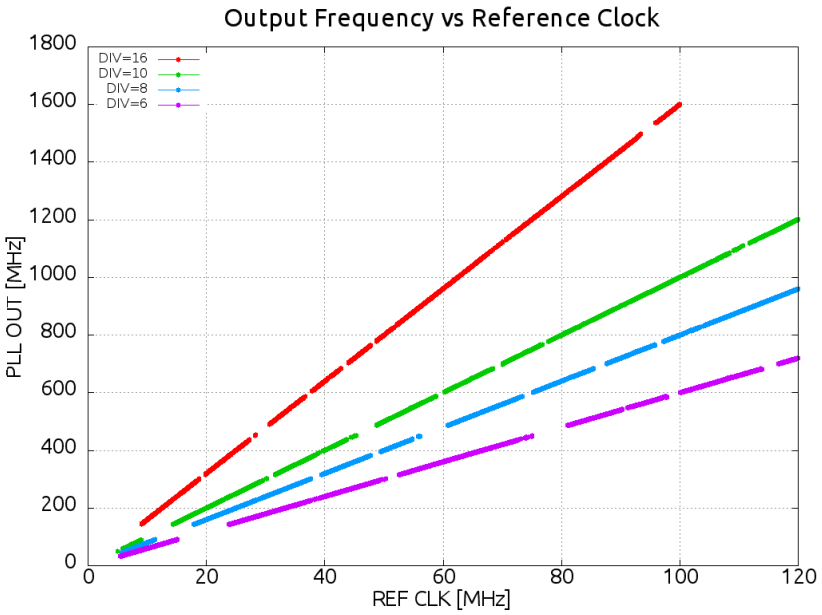
M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Swientek, "Development of scalable frequency and power Phase-Locked Loop (PLL) in 130nm CMOS technology", TWEPP2013 23-27 September 2013, Perugia Italy

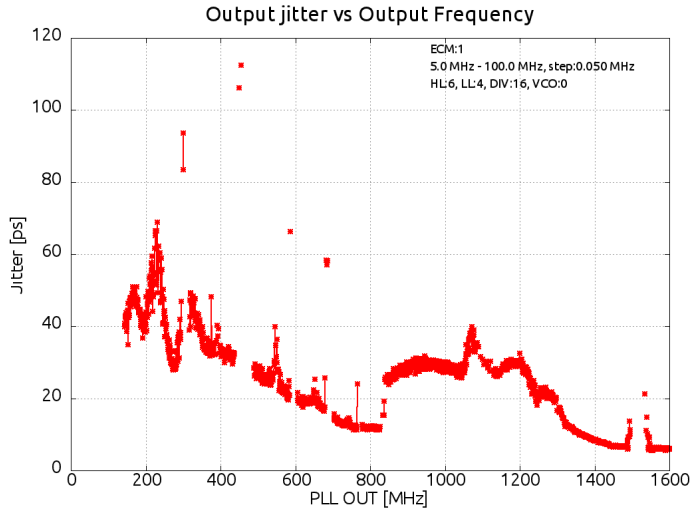
Multichannel ADC aspects
PLL design in IBM 130 nm
PLL - principle of automatic VCO mode change

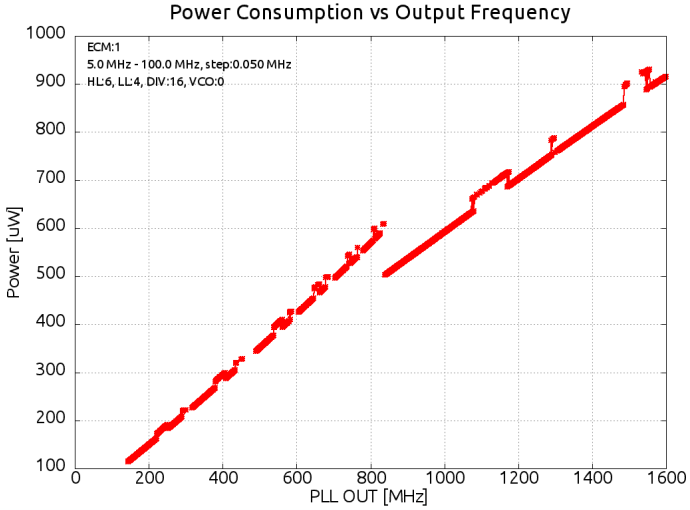


- Comparators check whether a voltage signal at the PLL filter (Vcn) is grater than Vhigh or lower than Vlow.
  - If Vcn > Vhigh (VCO too slow) for certain period (measured by counter) control logic switches the mode register to faster mode (up).
  - If Vcn < Vlow (VCO too fast) VCO mode register is switched to slower mode (down).
  - When Vcn voltage stays between Vhigh and Vlow the mode is not changed.

Multichannel ADC aspects
Performance of PLL prototype in IBM 130 nm

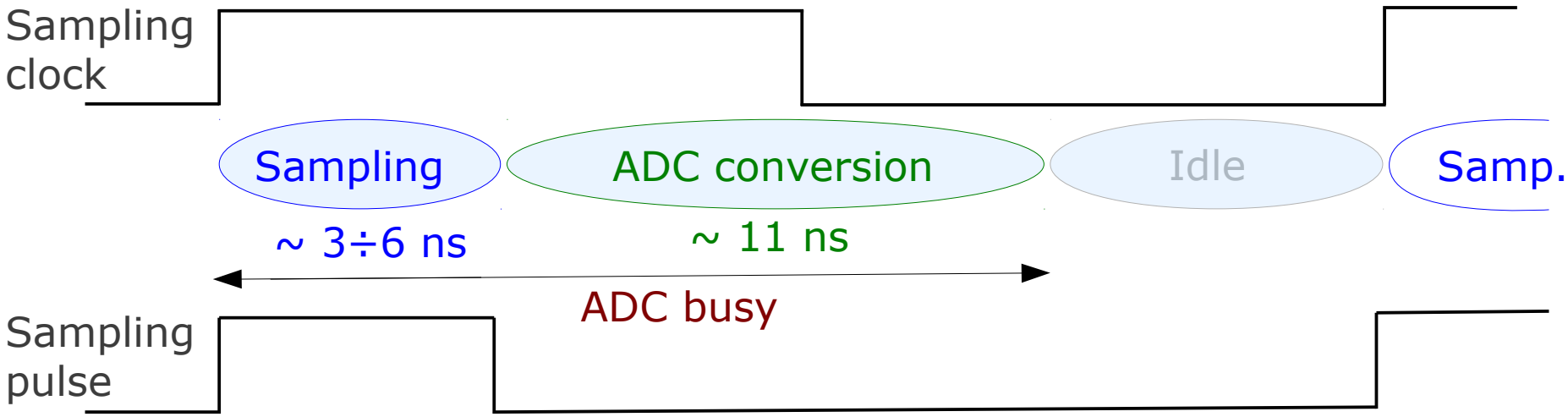






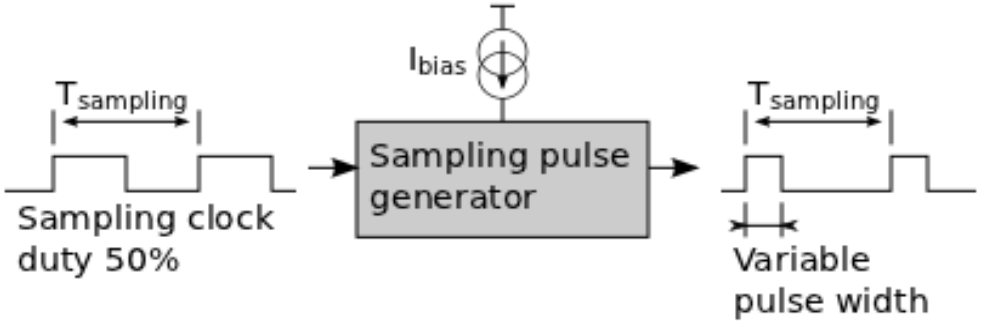
- Measurements confirm proper circuit operation in frequency range 20MHz-1.6GHz
- All four division factors work properly
- Automatic mode change positively verified
- Power consumption scales linearly with PLL clock frequency (two rings → two curves)

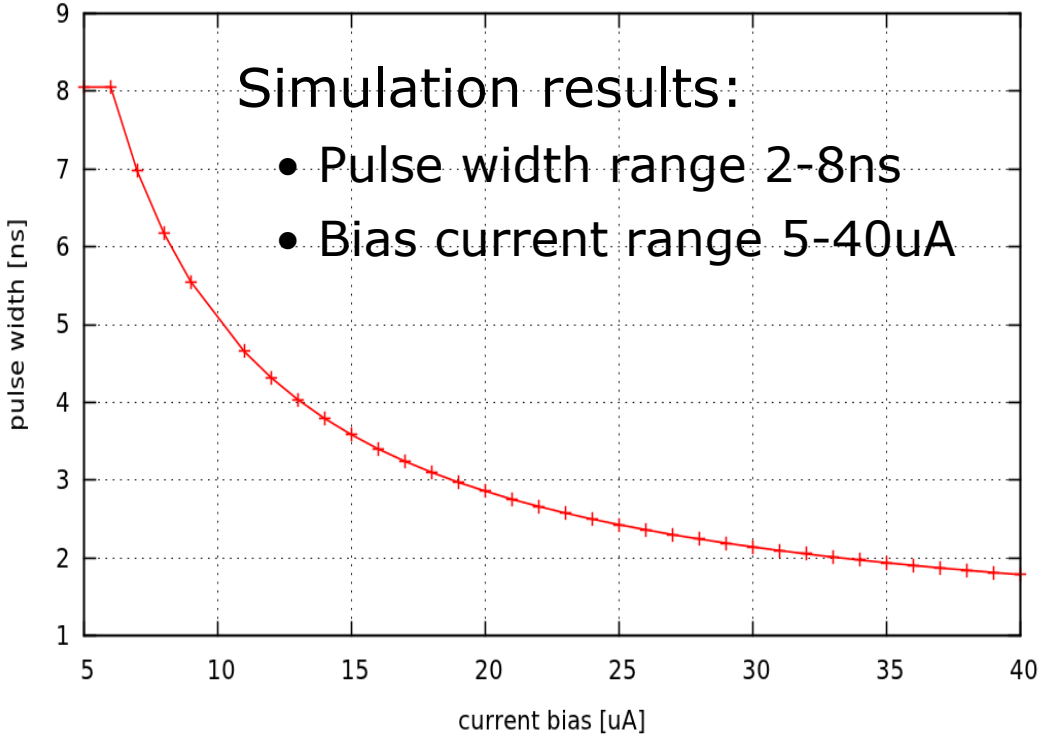
Multichannel ADC aspects
Generation of sampling pulse



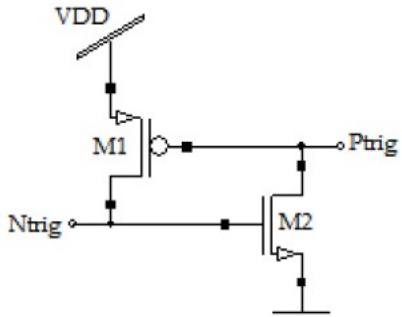
- ADC works with 50% duty cycle sample clock
- Input signal sampling time should be tuned:
  - If too short - decrease resolution
  - If too long - lowers maximum sampling frequency
- Current steered width pulse generator providing sample timing designed

Multichannel ADC aspects
Design of sampling pulse generator



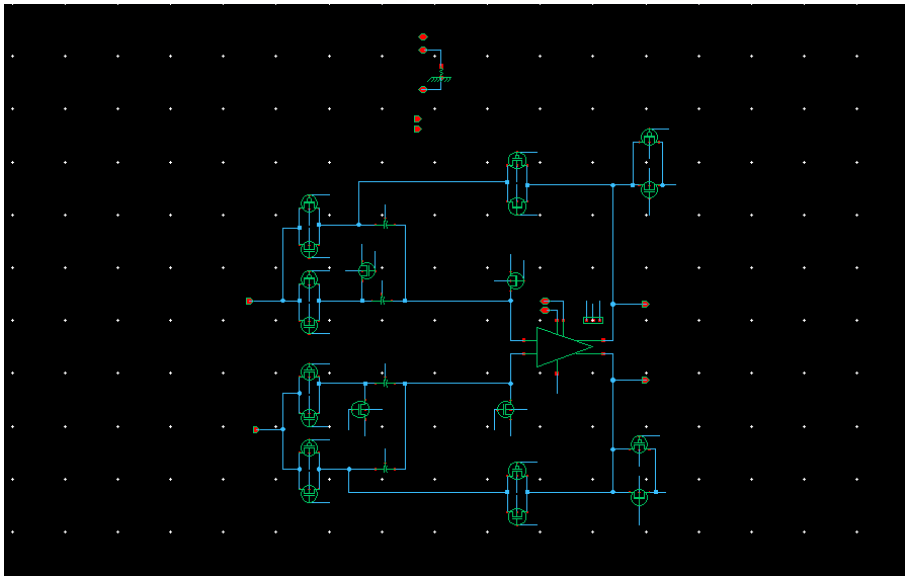


Generator of sampling pulse converts 50% duty external sampling clock into internal variable width pulse (controlled by Ibias)



Pulse generator design is based on MOS thyristor delay circuit.

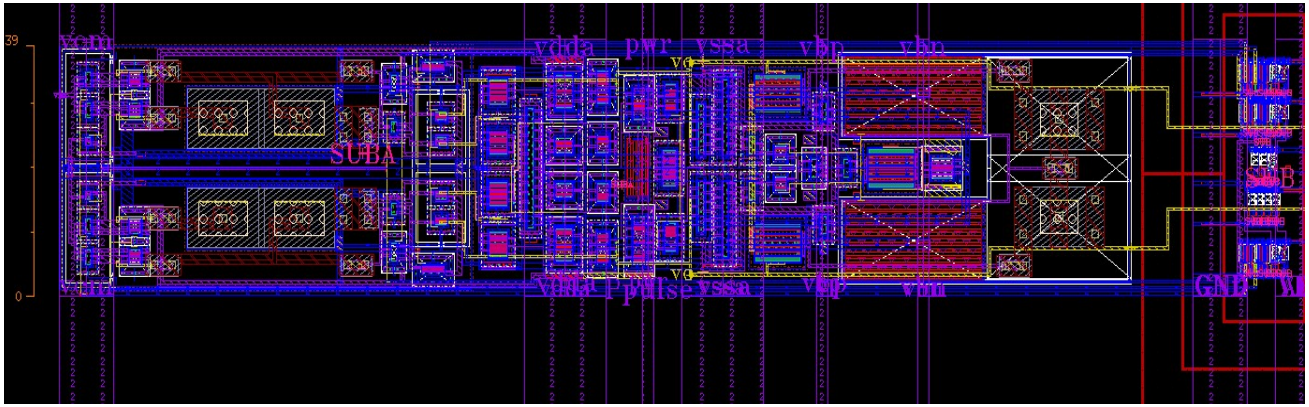
Multichannel ADC aspects
Design of Single-to-Differential converter in IBM 130 nm



Typically front-end electronics has single-ended output. In uch case a Single-to-Differential converter is needed.

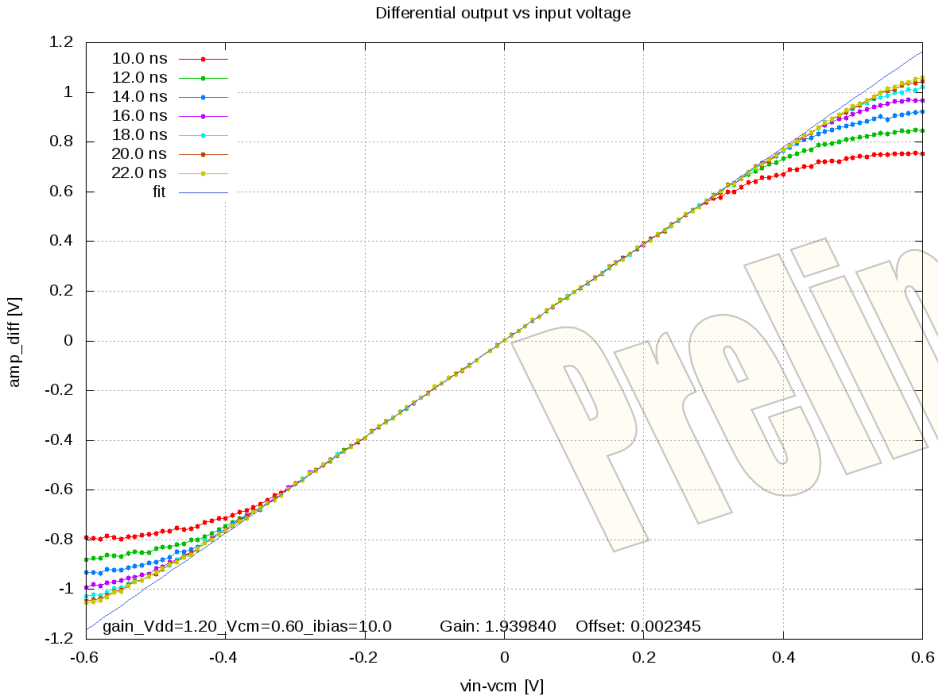
Main features of Single-to-Differential converter:

- Architecture: differential switched-capacitor amplifier
- Recycled folded cascode as amplifying stage
- Gain = 2
- Simulated power consumption ~0.25mW for 6-bit ADC and ~0.5mW for 10-bit ADC

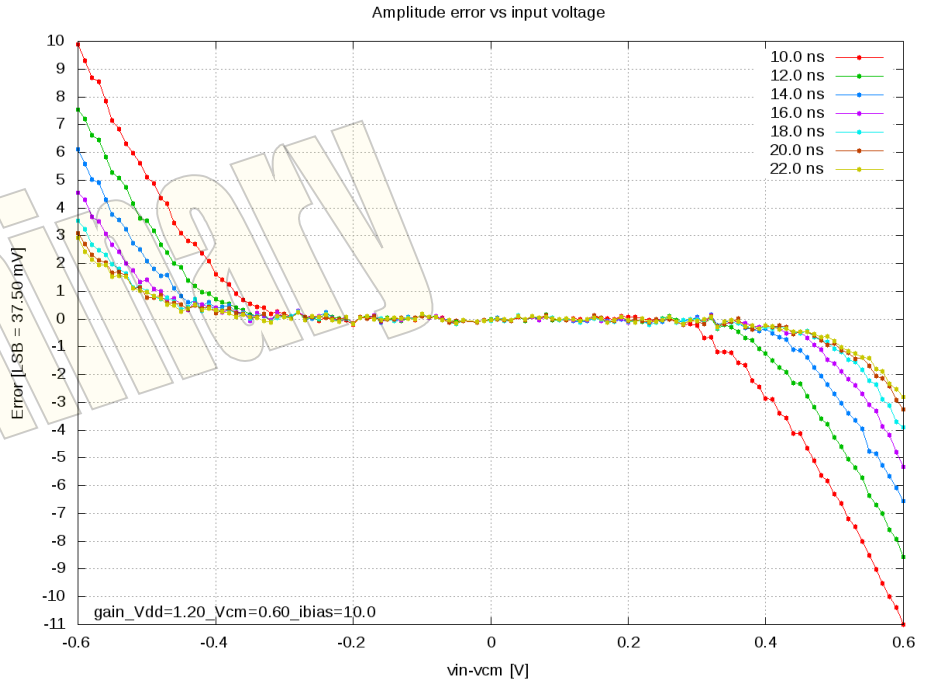


Multichannel ADC aspects
Single-to-Differential converter for 6-bit ADC
Preliminary measurements

Transfer curve of S-to-Diff converter for different sampling times



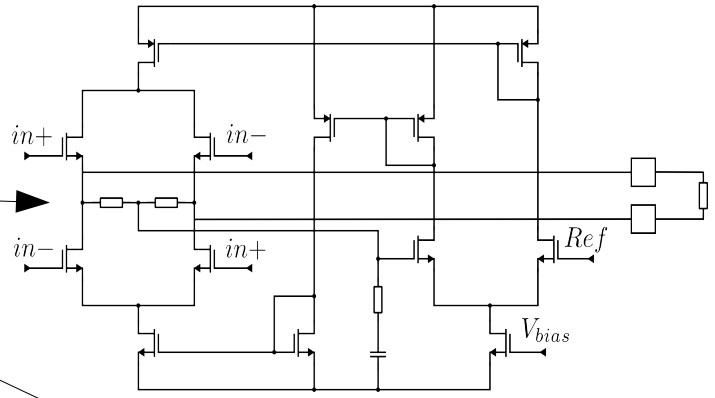
Error of S-toDiff transfer curve in LSB for different sampling times

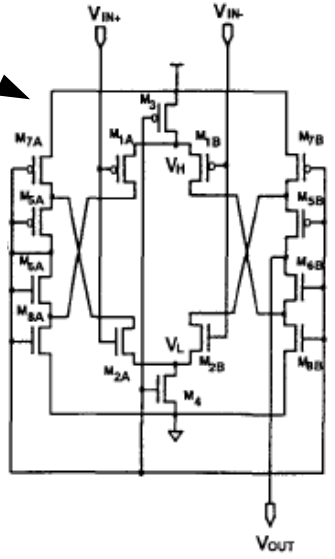


Good linearity is kept for more than half of input signal range

Multichannel ADC aspects
Design of SLVS interface

- Specifications:
  - Architecture
    - Driver – based on Boni paper
    - Receiver – based on self-biased amplifier (Bazes paper)
  - Technology – IBM 130 nm
  - Maximum frequency ~1GHz
  - Pitch matched to pads. Driver/receiver integrated with 2 pads (146um pitch)



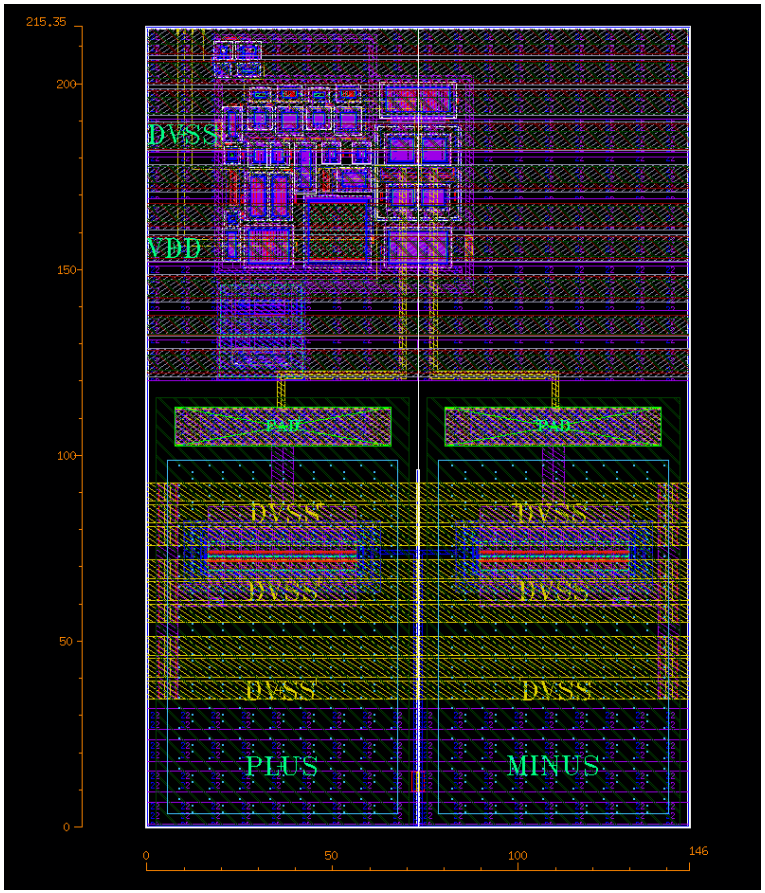


A. Boni, A. Pierazzi, D. Vecchi, LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35 µm CMOS, IEEE J. Solid-State Circuits, vol. 36, no. 4, pp. 706–711, April 2001

M. Bazes, Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers, IEEE J. Solid-State Circuits, vol. 26, no. 2, pp. 165–168, February 1991.

Multichannel ADC aspects
SLVS interface as differential I/O pads

Driver



Receiver

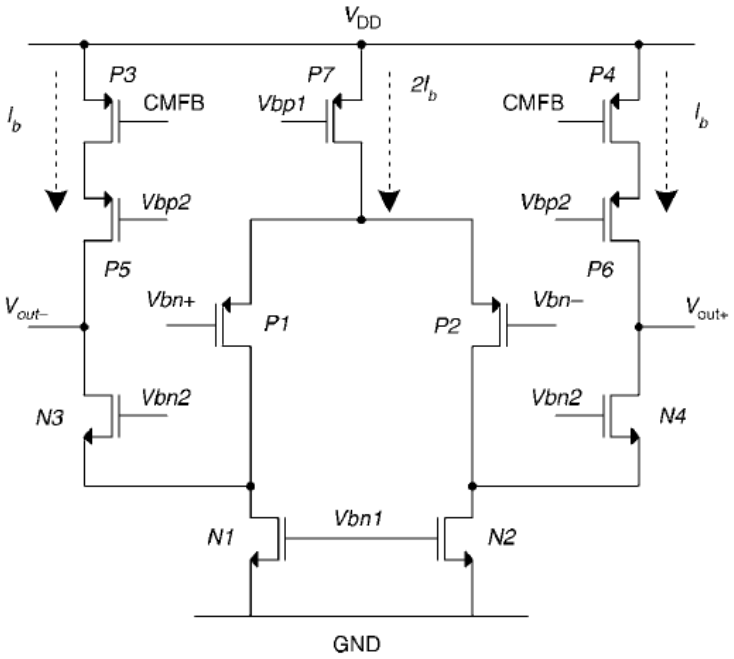
Functionality verified during ADC and PLL test up to ~1.5 GHz.
Dedicated quantitative tests not yet done (waiting in line...)

Summary

- Potential of deep-submicron CMOS technologies, together with recent developments in ADC architectures – SAR in particular, allow to build multichannel front-end ASICs comprising ADC in each channel, without penalty on power consumption
  - Modern ADC can consume significantly less power than preamp&shaper circuitry
- Multichannel readout ASIC with ADC becomes complex Systems on Chip (comprise hundreds of channels, front-end, ADC, DSP, PLL, DLL, serializer/deserializer, digital interfaces, etc...)
  - Various ADC aspects (e.g. reference voltage design) were not covered in this presentation...

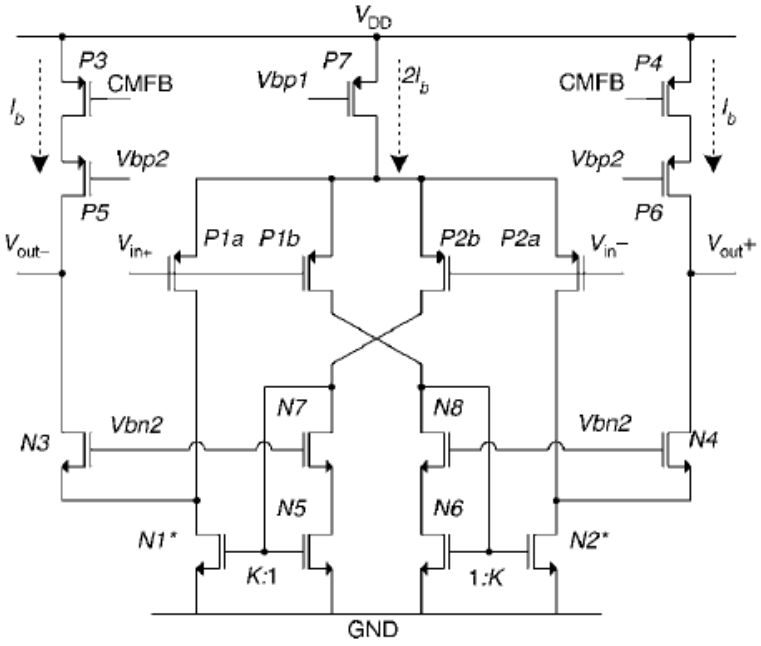
Thank you for attention

Sampling amplifier issues



Conventional folded cascode (FC)

$Gm_{FC}=gm_{P1}$, $SR_{FC}=2I_b/C_L$



Recycling folded cascode (RFC)

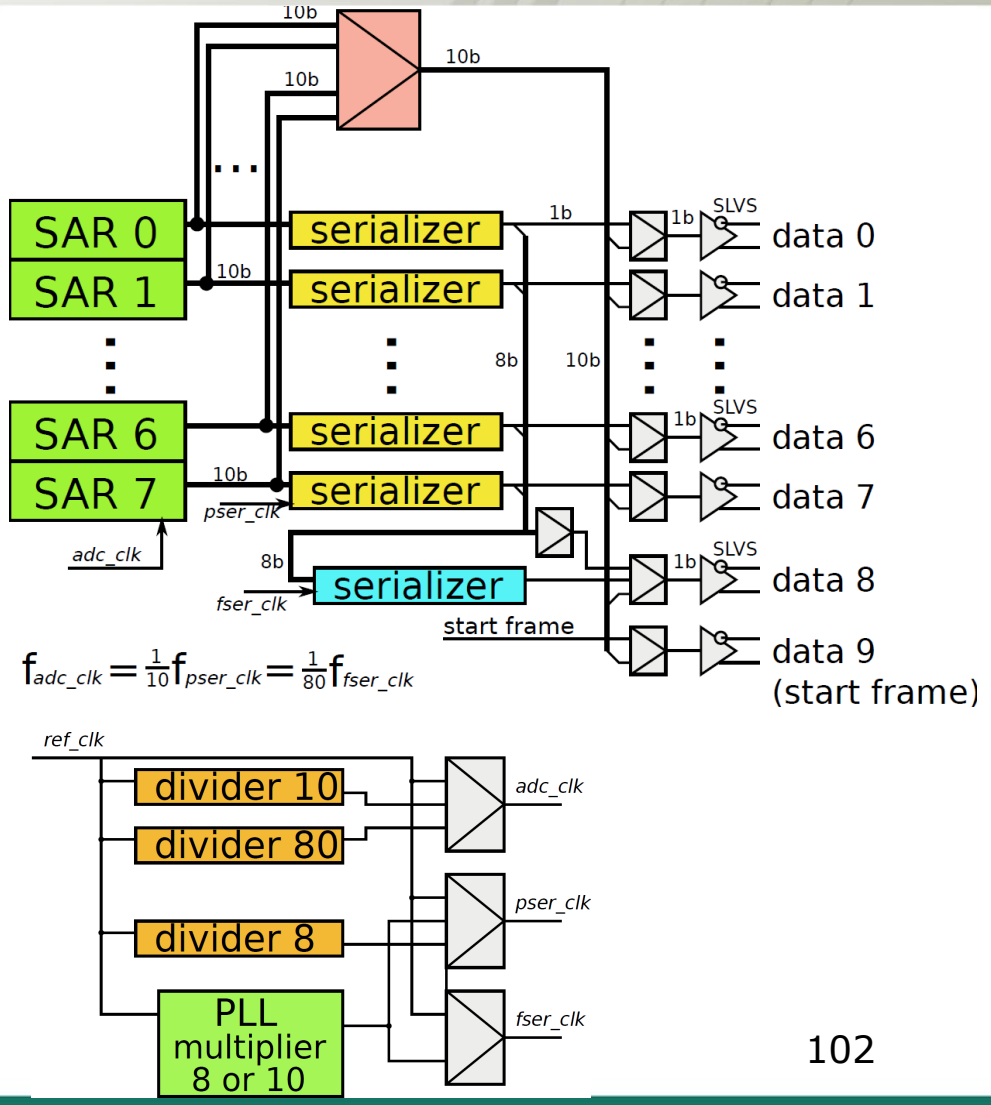
$Gm_{RFC}=gm_{P1}$ (1+K), $SR_{RFC}=2KI_b/C_L$

In 130nm a gain of few hundred may be achieved. For 10-bit accuracy a second stage or a gain boosting is needed

Design of SAR multichannel ADC

Specifications & implementation issues:

- 8 channels of 10-bit (6-bit) SAR ADC
- Technology IBM 130 nm
- Layout with 146um (40um) ADC pitch
- Multimode digital multiplexer/serializer:
  - Serial mode: one data link per all channels (external clk division or PLL clk generation)
  - Parallel mode: one data link per channel (external clk division or PLL clk generation)
  - Test mode: single channnel output (max fsmp ~50 Msps)
- PLL for data serialization
- High speed SLVS interface (~1GHz)
- Power pulsing
- Generation of short sampling pulse
- Bootstrapped S/H switches
- Voltage reference not yet addressed...
- SingleEnded-to-Differential converter ??

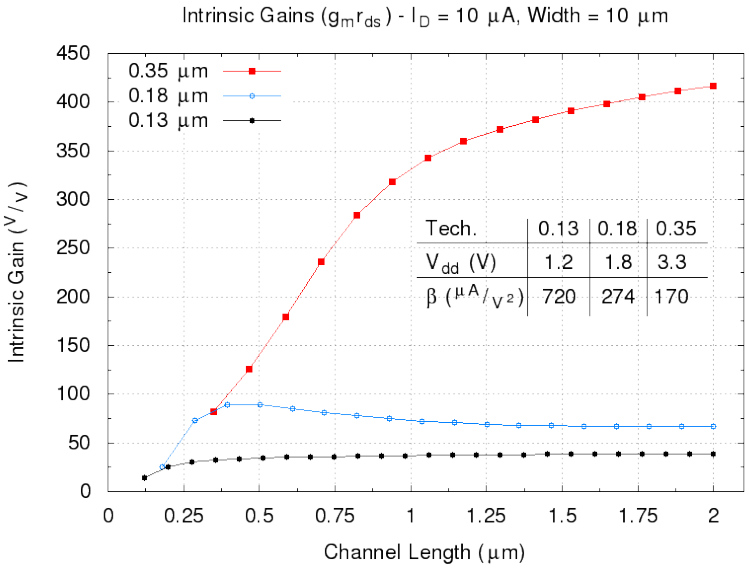


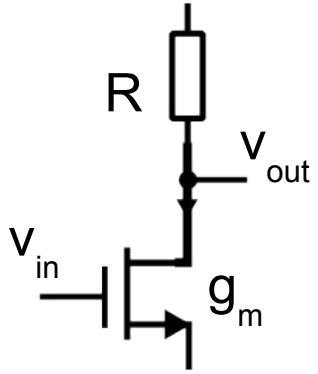
Design in deep sub-micron CMOS
Comparison of CMOS generations

Technology nodes used in HEP: 350nm – 250nm – 180nm – 130nm - 65nm
LHC FAIR SLHC/LC

Modern CMOS processes offer: higher speed, lower power, smaller area, better radiation hardness,

Intrinsic gain
Of NMOS



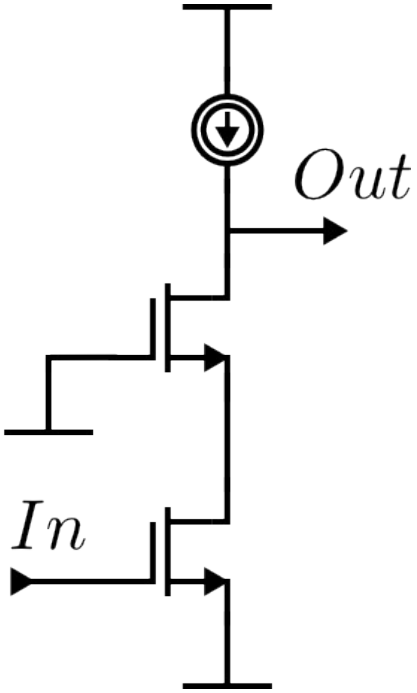


but also lower gain..., and hundreds of design rules

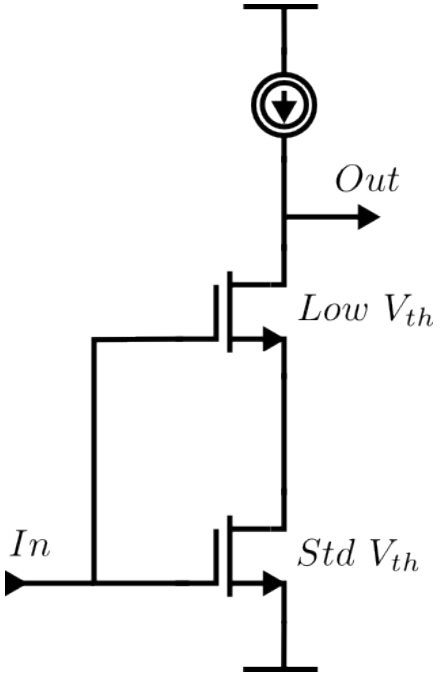
Design in deep sub-micron CMOS has become much more difficult !

Main front-end block: Amplifier
Amplifier design in deep sub-micron CMOS

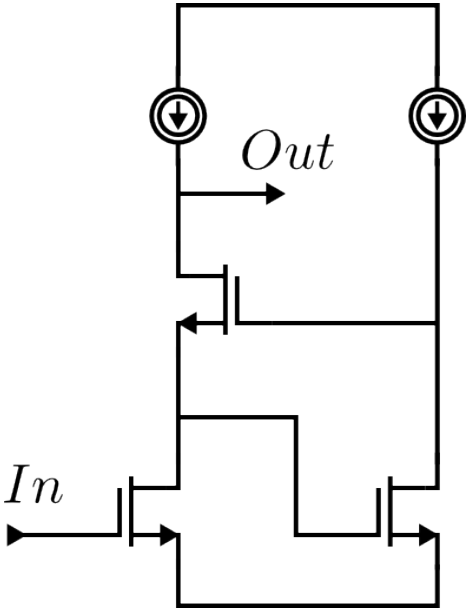
Cascode amplifier



Self-Cascode

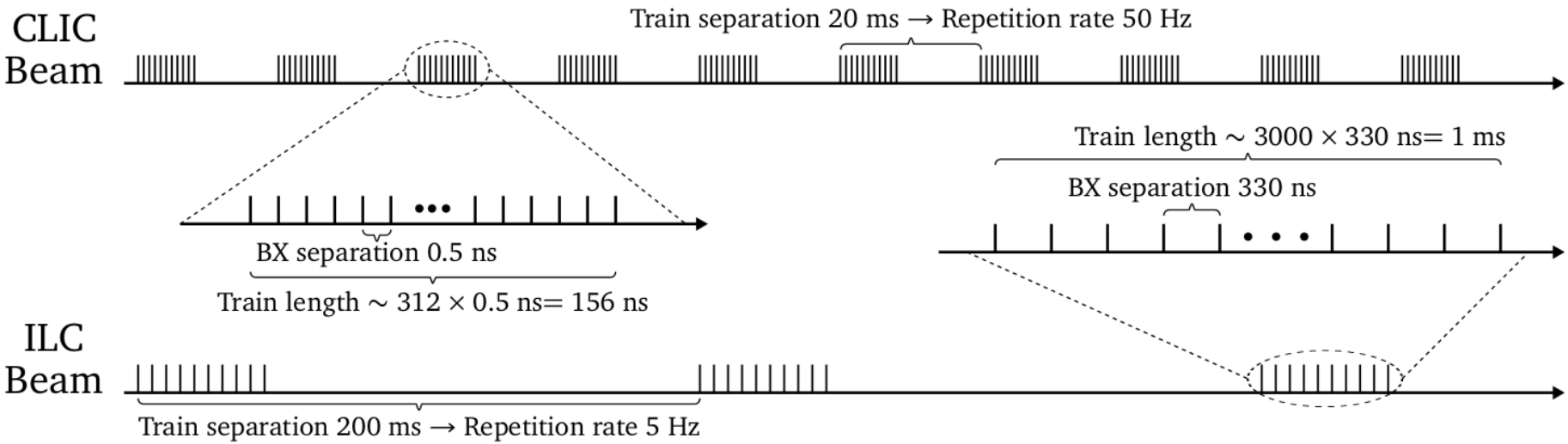


Regulated cascode (gain boosting)



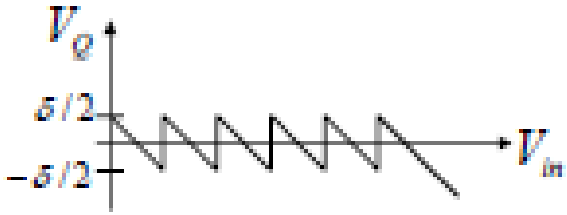
Low intrinsic gain and small power supply voltage make amplifier design difficult.
It is a challenge to obtain gain > 1000 in 130 nm CMOS !

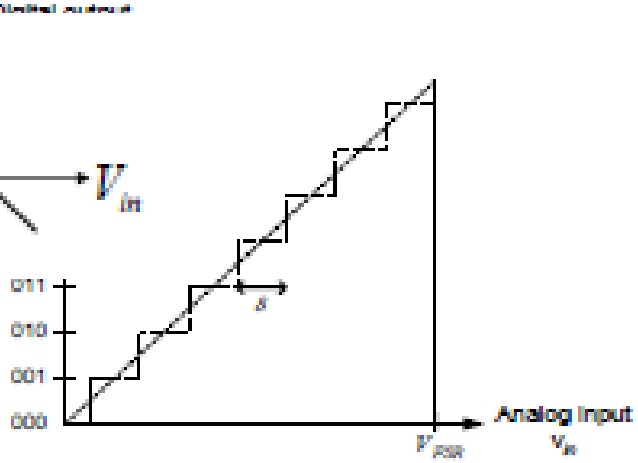
Readout electronics for future linear colliders
Power pulsing needed for huge power savings



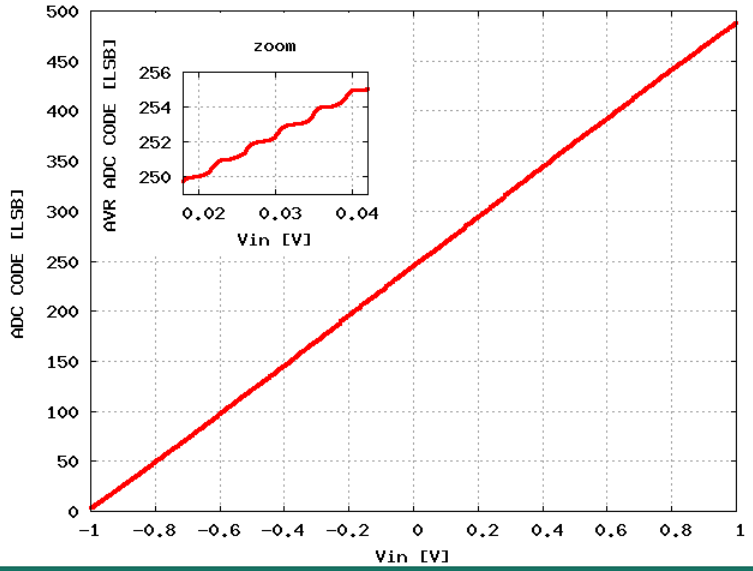
- Very low duty cycle (<<1%).
- The average power consumption can be dramatically reduced by turning the power off between the trains.
- Readout electronics should allow fast power switching.

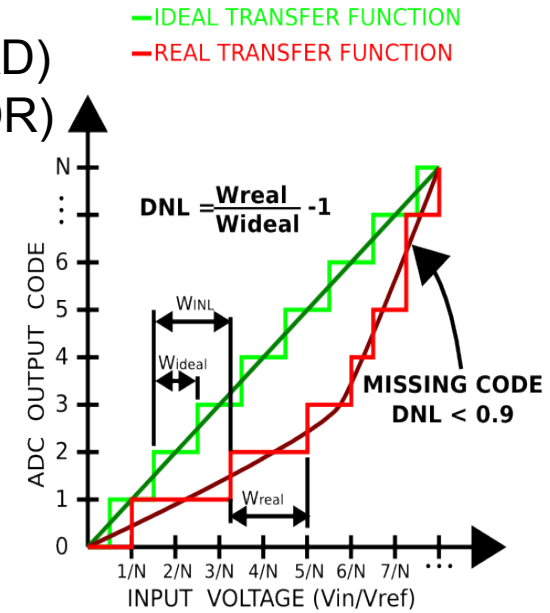
Real ADC
Static errors





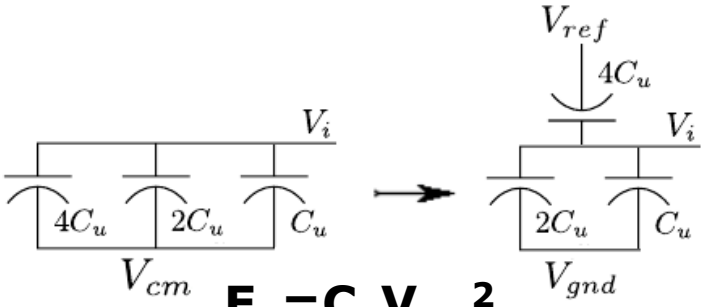
Differential Non-Linearity (DNL) – difference betwe
size
Integral Non-Linearity (INL) difference between ste
joinimg end points (or bast fit line)
Missing Codes – excessive DNL leads to missed codes in ADC
Non-Monotonicity – excessive DNL leads to non-monotonic behavior in ADC
Offset error
Gain error
Signal-to-Noise and Distortion (SINAD)
Spurious Free Dynamic Range (SFDR)





Key aspects of DAC in SAR ADC
DAC switching energy:
Principle 2-bit capacitor array example

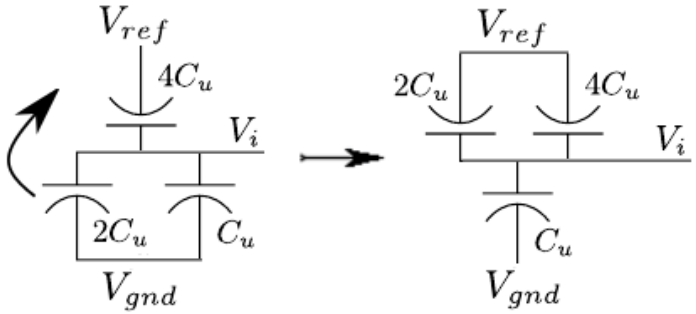
- Energy drawn from V_{ref}: **$E = V_{ref} \circ \Delta Q$**
  a) **up** transitions – nC_u short to V_{ref}
  b) **down** transitions – nC_u short to V_{gnd}



1) $4C_u$ goes **up**, $2C_u$ and C_u goes **down**:

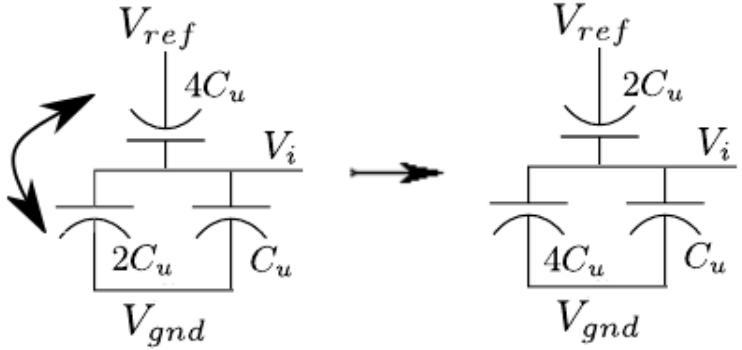
$E_1 = C_u V_{ref}^2$

2a) If $V_{in} > \frac{1}{2}V_{ref}$ then only $2C_u$ goes **up**:



$E_{2up} = \frac{1}{4}C_u V_{ref}^2$

2b) otherwise $2C_u$ goes **up** and $4C_u$ goes **down**:



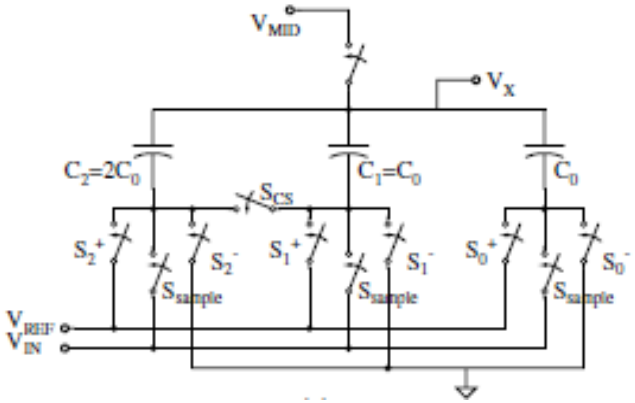
$E_{2down} = 5 \circ \frac{1}{4}C_u V_{ref}^2 = 5 \circ E_{2up}$

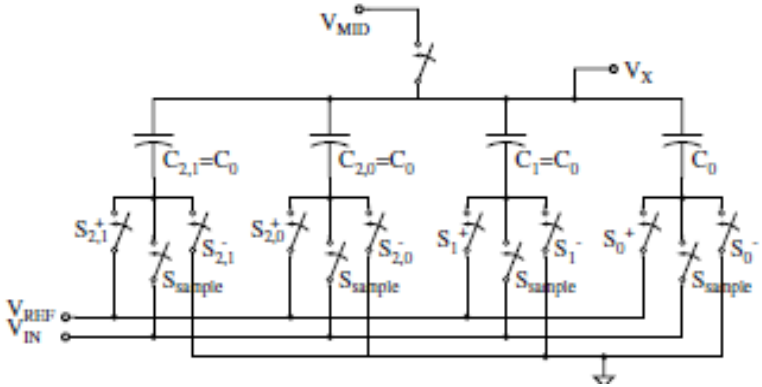
down transitions consume much power...

B. P. Ginsburg, A.P.Chandrakasan "An Energy-Efficient Charge Recycling Approach for SAR Converter With Capacitive DAC", IEEE Int. Symp. On Circuits and Systems, May 2005 pp. 184-187

Switching energy – principle
2-bit capacitor array example...

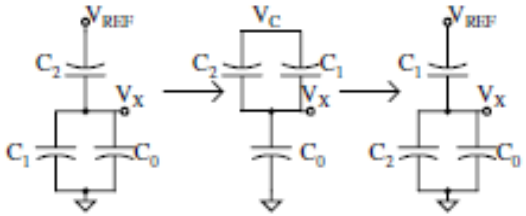
There are other ways to perform “down” transitions:

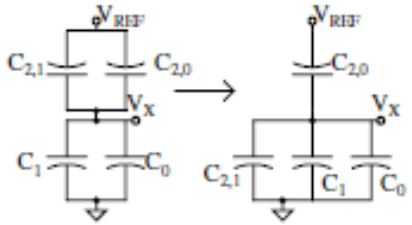




Charge sharing: $E=7C_0V^2_{ref}/12$

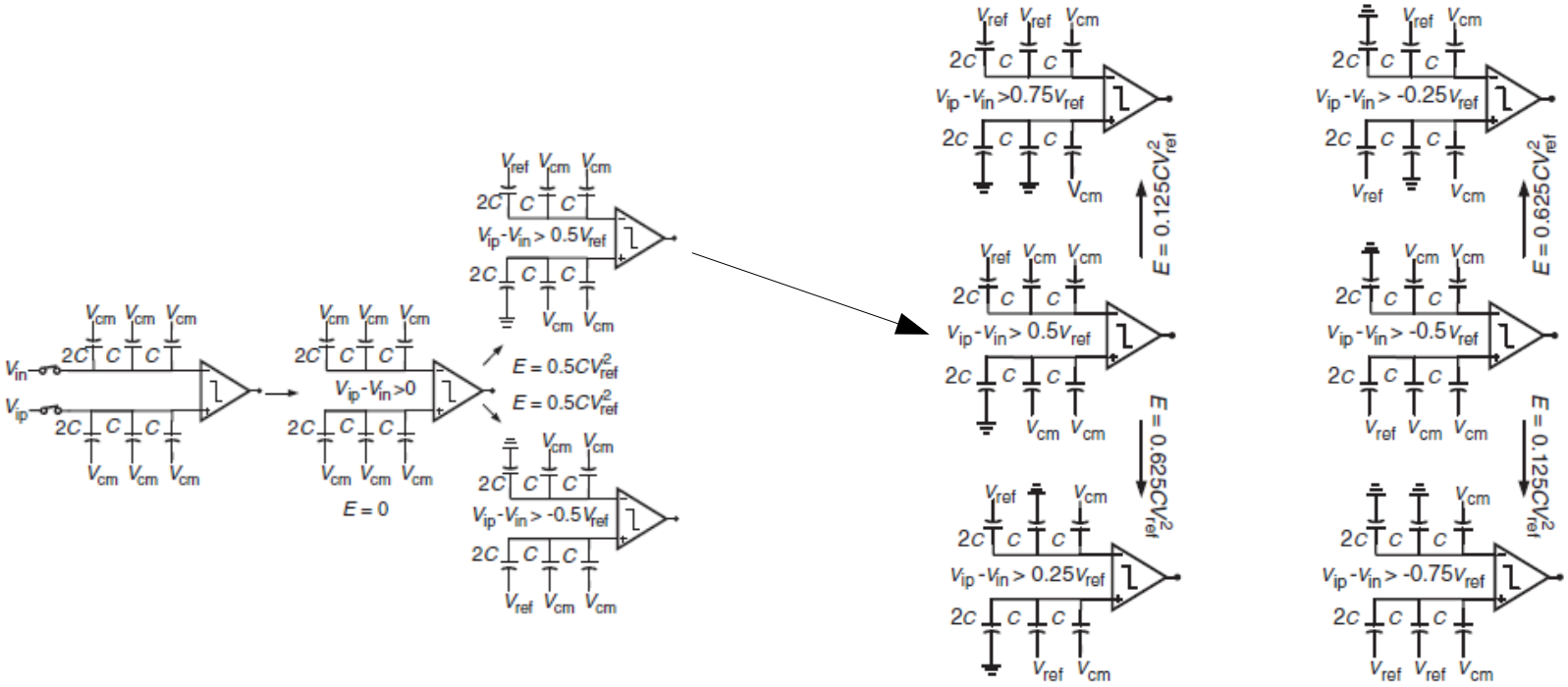
Split capacitor: $E=C_0V^2_{ref}/4$





Switching scheme may be optimized to save power in “down” transitions!

Switching energy – more efficient configurations
Merge Capacitor Switching (MCS) SAR ADC



Switching energy ~93% less than conventional SAR ADC

Such switching scheme is used in our present design

V. Hariprasath, J. Guerber, S-H. Lee, U-K. Moon "Merged capacitor switching based SAR ADC with highest switching energy-efficiency", Electronics Letterss v.46 No.9 April 2010