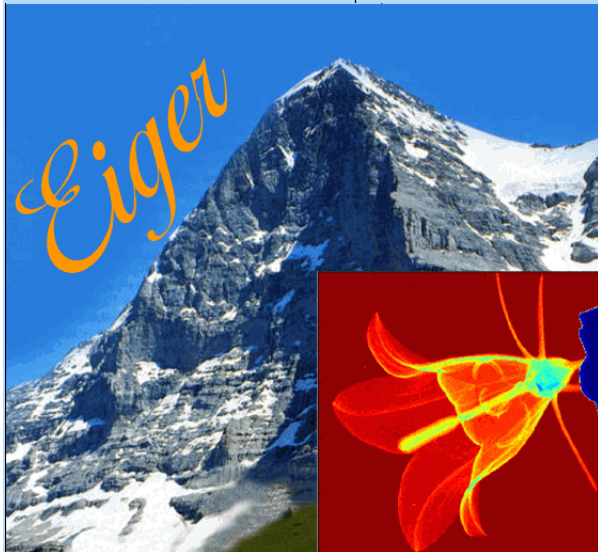


PAUL SCHERRER INSTITUT



Wir schaffen Wissen – heute für morgen



**Paul Scherrer Institut**

Roberto Dinapoli

[roberto.dinapoli@psi.ch](mailto:roberto.dinapoli@psi.ch)

# Single photon counting detectors for X-ray applications

- Introduction of Paul Scherrer Institut
- Chip design at PSI
- Basics of X-ray synchrotron radiation emission
- Detectors developed by the SLS Detector group for X-ray detection
  - Single photon counting detectors
    1. PILATUS (2D)
    2. MYTHEN (1D)
    3. EIGER (2D)

## **EIGER: next generation single photon counting detector for X-Ray applications**

- Motivation
- Main features and comparison with Pilatus II
- The pixel
- Readout architecture
- Testing a single photon counting detector

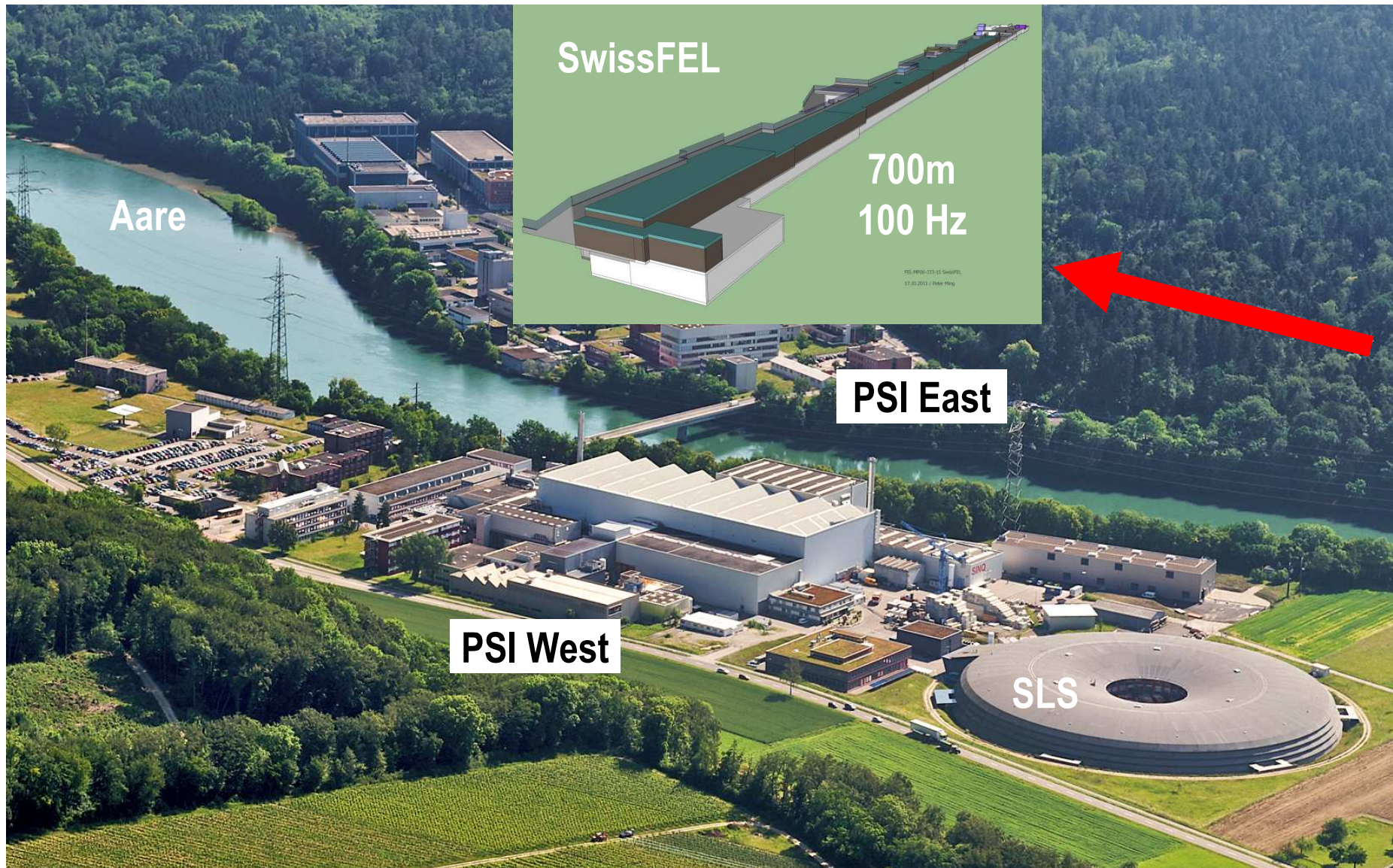
## *Charge integration detectors for X-ray applications*

**Wednesday 16:45**

- Quick summary of first talk
  - Charge integration detectors
    1. AGIPD (2D, XFEL)
    2. GOTTHARD (1D, XFEL & Synchrotron)
    3. JUNGFRAU (2D, XFEL & Synchrotron)
    4. MÖNCH (2D, XFEL & Synchrotron)
- MÖNCH, a small pitch, integrating hybrid pixel detector for X-ray applications



# PAUL SCHERRER INSTITUT (2011)

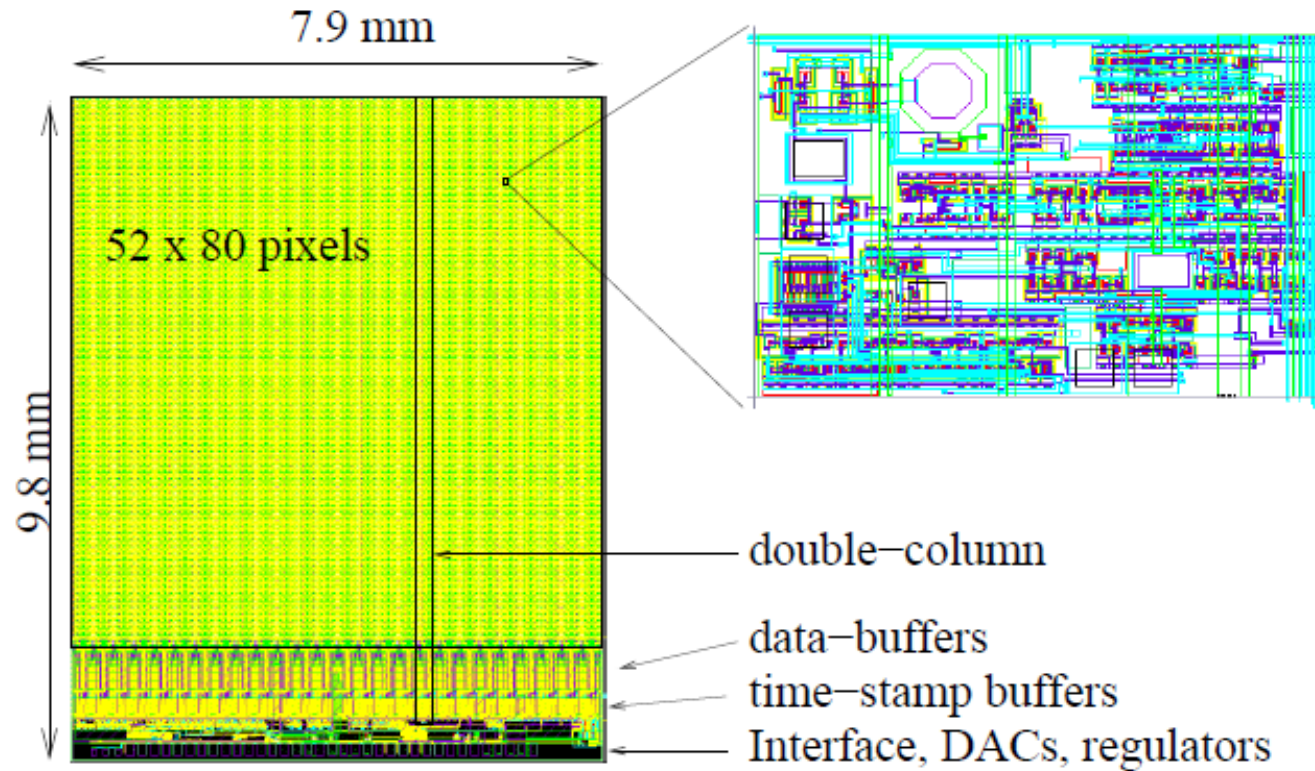


*~1700 Staff employees; 30Km from Zurich*



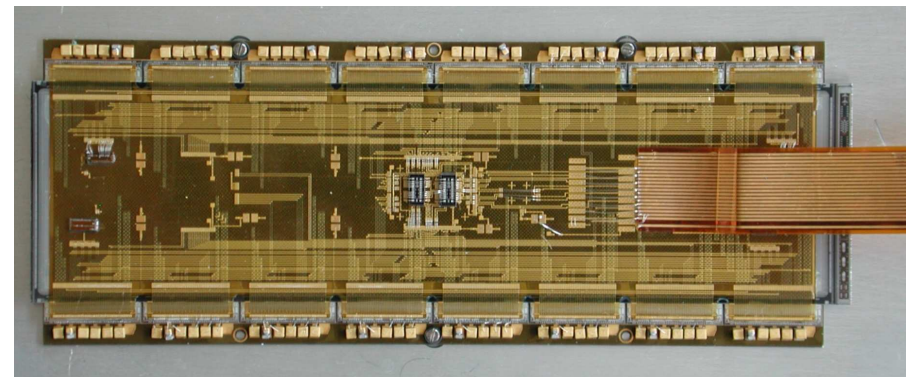


# The CMS Pixel Chip (Roland Horisberger)



- Technology: 0.25  $\mu\text{m}$  IBM
- Pixel size 150x100  $\mu\text{m}^2$
- Tested up to 100MHz/cm<sup>2</sup> ~ 20 kHz/pixel
- Time resolution: 25 ns
- Deadtime/ pixel: 100ns
- Module: 416 x 160 pixels (62.4 x 16 mm<sup>2</sup>)

**CMS module based on PSI46 Chip**



## Particle physics

CMS

Pixel chip for the inner tracker  
New version for LHC luminosity upgrade

MEG

Domino sampling chips (DRS4)  
New version for MEEE (DRS5)

## X-ray detection

Synchrotron light (Mythen, Pilatus, Eiger)

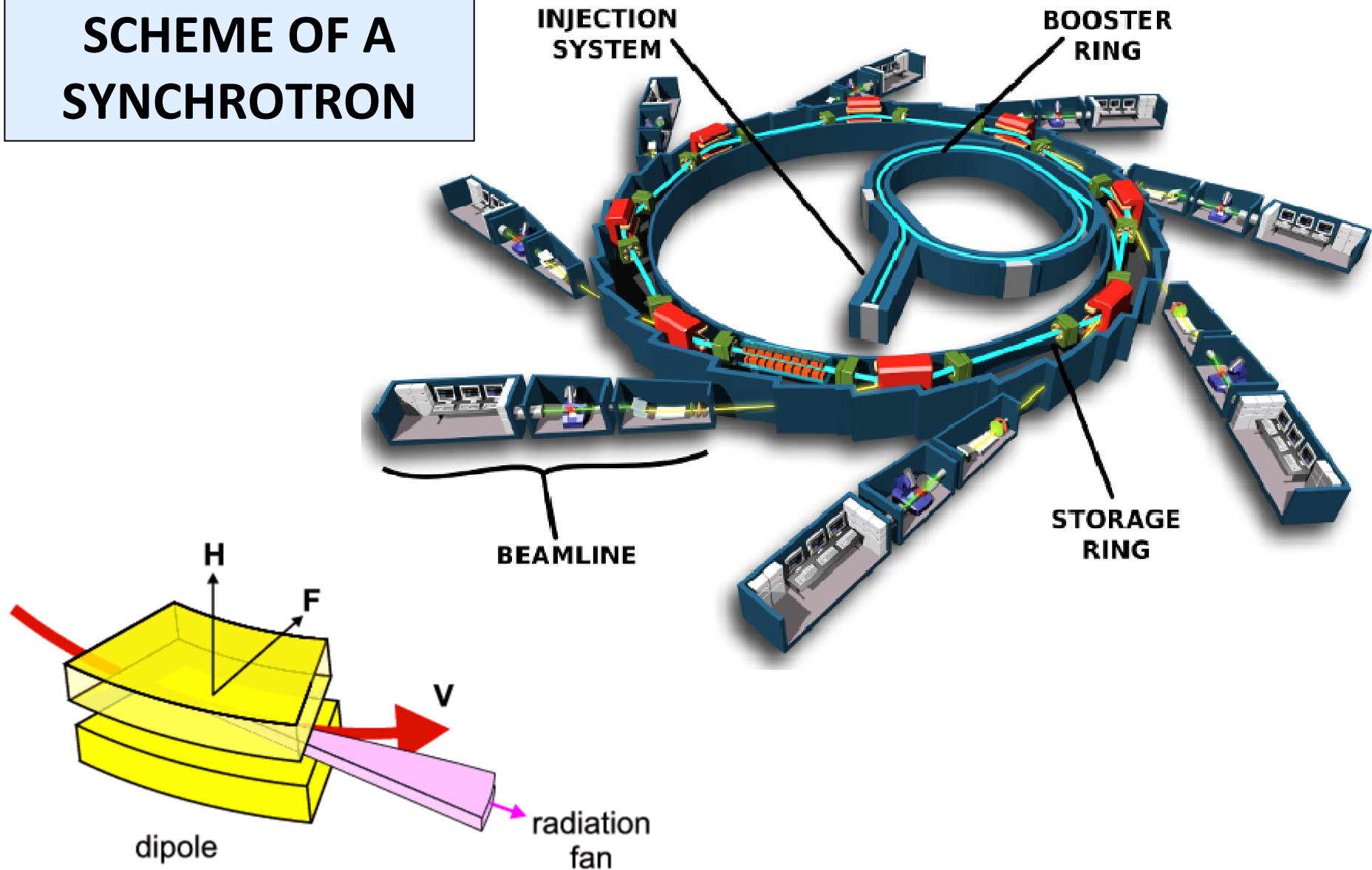
XFEL light (Agipd, Gotthard, Jungfrau, Mönch)

## Astronomy Research

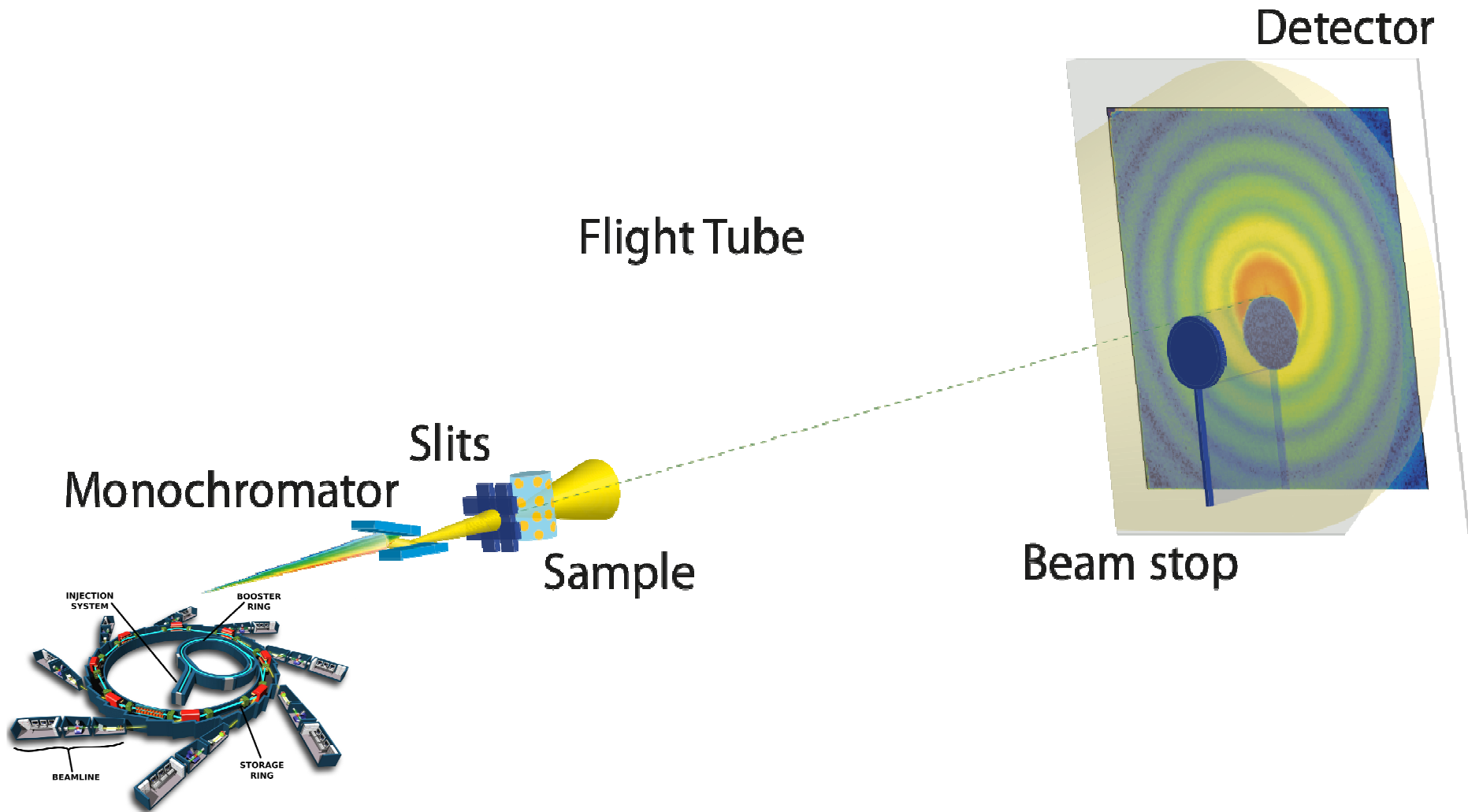
Sensor design

HiZ – Neutrons – Low energy X-ray – Electrons  
Detectors

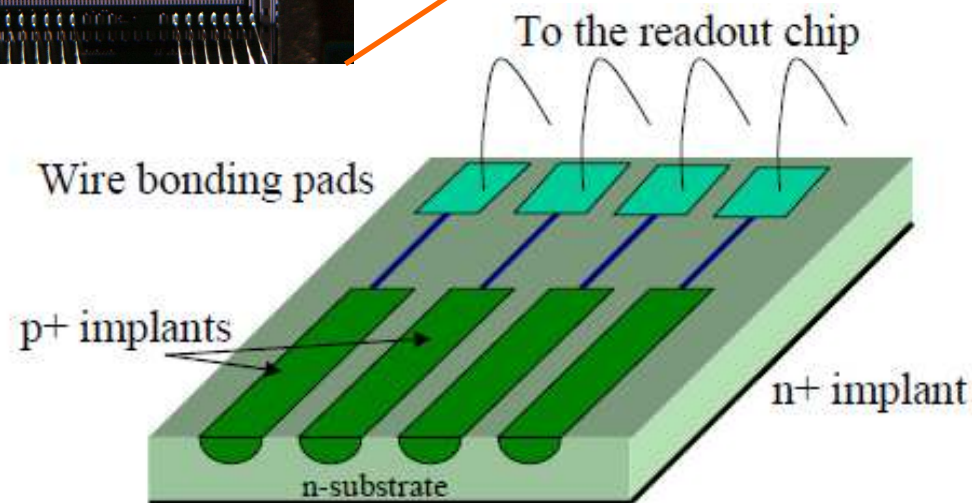
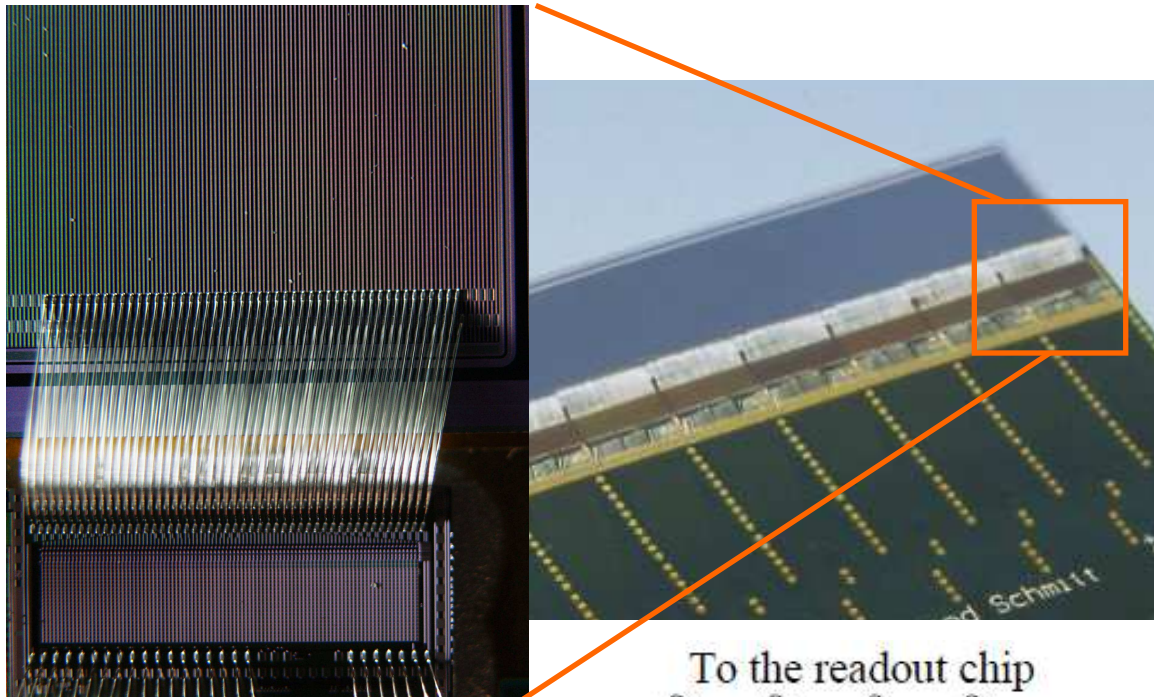
## SCHEME OF A SYNCHROTRON







# 1D hybrid detectors (strips)



## *Strip detectors*

- High segmentation
- Small data throughput
- Lower cost per area

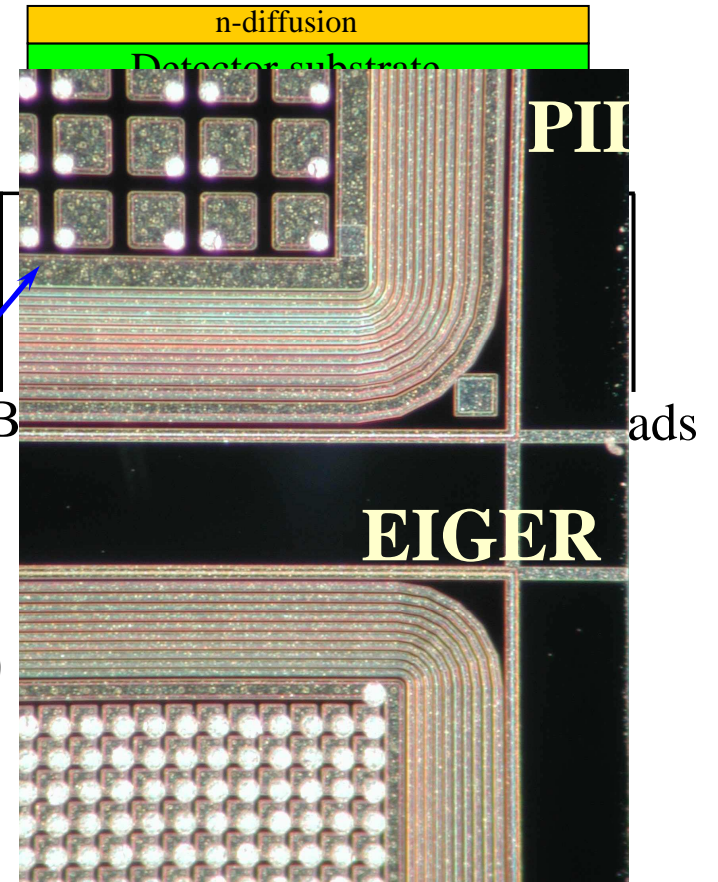
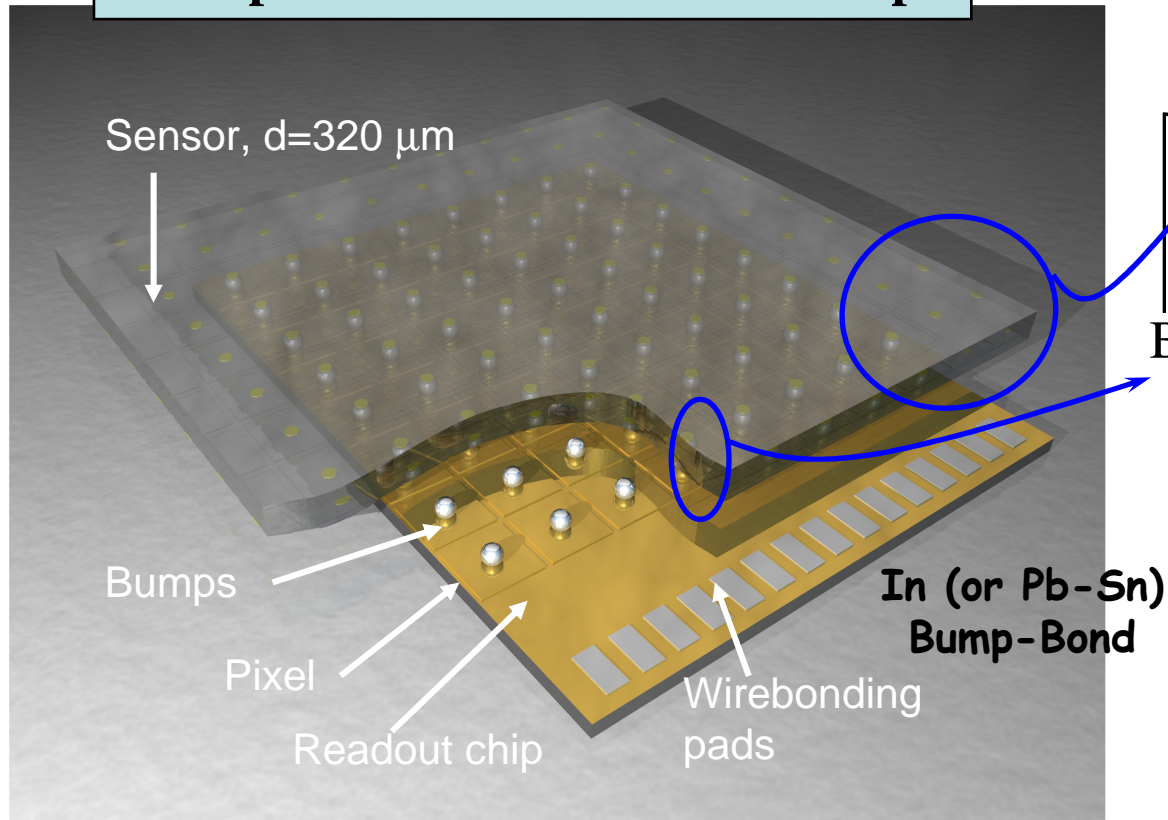
Powder diffraction

Fluorescence emission spectrometers

Beam position monitors

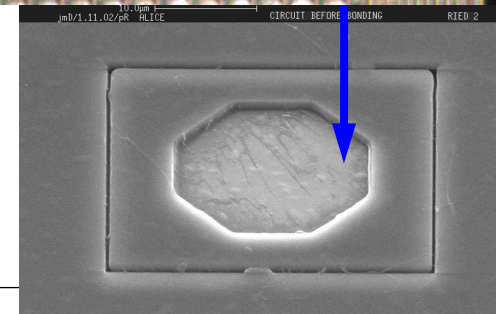
# 2D hybrid detectors (pixels)

**A silicon detector bump-bonded with a readout chip**



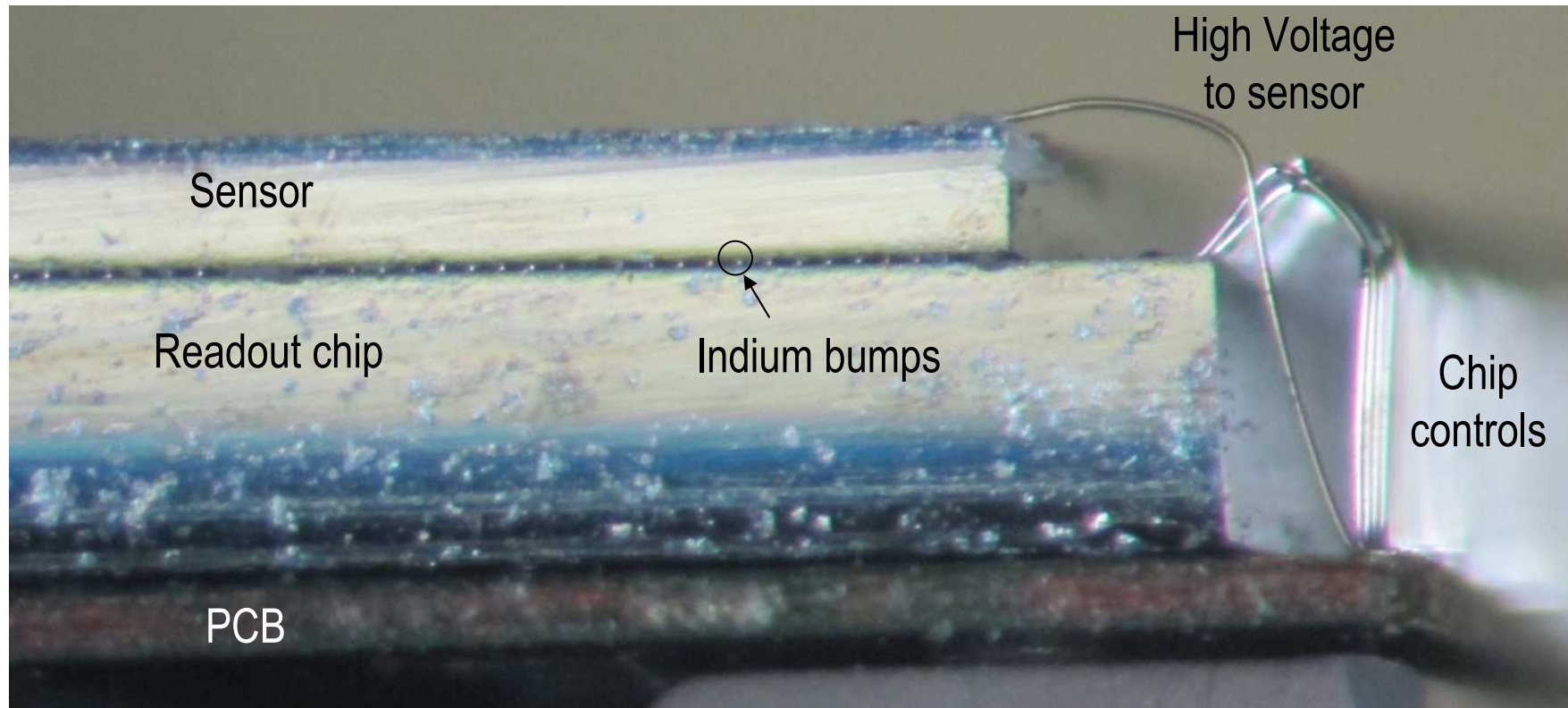
***2D information!***

**Bump-bond metal pad**





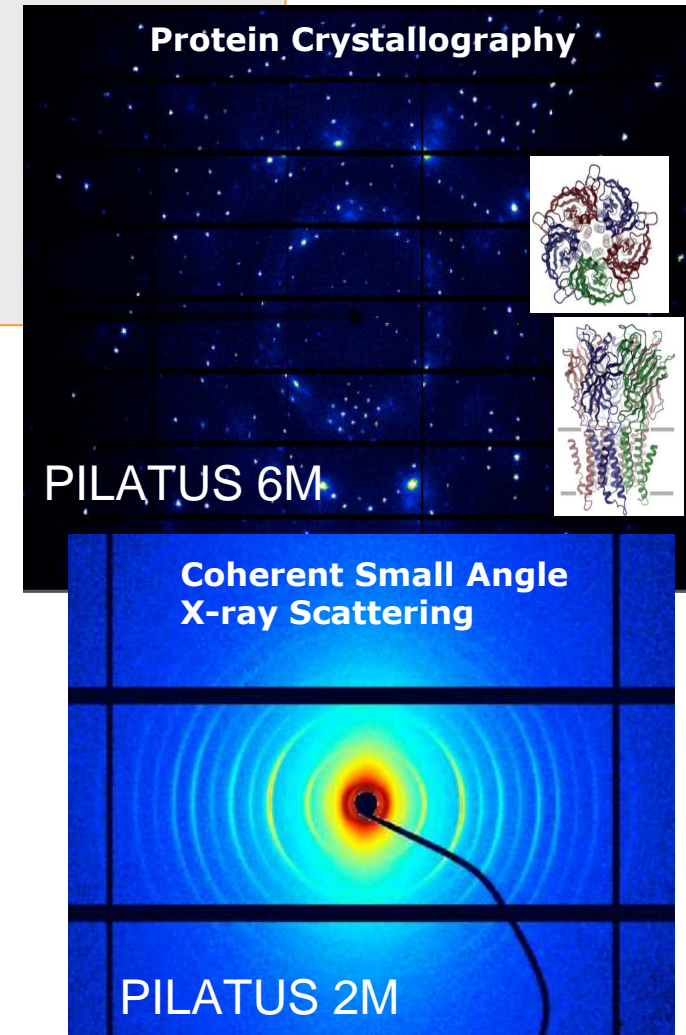
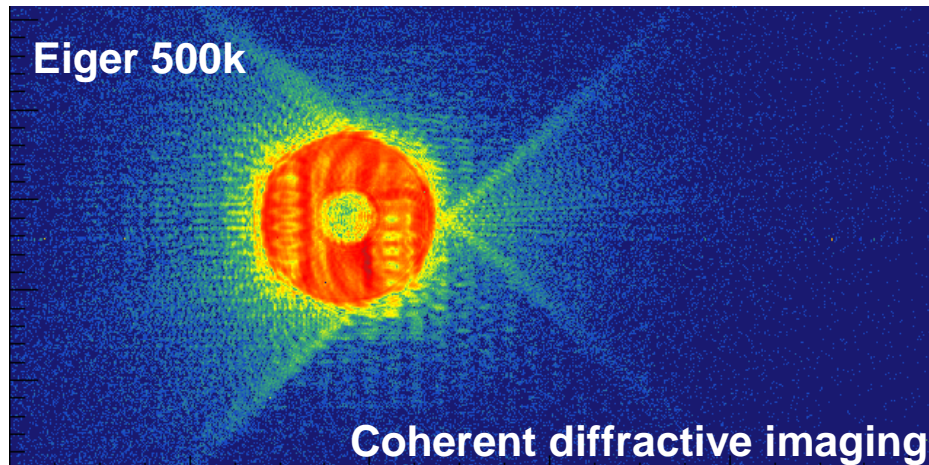
## Bump bonded pixel sensor



- Bump bonding requires additional processing of the chip and sensor surface to deposit an under-bump-metallization and the indium
- After reflow in the oven, the indium forms bumps

Single photon counting hybrid pixel detectors for synchrotron applications are aimed towards diffraction experiments

- Protein Crystallography
- Coherent Small Angle X-ray Scattering
- Coherent Diffractive Imaging
- X-ray Photon Correlation Spectroscopy

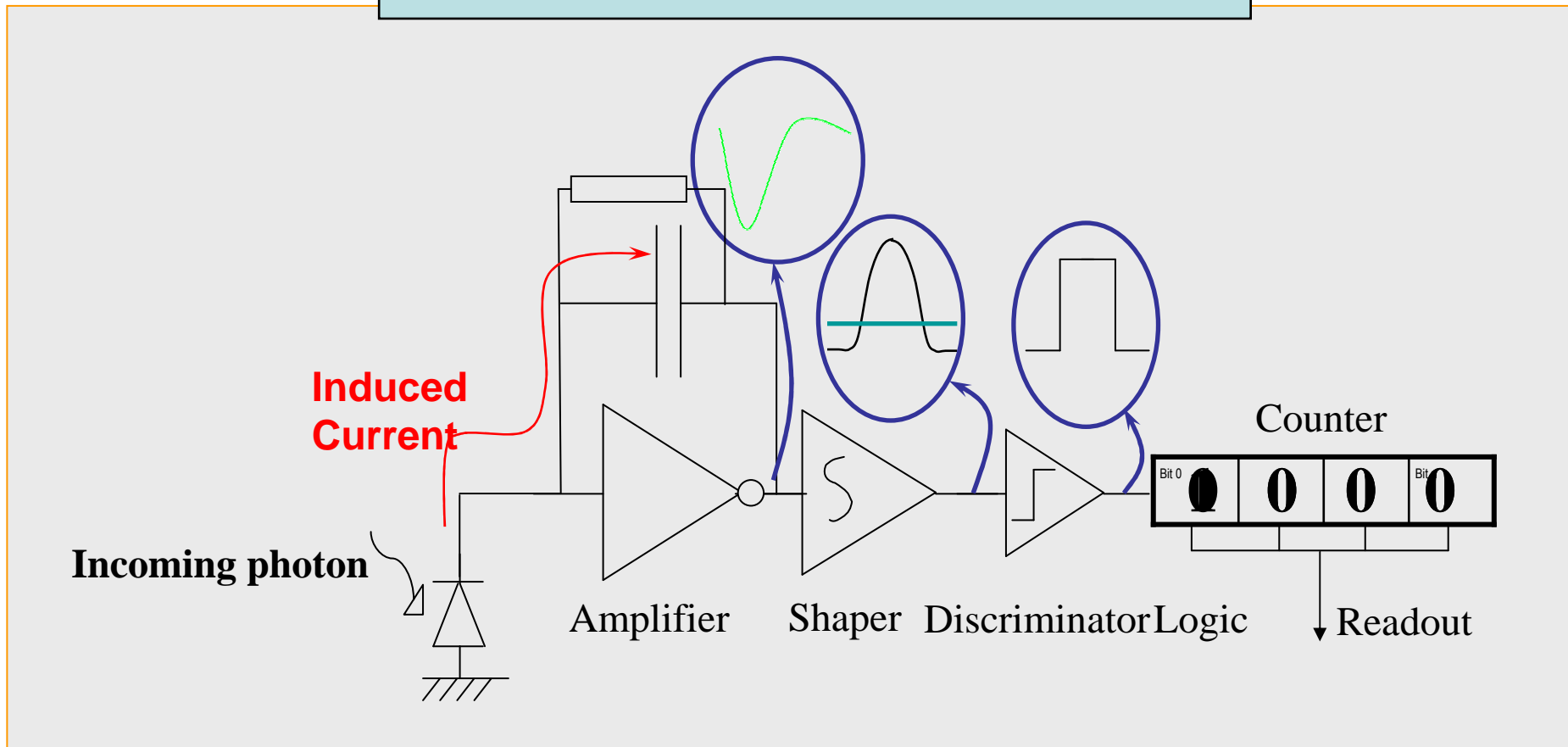




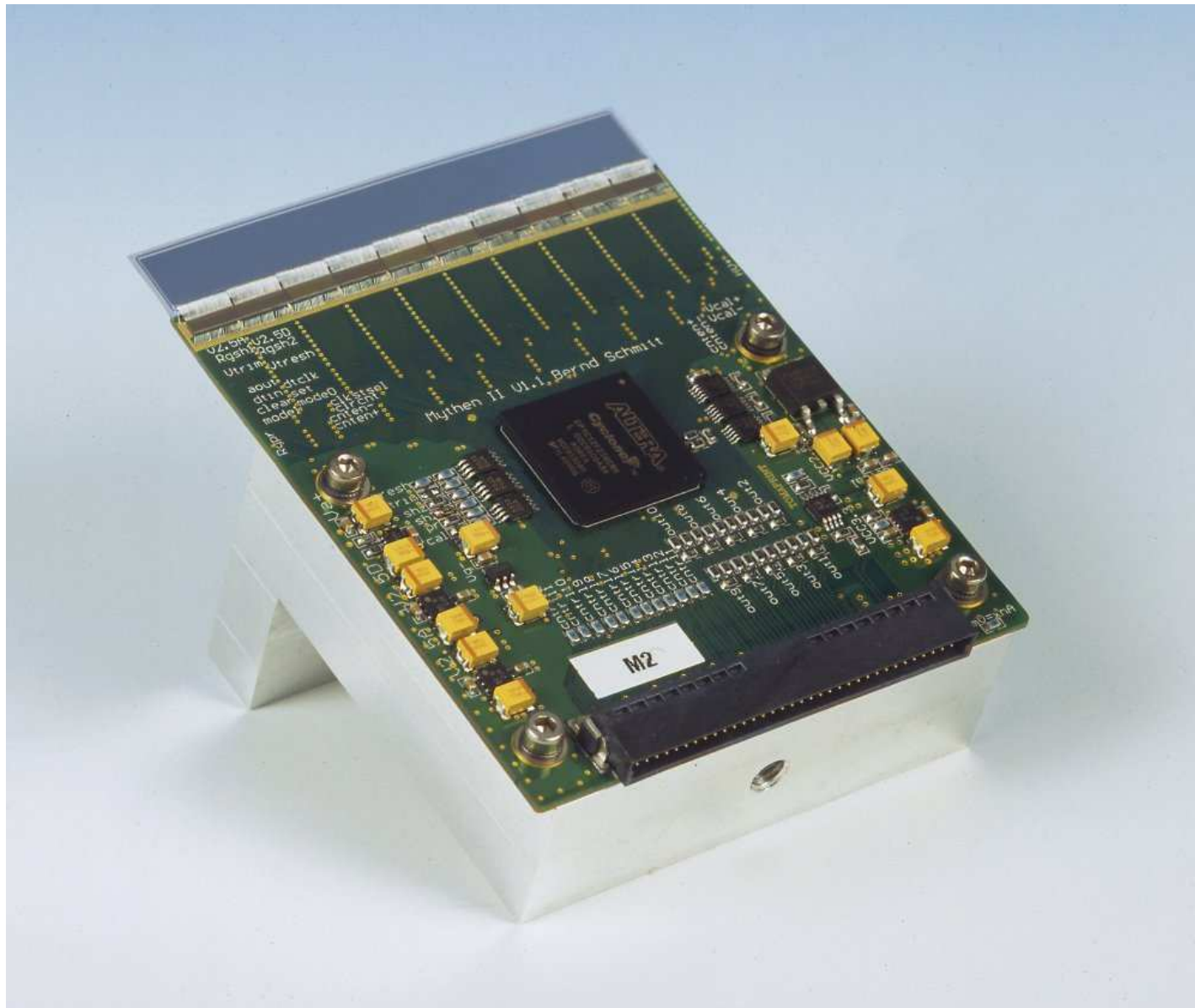
- Specs definition
- Chip design CAD maintenance (HW and SW)
- ASIC design
- Sensor design
- Bump-bonding masks design
- Bump bonding
- Wirebonding
- Design of the ASIC test system (HW, firmware, SW)
- ASIC tests

- Full readout system (HW, firmware, SW)
- Mechanics and cooling design (and partly production)
- Data transfer to long term storage
- Design of the wafer testing system
- Detector assembly
- Detector tests
- Detector commissioning
- Detector „mass“ production
- Detector support

## Simplified working scheme of a channel



# Mythen II



(MythenI: 2002-2007)

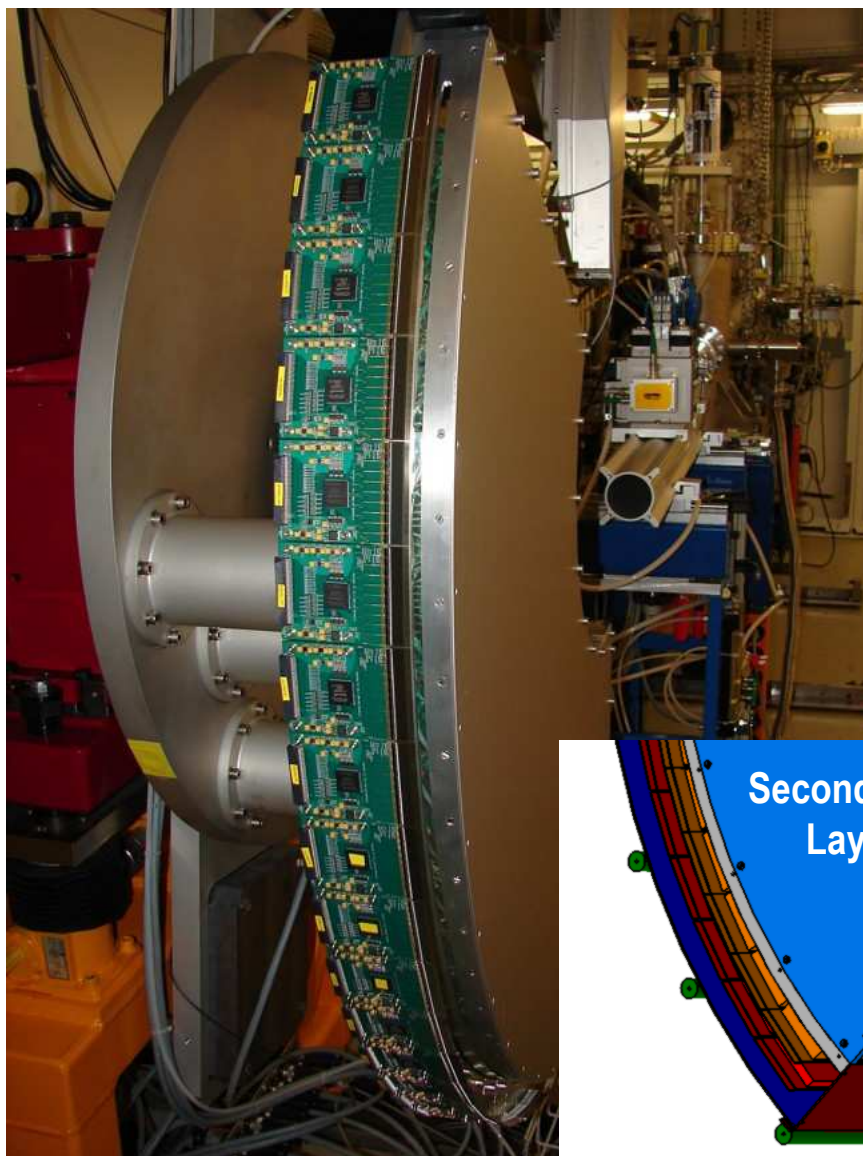
**Silicon sensor** with 1280 strips  
8 mm long, 50  $\mu\text{m}$  pitch, 300  $\mu\text{m}$  thick

## Read out chip:

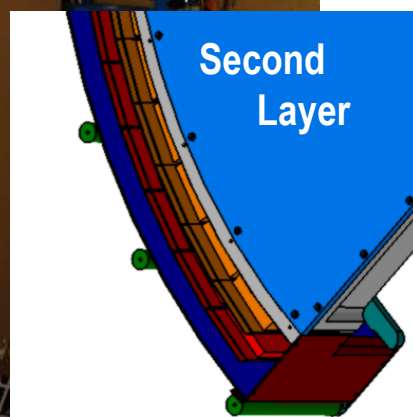
- 0.25  $\mu\text{m}$  readout chip, 128 channels
- low noise preamp: 190-240  $e^-$  ENC
- 6 bit DAC for threshold fine tuning  
1.4keV without trimming and 140eV Trimmed  
Minimum threshold: 3keV
- 24 bit binary counter
- Readout Time: variable length (4-24bits)



## Mythen II full detector



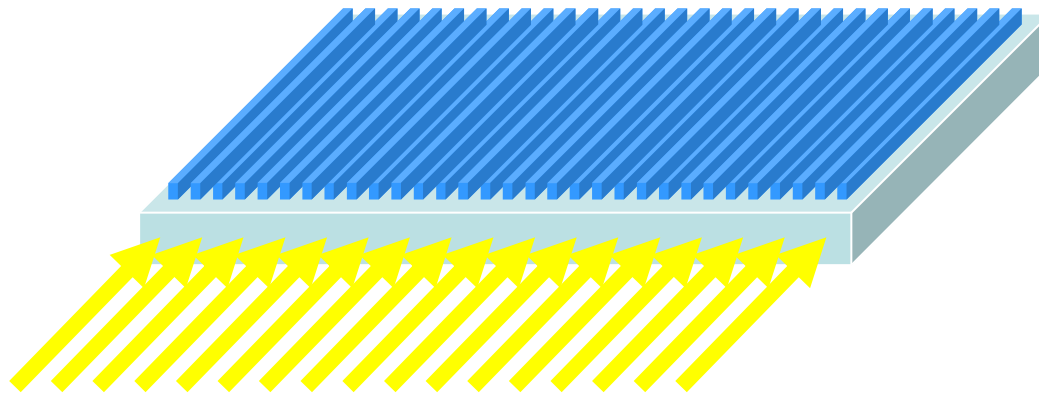
- full 120° spectrum taken in less than a second
- makes measurements 5000-15000 times faster
- solves problem of radiation damage in organics
- unique tool for time resolved 1D experiments (powder diffraction)



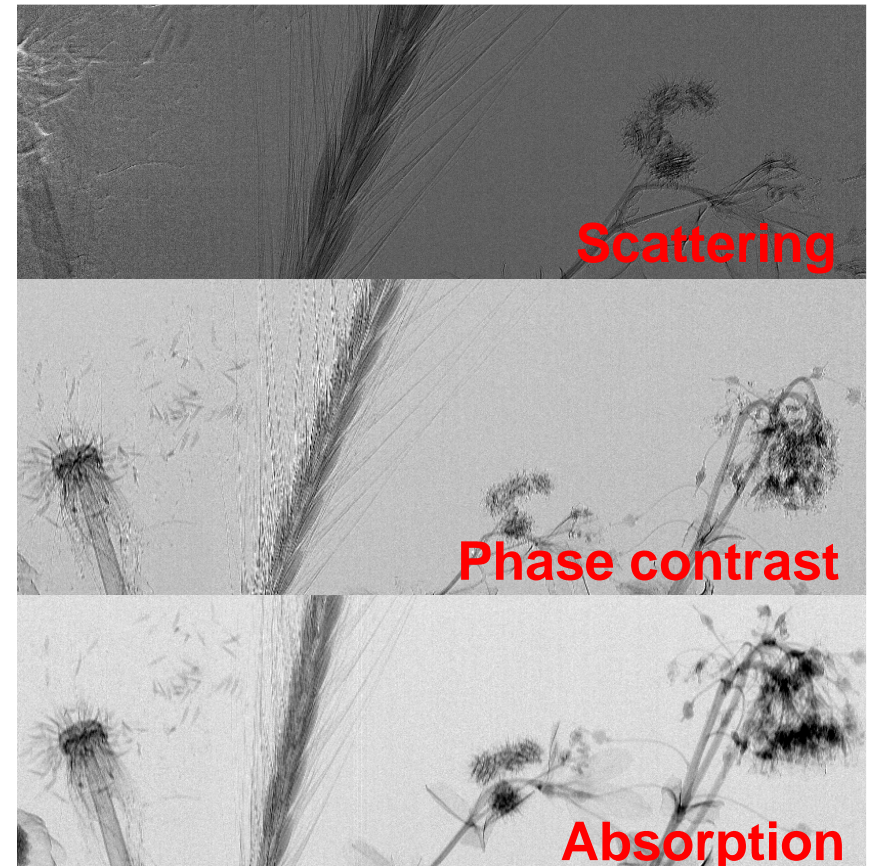
120° Mythen system at the Powder diffraction end station, MS beamline

Sensor oriented with the strips parallel to the beam

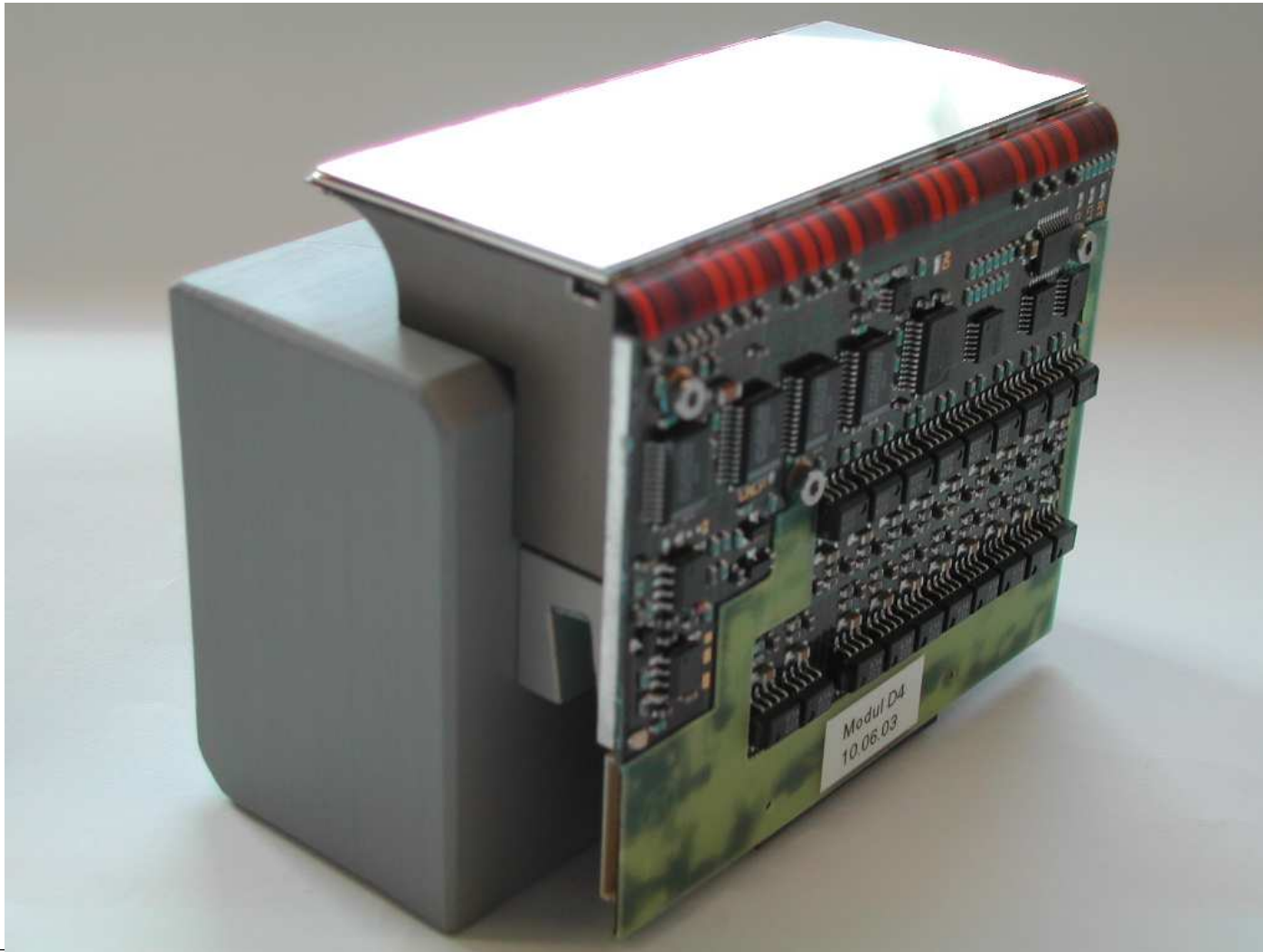
- Custom sensor to improve the efficiency at 20 keV



Measurements performed at the medical imaging beamline at Elettra (Italy)

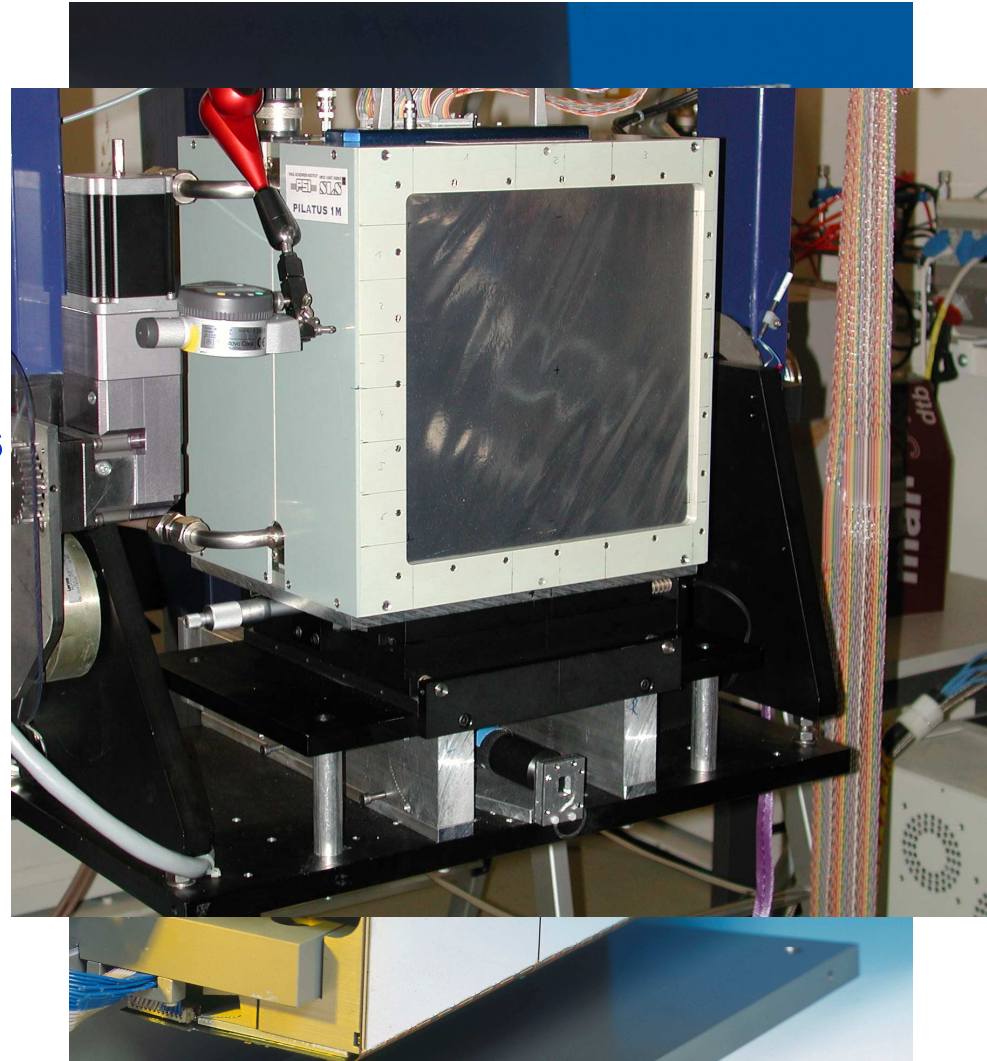


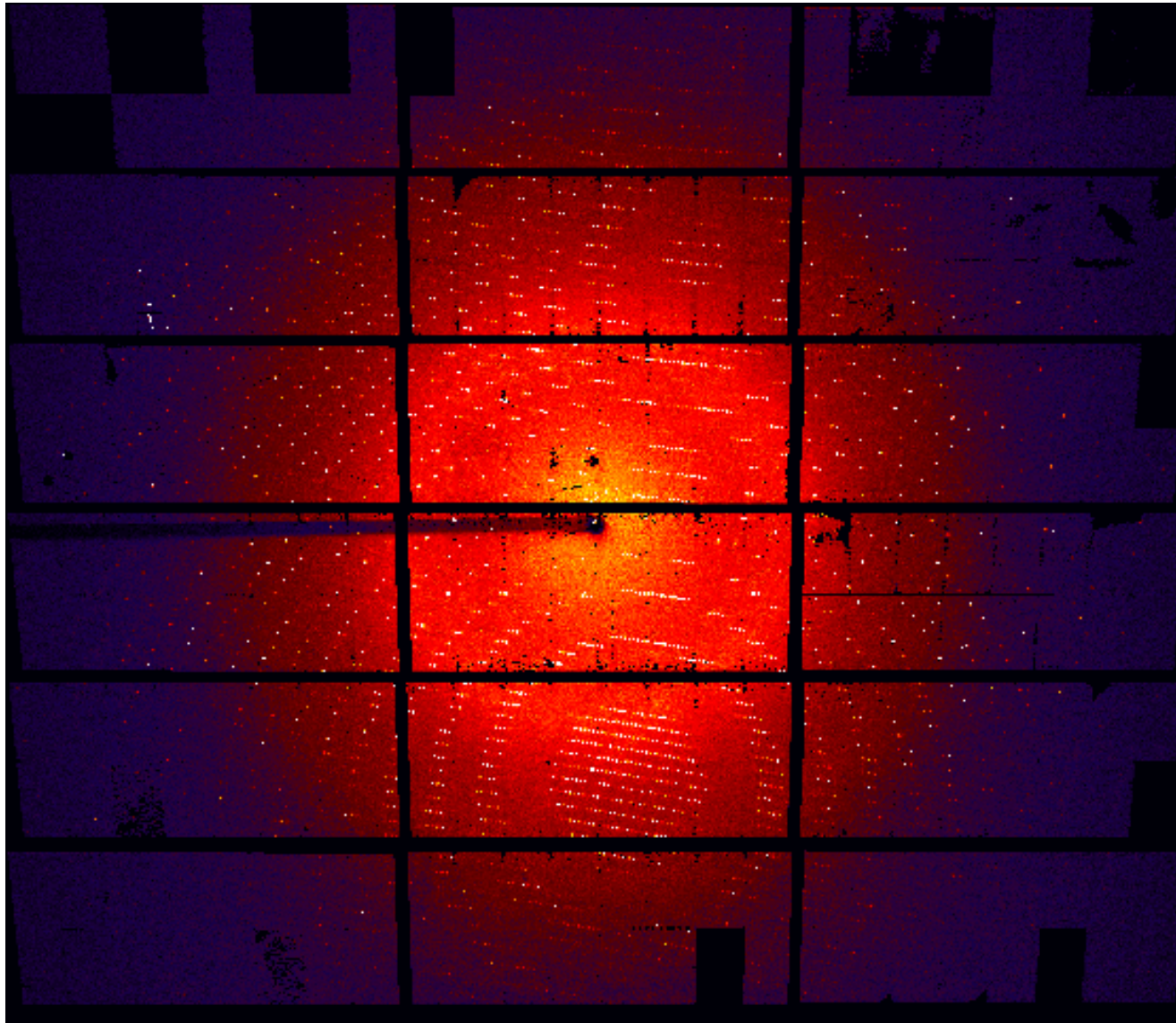
## Demonstrate feasibility of large area hybrid pixel detectors for synchrotron radiation detection





- DMILL rad-hard technology
- Pixel size: 217x217  $\mu\text{m}^2$
- Chip pixel array: 44 x 78
- Largest pixel detector array for SR
- 6 banks a 3 modules, 1120 x 967 pixels
- Area: 21 x 24  $\text{cm}^2$
- 288 chips  $\rightarrow$   $\sim 300 \times 10^6$  transistors
- Readout time: 6.7ms
- 2 frames/ s
- Active area: 85%
- Moderate count rates (<10kHz/pixel)





## Data Taking:

Data set: 120°

Exp Time: 4s

Integration: 1°

Beam energy: 11.9 keV

Beam intensity: 13.5%

D Sample-Det: 128 mm

Resolution: 1.4 Å

## Analysis:

3 data sets merged

full geometrical correction

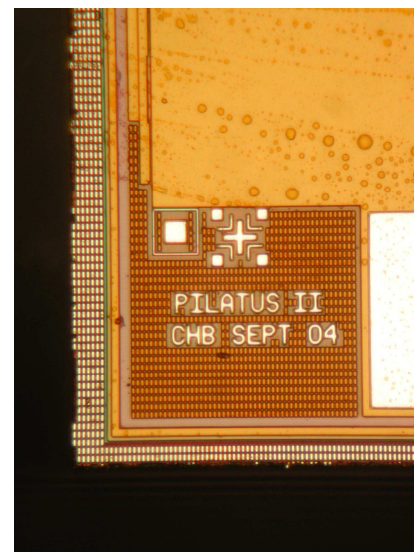
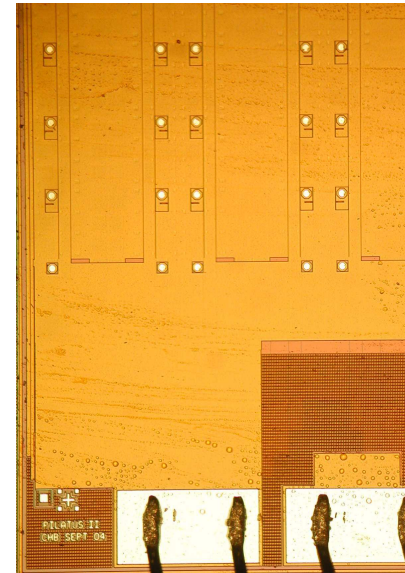
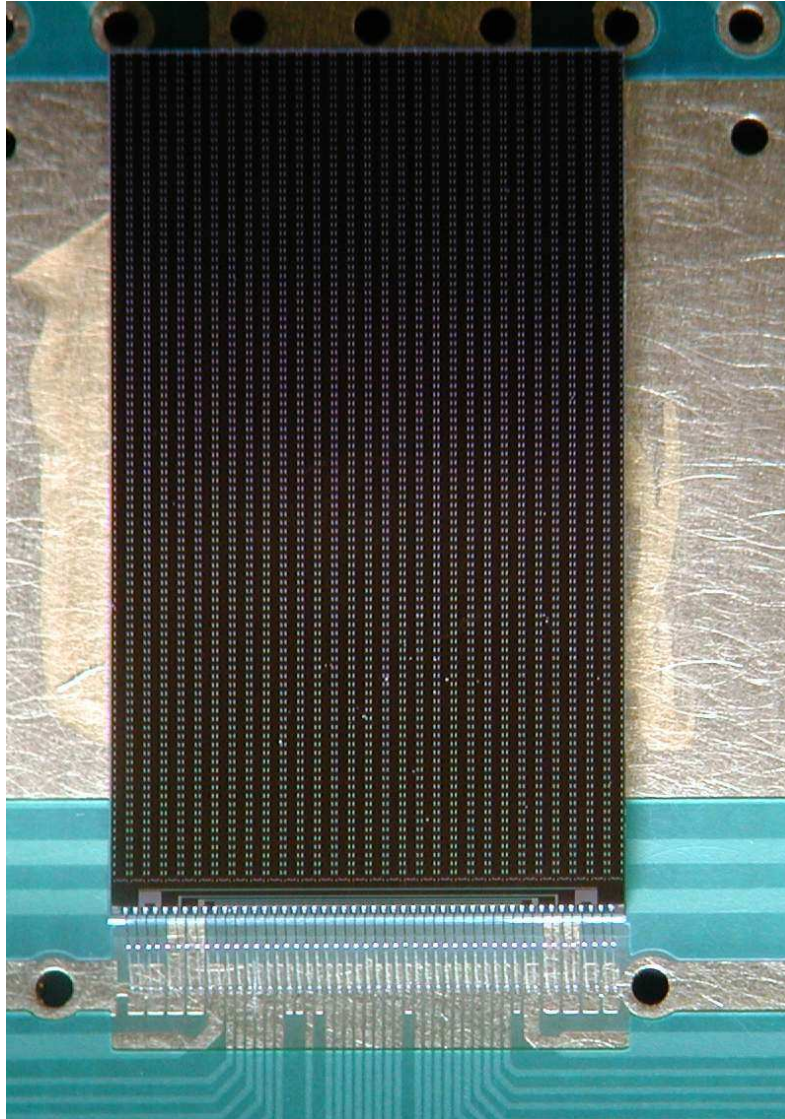
Processed with XDS

$R_{\text{obs}}$ : 8.9% (overall)

Completeness: 90%  
(98% up to 1.6 Å)

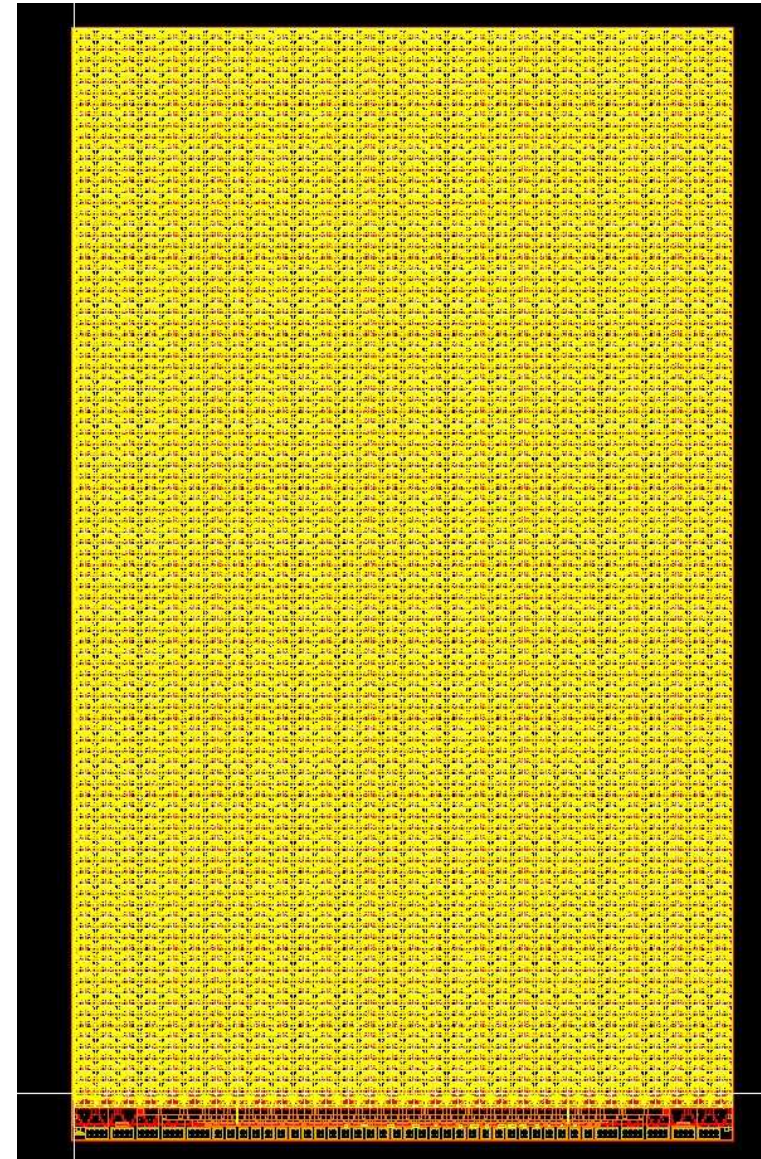


# PILATUS II





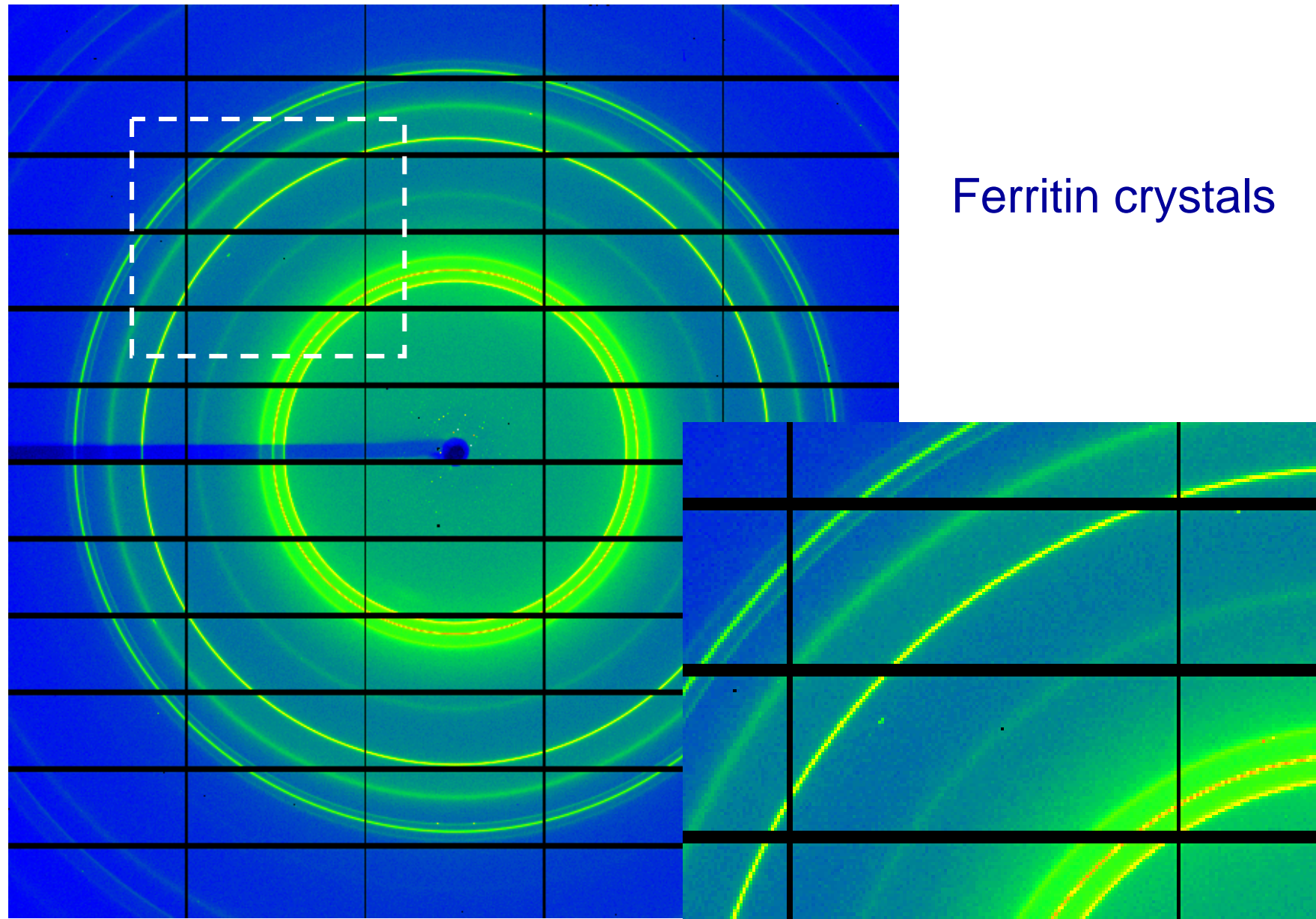
- **UMC\_25\_MMC process; Radiation hard design**
- **60 x 97 pixels = 5820 pixels**
- **Pixel size 172 x 172  $\mu\text{m}^2$**
- **17.540 x 10.450  $\text{mm}^2$**
- **Count rate: 1MHz/pixel**
- **20 bit counter**
- **Counting timer circuit**
- **6 bit DAC for threshold adjustment**
- **XY-adressable**
- **Analog output**
- **100 MHz LVDS readout ( $T_{ro} = 1.2 \text{ ms}$ )**
- **Submitted 29.09.04**
- **Received 1.12.04**       **$4 \cdot 10^6$  Transistors**





<b>No of Modules</b>	<b>60</b>
<b>Module size</b>	<b>487 x 195 pixels (90k)</b>
<b>Detector Size</b>	<b>431 x 448 mm<sup>2</sup></b>
<b>No of Pixels</b>	<b>2527 x 2463 pixels (6.2 * 10<sup>6</sup> pixels)</b>
<b>Spatial resolution</b>	<b>0.172 x 0.172 mm<sup>2</sup></b>
<b>Dynamic range:</b>	<b>20bits</b>
<b>Readout time</b>	<b>~2ms</b>
<b>Frame rate</b>	<b>5-10 Hz</b>
<b>Rate</b>	<b>1 MHz/pixel</b>
<b>Spatial distortion</b>	<b>Flat geometry</b>
<b>Dead area</b>	<b>~8.4 % (7 pixels in x, 17 pixels y)</b>
<b>Operation mode</b>	<b>Fine <math>\phi</math>-slicing</b>









## Requirements:

- X-ray sensitive  
Energy range few keV to 25 keV
- Single photon sensitivity  
Low noise
- Sufficient angular coverage  
Large area
- Spatial resolution  
Millions of small pixels
- High count rate capability  
Count rates in the millions of counts/pixel/second
- High frame rates  
Tens of kHz, parallel acquire/readout



# EIGER main features (I)

Technological process	UMC 0.25 $\mu\text{m}$
Radiation tolerance	Full radiation tolerant design (>4Mrad)
Analog Parameters	30 ns peaking time ~150 ns ret. Zero 8.8 $\mu\text{W}/\text{pixel}$ = 2.3 / Gain: 44.6 $\mu\text{V}/\text{e}^-$
Chip size	19.3 x 20.1 $\text{mm}^2$ (active 19.2x19.2 $\text{mm}^2$ ) > 2 x
Pixel size	75 x 75 $\mu\text{m}^2$ = / 5.3
Pixel array	256 x 256 = 65536 = 11.3 x
Count rate	3.4 x 10 <sup>9</sup> x-rays/ $\text{mm}^2/\text{s}$ = 5.3 x (1-2 Mcounts/pixel/s)
Transistors, Matrix:	28.44M = 9.5 x
Periphery:	>120 000
Transistors density:	430/pixel, ~5 x

**In red:**  
Improvement  
factor with  
respect to  
PILATUS

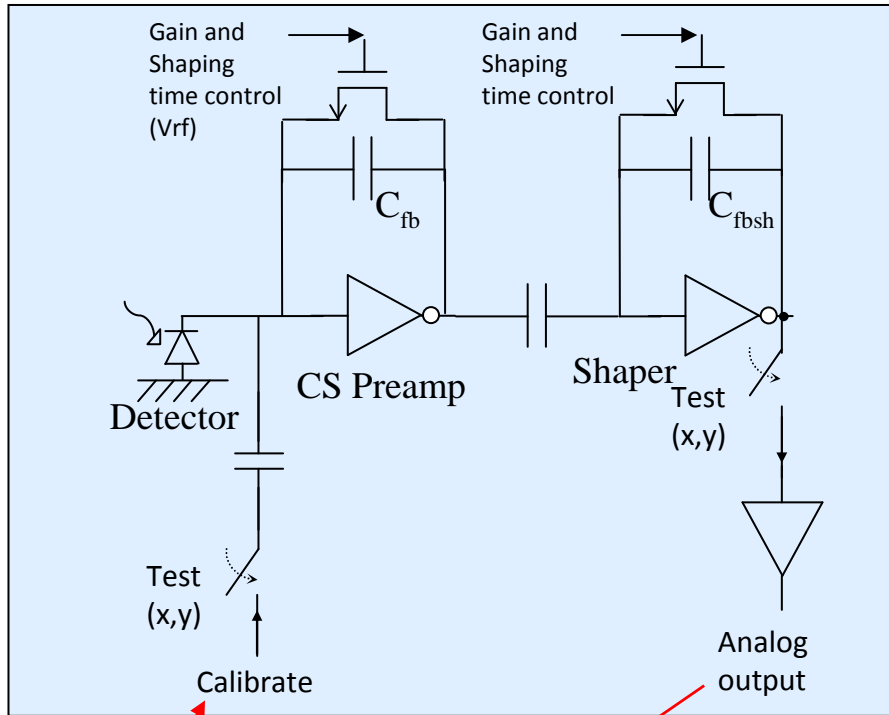
## EIGER main features (II)

<b>Nominal power supplies</b>	1.1 V (analog), 2V (digital), 1.8V (I/O)
<b>Counter</b>	12 bits, <b>binary, configurable (4,8,12 bit mode), double buffered</b>
<b>Continuous readout</b>	<b>yes</b>
<b>Detector readout speed</b>	~11 KHz @ 8 bit mode, (22 @ 4 bit) <b>Detector size doesn't matter</b> <b>= up to ~2000 x</b> <b>(Clock=100 MHz DDR)</b>
<b>Threshold adjustment</b>	6 bit DAC
<b>XY-addressable analog out for testing</b>	<b>yes</b>
<b>Overflow control</b>	<b>yes</b>

**Both the chip and the readout electronics were totally redesigned, and almost all chip blocks are on silicon for the first time.**

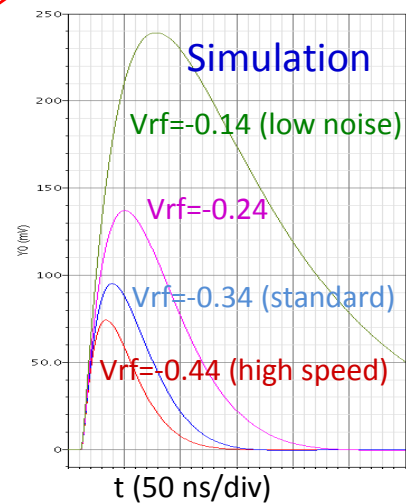
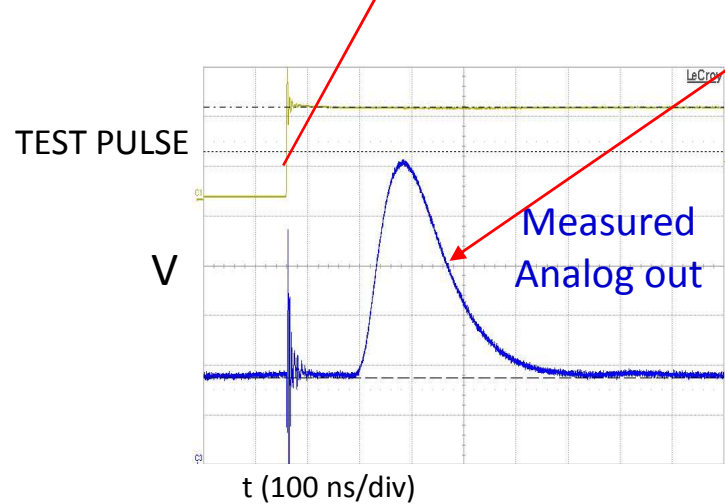
**Project start: 02.2005, chip design as a one man project**

# The EIGER pixel, analog part



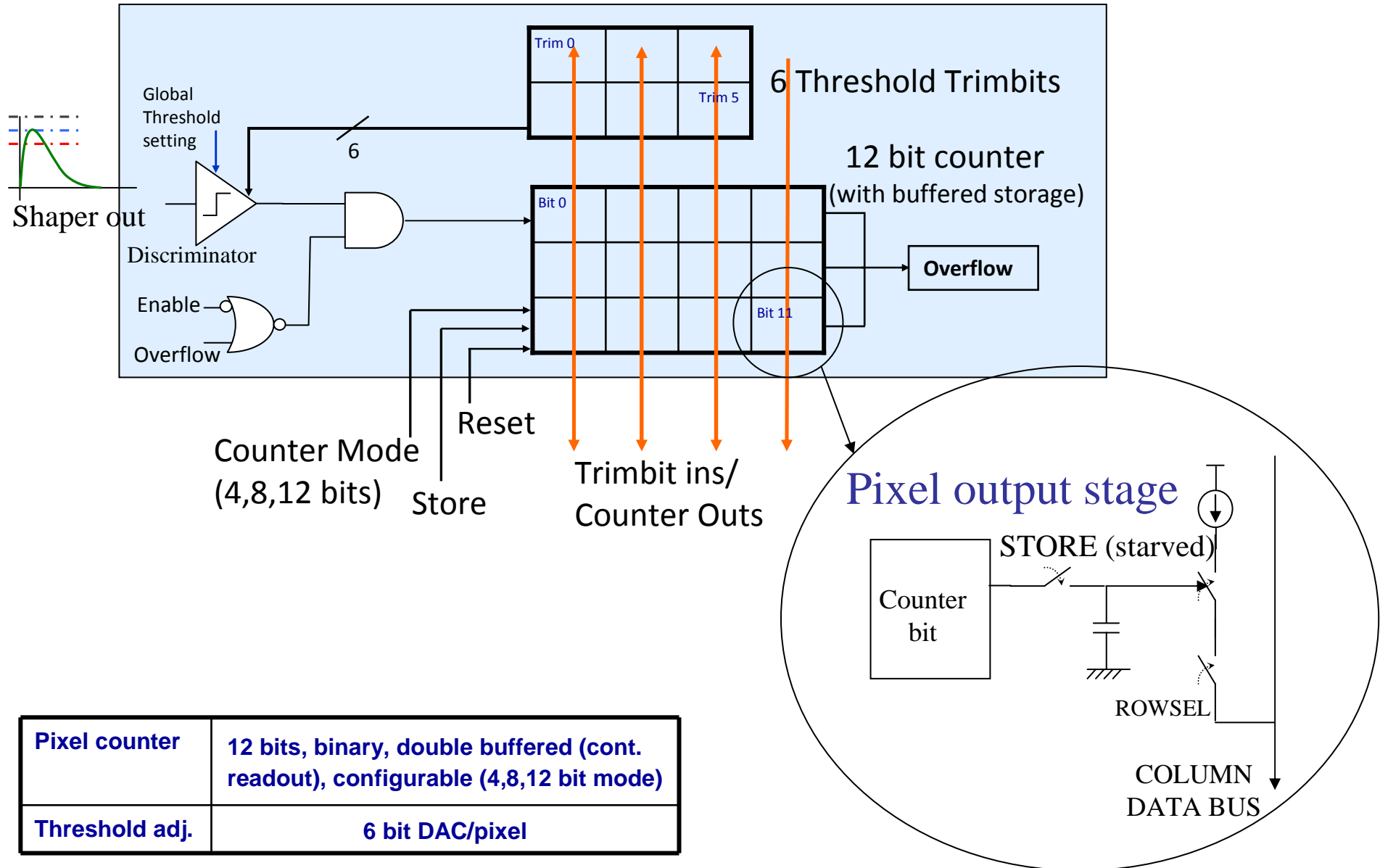
Simulated parameters with standard settings

<b>Gain</b>	<b>44.6 <math>\mu\text{V/e}^-</math></b>
<b>Timing</b>	<b>151 ns (Ret.to 0 @ 1%)</b>
<b>Noise (simul.)</b>	<b>135 e-rms</b>
<b>Static power</b>	<b>8.8 <math>\mu\text{W/pixel}</math> (<math>\sim 0.6\text{W/chip}</math>)</b>

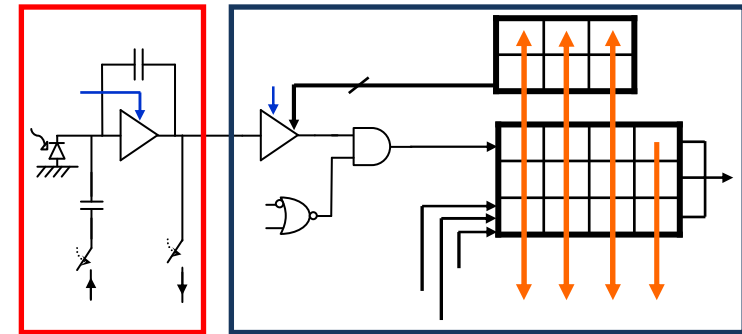
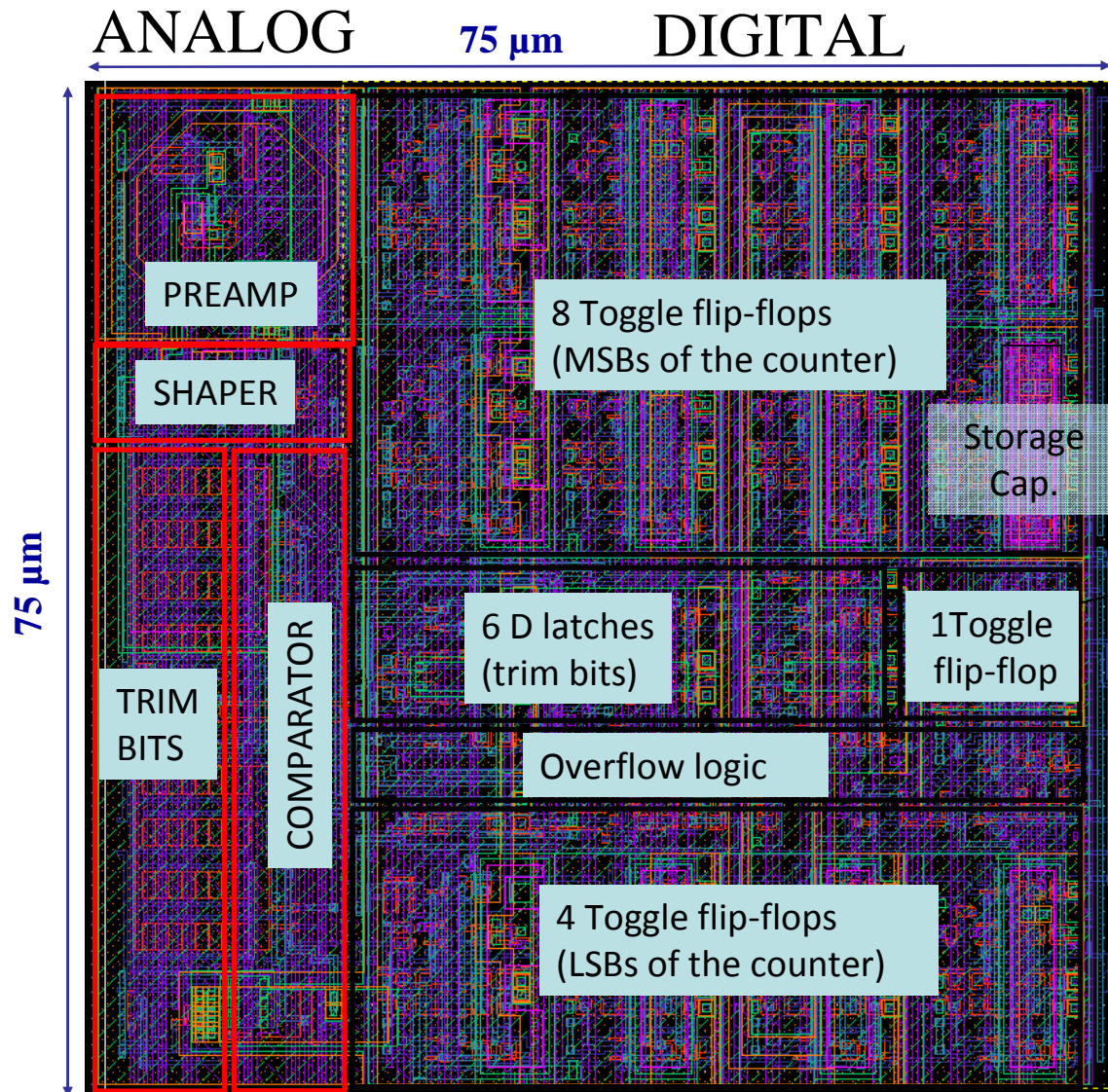




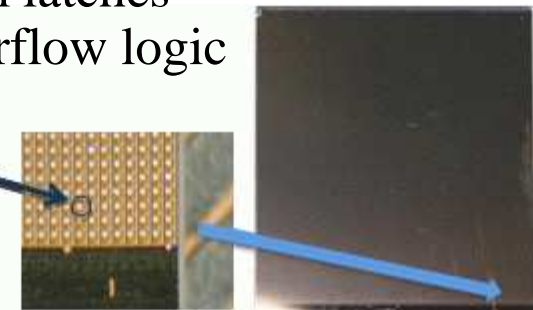
# The EIGER pixel, digital part



# The EIGER pixel on silicon

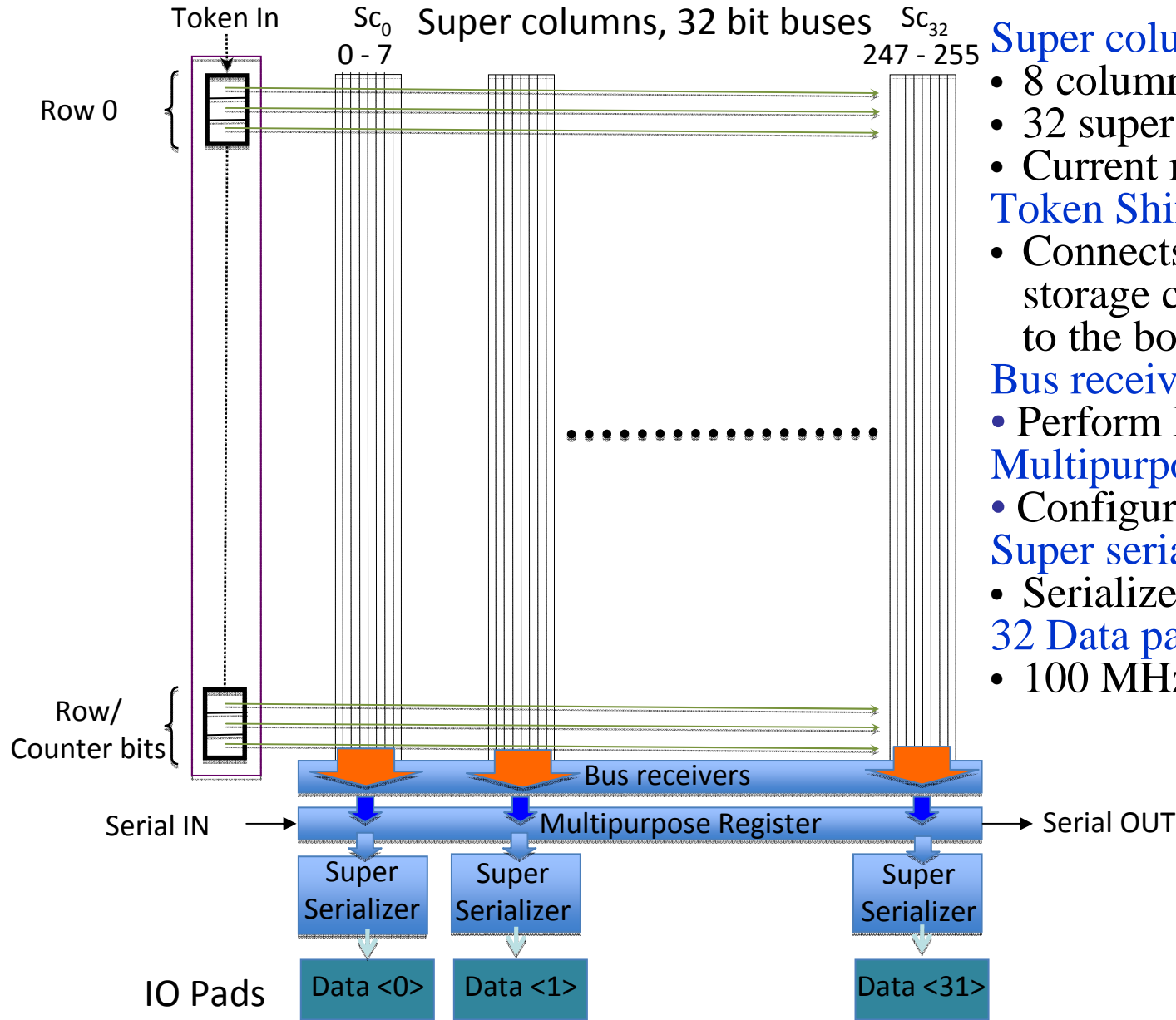


- Bump bond connection
- Preamp (TWELL)/shaper
- Comparator
  - Global threshold plus pixel trimming (6 bits)
- 12 bit counter
  - Counter logic
  - Buffered storage
  - Trim latches
  - Overflow logic



UMC 0.25 um Technology, full radiation tolerant layout; very high transistor density: 430 transistors/pixel, 5 metal layers only

# EIGER readout architecture



## Super column structure

- 8 columns/super column
- 32 super columns
- Current mode data buses

## Token Shift Register

- Connects 4 bits of the counter storage cells or trimbits of a row to the bottom register

## Bus receivers

- Perform I/V conversion

## Multipurpose register

- Configurable serial/parallel I/O

## Super serializers

- Serialize data sent to the pad

## 32 Data pads

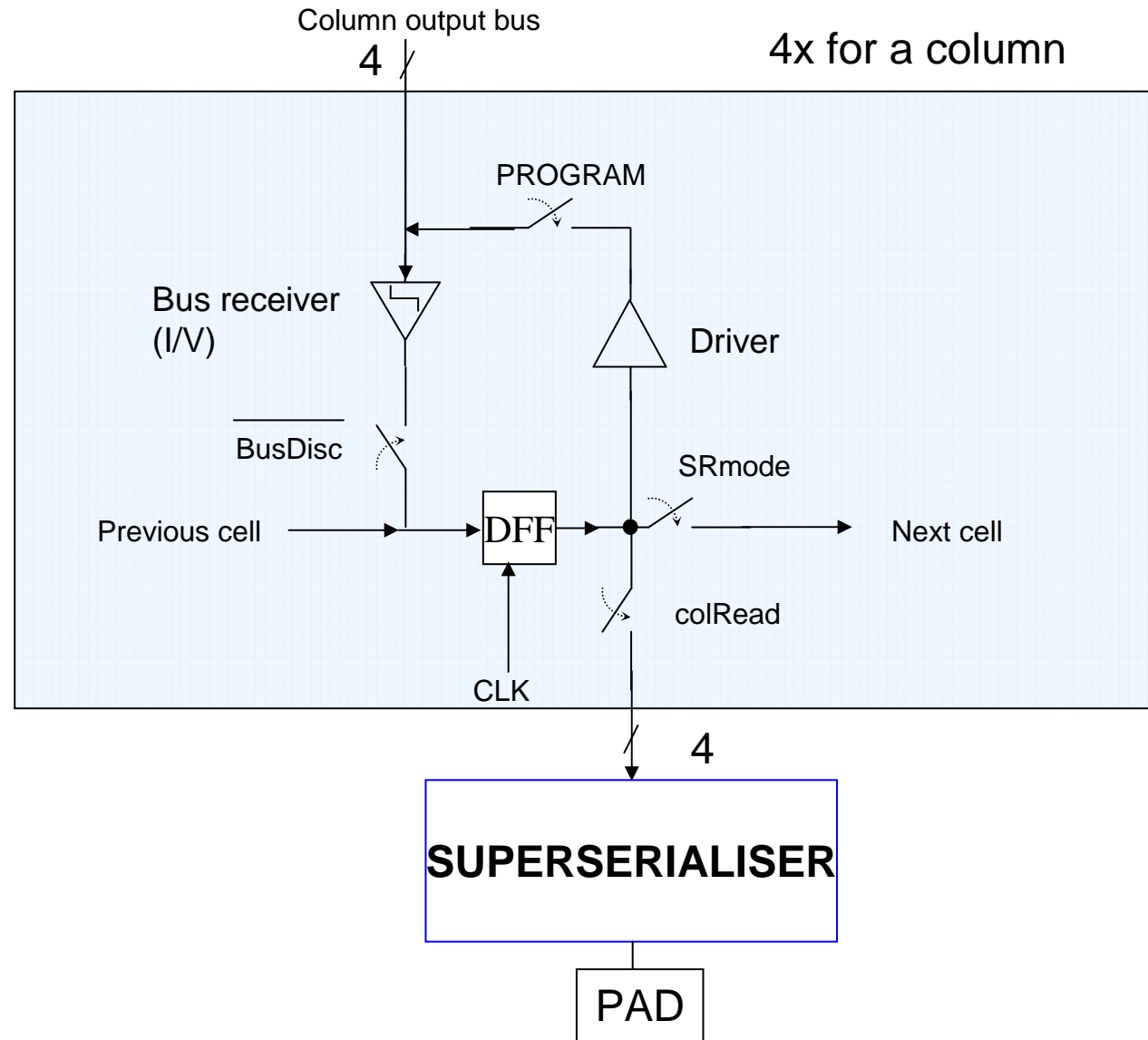
- 100 MHz DDR, TWELL



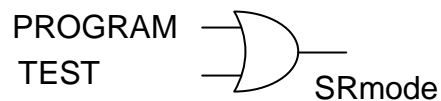
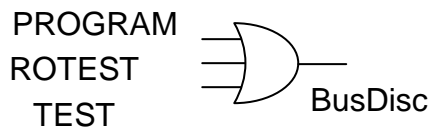
# Basic cell of the multipurpose shift register

## Modes of operation:

- Data taking
- Test
- RO test
- Program
- Serial readout



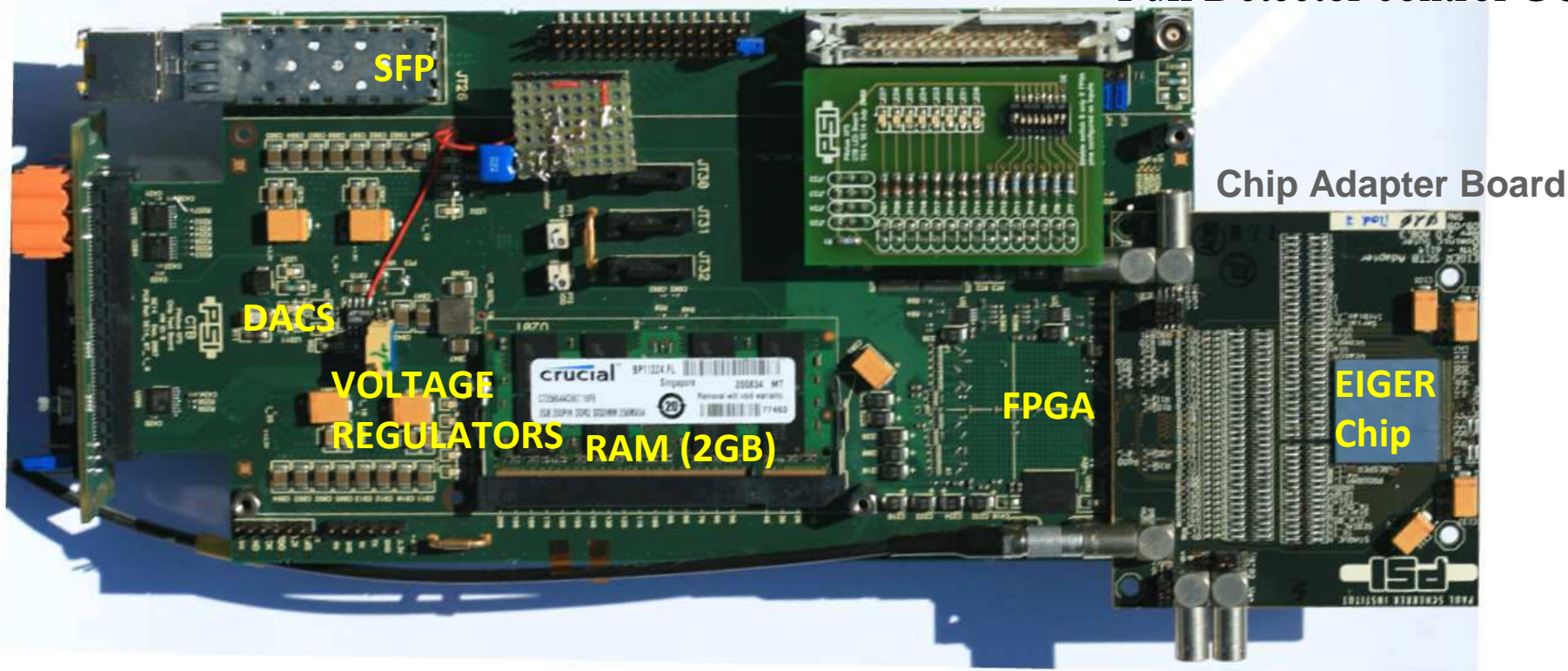
## CHIP CONTROL



# Single chip test setup

- Pattern generator
- Python scripts
- Full Detector control GUI

1Gb Ethernet Data Link

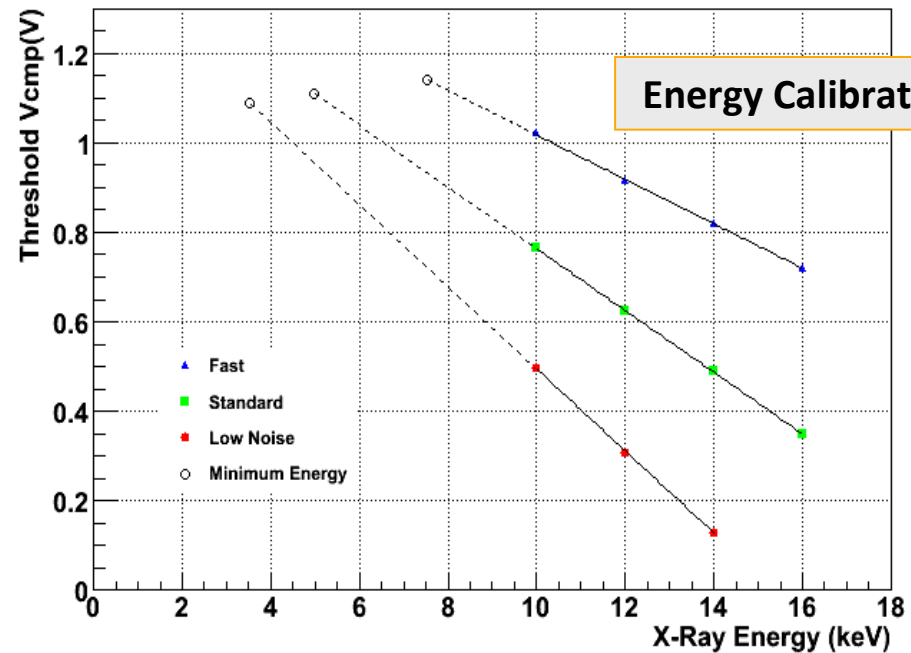
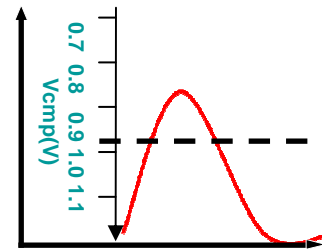
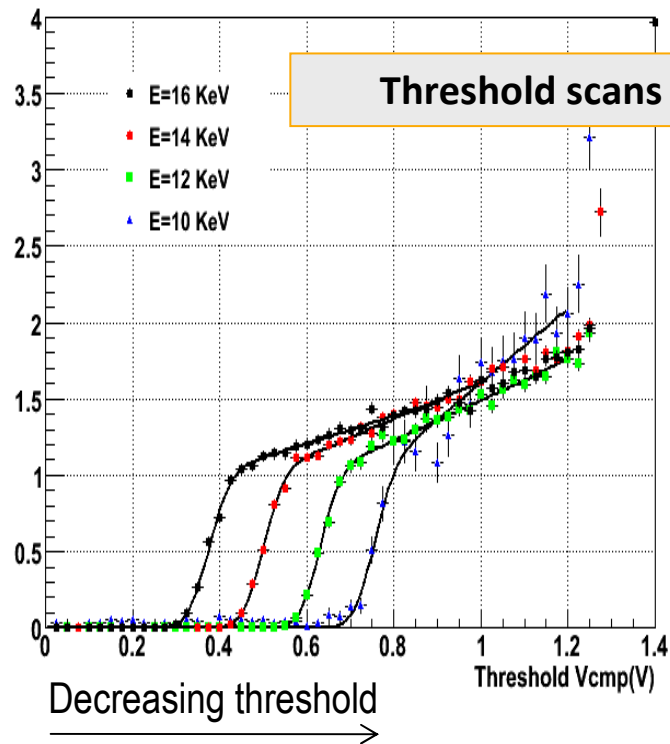


**ALL WAFERS FROM FOUNDRY WERE OFF SPECS!**

- Energy calibration
- Noise
- Trimming and threshold dispersion
- Rate capability
- Minimum energy
- Radiation tolerance

# Energy Calibration

- Energy Calibration: Monochromatic beam of known energy
- Threshold scans: Number of counts in each pixel vs Threshold

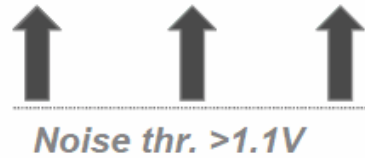


Fitting Function:  
Scurve·ChShar

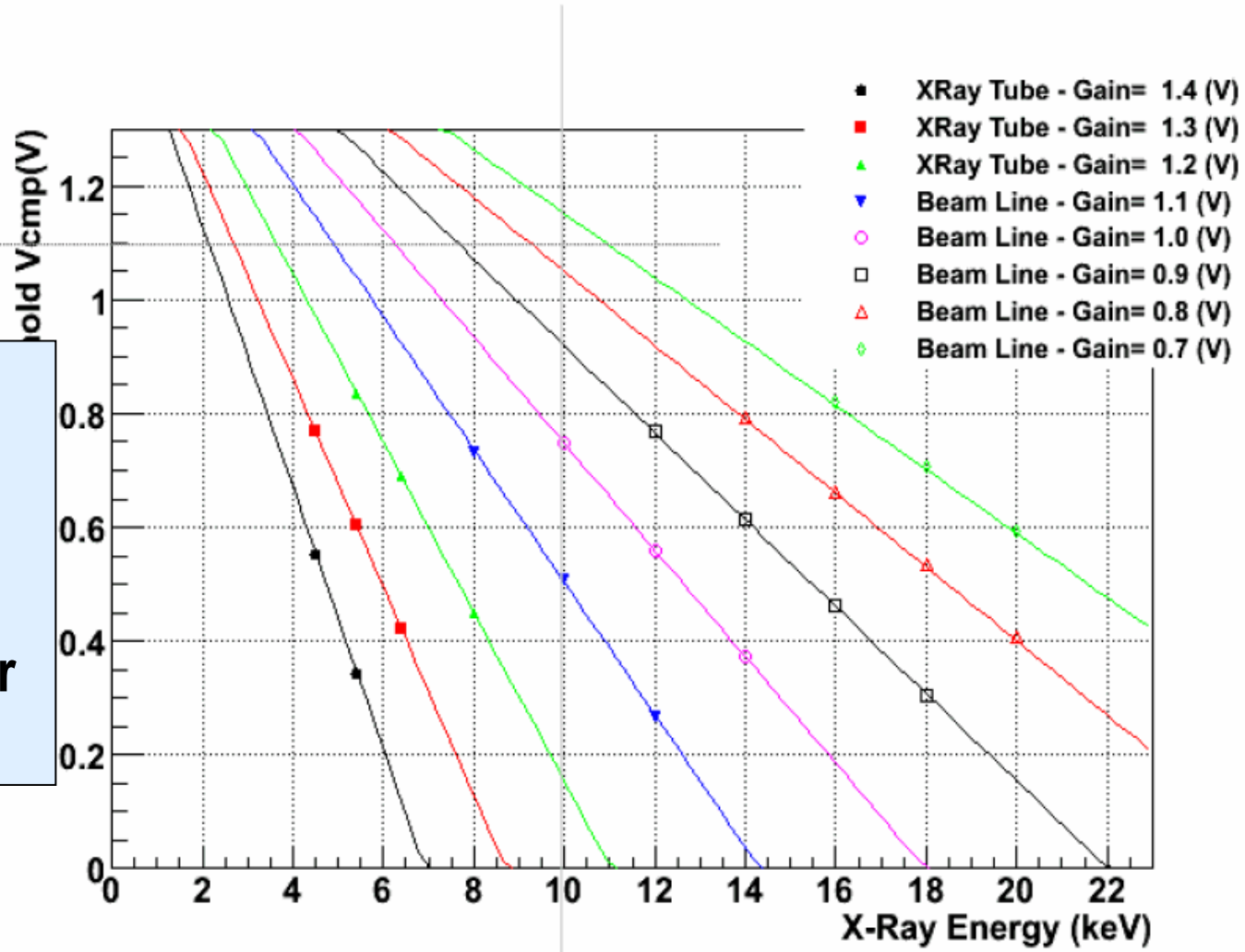
$$n(V_{cmp}) = \frac{1}{2} \left( 1 + \operatorname{erf} \left( \frac{V_{cmp} - a_0}{\sqrt{2} a_1} \right) \right) (a_2 + a_3 V_{cmp})$$

$a_0$  inflection point;  $a_1$  noise  
 $a_2$  flux;  $a_3$  charge sharing param.



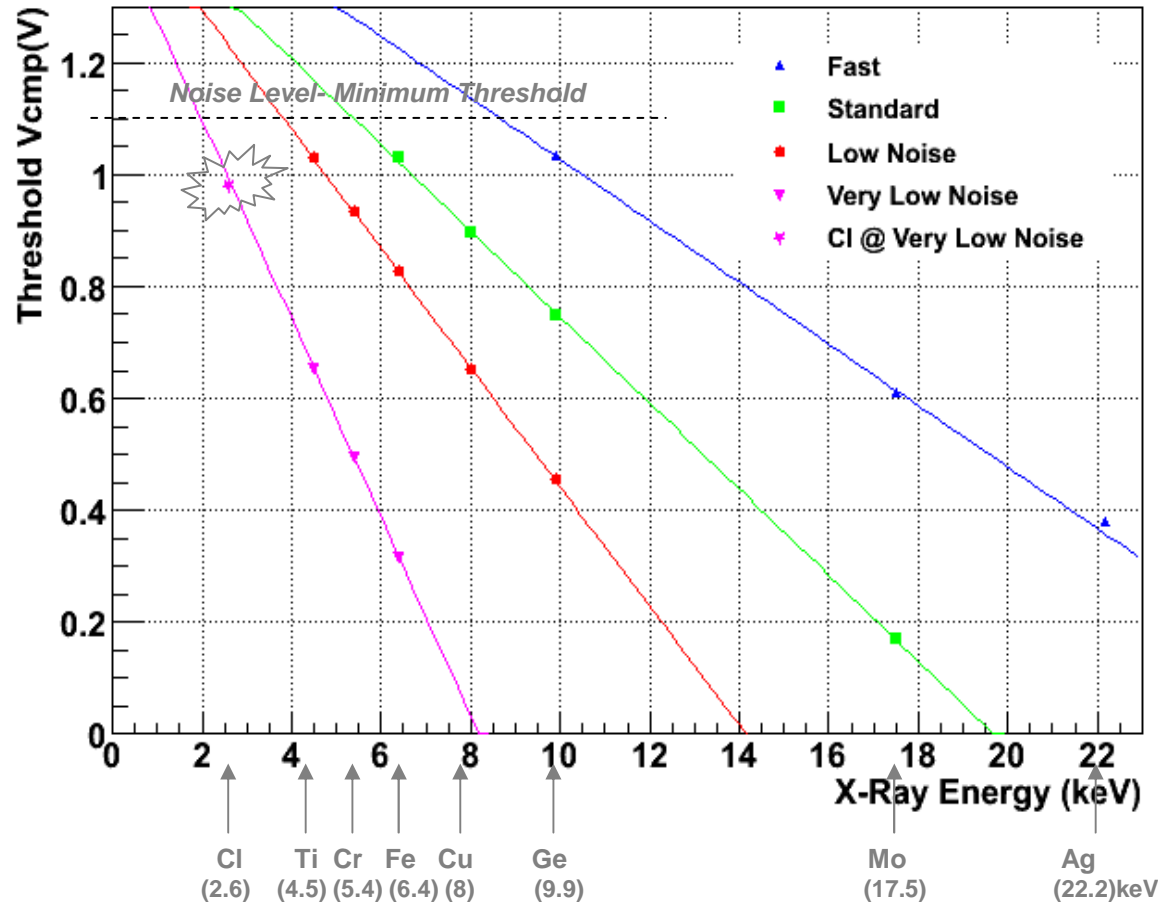


„Gain“ controls the feedback transistor bias. Increasing gain = less noise, slower ret. Zero.



# Low energy operation

- ❑ **Energy Calibration:** XRay tube and Fluorescence samples: from Ag (22KeV) to Ti (4.5KeV) and Cl (2.6KeV)
- ❑ **One new mode operation (Fuchsia):** “Very Low Noise” i.e. “Very High Gain of the Preamp.”

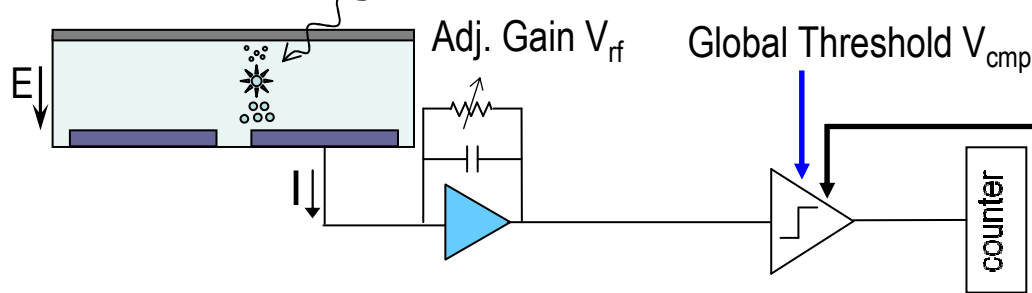


good performance of the chip at low energy:

- comparator is linear down to low energies
- minimum threshold  $V_{thr} \sim 1.1V$ ; safe operation of the comparator @ 1V
- threshold energy as low as 2.5keV can be set in the highest gain mode
- a further higher gain could also be investigated
- rate capability of “lower noise-higher gain” operation mode to be measured (good feedback from simulation )

# Trimming and Threshold dispersion

Monochromatic X-rays



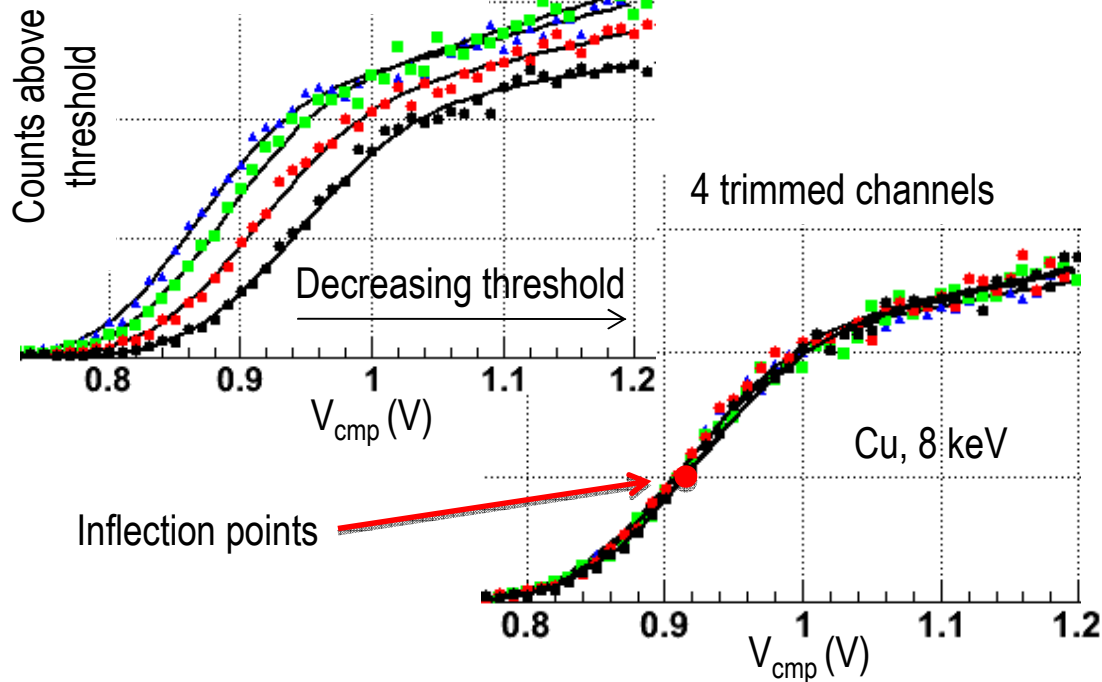
Trimbits

Trim 0		

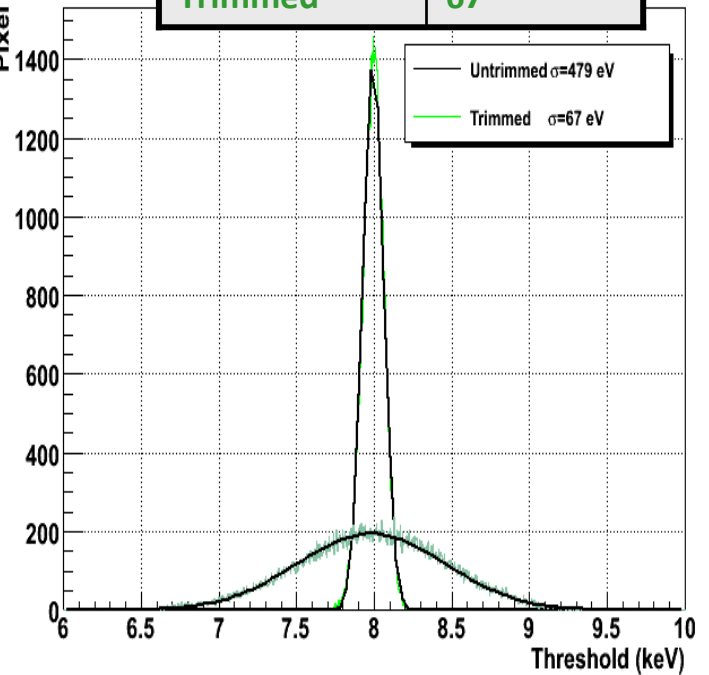
	$\sigma$ (eV)
Untrimmed	479
Trimmed	67

Threshold scan:

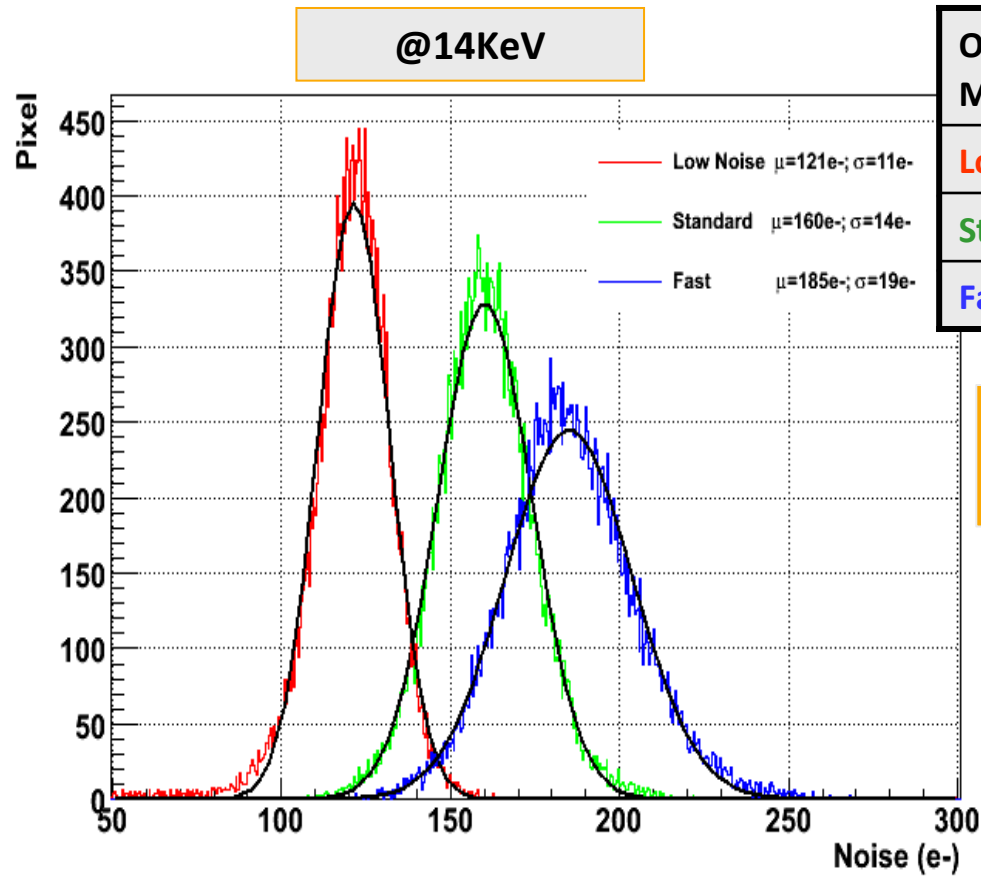
4 untrimmed channels



Number of channels



❑ **Noise distributions:** monochromatic beam at the Beam line

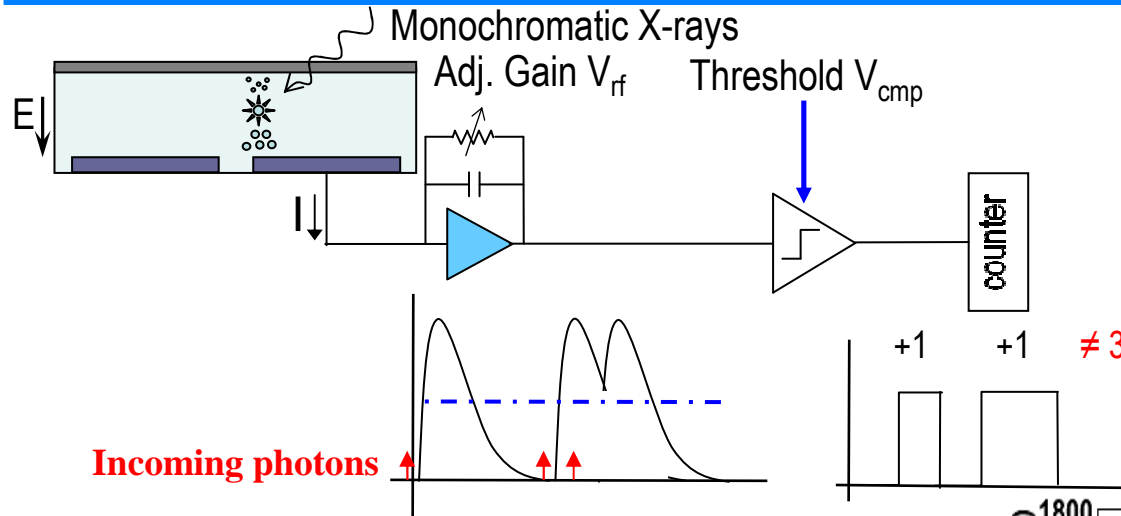


Operation Mode	Noise(e-)	Sigma (e-)
LowNoise	121.1±0.07	10.7±0.06
Standard	160.1±0.08	13.9±0.07
Fast	185.0±0.1	18.7±0.09

$$n(V_{cmp}) = \frac{1}{2} \left( 1 + \operatorname{erf} \left( \frac{V_{cmp} - a_0}{\sqrt{2a_1}} \right) \right) (a_2 + a_3 V_{cmp})$$

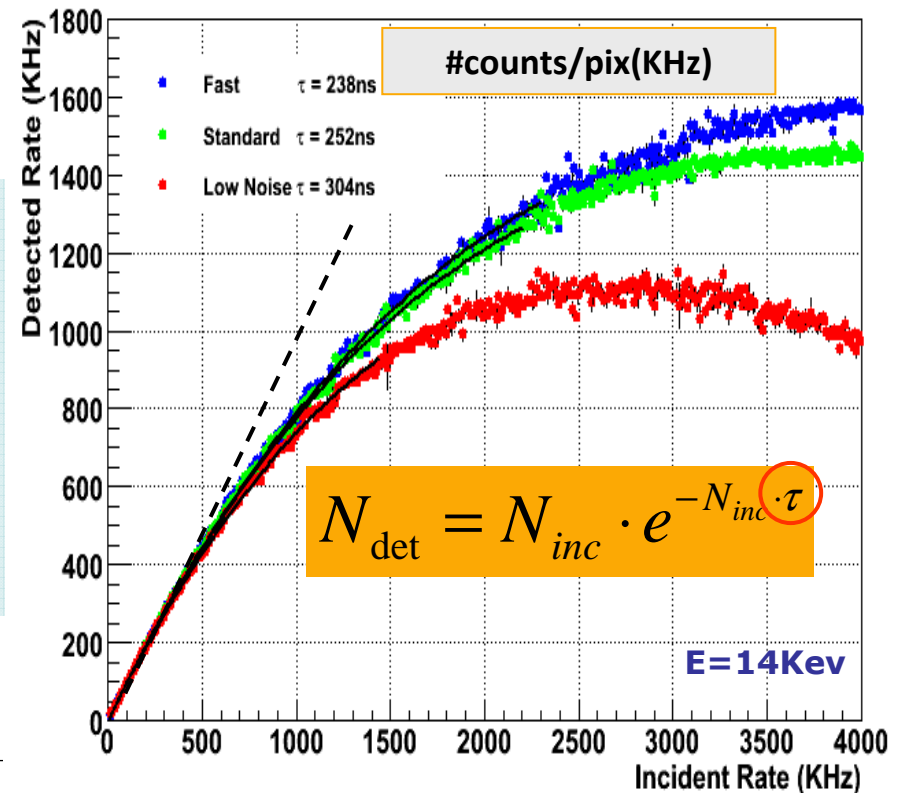


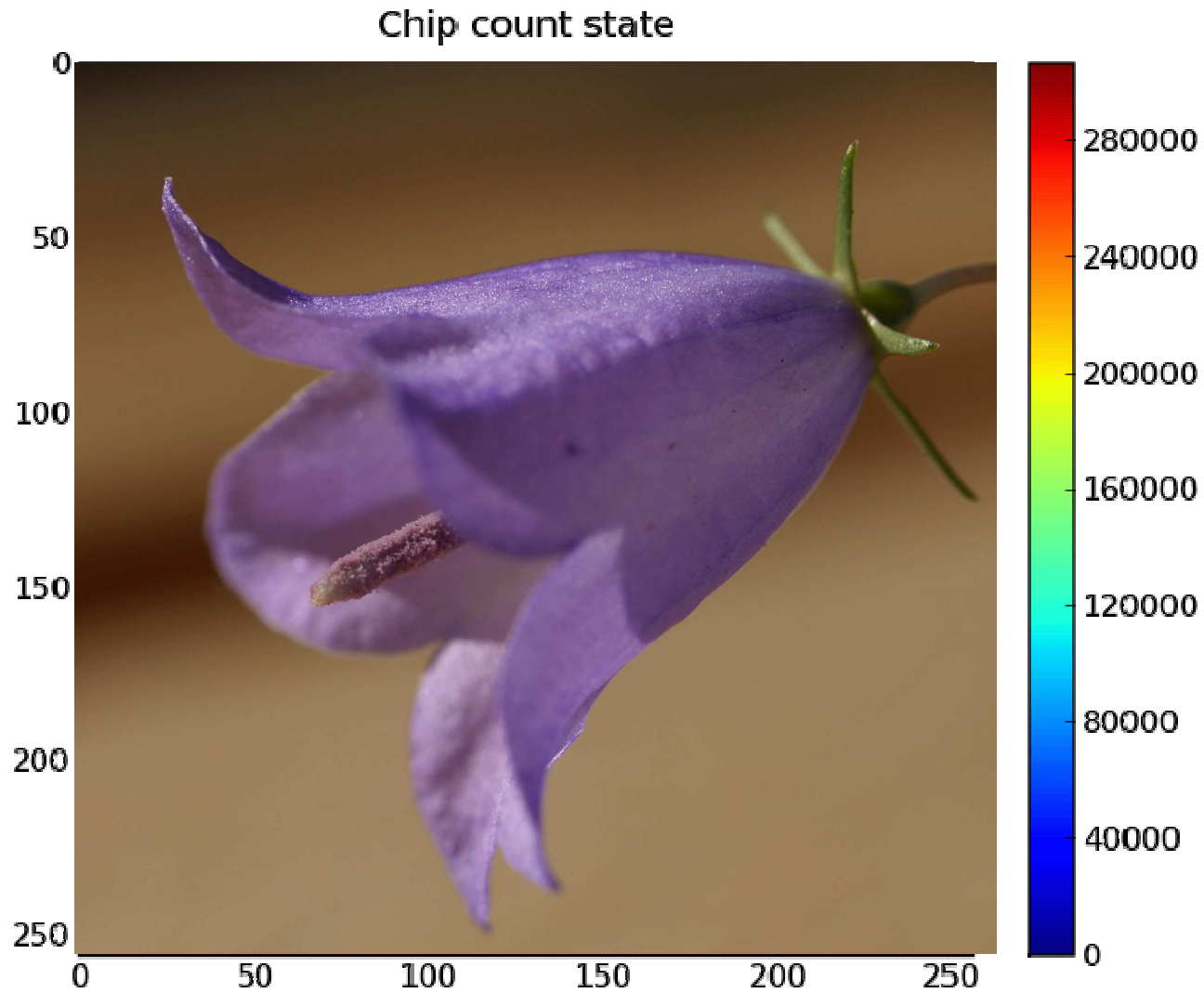
# Rate Capability

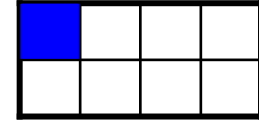


1) Measurement at low flux:  
use detector to calibrate source

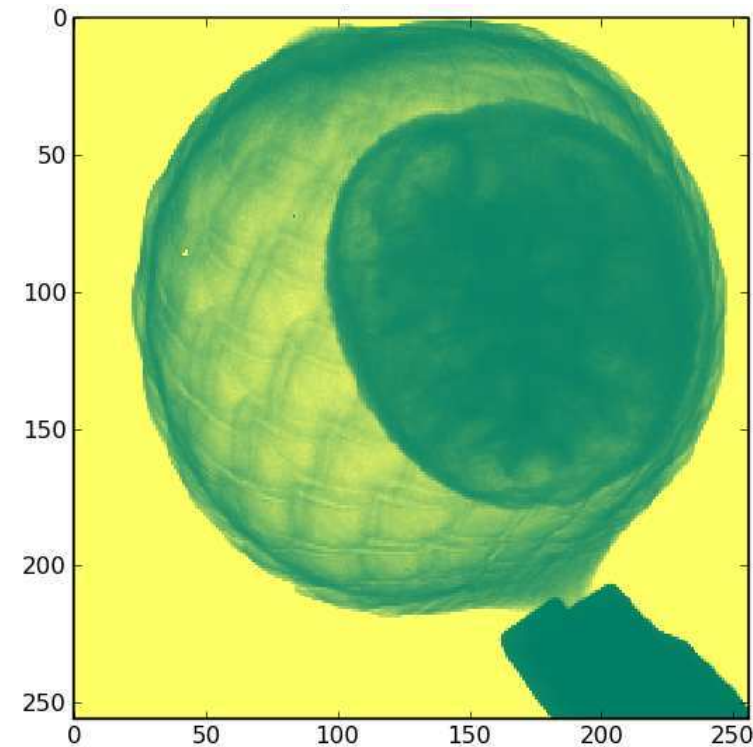
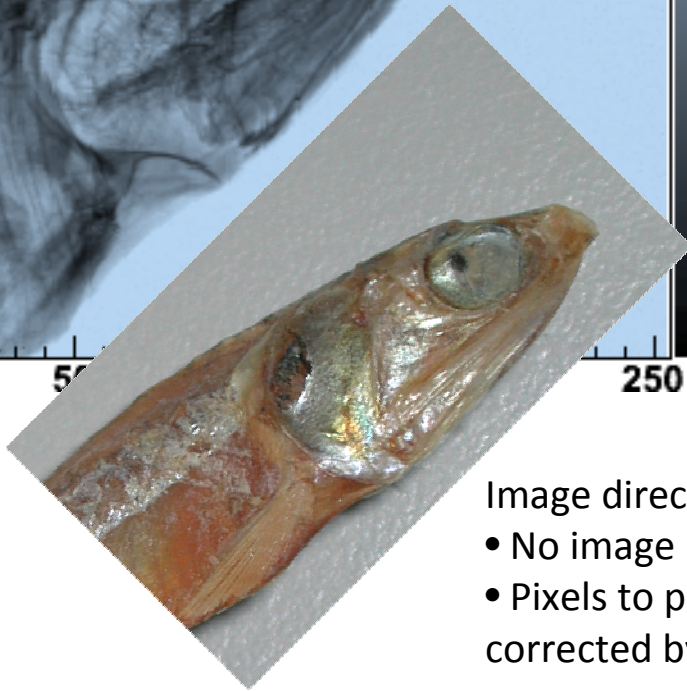
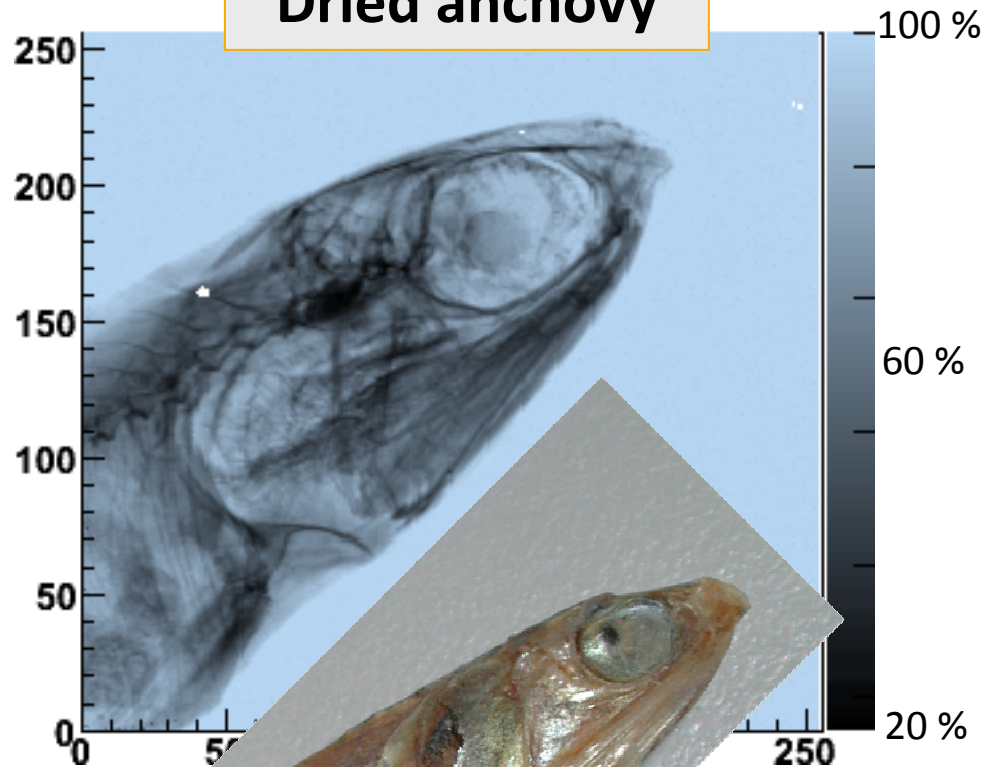
2) Measurement at high flux:  
use source to calibrate detector





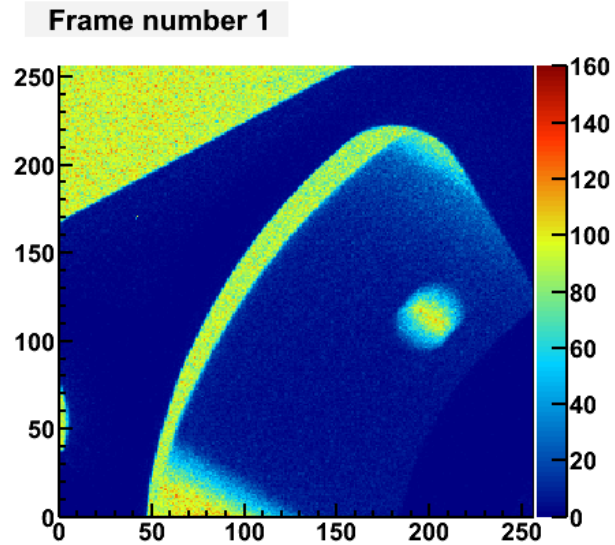


Dried anchovy



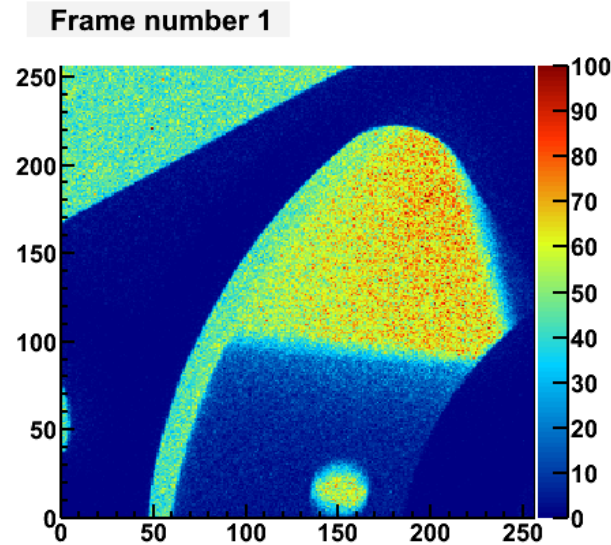
- Image directly from detector
- No image processing
  - Pixels to pixel differences corrected by trimming

$V = 50KV, I = 0.4mA$



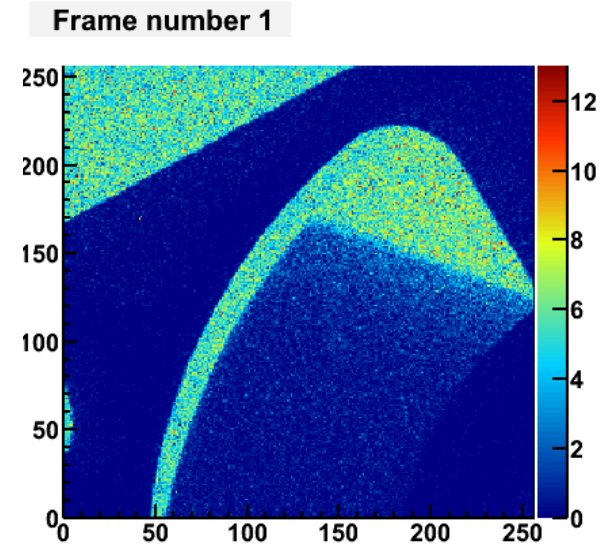
Chip in 12 bit Mode  
Exposure time  $125\mu s$   
Dead time  $3\mu s$   
Frame rate 7.8 kHz

$V = 50KV, I = 1 mA$



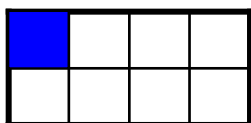
Chip in 8 bit Mode  
Exposure time  $85\mu s$   
Dead time  $3\mu s$   
Frame rate 11.4 kHz

$V = 50KV, I = 1 mA$

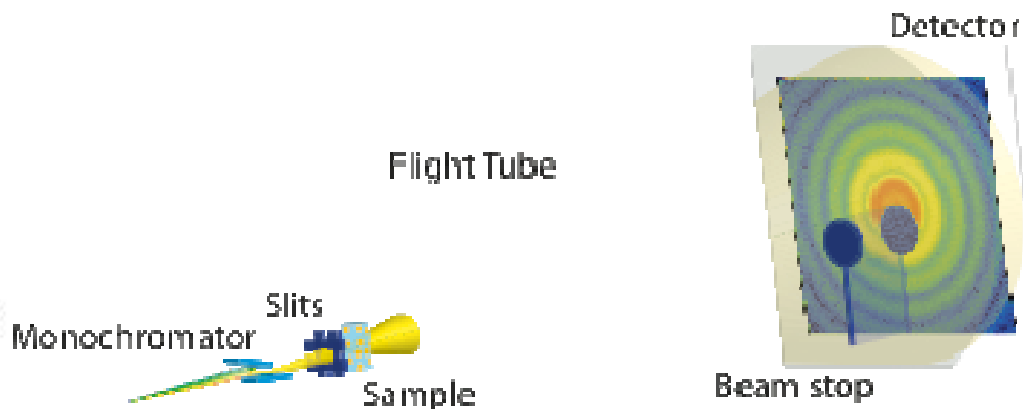
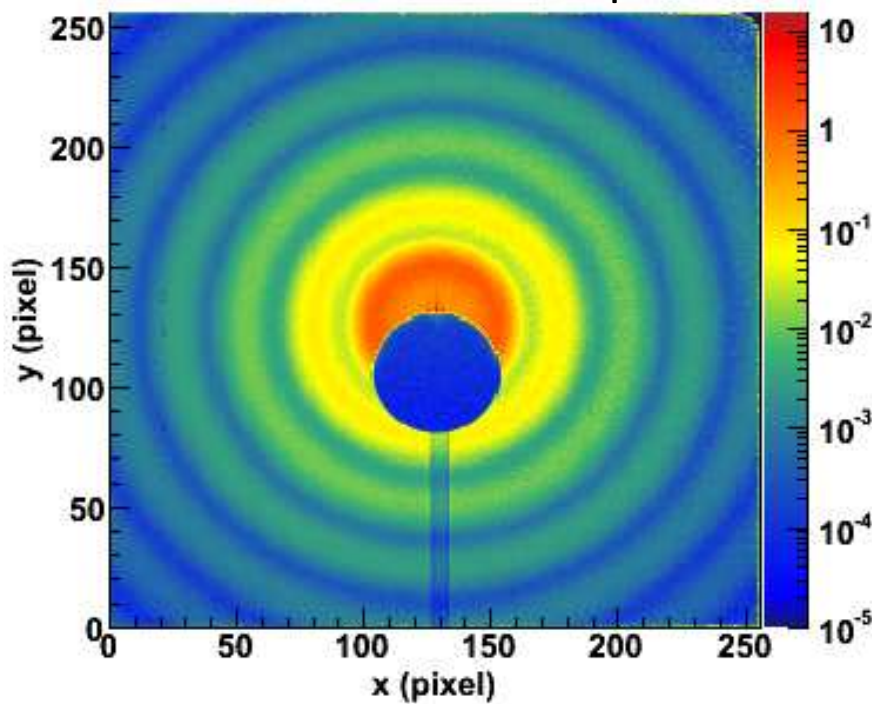


Chip in 4 bit Mode  
Exposure time  $45\mu s$   
Dead time  $3\mu s$   
Frame reate 20.8 kHz

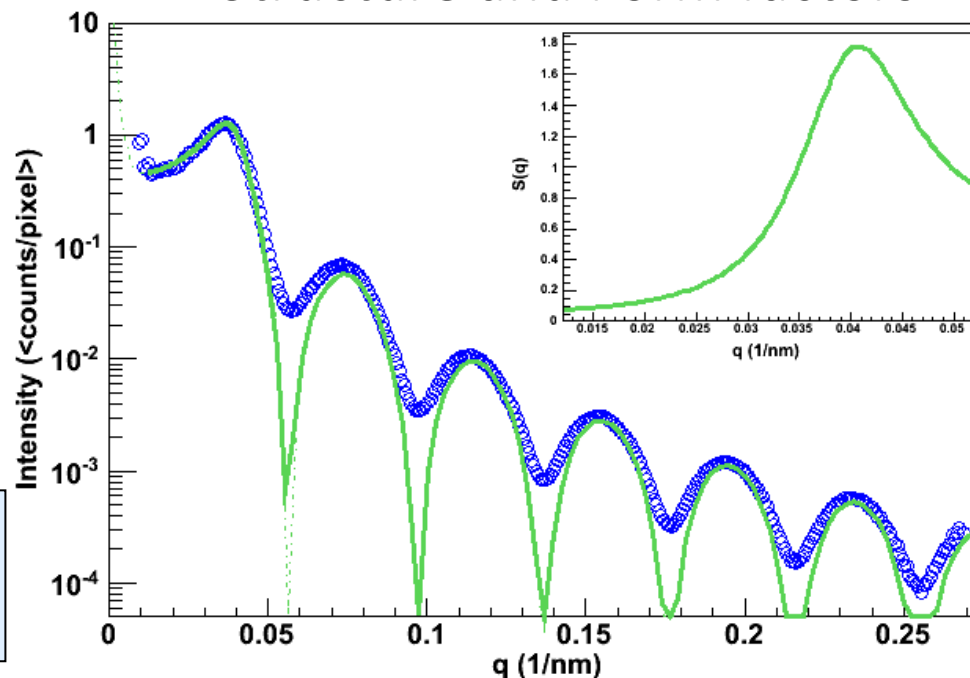




Average Diffraction Pattern  
Thousands of 50 us exposures

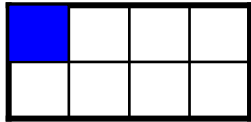


## Structure and Form factors



“Capturing dynamics with Eiger, a fast framing X-ray detector”

I. Johnson et al., J. Synchrotron Rad. (2012). 19, 1001



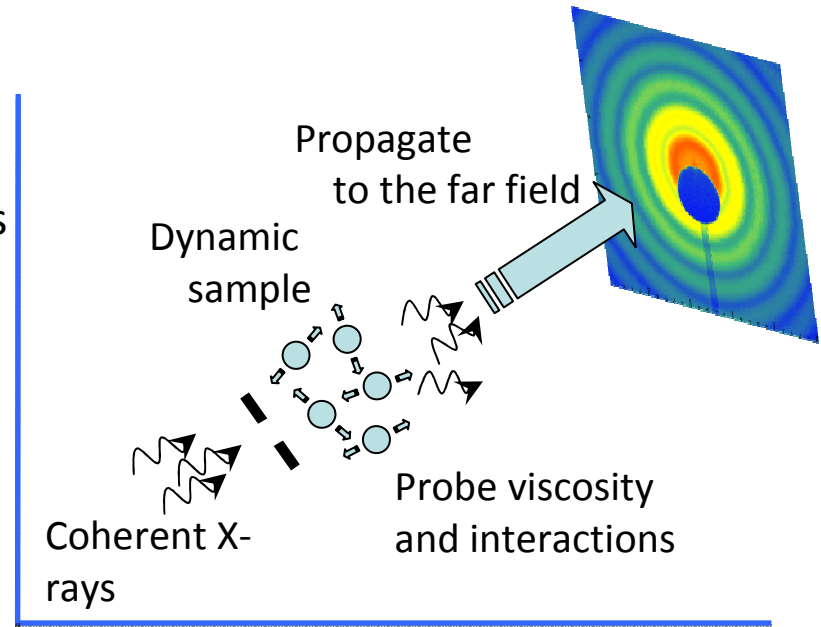
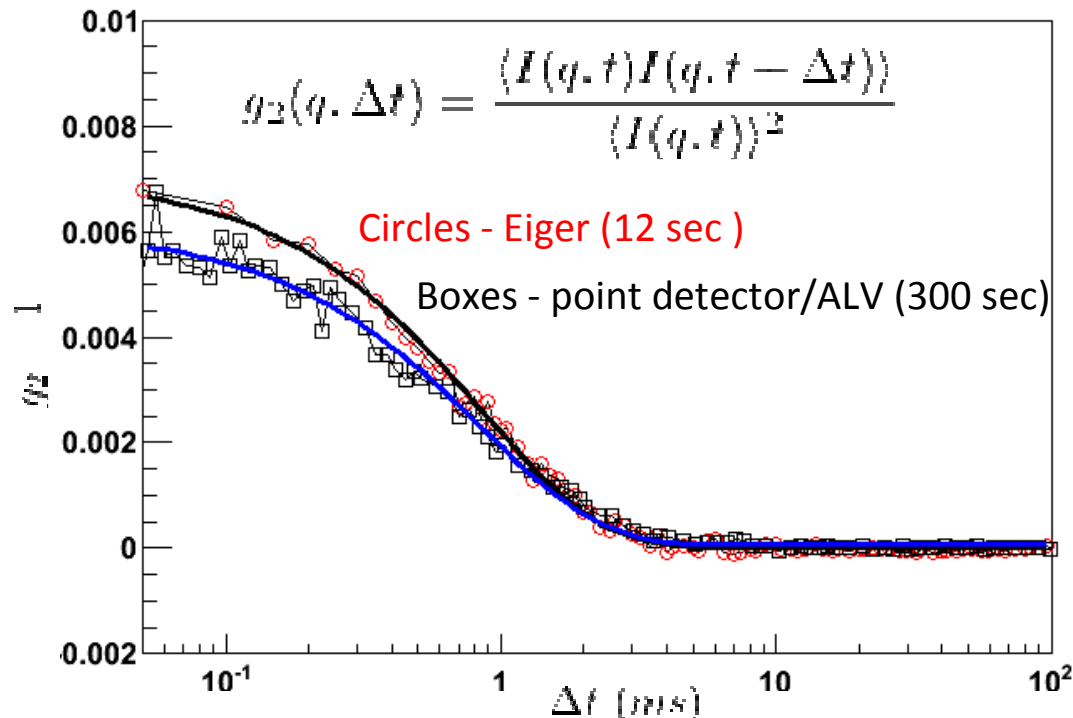
Eiger fast frame rate:

Second long exposure series @ 20 kHz

45 us exposure and 5 us dead time between frames

Intensity Fluctuations to probe the dynamics

Intensity-Intensity Auto Correlation Function



Siegert relation,

$$g_2(q, \Delta t) = 1 + \beta |g_1(q, \Delta t)|^2$$

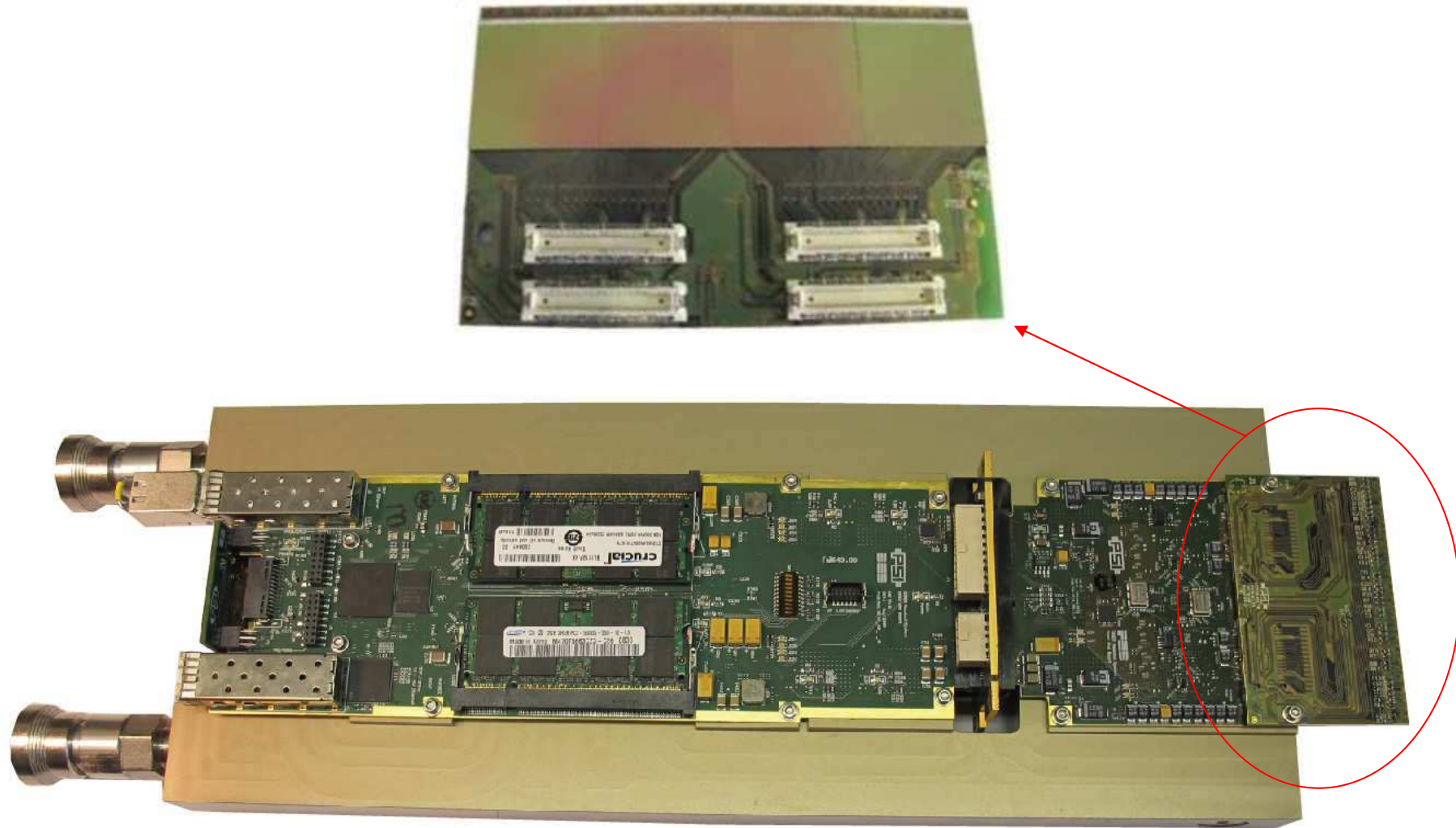
Normalized field correlation function

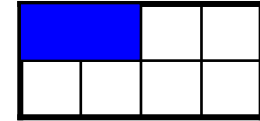
$$g_1(q, \Delta t) = e^{-Dq^2 \Delta t}$$

Brownian motion,

$$D = D_0 \frac{kT}{6\pi \eta r}$$

# Half Module System



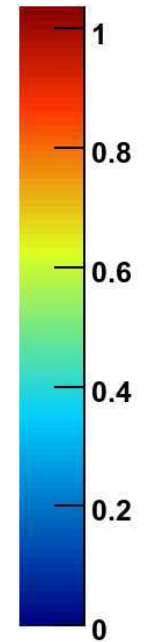
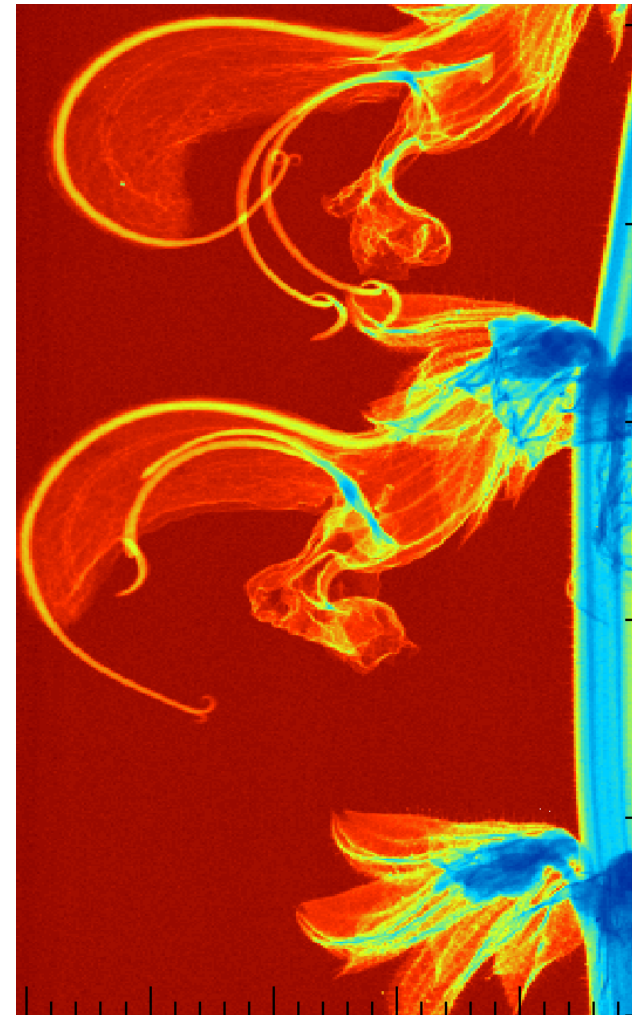


## Wild flower

No stitching, no trimming, with background correction



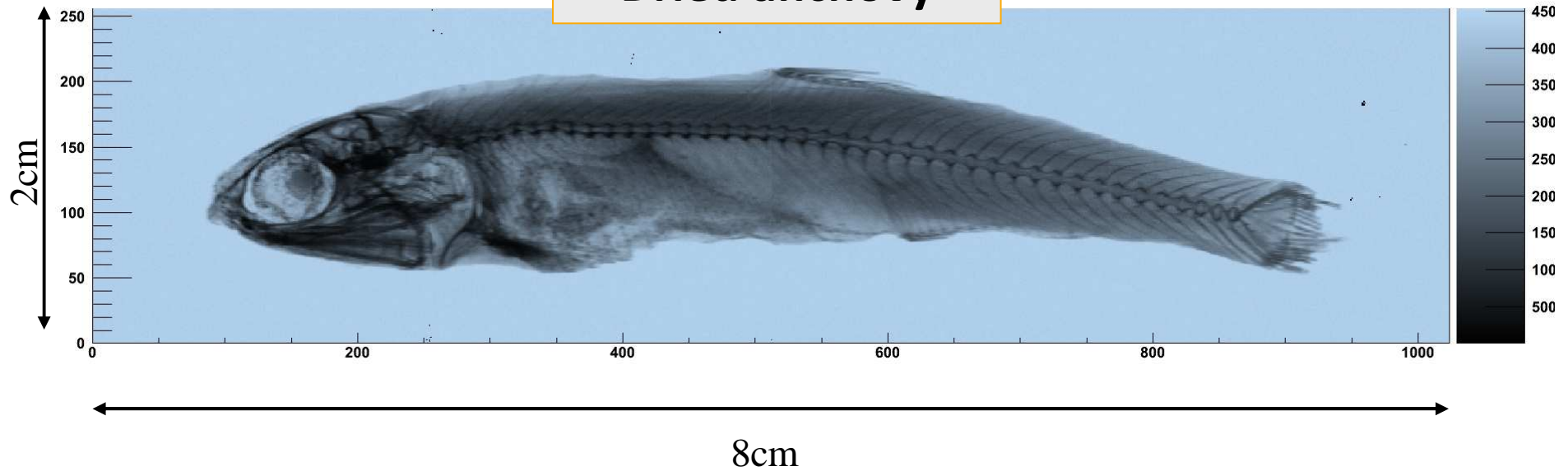
4cm





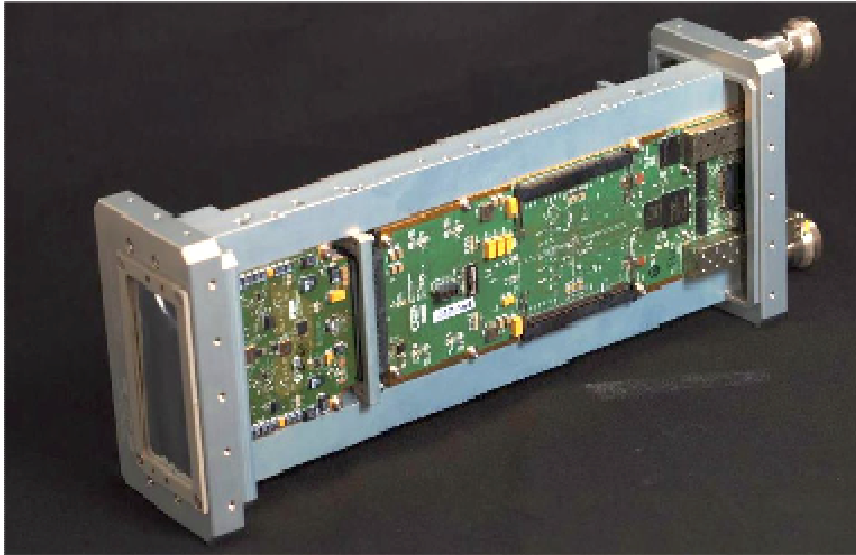


**Dried anchovy**



**No stitching, no trimming, with background correction**

# The Eiger Module: Eiger 500k



- 4x2 chips/module
- Electronics is separated for top and bottom halves
- Data buffering
  - 8 GB of on board memory per module
  - 32 k frames for 4 counter bits

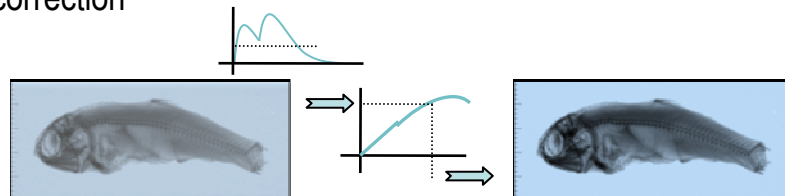
- Firmware data processing

- Image summation
  - **extends the dynamic range from 4096 (12 bits) to  $4 \times 10^9$  (32 bits)**

Image summation



Rate correction



- Rate correction

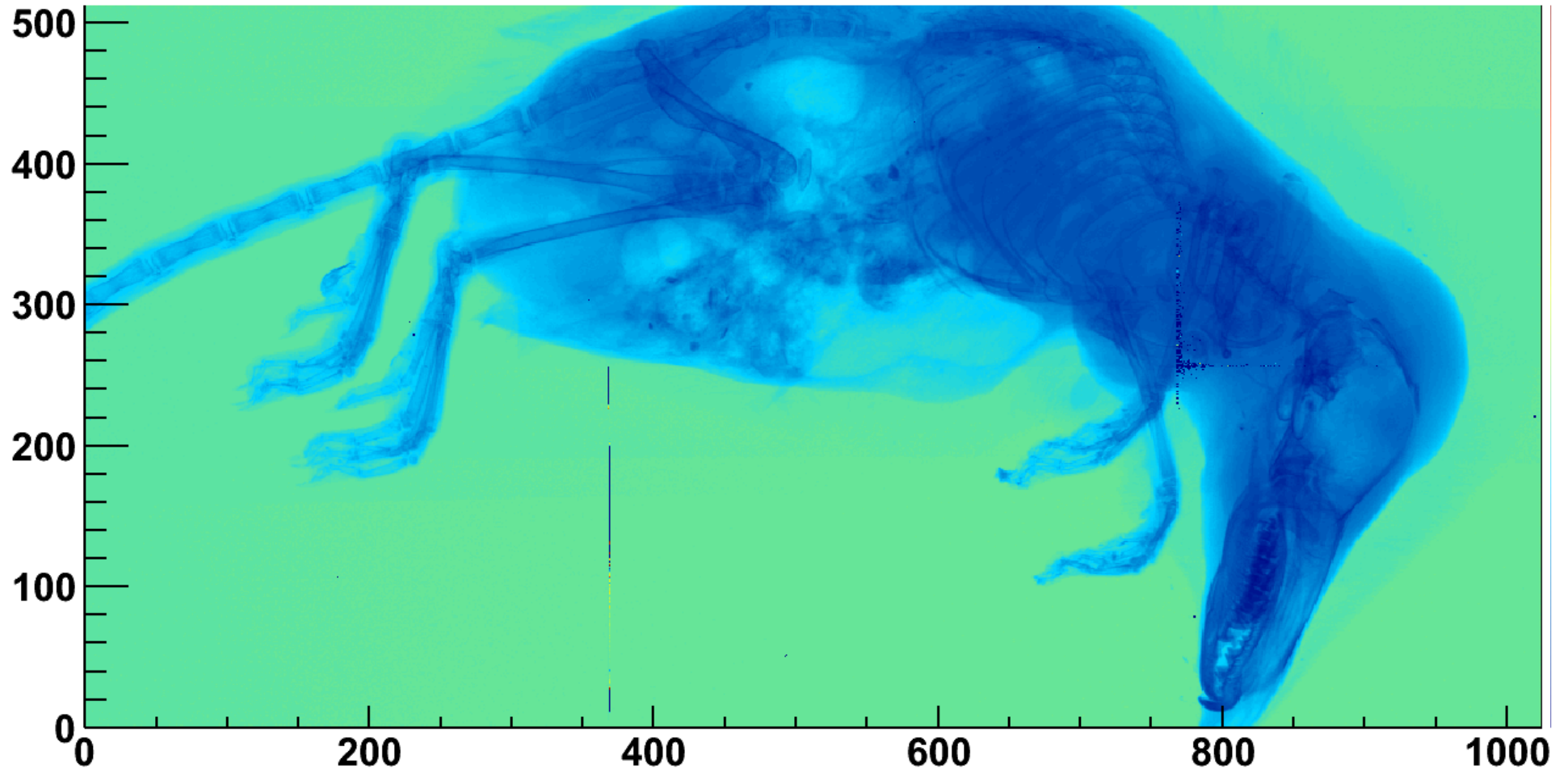
- Readout architecture

- High speed data transfer: data is sent over 1 GbE or 10 GbE connections, one per half module
- Online compression: HDF5 libraries



**First working module after recovery from bump-bonding disaster.  
No stitching, no trimming, no setup optimization, with background correction. New module.**

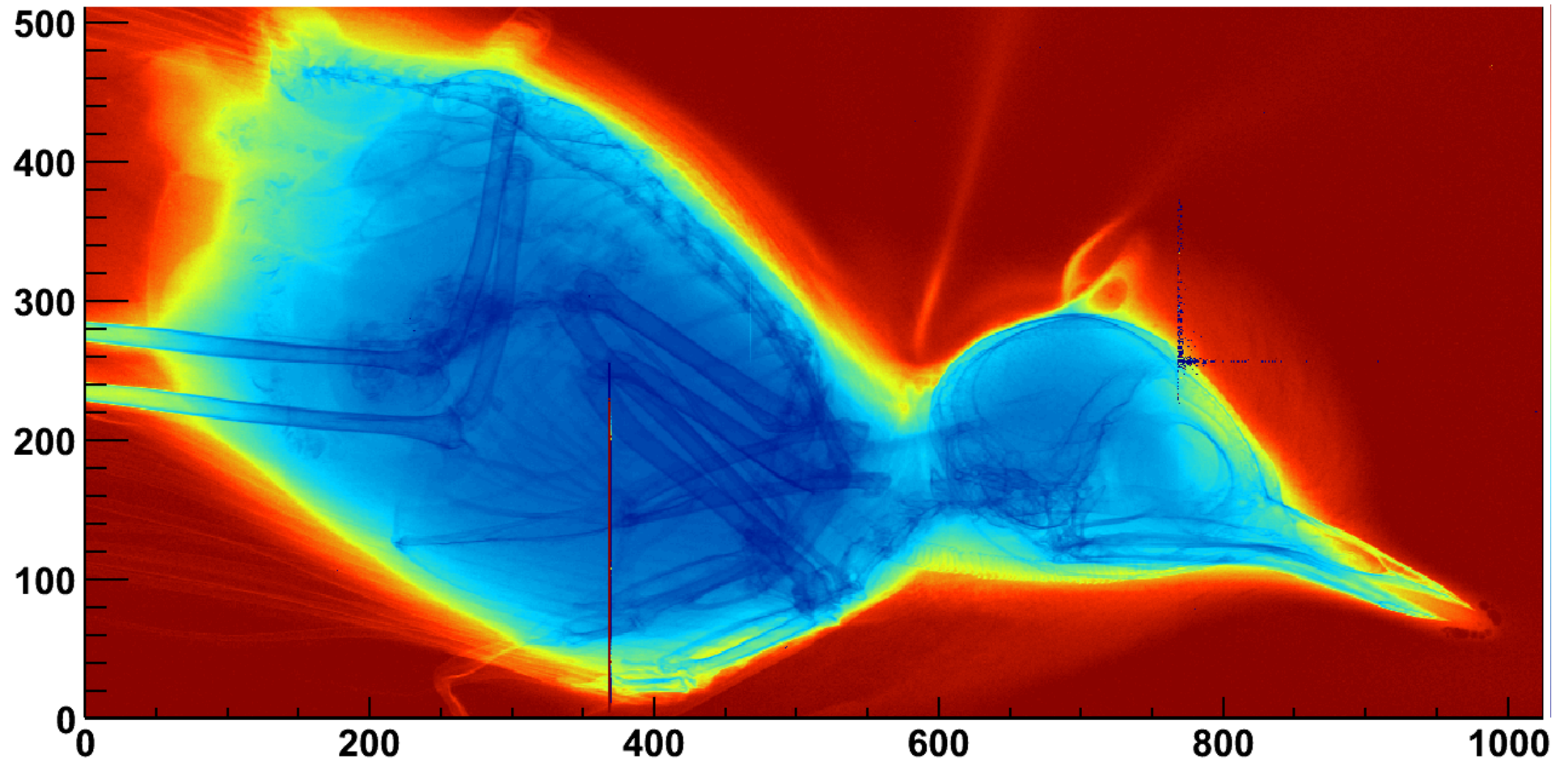
**Shrew**





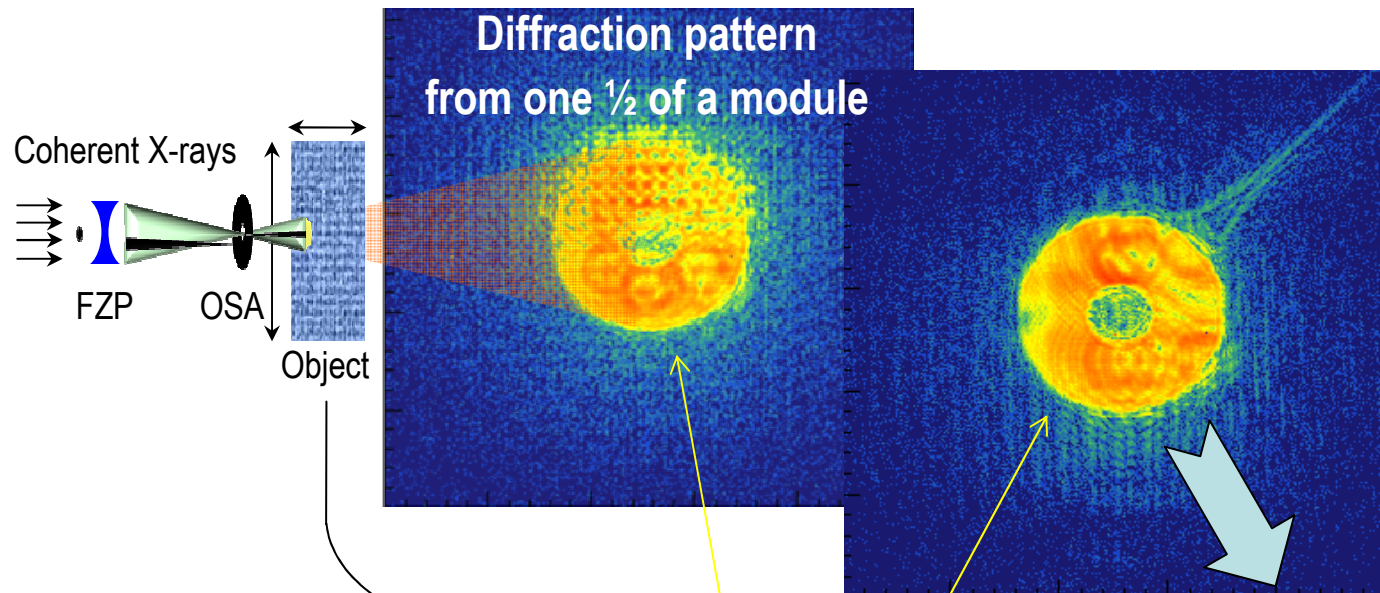
**First working module after recovery from bump-bonding disaster.  
No stitching, no trimming, no setup optimization, with background correction. New module.**

**Robin**

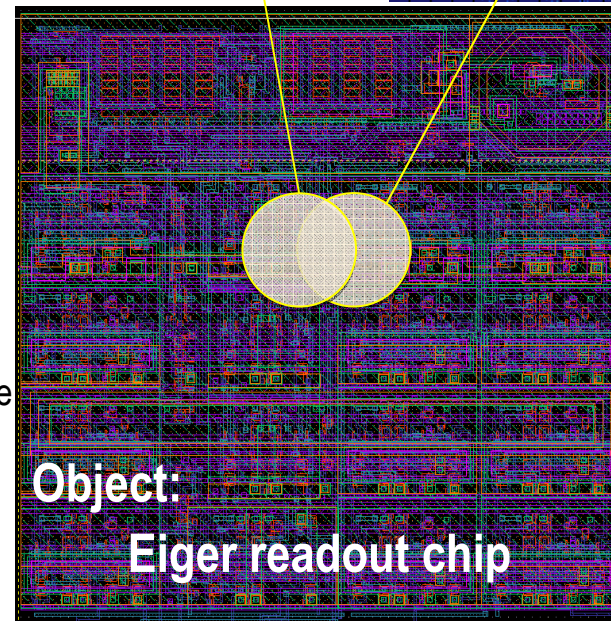




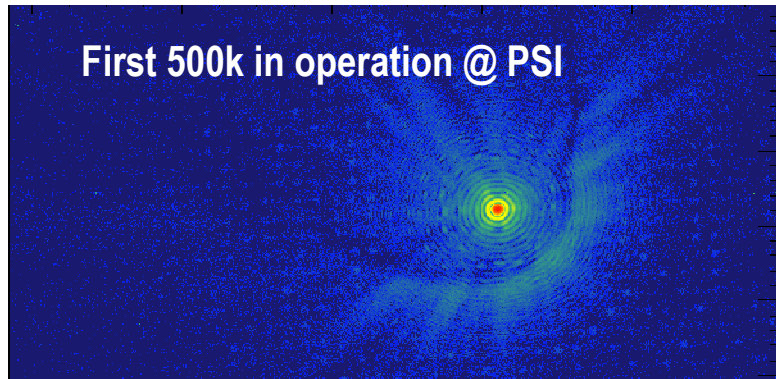
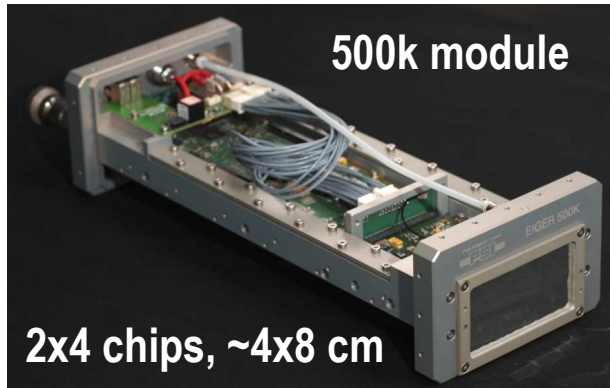
# An Eiger self portrait (Ptychography)



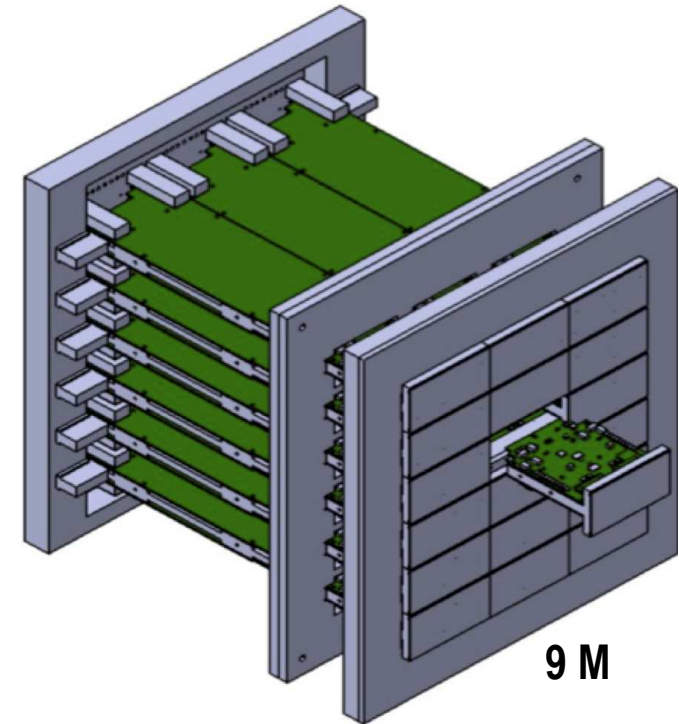
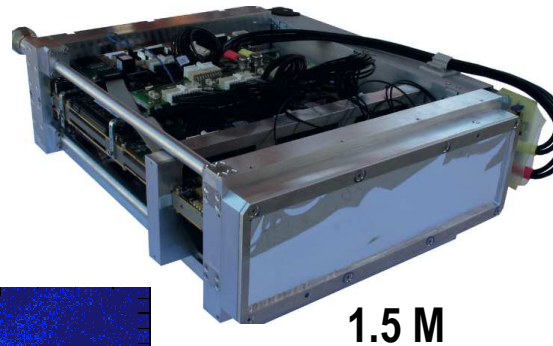
- The object is raster scanned by an out of focus beam
- Diffraction patterns at overlapping positions on the object are recorded
- The information in the overlap is used to recover the dp phase
- Both the attenuation and phase shift in the object can be reconstructed



← 80 μm →

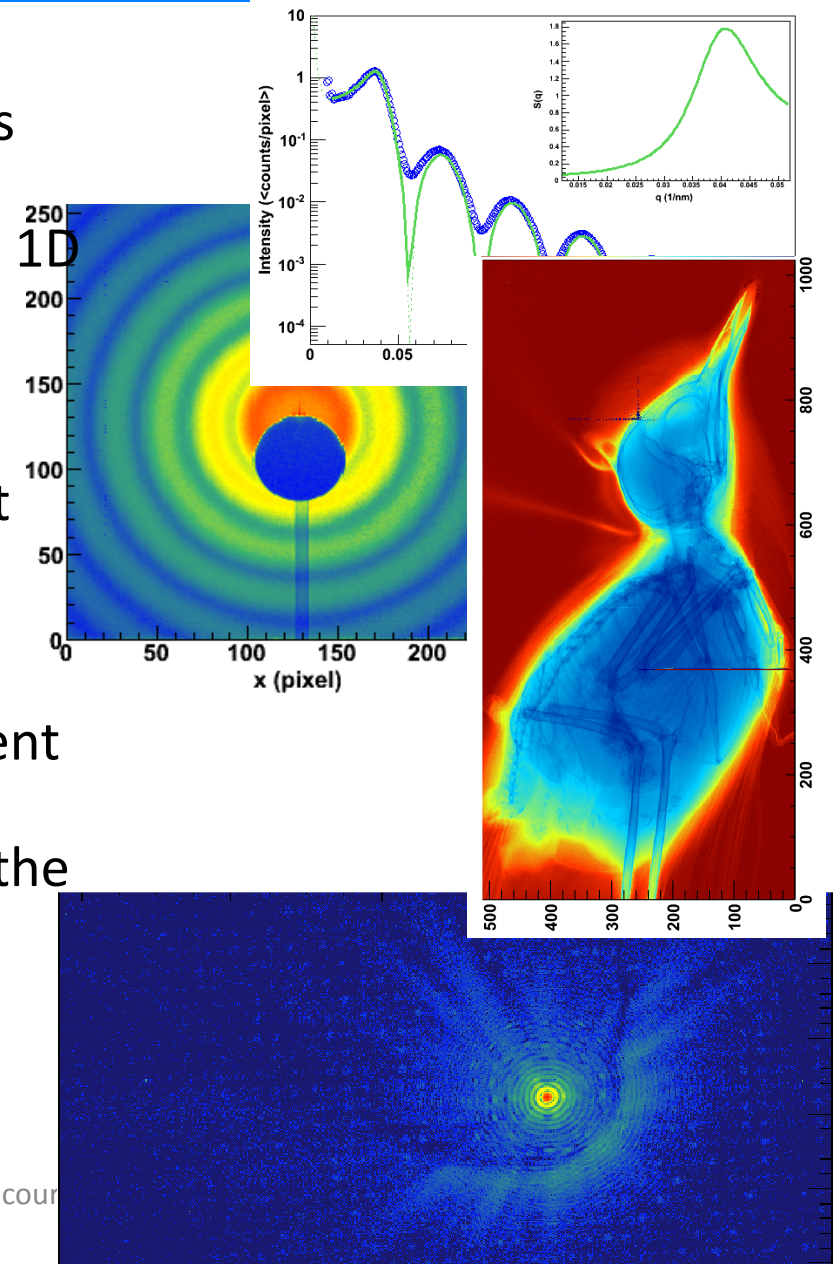


## Multi-module detectors



	Pixel array	Data rate <sup>1</sup> @ 12 kHz	Data rate <sup>2</sup> @ 1kHz	Data rate <sup>2</sup> @ 100 Hz	Data rate <sup>3</sup> @ 10 Hz
Module	512 x 1024	50.3 Gb/s	8.39 Gb/s	839 Mb/s	168 Mb/s
1.5M	512 x 3072	150 Gb/s	25.2 Gb/s	2.52 Gb/s	503 Mb/s
9M	3072 x 3072	<b>906 Gb/s</b>	151 Gb/s	15.1 Gb/s	3.02 Gb/s

- PSI is active in chip design targeting many different applications but the main focus is detectors for X-ray applications
- The SLS Detector group developed several 1D and 2D hybrid detectors for synchrotron radiation applications
- The latest detector family is called EIGER.
- Results from extensive testing show that it fulfills the challenging requests from the beamlines in terms of noise and energy resolution
- The frame rate is up to  $\sim 24$  kHz independent on the detector size.
- The first module is already operational at the cSAXS beamline at PSI
- We are working towards larger detector systems (1.5M, 9M)





# ACKNOWLEDGMENTS

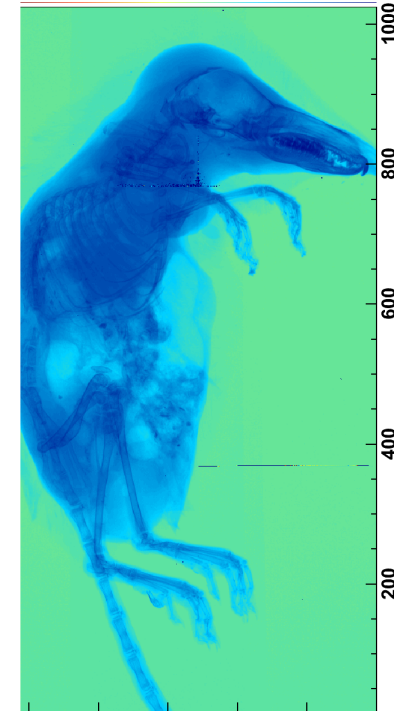
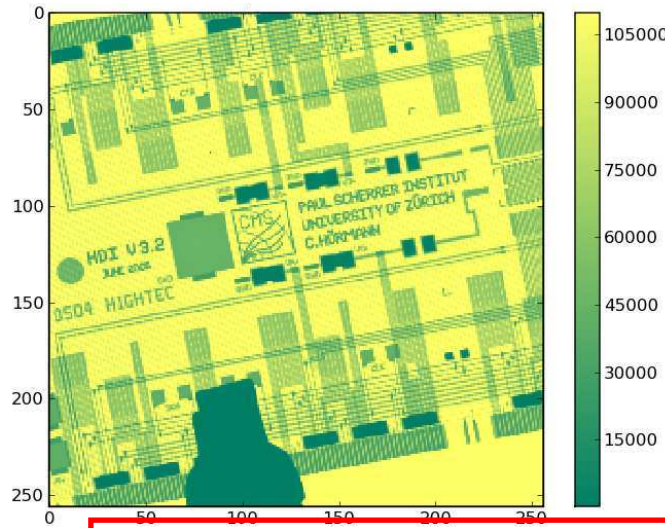
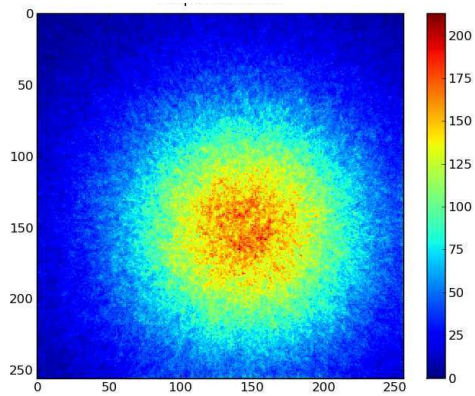
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Not in the picture:  
**Julia Jungmann**,  
**Davide Mezza**





THANKS!

