- VMM -

a self-triggered front-end ASIC for ATLAS upgrades

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Brookhaven National Laboratory

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Outline

- Microelectronics (ASICs) at BNL
- VMM1
  - motivation
  - architecture
  - circuits
  - results
- VMM2
  - architecture
  - circuits

Microelectronics at BNL

15 years of **ASIC** design for a broad range of applications

STAR	Bipolar Junction Transistor front-end for silicon vertex tracker
PHENIX	Front-end and flash ADC for time expansion chamber
ATLAS	Cathode strip chamber, LAr calorimeter upgrade (SiGe), muon upgrade
LEGS	Gas Electron Multiplier TPC for laser electron gamma source experiments
µBooNE	Front-end cryogenic ASIC for LAr TPC
LBNE	Front-end and mixed signal cryogenic ASICs for LAr TPC
NNS	ASICs for high-resolution Gamma spectrometers
NSLS	Si detectors EXAFS and powder diffraction, High-resolution X-ray spectroscopy (MAIA), ASIC for high spatial resolution spectroscopy and photon counting
NASA	Silicon Drift Detector based X-ray Spectrometer for elemental mapping
SLAC	High-voltage matrix switching ASIC, front-end ASIC
SNS	^{3}He detector for neutron imaging
NRL	Compton imager
OXI	DRIFT Dark Matter
LBL	Ge Gamma spectrometers
WUSL	Hard X-ray missions
LLNL	Si-sci Gamma spectrometer
NATL SEC.	3D position sensitive detector (U.Mich, DoD, DHS), co-planar grid detector (LANL, DoD)
MEDICAL	Micro-PET for RatCAP, PET-MRI and wrist scanner, CZT-based PET, portable gamma camera, prostate cancer imager (NNS ProxyScan), eye-plaque dosimeter (CMRP)
CRADAs	eV-Products (CZT), Digirad (Si-sci Medical), Photon Imaging (Si), Symbol Tech. (Wireless), RMD (Si-sci)

over 20 designs and 40 revisions

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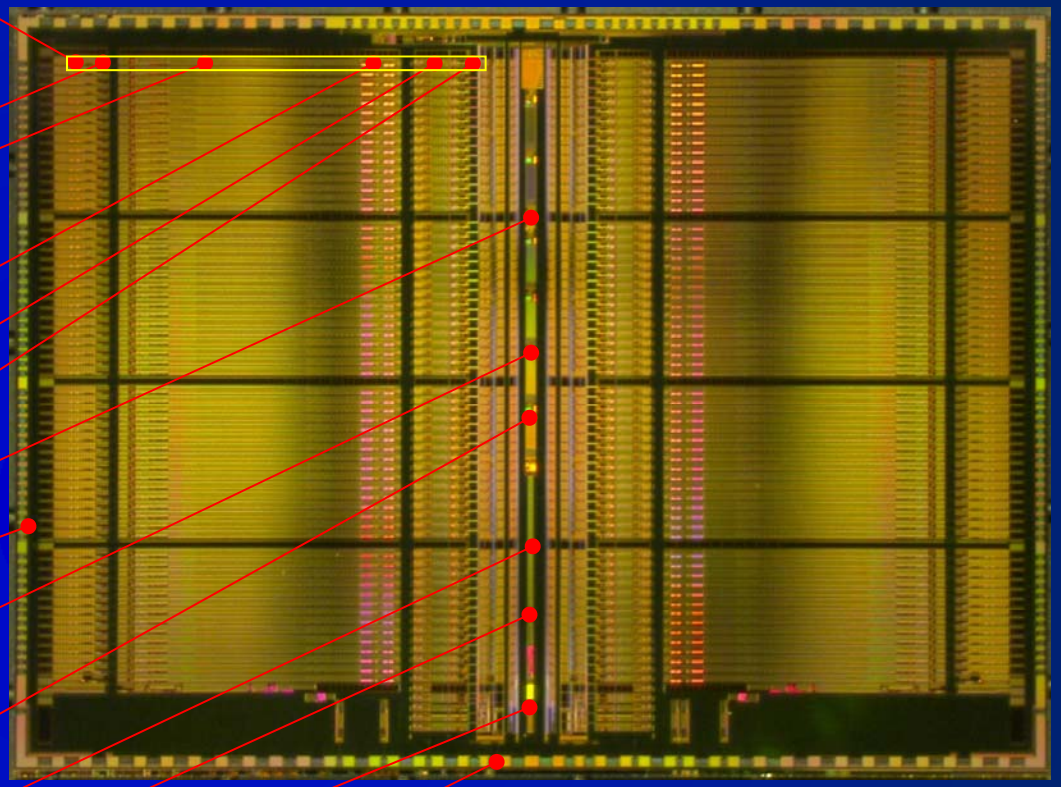
Circuits

- Low-noise, low-power charge amplifiers
  - gas, liquid, solid state detectors
  - capacitances from 10 fF to 10 nF
- Switched and continuous adaptive reset
- High-order filters, stabilizers, drivers
  - peak time / gain adjustment
- Single- and multi-level discriminators
- Peak and time detectors, derandomizers
- Analog memories and multiplexers
- Counters and digital memories
- Configuration registers
- ESD protections
- Calibration pulse generators
- Analog-to-digital converters
- Digital-to-analog converters
- Precision band-gap references
- Temperature sensors
- Readout control logic
- Low-voltage differential signaling
- Current-mode analog and digital interface

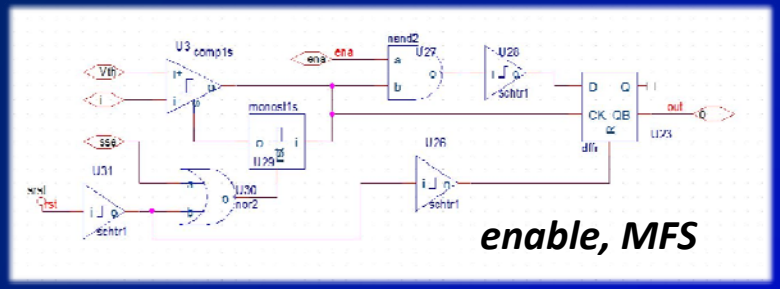


ASIC for 3D Position Sensitive Detectors

- 128 channels
- 2 mW/channel
- 13 x 10 mm²
- 300,000 transistors
- CMOS 250 nm
- 2009

complexity increases by the year

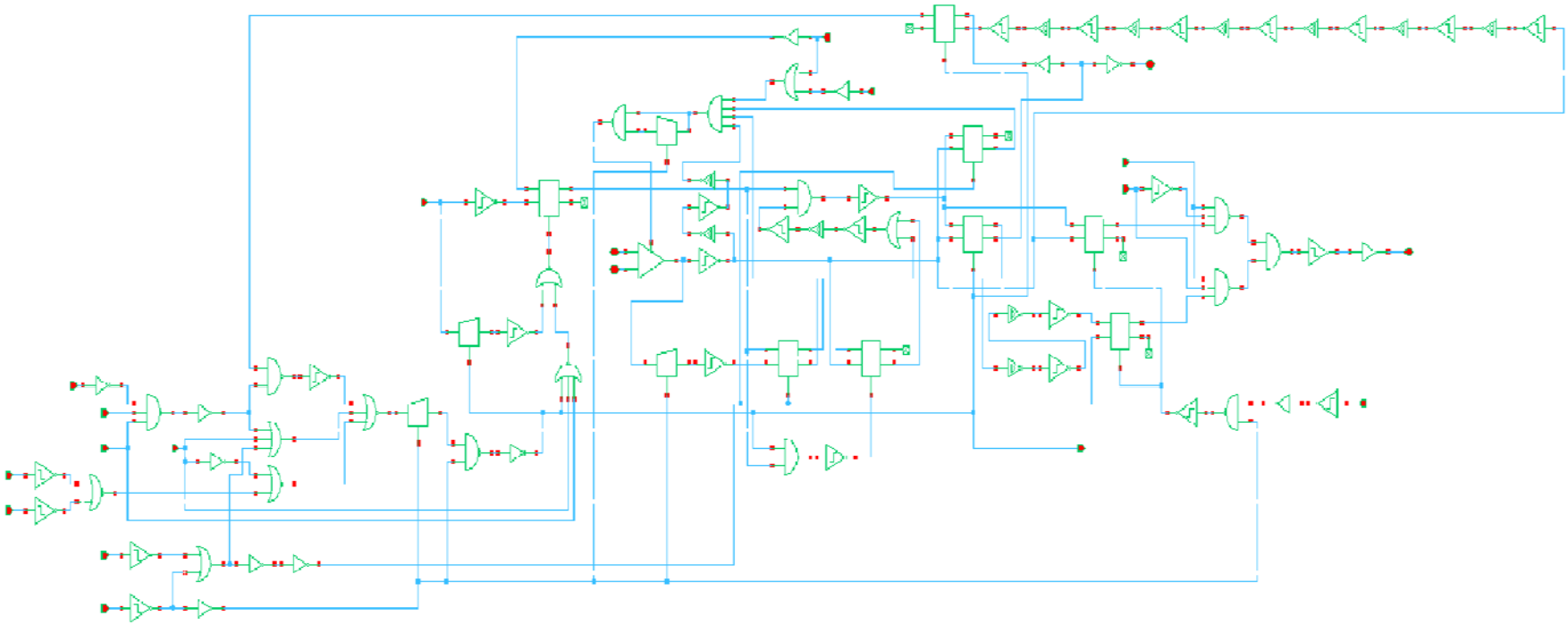
Discriminator Circuit



enable, MFS

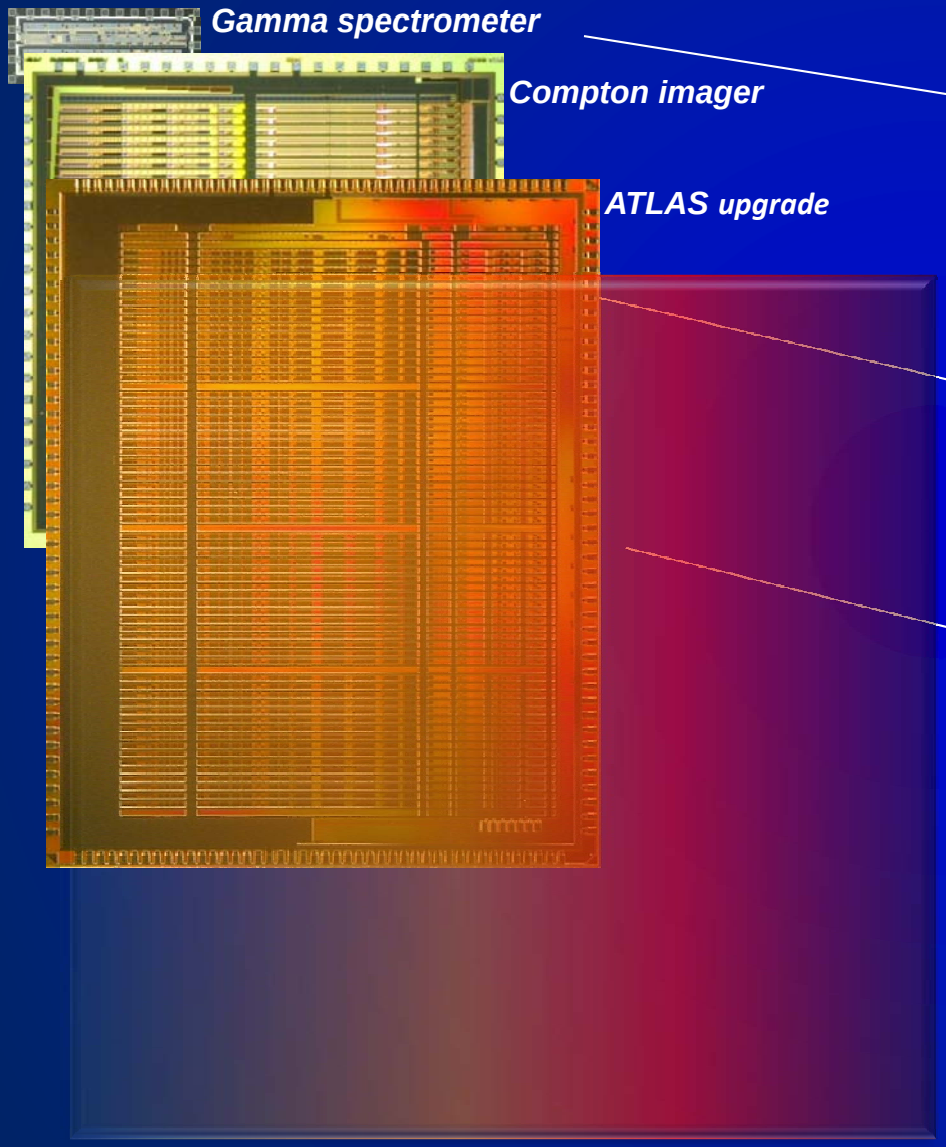
year 2006

year 2012



enable, rmode, reset, SHD, ToT, TtP, ADCs

Progress in ASICs



~ year 2001
tech. CMOS 500nm, 3.3V
~ 10k transistors, ~ 2mm²
preamplifier/filter

1-2 designers

~ 2006
250nm, 2.5V
~ 100k transistors, ~ 25mm²
+ discrim/peak-det/mux

3-4 designers

~ 2011
130nm, 1.2V
~ 1M transistors, ~ 50mm²
+ time-det/tots/mux/ART

5-6 designers

~ 2015
< 90nm, <1V
> 10M transistors, > 100mm²
+ ADCs/DSP/SOC/EOC
(DSP=Digital Signal Processing)
(SOC=System on Chip)
(EOC=Experiment on Chip)

7-8 designers

~ 1-2 new designs /year, ~ 3-4 revisions /year

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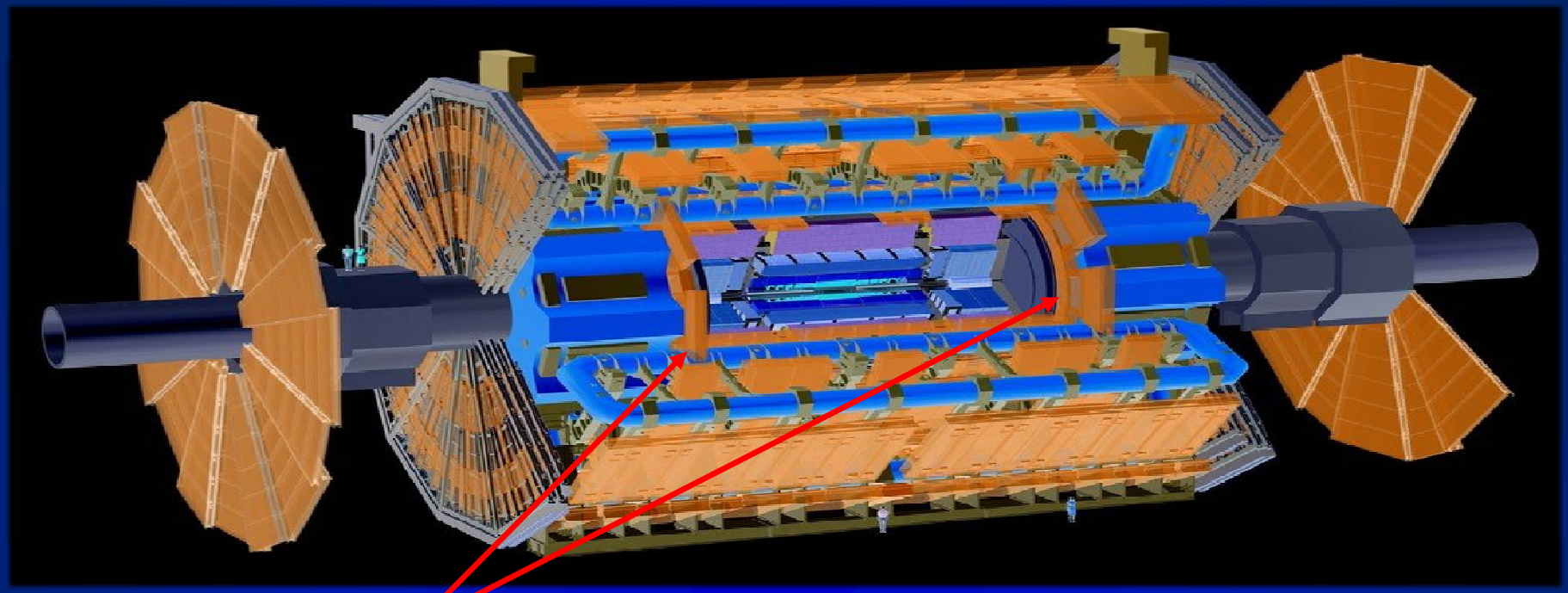
ASIC for ATLAS Muon Spectrometer Upgrade

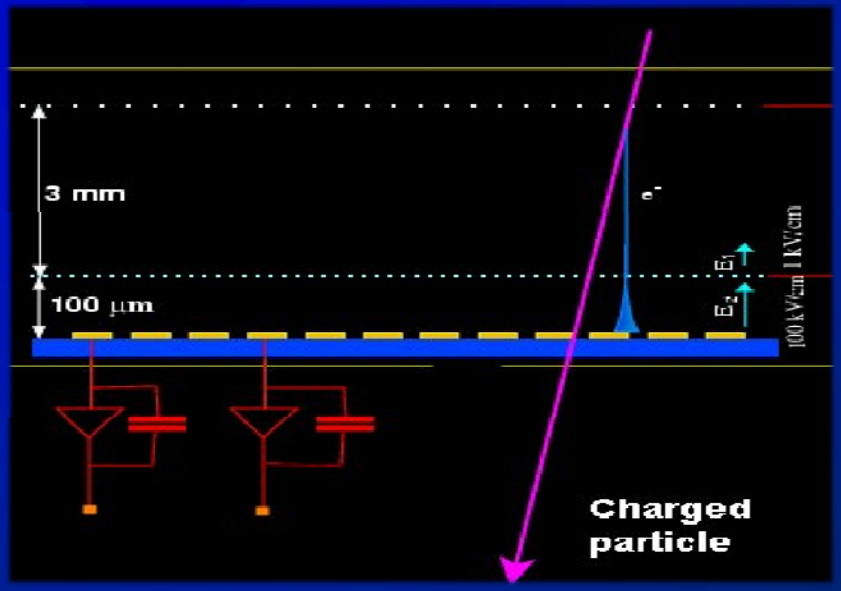


New Small Wheels

- **TGC** (Thin Gap Chamber)
- **MICROMEGAS**
  (MICROMEsh GAseous Structure)
- **> 2M channels**

Front-end ASIC

- 10-200 pF
- 2 pC @ < 1 fC rms
- 100 ns @ < 1ns rms



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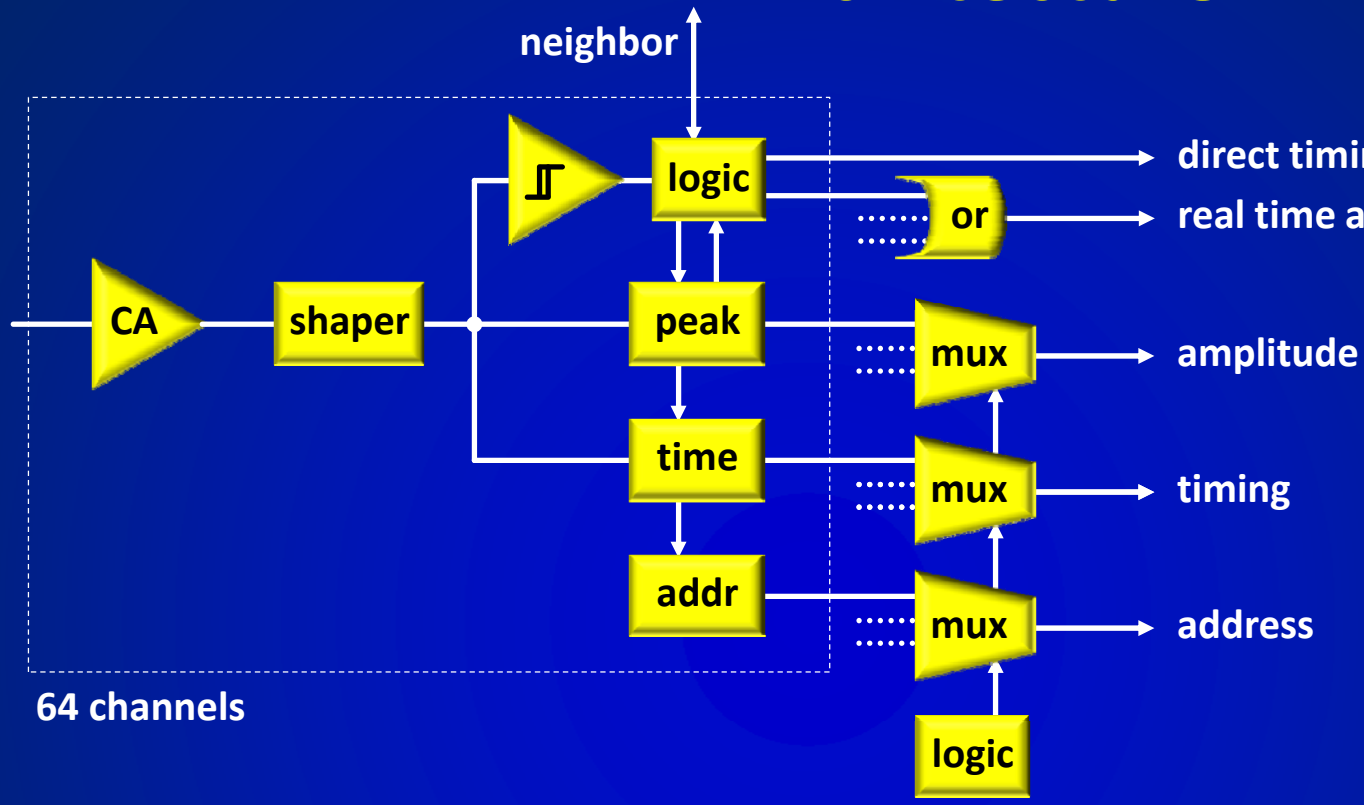
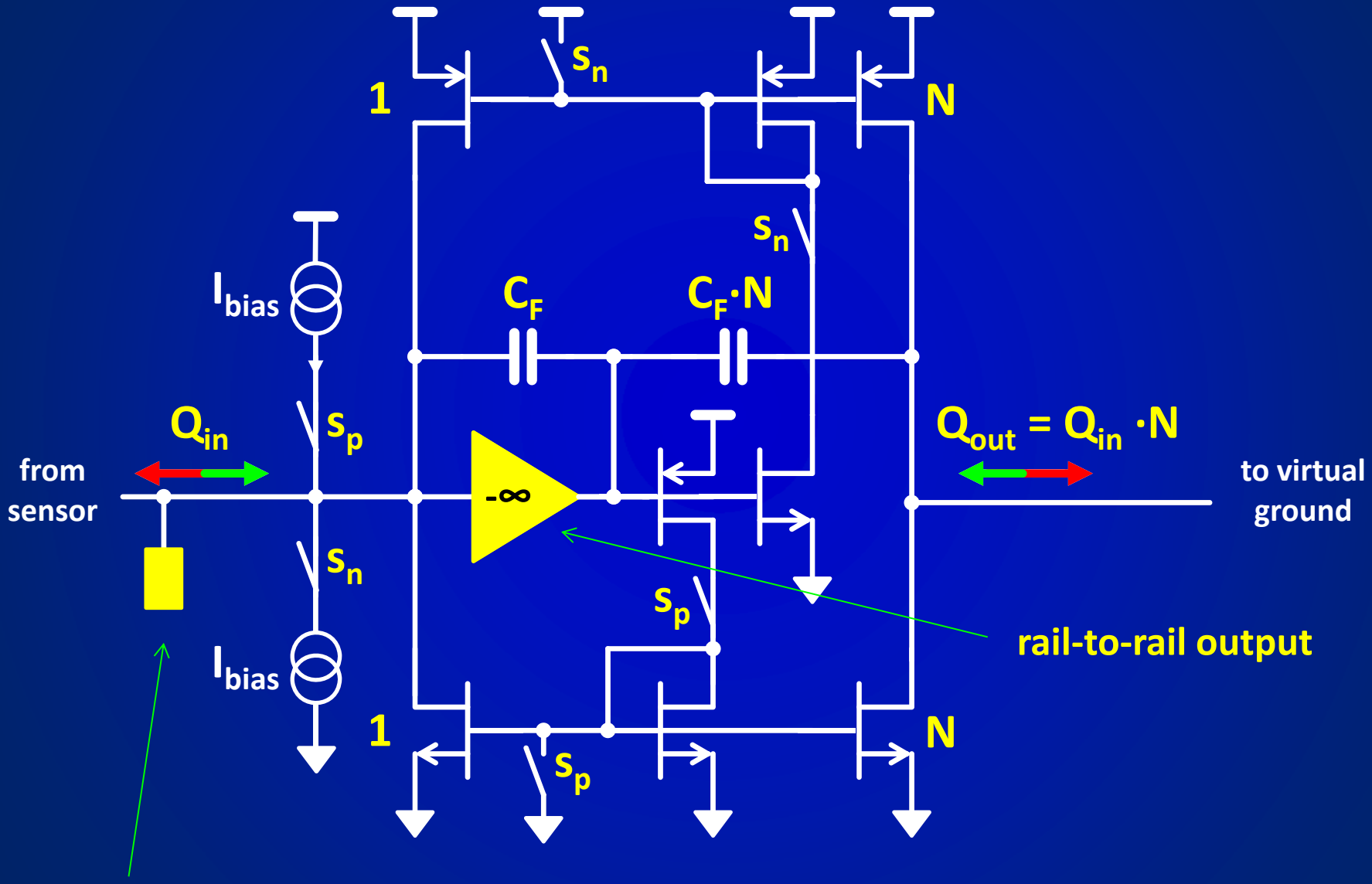
VMM1 - Architecture



- dual polarity, adj. gain (0.5-9 mV/fC), adj. peaktime (25-200 ns), DDF shaper
- discriminator with sub-hysteresis and neighboring (channel and chip)
- address of first event in real time at dedicated output (ART)
- direct timing outputs: time-over-threshold or time-to-peak
- peak detector, time detector
- multiplexing with sparse readout and smart token passing (channel and chip)
- threshold & pulse generator, analog monitor, mask, temperature sensor, 600mV BGR, 600mV LVDS
- power 4.5 mW/ch, size 6 x 8.4 mm², process IBM CMOS 130nm 1.2V, test structures

Dual-Polarity Charge Amplifier



ESD protection – *beware of leakage*

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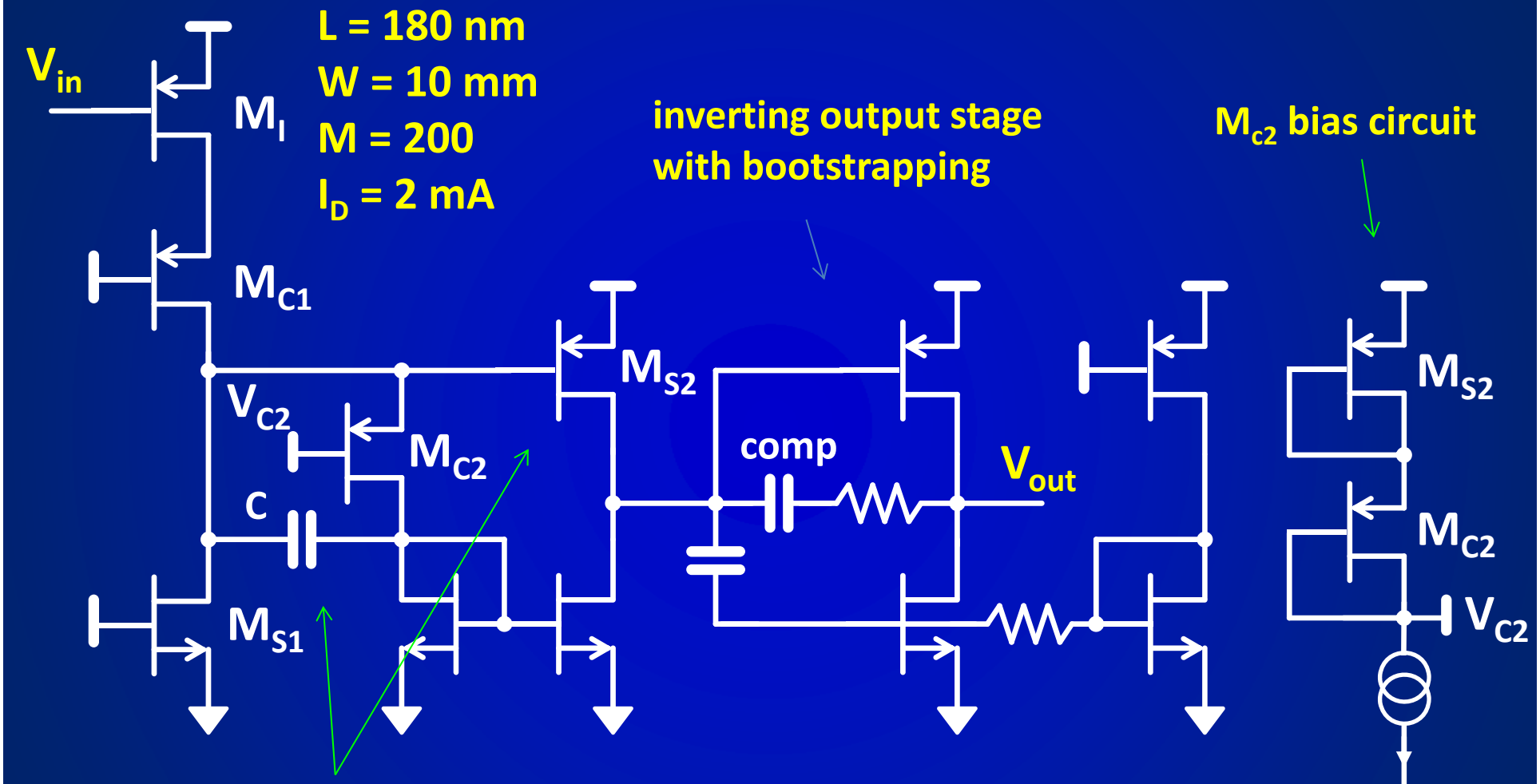
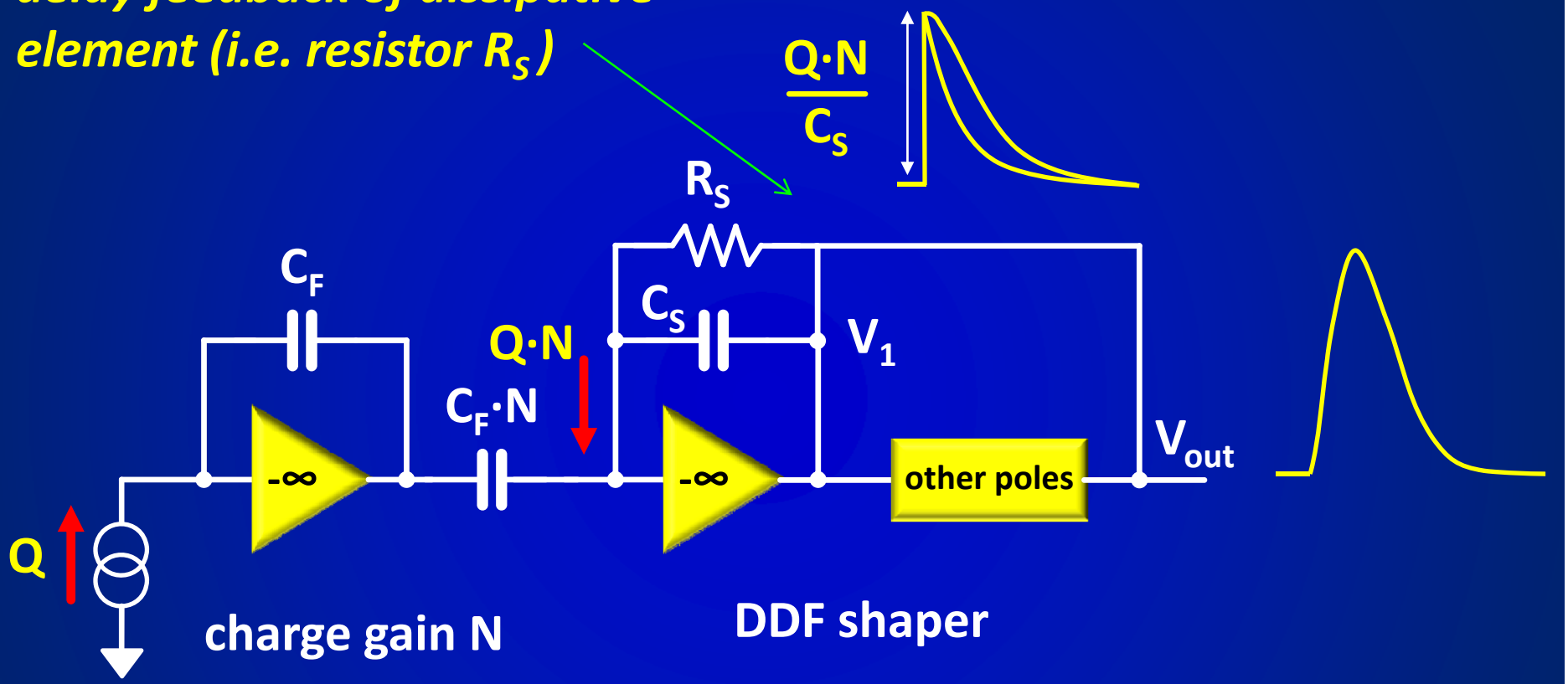
Front-End Voltage Amplifier



Delayed Dissipative Feedback (DDF)

delay feedback of dissipative element (i.e. resistor R_S)



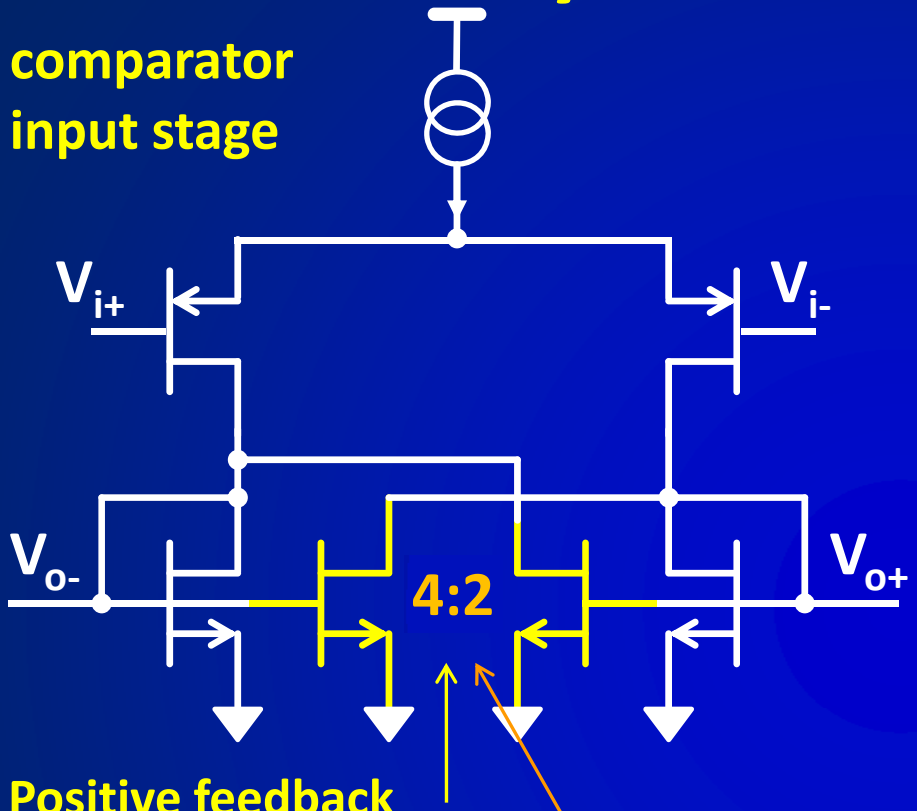
higher analog dynamic range

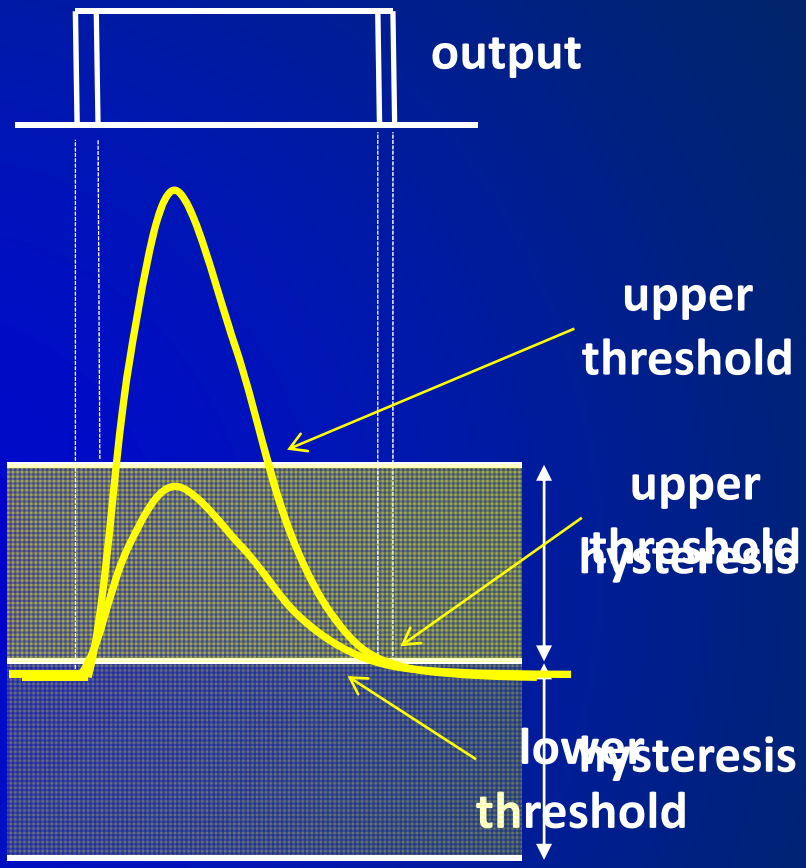
$$DR_a = \frac{Q_{max}}{\sqrt{ENC_{CA}^2 + ENC_S^2}}$$

Applies also to the other stages of the shaper

see G. De Geronimo and S. Li, TNS 58, Oct. 2011

Sub-Hysteresis Discrimination





Positive feedback

- high speed at low V_{i+}-V_{i-}
- hysteresis set NMOS ratio
  sets minimum detectable

Sub-hysteresis

1 - set window lower

2 - raise window after trigger *switch NMOS ratio*
hold until triggers back

- *limit reduced to overlap*
- *no action on input or threshold signals*

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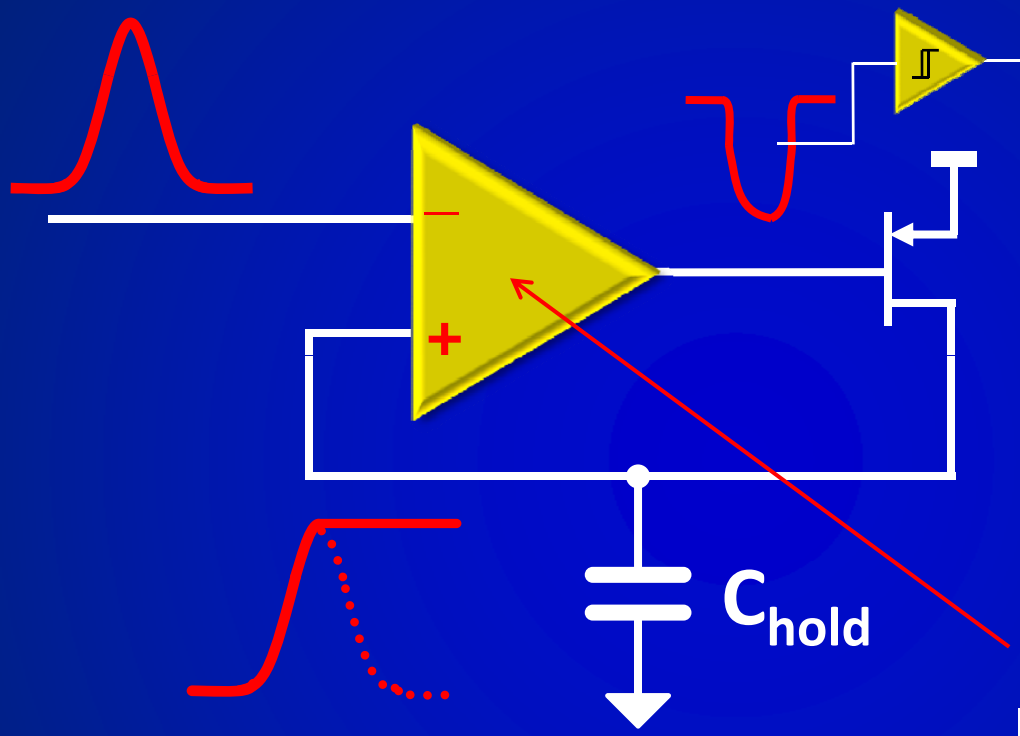
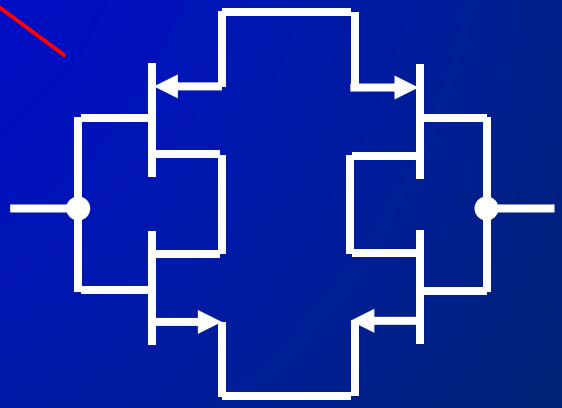
Peak Detector



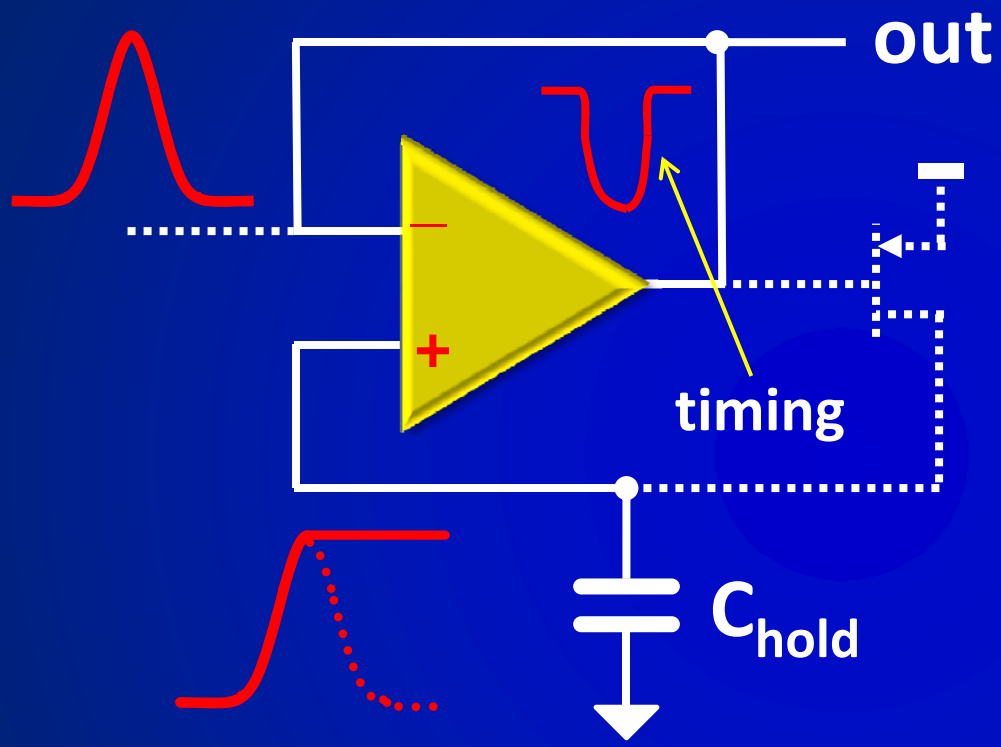
- peak and time
- large offsets
- low drive



rail-to-rail differential input

(from low-voltage of deep submicron CMOS)

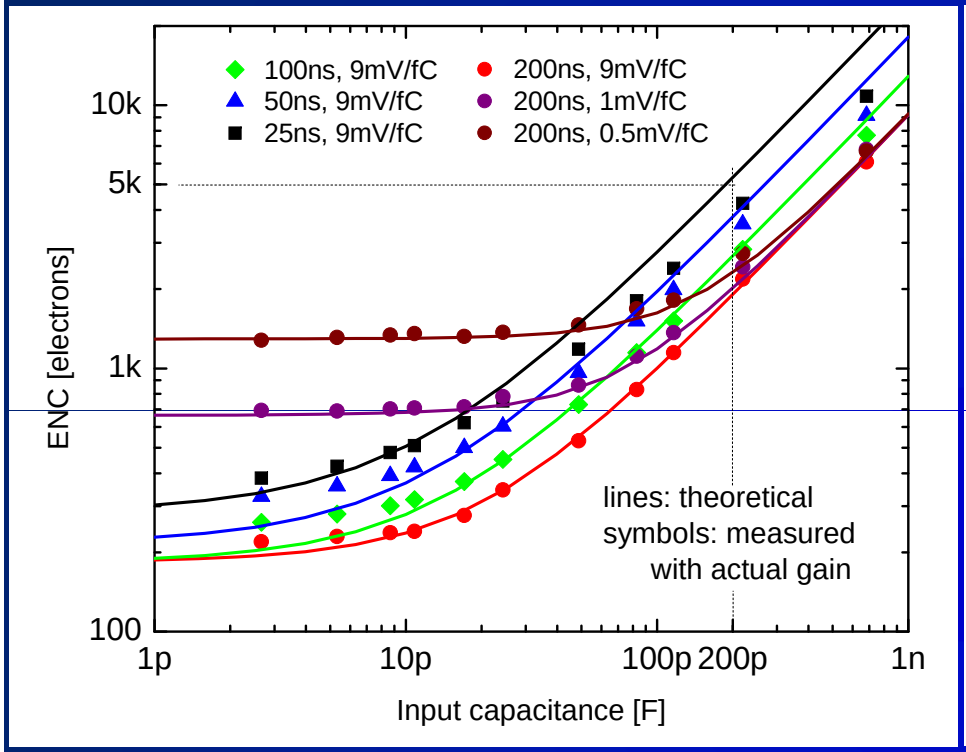
Multi-Phase Peak Detector



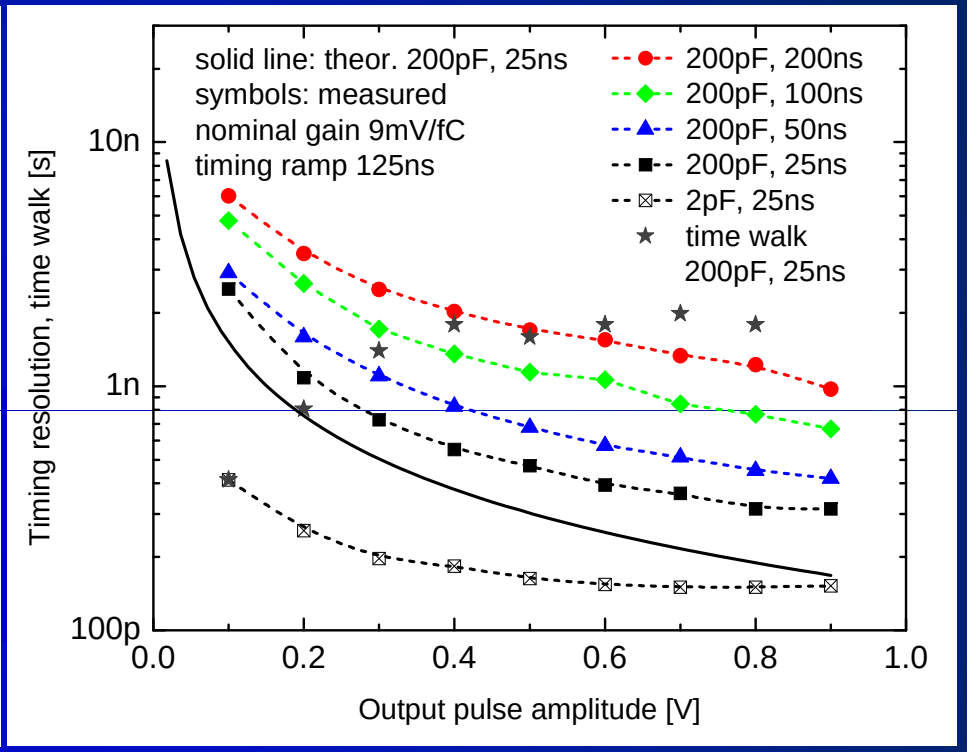
- peak
- timing at peak
- analog memory
- offsets cancel
- high drive

Resolution Measurements

charge resolution



timing resolution



- **charge resolution** ENC < 5,000 e^- at 25 ns, 200 pF
- **analog dynamic range** Q_{max} / ENC > 12,000 → DDF
- **timing resolution** < 1 ns (at peak-detect)

$$\sigma_t \approx \frac{ENC\ \tau_P}{Q}\frac{\lambda_P}{\rho_P}$$

≈ 0.3-0.8

G. De Geronimo, in "Medical Imaging" by Iniewski

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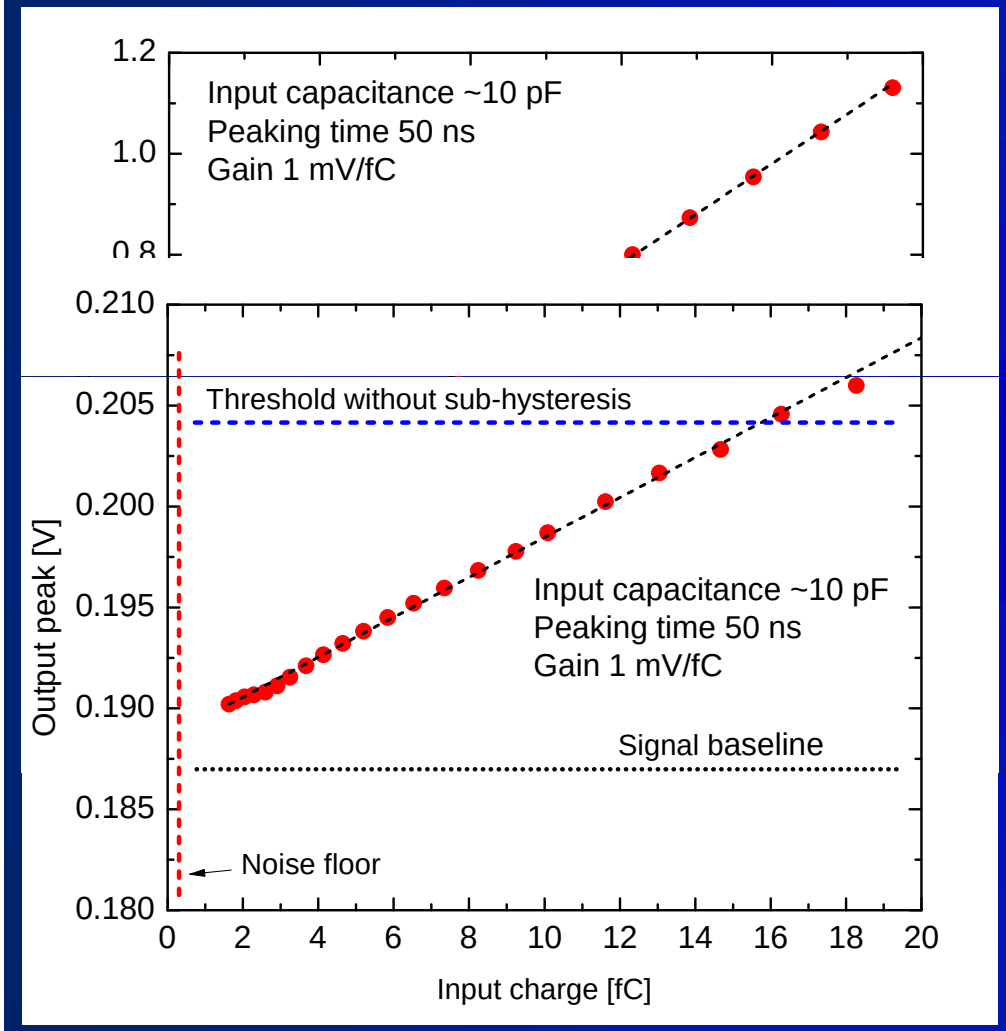
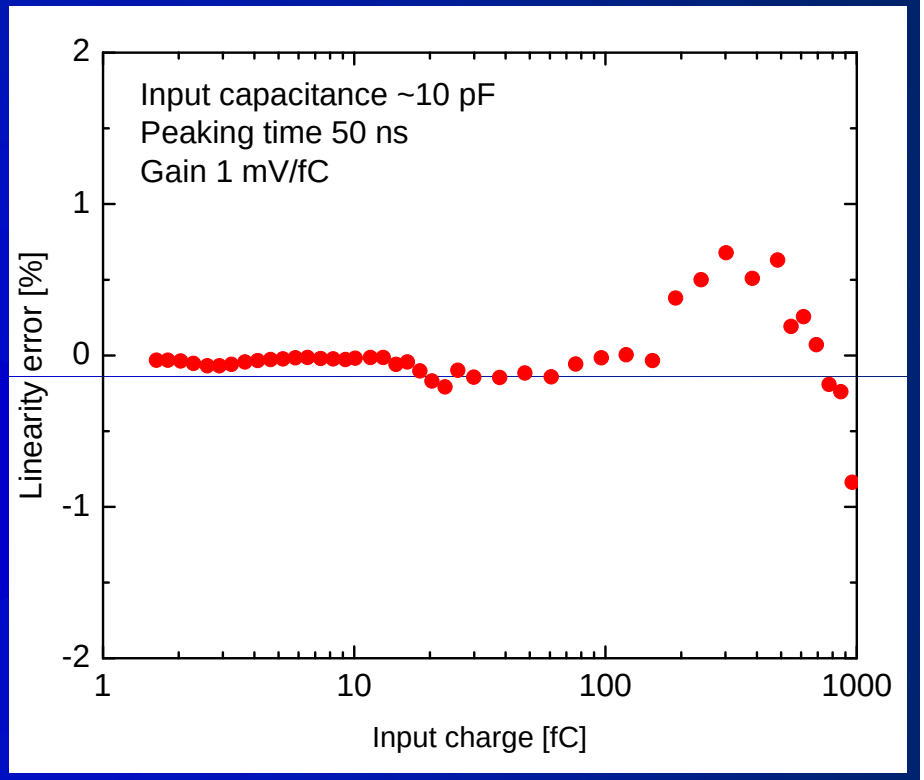
Peak Measurements

Peak vs charge

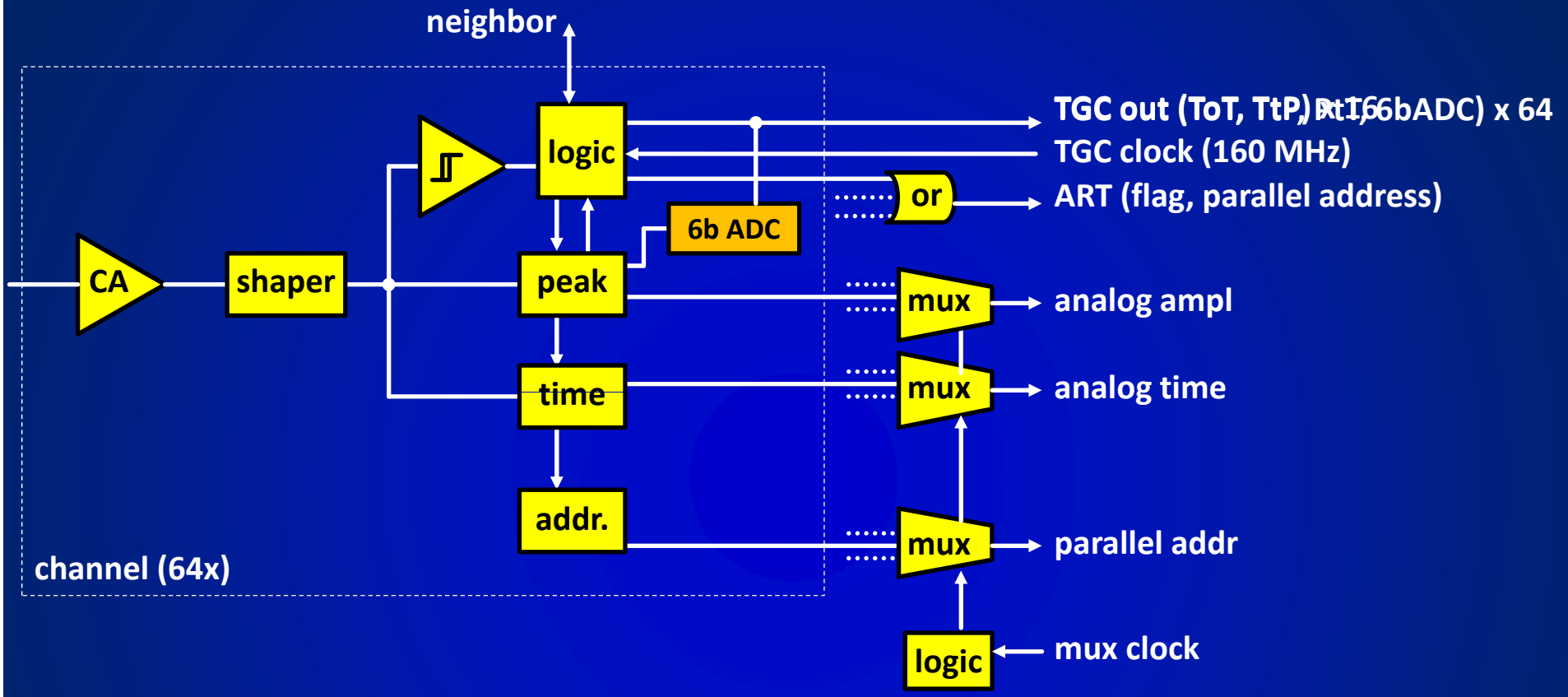


Linearity error



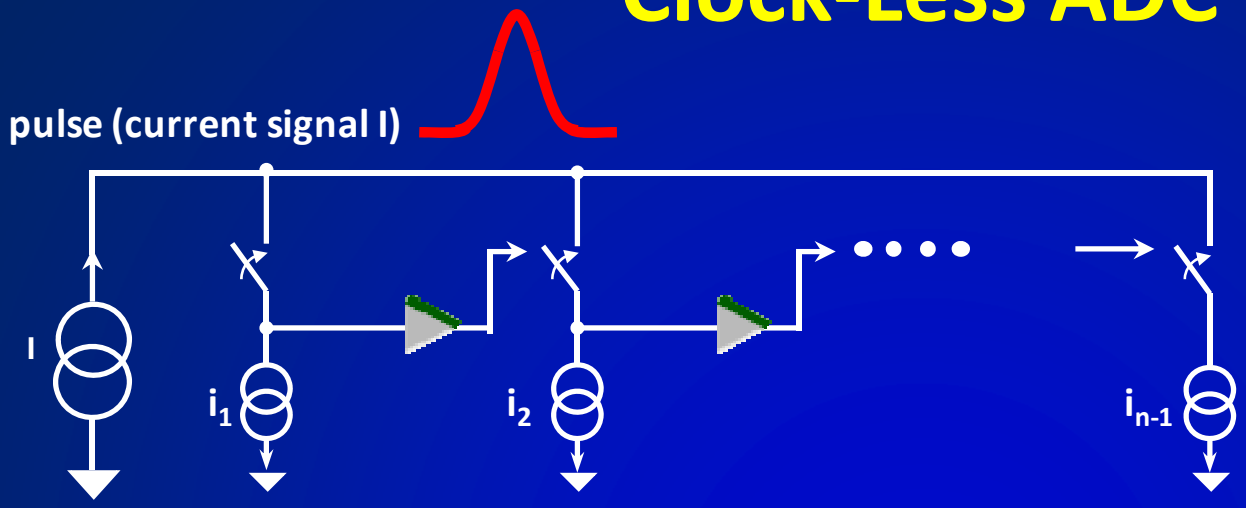
- **discriminating few mV**
  from baseline, in sub-hysteresis mode
- **linearity error < 1%**
  full 1V swing

Architecture of VMM2



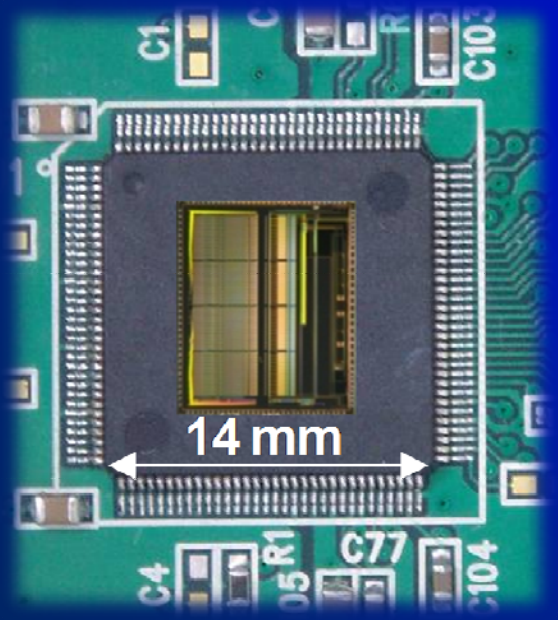
- TGC: 64 outputs, 6-bit ADC 25ns with serialized output

Clock-Less ADC

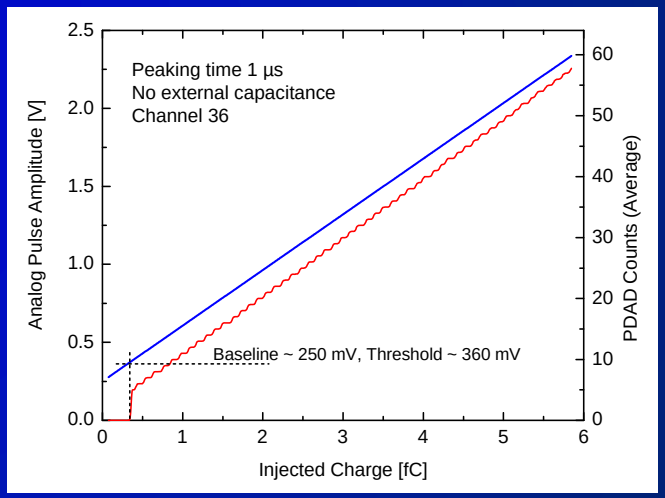


- current mode
- clock-less
- peak-detect
- real-time
- low power

digital thermometer



year 2007
64 channels
PDD 500ns, 6-bit



ADC not fast enough for ATLAS (25ns): need a <u>current-output peak detector</u>

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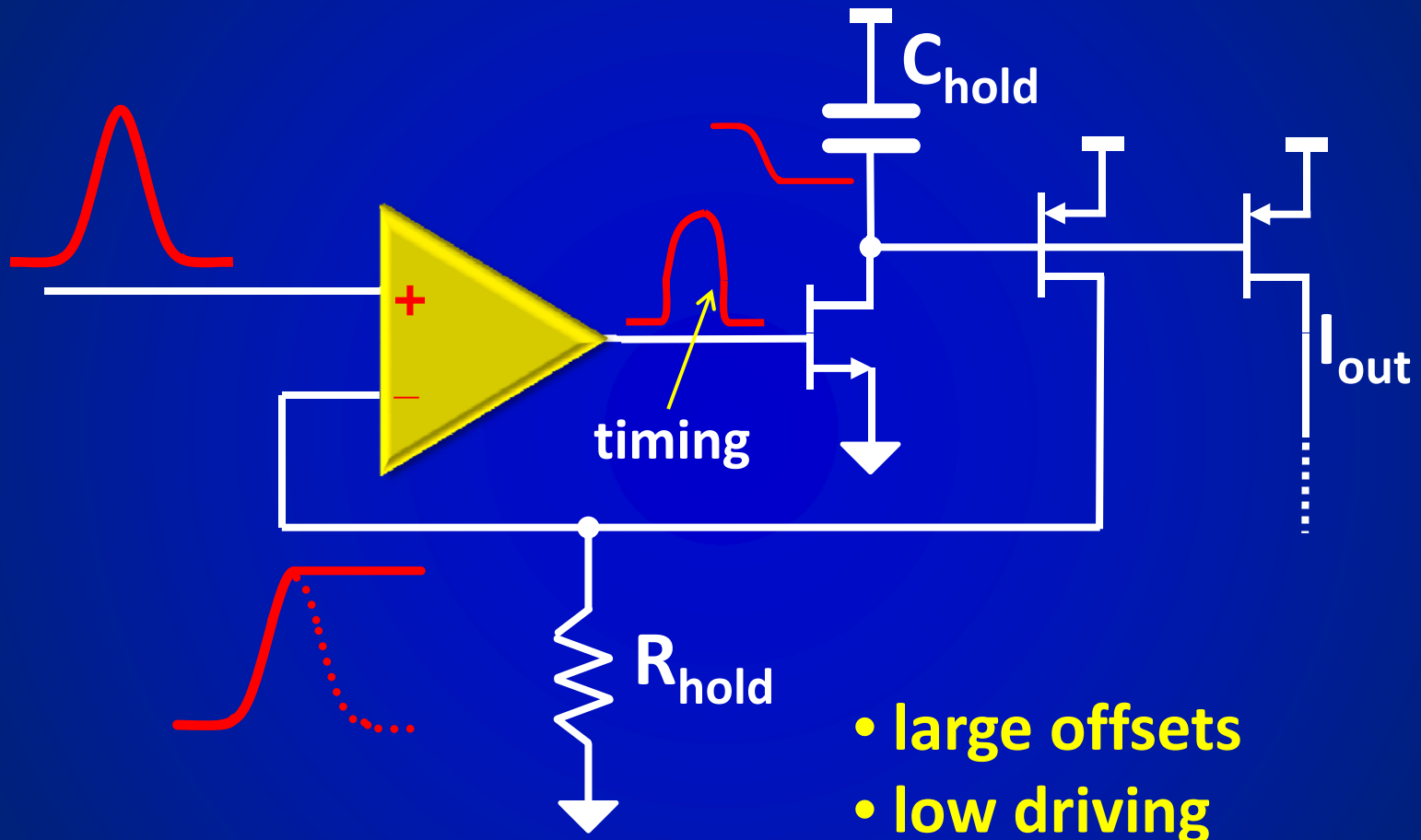
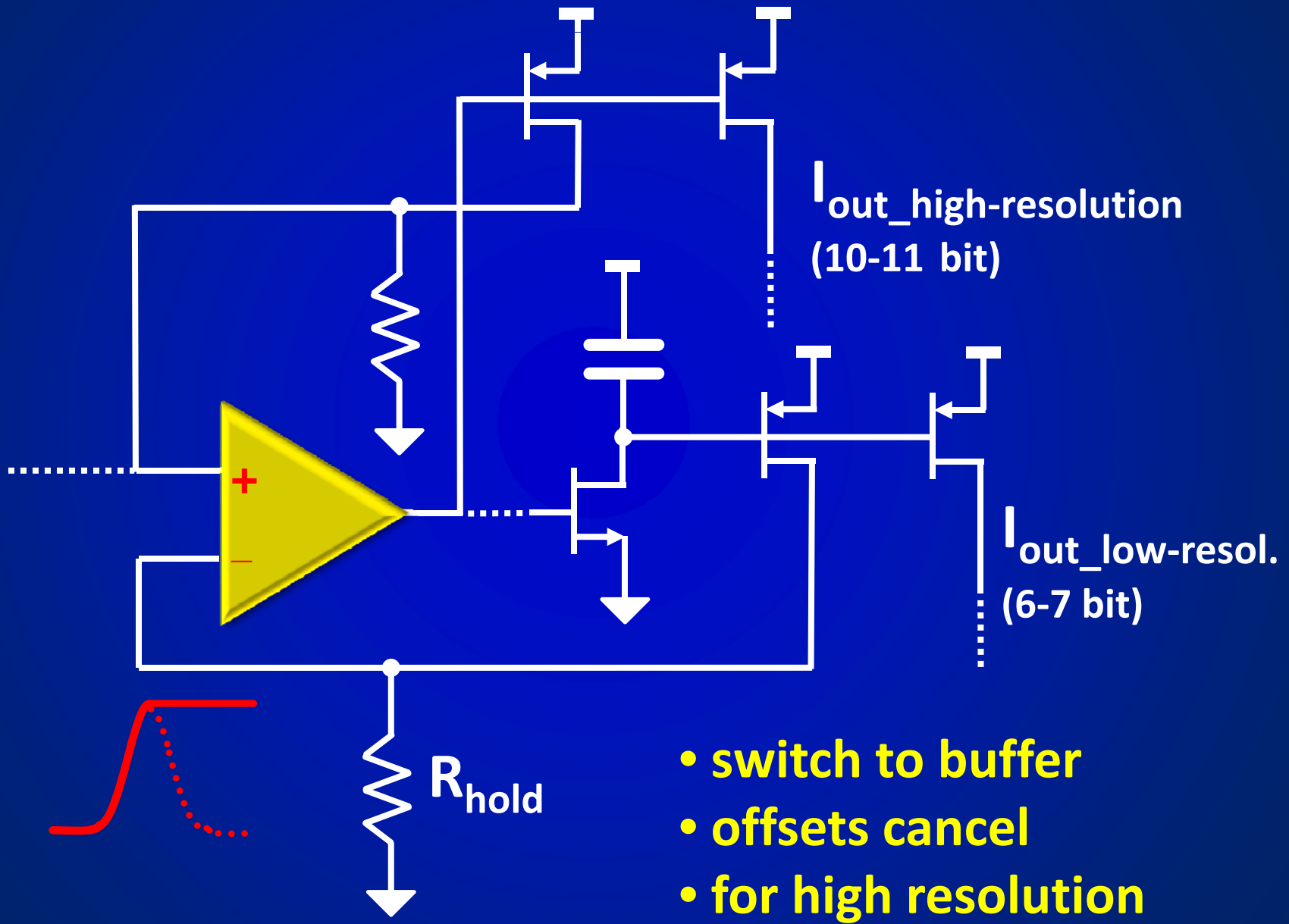
Current-Output Peak Detector (COPD)



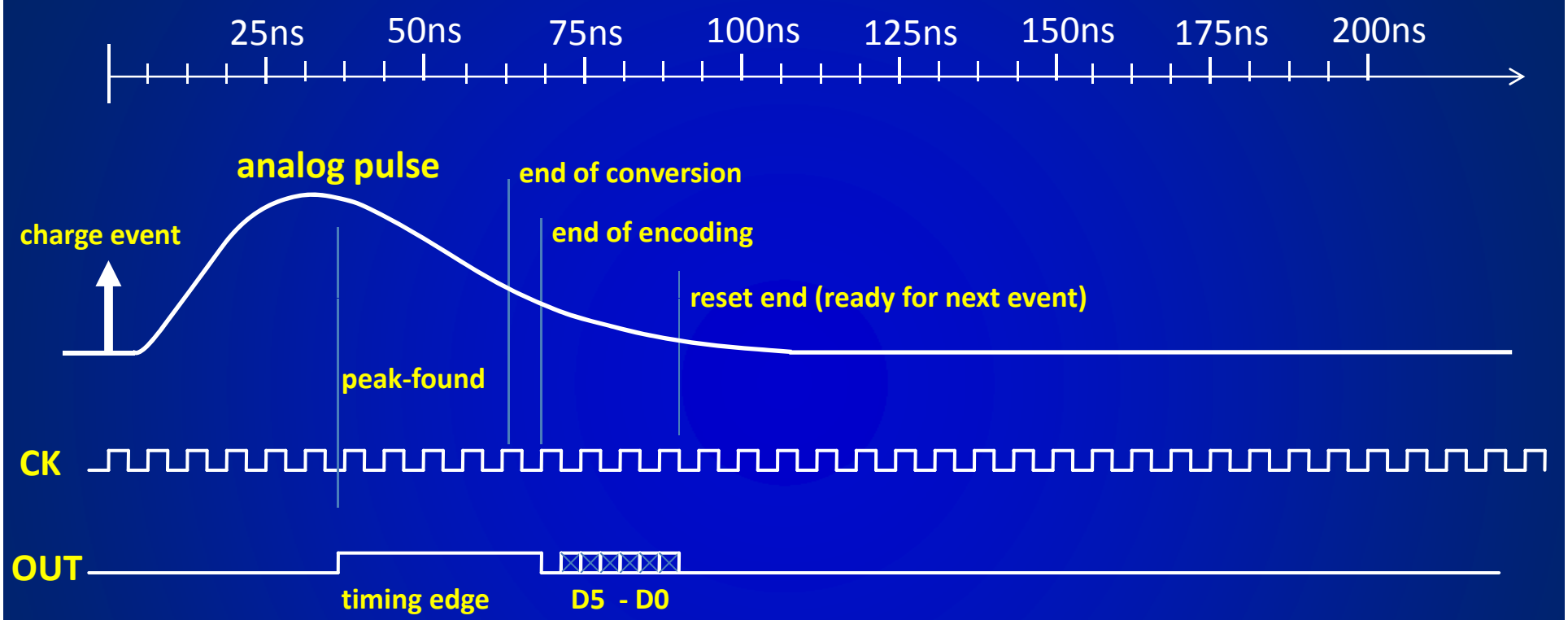
- large offsets
- low driving
- low resolution

Multi-Phase COPD



- switch to buffer
- offsets cancel
- for high resolution

TGC ADC and Serializer



- conversion ends ~25ns after peak-found, programmable
- dead time from event <100ns
- amplitude data *D5-D0* shifted at each clock edge
- 160 MHz readout

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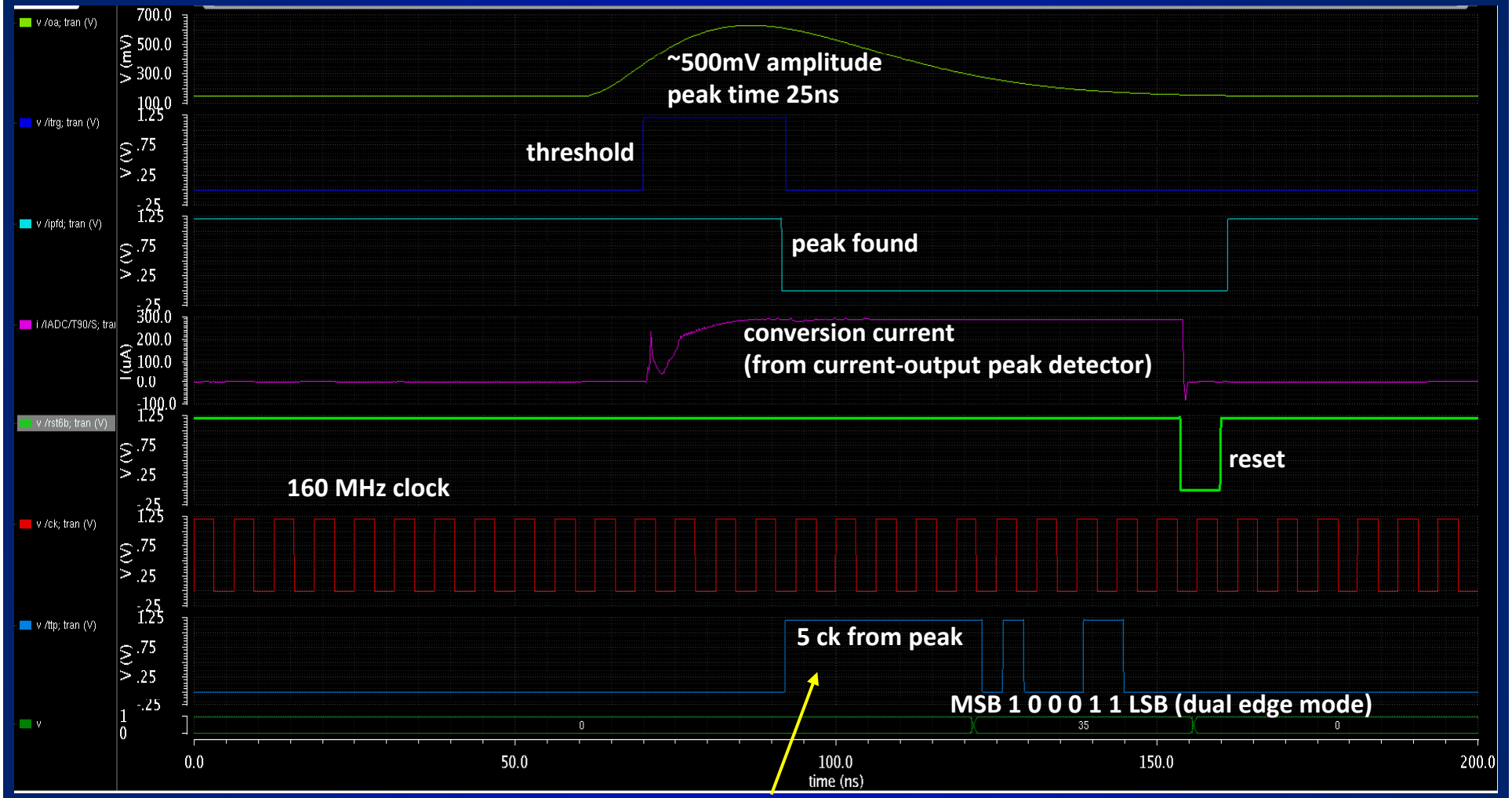
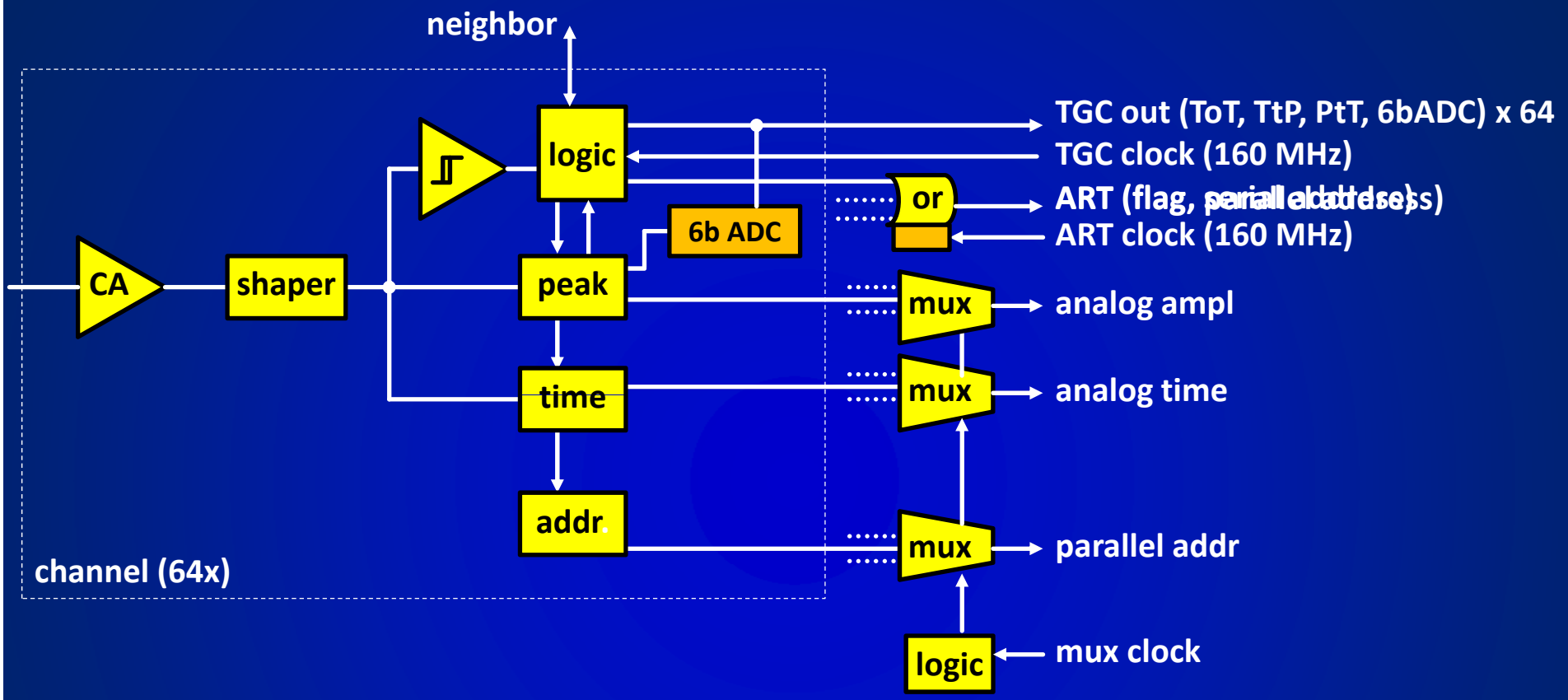
COPD, 6b-ADC, Serialization - Simulation



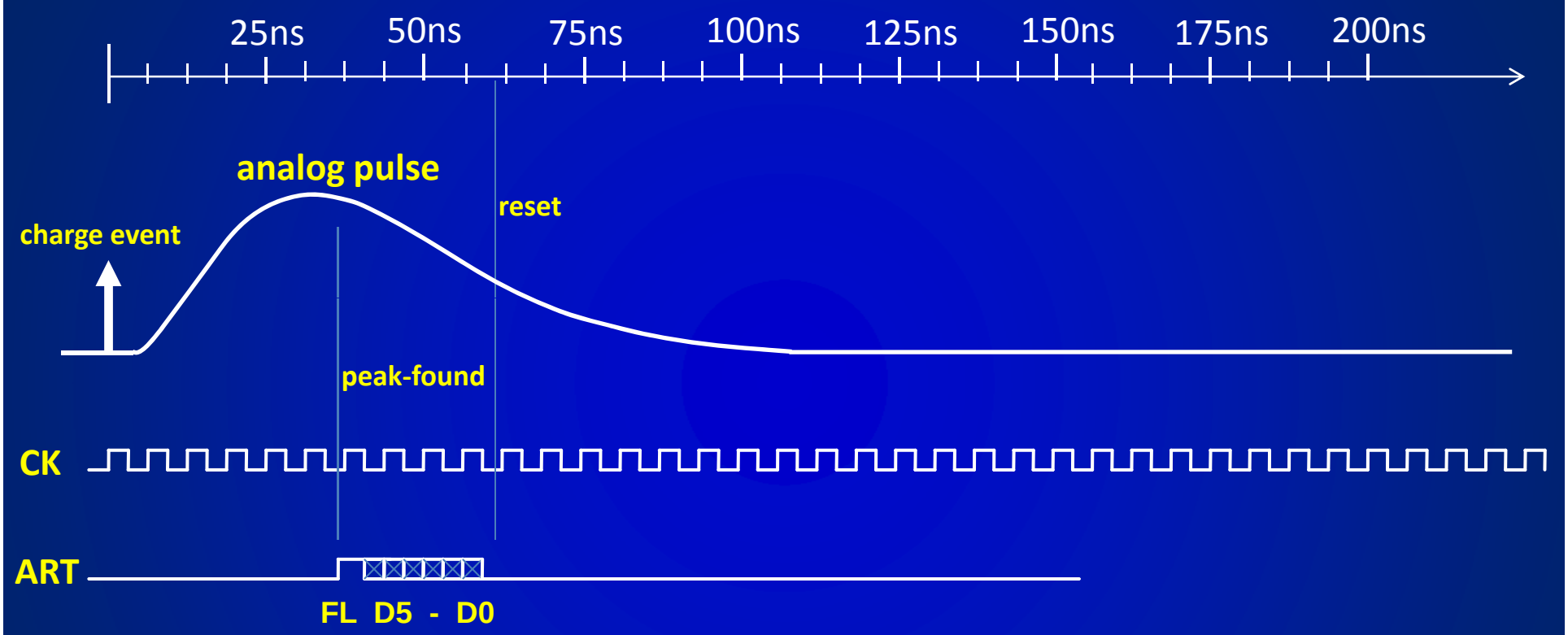
- programmable conversion time (3-bit, 1 to 8 clocks from peak found)
- programmable serialization (single or dual edge clock)
- programmable baseline subtraction (3-bit)

Architecture of VMM2



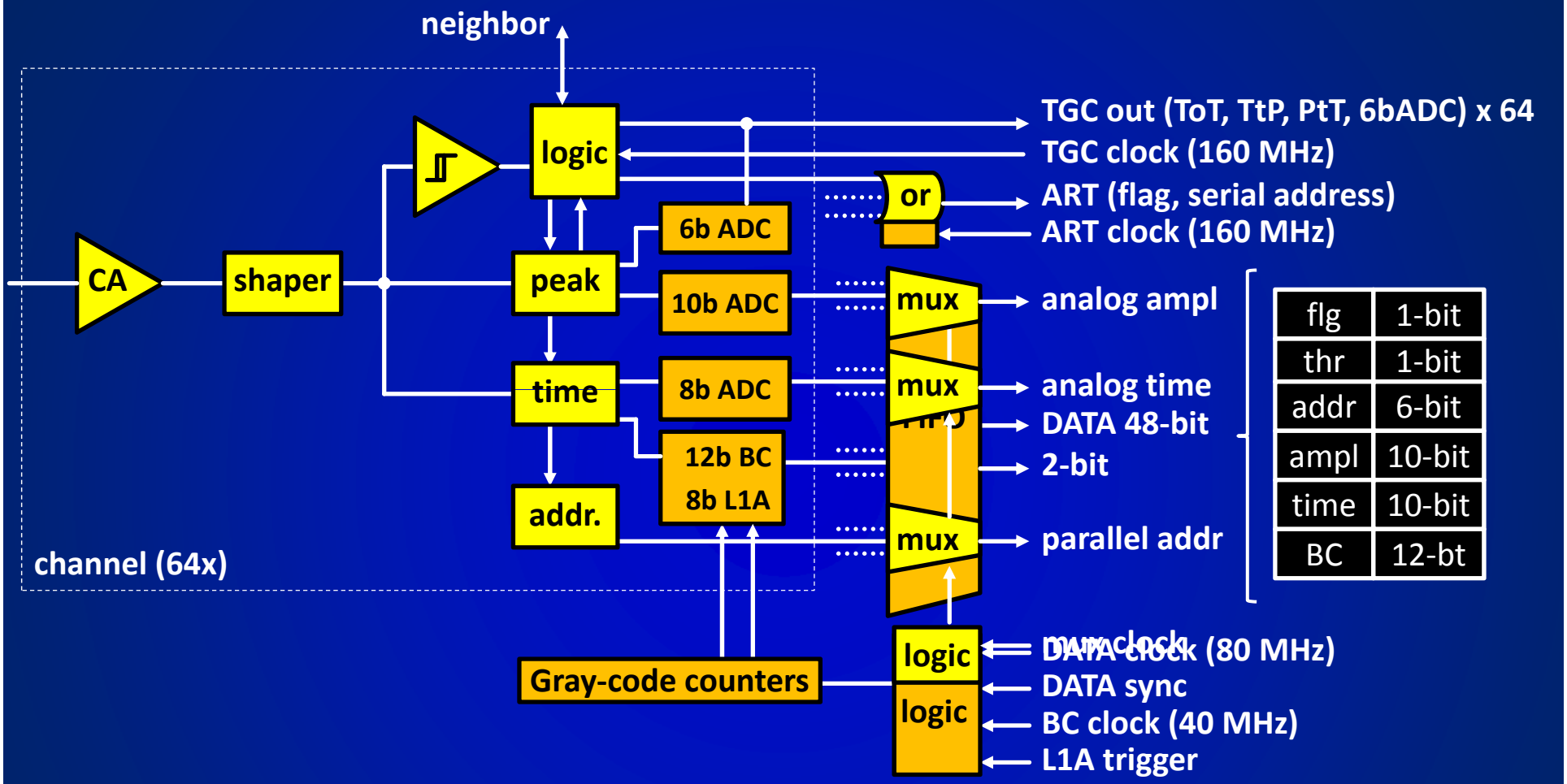
- TGC: 64 outputs, PtT, 6-bit ADC 25ns with serialized output
- ART (Address in Real Time): serialized flag and address

ART (Address in Real Time)



- flag and address serialized
- address data optionally D5-D0 shifted at each clock edge
- 160 MHz readout

Architecture of VMM2



- TGC: 64 outputs, PtT, 6-bit ADC 25ns with serialized output
- ART: serialized flag and address
- 10-bit ADC 250ns for amplitude, 8-bit ADC 125ns for timing, FIFO
- 12-bit Gray-code counter for BC timestamp
- Serialized 2-bit DATA output with dedicated sync, 160 MHz clock

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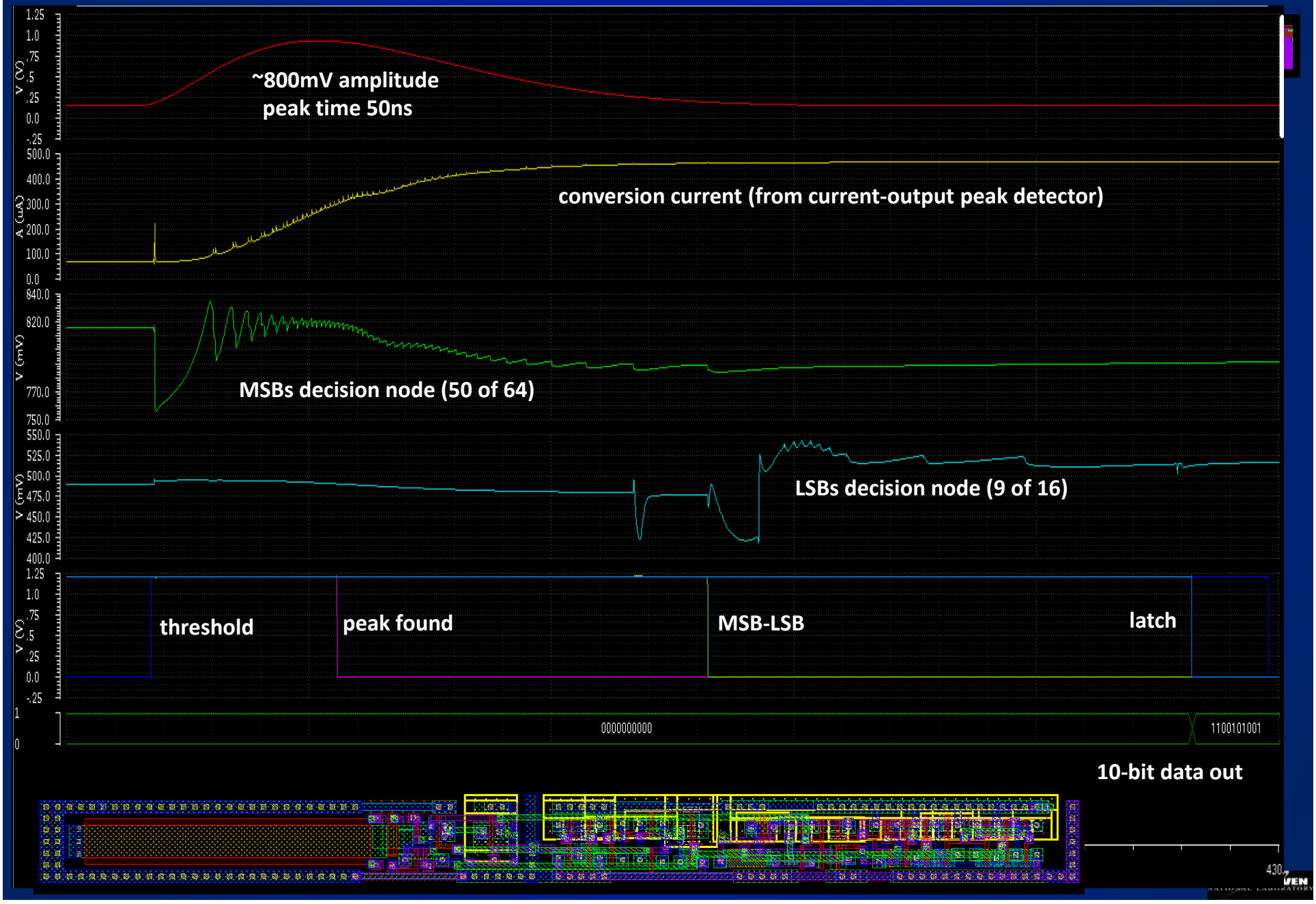
10-bit ADC


~800mV amplitude
peak time 50ns
conversion current (from current-output peak detector)
MSBs decision node (50 of 64)
LSBs decision node (9 of 16)
threshold
peak found
MSB-LSB
latch
0000000000
1100101001
10-bit data out

Conclusions

- VMM is an ASIC family for the ATLAS muon spectrometer small wheel upgrade
- VMM1 has been developed and tested at BNL and CERN, with results in agreement with the design - some issues with charge amplifier rise time, ESD protection leakage, digital pick-up
- VMM2 (in progress) will integrate a number of improvements (ADCs, FIFO) for simultaneous measurement and readout

Acknowledgment

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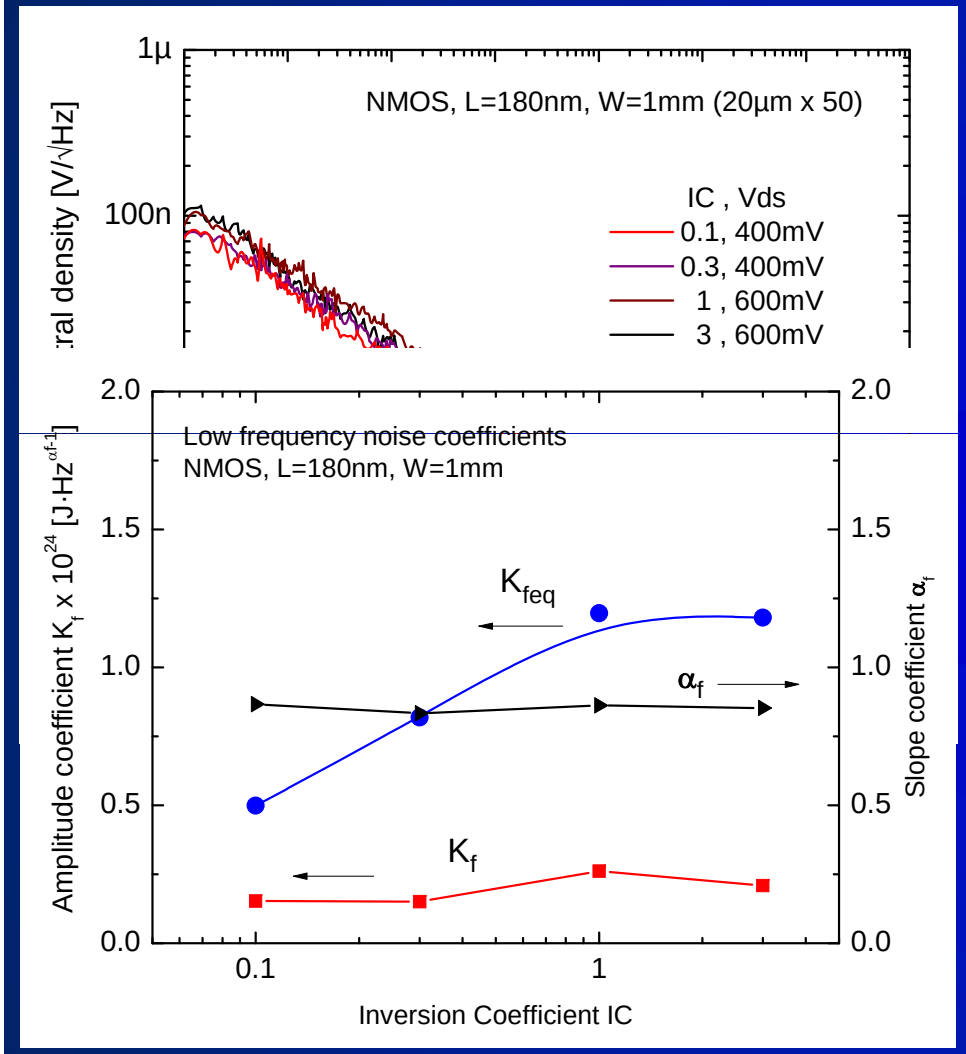
Howard Gordon and Craig Woody (BNL, USA)

ATLAS Collaboration, CERN (Alessandro Marchioro)

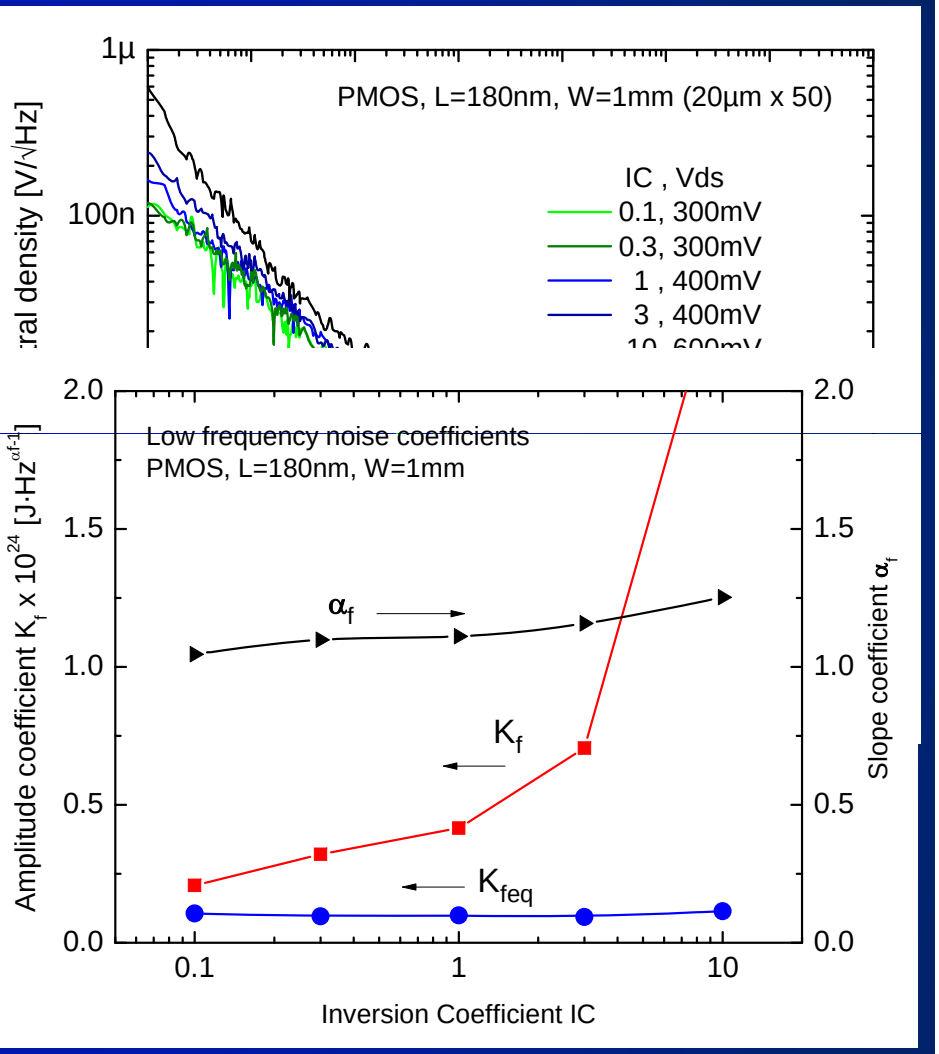
Backup

Noise measurements

NMOS



PMOS



Equivalent 1/f (K_{feq}) : equal value at twice the white component