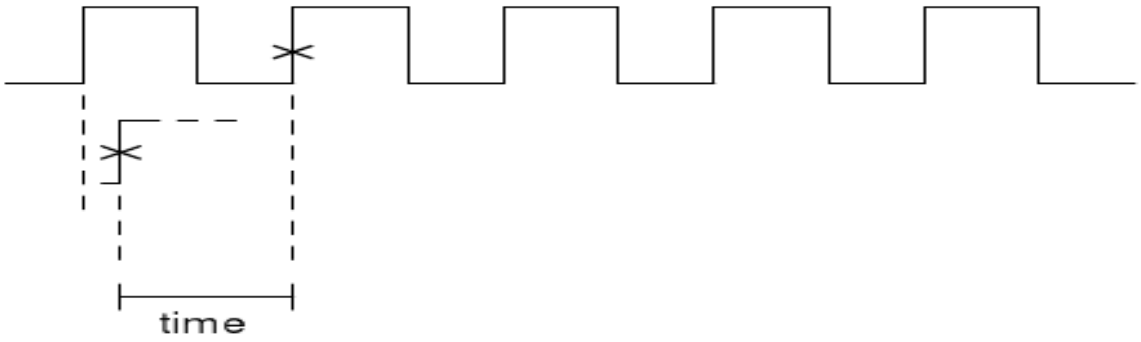
VLSI studens Internal talks

TDC and Hysteresis Comparator

Alberto Riccardi

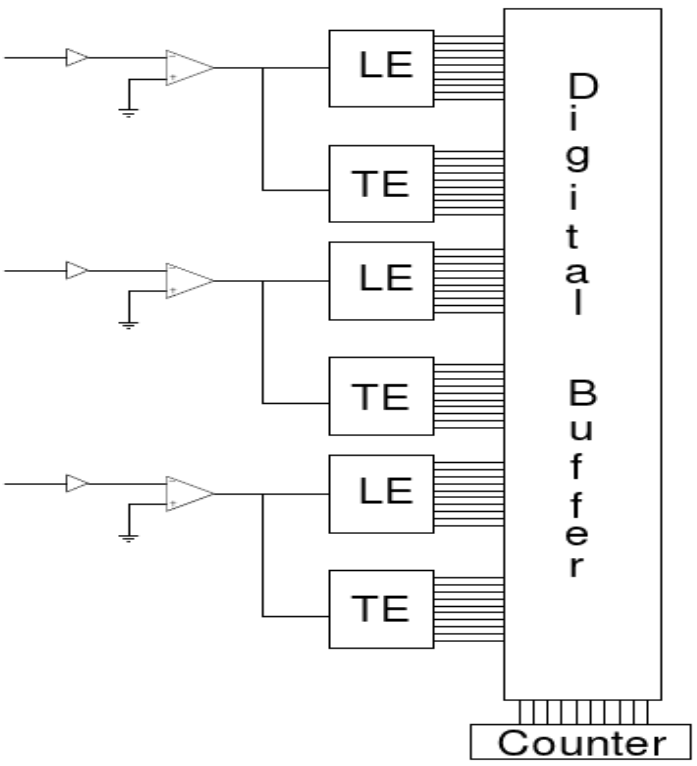
Clock resolution

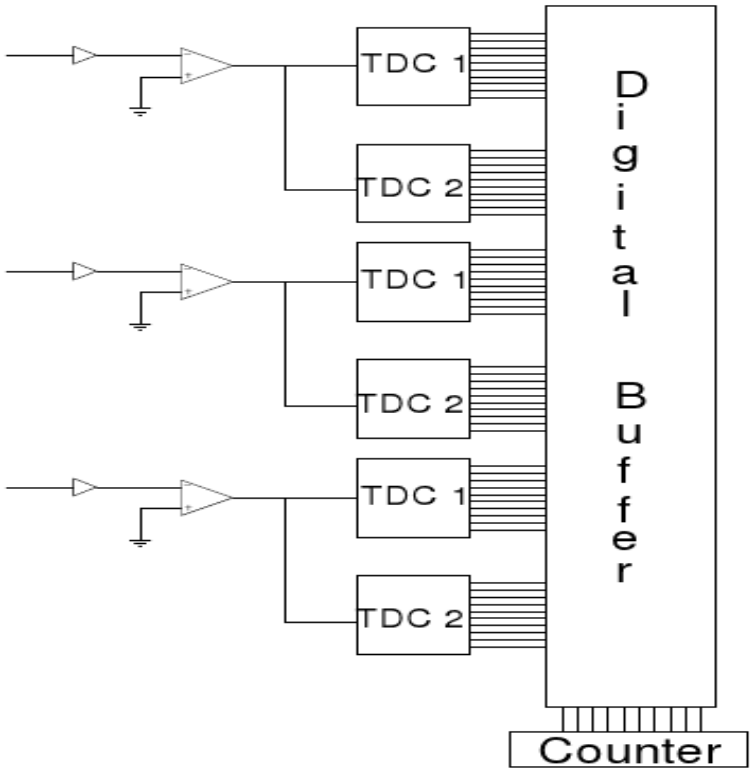
$2^9 = 512$ → 6.25ns • 512 = 3.2us



Since the rate per strip is about 30 kHz the biggest signal is exhausted in 3.2us, so we have a pile-up problem.
We want a system that has 1LSB = 400ps

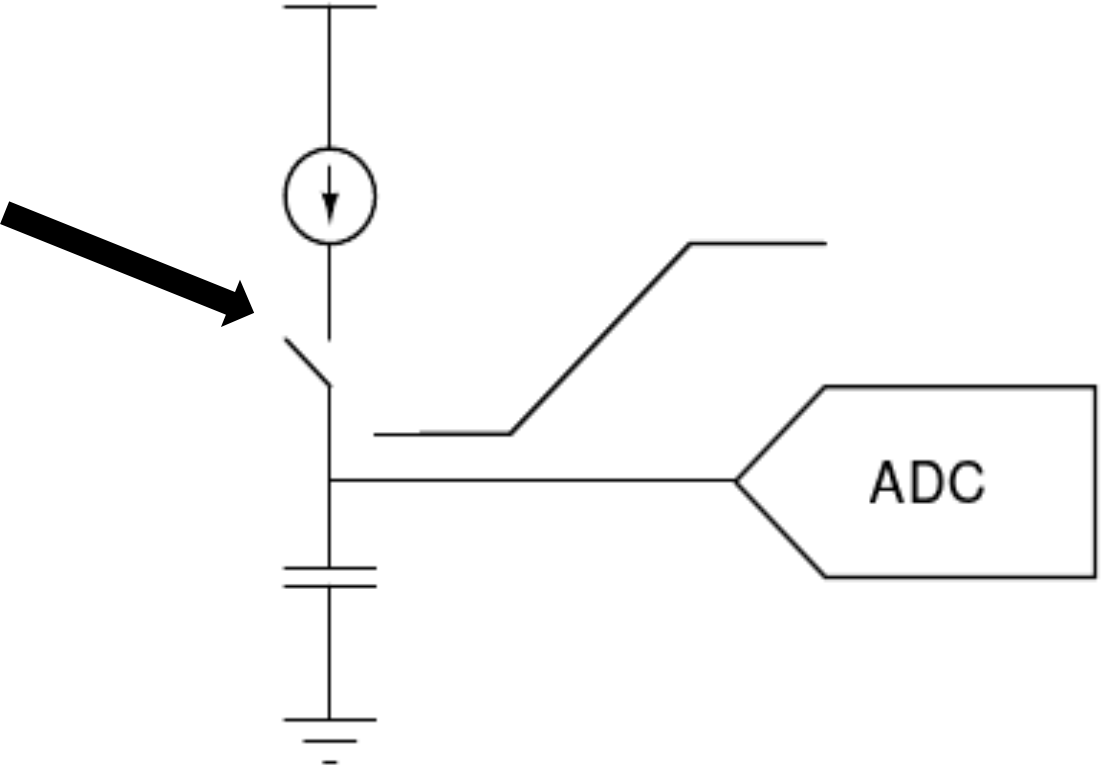
Goals





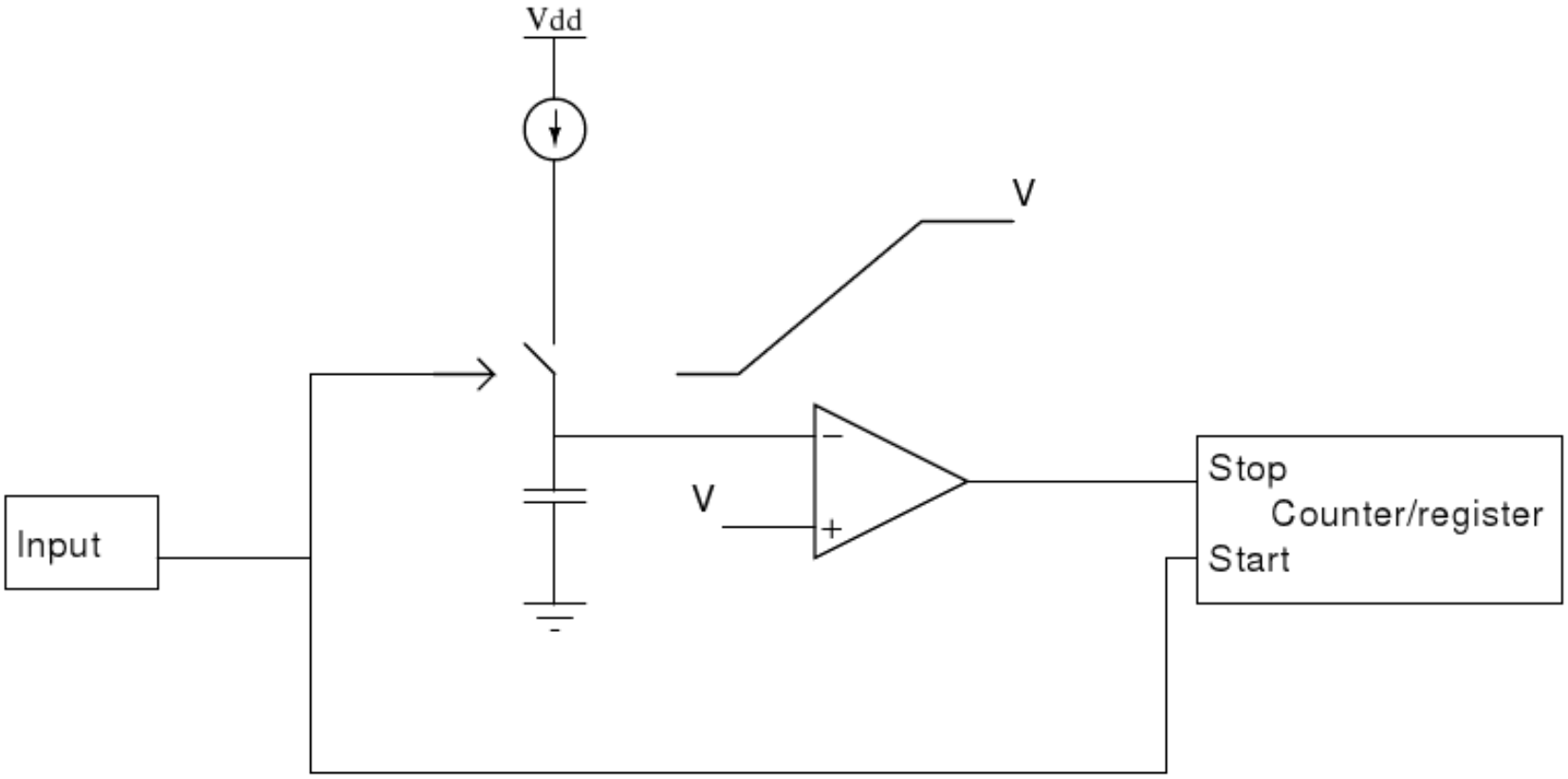
- Redesign and optimization the TDC
- Investigation about new technology

Time to Digital Converter

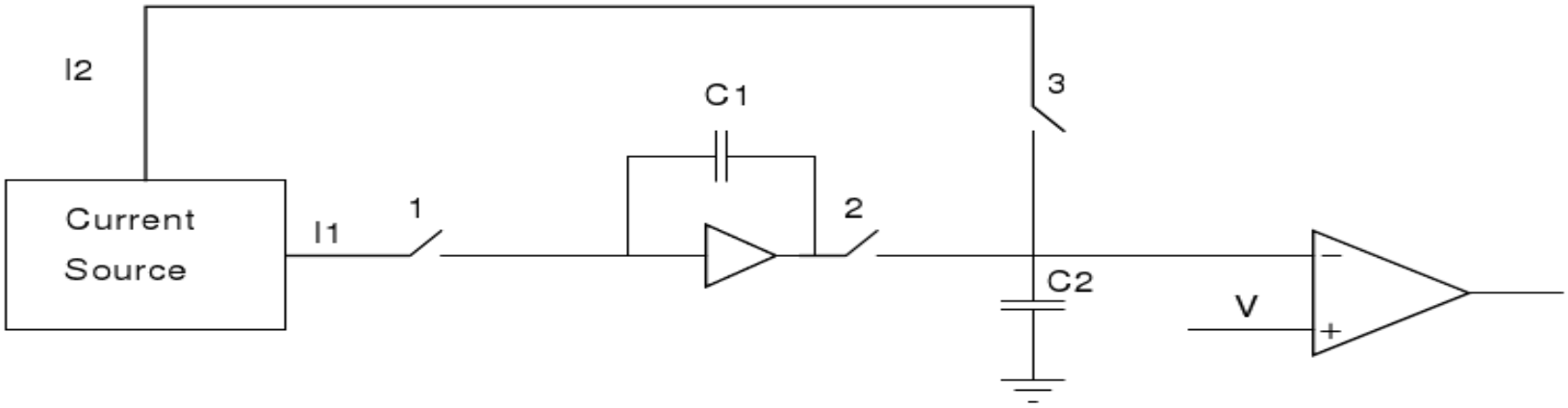


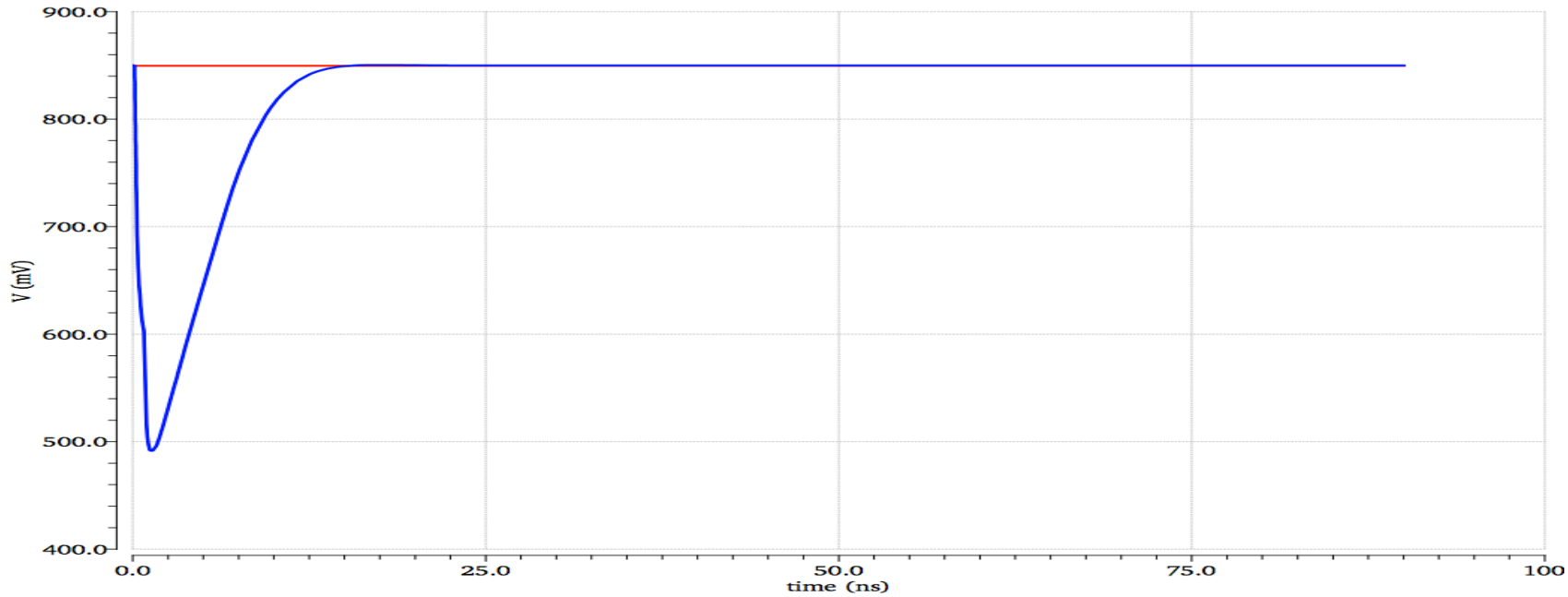
- Accurate
- Low power
- Compact
- Slow

Wilkinson ADC

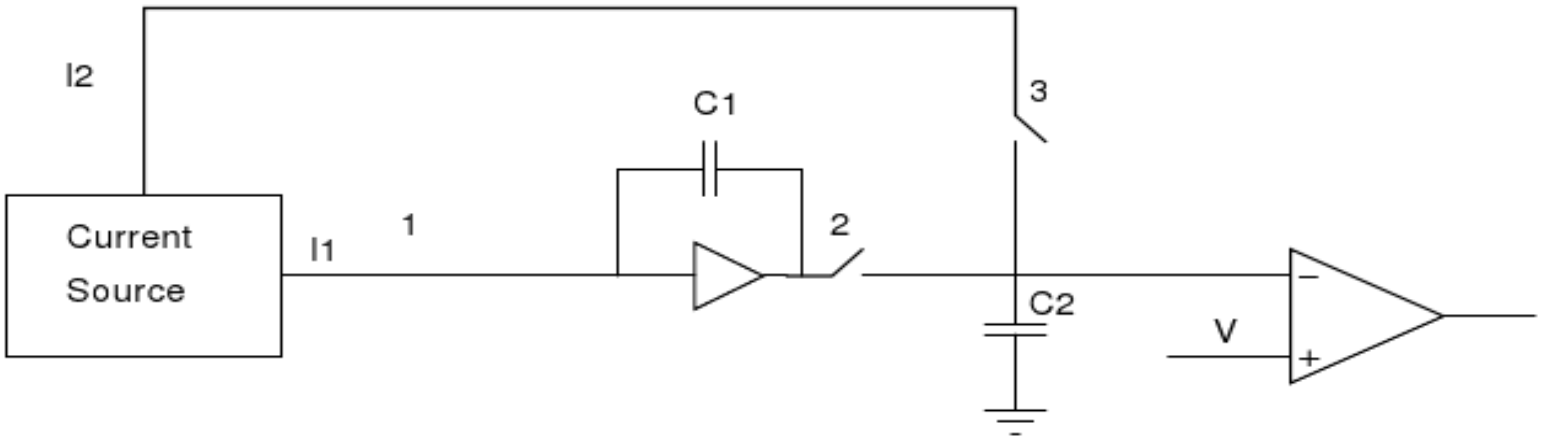


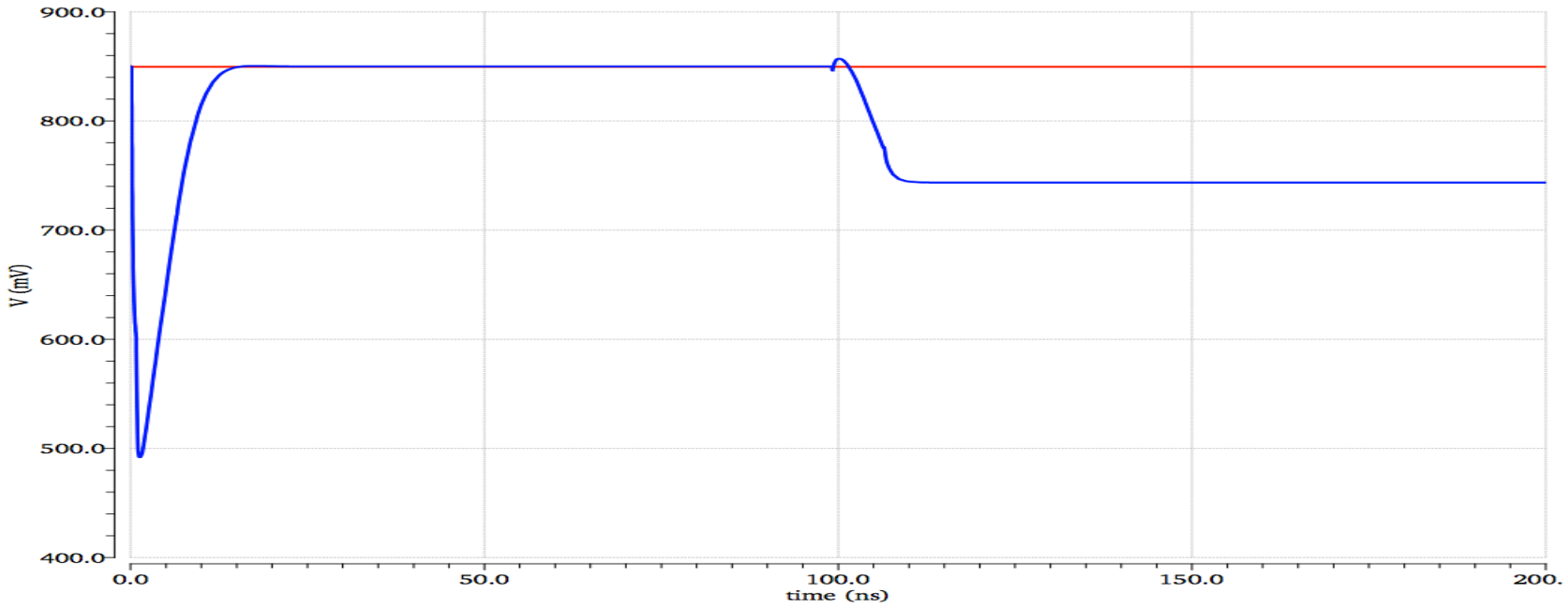
TDC implementation



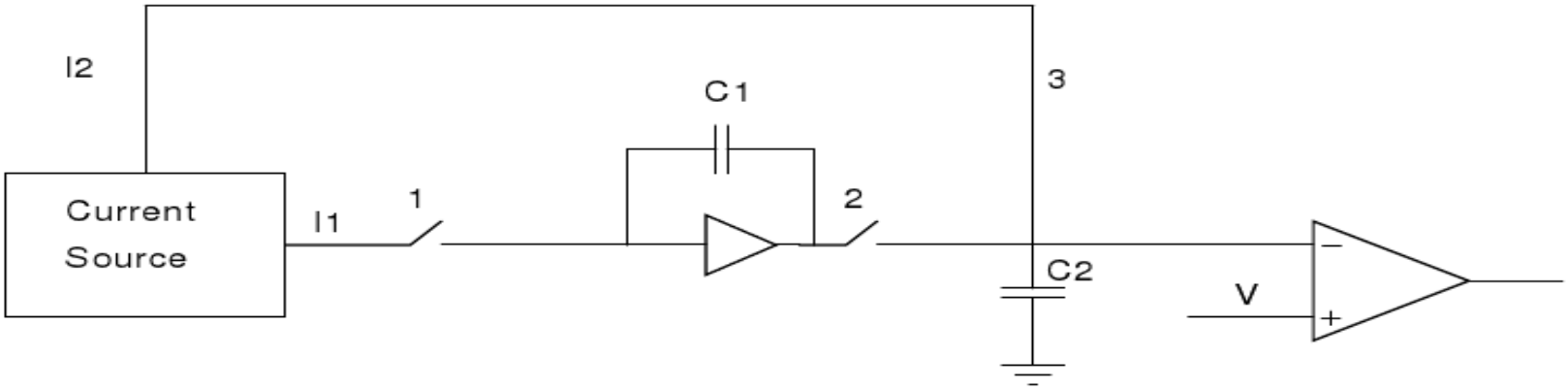


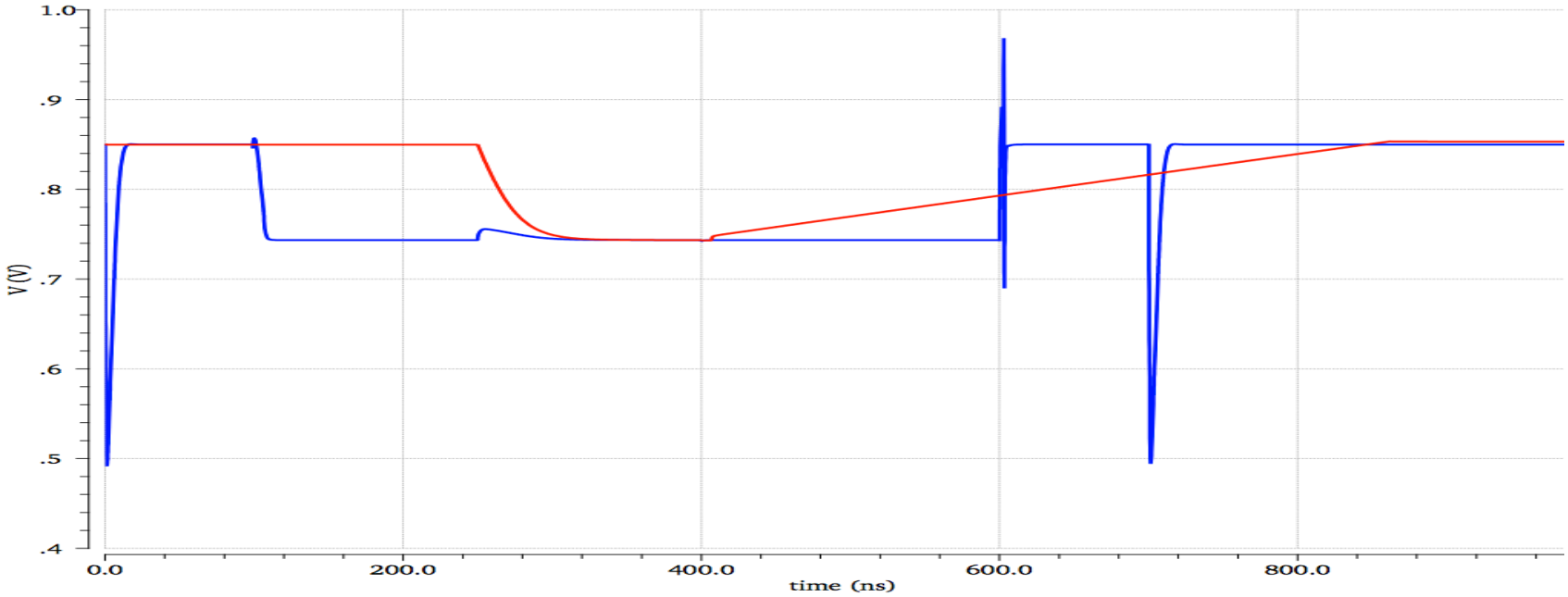
TDC implementation



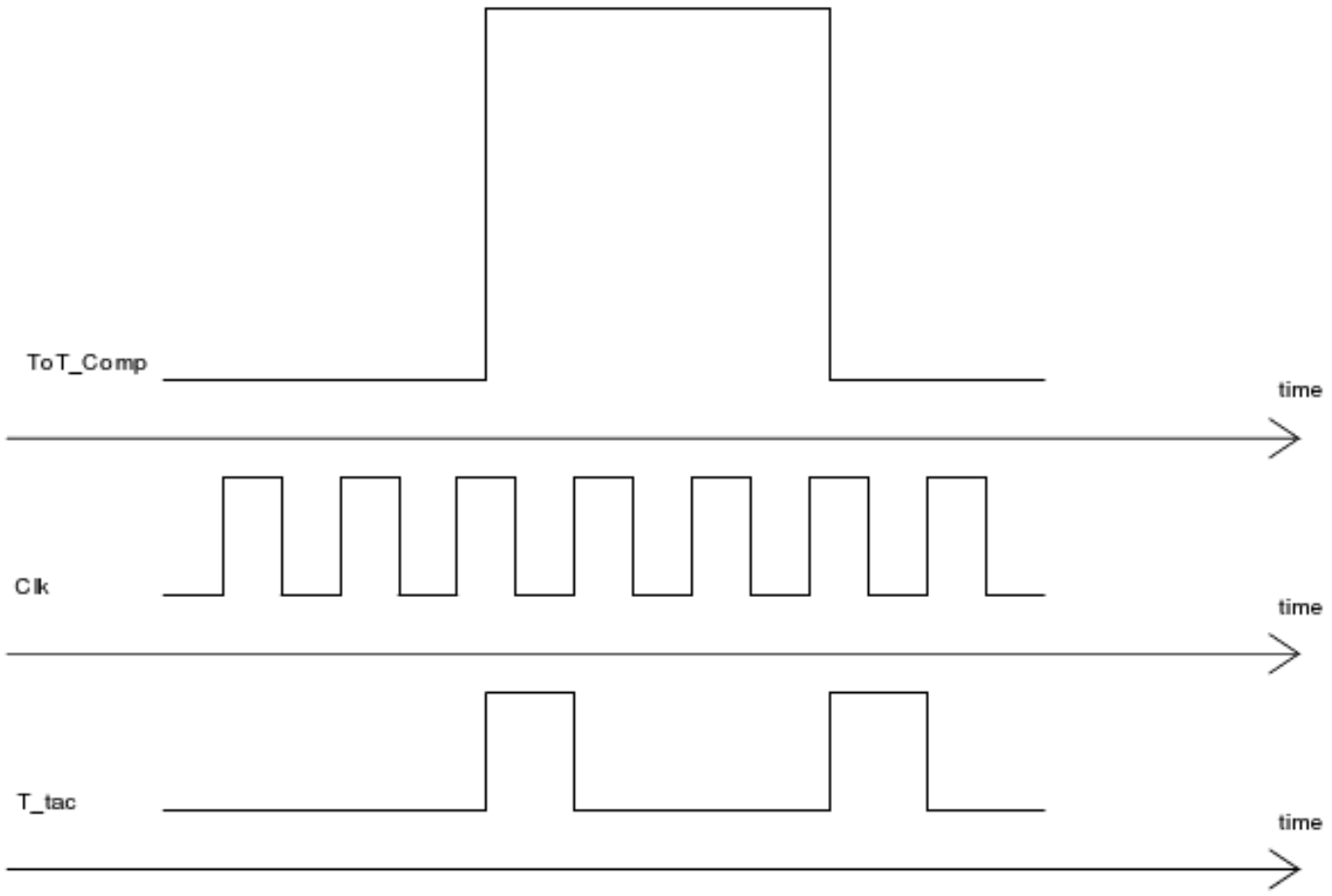


TDC implementation



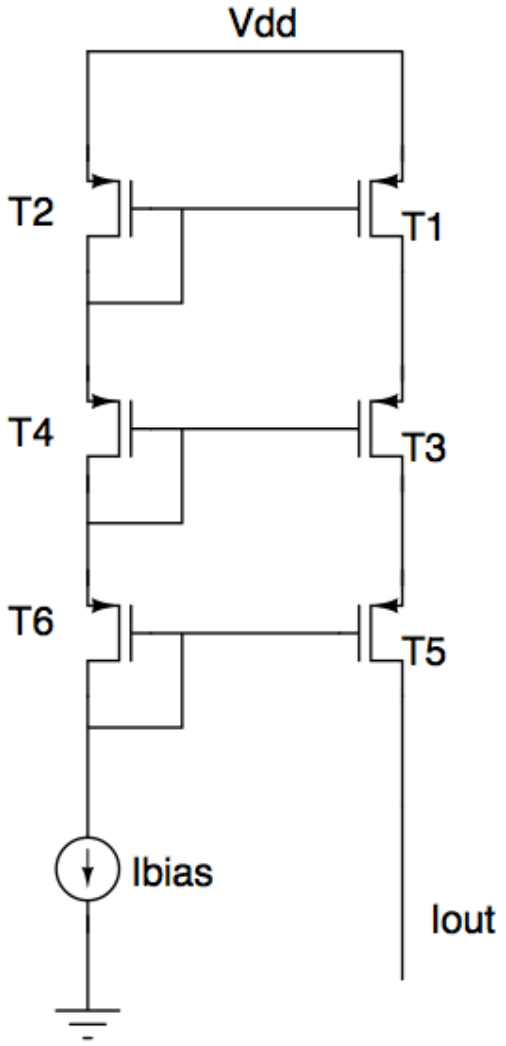


Timing



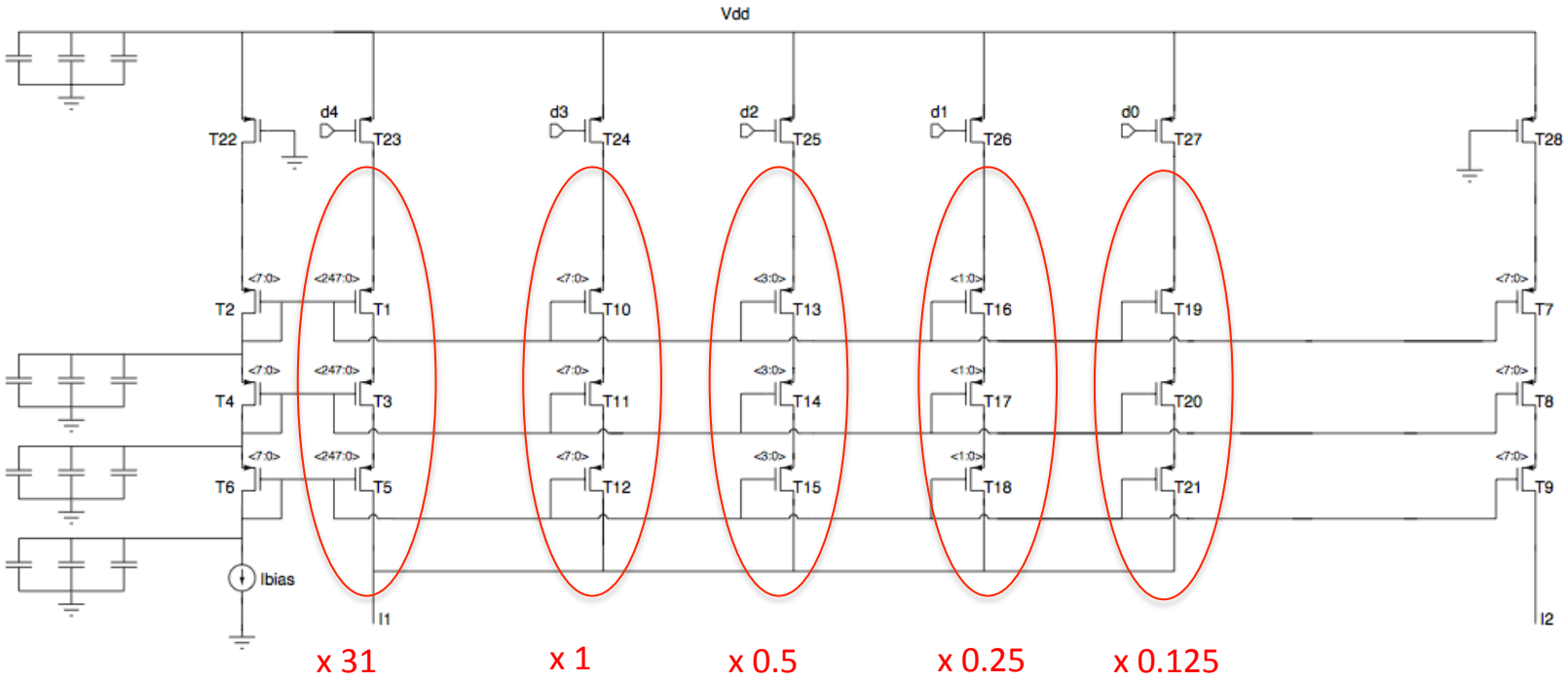
With this system we obtain that 1LSB = 49ps, since we have 6.25ns/128

Double cascode current mirror

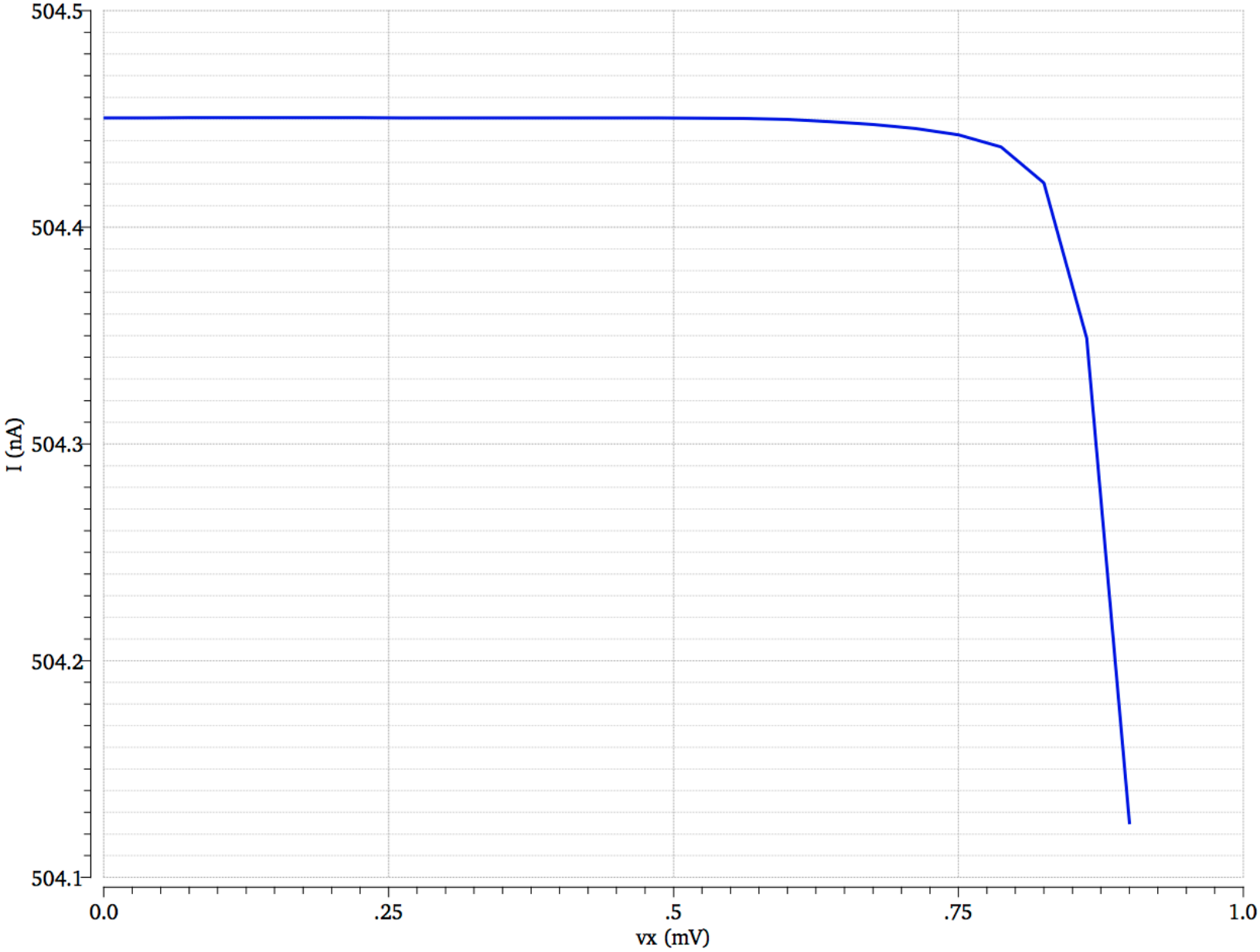


$$r_{out} \approx g_{m5} r_{05} r_{out1} = g_{m5} r_{05} g_{m3} r_{03} r_{01} \approx 550 M\Omega$$

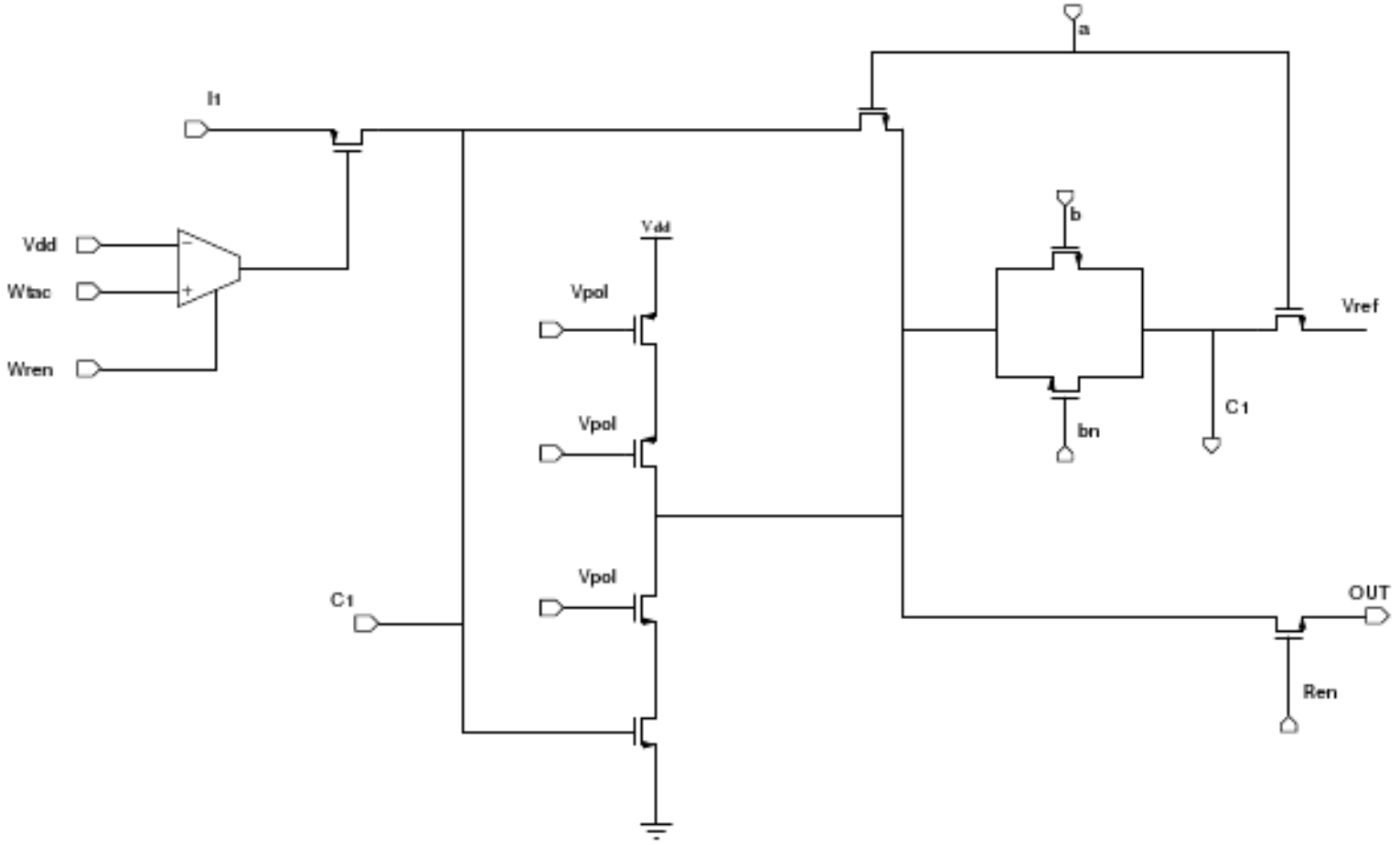
Transistor level implementation



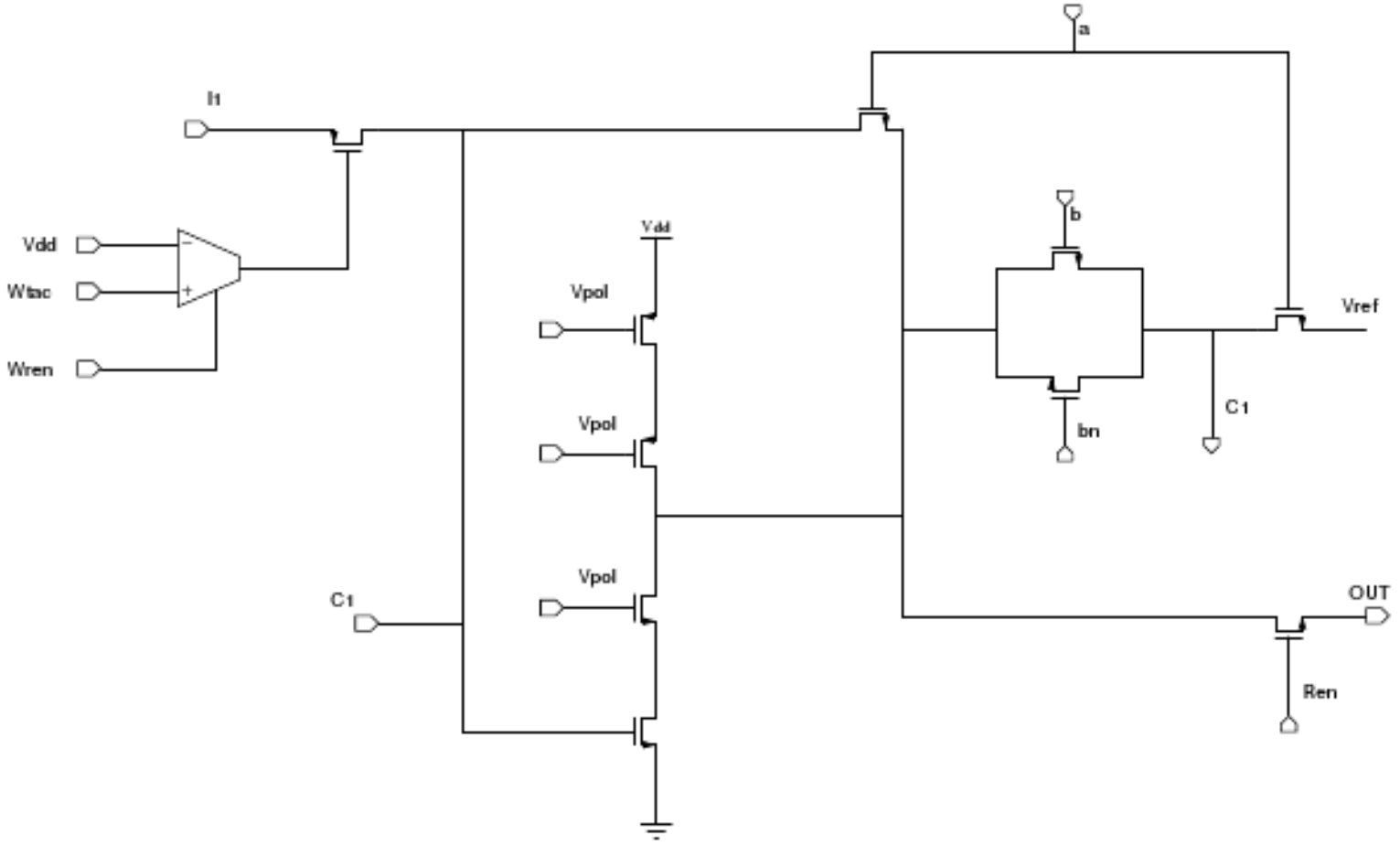
Current sweep



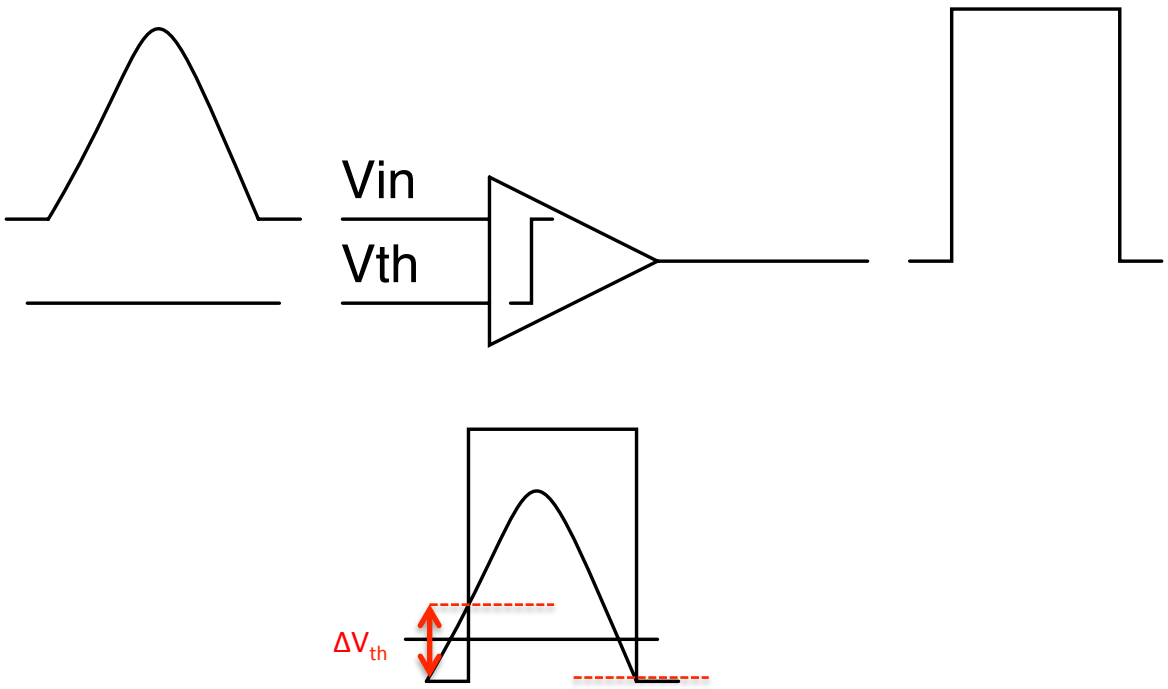
Time to Amplitude Converter



Time to Amplitude Converter

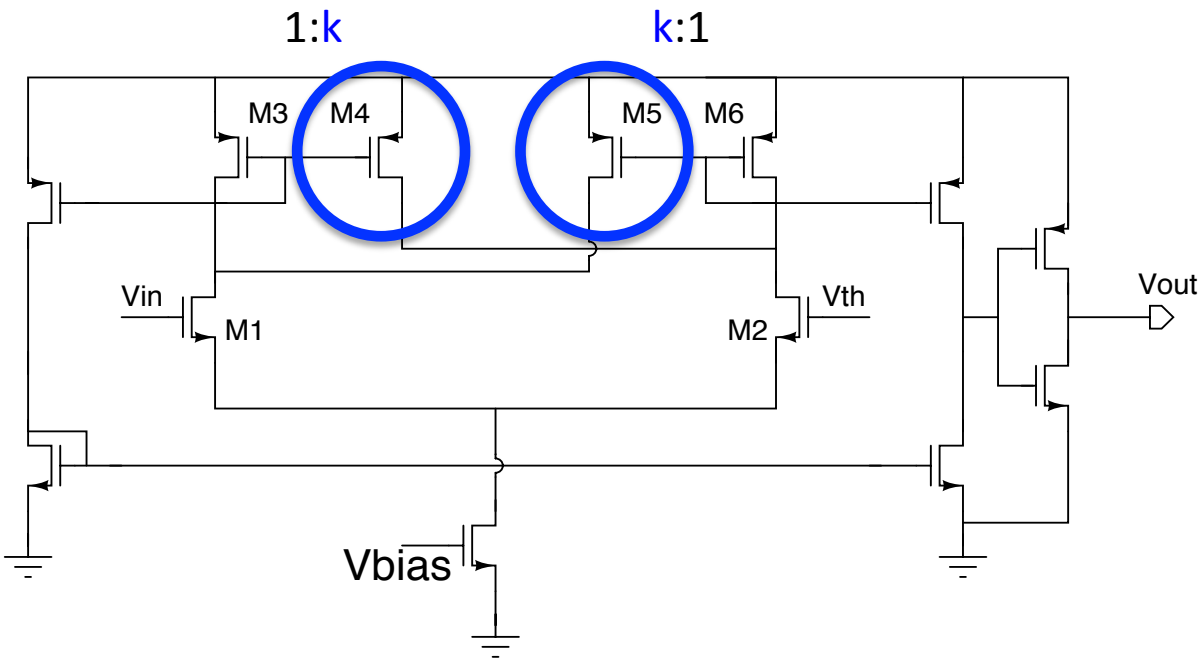


Hysteresis Comparator II



The output doesn't fire when the signal reaches the set threshold.

Hysteresis Comparator Transistor Level

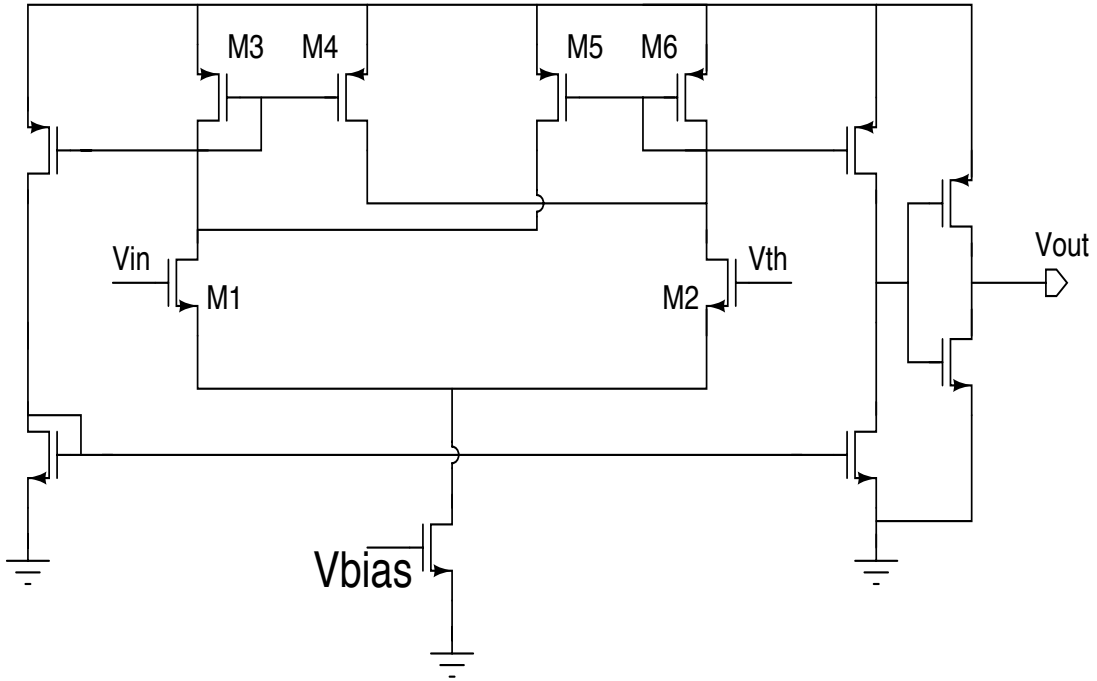


In the “classic” comparator the ouput changes when the current flowing into M1 is equal to the one into M2

In the hysteresis comparator we don’t have this effect

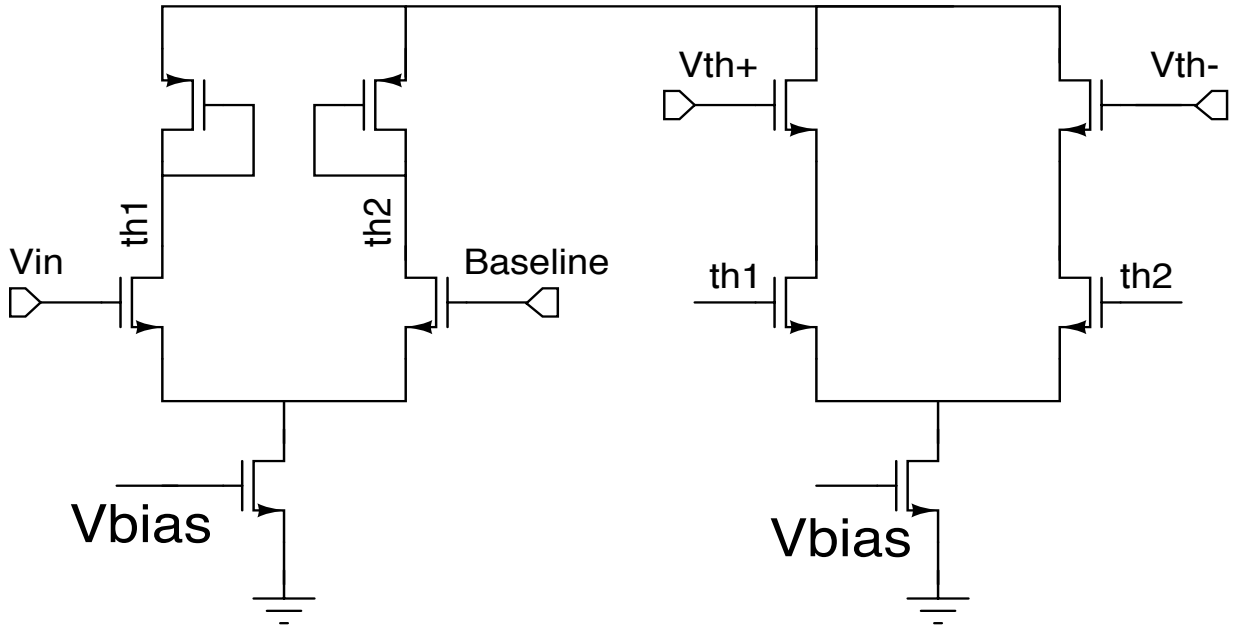
Hysteresis Comparator Current

- $i_{M1} = i_{M5}$
- $i_{M2} = i_{M4}$
- $i_{M5} = k^* i_{M6} = k^* i_{M2}$
- $i_{M1} + i_{M2} = i_{bias}$



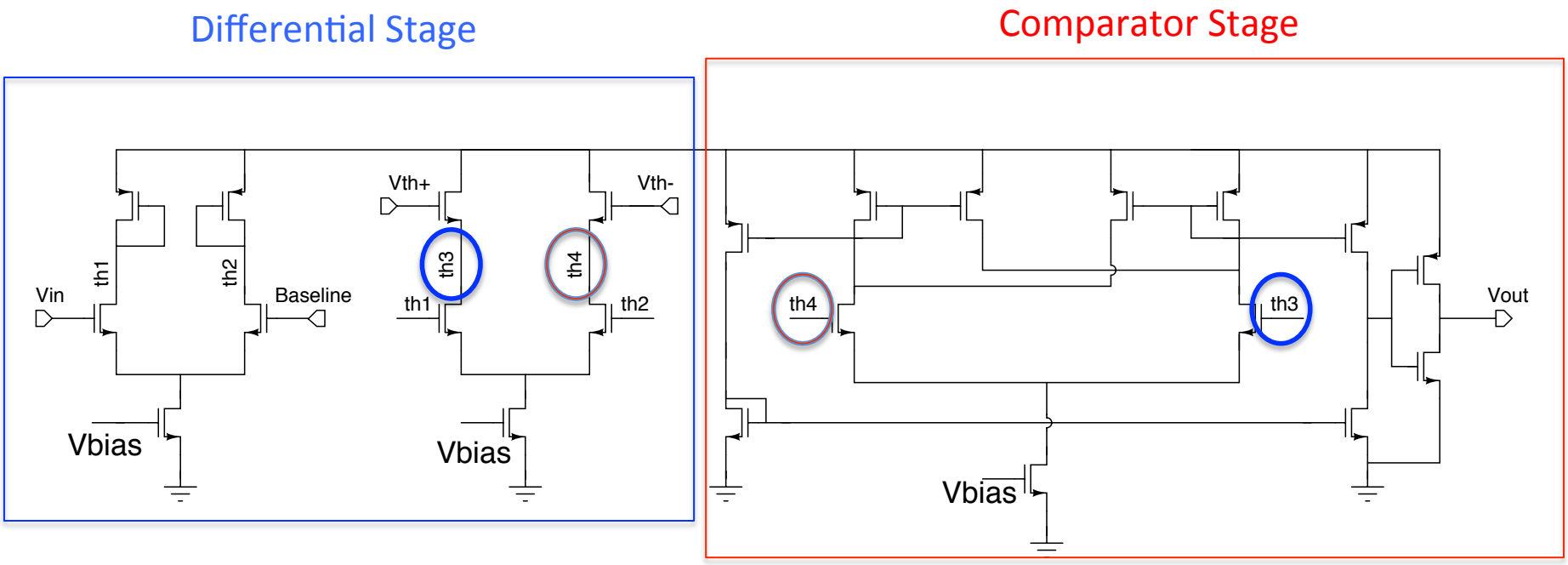
- $i_{M1} = k/(1+k)\, i_{bias}$
- $i_{M2} = 1/(1+k)\, i_{bias}$

Single to Differential Stage



- The first part converts Vin from single ended to differential
- The second part is necessary to set a differential threshold

Complete Hysteresis Comparator



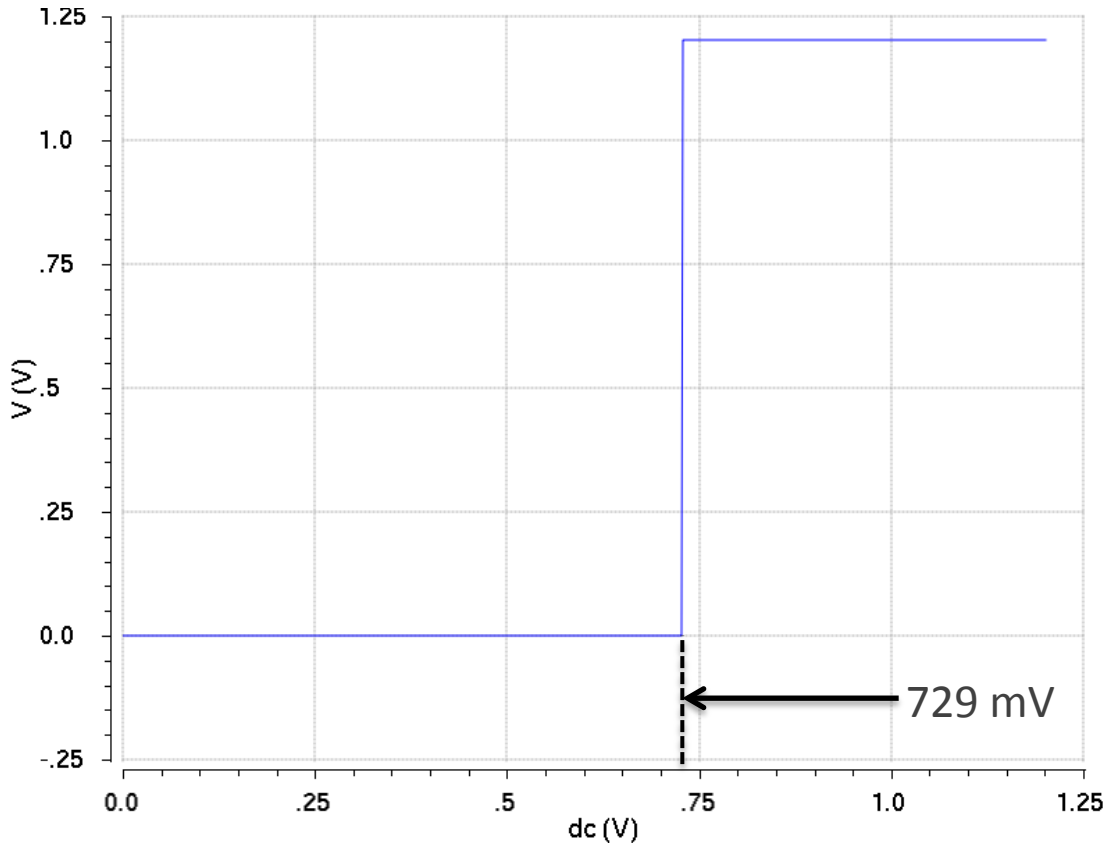
Theoretical Threshold

A = 2.612

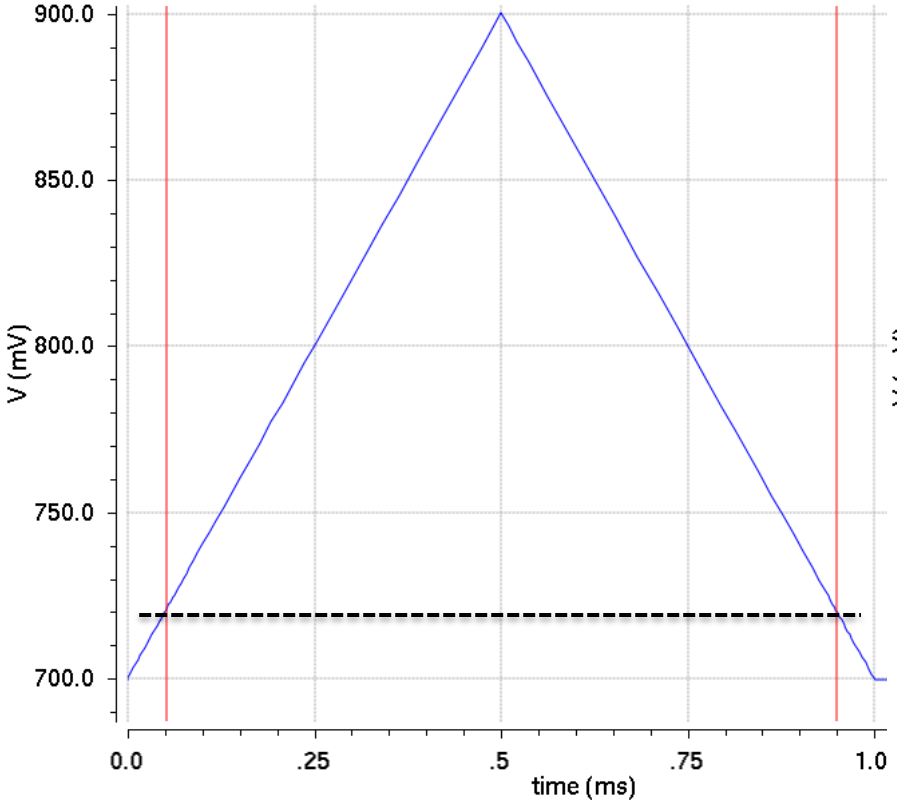
Baseline=700 mV

$(V_{th+}-V_{th-}) = 60$ mV

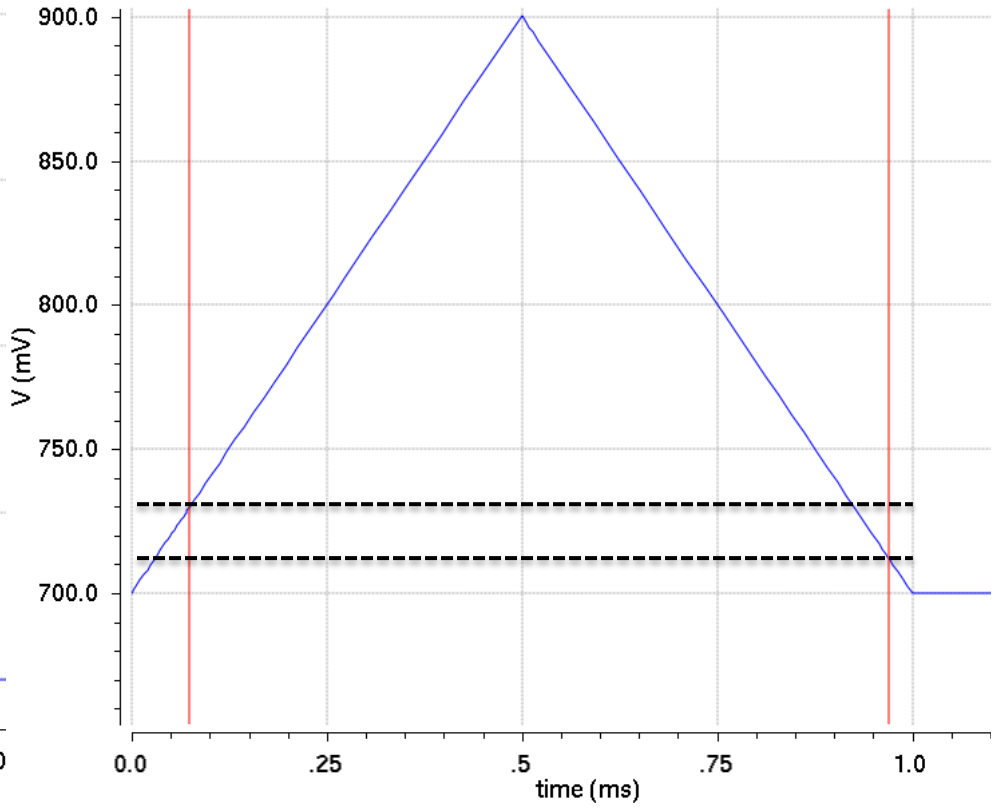
V_{th}= 22.89 mV + Baseline



Hysteresis Comparator II

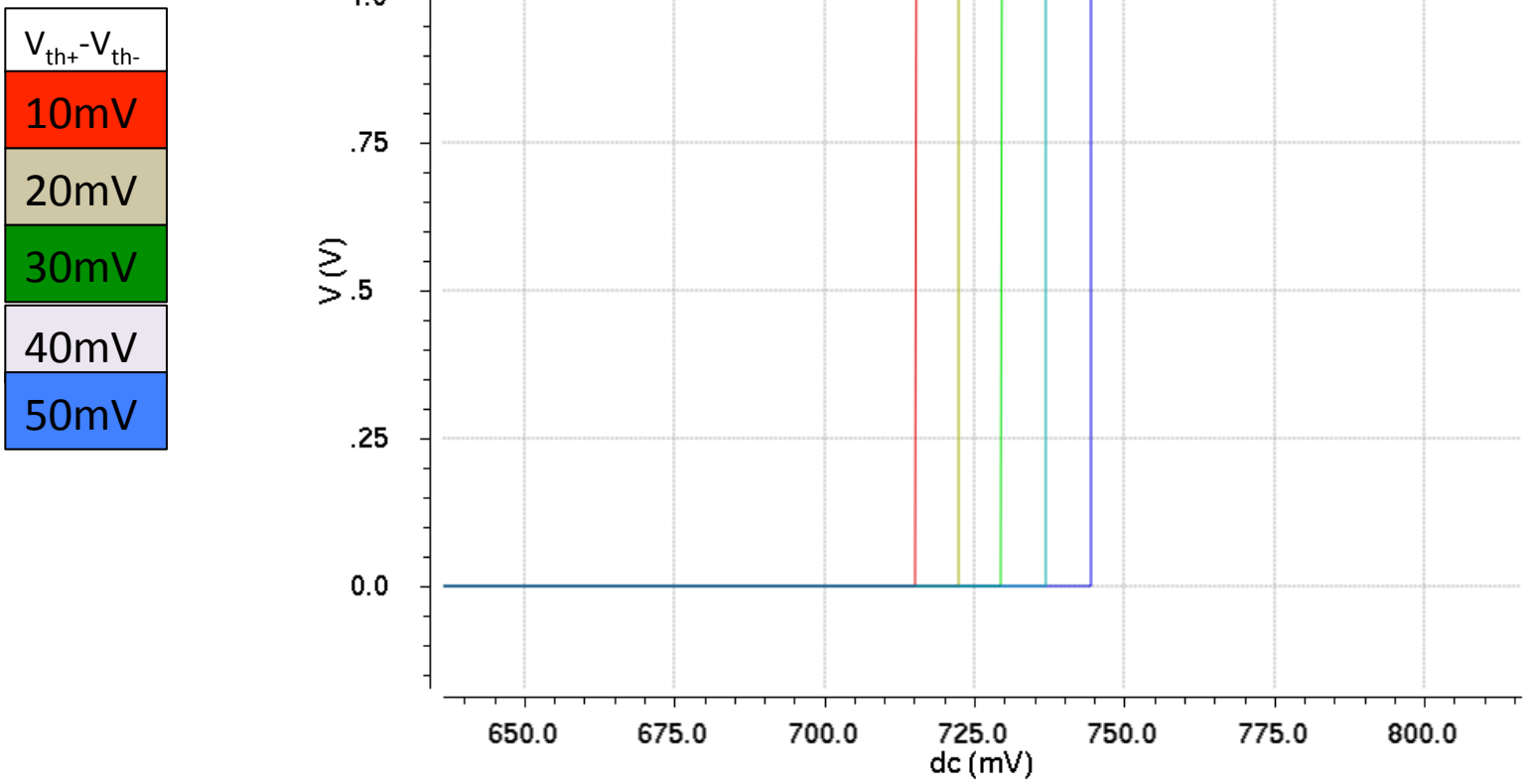


Without Hysteresis



With Hysteresis

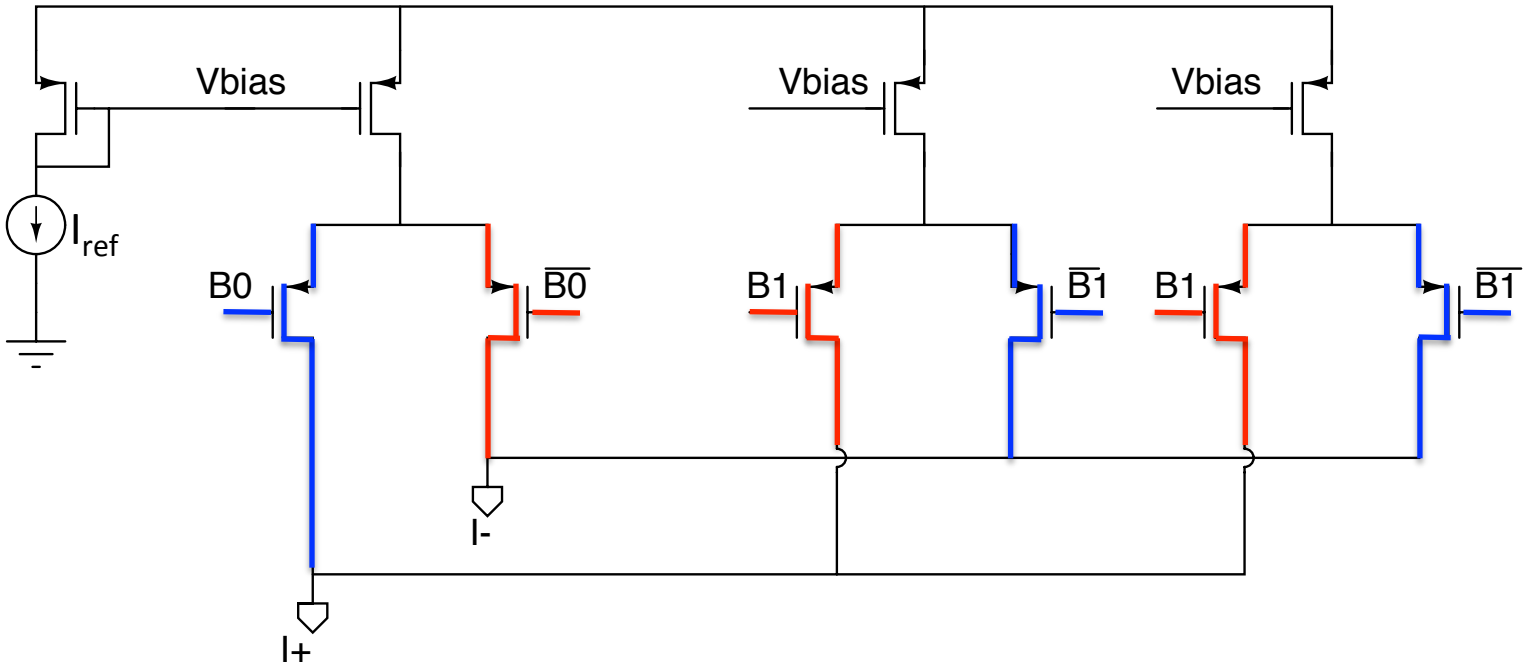
Sweep Threshold



Differential DAC

Standard configuration: 10

B1 B0



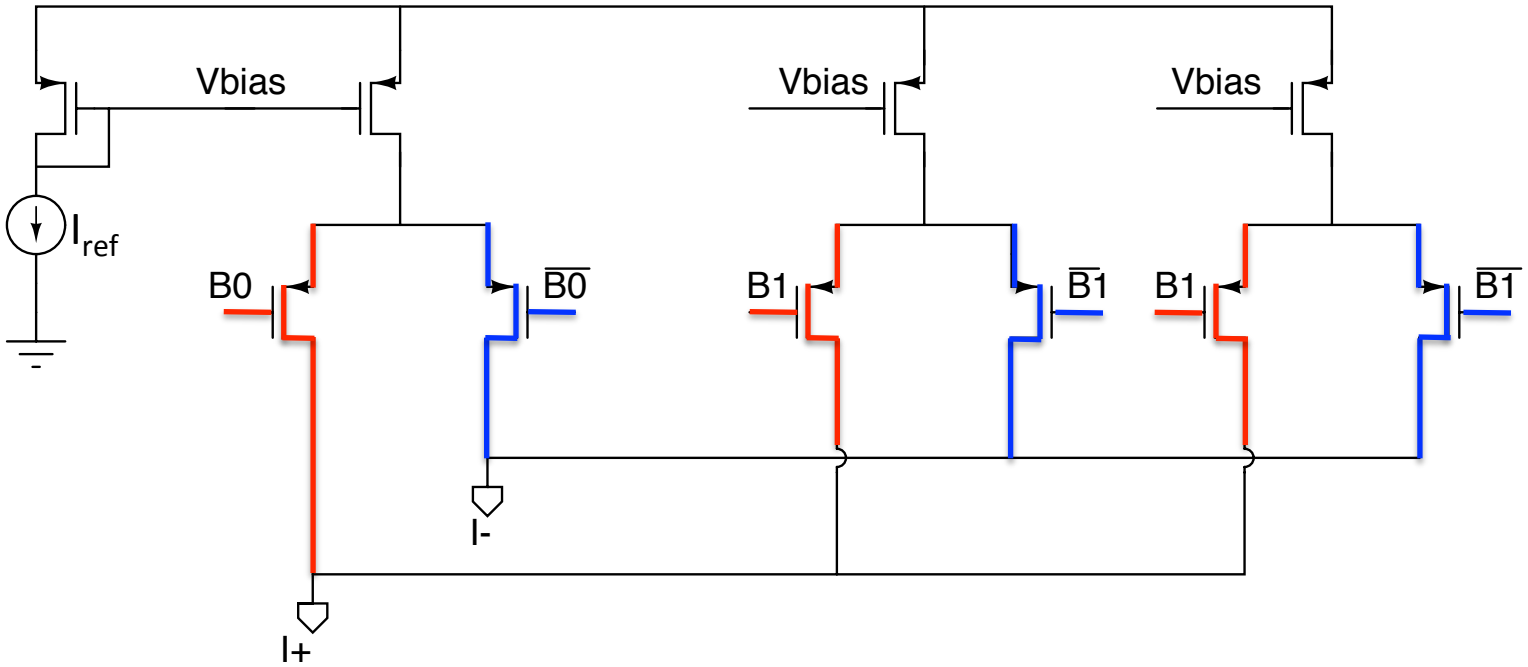
$I_- = 2\ I_{ref}$

$I_+ = 1\ I_{ref}$

Differential DAC

Standard configuration: 11

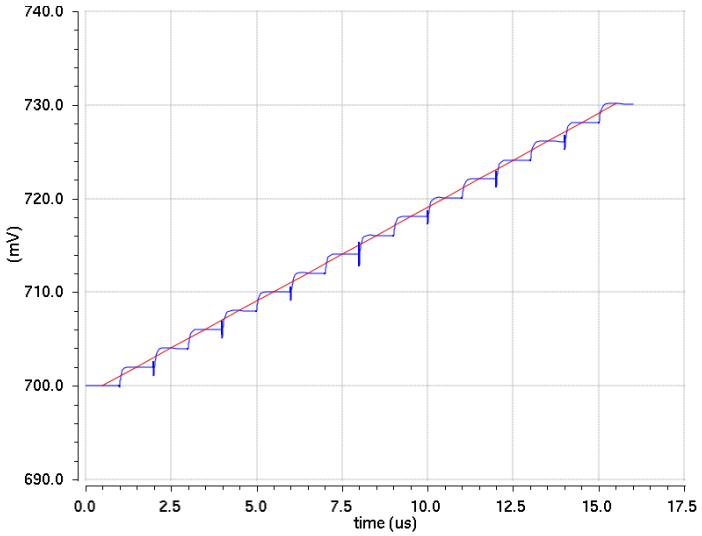
B1 B0

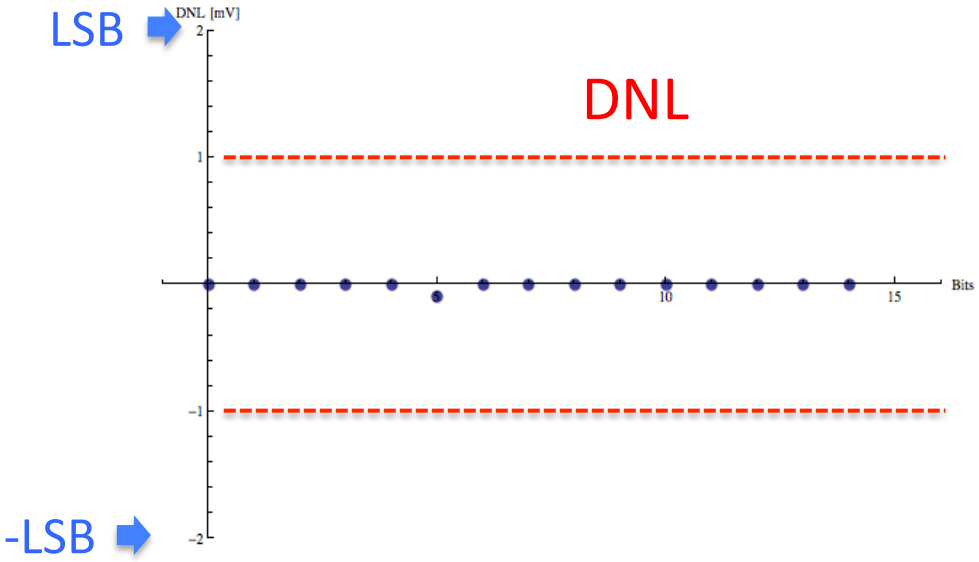


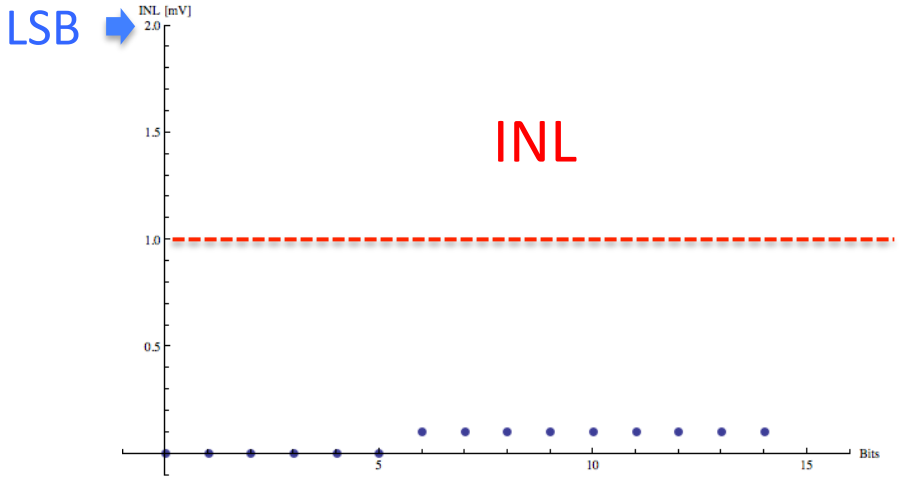
$I_- = 3\ I_{ref}$

$I_+ = 0\ I_{ref}$

Nonlinearity







DNL = differential nonlinearity

INL = integral nonlinearity