

1st Students' Meeting

Something about the Digital Flow

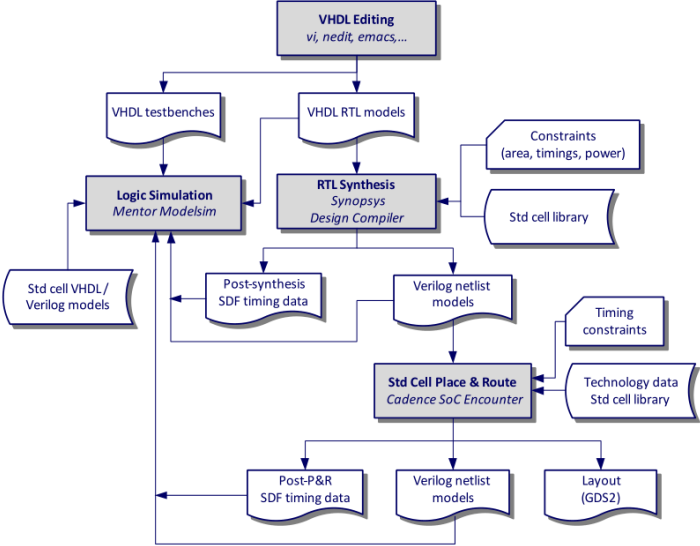
I/II

Serena Panati

Monday, January 20, 2014

- 1 Top-Down Design Flow
- 2 HDL Model
- 3 Register Transfer Level Synthesis
- 4 Post-synthesis logic simulation
- 5 Links and resources
- 6 Next meetings

DF Flowchart



HDL Model

Hardware Description Languages:

- **VHDL** - Std. IEEE 1076-1993

Text editors: gedit, nedit, emacs, vi...

Examples: encoder 8b/10b + non-synthesizable VHDL code ★

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 - ▶ *Gateway Design Automation* was purchased by **Cadence Design Systems** in 1990.

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Pre-synthesis logic simulation

→ Cadence IC 6.1.5 (also IC 6.1.4 is ok)

Tools:

- **NCLaunch** (compiler + elaborator)
- **SimVision** (simulator)

Pre-synthesis logic simulation

The screenshot shows the Cadence NCLaunch application interface. The title bar reads "NCLaunch : /export/elt78xl/disk0/users/panati/projects/shiftregister/syn_shiftre: ...". The menu bar includes "File", "Edit", "Tools", "Utilities", "Plug-Ins", and "Help". The toolbar contains various icons for file operations and simulation. The main window is divided into a file browser on the left and a file tree on the right. The file browser shows the directory structure: "/export/elt78xl/disk0/users/panati/projects/shiftregister/syn_shiftregister/vhdl". The file tree on the right shows a list of directories and files, with "worklib.tb_shiftregister_archi:configuration" selected. The terminal window at the bottom displays the following output:

```
ncvhdll CPU Usage - 0.0s system + 0.0s user = 0.0s total (0.2s, 10.9% cpu)
nclaunch: ncvhdll -work worklib -cdlib /export/elt78xl/disk0/users/panati/projects/shiftregister/syn_shiftregister/netlist_injcds.lib -logfile ncvhdll.log
ncvhdll(64): 10.20-s073: (c) Copyright 1995-2011 Cadence Design Systems, Inc.
ncvhdll_p: Memory Usage - 10.4M program + 13.4M data = 23.8M total
ncvhdll_cg: Memory Usage - 7.6M program + 10.7M data = 18.3M total
ncvhdll: CPU Usage - 0.0s system + 0.0s user = 0.0s total (0.5s, 6.4% cpu)
nclaunch: ncelab -work worklib -cdlib /export/elt78xl/disk0/users/panati/projects/shiftregister/syn_shiftregister/netlist_injcds.lib -logfile ncelab.log
ncelab(64): 10.20-s073: (c) Copyright 1995-2011 Cadence Design Systems, Inc.
ncelab: Memory Usage - 31.7M program + 30.9M data = 62.6M total
ncelab: CPU Usage - 0.0s system + 0.0s user = 0.1s total (0.7s, 10.0% cpu)
nclaunch:
```

At the bottom right of the terminal window, it says "1 items selected".

cds.lib and hdl.var - Examples

- **cds.lib** ★

- **hdl.var** ★

cds.lib and hdl.var - Examples

- **cds.lib** ★
 - ▶ ASCII text file

- **hdl.var** ★

cds.lib and hdl.var - Examples

- **cds.lib** ★
 - ▶ ASCII text file
 - ▶ defines which libraries are accessible and where they are located

- **hdl.var** ★

cds.lib and hdl.var - Examples

- **cds.lib** ★
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 - ▶ defines which libraries are accessible and where they are located
 - ▶ contains statements that map logical library names to their physical directory paths
- **hdl.var** ★

cds.lib and hdl.var - Examples

- **cds.lib** ★
 - ▶ ASCII text file
 - ▶ defines which libraries are accessible and where they are located
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- **hdl.var** ★
 - ▶ optional ASCII text file

cds.lib and hdl.var - Examples

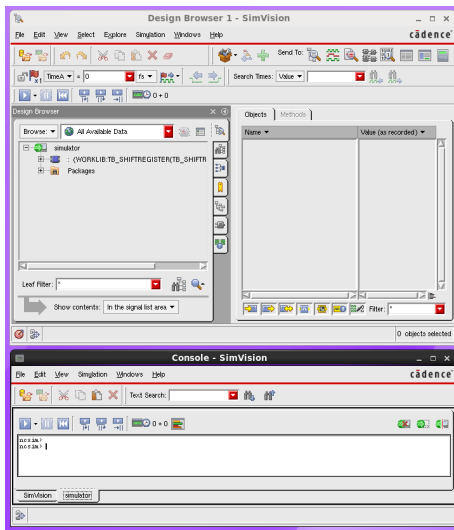
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- ▶ defines which libraries are accessible and where they are located
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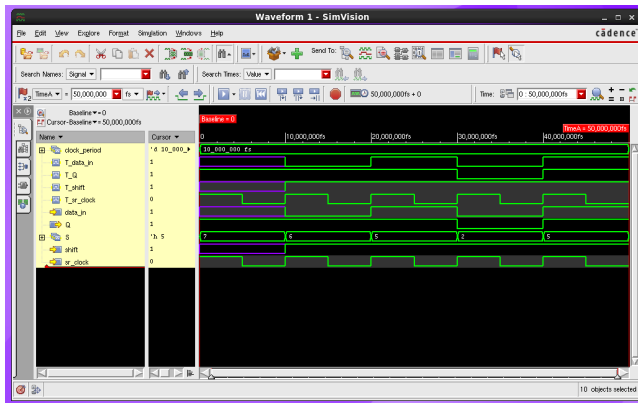
- **hdl.var** ★

- ▶ optional ASCII text file
- ▶ contains definitions for system variables. One of these variables is the WORK variable that specifies the work library in which the compiler stores compiled objects and other derived data.

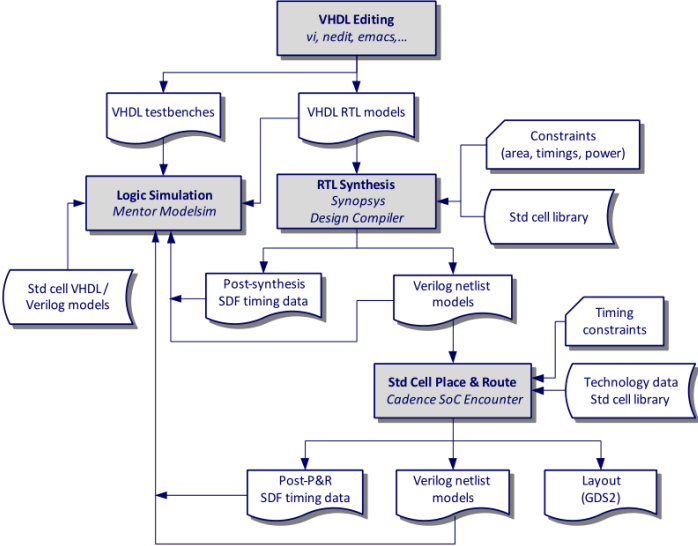
Pre-synthesis logic simulation



Pre-synthesis logic simulation



DF Flowchart



Register Transfer Level Synthesis

→ Cadence EDI 9.12

Tools:

- **Encounter RTL Compiler**

What we need to define:

- timing → .sdc scripts ★

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Register Transfer Level Synthesis

→ Cadence EDI 9.12

Tools:

- **Encounter RTL Compiler**

What we need to define:

- timing → .sdc scripts ★
- constraints (area, power...) → .tcl scripts ★
- process corners libraries (.lib, .lef, .CapTbl) ★

Register Transfer Level Synthesis

LEF: Library Exchange Format (LEF) is a specification for representing the physical layout of an integrated circuit in an ASCII format. It includes design rules and abstract information about the cells. LEF only has the basic information required at that level to serve the purpose of the concerned CAD tool. It helps in saving valuable resources by providing only an abstract view and thus consuming less memory head. LEF is used in conjunction with Design Exchange Format (DEF) to represent the complete physical layout of an integrated circuit while it is being designed. LEF was developed by Cadence Design Systems.[via Wikipedia]

PROCESS CORNERS: In semiconductor manufacturing, a process corner is an example of a design-of-experiments (DoE) technique that refers to a variation of fabrication parameters used in applying an integrated circuit design to a semiconductor wafer. Process corners represent the extremes of these parameter variations within which a circuit that has been etched onto the wafer must function correctly. A circuit running on devices fabricated at these process corners may run slower or faster than specified and at lower or higher temperatures and voltages, but if the circuit does not function at all at any of these process extremes the design is considered to have inadequate design margin. [via Wikipedia]

CAPTABLE: Captable file contains resistance and capacitance values which are used to model the interconnect parasitics of a design. Captable files usually contains resistance value and capacitance values. The capacitance values for a range of width and spacing of each metal used in the corresponding technology are defined. This information is used while extracting the nets.

GATES LIST EXAMPLE check it! ★

Register Transfer Level Synthesis

```
panati@elt56xl:work$
File Edit View Search Terminal Help
[1c] IC 6.1.4
[1d] IC 6.1.4
[2a] RC 8.10
[2b] RC 9.10
[2c] SOC 8.10
[2d] EDI 9.12
[3a] SPB 16.34
[3b] SPB 16.54

2d
Available technologies are :
[1a] AMS 0.35
[1b] AMS 0.35
[2a] IBM 0.13
[2b] IBM 0.13
[4a] UMC 0.11
[5a] Tower/Jazz 0.18

5a
Technology is Tower/Jazz 0.18 um

Execute Global CADENCE Definition EDI version
Release 19 May 2010
[1] 18277
[panati@elt56xl:work]$

panati@elt56xl:work
Warning: Possible timing problems have been detected in the
: The design is 'shiftregister'.
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Warning: Output of the LEC run will not be kept in a log file
: Warning: '-logfile' is not specified.
Info: 'Conformal LECO_14SR1' or later builds is recommended
: the use of 'Conformal LECO_14SR1' or later build
Generating a logfile for design 'shiftregister' in file '...'
Warning: Forcing flat compare. (400-222)
: The design hierarchies are too small to qualify for
: d according to hier compare.
Warning: Possible timing problems have been detected in the
: The design is 'shiftregister'.
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: The design is 'shiftregister'.
Info: Time taken to report power. [RP1-7]
: 0 cpu seconds
Info: Nothing to report. [RP1-22]
: No unpowered isolation instances found in design 'shiftregister'.
: There is no more help available in this message, if the help in this message was invoked
: with this message ID.
EC INFO: End at: 09/05/13 15:11:07
EC INFO: Elapsed-time: 10 seconds

panati@elt56xl:work$
```

The screenshot shows the Cadence Encounter RTL Compiler interface. The main window displays a schematic diagram of a shiftregister design. The design consists of three DFF (Data Flip-Flop) blocks connected in a chain. The first DFF has two data inputs, one of which is connected to a multiplexer. The multiplexer has two data inputs and one select input. The output of the multiplexer is connected to the D input of the first DFF. The output of the first DFF is connected to the D input of the second DFF, and so on. The design is named 'shiftregister' and is located in the file 'App_RC_C1_XXXA_S011'. The terminal window shows the execution of the Global CADENCE Definition EDI version, which includes several warnings about timing problems and a final message indicating that the design is trapped.

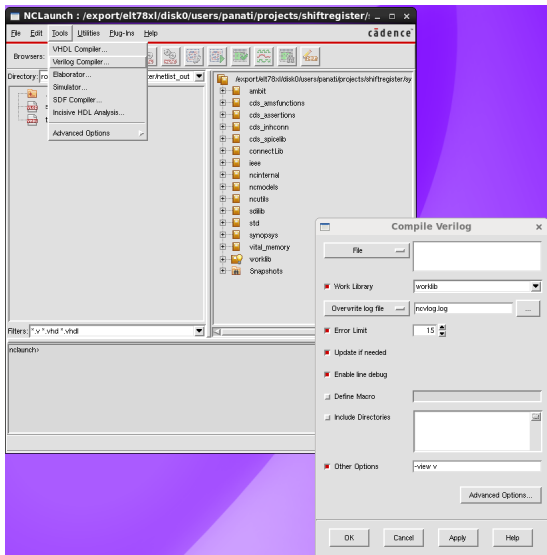
Post-synthesis logic simulation

Tools:

- **NCLaunch** (compiler + elaborator)
- **SimVision** (simulator)

→ Synthesis output: **Verilog!** Some trouble with the VHDL test bench...

Post-synthesis logic simulation



Post-synthesis logic simulation

The screenshot displays the Cadence NCLaunch interface. The main window shows a file browser with a directory tree containing 'shiftregister.v' and 'tb_shiftregister.vhd'. Below the browser, a status bar shows system information: 'indianhu: noclabs@4: 10.20-4073: (c) Copyright 1995-2011 Cadence Design Systems, Inc. Received design and top_level_HDL_AUTO_shift_0 (0x) x ? : 0 : 0'. The 'Elaborator Advanced Options' dialog is open, showing settings for VHDL and Verilog. The 'Elaborate' dialog is also open, showing 'Design Unit' as '(to_3el[view])', 'Work Library' as 'worklib', and 'Error Limit' as '15'. The 'Elaborate' dialog also shows 'Access Visibility' as 'All' and 'Other Options' as '-timescale 1ns/1ns -overrida_timescale'. The 'Elaborate' dialog has buttons for 'OK', 'Cancel', 'Apply', and 'Help'.

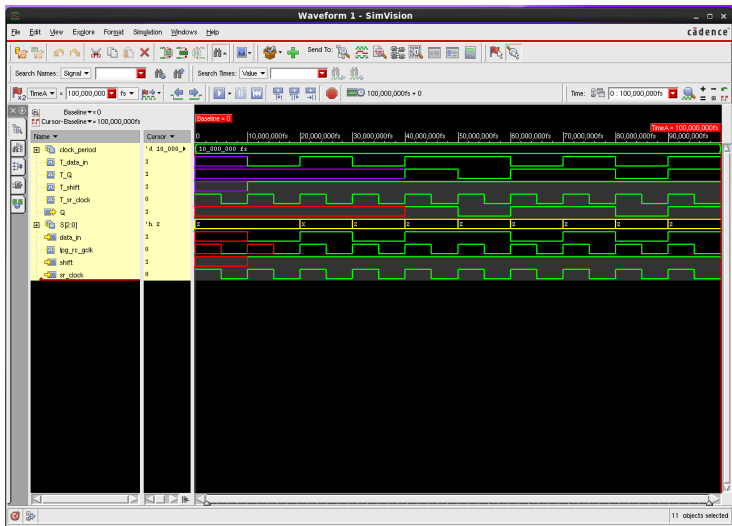
Elaborator Advanced Options

- VHDL Performance
- Verilog Performance
- Comprehensive Coverage
- Timing
- Programming Language Interface
- Annotation
- Configuration File
- Errors and Messages
- General

Elaborate

- Design Unit: (to_3el[view])
- Snapshot Name: []
- Work Library: worklib
- Overwrite log file: noelab.log
- Error Limit: 15
- Update if needed: []
- Access Visibility: All
- Executable Filenames: []
- Other Options: -timescale 1ns/1ns -overrida_timescale

Post-synthesis logic simulation



Links and resources

- Top Down Digital Flow Tutorial:
<http://lsm.epfl.ch/files/content/sites/lsm/files/shared/Resources%20documents/TopdownDF.pdf>
- Cadence Tools Overview (not only digital...):
http://www.phys.hawaii.edu/~varner/PHYS476_Spr10/Lectures/CadenceTools.pdf
- Cadence NCLaunch Tutorial:
<http://www.ee.virginia.edu/~mrs8n/soc/nlaunchtut.pdf>

Next meetings

- Automatic place and route (PnR)

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- Simulation post-PnR

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- Automatic place and route (PnR)
- Simulation post-PnR
- GDS II → Virtuoso

Thank you all, guys...

