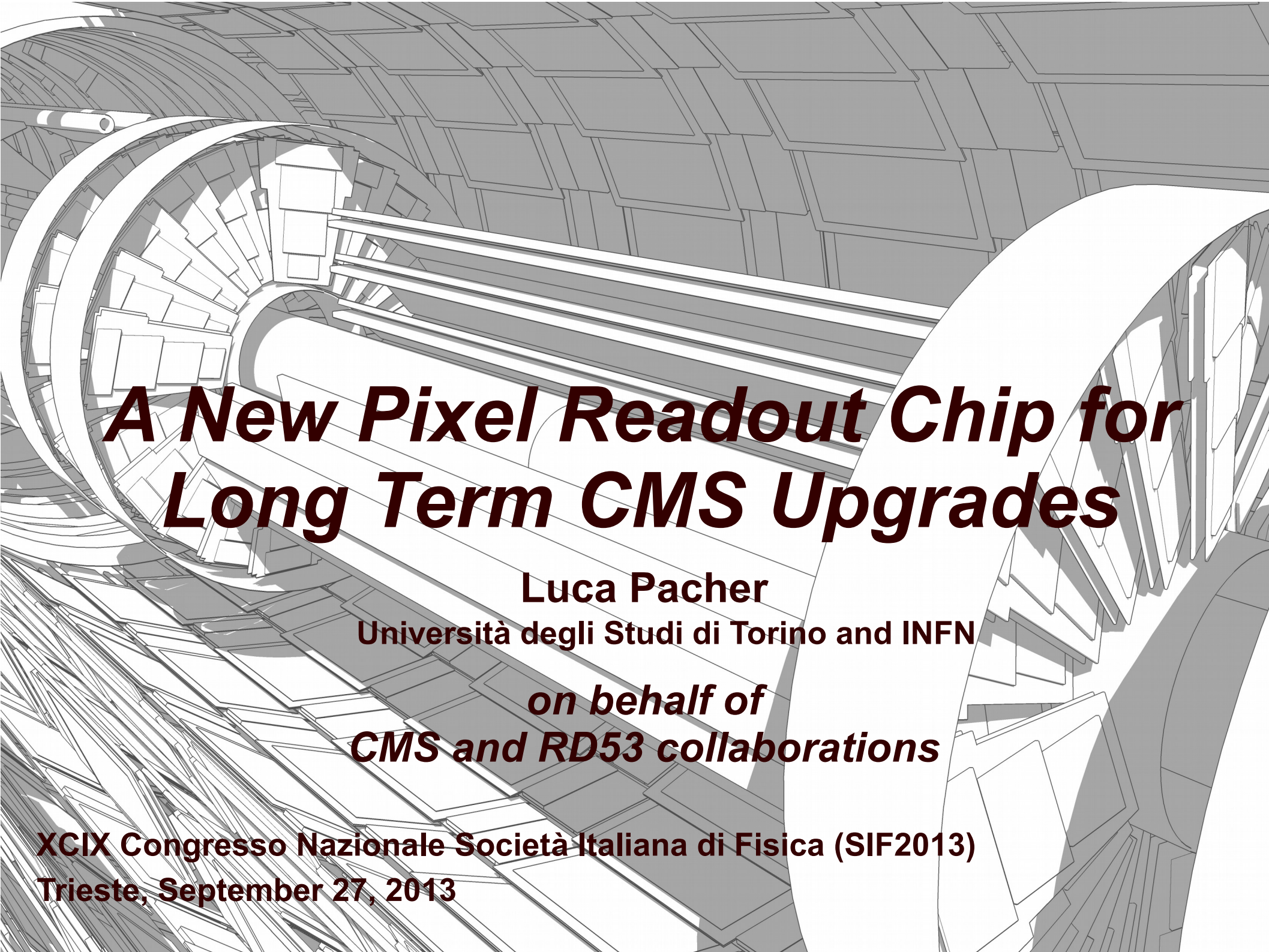

A New Pixel Readout Chip for Long Term CMS Upgrades

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on behalf of
CMS and RD53 collaborations

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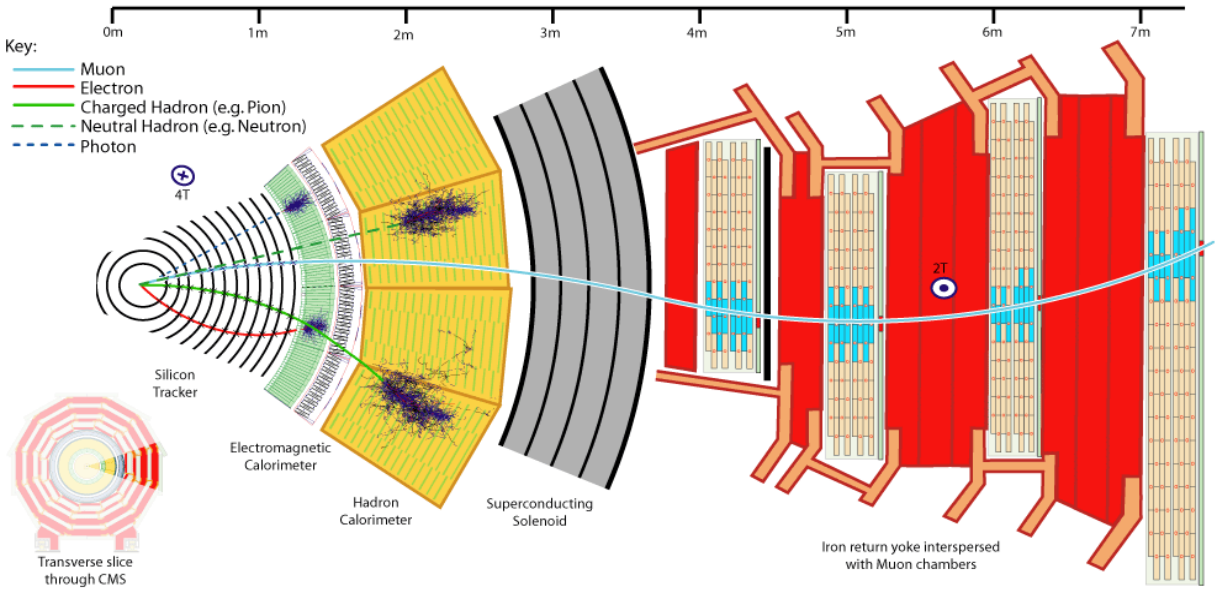
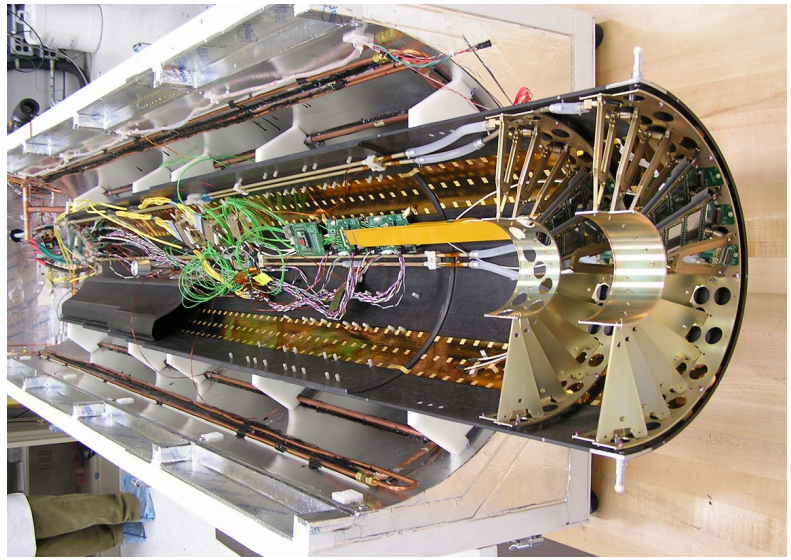
Outline

- Background and motivations
- CMS pixel detector upgrade plans
- New ROC requirements
- Analog design considerations
- First exercises in 65nm
- Summary and outlook

CMS Silicon Pixel Detector



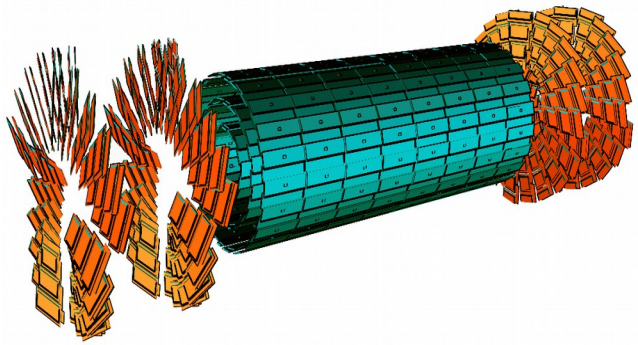


Current CMS silicon pixel detector layout:

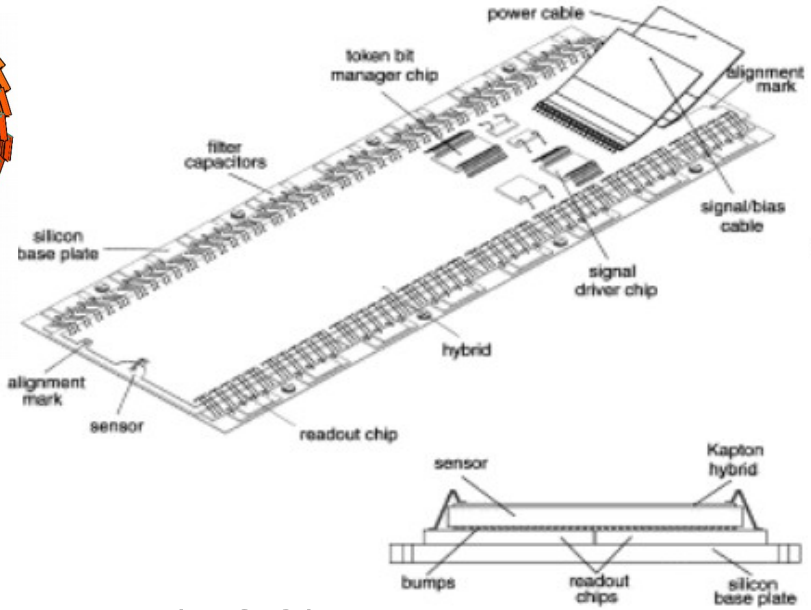
- 3 barrel layers (BPIX) + 2 disks each side (FPIX)
- R = 4.4 cm, 7.3 cm and 10.2 cm, $|\eta| < 2.5$, ~ 1 m^2, 66 Mpixels
- **3 hits track seeding** → IP resolution and SV reconstruction

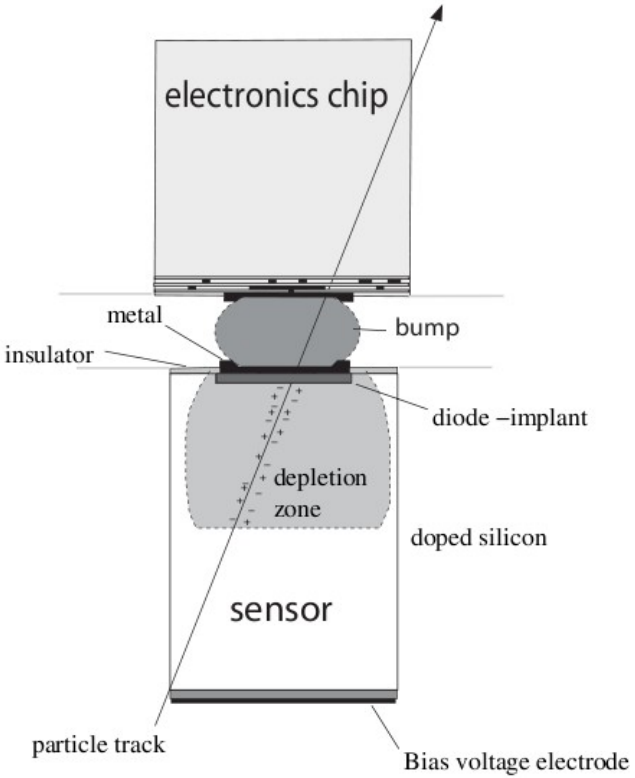
Pixel Readout Chip (ROC)

BPIX/FPIX → module → readout chip (ROC) → pixel unit cell (PUC)



8 or 16 ROCs/module
52 x 80 pixels/ROC

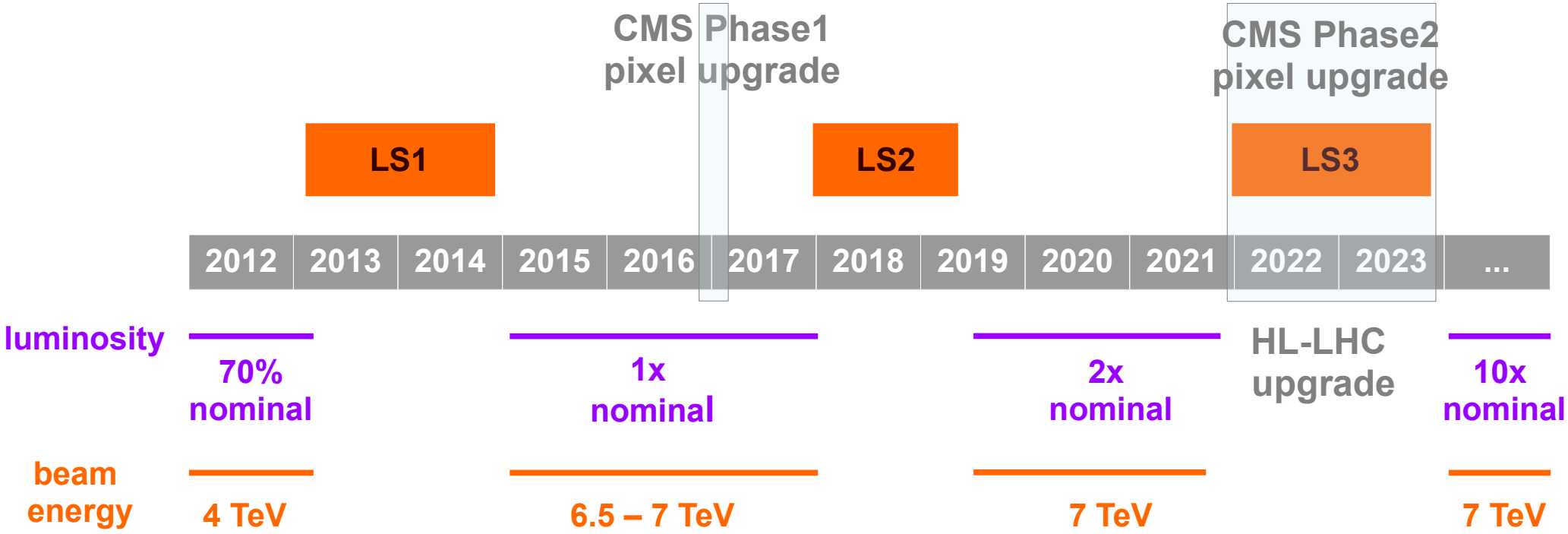




Current CMS pixel readout chip (ROC):

- usage of **hybrid pixel detectors** (***bump-bonding*** technique)
- n^+- on-n planar silicon sensors, 100μm x 150μm pixel size
- each ROC is a **full-custom ASIC** (PSI46 chip, 0.25μm CMOS)

LHC timeline



- LHC activity: **Phase0** → **Phase1** (after LS2) → **Phase2** (after LS3)
- **nominal** luminosity → 10^{34} cm^{-2} s^{-1}, 23 fb^{-1}/year in 2012
- HL-LHC upgrade → 10^{35} cm^{-2} s^{-1}, 300fb^{-1}/year, foreseen 3000 fb^{-1} in 10 years
  - unprecedented **Pile-Up (PU) conditions**
  - unprecedented **radiation levels**

Phase2 Pixel Upgrade: motivations

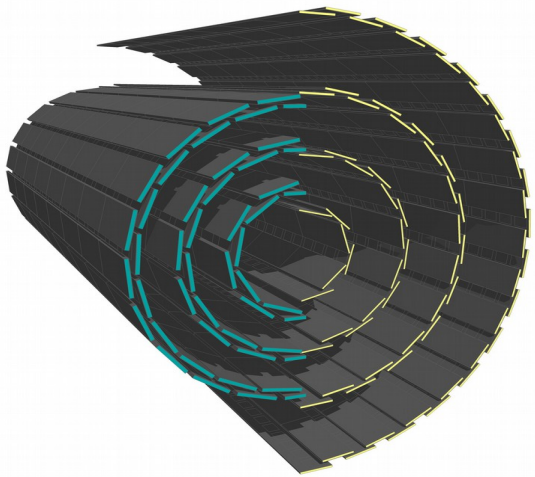
Parameter	LHC Phase0	LHC Phase1	LHC Phase2
PU	~20	~50	140 or higher
particle flux	50 MHz/cm^2	200 MHz/cm^2	500 MHz/cm^2
pixel flux	200 MHz/cm^2	600 MHz/cm^2	1-2 GHz/cm^2
TID (10 years)	1.5 MGy	3.5 MGy	10 MGy
signal threshold	2.5-3 ke	1.5-2 ke	1 ke or below
L1 trigger latency	2-3 μs	4-6 μs	6-20 μs

- **HL-LHC upgrade** will introduce unprecedented operating conditions
- we want to maintain or improve **tracking performance** in terms of:
  - spatial resolution and tracks separation → reduce the **pixel size**
  - hit efficiency > 99.9% → reduce the **data loss** due to readout electronics

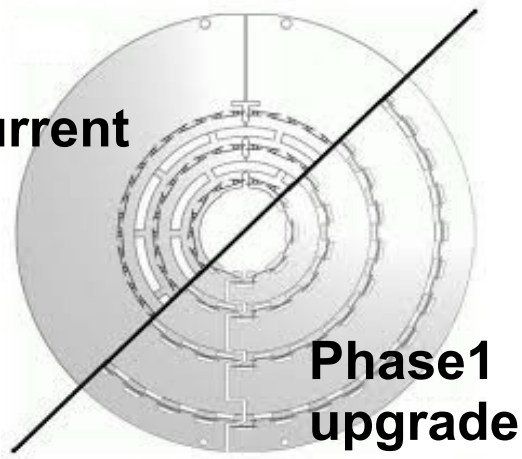
→ ***design of a new pixel readout chip required !***

Phase2 Pixel Detector

- CMS **Phase1** pixel detector upgrade (end of 2016)
  - BPIX: 3 → 4 layers
  - FPIX: 2 → 4 disks
  - pixel ASIC (ROC): PSI46 → PSI46DIG



- CMS **Phase2** pixel detector upgrade (~2022)
  - **geometry** similar to Phase1 (4 barrel layers)
  - possible extension in the disk part
  - improvement in **granularity** → reduced **pixel size**
  - **new pixel ASIC** !
  - ongoing detector simulations



- **sensor choice** not yet finalized
  - very likely **planar sensors** in the outer layers 3 and 4
  - ongoing RD studies for layers 1 and 2
  - very thin **planar sensors**? **3D sensors**? **diamonds**?
  - sensors simulation and qualification required

New pixel ASIC requirements

- smaller **pixel area**
  - 100μm x 150μm Phase0 → **50μm x 100μm** or **25μm x 100μm** Phase2
  - to be determined from simulations (e.g. IP resolution vs. PU)
- **thinner silicon sensors** to increase radiation tolerance
  - 280μm Phase0 → assume **~100μm** thickness (1MIP ~10ke) for Phase2
  - **~1000e minimum detectable charge** (signal threshold)
- increased **pixel rates** (assume 2GHz/cm^2 particle flux)
  - 10kHz/pixel Phase0 → **100kHz/pixel** with 50μm x 100μm pixels or **50kHz/pixel** with 25μm x 100μm pixels
- electronics requirements:
  - speed, low-noise, **low-threshold**, low-power consumption, rad. tolerance
  - more on-chip intelligence and local data storage capabilities
  - **sensor-independent** front-end electronics

IC technology choice

- new ROC requirements led to the choice of a commercial ***CMOS 65nm process*** as the present favored IC fabrication technology
  - present LHC experiments based on **CMOS 250nm**
  - Phase1 LHC experiments upgrades will exploit also **CMOS 130nm** (e.g. **FE-I4** chip for the ATLAS IBL)

- why 65nm ?
  - demonstrated to be **radiation tolerant** up to 2 MGy, better than 130nm (to be confirmed up to 10 MGy)
  - higher integration density, improved speed, low power (1.2 V supply)
  - mature technology (introduced ~10 years ago, LTS and availability)

New community on 65nm: RD53

- similar requirements (and uncertainties) between ATLAS/CMS experiments Phase2 pixel upgrades
  - joint ATLAS/CMS collaboration for sharing efforts in technology qualification
  - collaboration extended to other groups interested in designing in 65nm
- new **RD collaboration proposal** for the development of pixel ASICs in 65nm technology presented to the last LHCC in June
- project now approved and officially supported by CERN as ***RD53***
- 17 institutes involved
  - about 100 collaborators, 50% ASIC designers !
  - very strong **Italian component** from INFN institutes (Bari, Bergamo/Pavia, Padova, Perugia, Pisa and Torino)

Analog brainstorming...

- **Front-End electronics** is of primary importance in pixel detector ASICs
  - Torino INFN **IC designers** started working with 65nm
- **analog design** more challenging in CMOS 65nm
  - ref. to A. Rivetti SIF presentation, ***Front-End electronics for radiation sensors in ultra-deep submicron CMOS technologies***
- move as much as possible the signal processing in the **digital domain**, exploiting speed and higher densities offered by a 65nm CMOS technology
  - keep analog parts to the bare-minimum
  - a few analog blocks ***'embedded'*** in a fully-digital environment
- ***4-5 bit charge encoding*** vs. ***binary readout***
  - do we really need charge information from pixels?
- try to explore innovative (yet simple) solutions for the analog part
  - what about a ***synchronous front-end*** ?
  - local/regional **SAR ADC** vs. **ToT** charge measurements

Specs review

Parameter or Feature		ATLAS	CMS
Hit rates and radiation			
Interactions /25 ns		200 (140 w/leveling)	
Particle flux inner barrel		<500 MHz/cm^2	
Pixel hit rate inner barrel		≈ 1 GHz/cm^2 (30 KHz/pixel 25×150 μm^2)	≈ 2 GHz/cm^2 (50 KHz/pixel 25×100 μm^2) (100 KHz/pixel 50×100 μm^2)
10yr, 3 ab^{-1}	TID	10 MGy	
	1 MeV n. eq.	2×10^{16}	
SEU tolerance		Re-configure <1 module/lyr/hr <0.1% hit data loss	
Sensor			
Signal	Polarity	negative	negative (TBC)
	MIP charge	10 Ke$^-$	5-10 Ke$^-$
	Max. charge	TBD	linear up to 2 (4) MIP
Pixel max. capacitance		200 fF (<400 fF)	200 fF TBC
Pixel max. leakage current		20 nA (<100nA)	20 nA TBC
Readout Chip			
Hit loss at max rate		<1%	<1%
Threshold	minimum	≈ 1000 e^-	≈ 1000 e^-
	dispersion (tuned)	< 100 e^-	< 200 e^- (100 e^-)
	variation w/time	< 100 e^-	< 200 e^- (100 e^-)
Min. thr. noise occupancy		< 10^{-6}	< 10^{-6}
Hit time resolution		25 ns	25 ns
Charge measurement		TBD	4-8 bits Resolution to TBD by detector simulations

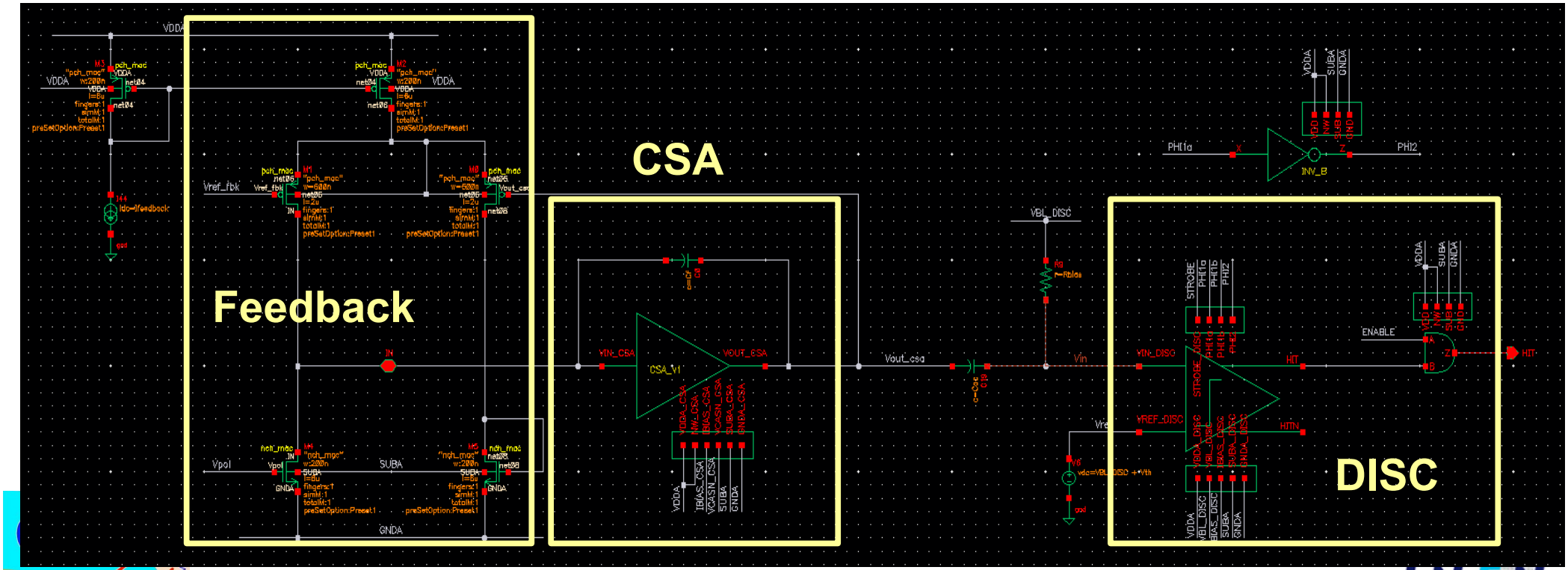
Design inputs:

- 100 fF to 300 fF total input capacitance
- 1000e minimum detectable charge
- < 25ns Hit time resolution
- 100kHz/pixel hit rate

Getting started exercises in 65nm

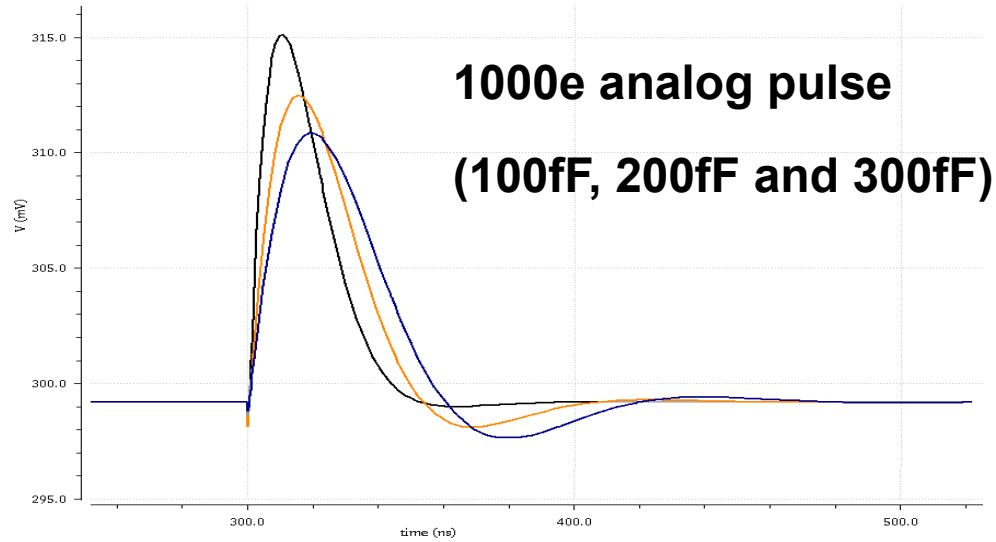
Design of a complete fully-featured ***synchronous binary front-end***

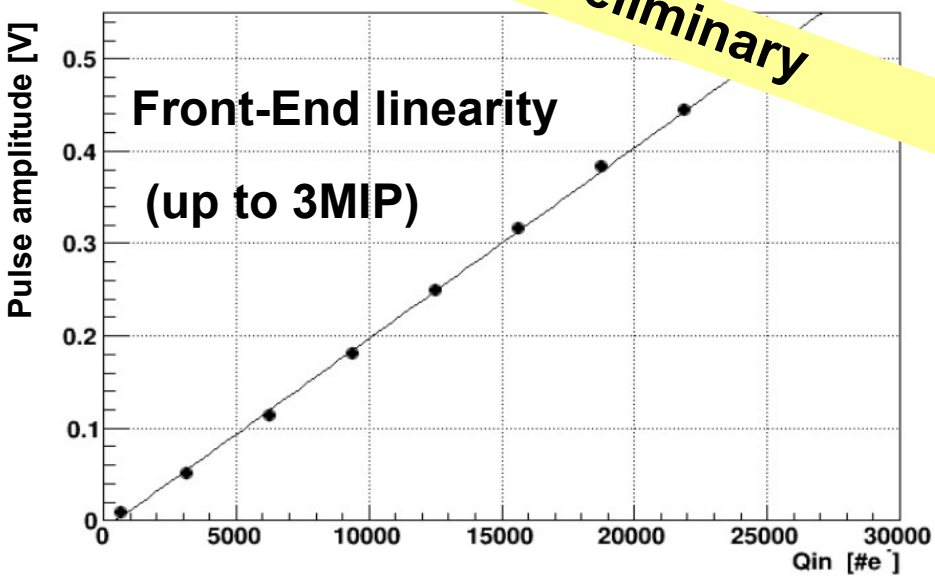
- low-noise CSA with different feedback network architectures
- low-threshold ***discrete-time comparator*** with ***self offset compensation***
- hit generation synchronized with a 25ns (40 MHz) bunch crossing



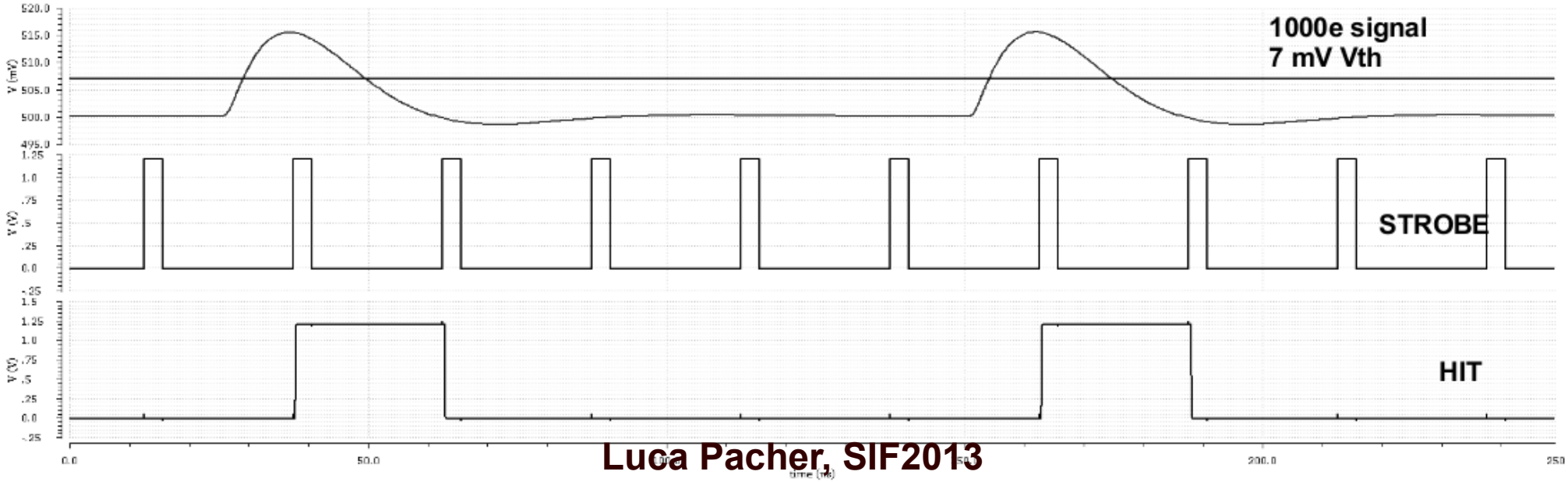
Simulation examples (1)

preliminary

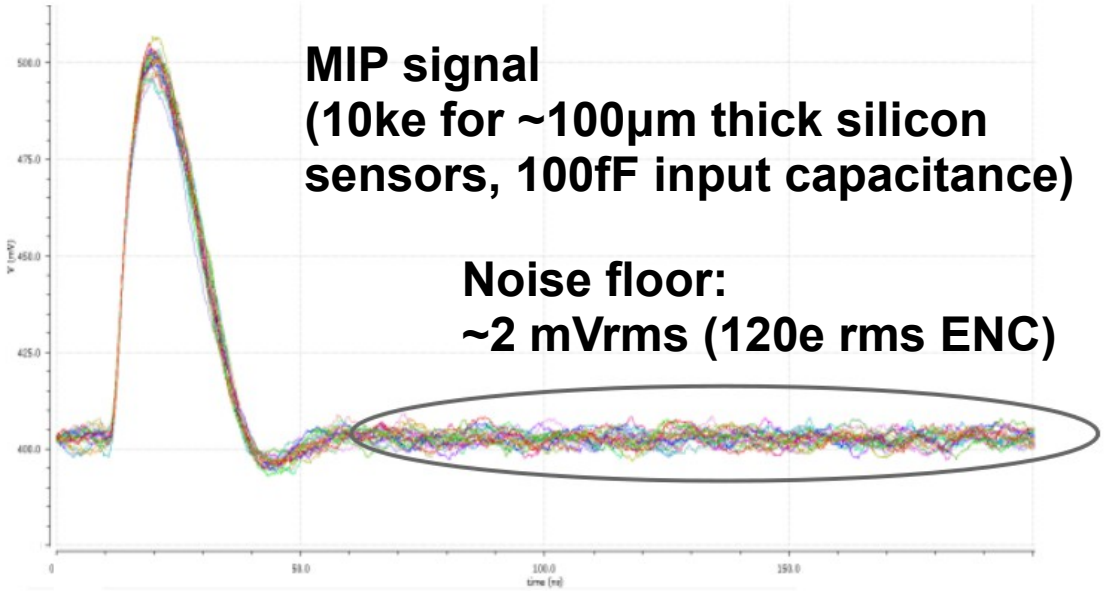




Synchronous discriminator:



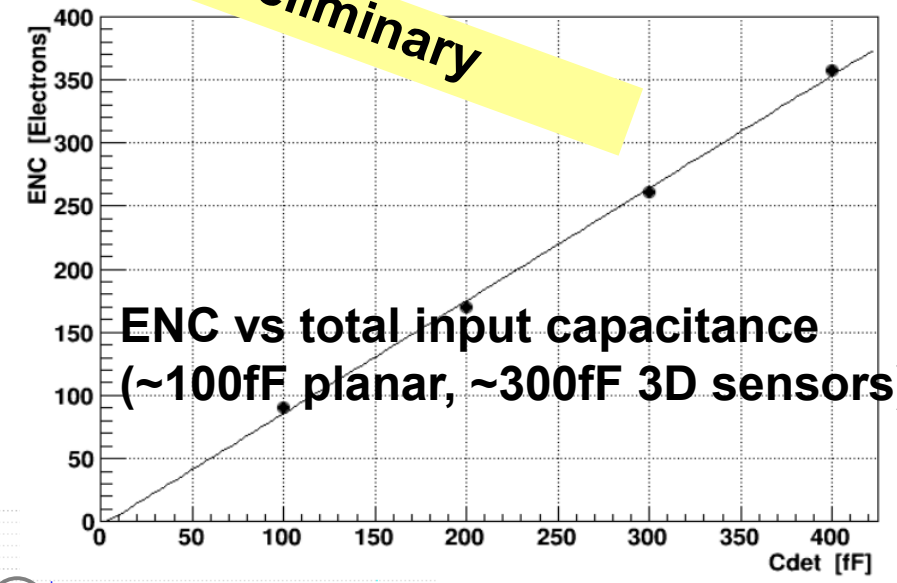
Simulation examples (2)



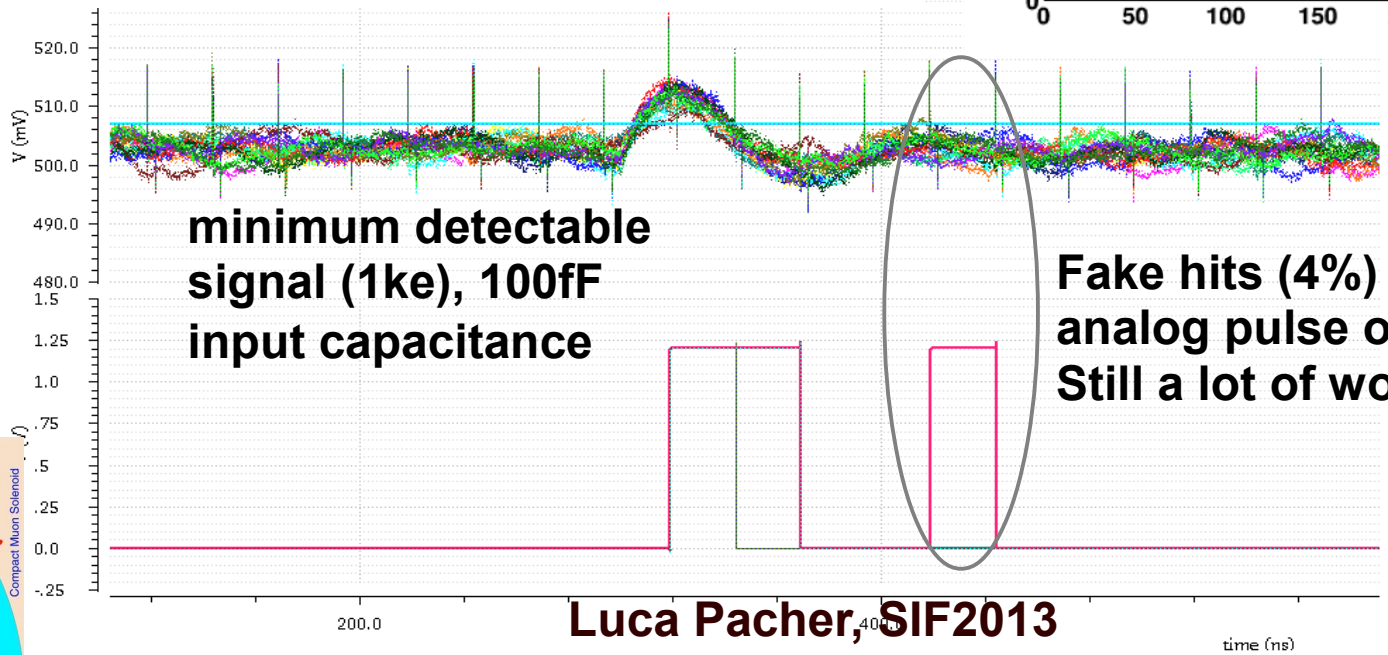
MIP signal
(10ke for ~100μm thick silicon sensors, 100fF input capacitance)

Noise floor:
~2 mVrms (120e rms ENC)

preliminary



ENC vs total input capacitance
(~100fF planar, ~300fF 3D sensors)



minimum detectable signal (1ke), 100fF input capacitance

Fake hits (4%) appear due to analog pulse overshoots !
Still a lot of work to be done...

Conclusions

- HL-LHC upgrade very challenging (PU, radiation levels)
- a new pixel ASIC (ROC) is required for the CMS Phase2 pixel upgrade
- a commercial CMOS 65nm process is the present favored IC fabrication technology for the design of the new readout chip
- 3-year joint ATLAS/CMS collaboration (now RD53) to investigate 65nm technology capabilities
- ongoing preliminary studies in 65nm on different analog front-end architectures are very encouraging
- first test-prototypes expected for ~Spring 2014


Thanks for your attention!

References

- ***RD Collaboration Proposal: Development of Pixel Readout Integrated Circuits for Extreme Rate and Radiation***
  http://cds.cern.ch/record/1553467
- ***Letter of Intent: Development of Pixel Readout Integrated Circuits for Extreme Rate and Radiation***
  http://cds.cern.ch/record/1520875
- ***CMS Technical Design Report for the Pixel Detector Upgrade***
  http://cds.cern.ch/record/1481838
- ***ATLAS and CMS 65nm pixel ASIC meeting***, CERN, Nov 26-27, 2012
  https://indico.cern.ch/conferenceDisplay.py?confId=208595