Low-Power Analog IC Design Course Final Report for ECTS Assignment

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Abstract

This report presents a critical analysis of four different CMOS operational transconductance amplifiers (OTAs). Advantages and drawbacks of each circuit topology with respect to gain, speed, swings, power and noise are discussed. All design considerations are presented for single-ended output amplifiers. Pratical design examples and CAD simulations using a commercial 1.5 V supply voltage 130 nm technology have been included.

Introduction

Operational amplifiers (op-amps) are certainly the most widely used building blocks in analog and mixed-signal systems. According to the standard definition, an op-amp is a high voltage gain differential amplifier with high input impedance and low output impedance. Usually op-amps provide single-ended outputs, but differential outputs can be implemented as well in fully-differential architectures. Thanks to high gain and differential operation, op-amp are mainly employed in closed-loop configuration in feedback networks. The usage of op-amps range from signal amplification and filtering to DC bias generation. Furthermore, high-gain open-loop differential amplifiers can be used as voltage comparators. In the past decades most op-amps were primarily designed to serve as general-purpose analog building blocks. In modern IC design op-amps are typically developed as application-specific circuits indeed, determining at first which are the required specifications and then choosing a circuit topology that favours critical aspects at cost of other performance parameters.

The rest of this report is organized as follows. In the next section, most important design metrics and performance parameters involved in op-amp design are discussed. Four op-amps topologies are then presented: telescopic and folded cascode differential amplifiers, the two-stage Miller compensated OTA and the symmetrical OTA with cascodes. Finally a comparison between the different topologies is given.

Design metrics

A large number of design parameters and specifications contribute to define the overall performance of modern CMOS op-amps [1, 2]. Most of such design parameters trade with each other. As a result, the design activity becomes a multi-dimensional optimization problem, requiring to achieve acceptable compromises between specifications. Further challenges and trade-offs arise as the supply voltage and transistor channel lengths scale down with new generations of CMOS technologies, resulting in much lower available gain per transistor and voltage headrooms.

According to the feedback theory, the primary requirement for an op-amp is certainly to have a sufficient large open-loop gain at low frequencies, so that when negative feedback is applied the closed-loop gain is practically independent of the open-loop one. The value of the open-loop gain is therefore determined by the desired precision for the feedback system employing the op-amp. Gains can vary by several orders of magnitude depending on the application. The minimum required open-loop gain is therefore the first design parameters that must be considered. As technologies scale down, the maximum achievable gain per transistor decreases dramatically, requiring the usage of gain enhancement techniques such as current starving, cascoding, gain boosting or positive feedback.

Speed is related to the frequency response of the op-amp. As the frequency of operation increases, the open-loop gain of the amplifier decreases due to capacitances, introducing larger errors in the feedback. A typical frequency response is given as

$$A_{OL}(s) = \frac{A_{OL}(0)}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})\,...} \tag{1}$$

where $A_{OL}(0)$ is the open-loop gain at low frequencies (DC gain) and ω_{p1}, ω_{p2}, etc. are poles of the open-loop transfer function. The transfer function may include zeroes as well, increasing the complexity of the frequency behaviour. The frequency at which the gain starts decreasing represents the bandwidth (BW) of the amplifier and is usually measured as the -3 dB frequency in the Bode plot for the AC gain magnitude. The unity-gain frequency f_u is the frequency at which the magnitude of the voltage gain drops to 0 dB instead. Since op-amps are usually designed to be employed in feedback systems, stability in closed-loop configuration is also of primary importance and requires frequency compensation.

The most important design specification for an amplifier is the product of DC gain and BW indeed, which is called gain-bandwidth product (GBW). For single-pole amplifiers the GBW equals the unity-gain frequency. The GBW can be always expressed as a ratio between a transistor transconductance g_m and either a load capacitance or a compensation capacitance. GBW is therefore a design metric of primary importance.

In order to characterize op-amp performance, a figure-of-merit (FOM) that combines GBW, output load capacitance C_L and power consumption can be defined as [3]

$$FOM = \frac{GBW\ C_L}{I_{bias}} \qquad \left[\frac{\text{MHz pF}}{\text{mA}}\right] \tag{2}$$

where I_{bias} is the total DC bias current flowing in circuit. The figure-of-merit quotes how much GBW can be obtained for a given load capacitance and power consumption. Op-amps with FOM grater than $100 \div 200$ MHz pF/mA are usually good amplifiers. Note that most of modern integrated CMOS op-amps are designed to drive capacitive-only loads. As a result, a unity-gain output stage (buffer) is normally added only when a resistive load needs to be driven. If the load is purely capacitive a buffer is not required and the amplifier is referred to as an Operational Transconductance Amplifier (OTA).

Noise determines the minimum signal level that can processed with adequate quality. In low-noise applications, signal-to-noise ratio (SNR), common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) design constraints are introduced. As a matter of fact, gain, speed, power and noise always trade with each other. For instance, op-amps designed for low-noise applications will be different with respect to op-amps designed for precision techniques.

Further design constraints can be introduced by input common-mode range (ICMR), slew-rate (SR), output swing and linearity requirements. Differential signals double the maximum achievable voltage swing, which is a useful property as core voltages decrease with technology scaling.

Differential inputs in op-amps are usually provided by a PMOS or NMOS differential pair stage. The choice of using PMOS or NMOS input devices is driven by several tradeoffs in terms of gain, speed, common-mode input range and noise [4]. NMOS are faster than PMOS devices due to larger mobilities and offer larger transconductances. On the other hand PMOS transistors exhibit less $1/f$ noise than NMOS counterparts. Hence PMOS input pairs minimizes the output noise due to the flicker component. Furthermore, PMOS pairs have the advantage that body effect can be removed by connecting device sources to the bulk contact, resulting into a better isolation and therefore higher PSRR with respect to V_{DD} ripples. PMOS devices also are characterized by better matching.

Telescopic and folded cascode OTAs

In this section, telescopic and folded cascode differential amplifiers are reviewed.

The schematic of a telescopic cascode OTA with single-ended output is shown in Figure 1. A PMOS input differential pair (M1-M2) with cascode devices (M3-M4) is loaded by a complementary wide-swing cascode current mirror (M5-M8) which provides a single-ended output.

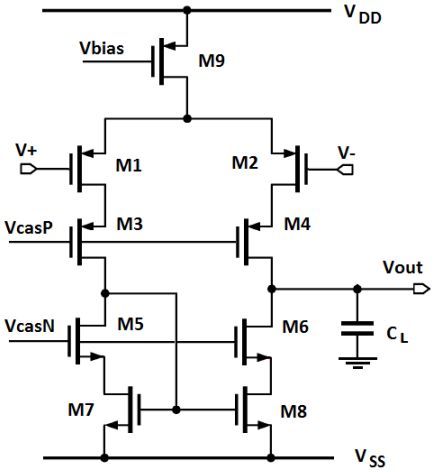

Figure 1: Schematic of a telescopic cascode OTA.

The usage of a wide-swing cascode current mirror is preferable in order to increase headrooms. The circuit requires a single tail bias current (transistor M9), resulting into lower power dissipations. Proper bias voltages Vbias, VcasP and VcasN are generated by using current mirror techniques.

The output node is the only high-impedance node in the circuit, whereas the resistance seen at all the other nodes is of the order of single transistor $1/g_m$. The amplifier is therefore a single-pole system, as expected for any single-stage amplifiers. Since all internal nodes exhibit low impedance, speed is maximized. Moreover, frequency compensation is simply performed by the load capacitance C_L connected to the output, which implements a dominant-pole compensation. Telescopic cascode OTAs are therefore very fast and stable circuits.

The total small-signal resistance seen at the output node is given by the parallel connection $R_{casP}//R_{casN}$ between PMOS and NMOS cascode resistances, where

$$R_{casN} = [1 + (g_{m4} + g_{mb4})r_{ds4}]r_{ds2} + r_{ds4} \tag{3}$$

and

$$R_{casP} = [1 + (g_{m6} + g_{mb6})r_{ds6}]r_{ds8} + r_{ds8} \tag{4}$$

resulting into a high output impedance (up to $\sim$MΩ).

The small-signal gain at low frequencies is determined by the product of input transistor transconductances and the total output resistance,

$$A_V = g_{m1,2}\, R_{casP}//R_{casN} \tag{5}$$

which in turn is proportional to the square of the product of a transistor transconductance and an output resistance,

$$A_V \sim (g_m\, r_{ds})^2 \tag{6}$$

The time constant seen at the output node determines the bandwidth of the amplifier, which is given by

$$BW = \frac{1}{2\pi\ R_{casN}//R_{casP}\ C_L} \tag{7}$$

Hence, the GBW only depends on the input transistor transconductance and the load capacitance,

$$GBW = \frac{g_{m1,2}}{2\pi\, C_L} \tag{8}$$

but not on the output resistance. Cascodes increase the gain at low frequencies but not the GBW, which is limited by the load capacitance.

The maximum current available to charge or discharge the load capacitance is the tail current, hence the slew-rate is given by

$$SR = \frac{I_{tail}}{C_L} \tag{9}$$

Thanks to cascoding, the total input-referred noise is minimized. Cascode devices M3-M6 contribute with negligible noise, leaving input devices M1-M2 and M7-M8 loads as the primary noise sources. As mentioned above, PMOS input devices minimizes $1/f$ noise.

The telescopic cascode OTA is therefore a moderate gain, high speed, low power consumption and low noise amplifier. The main drawback is certainly the limited output swing due to the stack of five transistors between supply rails, making more difficult to use telescopic cascodes in low-voltage applications. Another disadvantage is the difficulty in shorting the output with the inverting input to implement a unity-gain buffer.

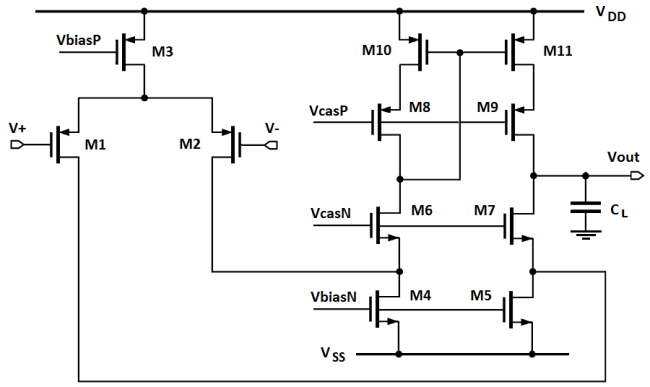

Figure 2: Schematic of a folded cascode OTA.

A popular alternative to the telescopic cascode OTA is the folded cascode topology depicted in Figure 2. In this case input transistors (M1-M2) and cascode devices (M6-M7) are complementary. The differential to single-ended conversion is again obtained by using a wide-swing current mirror load (M8-M11). Input devices are biased with a main tail current (M3) whereas cascode branches require two additional current-source loads (M4-M5). Cascode bias currents I_{6-11} are usually chosen equal to those flowing in the input transistors. Hence this circuit consumes twice the current with respect to a telescopic cascode amplifier, doubling the power consumption.

All considerations related to nodes, output resistance, gain, bandwidth, GBW and slew-rate made for the telescopic cascode OTA apply to the folded one. The output node is the only high-impedance node and the circuit is basically a single-stage amplifier. The voltage gain is generally 2-3 times lower than a telescopic cascode with comparable device sizes and bias currents, while noise slight increases [5]. However, a folded topology offers a few more advantages with respect to the telescopic approach. Due to the usage of opposite-type transistors only four devices are stacked between supply rails, increasing output swings. Furthermore, the single-ended output can be shorted at the same DC bias level of differential inputs. That is, a folded cascode OTA can be used as a unity-gain buffer with negligible swing limitations. Another important advantage is that the input common-mode voltage can include one supply rail (V_{DD} for NMOS input devices and V_{SS} in case of PMOS devices). As a matter of fact, the folded cascode OTA offers medium performance in terms of gain, speed, swing, power and noise.

Design examples

Pratical design examples have been included in this report for each circuit topology. CAD simulations were performed within the Cadence environment using a commercial 1.5 V supply voltage 130 nm CMOS technology. In order to ensure adequate gain, a design length of 0.6 μm $\approx 5L_{min}$ was chosen. The following considerations assume 20 pF load capacitance.

As a first example, a 10 MHz GBW telescopic cascode OTA has been implemented. From GBW and load capacitance specification and using (8) one can derive the input transistors transconductances, $g_{m1,2} \approx 1.2$ mS. Next step in the design procedure consists in the estimation of the bias current. According to the g_m/I_D design methodology [6, 7], one can assume that $g_m/I_D \approx 10$ V^{-1}, which in turn correspond to an overdrive voltages $V_{GS} - V_{TH} \approx$ 200 mV. This value represents an optimum compromise between speed, power consumption and device sizes. Thus, 120 μA drain current must flow in input devices M1-M2, resulting in 240 μA total bias current and 360 μW power consumption for 1.5 V supply voltage. The FOM is therefore 833 MHz pF/mA. Assuming a design length of 0.6 μm the width of input devices can be automatically determined from g_m/I_D parametric simulations as shown in Figure 3.

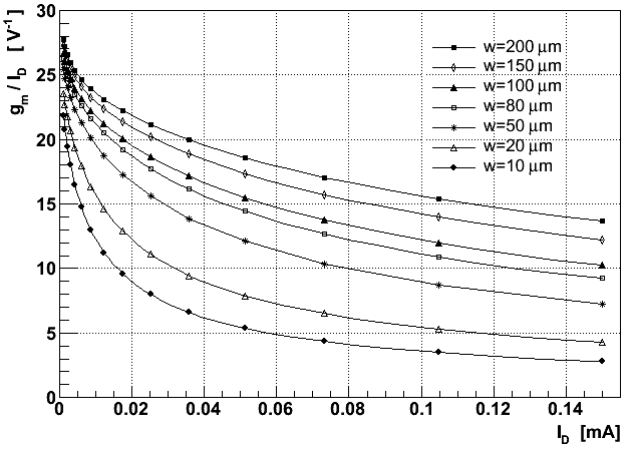

Figure 3: g_m/I_D vs. I_D parametric simulations for a commercial 1.5 V supply voltage 130nm CMOS technology ($L =$ 0.6 μm).

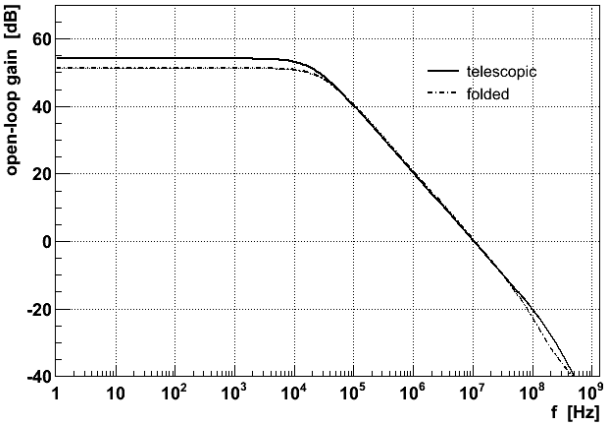

Figure 4: Telescopic and folded cascode OTAs: simulated AC gain magnitude for nominal 20 pF load capacitance and 10 MHz GBW.

As a result, an aspect ratio $(W/L)_{1,2} = 60\ \mu$m/0.6 μm is required to drive 120 μA drain current with 1.2 mS transconductance and about 200 mV overdrive voltage. At the end, cascodes have been sized requiring $\approx$ 200 mV overdrive voltages and adequate drain-source swings for a 700 mV common-mode input voltage. The simulated open-loop gain at low frequencies was 54.2 dB with about 87 degree phase-margin and 10.39 MHz GBW.

The design procedure can be repeated for a folded cascode OTA. For same 10 MHz GBW and 20 pF load capacitance constraints, input device transconductances, bias currents and therefore aspect ratios does not change with respect to telescopic design. The 120 μA bias current flowing in the input transistors have been used also in the cascode branches. NMOS current-source loads aspect ratios have been doubled in order to drive twice the tail current each one, with $(W/L)_{4,5} = 120\ \mu$m/0.6 μm. Of course power dissipation increases, resulting in 480 μA total bias current and about 416 MHz pF/mA FOM. The simulated open-loop gain at low frequency was 51.2 dB with 84 degree phase-margin and 10.9 MHz GBW.

Plots in Figure 4 represent the simulated AC gain magnitudes for the above described telescopic and folded cascode implementations.

Two-stage Miller compensated OTA

Telescopic and folded cascode topologies offer moderate gain with limited voltage headrooms. Two-stage configurations must be adopted in order to fulfil high gain and large swing requirements.

The two-stage Miller compensated OTA shown in Figure 5 is probably the most popular solution. The first stage is a differential pair (M1-M2) with a current mirror load (M3-M4) that converts differential inputs into a single-ended output, which in turn is fed to a second gain stage implemented with a simple common source amplifier (M6-M7).

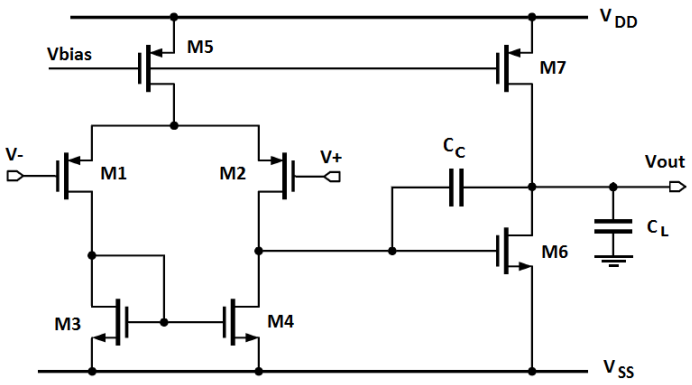

Figure 5: Schematic of a two-stage Miller compensated OTA with PMOS input pair.

As already mentioned, usually PMOS transistors are the best choice for the input stage, resulting in lower $1/f$ noise, larger slew-rate and better matching. Moreover, a PMOS input pair implies a NMOS drive transistor in the second stage, which offers larger trasconductances and therefore higher gain. Note that the usage of a simple common source gain stage maximizes the output swing. The proper DC voltage Vbias is provided by an external current mirror which fixes the required bias currents flowing in the differential pair and in the output branch. A compensation capacitance C_c must be included to ensure stability, as reviewed below.

The open-loop gain at low frequencies is derived from the small-signal model as

$$\begin{aligned} A_V &= (g_{m2}\ r_{ds2}//r_{ds4})\,(g_{m6}\ r_{ds6}//r_{ds7}) \\ &= \left(\frac{g_{m2}}{g_{ds2}+g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6}+g_{ds7}}\right) \end{aligned} \tag{10}$$

being $r_{ds2}//r_{ds4}$ the total resistance seen at the output of the differential pair and $r_{ds6}//r_{ds7}$ the total resistance at the output of the common source stage.

Both differential pair and common source output nodes cause two poles which are close together. Thus, frequency compensation is required to guarantee adequate phase margin and avoid peaking in feedback configurations. Thanks to Miller effect, compensation can be simply performed by adding a capacitor C_c which moves the dominant pole towards low frequencies and the first non-dominant pole

$$f_{nd} \approx \frac{1}{3}\frac{g_{m6}}{2\pi\, C_L} \tag{11}$$

at sufficiently high frequency, beyond the required GBW (pole-splitting). The GBW of the system taking into account the Miller capacitance is given by

$$GBW = \frac{g_{m1}}{2\pi\, C_c} \tag{12}$$

as expected for a generic two-stage amplifier with Miller compensation. Typically C_c is chosen in order to push f_{nd} 2-3 times the required GBW. Unfortunately, the Miller capacitance introduces also a positive zero placed at frequency

$$f_z = \frac{g_{m2}}{2\pi\ C_c} \tag{13}$$

which behaves like a negative pole, degrading the phase margin. Such a zero can lead to instability if it is located close to the new unity-gain frequency, thereby it must be controlled and compensated with specific techniques if necessary.

Design example

Systematic design optimizations and compensation procedures of the two-stage Miller OTA have been extensively discussed in literature [8, 9, 10, 11]. One can recognize that the circuit design is driven by equations (11) and (12). As a result, when a specific GBW is required for a given load capacitance C_L the design requires to solve these equations with g_{m1}, g_{m6} and C_c free variables. A good compromise between stability, speed and power is given by choosing

$$\frac{g_{m6}}{g_{m1}} \approx 4\frac{C_L}{C_c} \tag{14}$$

As a design example, let assume 50 MHz GBW with 20 pF load capacitance. As first guess, one can choose for the value of the compensation capacitance one half the load capacitance, thus $C_c = 10$ pF. From (12) follows that $g_{m1} \approx 3$ mS. At the same time from (11) one can derive a lower limit for the transconductance g_{m6} of the output stage,

$$g_{m6,min} = 2\pi\ C_L\ (3GBW) \tag{15}$$

assuming that Miller compensation will move at high frequencies the first non-dominant pole f_{nd} three times the nominal GBW. Thus 50 MHz GBW leads to $g_{m6,min} \approx$ 18.8 mS. With $g_{m1} = 3$ mS, $g_{m6} = 20$ mS and assuming $g_m/I_D \approx 10\ \mathrm{V}^{-1}$ follows that 20 mA and 300 μA bias currents must flow in the output branch and in the input devices respectively. With these values, $g_{m6}/g_{m1} = 6.6$ and $4\,C_L/C_c = 8$. The final choice has been to decrease C_c at a value of 8 pF in order to satisfy (14), obtaining $g_{m1} = 2.5$ mS and therefore $g_{m6} = 25$ mS, resulting into 250 μA and 2.5 mA bias currents respectively. Devices sizes were then obtained through parametric simulations, $(W/L)_{1,2} = 170$ μm/0.6 μm and $(W/L)_6 = 280$ μm/0.6 μm.

Figure 6 shows the AC gain magnitude for both $C_c = 0$ (uncompensated) and $C_c = 8$ pF (compensated) cases. The open-loop gain at low frequencies was about 60 dB, with 72 degree phase-margin and 54.5 MHz GBW. With a total bias current of 2.75 mA the resulting FOM is about 330 MHz pF/mA and 4.1 mW the power dissipation.

Symmetrical OTA with cascodes

For low-voltage applications, current-mirror amplifiers are the most popular alternatives to the two-stage Miller compensated OTA. In this section, the symmetrical CMOS OTA with cascodes is discussed.

As shown in Figure 7, a current-mirror OTA basically consists of a differential pair (M1-M2) loaded by a couple of current mirrors. Unlike a simple single-ended symmetrical OTA with three current mirrors, cascodes (M6-M13)

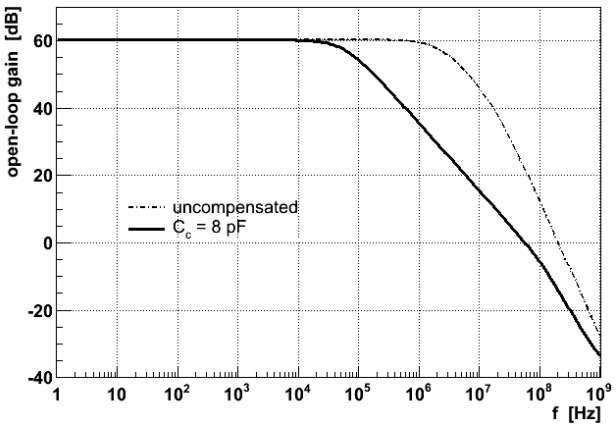

Figure 6: Two-stage Miller compensated OTA: simulated AC gain magnitude for nominal 20 pF load capacitance and 50 MHz GBW before and after compensation.

can be added on both sides to increase the gain. A wide-swing cascode current mirror (M10-M13) is used to provide a single-ended output and preserve voltage headroom. As in telescopic and folded cascode topologies, proper bias voltages Vbias, VcasP and VcasN must be generated with current mirror techniques.

All nodes exhibit low impedance except for the output one, which is the only high-impedance node in the circuit. Despite this is a two-stage amplifier it closely approximates a single-pole system and frequency compensation is performed by the load capacitance connected to the output.

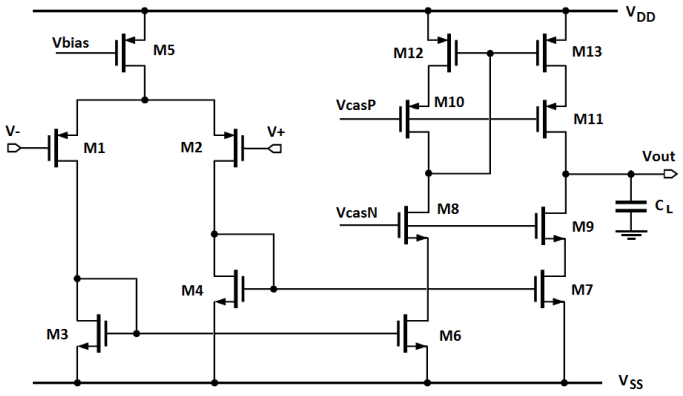

Figure 7: Schematic of a symmetrical OTA with wide-swing cascode current mirror.

The key design parameter in terms of gain, GBW and slew-rate is the current gain (current ratio) B between input and output branches ($I_{6-13} = B\,I_{1-4} = B\,I_{tail}/2$). Since the circuit behaves like a single-stage amplifier the small-signal open-loop gain at low frequencies is determined by the product between the input transistor transconductance and the total resistance seen at the output node. Actually extra gain is provided by the current ratio B, resulting in

$$A_V = B\ g_{m1,2}\,R_{out} = B\ g_{m1,2}\,R_{casN}//R_{casP} \tag{16}$$

where R_{casN} and R_{casP} small-signal resistances are similar to (3) and (4) introduced for telescopic and folded cascode amplifiers. Since all internal nodes introduce non-dominant poles, the bandwidth is only determined by the time constant at the output node $R_{out}\,C_L = R_{casN}//R_{casP}\,C_L$. Hence the GBW is

$$GBW = B\,\frac{g_{m1,2}}{2\pi C_L} \tag{17}$$

The maximum current available to charge or discharge the load capacitance is $B\ I_{tail}$, thus the slew-rate is

$$SR = B\,\frac{I_{tail}}{C_L} \tag{18}$$

From (17) and (18) follows that the main advantages of a current-mirror OTA are GBW and slew-rate, which are increased by the current gain B. Note that with respect to the simple symmetrical OTA, cascoding increases the gain at low frequencies but not the GBW, which in turn is limited by the load capacitance. In order to further increase the gain, regulated cascodes or shunt current sources techniques can be used [12].

The total current flowing in the circuit is $(B+1)\,I_{tail}$, resulting into a larger power dissipation compared to telescopic and folded cascode topologies. Finally, a symmetrical OTA suffers from larger thermal noise due to input transistors biased with a smaller fraction of the total bias current, resulting into smaller transconductances.

Design example

A pratical implementation of a symmetrical OTA with cascodes is now described. Let assume 50 MHz GBW as in the two-stage Miller OTA, with 20 pF load capacitance. The free design parameter is the current ratio B. Usually B values are chosen between 2 and 5. Here $B = 5$ was chosen. Thus the value of input transistor transconductances is immediately derived from (17), $g_{m1} \approx 1.2$ mS, which in turn requires 120 μA bias current flowing in the input devices and $(W/L)_{1,2} = 60\ \mu$m/0.6 μm under the $g_m/I_D \approx 10$ V^{-1} basic assumption. Note that these values are the same obtained for telescopic and folded cascode input stages. The bias current mirrored into each cascode branch is 600 μA and the aspect ratios of the NMOS current-source loads must be 5 times larger. At the end, PMOS cascode aspect ratios and biases can be optimized to ensure adequate overdrives and drain-source swings.

The simulated open-loop AC gain magnitude is shown in Figure 8. The gain at low frequencies was 57 dB with 63.4 phase-margin. With 1.44 mA total bias current the resulting FOM is 694 MHz pF/mA, whereas power consumption is 2.16 mW under 1.5 V supply voltage.

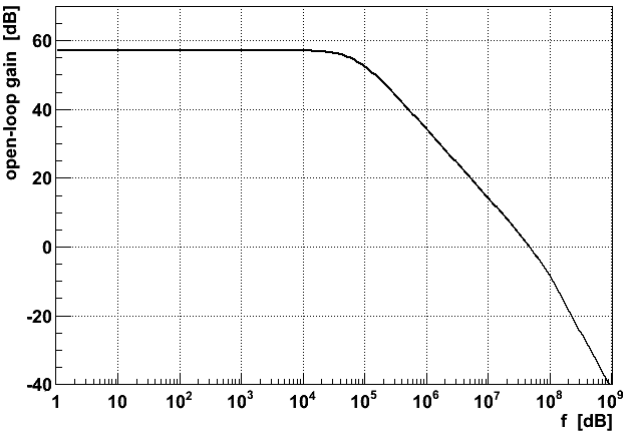

Figure 8: Symmetrical CMOS OTA with cascodes: simulated AC gain magnitude for nominal 20 pF load capacitance and 50 MHz GBW.

Comparison

Four different circuit topologies have been discussed: telescopic cascode and folded cascode OTAs, two-stage Miller compensated OTA and symmetrical OTA with cascodes. Each solution offers advantages and disadvantages, introducing different trade-offs. A comparison in terms of gain, output swing, speed, power dissipation and noise is presented in Table 1.

The maximum voltage gain achievable with a single-stage amplifier is limited to the product between the input transistor transconductance and the total output resistance. Cascoding can be used to increase the gain at low frequencies at cost of limiting the voltage headroom. If more gain and swing are required, two-stage configurations or gain enhancement techniques must be used. Telescopic, folded cascode and symmetrical topologies offer moderate gain but are affected by limited swings. The two-stage Miller OTA provides the highest voltage gain and the largest output swing.

However, gain trades with speed. More gain at low frequencies results into a reduced bandwidth for a given GBW. The telescopic cascode OTA is fast, whereas the two-stage Miller OTA offers limited speed. Design optimizations to increase speed in two-stage Miller OTAs exist, at cost of reducing the gain. Larger GBW can be obtained with the symmetrical OTA as well. Note that frequency compensation is simply performed by the load capacitance in circuits that exhibit a single-pole system behaviour. Neither telescopic cascode, folded cascode and symmetrical OTAs require to use compensation techniques.

Power consumption is determined by the choice of the DC bias currents and by the number of branches in the circuit. More branches of course lead to more power dissipation. The telescopic cascode OTA provides the lowest current dissipation, which doubles if a folded cascode topology is chosen. The two-stage Miller compensated OTA takes the highest power consumption due to the large current required in the second stage. Moderate and weak inversion can be exploited to save power, but at cost of reduced transconductances and therefore gain.

Further trade-offs arise between noise, power consumption and gain. In order to decrease the noise, larger bias currents must be used, resulting in higher power dissipation. On the other hand, thermal noise currents decreases by decreasing transconductances, which in turn decreases the gain. Noise can be limited by using cascodes. Telescopic cascode and two-stage Miller OTAs exhibit low noise, whereas folded cascode and symmetrical topologies offer medium noise performance.

Circuit topology	Gain	Output swing	Speed	Power consumption	Noise
telescopic cascode OTA	medium	low	highest	low	low
folded cascode OTA	medium	medium	high	medium	medium
two-stage Miller OTA	highest	highest	low	highest	low
symmetrical OTA with cascodes	high	medium	high	high	medium

Table 1: Comparison of performance for different CMOS OTA topologies

One can note that the folded cascode OTA offers the best compromise between gain, swing, speed, power and noise. As a matter of fact, it represents the most popular choice for the implementation of a general purpose amplifier.

Conclusions

A critical analysis of four different CMOS operational transconductance amplifiers has been presented. Advantages and disadvantages of each circuit topology in terms of gain, speed, output swing, power consumption and noise were discussed. Pratical design examples and CAD simulations have been included, using a commercial 1.5 V supply voltage 130 nm CMOS technology and assuming 20 pF load capacitance. At the end, a comparison between different circuit performance was given.

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