A Low-Power Low-Noise Synchronous Pixel Front-End Chain in 65 nm CMOS Technology with Local Fast ToT Encoding and Autozeroing for Extreme Rate and Radiation at HL-LHC

Luca Pacher [a,b,†], *Student Member IEEE*, Ennio Monteil [a,b],
Angelo Rivetti [b], *member IEEE*, Natale Demaria [b] and Manuel Da Rocha Rolo [b]

[a] University of Torino, Department of Physics, 10125, Torino, Italy
[b] INFN, Section of Torino, 10125, Torino, Italy

[†] Speaker candidate and corresponding author - pacher@to.infn.it

***Abstract*—A low-power and low-noise synchronous front-end chain in a commercial 65 nm CMOS technology suitable for the future pixel upgrades at the CERN Large Hadron Collider (LHC) is presented. A shaper-less charge-sensitive amplifier with constant current feedback provides triangular pulse shaping for linear time-over-threshold (ToT) charge measurements. Sensor leakage currents are compensated by the same feedback network. A track-and-latch voltage comparator is proposed for the hit discrimination. The hit generation is synchronized with a 40 MHz clock, avoiding time-walk issues in the time-stamp assignment. Fast ToT charge encoding up to 8-bit resolutions can be retrieved at the pixel level using high-frequency self-generated clock signals obtained by turning the latch into a voltage-controlled oscillator using asynchronous logic. Pixel-to-pixel threshold variations are compensated by means of an autozeroed scheme, without the usage of a on-pixel D/A converter. A pixel array of 8 $\times$ 8 pixel cells with 50 μm $\times$ 50 μm pixel size has been prototyped. Design specifications, implementation and test results will be discussed.**

SUMMARY

The foreseen High-Luminosity (HL) LHC upgrade will impose the installation of new silicon pixel detectors in the inner tracking systems of general-purpose experiments.

With increased performance the machine will deliver proton collisions with an instantaneous luminosity of the order of 10^{35} cm^{-2}s^{-1}, one order of magnitude higher with respect to the current design value, targeting to reach an integrated luminosity of 3000 fb^{-1} in 10 years. With such a luminosity and a centre-of-mass energy of 14 TeV the nominal collision rate of 40 MHz will lead to unprecedented track densities, introducing extreme rates and radiation levels. More layers equipped with sensors featuring high granularity, speed and radiation hardness will be required close to the interaction regions. Thus hybrid silicon pixel detectors will continue to play a fundamental role.

The innermost pixelated layer will have to cope with an expected Total Ionizing Dose (TID) of 10 MGy in 10 years, corresponding to 10^{16} (1 MeV) n_{eq}/cm^2. Smaller pixels of the order of 50 μm $\times$ 50 μm will be required to maintain high spatial resolution and two-tracks separation. The particle flux will increase to 500 MHz/cm^2, leading to hit rates of the order of 1 GHz/cm^2 and an estimated average rate per pixel of 50 kHz. The foreseen usage of thinner sensors of 100-150 μm thickness to increase the radiation tolerance will determine reduced signals, needing low-threshold (as low as 1 ke^- minimum detectable charge) and low-noise (below 150 e^- RMS at nominal 100 fF input capacitance including strays) performance for the analogue front-end. Moreover a time response below 25 ns is required in order to cope with the nominal LHC bunch crossing rate, while keeping bias currents to acceptable values and targeting to a total maximum power dissipation of 10 μW per pixel. More on-chip intelligence and much higher readout bandwidth will be required in order to cope with unprecedented data rates.

Research and development activities devoted to the design of new pixel Application Specific Integrated Circuits (ASIC) suitable for HL-LHC upgrades have started. A commercial 65 nm CMOS process has been identified by the pixel ASIC community as a promising fabrication technology for the implementation of new generation pixel readout chips. Such a 65 nm was already demonstrated to be radiation tolerant up to 3 MGy [1]. Technology qualification and radiation hardness studies using 65 nm CMOS are now part of the international RD53 collaboration research program officially supported by CERN [2] and of the Italian INFN CHIPIX65 project.

Preliminary pixel front-end test structures, small pixel arrays and other analogue, digital and mixed-signal building blocks have been submitted by the CHIPIX65 collaboration to the foundry access service. They were received back from the manufacturer for laboratory test measurements and bench characterizations at the beginning of 2015.

A small pixel array of 8 $\times$ 8 cells with 50 μm $\times$ 50 μm pixel size has been prototyped as part of the first CHIPIX65 submission. The final layout of the chip, referred to as CHIPIX_VFE1/TO, is presented in Fig.1. In order to gain from increased speed offered by a 65 nm CMOS technology node and meet low-threshold and low-power requirements a synchronous front-end architecture has been implemented. The analogue part occupies about 50% of the total pixel size and features the following components.

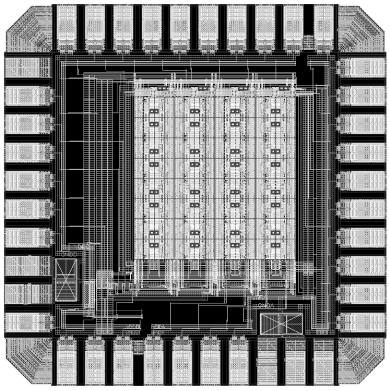

Fig. 1. Complete layout of the CHIPIX_VFE1/TO chip, 945 μm $\times$ 945 μm. The prototype contains 8 $\times$ 8 pixels with synchronous front-end and full-analogue readout at the oscilloscope of all channels.

The input stage is a Charge Sensitive Amplifier (CSA) implemented as a single-ended, 60 dB open-loop gain inverting amplifier with two selectable feedback capacitors. In order to save power and area a shaper-less solution was adopted. Hence the CSA output directly drives the front-end discriminator. Linear charge measurements up to 40 ke^- are performed using the ToT technique, therefore triangular pulse shaping is adopted. A time-invariant feedback network based on an auxiliary transconductance amplifier discharges the feedback capacitance with a selectable constant current in the 5-100 nA range after a charge signal has been detected [3]. The same feedback circuit compensates sensor leakage currents up to 50 nA. A calibration circuit is used to inject a test charge at the CSA input node. Selectable test capacitors have been added to mimic different values of pixel sensor capacitance.

The front-end amplifier is AC coupled to a discrete-time hit discriminator. A track-and-latch voltage comparator has been adopted. It is implemented as a low-gain high-bandwidth differential preamplifier coupled to a regenerative latch stage. Thanks to positive feedback precise and fast voltage comparisons can be obtained with low-power dissipations, allowing to discriminate very low charge-induced signals above the nominal threshold. The generation of a CMOS digital hit pulse is synchronized with a 40 MHz master clock, sampling the CSA analogue output. This provides a reliable solution that overcomes time-walk issues in the time-stamp assignment.

The latch can be turned into a voltage-controlled oscillator (VCO) by means of a dedicated asynchronous logic. Similar techniques are employed in the design of modern charge redistribution Successive Approximation Register (SAR) A/D converters which internally generate necessary clock signals for SAR operations [4]. As derived from transient simulations flexible and high-speed ToT digitizations up to 8-bit resolution can be performed in less than 400 ns using selectable on-pixel self-generated clock waveforms in the 100-900 MHz range.

Pixel-to-pixel threshold variations are compensated without the need of a local D/A converter for digital trimming. The offset voltage is periodically sampled and stored on capacitors using Output-Offset Storage (OOS) between the preamplifier and the latch [5]. The lack of a on-pixel D/A converter introduces fundamental advantages in perspective of pixel operations in a harsh radiation environment, avoiding the necessity of dedicated Single Event Upset (SEU) tolerant registers to store the configuration bits for digital trimming. The available area for local temporary data storage (buffering) and signal processing in the digital part can significantly increase. Furthermore efficient calibration schedules can be defined according to online machine operations.

Tests results obtained from CHIPIX_VFE1/TO synchronous pixels will be presented. All basic electrical functionalities in terms of gain, linearity, noise and threshold dispersion have been validated. Latch operations as a local oscillator have been proved to work. Sample oscilloscope waveforms are presented in Fig. 2. The measured Equivalent Noise Charge (ENC) is about 100 e^- RMS at nominal 100 fF input capacitance. The total power consumption is 6.4 μW per pixel. Measurements are in agreement with CAD simulations. First irradiation tests with X-rays and 3 MeV protons are foreseen in summer 2015.

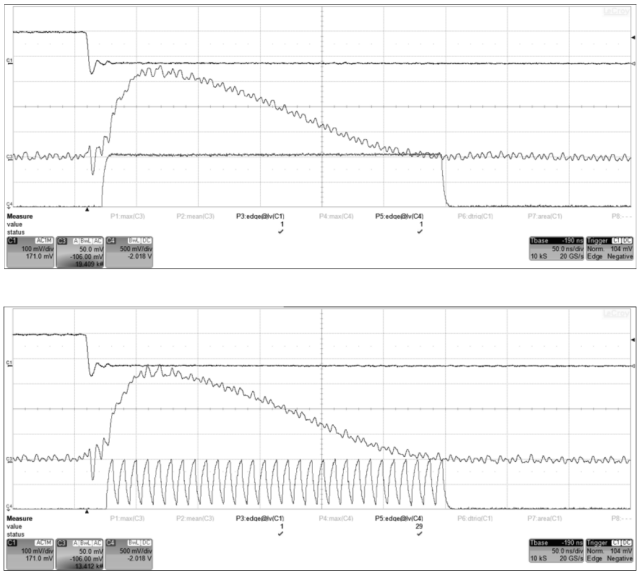

Fig. 2. Sample waveforms at the oscilloscope for 10 ke^- injected charge and 40 nA feedback current. The CSA output pulse with triangular shaping is sampled at 40 MHz. The width of the hit pulse is an integer number of clock cycles (top). Latch operations when turned into a local oscillator for fast ToT counting (bottom). The time base is 50 ns/div.

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