PSpice Tutorial

(usage of simulator) × (common sense) ≈ constant

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SPICE

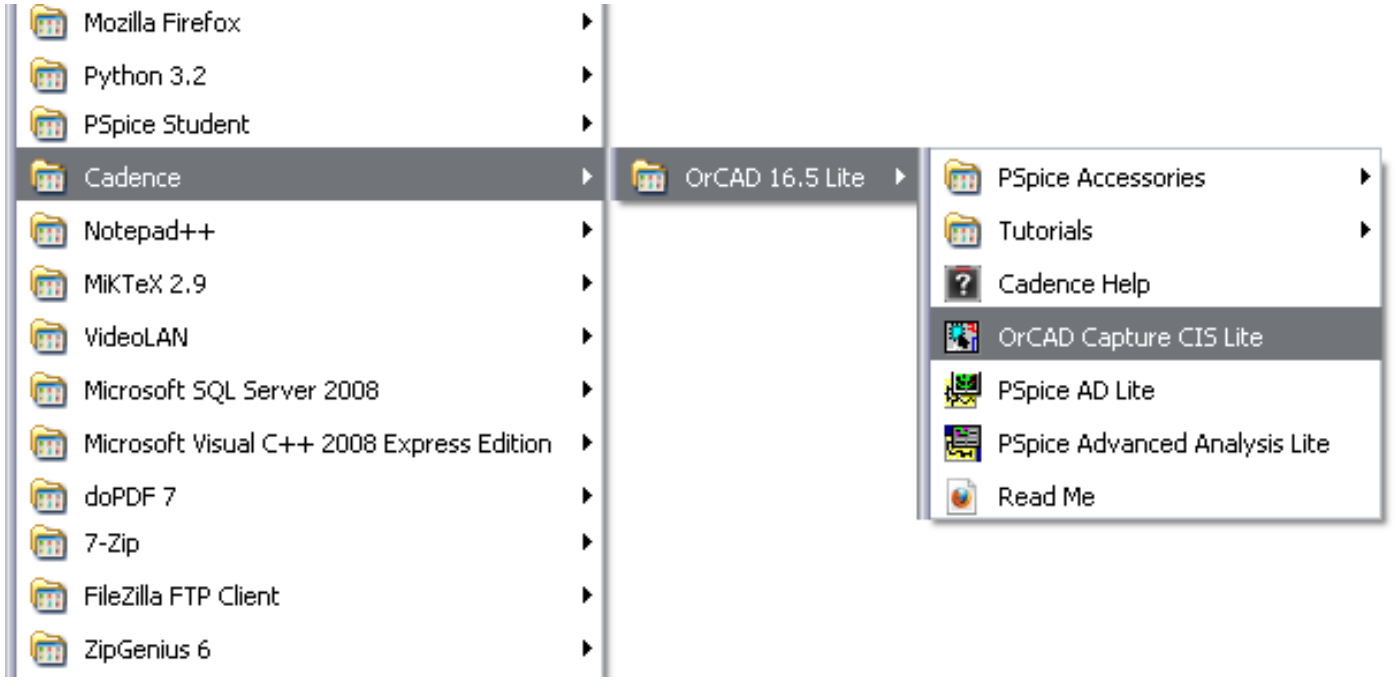
- **S**imulation **P**rogram with **I**ntegrated **C**ircuits **E**mphasis
- Berkeley University open source code (initially coded in FORTRAN, rewritten in C)
- analog-only circuits simulator
- ***command-line tool*** with a plain text input file (**.cir**)
  - interpreted 'markup' and programming language (both UNIX and MS-DOS shells)
  - ***input file = netlist + electrical models + analysis statements***
  - `spice < inputFile.cir | more`
  - plain text output file
- new SPICE-like commercial versions with ***graphical interfaces*** :

  PSpice, ***HSpice***, ***LTSpice***, ***Spectre*** *etc.*

PSpice

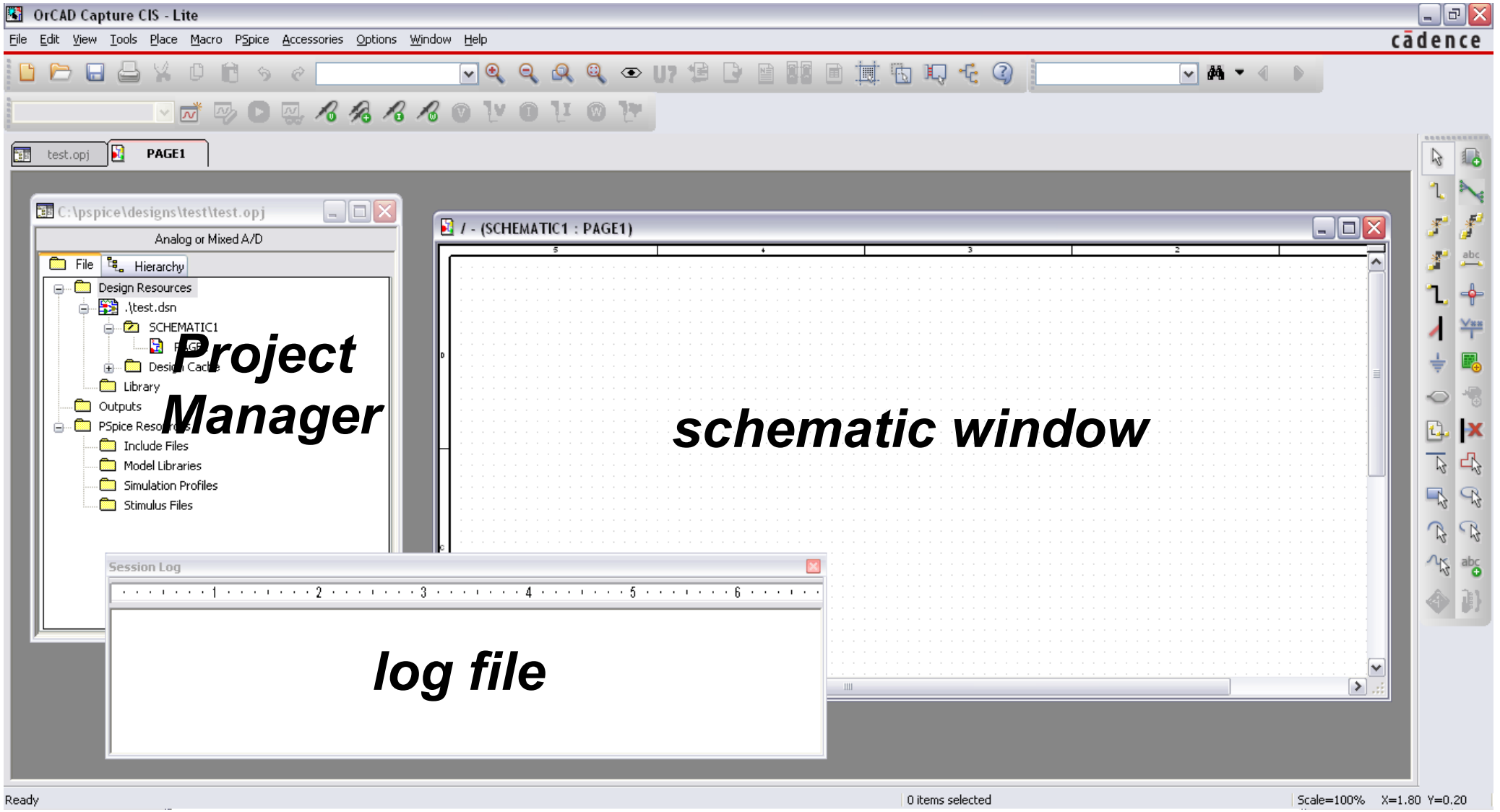
- **P**ersonal **SPICE**
- the SPICE version for personal computers with MS Windows operating systems
- analog, digital and mixed-signals simulator
- initially developed by MicroSim and then bought by OrCAD
- at present purchased by ***Cadence Design Systems***
- free versions:
  - ***PSpice Student 9.1*** - *max. 10 transistors*
  - ***OrCAD PCB Designer 16.5 Lite (demo)*** - *max. 20 transistors*
- industry standard PCB development suite

Tools overview

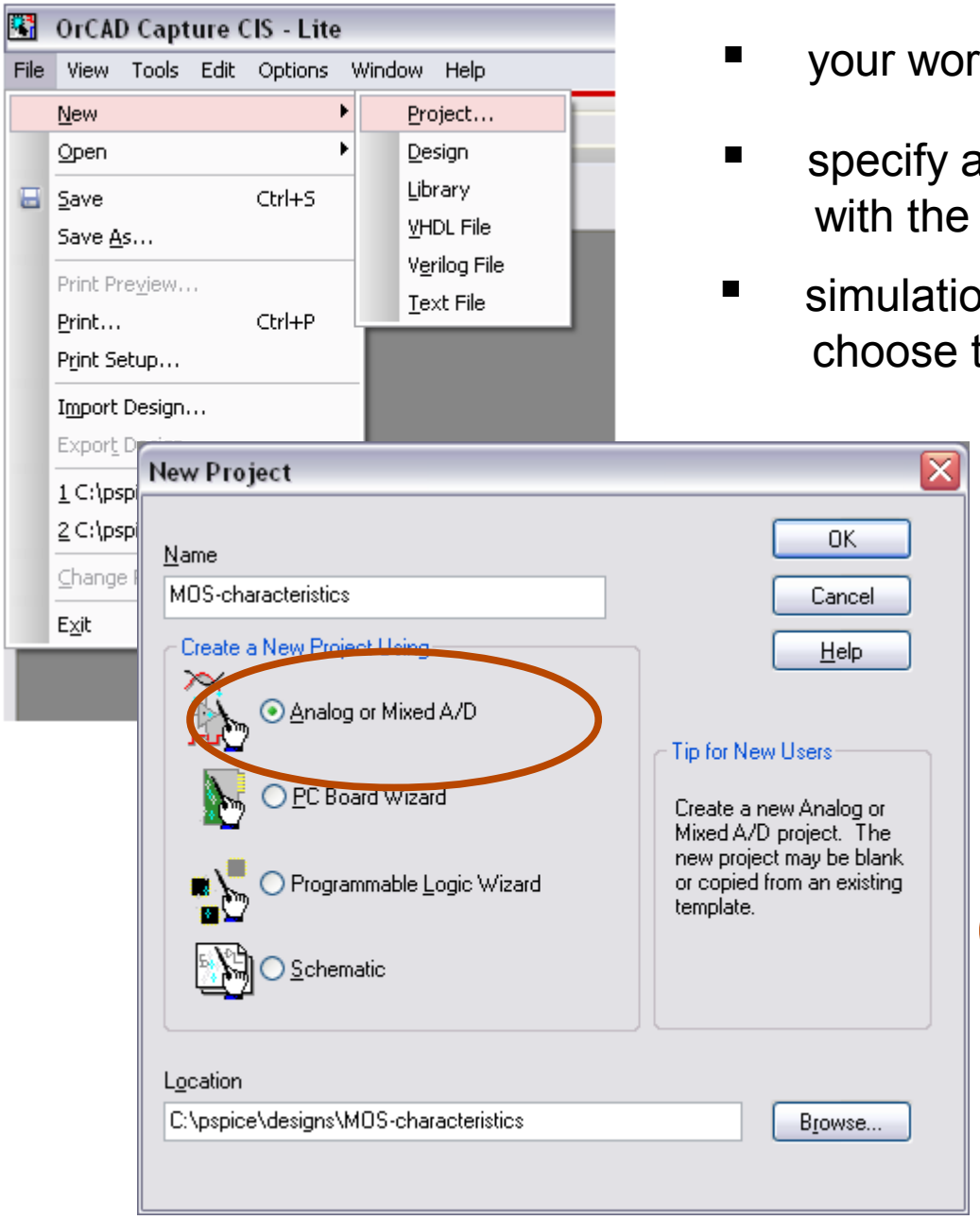


- ***Capture*** - schematic entry tool
- ***PSpice A/D*** - analog, digital and mixed-circuits simulator
- ***PSpice Advanced Analysis*** - Monte Carlo, sensitivity/worst case etc. analyses
- ***PSpice Model Editor*** - edit text SPICE models or extract models from data sheets
- ***PSpice Stimulus Editor*** – graphical editor for time-based waveform

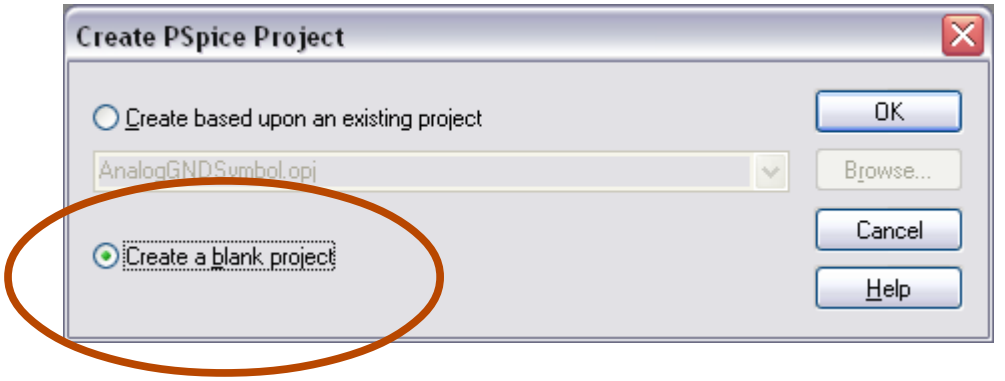
Getting started



Working with projects



- your work is organized into ***projects*** (**.opj** main file)
- specify a new folder in `C:\pspice\designs` with the same name of the project
- simulations with PSpice are available only if you choose the ***Analog or Mixed A/D*** option



Running SPICE programs

- you can run SPICE programs with PSpice at the Windows command-line by using ***pspice.exe*** or ***psp_cmd.exe*** executables
  - `pspice [options] [input file(s)]`
  - write the SPICE program with a simple text editor and save it as a **.cir** file
  - at the command line type one of the following:

    `pspice -r inputFile.cir` (interactive mode)

    `psp_cmd -r inputFile.cir` (batch mode)
  - PSpice produces a plain text **.out** file containing simulation results
  - the .cir file must be placed in the same directory where you run the command
- `%CDSROOT%\tools\pspice` must be in the `PATH` environment variable

Input file example

```
NMOS I-V characteristic

* this is a comment

* circuit description (netlist)
VGS    1    0    DC   1.5
VDS    2    0    DC   2.5
M1    2    1    0    0    nfet    W=50u    L=1u

* device SPICE model
.MODEL nfet NMOS(
+ LAMBDA = 0.002
+ VTO = 0.424
+ KP = 250e-6
+ GAMMA = 0.37
+ PHI = 0.7 )

* analyses
.OP
.DC    VDS    0    6    50m

* output results
.PRINT DC   ID(M1)

.END
```

title line

netlist

device SPICE model

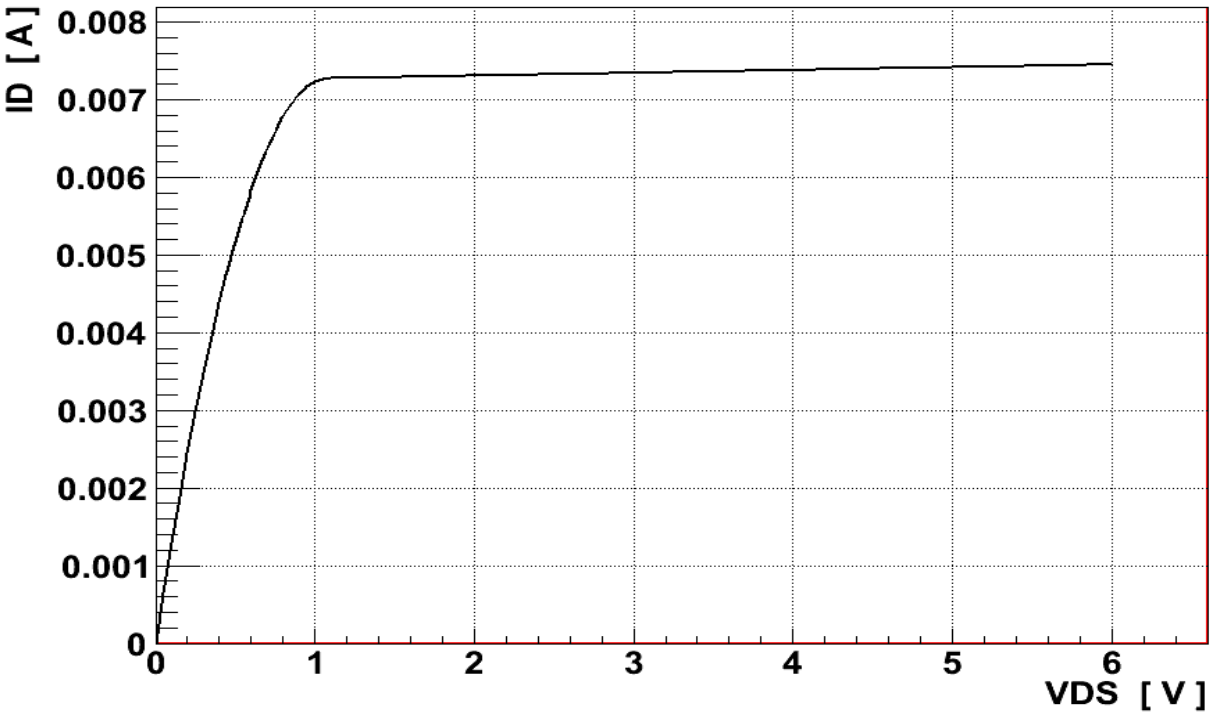
analysis statements

output results

```
Command Line
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

C:\Documents and Settings\luca>cd \pspice\SPICE

C:\pspice\SPICE>
C:\pspice\SPICE>
C:\pspice\SPICE>mkdir test

C:\pspice\SPICE>cd test

C:\pspice\SPICE\test>
C:\pspice\SPICE\test>
C:\pspice\SPICE\test>notepad test.cir

C:\pspice\SPICE\test>
C:\pspice\SPICE\test>
C:\pspice\SPICE\test>psp_cmd -r test.cir

**** PSpice 16.5.0 (April 2011) ****

NMOS I-V characteristic
Reading and checking circuit
Circuit read in and checked, no errors
DC Analysis
DC Analysis finished
Calculating bias point
Bias point calculated
Simulation complete.

C:\pspice\SPICE\test>dir
 Volume in drive C has no label.
 Volume Serial Number is A030-8387

 Directory of C:\pspice\SPICE\test

04/30/2012  08:56 PM    <DIR>          .
04/30/2012  08:56 PM    <DIR>          ..
04/30/2012  08:56 PM               389 test.cir
04/30/2012  08:56 PM             6,977 test.out
               2 File(s)          7,366 bytes
               2 Dir(s)  42,950,078,464 bytes free

C:\pspice\SPICE\test>notepad test.out

C:\pspice\SPICE\test>_
```

```
test.out - Notepad
File  Edit  Format  View  Help

**** 04/30/12 20:56:23 ******** PSpice Lite (April 2011) ******** ID# 10813 ****

 NMOS I-V characteristic

 ****     DC TRANSFER CURVES                    TEMPERATURE =   27.000 DEG C

******************************************************************************


  VDS          ID(M1)

  0.000E+00    0.000E+00
  5.000E-02    6.569E-04
  1.000E-01    1.283E-03
  1.500E-01    1.877E-03
  2.000E-01    2.441E-03
  2.500E-01    2.973E-03
  3.000E-01    3.475E-03
  3.500E-01    3.945E-03
  4.000E-01    4.384E-03
  4.500E-01    4.791E-03
  5.000E-01    5.168E-03
  5.500E-01    5.513E-03
```

the `PRINT` statement specifies that numerical results must be tabulated in the .out file



A little SPICE primer

- basic syntax:
  - SPICE is ***not case-sensitive***, upper case and lower case letters are equivalent
  - ***comments*** begin with *
  - all statements begin with a dot, e.g. `.OP .TRAN .PRINT .PLOT`
  - leading + characters indicate a ***line continuation***
  - netlist elements and analysis statements can be written in any order
- netlist and analysis directives are ***automatically generated*** by a ***shematic entry tool*** (***Capture*** in PSpice)
- you are not required to learn SPICE programming, but you should be able to read and understand the ***PSpice text output file*** *!*
- more knowledge about SPICE is useful to better understand Capture symbols parameters and PSpice simulations and options

Netlist

- '*schematic*' is a meaningless word for SPICE, just a human graphical visualization of the circuit
- a ***netlist*** is the SPICE description of a circuit using a simple description language
- each component has two or more terminals attached to ***nodes***
  - each circuit node is identified by a unique name (a number, a character or a string)
  - ***at least one node MUST be named 0 for the ground (common reference)***
  - no simulations can be performed with a missing 0 node (***floating-node error***)
- circuit components are identified by letters (e.g. `R` for resistors, `M` for MOSFETs etc.)
- each ***component line*** follows the simple syntax:

```
component  node1  node2  node3 .. value(s)
```

component	basic SPICE syntax
resistor	`Rxx node1 node2 [model_name] value [TC= ]`
capacitor	`Cxx node1 node2 [model_name] value [IC= ]`
inductor	`Lxx node1 node2 [model name] value [IC= ]`
diode	`Dxx node1 node2 model_name`
BJT	`Qxx C B E [sub] model_name`
MOSFET	`Mxx D G S B model_name [L= ] [W= ]` `+[AD= ] [AS= ] [PD= ] [PS= ]`
VDC [1]	`Vxx node1 node2 [DC] value`
VAC	`Vxx node1 node2 [[DC] value] AC value`
VSIN [2]	`Vxx node1 node2 SIN(VOFF VAMPL FREQ` `+[TD][DF][PHASE])`
VPULSE	`Vxx node1 node2 PULSE(V1 V2 TD TR TF PW PER)`
VPWL [3]	`Vxx node1 node2 PWL(t0 V0 t1 V1 ... tn Vn)`

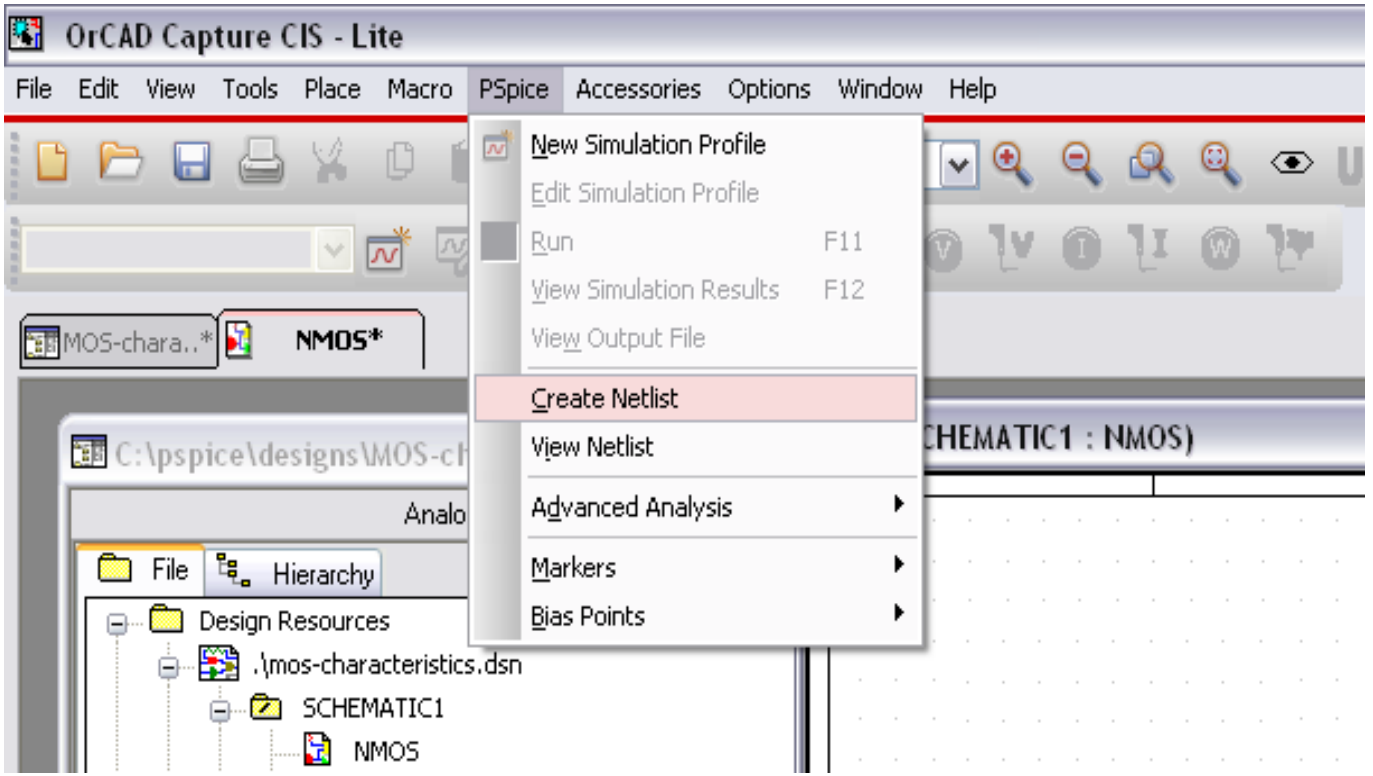
[ ] indicate optional terms

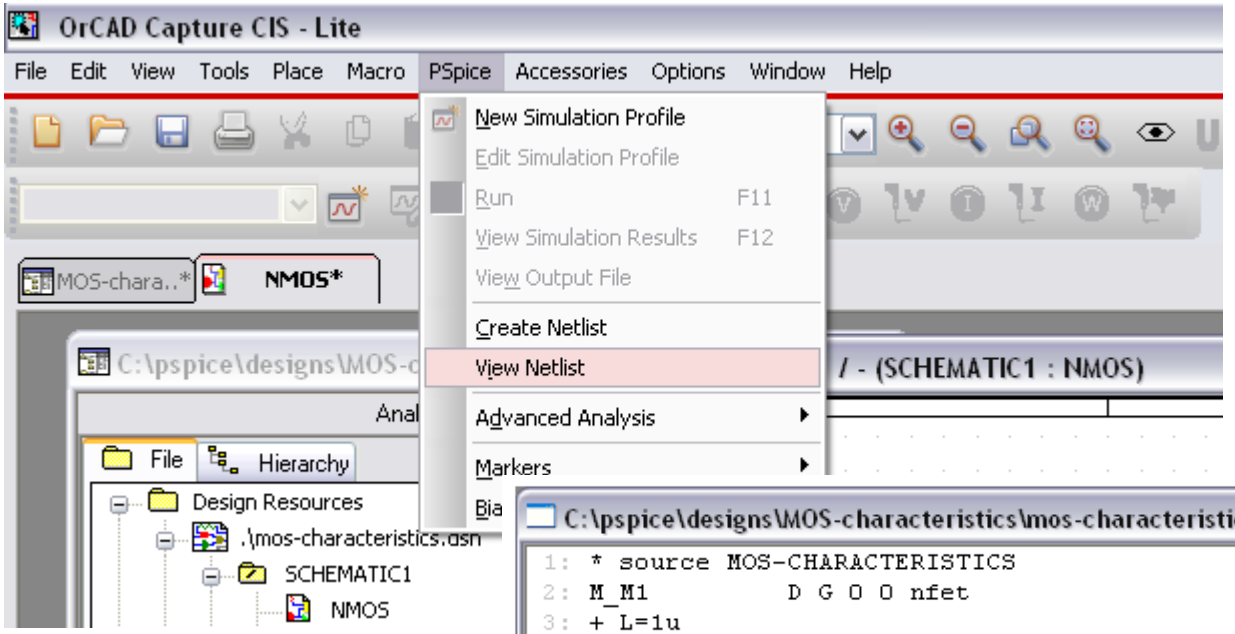
[1] current sources (IDC, IAC, ISIN, IPULSE, etc.) follow the same syntax

[2] more in general an exponential-dumped sinusoidal waveform

[3] piece-wise linear

PSpice netlist generation



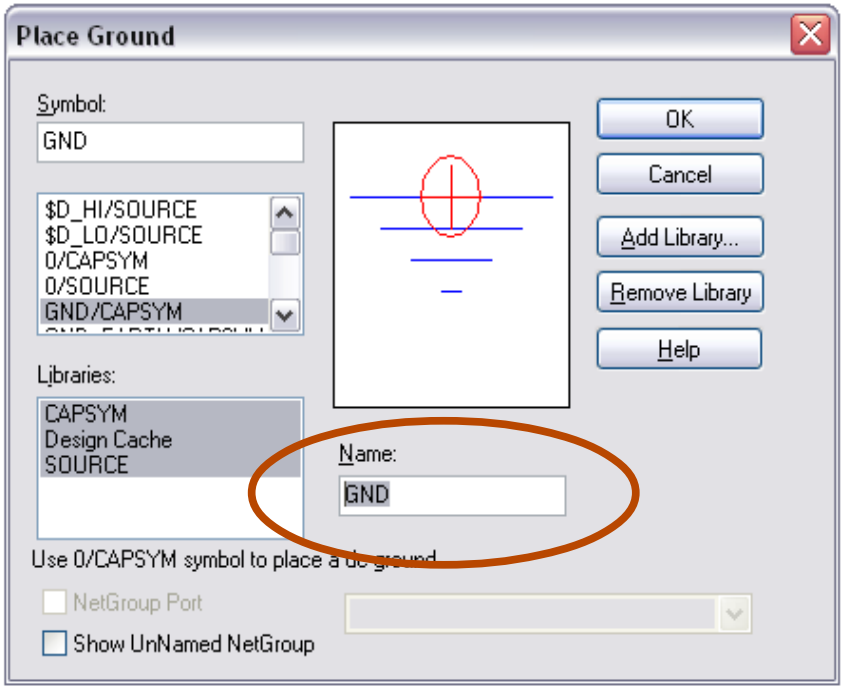


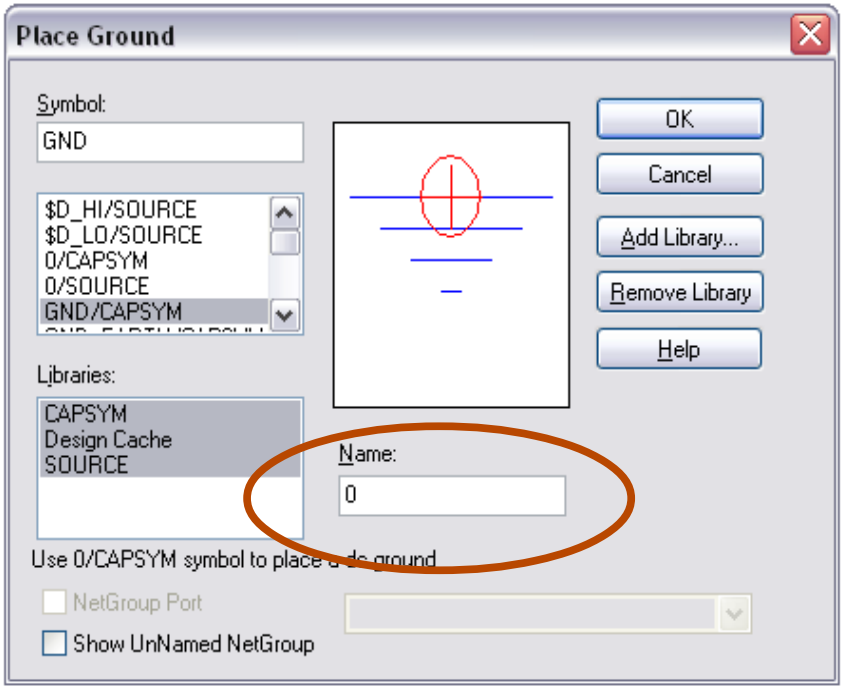
C:\pspice\designs\MOS-characteristics\mos-characteristics-pspicefiles\schematic1\schematic1.net

```
1: * source MOS-CHARACTERISTICS
2: M_M1          D G 0 0 nfet
3: + L=1u
4: + W=50u
5: V_V1          G 0 {Vgs}
6: V_V2          D 0 {Vds}
7: .PARAM  vgs=1.5 vds=2.5
8:
9:
10: ** Wrapper definitions for AA legacy support **
11:
12:
13: .model nfet nmos
14:
15: + level=3
16: + tox=5.7e-009
17: + nsub=1e+017
18: + gamma=0.431731
19: + phi=0.7
20: + vto=0.423825
21: + delta=0
22: + uo=425.647
23: + eta=0
24: + theta=0.175405
25: + kp=0.000250105
26: + vmax=82878.5
27: + kappa=0.168678
```

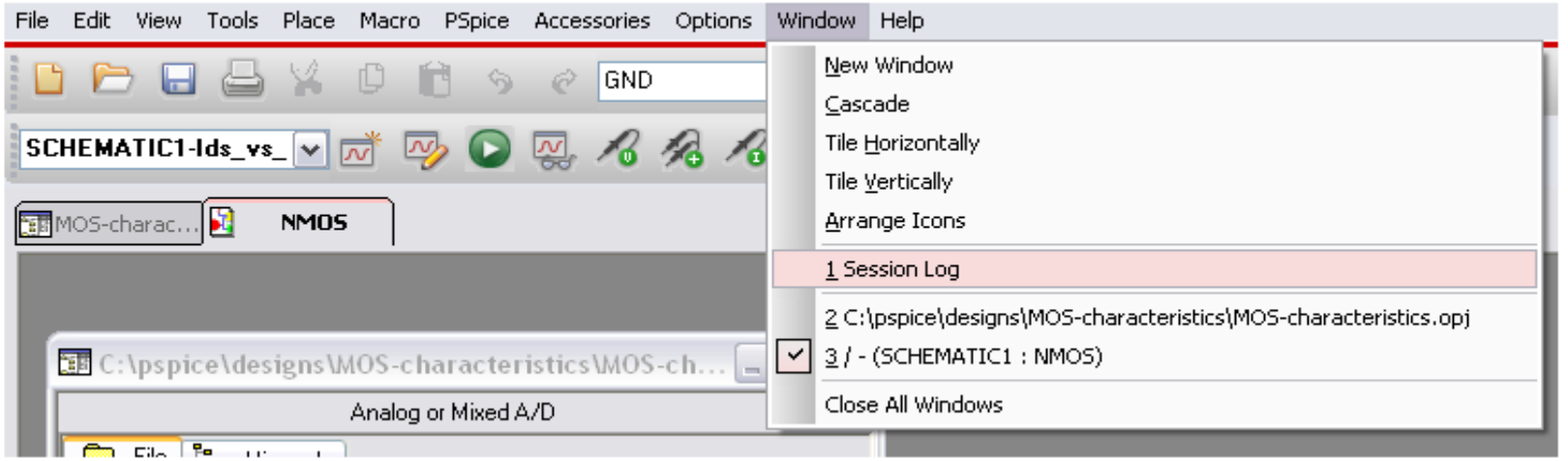
Placing grounds

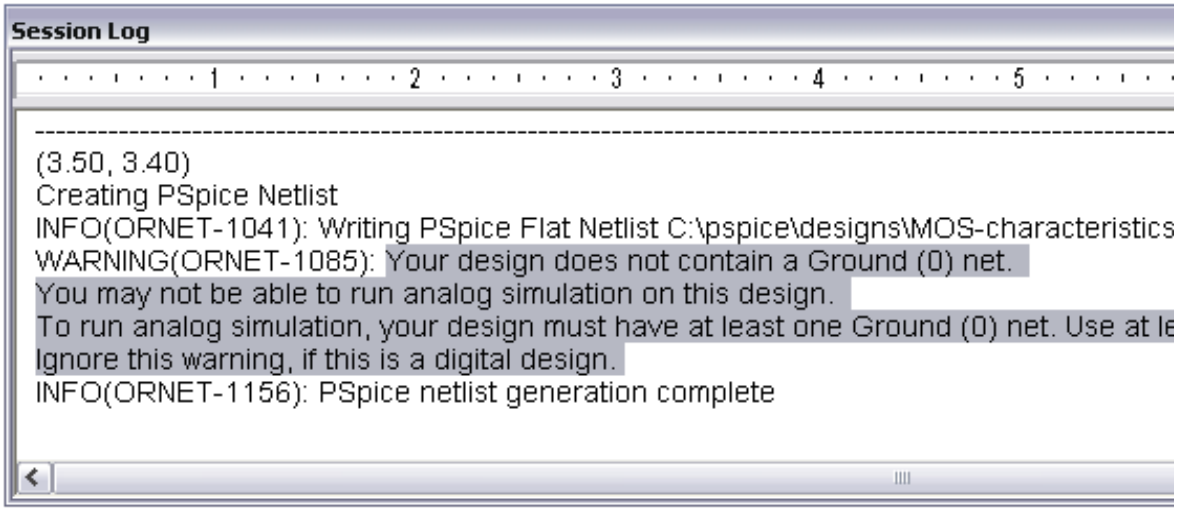
- remind: ***at least one node must be named 0*** (floating-node error otherwise)
- go to ***Place*** **> Ground** or press G
- use **CAPSYM / 0** or any other **CAPSYM /GND** symbol (GND, GND_EARTH, etc)
  but ***change Name into 0***

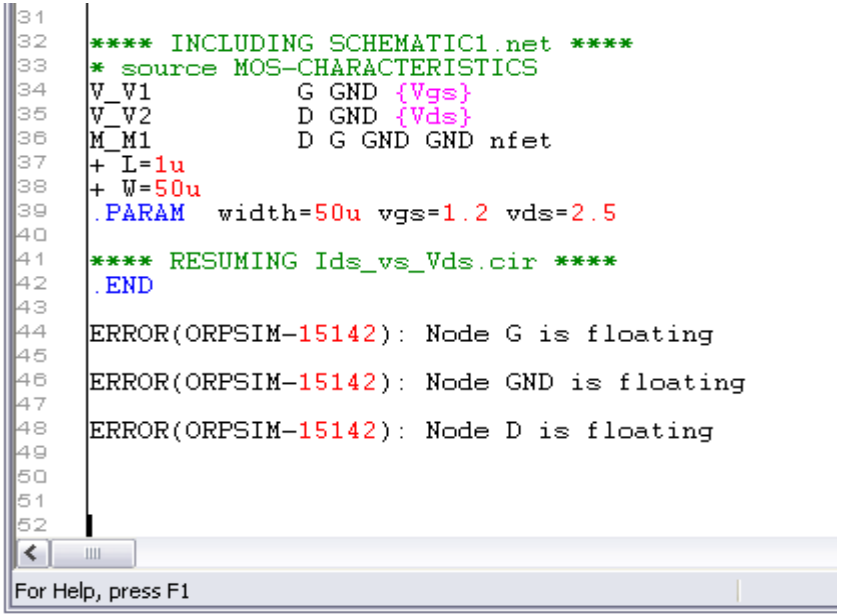




Checking the Session Log







SPICE SI units prefixes

name	SI	SPICE	C/C++ style
tera	T	T, t	1e12, 1E12
giga	G	G, g	1e9, 1E9
mega	M	MEG, meg	1e6, 1E6
kilo	k	K, k	1e3, 1E3
milli	m	M, m	1e-3, 1E-3
micro	μ	U, u	1e-6, 1E-6
nano	n	N. n	1e-9, 1E-9
pico	p	P, p	1e-12, 1E-12
femto	f	F, f	1e-15, 1E-15

- SPICE is ***not case-sensitive***, upper case and lower case letters are equivalent
- be careful not to use M for mega! 15Mohm are 15 milliohm for SPICE
- the unit name can be neglected
- numerical values and prefixes must be typed without spaces

e.g. *C = 10uF, 10u, 10e-6, 10E-6f*

Basic analyses

- PSpice (not SPICE) can simulate circuits containing any mix of analog and digital devices
- ***DC analyses***
  - bias point (`.OP`)
  - DC sweep (`.DC`)
- ***time-domain analyses***
  - transient (`.TRAN`)
  - Fourier (`.FOUR`)
- ***frequency-domain analyses***
  - AC sweep (`.AC`)
  - noise (`.NOISE`)

Bias point (.OP)

- large-signal DC solution for a particular input voltage/current condition
- ***the time is removed from the circuit***
  - sources with time specifications are set to zero
  - all capacitors are considered open circuits, all inductors shorts
  - DC analysis is a particular case of transient analysis ($dv/dt = 0,\ di/dt = 0$)
- automatically computed in any other simulation
- simulation results are printed in the ***text output file***
  - list of all node voltages, voltage source currents and total power dissipation
  - ***detailed bias point information for semiconductor devices***

```
.OP
```

DC sweep (.DC)

- ***large-signal steady-state circuit DC response*** when sweeping a voltage/current source, a global parameter, a model parameter or the temperature over a range of values
  - the bias point of the circuit is calculated for each value of the sweep

- ***nested DC sweep analysis*** can be performed
  - a second sweep variable can be selected after a primary sweep value has been specified
  - curve families are obtained

```
.DC [sweep]  source1/parameter1 START1  STOP1  STEP1
   +[source2/parameter2  START2  STOP2  STEP2]
```

  - parametric sweeps are available with PSpice only
  - the sweep parameter can be `LIN` (linear) `DEC` (logarithmically by decades) or `OCT` (logarithmically by octaves) , available with PSpice only

Transient analysis (.TRAN)

- large-signal response of the circuit to one or more time-dependent inputs
  - ***numerical integration*** of a non linear differential equations system
  - a first DC analysis determines the ***initial circuit bias conditions***

- voltages and currents tracked over time
  - a smaller integration time step increases both the results accuracy and the simulation duration
  - sometimes convergence problems can occur

```
.TRAN TSTEP TSTOP [TSTART [TMAX]]
```

  - a transient analysis always begins at *t = 0* and ends at *t =* `TSTOP`
  - `TSTEP` is the time interval for reporting simulation results in the output file
  - before the time `TSTART` no results are recorded
  - `TMAX` is the maximum step size in incrementing the time during transient analysis (numerical integration time-step)

AC sweep (.AC)

- small-signal frequency response of the circuit ***linearized*** around the bias point sweeping one or more sources over a range of frequencies
  - non-linear devices are linearized to determine their AC small-signal models
  - all independent voltage and current sources that have ***AC specifications*** are inputs to the circuit, e.g. VAC and IAC

- outputs include voltages and currents with ***magnitude*** and ***phase***
  - the best way to use AC sweep analysis is ***to set the source magnitude to one***, (e.g. ACMAG = 1) in this way ***the measured output equals the gain***, relative to the input source, at that output

```
.DC sweep points START  STOP
```

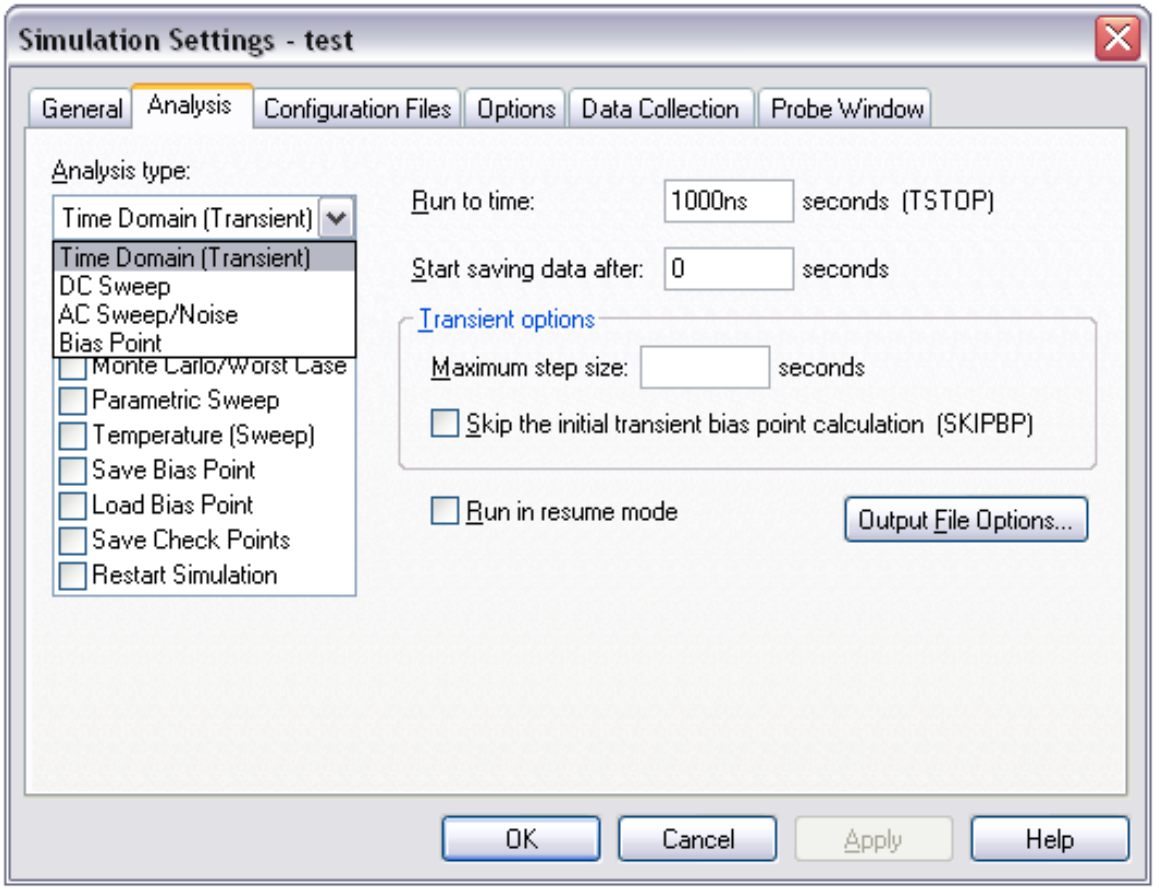
  - the `sweep` option can be `LIN` (linear) `DEC` (logarithmically by decades) or `OCT` (logarithmically by octaves)
  - specify the number of points per decade

PSpice simulations (1)

- during the schematic entry phase we use ***symbols***, defined inside the ***Capture libraries*** (**.olb** files) :
  - `%CDSROOT%\tools\capture\library`
  - `%CDSROOT%\tools\capture\library\pspice`
- only symbols associated with ***SPICE electrical models*** can be simulated by PSpice !
  - symbols of the `pspice` Capture library can be simulated with the standard ***PSpice model libraries*** (**.lib** files) listed in the ***nomd.lib*** file
  - `%CDSROOT%\tools\pspice\library`
- models of semiconductor devices can be modified using the ***PSpice Model Editor***
- ***custom*** PSpice model libraries must be ***included*** by hand (see later)

PSpice simulations (2)

- for each simulation you have to create a new ***simulation profile*** (**.cir** file)
- you can define multiple simulation profiles, but PSpice can run ***only one simulation at a time***



PSpice > New Simulation Profile

*The **Simulation Settings** window is a graphical user interface that automatically generates the SPICE analysis directives and writes them in a .cir simulation file*

PSpice simulation file example

```
****     CIRCUIT DESCRIPTION

******************************************************************************



** Creating circuit file "tran.cir"
** WARNING: THIS AUTOMATICALLY GENERATED FILE MAY BE OVERWRITTEN BY SUBSEQUENT SIMULATIONS

*Libraries:
* Profile Libraries :
* Local Libraries :
* From [PSPICE NETLIST] section of C:\pspice\OrCAD_Lite\tools\PSpice\PSpice.ini file:
.lib "nomd.lib"

*Analysis directives:
.TRAN  0 50u 0 10n
.PROBE V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))
.INC "..\SCHEMATIC1.net"


**** INCLUDING SCHEMATIC1.net ****
* source SYNTAX-TEST
C_C1         0 2  100p  TC=0,0
R_R1         1 2  10k TC=0,0
V_V1         1 0
+SIN 0 10m 50k 0 0 0

**** RESUMING tran.cir ****
.END
```

a simple RC filter

MOSFET SPICE models

- the simulator provides ***8 MOSFET device models***, which differ in the formulation of the I-V characteristic
- the `LEVEL` parameter selects among different models
  - `LEVEL = 1` ***Shichman-Hodges*** *model*
  - `LEVEL = 2` *geometry-based, analytic model*
  - `LEVEL = 3` *semi-empirical, short-channel model*
  - `LEVEL = 4` ***BSIM*** *model (Berkely short-channel IGSIM model)*
  - `LEVEL = 5` ***EKV*** *model version 2.6 (Enz-Krummenacher-Vittoz)*
  - `LEVEL = 6` ***BSIM3*** *version 2.0*
  - `LEVEL = 7` ***BSIM3*** *model version 3.2*
  - `LEVEL = 8` ***BSIM4*** *model version 4.1.0*
- present day sophisticated models become inadequate after one or two technology generations!

Shichman-Hodges model (1)

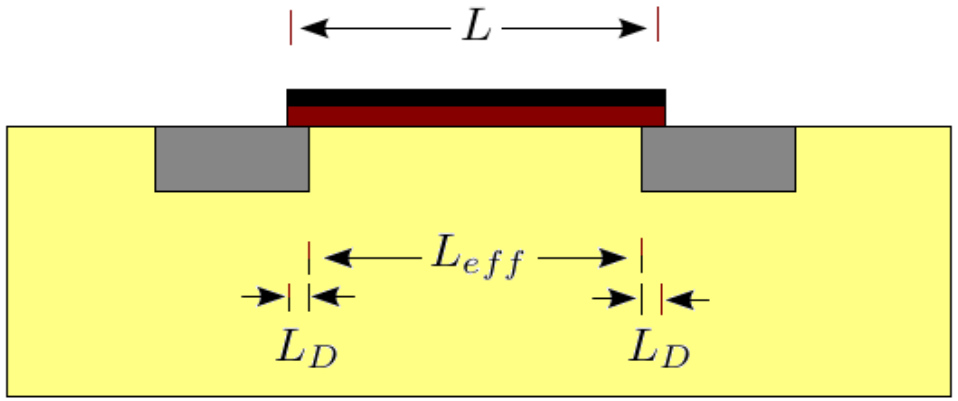
- the simplest MOS SPICE model
- the I-V characteristic takes into account the ***channel-length modulation*** and the ***gate overlap*** with source and drain implants

$$I_{DS} = \frac{1}{2} K_P \frac{W}{L - 2L_D} \left[2 \left(V_{GS} - V_{TH} \right) V_{DS} - V_{DS}^2 \right] \left(1 + \lambda V_{DS} \right)$$

linear (triode) region

$$I_{DS} = \frac{1}{2} K_P \frac{W}{L - 2L_D} \left(V_{GS} - V_{TH} \right)^2 \left(1 + \lambda V_{DS} \right)$$

saturation region



$$K_P = \mu C_{ox}$$

transconductance parameter

The actual distance between the source and the drain is slightly less than L

Shichman-Hodges model (2)

- the threshold voltage is given by the ***body effect formula***

$$V_{TH} = V_{TH0} + \gamma \left[\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right]$$

$$2\phi_F = \phi_B = 2\frac{kT}{q} \ln\left(\frac{N_{sub}}{n_i}\right)$$

2 x *(substrate Fermi potential)* - conventionally assumed equal to the built-in voltage

$$\gamma = \frac{\sqrt{2\varepsilon q N_{sub}}}{C_{ox}}$$

body effect coefficient **~ 0.3 ÷ 0.5 $V^{1/2}$** ($C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$)

- the model includes ***MOS parasitic capacitances***
- the model ***does not include*** sub-threshold conduction or any short-channel effects

SPICE parameters

SPICE parameter	description	unit
VTO[1]	threshold voltage without body effect	**V**
GAMMA	body effect coefficient	**$V^{1/2}$**
PHI	$2\phi_F$	**V**
TOX	gate oxide thickness	**m**
NSUB	substrate doping	**cm^{-3}**
LD	gate-source/drain overlap	**m**
UO	channel mobility	**cm^2 / Vs**
LAMBDA[2]	channel-length modulation coefficient	-
KP	transconductance parameter μC_{ox}	**A / V^2**
W	gate width	**m**
L	gate length	**m**

[1] becomes `VTH0` for `LEVEL > 5`

[2] defined only for `LEVEL = 1, 2`

SPICE modeling

```
.MODEL <model_name> XMOS( <parameters> )
```

- equations show that ***8 parameters*** are required to specify the I-V device characteristic:
  - 3 geometric parameters (`W`, `L`, `LD`)
  - 5 electrical parameters (`KP`, `LAMBDA`, `VTO` , `GAMMA`, `PHI`)
- another possibility is to use ***process and technology-related parameters***
  - `TOX`, `UO`, `NSUB` + `VTO`, `LAMBDA` + geometric parameters
  - this represents the SPICE default choice (if also `KP`, `GAMMA` and `PHI` are specified in the code the simulator re-evaluate them from `TOX`, `UO` and `NSUB` values)
- `W` and `L` can be specified for each transistor, using a common device model for the other parameters

Examples

```
.MODEL nfet NMOS(
+ LEVEL = 1      VTO = 0.7      GAMMA = 0.45      PHI = 0.9
+ NSUB = 9e14    LD = 0.08e-6   UO = 350          LAMBDA = 0.1
+ TOX = 9e-9     PB = 0.9       CJ = 0.56e-3      CJSW = 0.35e-11
+ MJ = 0.45      MJSW = 0.2     CGDO = 0.4e-9     JS = 1.0e-8 )
```

```
.MODEL pfet PMOS(
+ LEVEL = 1      VTO = -0.8     GAMMA = 0.4       PHI = 0.8
+ NSUB = 5e14    LD = 0.09e-6   UO = 100          LAMBDA = 0.1
+ TOX = 9e-9     PB = 0.9       CJ = 0.94e-3      CJSW = 0.32e-11
+ MJ = 0.5       MJSW = 0.3     CGDO = 0.3e-9     JS = 0.5e-8 )
```

- capacitive parameters are not described in this lecture
- *B. Razavi,* ***Design of Analog CMOS Integrated Circuits****,* ch 2, pp. 36-37

Higher level models

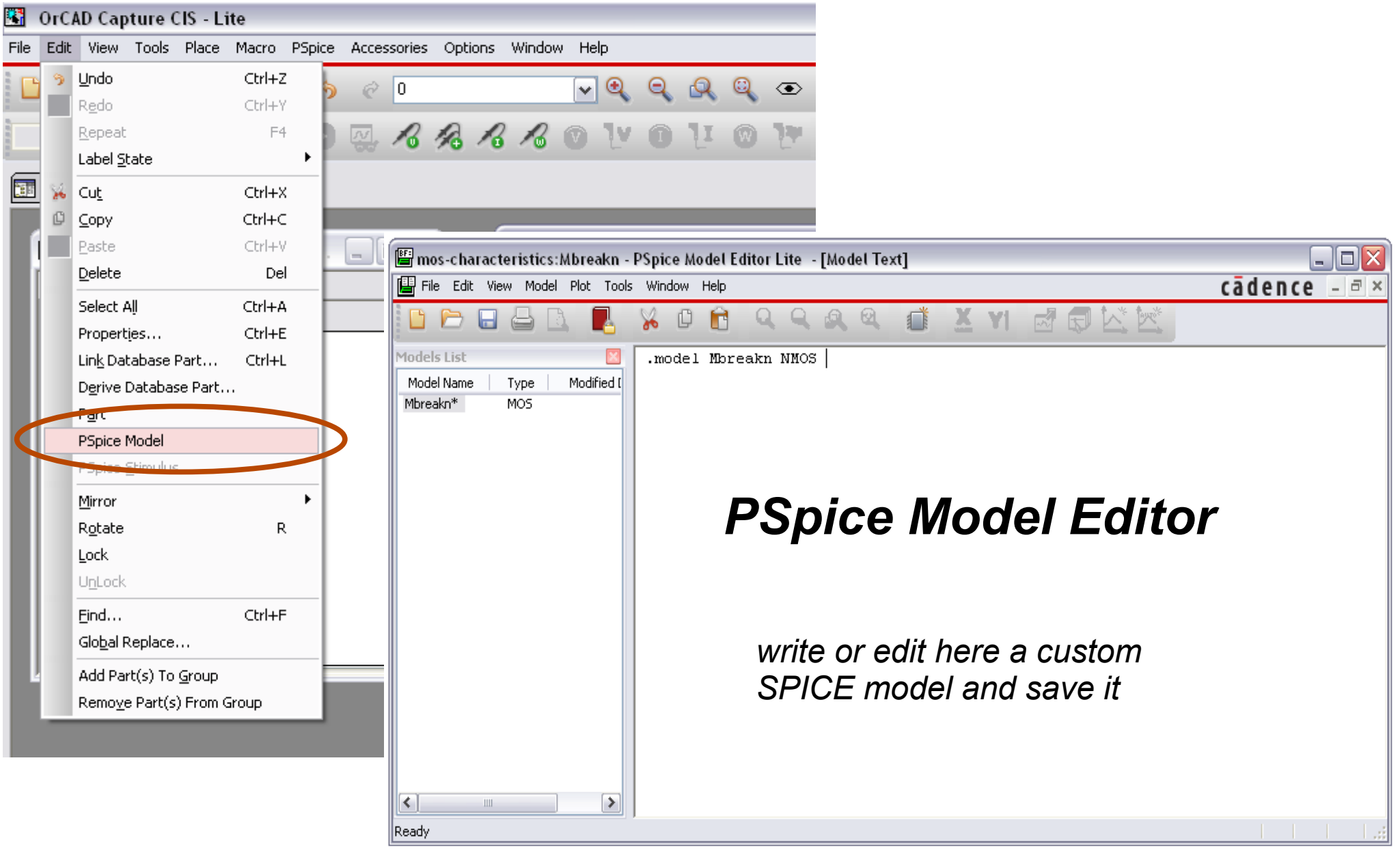
- the `LEVEL = 1` model maintains reasonable I-V accuracy for channel lengths as small as 4 μm

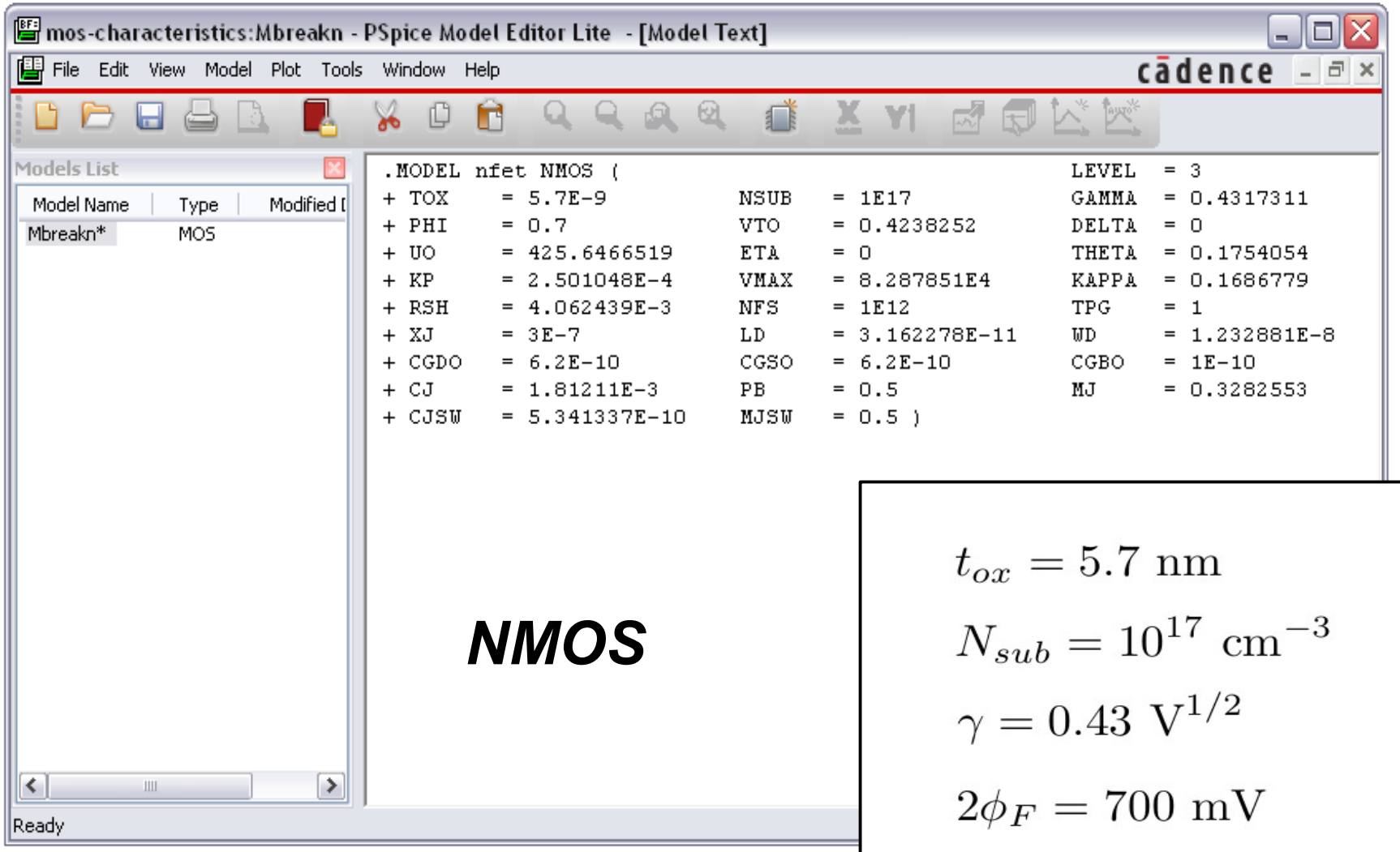
- ***high-order effects*** must be considered for more accurate simulations
  - the threshold voltage is not constant along the channel, neither for long-channel devices
  - sub-threshold conduction
  - the modelization of the channel-length modulation with only λ is far from accurate !

- ***empirical constants*** and ***parameterizations*** are introduced to improve the accuracy of models for short-channel devices (`L` < 1 μm)

- for more information see :
  - *B. Razavi,* ***Design of Analog CMOS Integrated Circuits****,* ch 16, pp. 591-599
  - ***PSpice Reference Guide****,* ch. 2 pp. 222-269

Edit SPICE models in PSpice





NMOS

$t_{ox} = 5.7 \text{ nm}$

$N_{sub} = 10^{17} \text{ cm}^{-3}$

$\gamma = 0.43 \text{ V}^{1/2}$

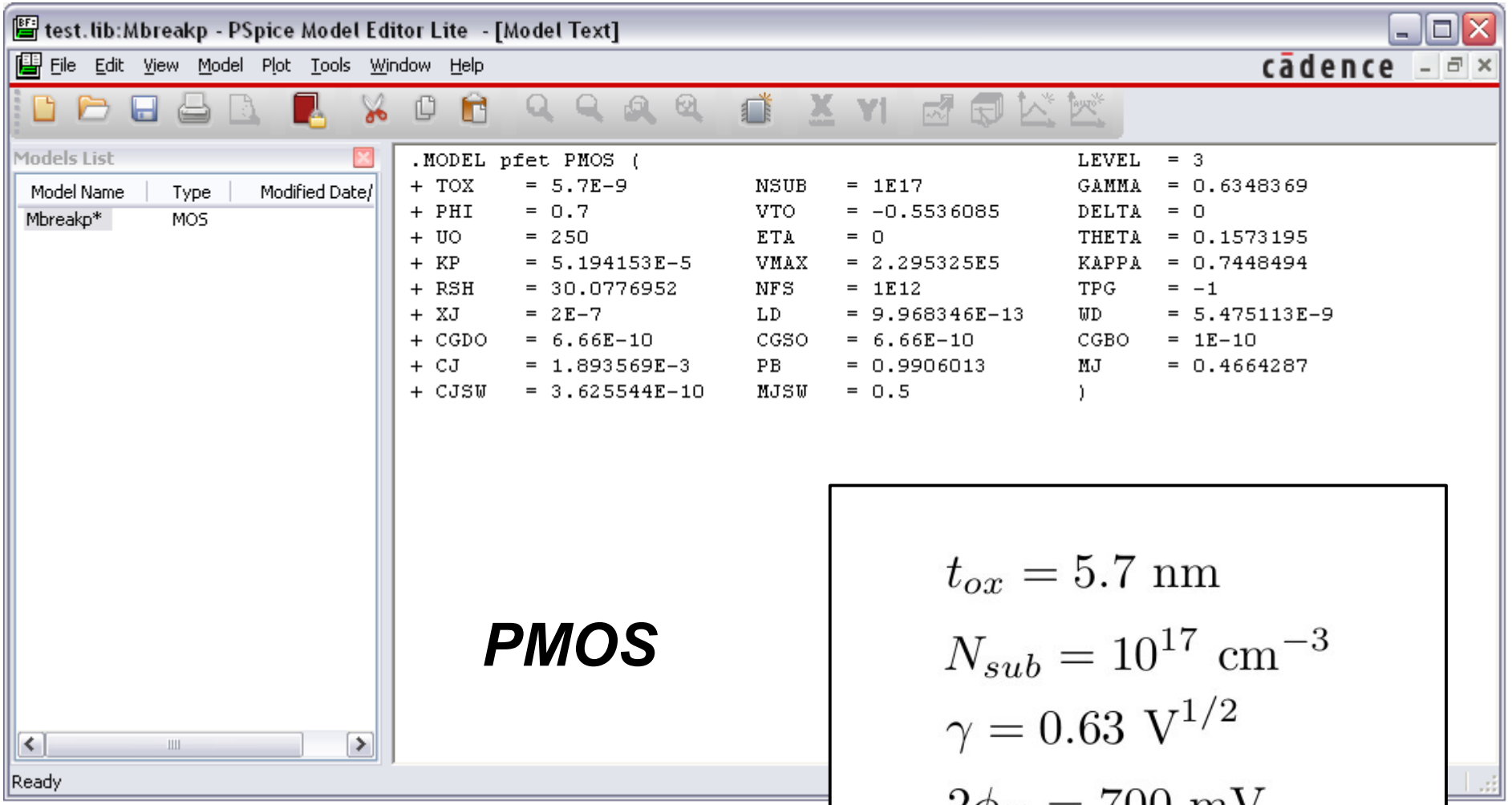
$2\phi_F = 700 \text{ mV}$

$V_{TH0} = 424 \text{ mV}$

$\mu_n = 426 \text{ cm}^2 \text{ / Vs}$

$\mu_n C_{ox} = 250 \ \mu\text{A} \ / \text{V}^2$

http://www.mosis.com/requests/test-data



PMOS

$$t_{ox} = 5.7 \text{ nm}$$

$$N_{sub} = 10^{17} \text{ cm}^{-3}$$

$$\gamma = 0.63 \text{ V}^{1/2}$$

$$2\phi_F = 700 \text{ mV}$$

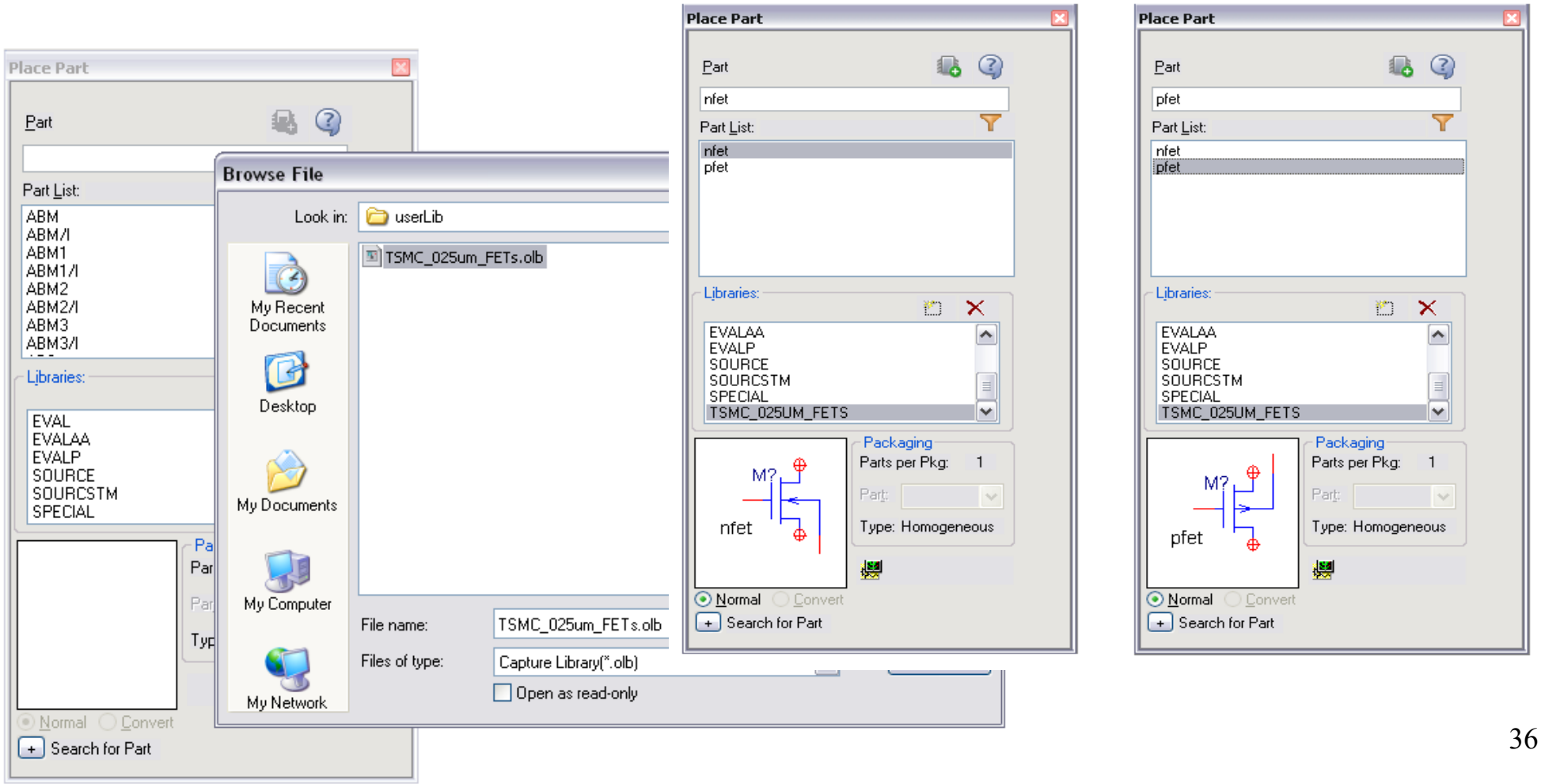
$$V_{TH0} = -554 \text{ mV}$$

$$\mu_p = 250 \text{ cm}^2 \text{ / Vs}$$

$$\mu_p C_{ox} = 52 \ \mu\text{A} \ /\text{V}^2$$

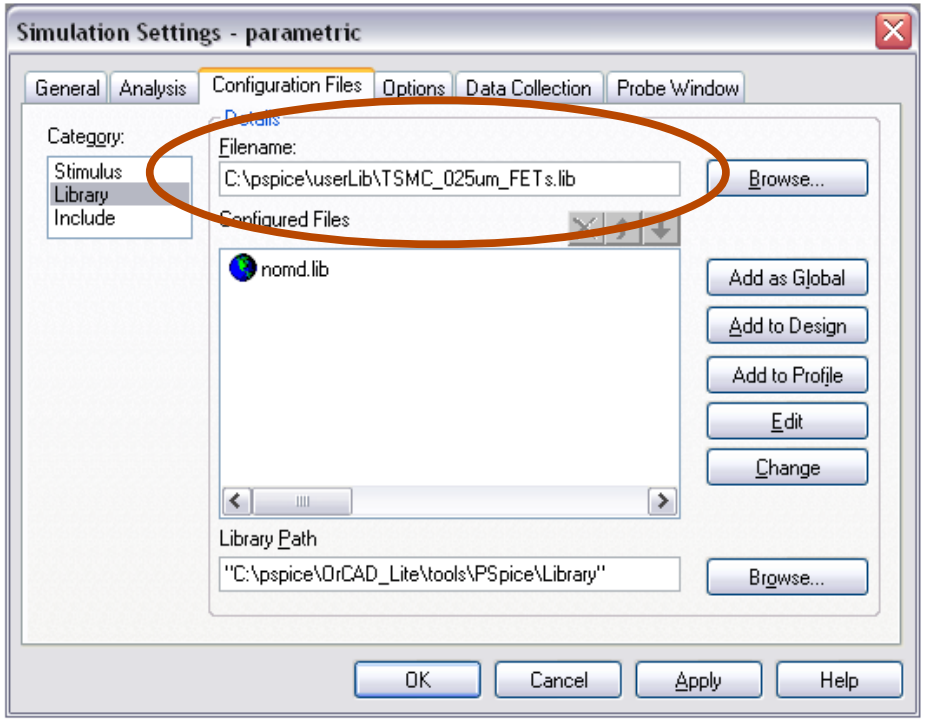
- NMOS and PMOS transistor symbols are defined in the **TSMC_025UM_FETS.olb** Capture library

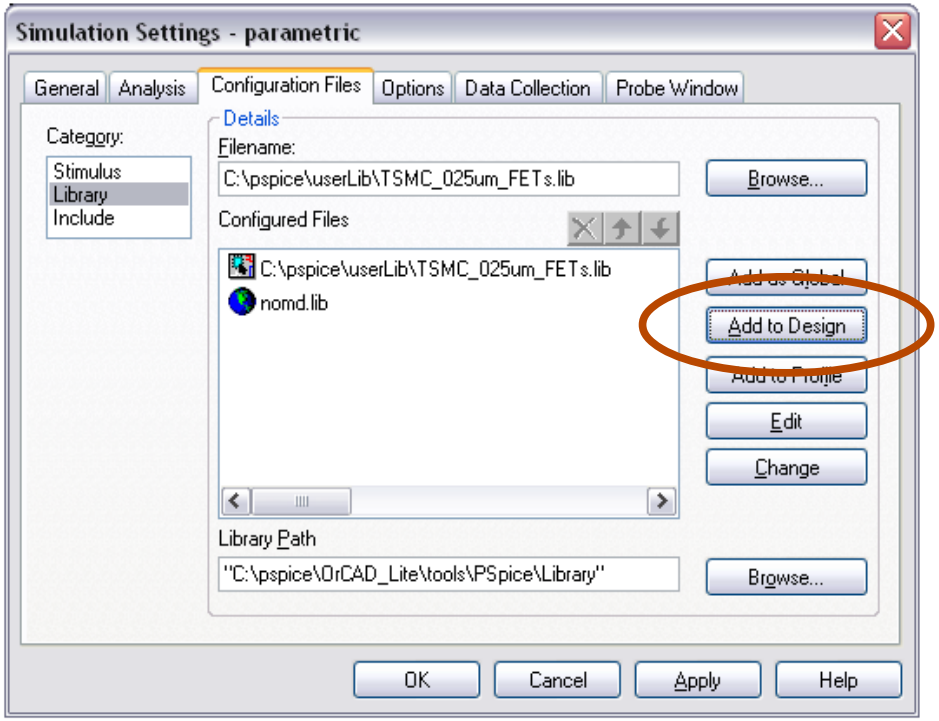
- add `C:\pspice\userLib\TSMC_025um_FETs\TSMC_025UM_FETS.olb` from the Place Part window (Ctrl + A)

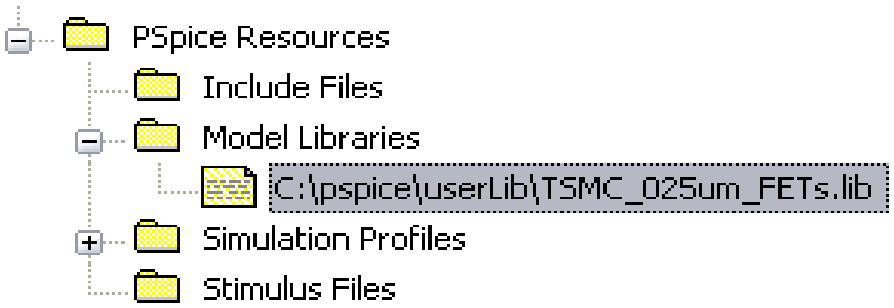


Including external PSpice libraries

Simulation Settings > Configuration Files > Category > Library







*In order to perform simulations, **custom** PSpice model libraries (.lib) must appear in the Project Manager window, in the **Model Libraries** folder*

More technicalities

- PSpice always performs a bias analysis, but ***detailed transistor parameters*** such as V_{TH} g_m g_{ds} etc. are available in the output file only if explicitly required by checking the ***Include detailed bias point information for non linear controlled sources and semiconductors (.OP)*** option (select *Output File Options* if a *Time Domain (Transient)* analysis is performed)

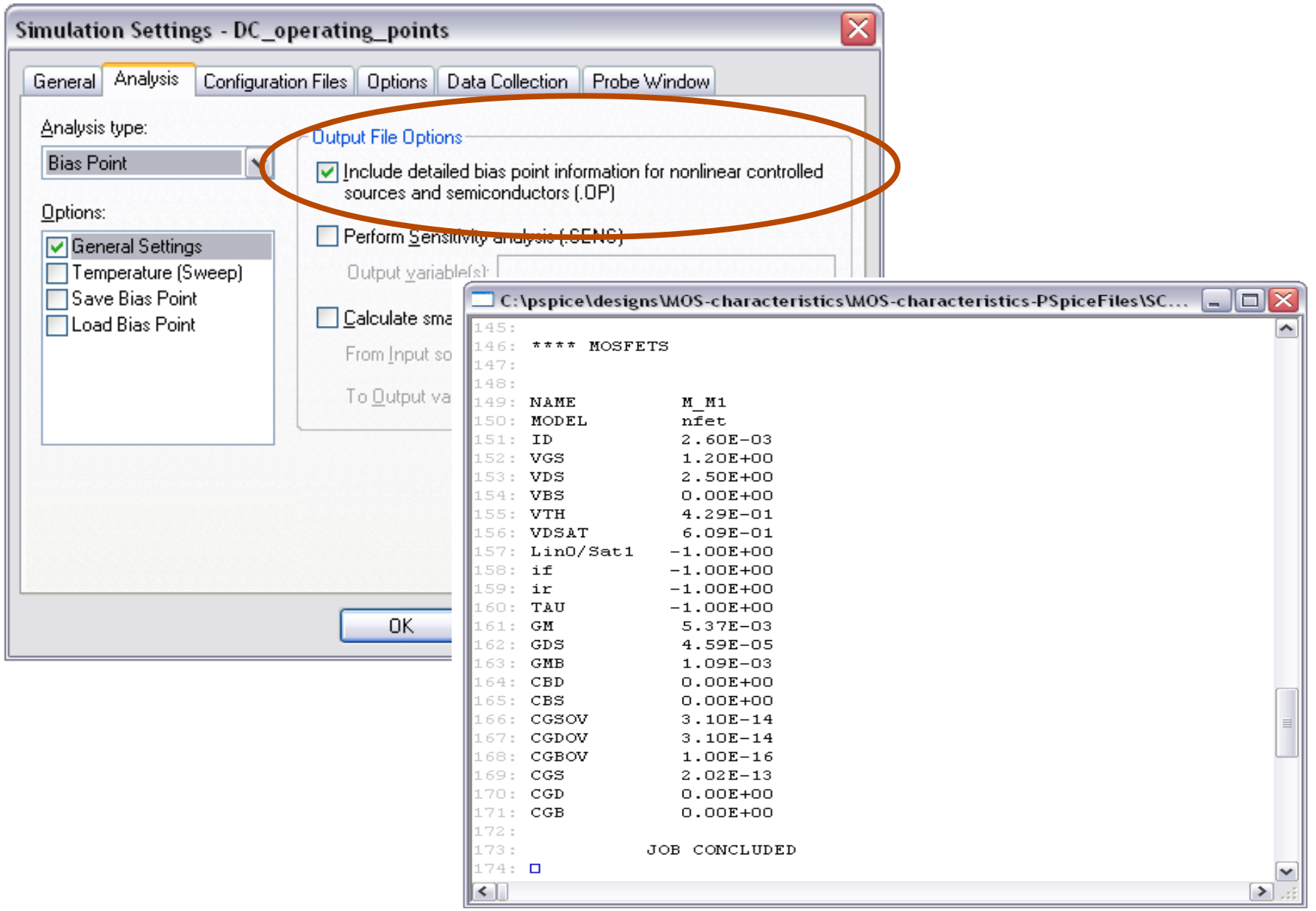
- some transistor defaults can be modified through

  Simulation Settings > Options > Analog Simulation > MOSFET Options

- ***global parameters*** and ***mathematical expressions*** are identified with braces { }

- add global parameters to **SPECIAL /PARAM** instances

DC operating point details (1)



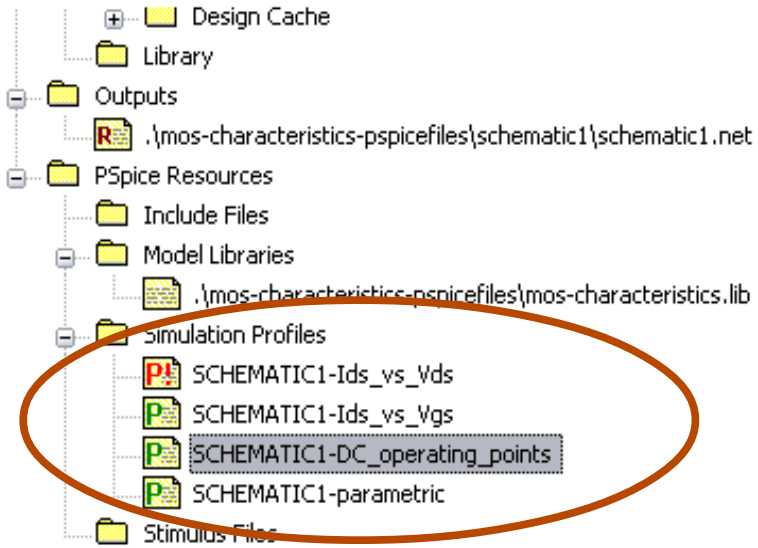
DC operating point details (2)

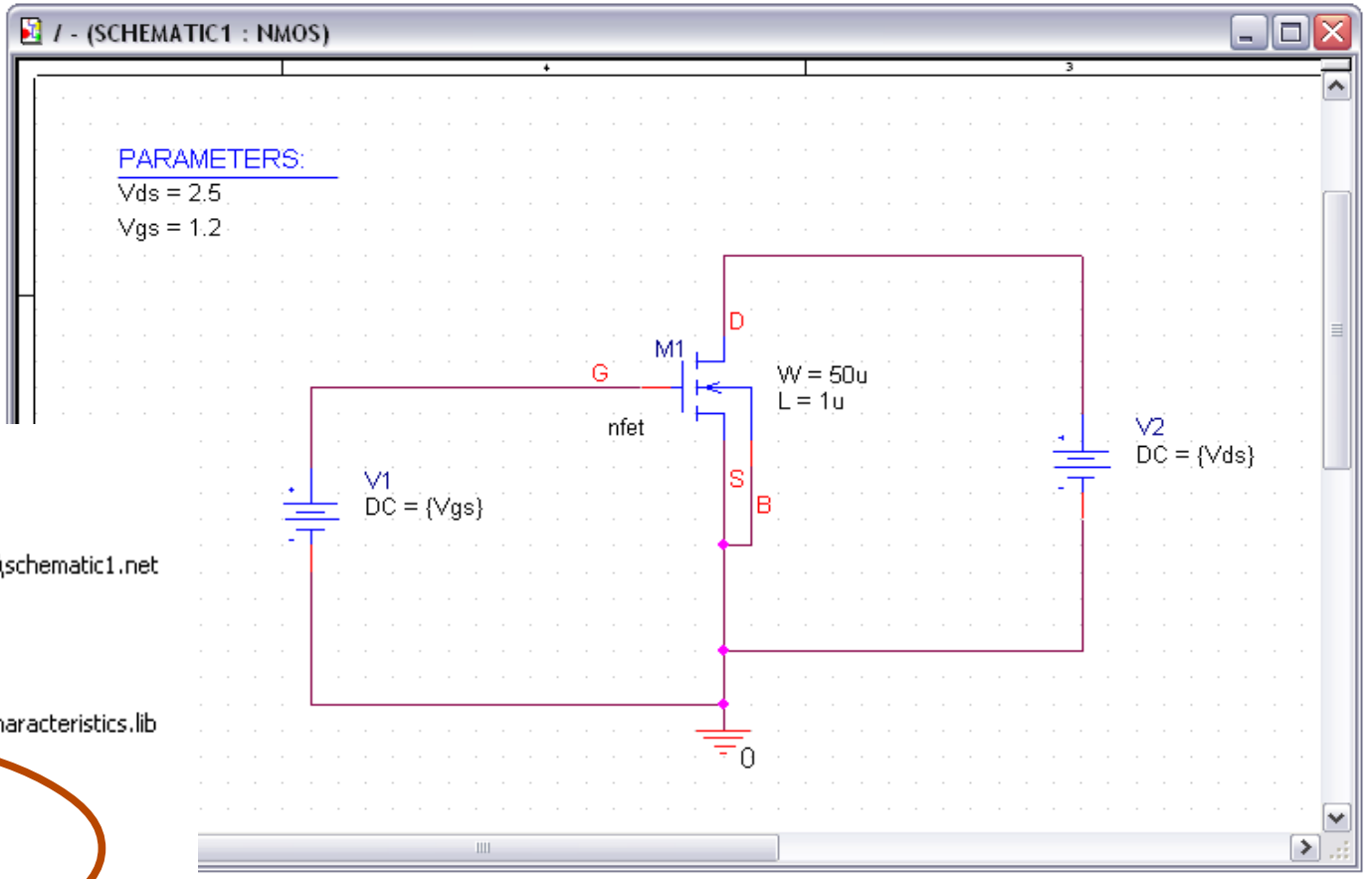
.out file MOS parameter	description	unit
ID	drain current	**A**
VGS	gate-source voltage	**V**
VDS	drain-source voltage	**V**
VBS	bulk-source voltage	**V**
VTH	threshold voltage (with body-effect)	**V**
VDSAT	saturation voltage	**V**
Lin0/Sat1[1]	operating region	-
if[1]	-	-
ir[1]	-	-
TAU[1]	drain current time delay with respect to changes in the gate voltage	**sec**
GM	transconductance	**S**
GDS	output conductance (ro = 1/GDS)	**S**
GMB	bulk-effect transconductance	**S**

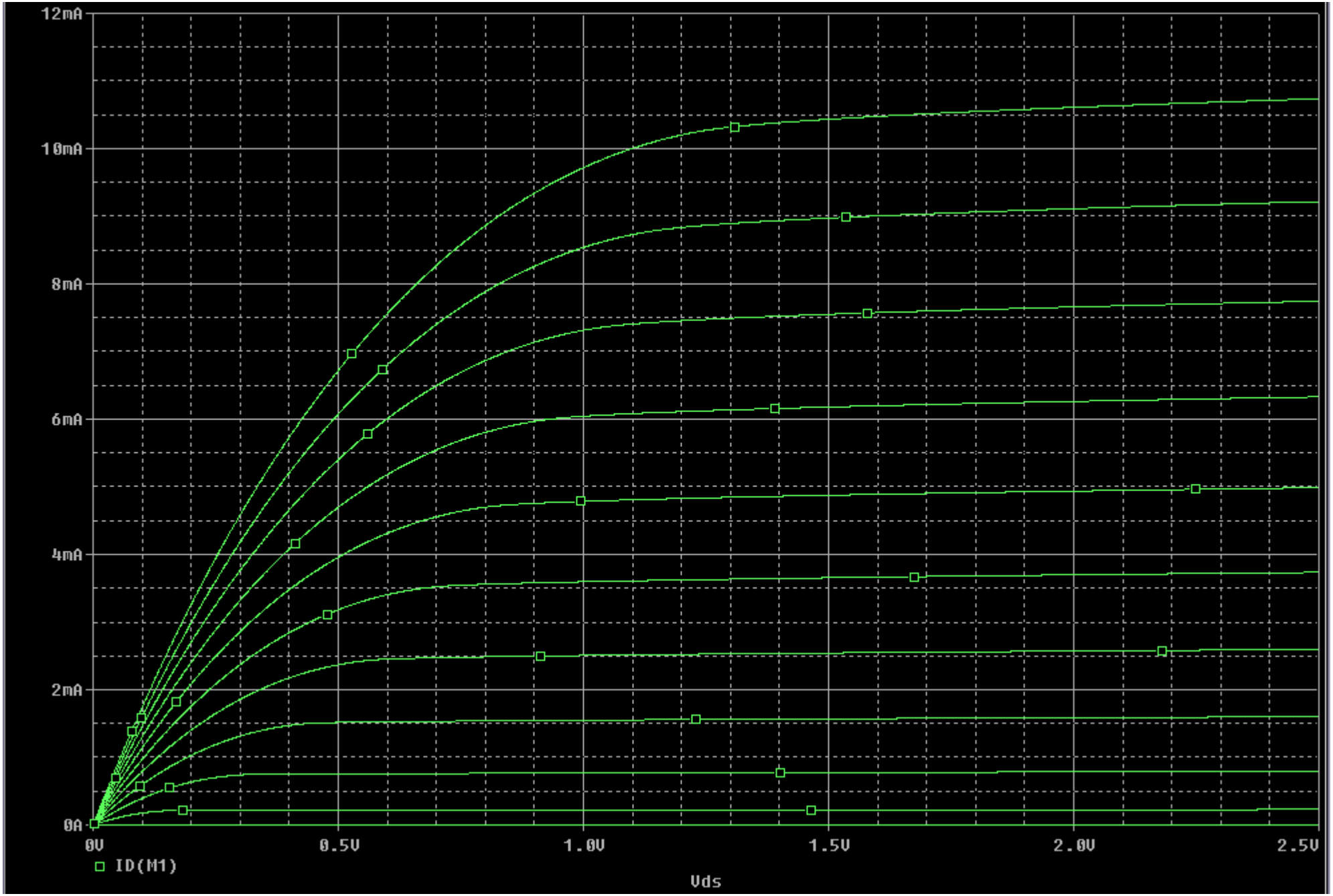
[1] meaningless for LEVEL = 1, 2, 3

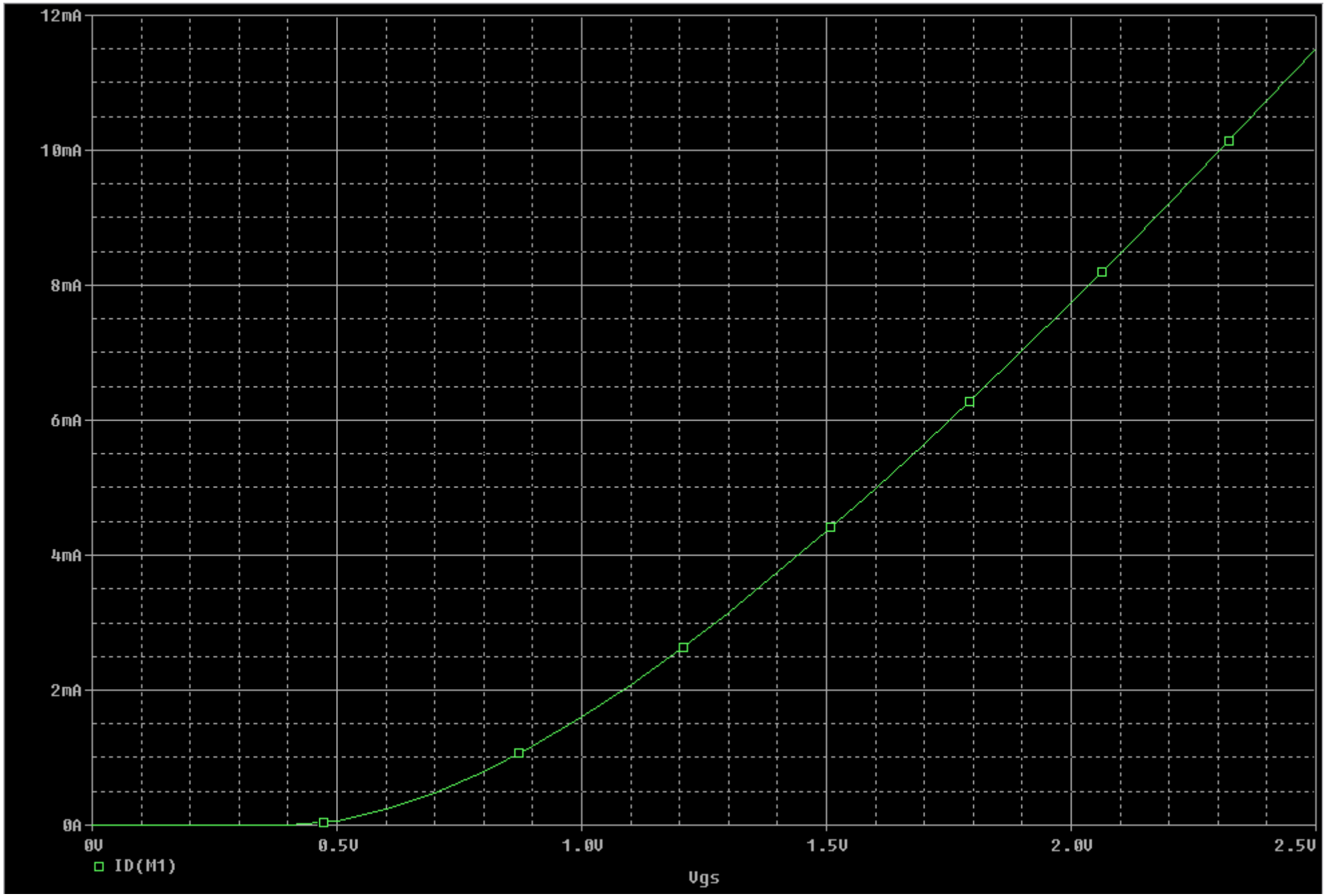
Capture shortcut	description
P	place part
Ctrl + A	add library
G	place ground
F	place power
Ctrl + E	edit component properties
W	place wire
N	place net alias
J	place junction
ESC	end mode
R	rotate component
H / V	mirror horizontally/vertically
T	place text
I /O or **Ctrl + rolling**	zoom in/out
rolling	scroll up/down
Shift + rolling	scroll left/right
Ctrl + X / Ctrl + V	cut/paste
DEL, **CANC**	delete component

Ex. 1 – NMOS characteristics

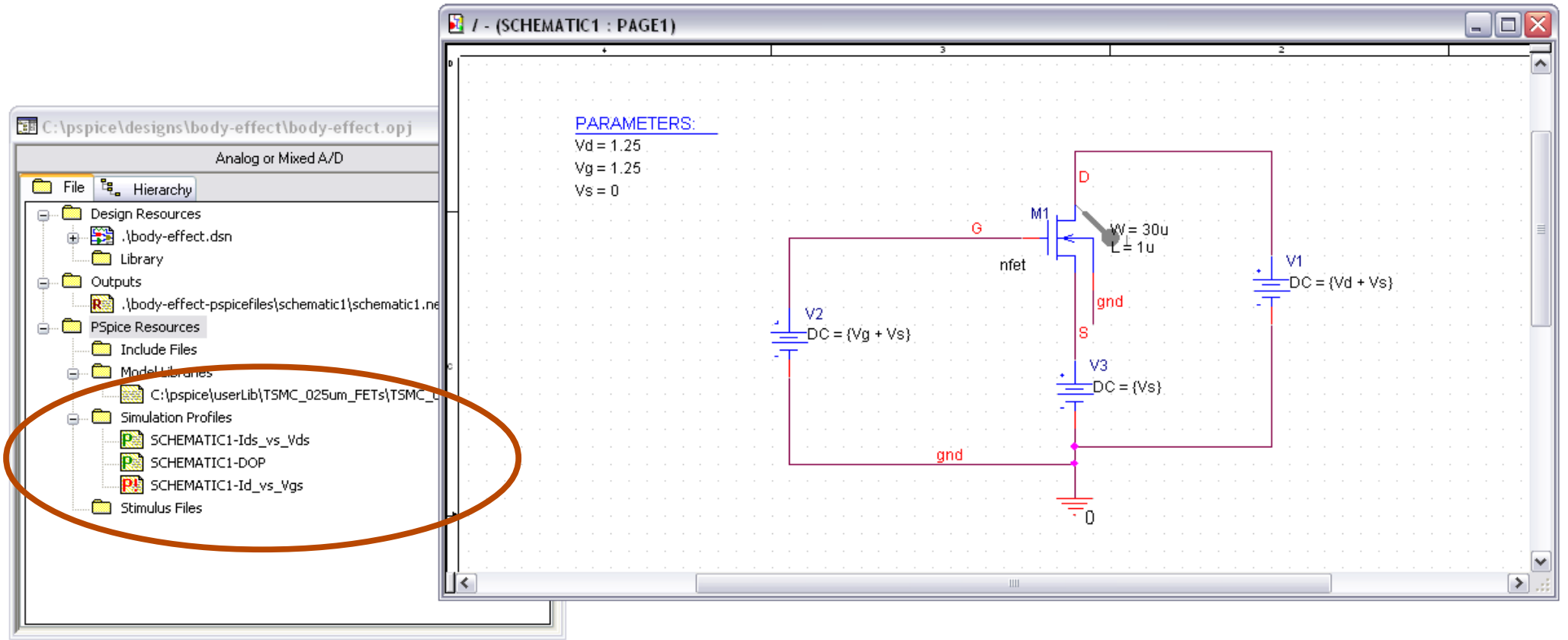


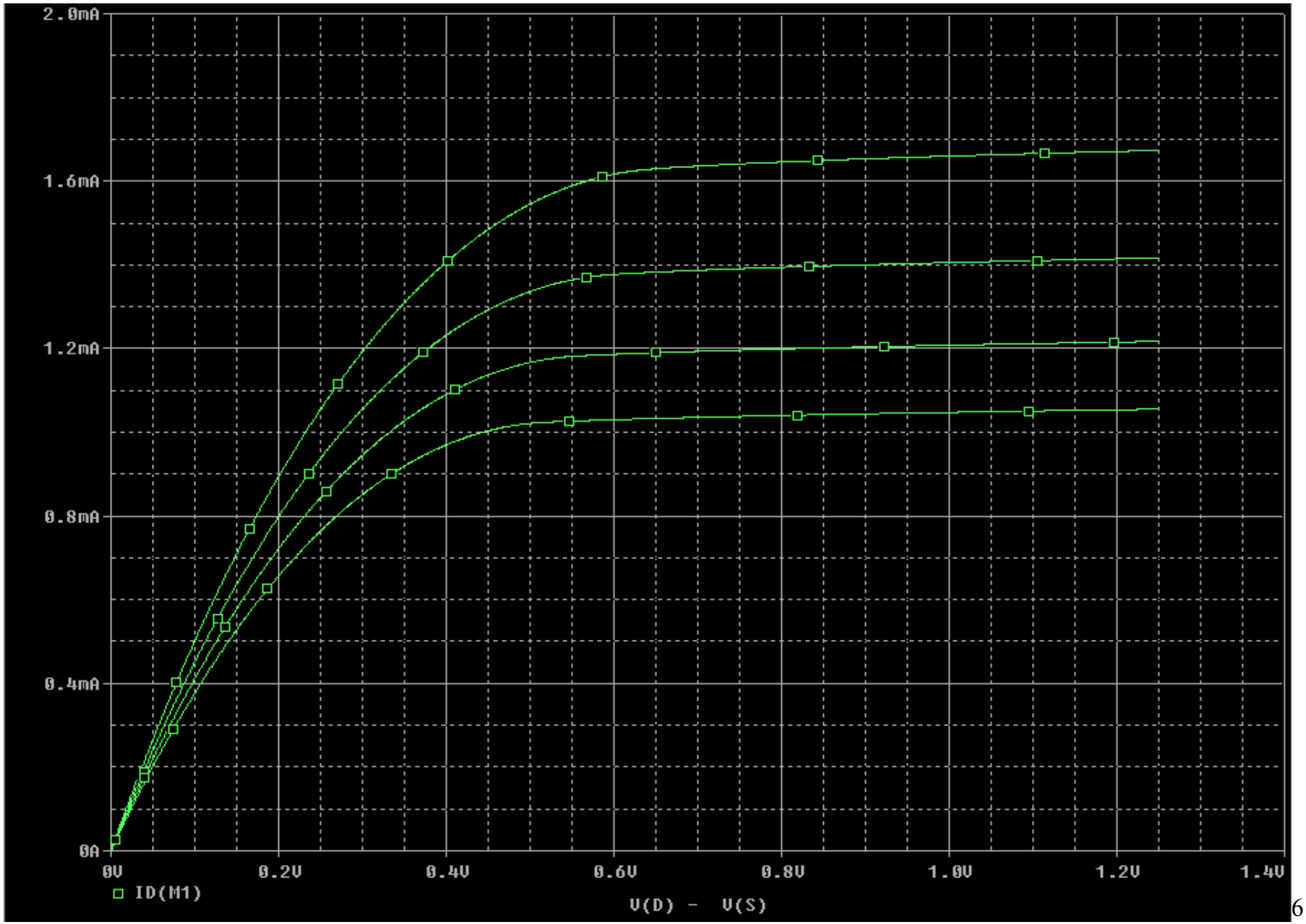


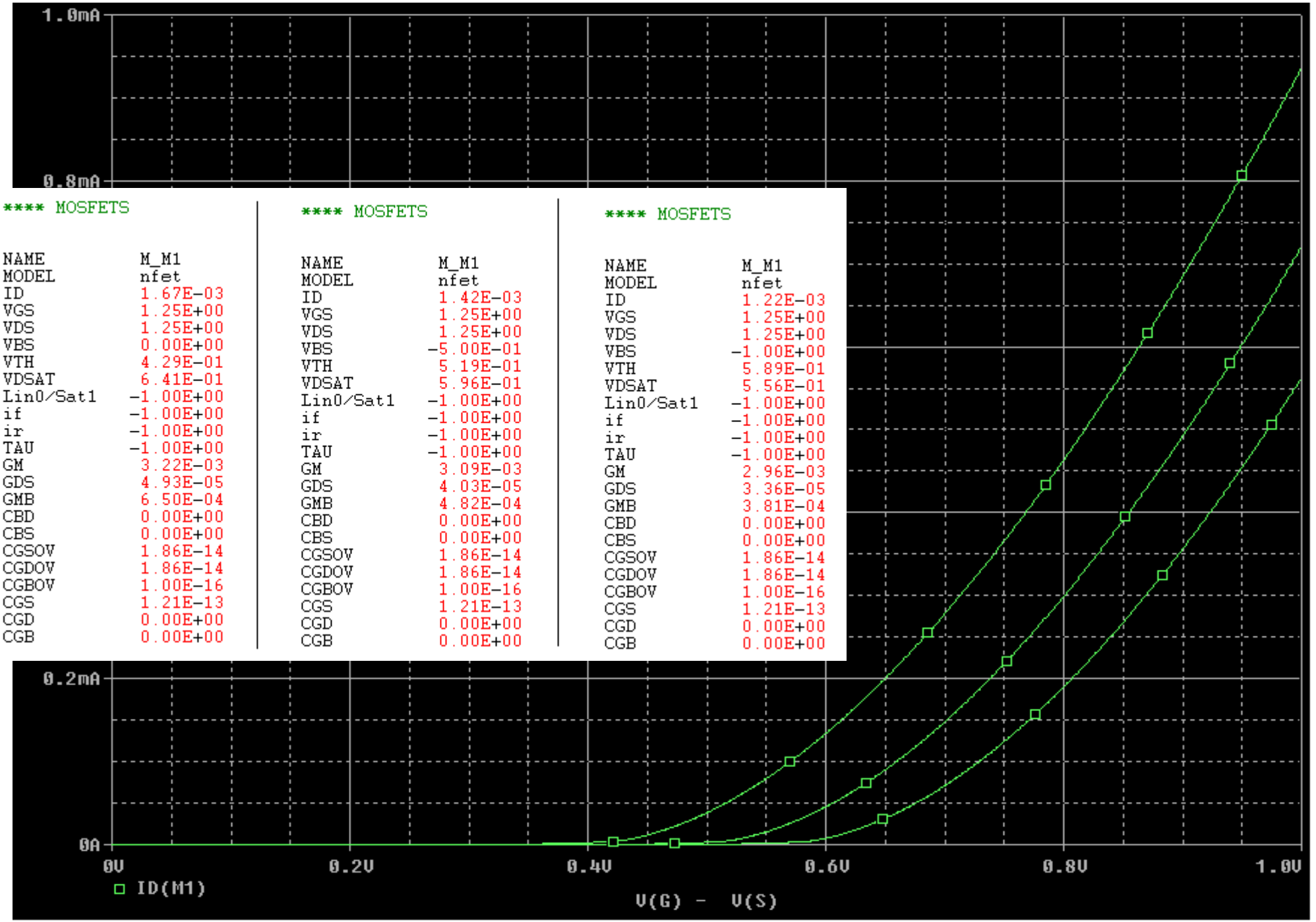

12mA
10mA
8mA
6mA
4mA
2mA
0A
0V
0.5V
1.0V
1.5V
2.0V
2.5V
ID(M1)
Vds


12mA
10mA
8mA
6mA
4mA
2mA
0A
0V
0.5V
1.0V
1.5V
2.0V
2.5V
ID(M1)
Vgs

Ex. 2 – Body effect




2.0mA
1.6mA
1.2mA
0.8mA
0.4mA
0A
0V
0.2V
0.4V
0.6V
0.8V
1.0V
1.2V
1.4V
ID(M1)
V(D) - V(S)



**** MOSFETS

NAME	M_M1
MODEL	nfet
ID	1.67E-03
VGS	1.25E+00
VDS	1.25E+00
VBS	0.00E+00
VTH	4.29E-01
VDSAT	6.41E-01
Lin0/Sat1	-1.00E+00
if	-1.00E+00
ir	-1.00E+00
TAU	-1.00E+00
GM	3.22E-03
GDS	4.93E-05
GMB	6.50E-04
CBD	0.00E+00
CBS	0.00E+00
CGSOV	1.86E-14
CGDOV	1.86E-14
CGBOV	1.00E-16
CGS	1.21E-13
CGD	0.00E+00
CGB	0.00E+00

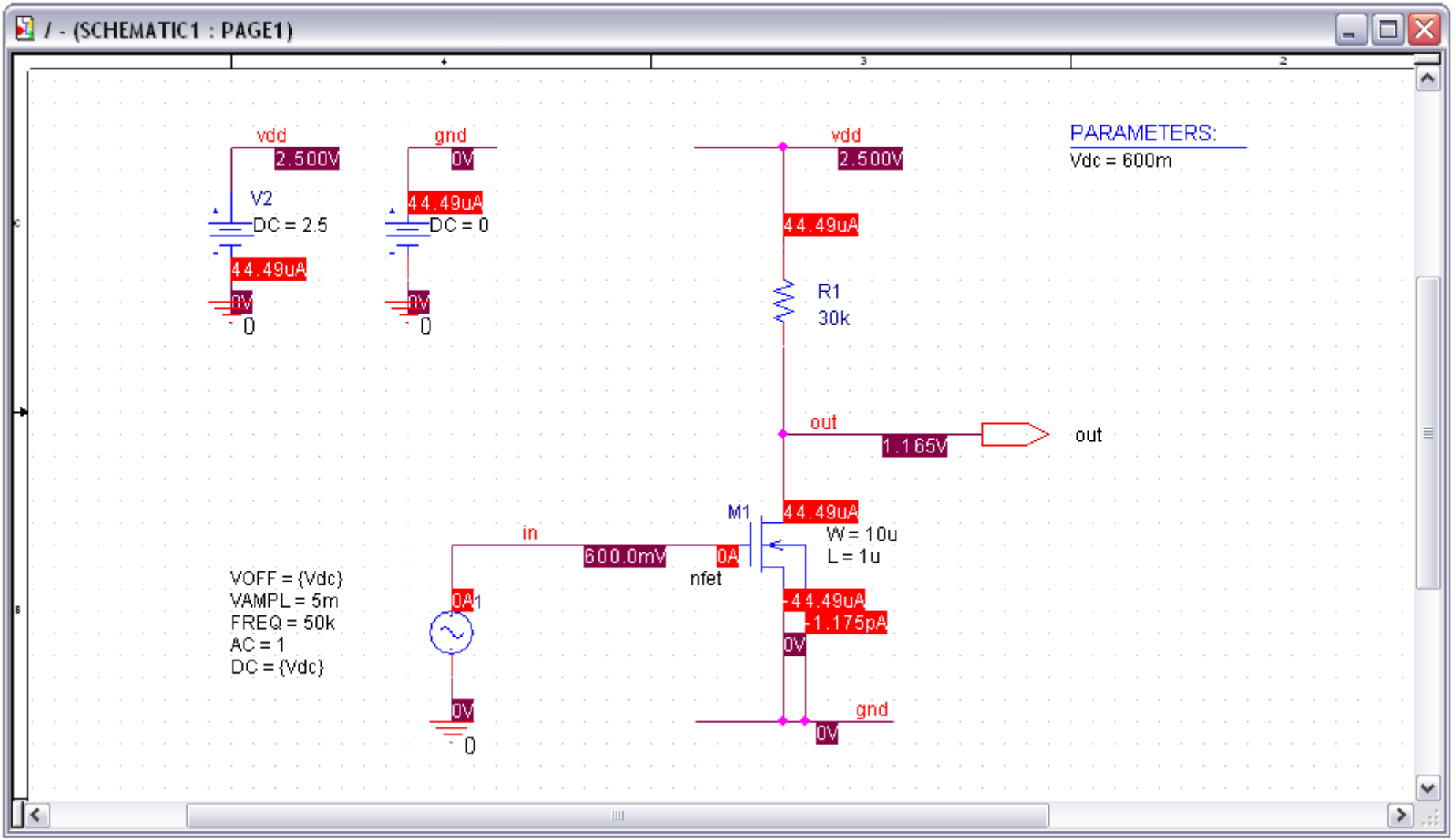
**** MOSFETS

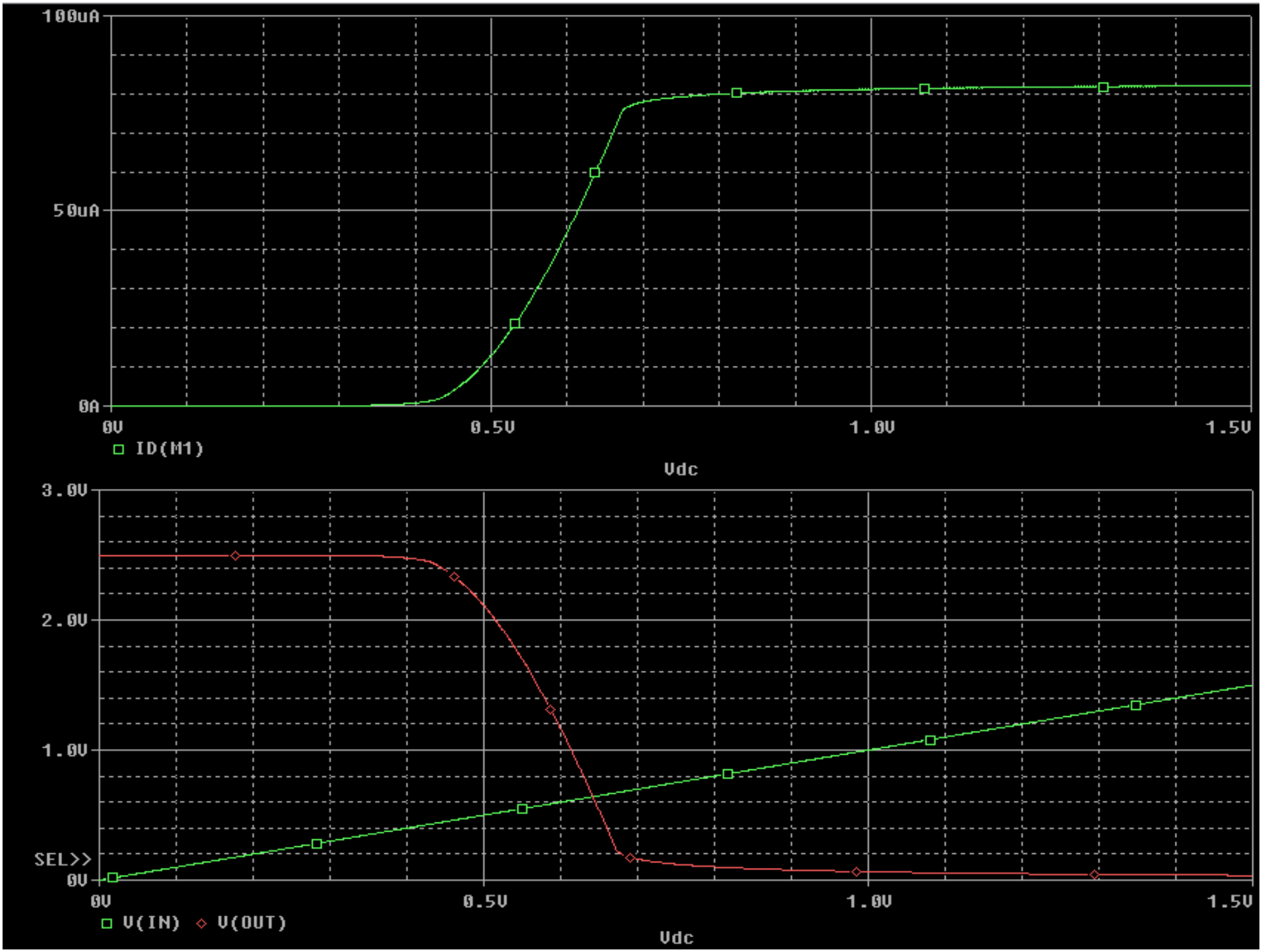
NAME	M_M1
MODEL	nfet
ID	1.42E-03
VGS	1.25E+00
VDS	1.25E+00
VBS	-5.00E-01
VTH	5.19E-01
VDSAT	5.96E-01
Lin0/Sat1	-1.00E+00
if	-1.00E+00
ir	-1.00E+00
TAU	-1.00E+00
GM	3.09E-03
GDS	4.03E-05
GMB	4.82E-04
CBD	0.00E+00
CBS	0.00E+00
CGSOV	1.86E-14
CGDOV	1.86E-14
CGBOV	1.00E-16
CGS	1.21E-13
CGD	0.00E+00
CGB	0.00E+00

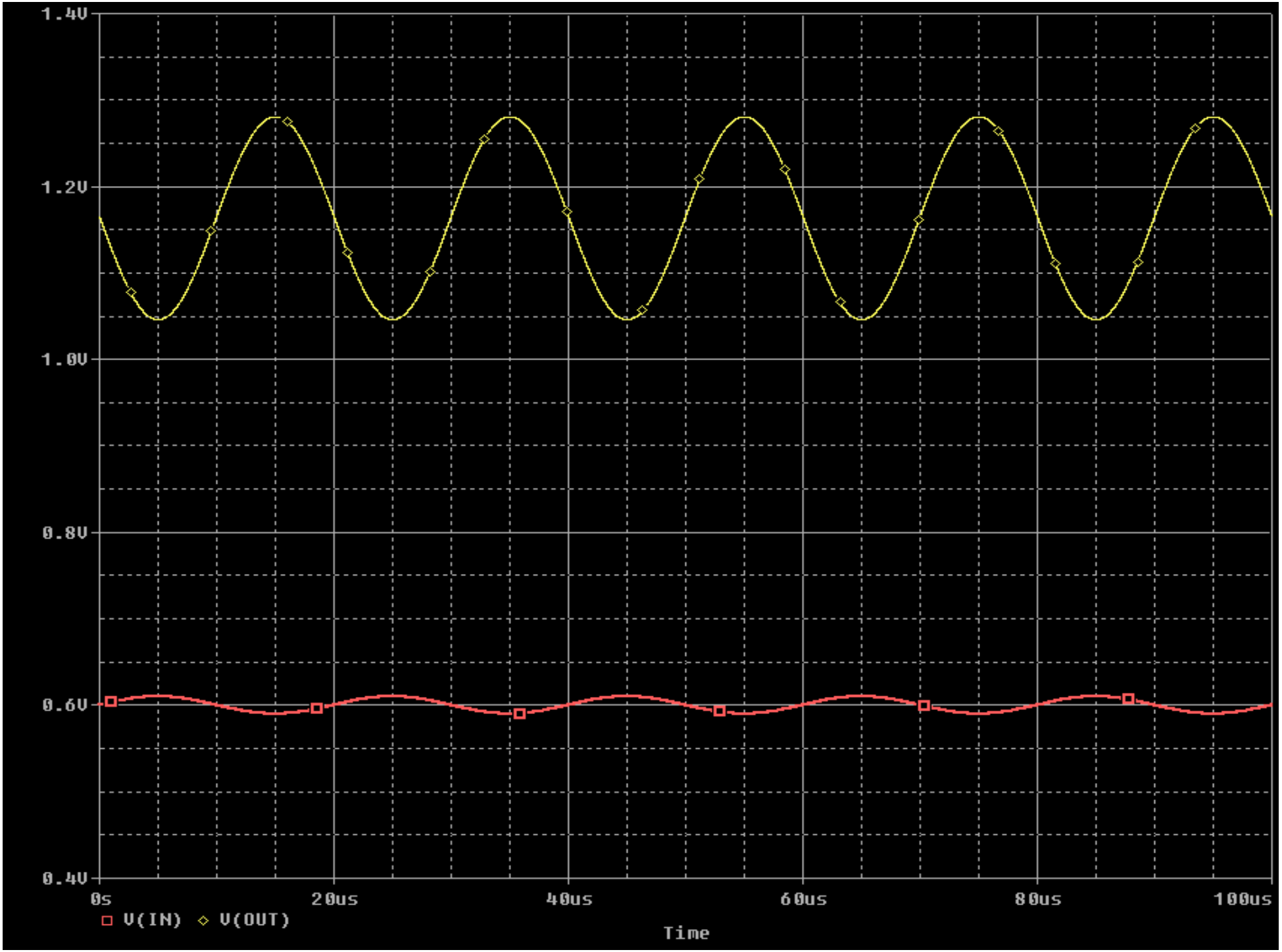
**** MOSFETS

NAME	M_M1
MODEL	nfet
ID	1.22E-03
VGS	1.25E+00
VDS	1.25E+00
VBS	-1.00E+00
VTH	5.89E-01
VDSAT	5.56E-01
Lin0/Sat1	-1.00E+00
if	-1.00E+00
ir	-1.00E+00
TAU	-1.00E+00
GM	2.96E-03
GDS	3.36E-05
GMB	3.81E-04
CBD	0.00E+00
CBS	0.00E+00
CGSOV	1.86E-14
CGDOV	1.86E-14
CGBOV	1.00E-16
CGS	1.21E-13
CGD	0.00E+00
CGB	0.00E+00

Ex. 3 – Basic common source




100uA
50uA
0A
0V
0.5V
1.0V
1.5V
ID(M1)
Vdc
3.0V
2.0V
1.0V
SEL>>
0V
0V
0.5V
1.0V
1.5V
V(IN)
V(OUT)
Vdc


1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0s
20us
40us
60us
80us
100us
V(IN)
V(OUT)
Time

```
**** MOSFETS


NAME            M_M1
MODEL           nfet
ID               4.45E-05
VGS              6.00E-01
VDS              1.17E+00
VBS              0.00E+00
VTH              4.29E-01
VDSAT            1.79E-01
Lin0/Sat1       -1.00E+00
if              -1.00E+00
ir              -1.00E+00
TAU             -1.00E+00
GM               4.02E-04
GDS              9.28E-07
GMB              8.54E-05
CBD              0.00E+00
CBS              0.00E+00
CGSOV            6.18E-15
CGDOV            6.18E-15
CGBOV            1.00E-16
CGS              4.03E-14
CGD              0.00E+00
CGB              0.00E+00
```

$$A_V = -g_m \frac{r_o R_D}{r_o + R_D} \approx -g_m R_D$$

$$R_D = 30 \text{ k}\Omega$$

$$g_m = 402 \ \mu\text{S}$$

$$g_{ds} = 0.928 \ \mu\text{S}$$

$$r_o = \frac{1}{g_{ds}} \approx 1 \text{ M}\Omega$$

$$|A_{V,sim}| = \frac{234 \text{ mV } pk\text{-}pk}{20 \text{ mV } pk\text{-}pk} = 11.7$$

$$|A_{V,exp}| = 402 \times 10^{-6} \frac{30 \times 10^3 \ 10^6}{(30 + 10^3)10^3} = 11.7$$

Laplace theory - refresh

$$F(s) = \int_0^\infty dt\ f(t)\, e^{-st} \qquad s = \sigma + j\omega$$

Capacitor :

$$i_C(t) = \frac{dq(t)}{dt} = C\frac{dv_C(t)}{dt}$$

$$v_C(t) = \frac{1}{C}\int_{-\infty}^{t} i_C(t')dt'$$

$$Z_C(s) = \frac{1}{sC} = \underbrace{\frac{1}{j\omega C}}$$

sinusoidal waveforms

Inductor :

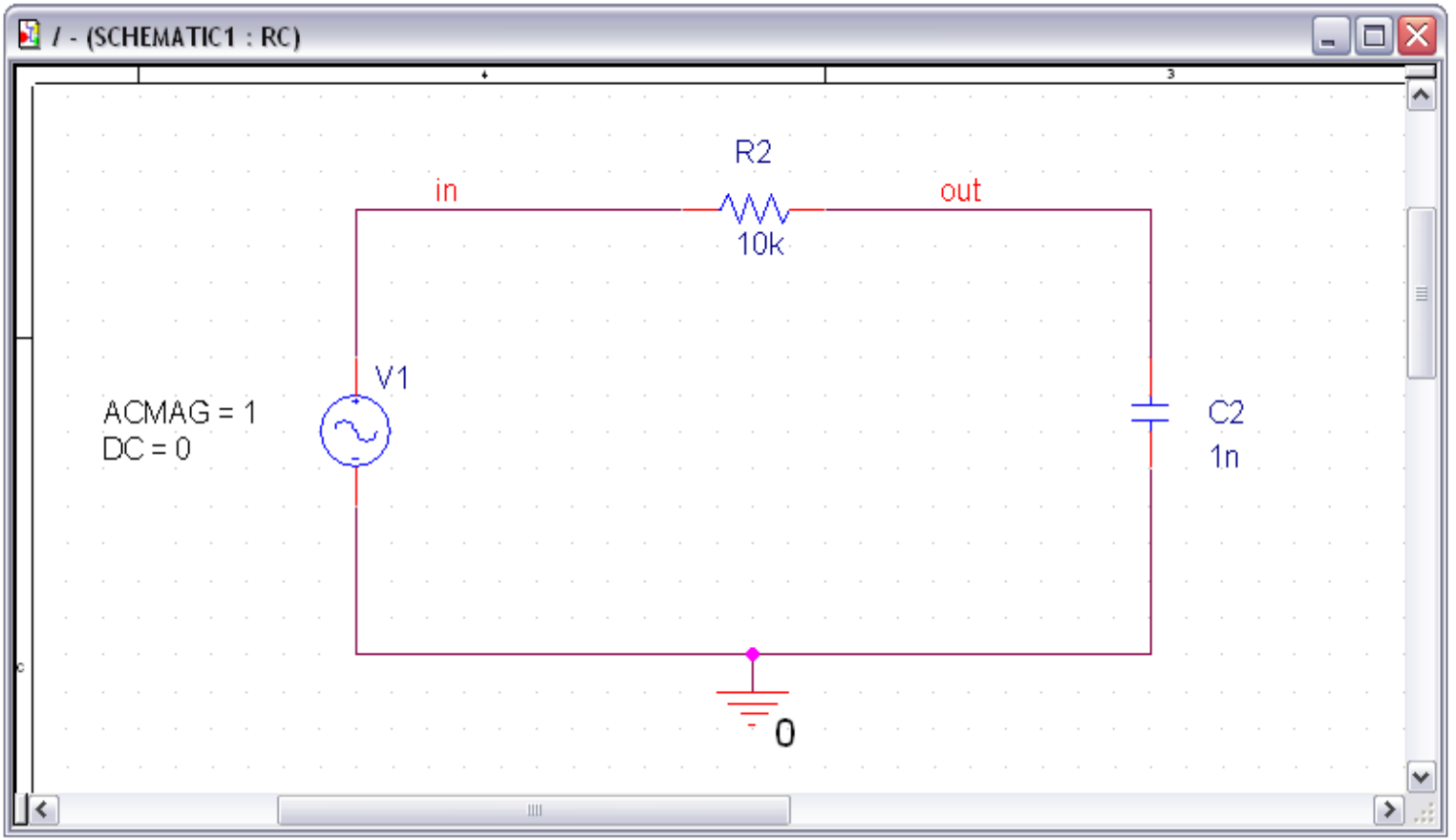
$$i_L(t) = \frac{1}{L}\int_{-\infty}^{t} v_L(t')dt'$$

$$v_L(t) = L\frac{di_L(t)}{dt}$$

$$Z_L(s) = sL = \underbrace{j\omega L}$$

sinusoidal waveforms

Ex. 4 – RC frequency analysis



$$V_{out}(s) = \frac{V_{in}(s)}{R + 1/sC}\ 1/sC$$

$$\boxed{\frac{V_{out}(s)}{V_{in}(s)} = H(s) = \frac{1}{1 + sRC}}$$

Voltage magnitude and phase

$$H(j\omega) = \frac{1}{1 + j\omega RC} = |H(j\omega)|\, e^{j\phi(\omega)}$$

$$|H(j\omega)| = \frac{1}{\sqrt{1 + \omega^2 R^2 C^2}} = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_L}\right)^2}} \qquad RC = \frac{1}{\omega_L} = \frac{1}{2\pi f_L}$$

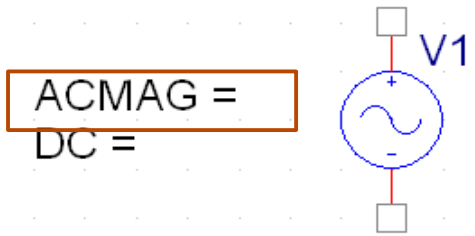
$$f_L = \frac{1}{2\pi RC}$$

cut-off frequency

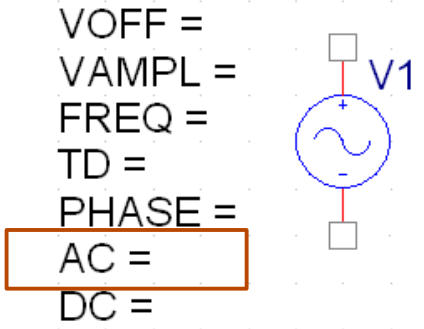
$$|H(j\omega)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_L}\right)^2}}$$

$$\phi(\omega) = -\arctan(\omega RC) = -\arctan\left(\frac{f}{f_L}\right)$$

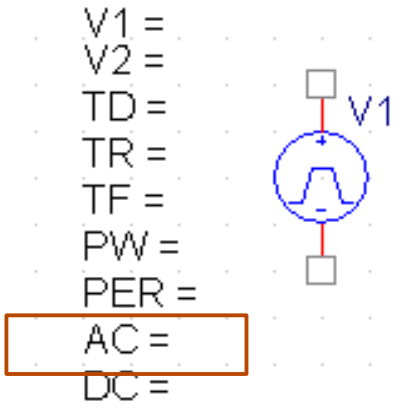
AC sources and markers



SOURCE /VAC



SOURCE /VSIN

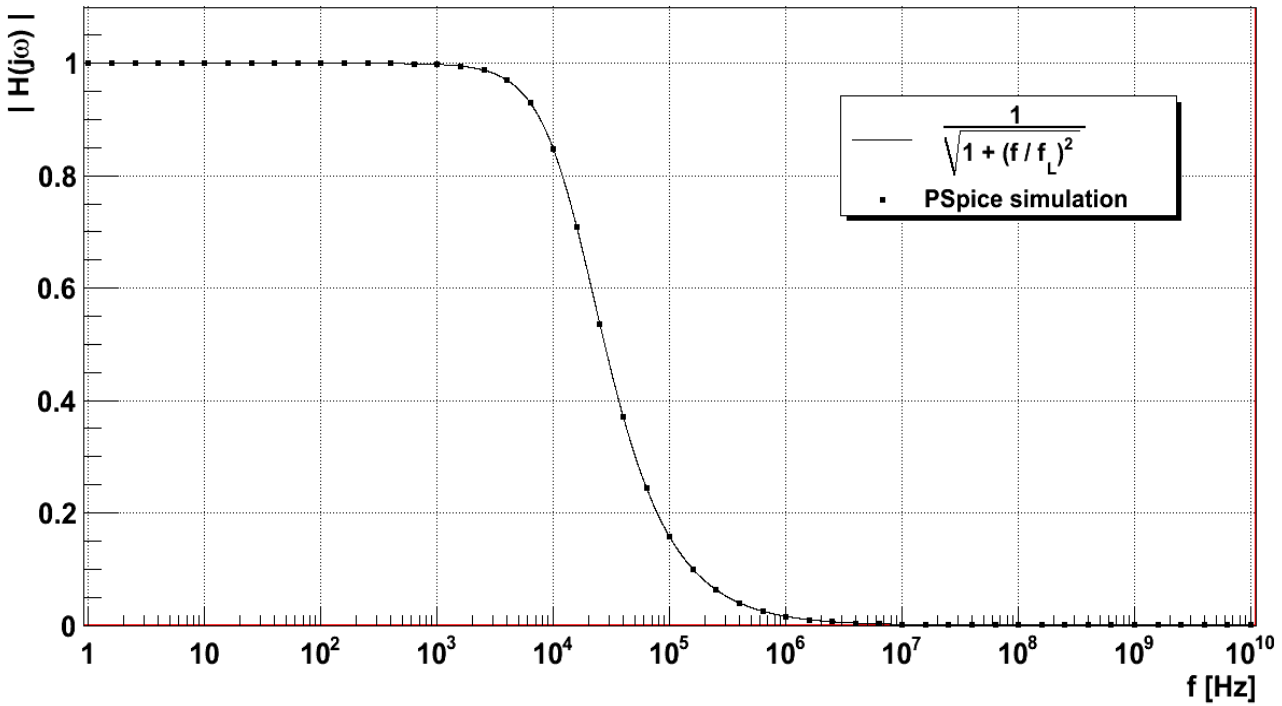


SOURCE /VPULSE

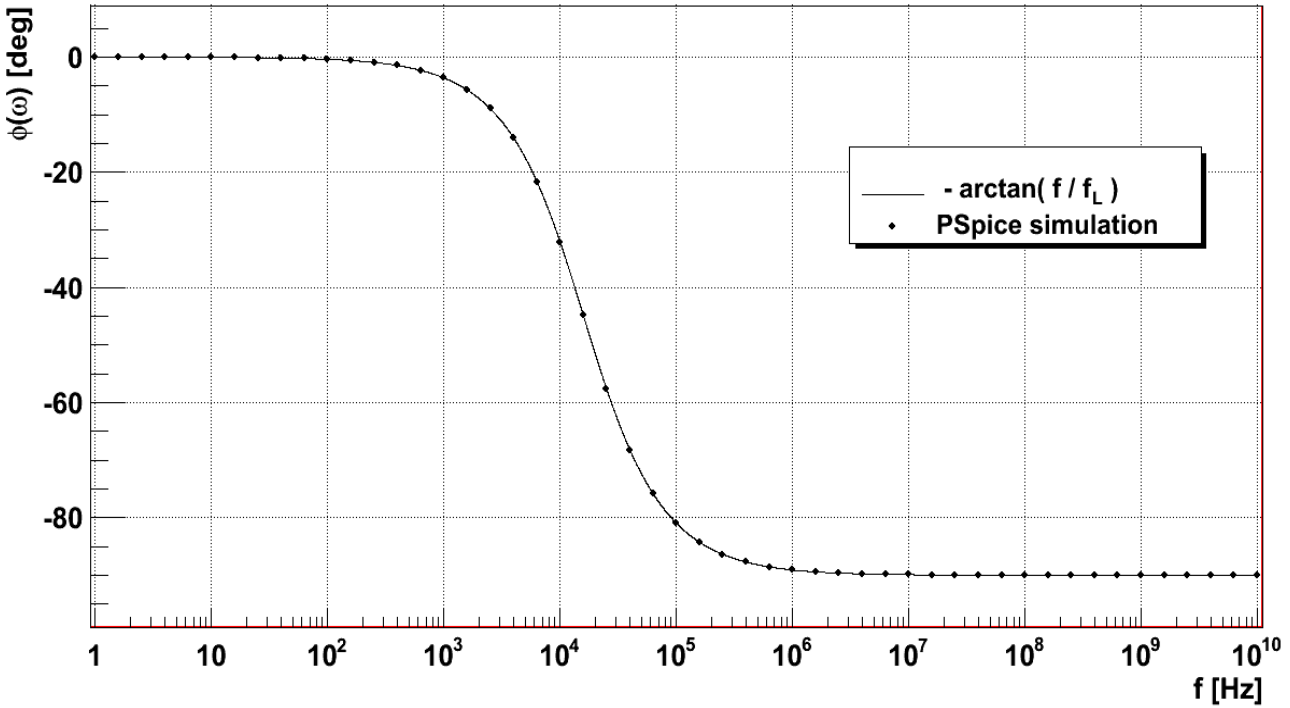
- all independent voltage and current sources that have ***AC specifications*** are inputs to the circuit, e.g. VAC and IAC
- the best way to use AC sweep analysis is ***to set the source magnitude to one***, (e.g. ACMAG = 1) in this way ***the measured output equals the gain***, relative to the input source, at that output
- outputs voltages and currents with ***magnitude*** and ***phase*** can be plotted using special markers :

PSpice > Markers > Advanced > dB Magnitude of Voltage (Current)
Phase of Voltage (Current)

magnitude



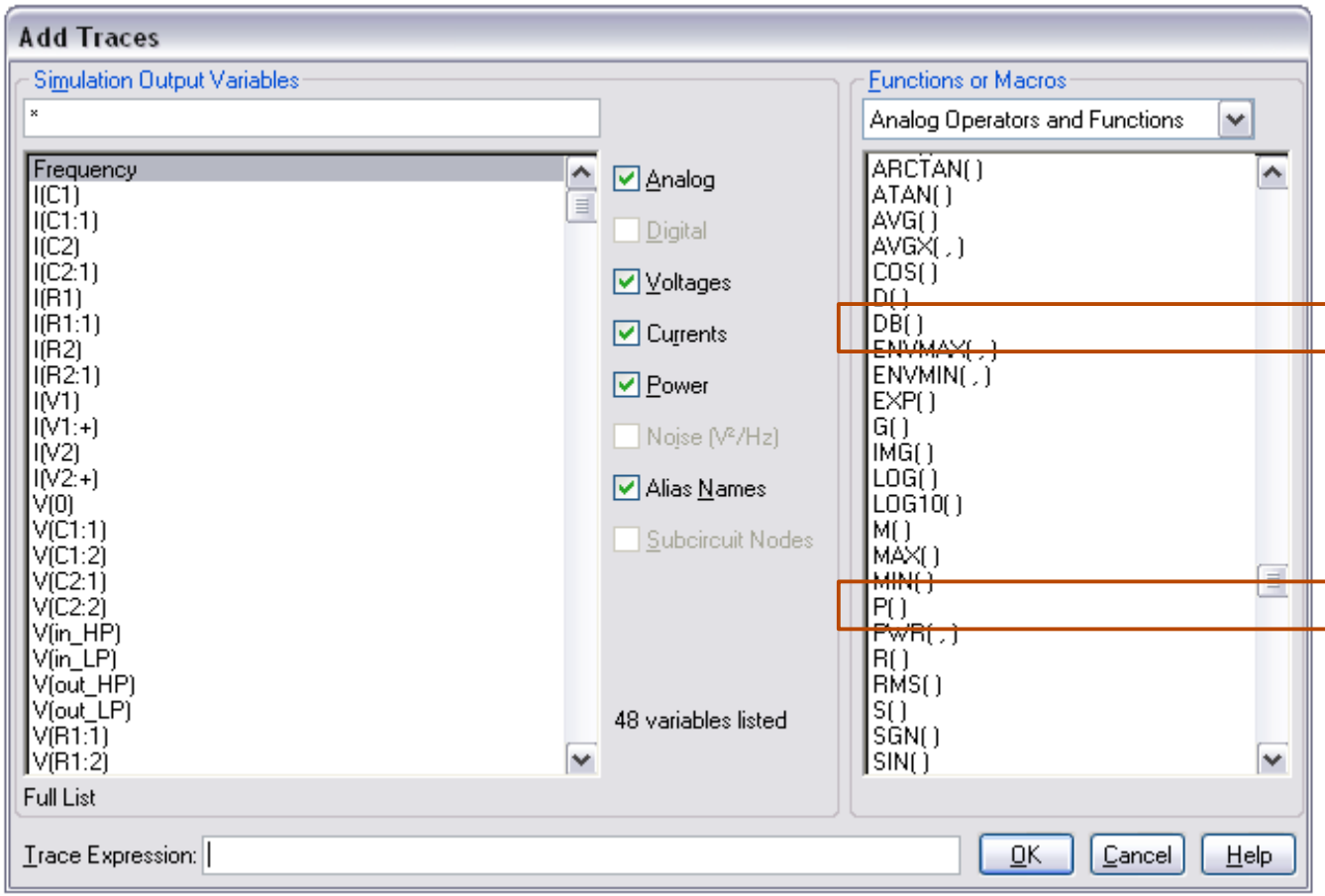
phase



Decibel magnitude

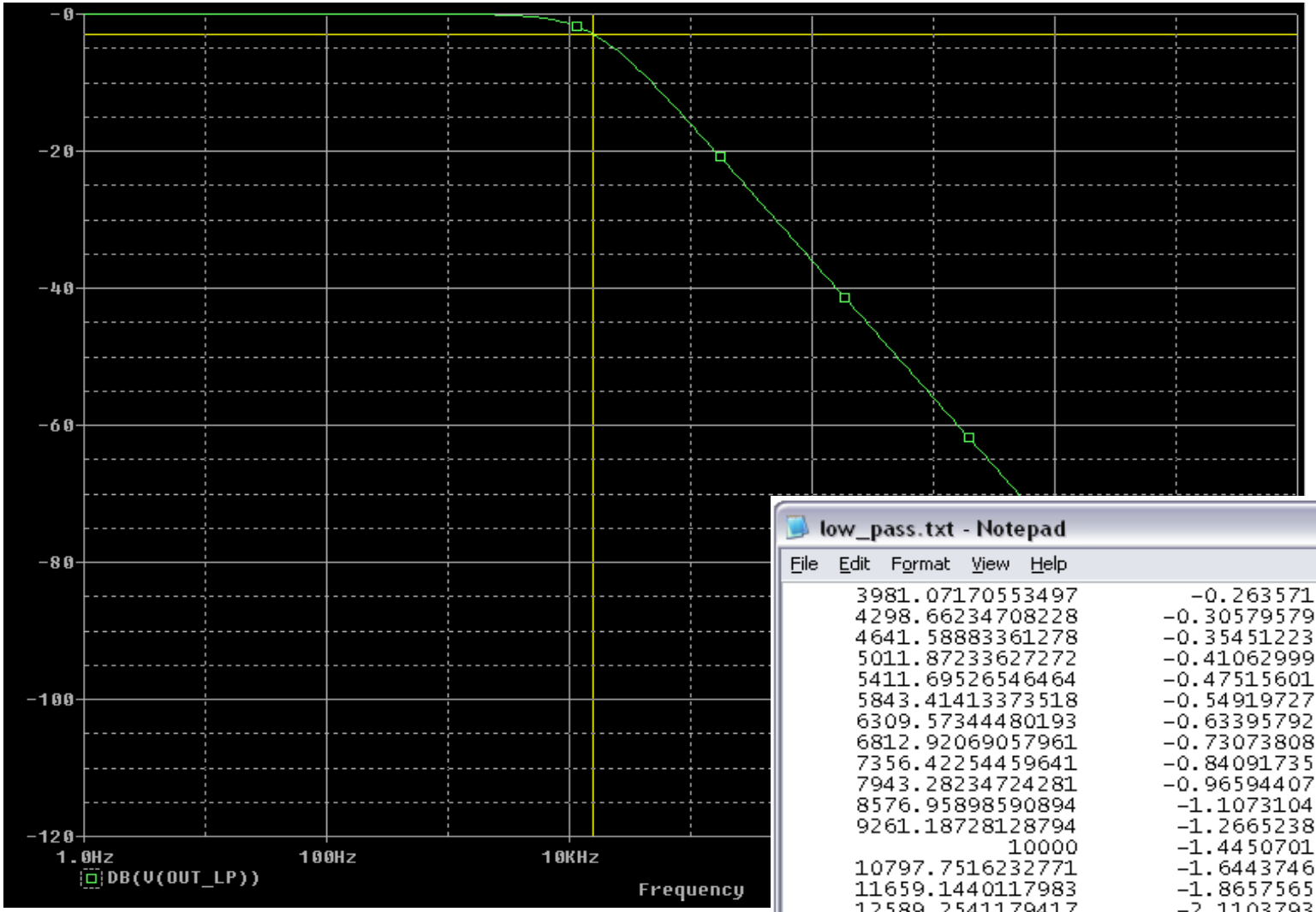
$$|H(j\omega)|_{dB} = 20\log|H(j\omega)|$$

$$f_{-3\,dB} = f_L$$



`DB(V(out))` ***dB operator***

`P(V(out))` ***phase operator***



$$R = 10\ \text{k}\Omega$$

$$C = 1\ \text{nF}$$

low_pass.txt - Notepad

File Edit Format View Help

3981.07170553497	-0.2635719608577
4298.66234708228	-0.305795790652123
4641.58883361278	-0.354512239691518
5011.87233627272	-0.410629992772777
5411.69526546464	-0.475156012331482
5843.41413373518	-0.549197277584987
6309.57344480193	-0.633957920840223
6812.92069057961	-0.730738082329548
7356.42254459641	-0.840917356462937
7943.28234724281	-0.965944070387479
8576.95898590894	-1.10731043868677
9261.18728128794	-1.2665238307477 4
10000	-1.44507017377166
10797.7516232771	-1.64437465336421
11659.1440117983	-1.86575657731268
12589.2541179417	-2.11037930693323
13593.5639087853	-2.37921029441665
14677.9926762207	-2.67297721284105
15848.9319246111	-2.99213644321896
17113.2830416178	-3.33685509256519
18478.4979742229	-3.70699909682846
19952.6231496888	-4.10214226660375
21544.3469003188	-4.52158544135189
23263.0506715363	-4.96438611917765
25118.8643150958	-5.42939860227927
27122.7257933203	-5.91531955222775
29286.4456462524	-6.42073366834477
31622.7766016838	-6.94415817457619

$$f_L = \frac{1}{2\pi 10^4 10^{-9}} \approx 16\ \text{kHz}$$

Designing tips and tricks

- schematics should contain ***only physical elements*** like transistors, resistors, capacitors etc.

- a real IC is biased through external PADS

  - for voltage supplies ***use net aliases*** and **CAPSYM /VCC**, **CAPSYM /VCC_BAR** etc. symbols

  - use an external VDC source for the GND itself, in this way you can also simulate ***ground voltage fluctuations***

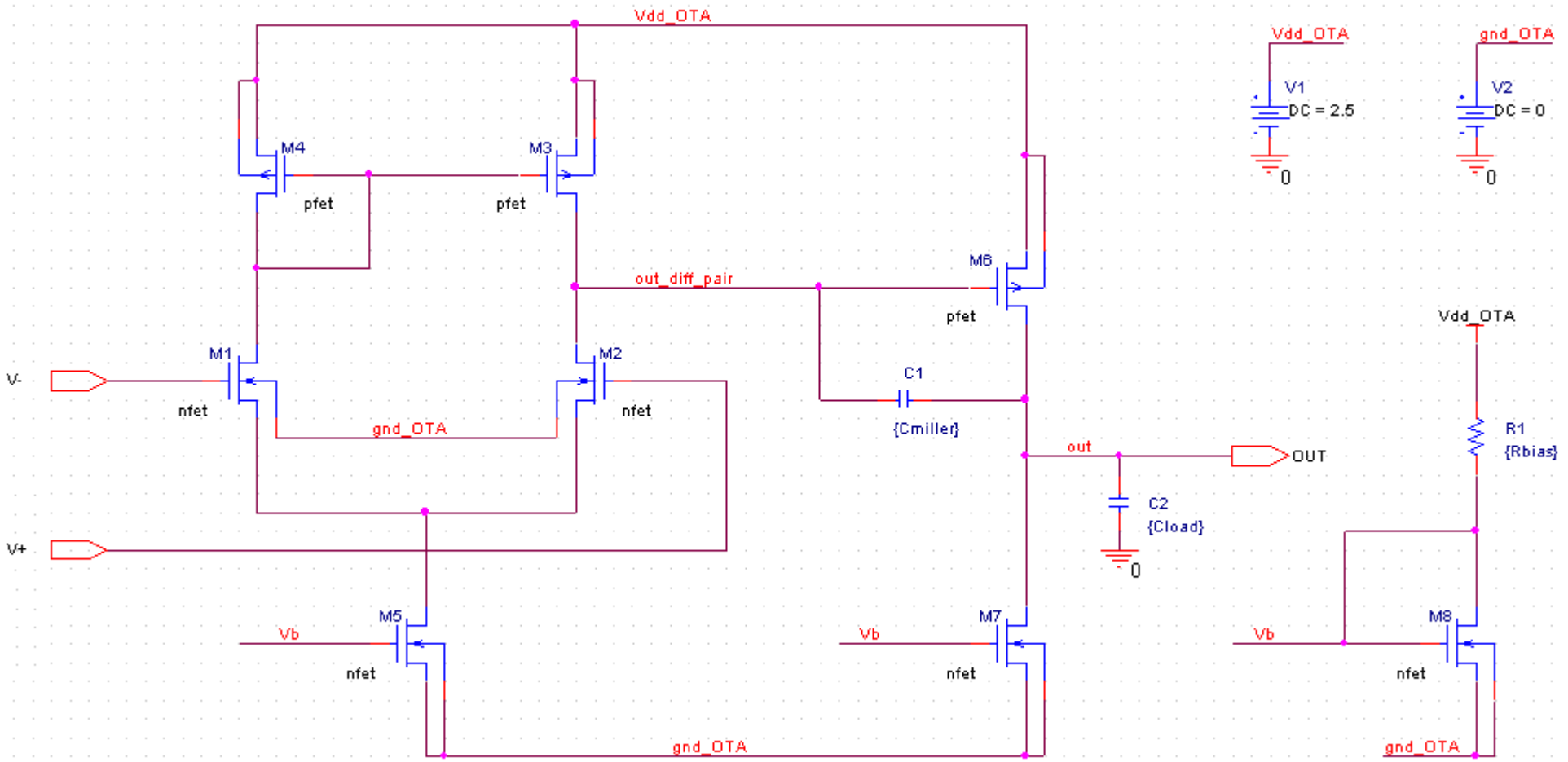
- use net aliases and hierarchical ports/off-page connectors for input and output nets

- check the ***Session Log*** and ***PSpice .out*** files for errors

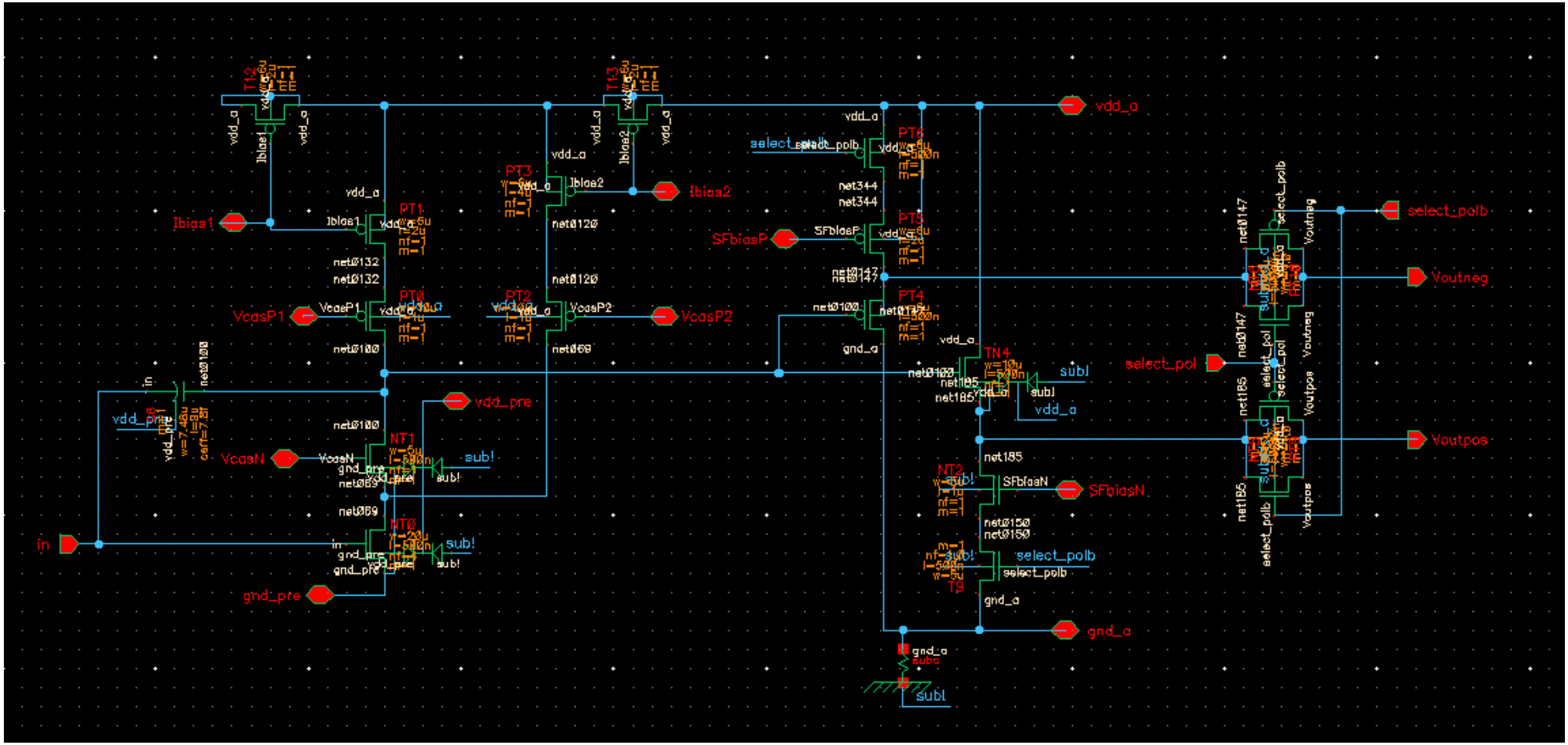
- always check ***each transistor operating region*** *!*

- ***(usage of simulator) × (common sense) ≈ constant***

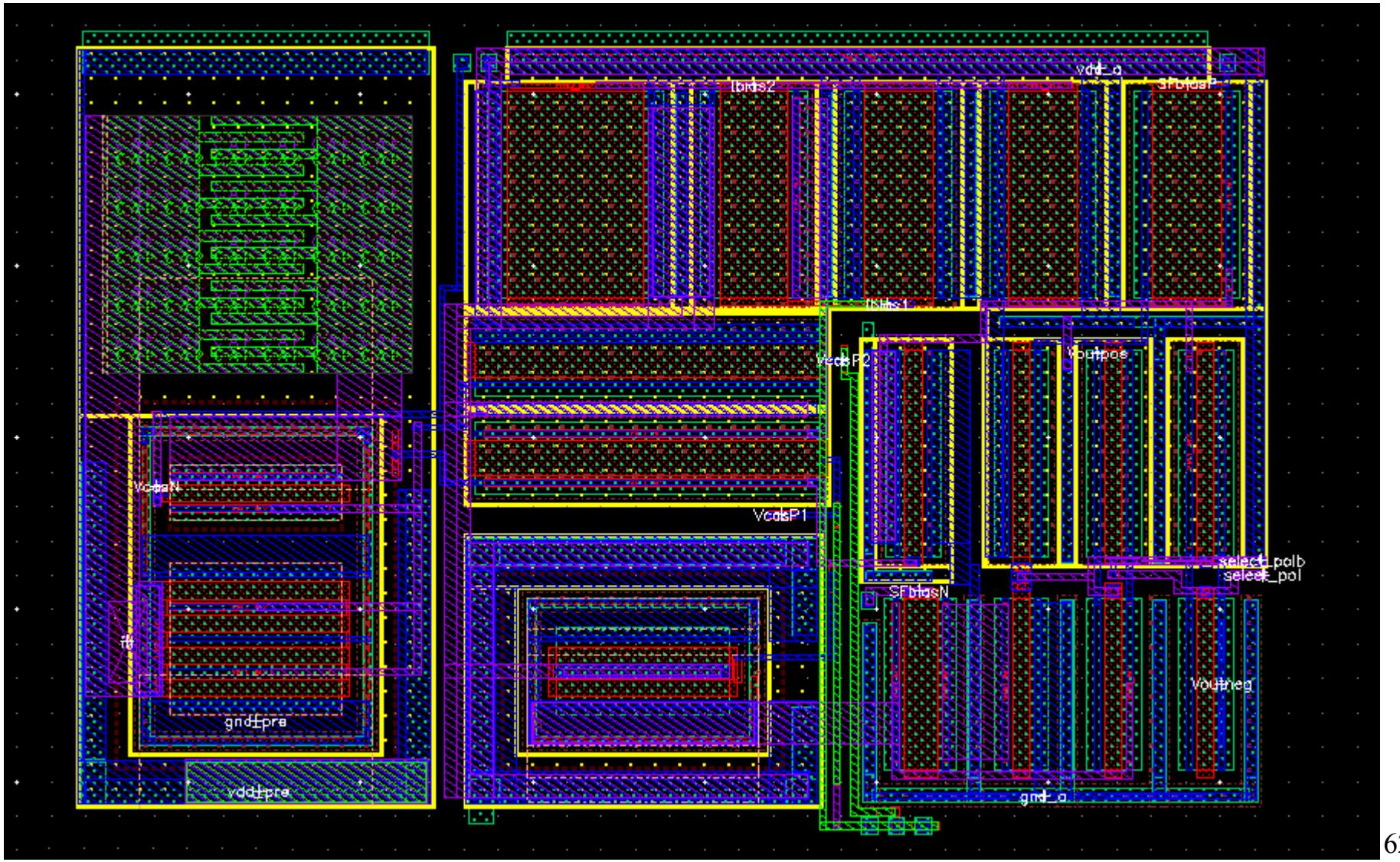
Example: OTA Miller



Cadence VLSI tools (Virtuoso)



Layout


vdd_a
Vcdsp2
Voutpos
VcdsP1
select_polb
select_pol
SFbiasN
Voutneg
gnd_a
gndfpre
vddfpre