Estimation of the depletion capacitance in a monolithic pixel sensor

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Outline

- ***monolithic pixel sensors***

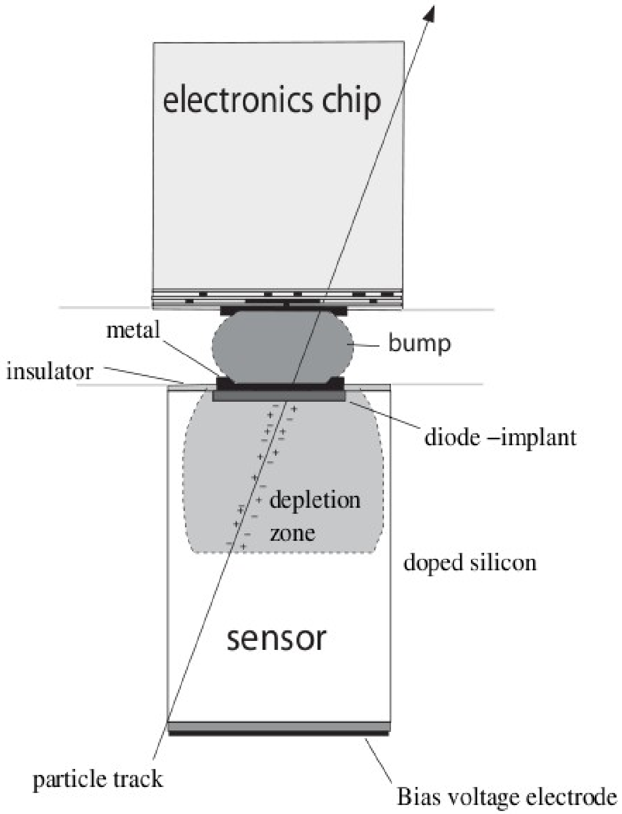
- ***pixel matrix segmentation***

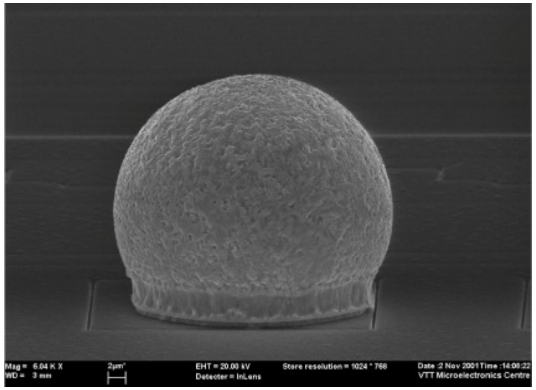
- ***on-chip and off-chip read-out electronics***

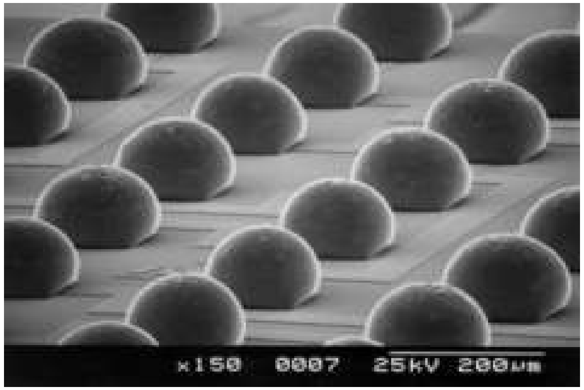
- ***DAQ system***

- ***lab measurements***
    - ***setup linearity***
    - ***sensor capacitance estimation***

Hybrid pixel detectors

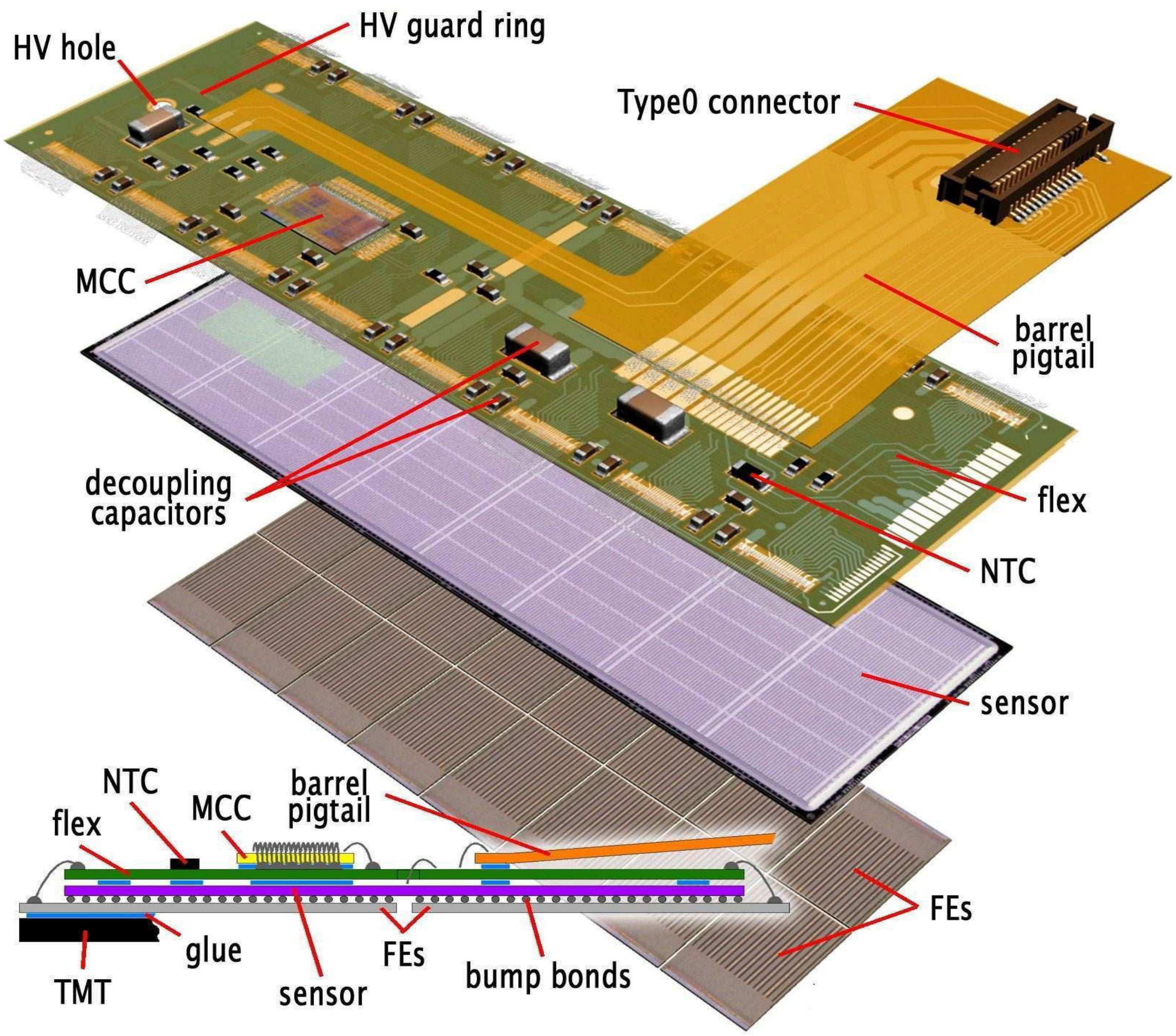




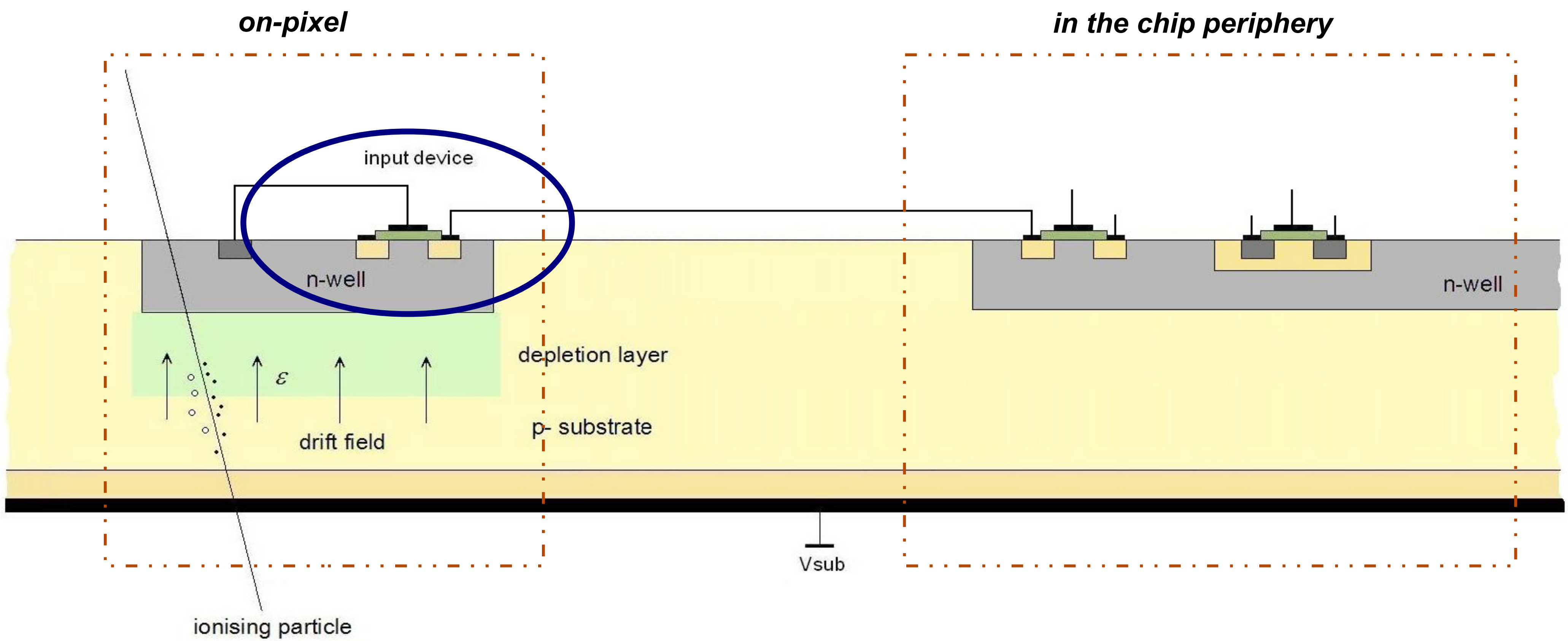


- sensor and electronics made on ***two different silicon dies*** and then mated together
  - ***bump bonding*** technique → expensive (cost can be afforded to cover max. area ~m^2)
  - charge collection ***by drift*** → OK speed and radiation hardness
  - power consumption ~ 250 mW/cm^2
  - material budget ~ 300 µm

Full module example (ATLAS)

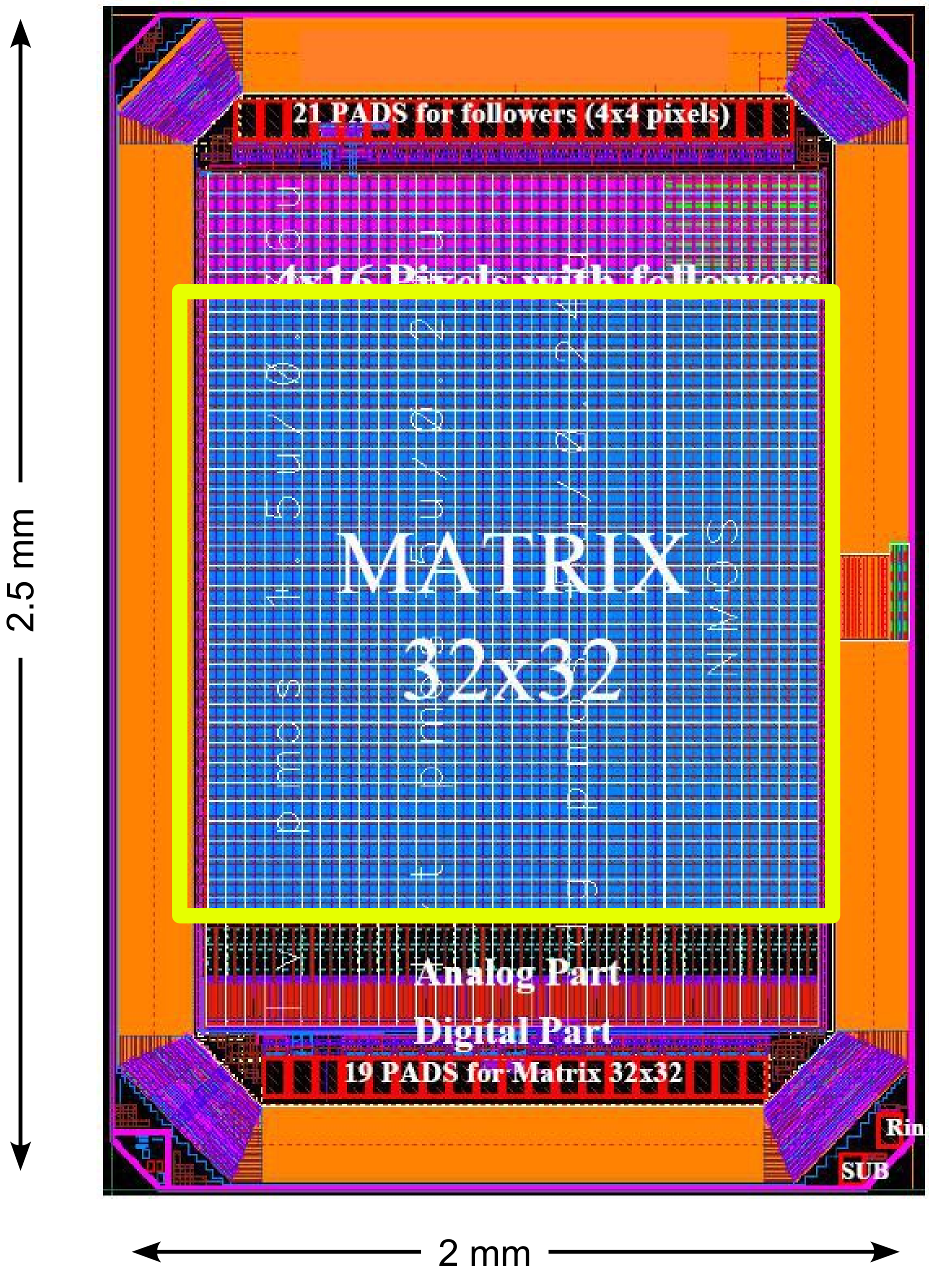


LePix



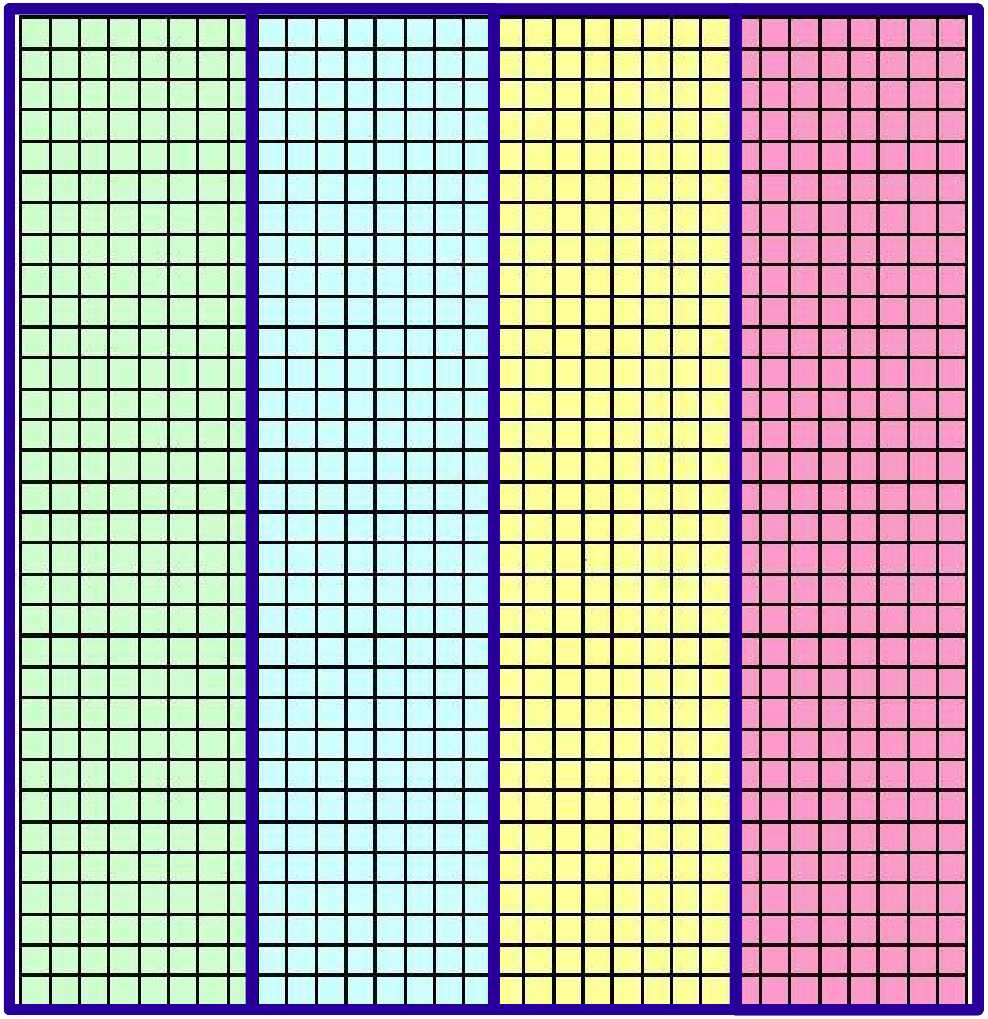
- 90 nm ***commercial*** CMOS technology
- ***reverse biased substrate*** (~ - 30V)→ charge collection ***by drift***
- the ***first transistor*** of the analog front-end electronics is built at the top of each the pixel !
- the remaining electronics is placed in a dedicated n-well ***at the periphery*** of the sensitive region
  - the n-well must be ***insulated*** from the reverse biased substrate to avoid ***breakdown*** !

Matrix segmentation (1)



- sensitive area + read-out electronics are ***integrated on the same chip*** !
  - ***monolithic*** approach
  - no separation between sensor and electronics
- a ***guard ring*** structure (200 μm around the matrix) ensures a uniform depletion region
- two asymmetric regions in the matrix
  - TOP part → 6 rows x 32 columns
  - CORE part → 32 rows x 32 columns
- only CORE part pixels (1024 pixels) will be used for lab measurements

Matrix segmentation (2)



thin oxide PMOS (1)

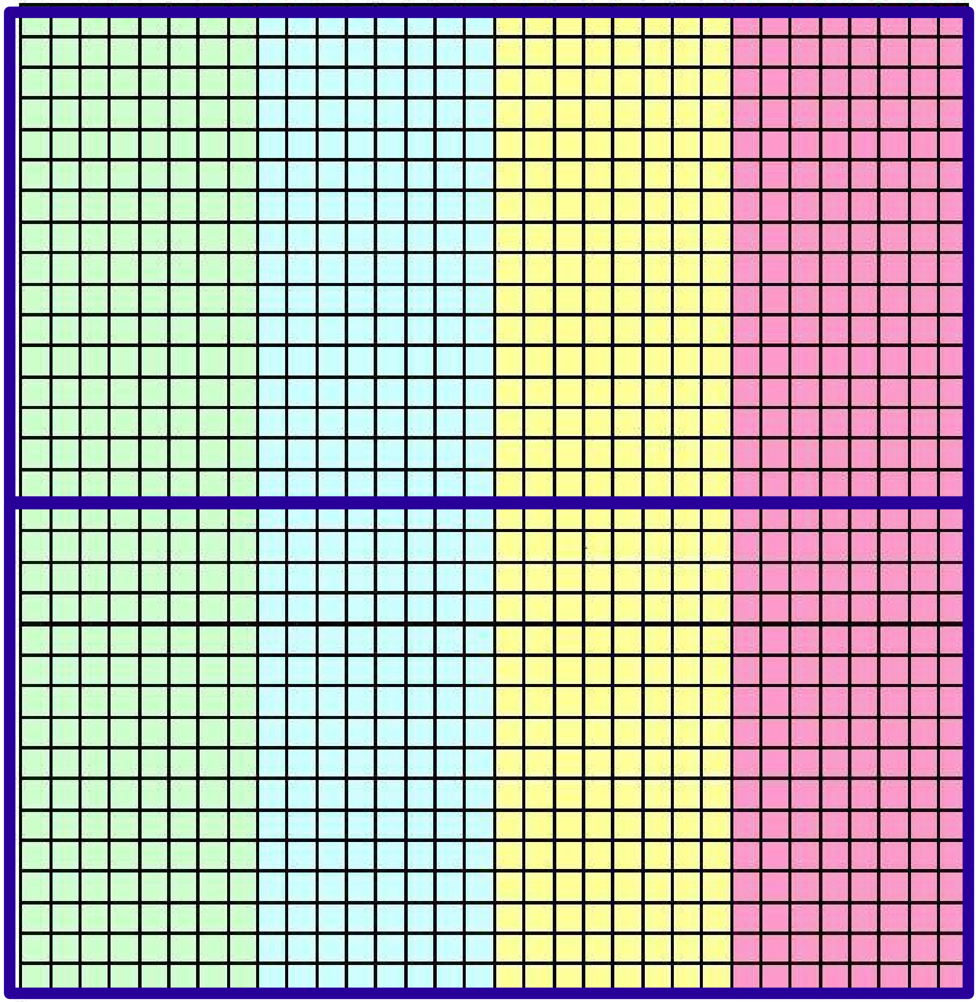
thin oxide PMOS (2)

thick oxide PMOS

thin oxide NMOS

- different options have been implemented for the on-pixel transistor
- vertical segmentation → pixels with ***4 different types of input transistor***
  - 8 columns thin oxide PMOS (1)
  - 8 columns thin oxide PMOS (2)
  - 8 columns thick oxide PMOS
  - 8 columns thin oxide NMOS
- due to the limited available area PMOS input devices are preferable

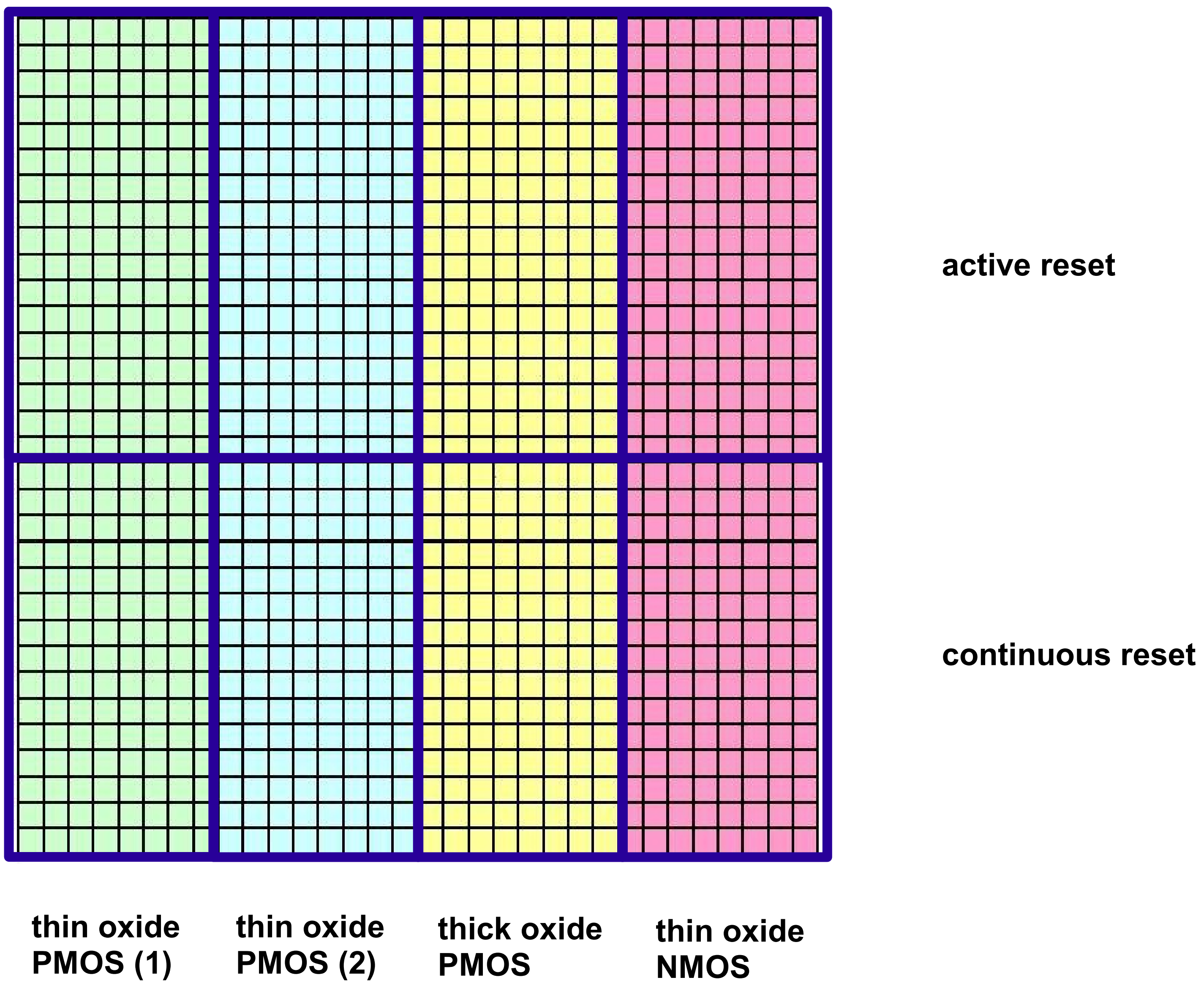
Matrix segmentation (3)



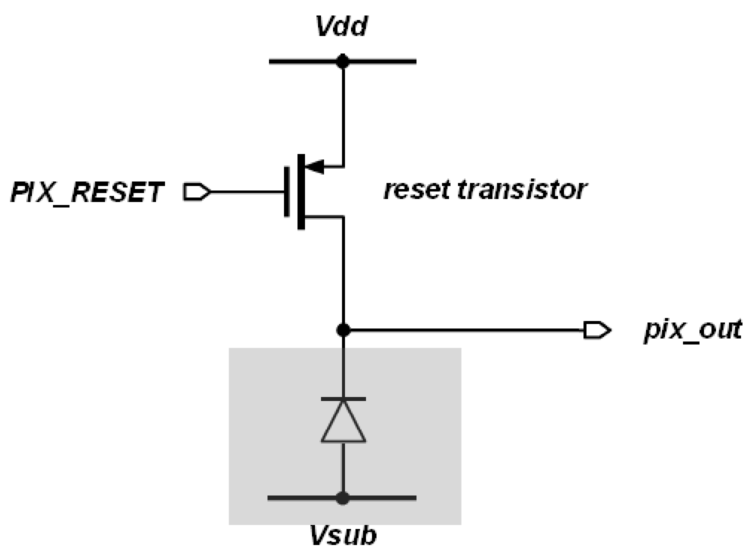
- each pixel cell needs to ***discharge*** the depletion capacitance after a particle hit has been detected
  - on-pixel ***reset scheme*** (next slide)

- horizontal segmentation → pixels with ***2 different types of reset schemes***
  - 16 raws with ***active reset***
  - 16 raws with ***continuous reset***

Matrix overall layout



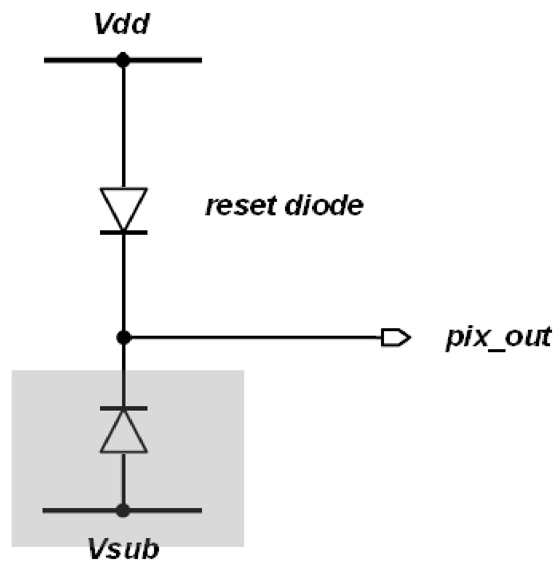
Reset schemes



Active reset

In active-reset pixels a PMOS ***reset transistor*** is used to reset the sensor. The gate is driven by a digital signal ***PIX_RESET***.

When ***PIX_RESET* = 0** a current discharges the pixel capacitance.PIX_RESET

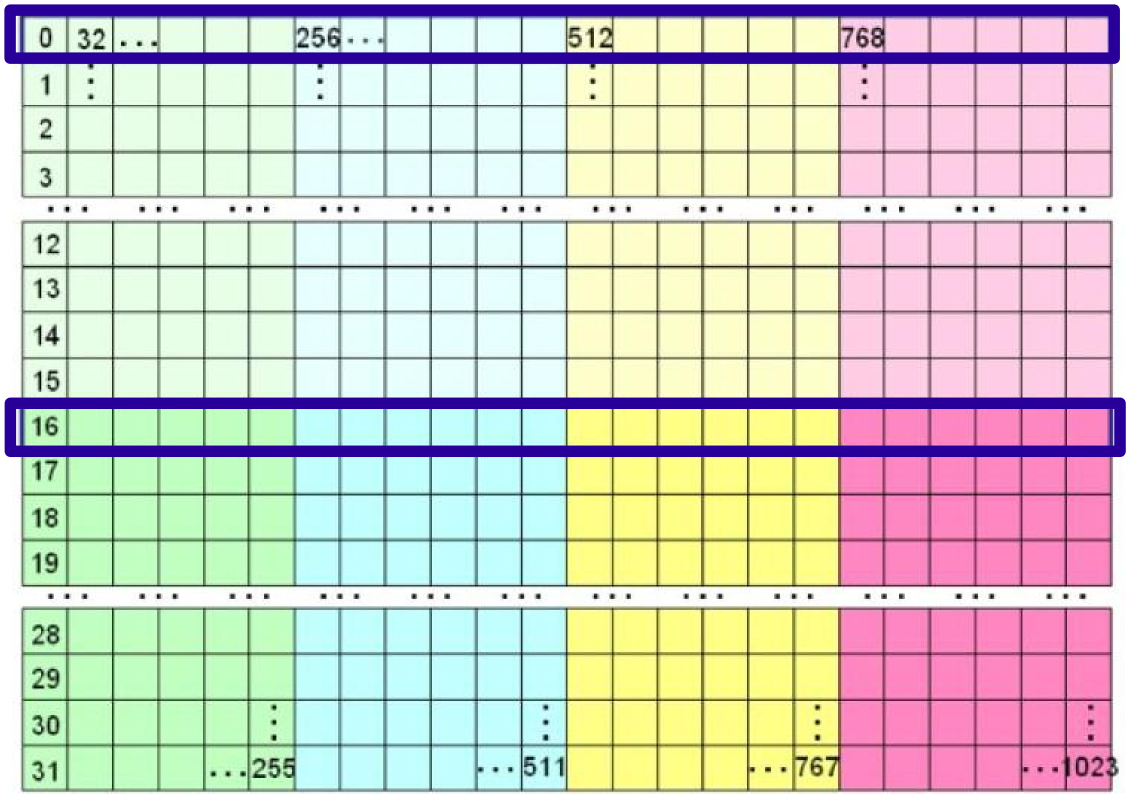


Continuous reset

Continuous-reset pixels discharge the sensor capacitance though a ***diode*** connected to a DC voltage.

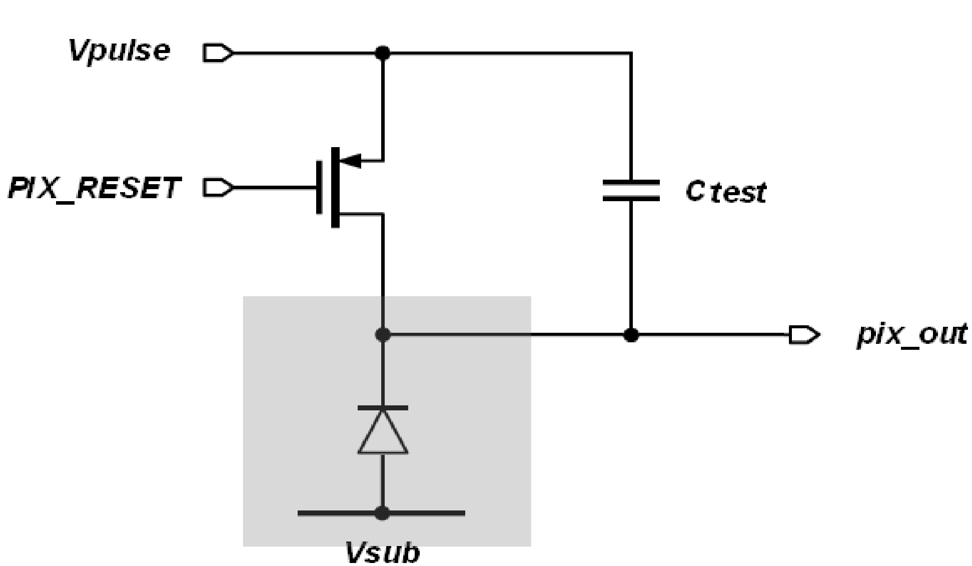
Pulsed rows

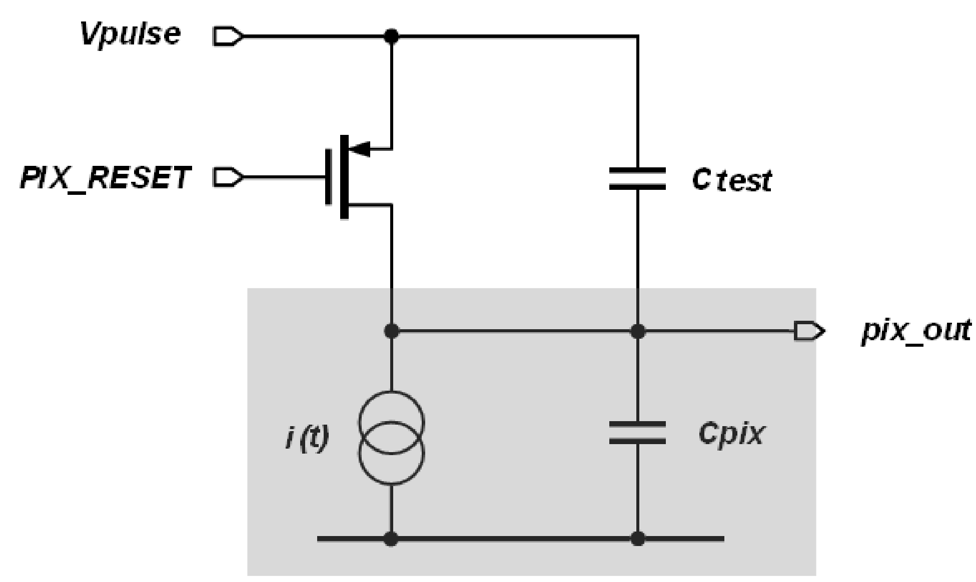
For testing purposes two rows (16 + 16 = 32 pixels) in the CORE part can be pulsed by using an external **test pulse** applied over a ***test capacitance***



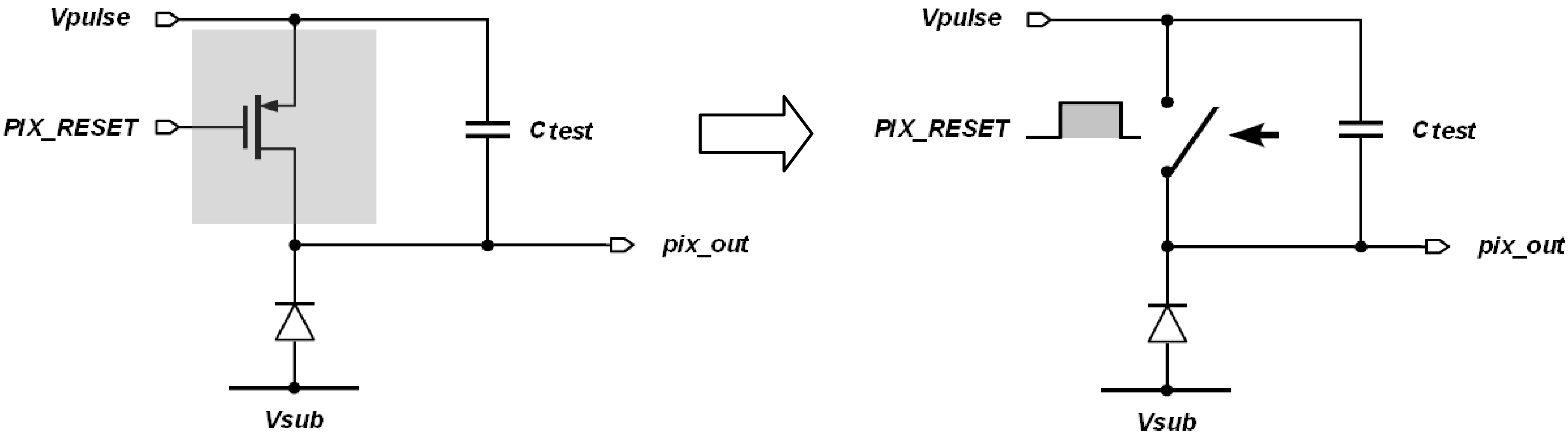
- 16 pixels with ***active reset*** (raw 0)
- 16 pixels with ***continuous reset*** (raw 16)

Sensor electrical model

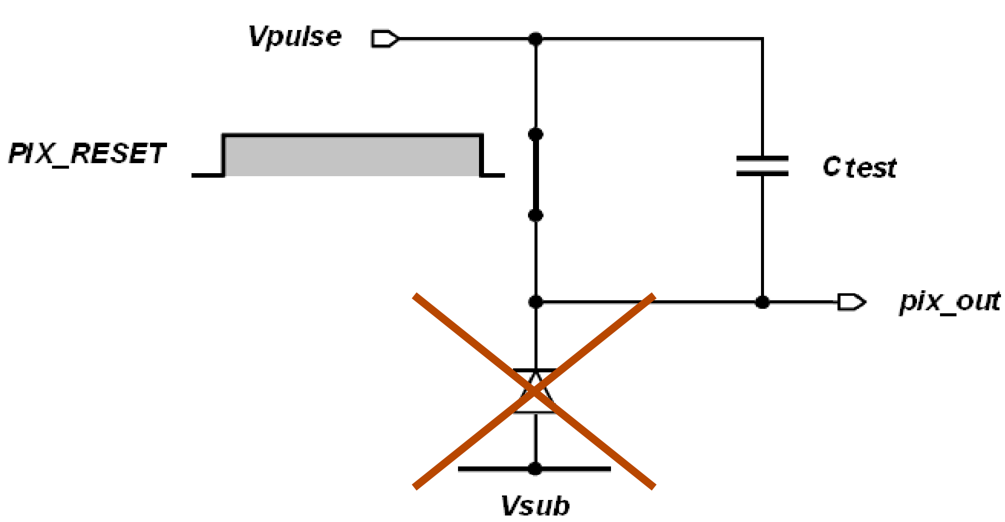


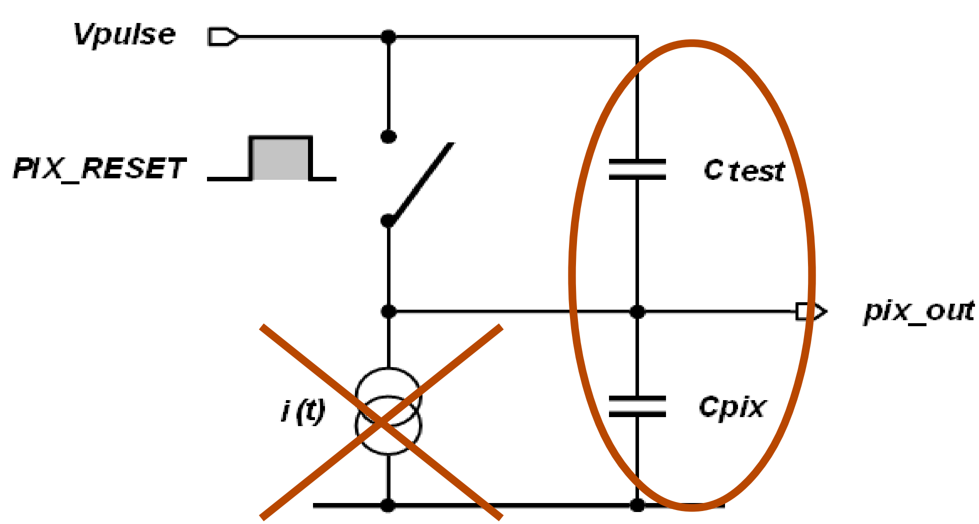


Active reset + pulsed pixels (1)



Active reset + pulsed pixels (2)

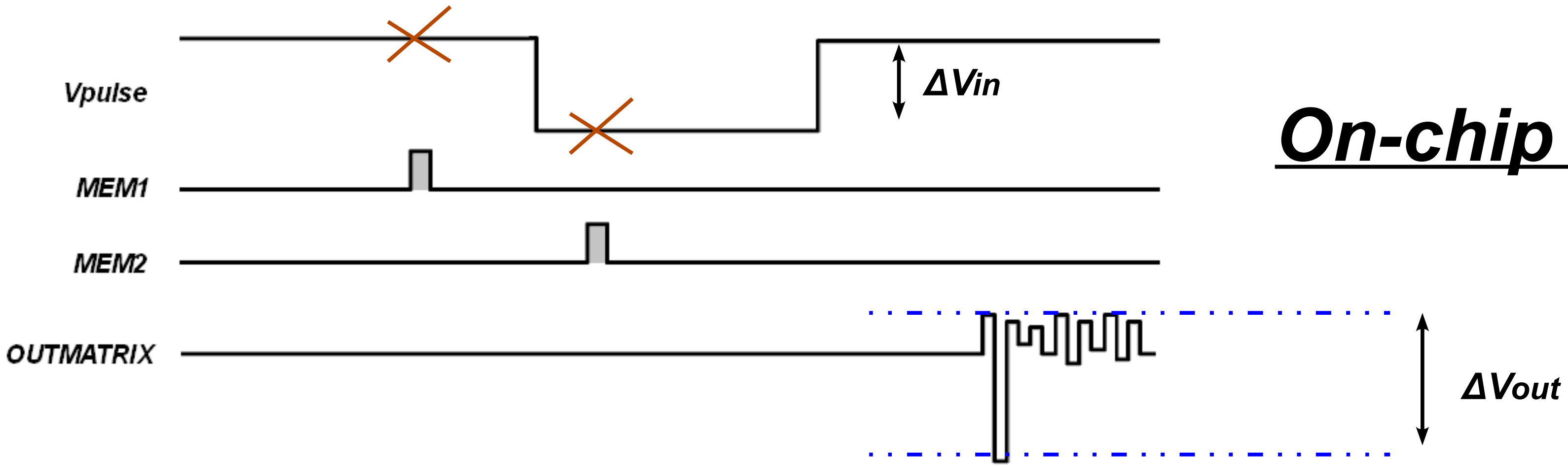


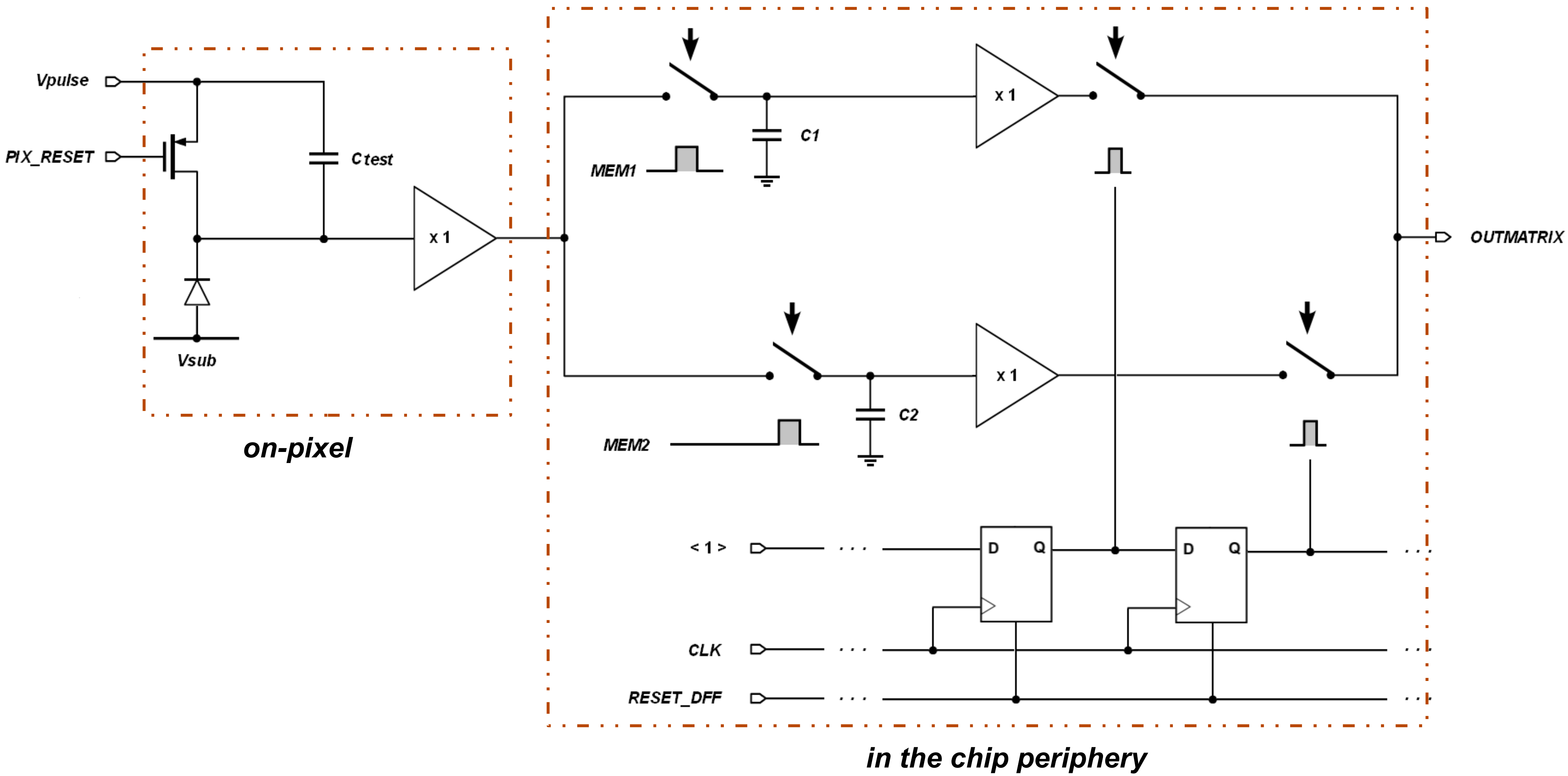


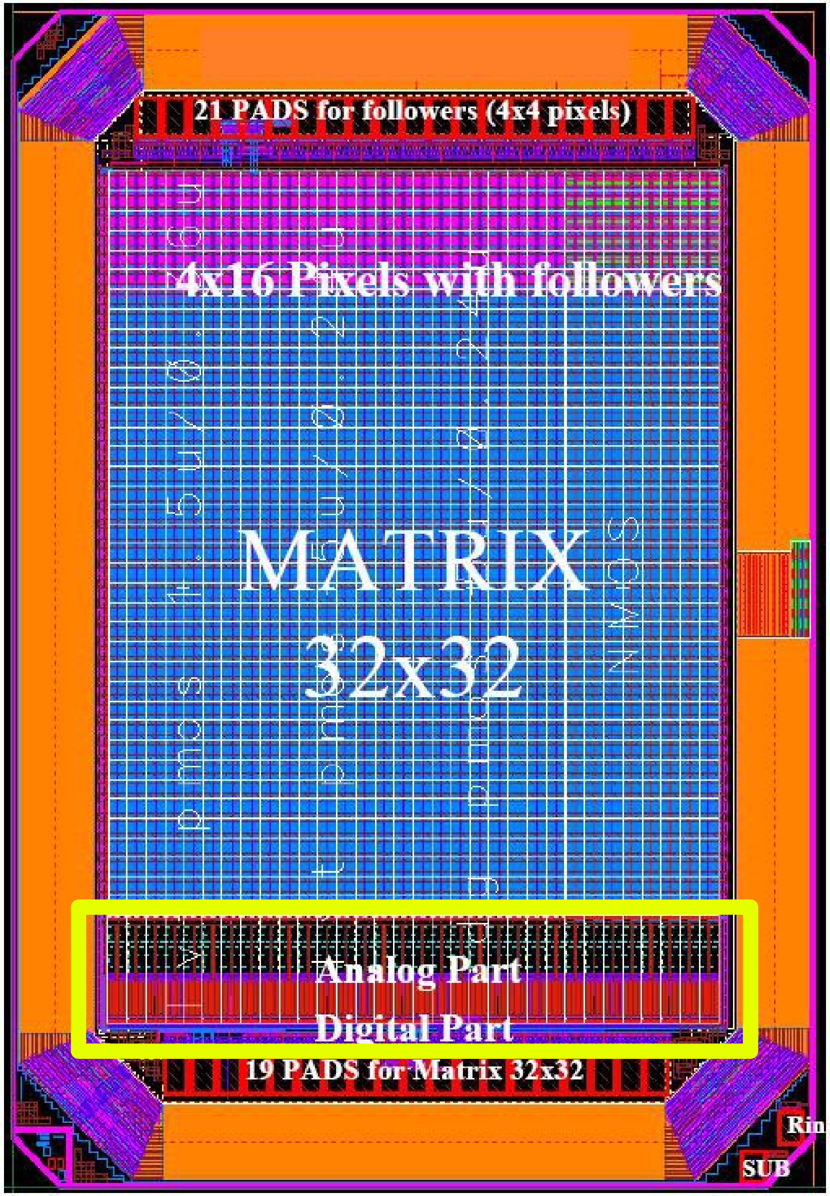
- ***PIX_RESET*** is kept high for the entire acquisition
  - PMOS switch ~short circuit
  - ***pix_out*** ≈ ***Vpulse***
- the sensor is ***excluded*** from the read-out !
  - useful configuration for ***electronics-only characterizations***

- ***PIX_RESET*** is a short pulse (a few clock cycles)
  - the switch opens when ***PIX_RESET*** goes low
  - *i(t) = 0* (you will not perform a test beam!)
  - test and sensor capacitances form a simple ***capacitive divider***
- an estimation of the sensor capacitance *Cpix* can be obtained by applying a test pulse ***Vpulse***

On-chip S/H read-out







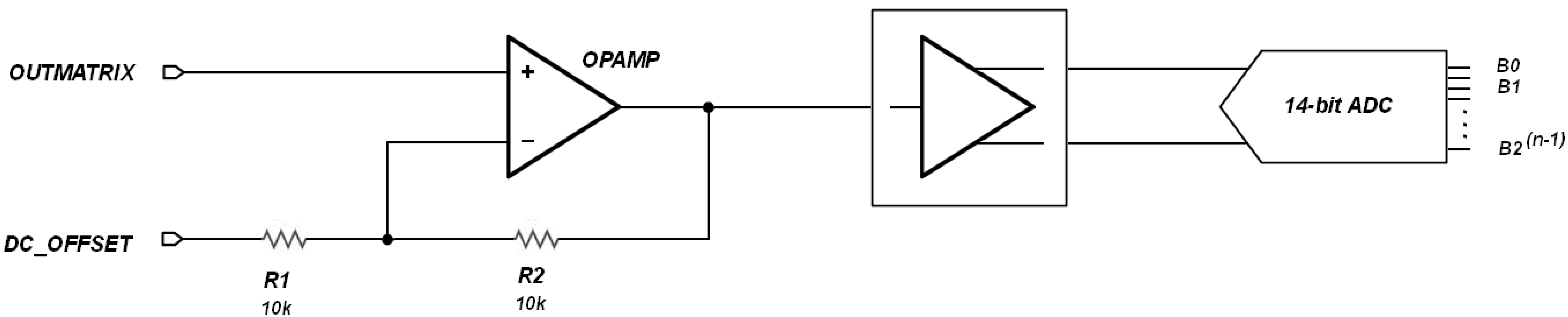
Analog and digital circuits are built in the ***chip periphery*** and ***integrated*** on the same sensor silicone die !

analog part

digital part

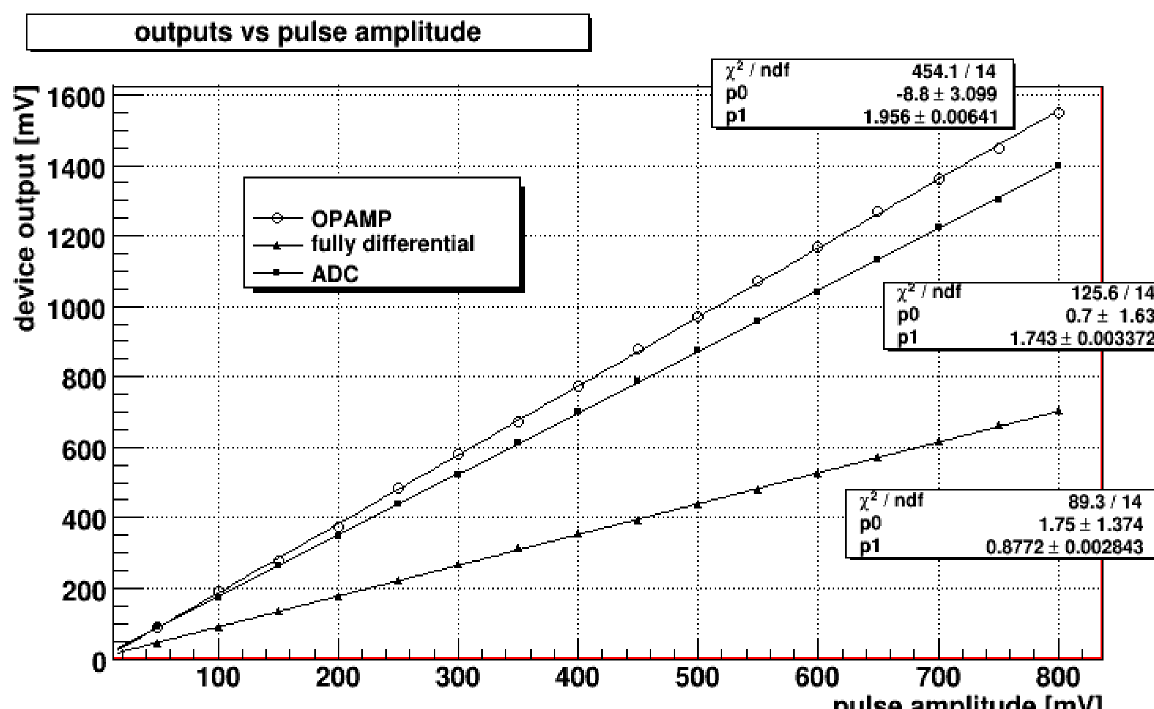
Off-chip read-out

single ended → fully differential

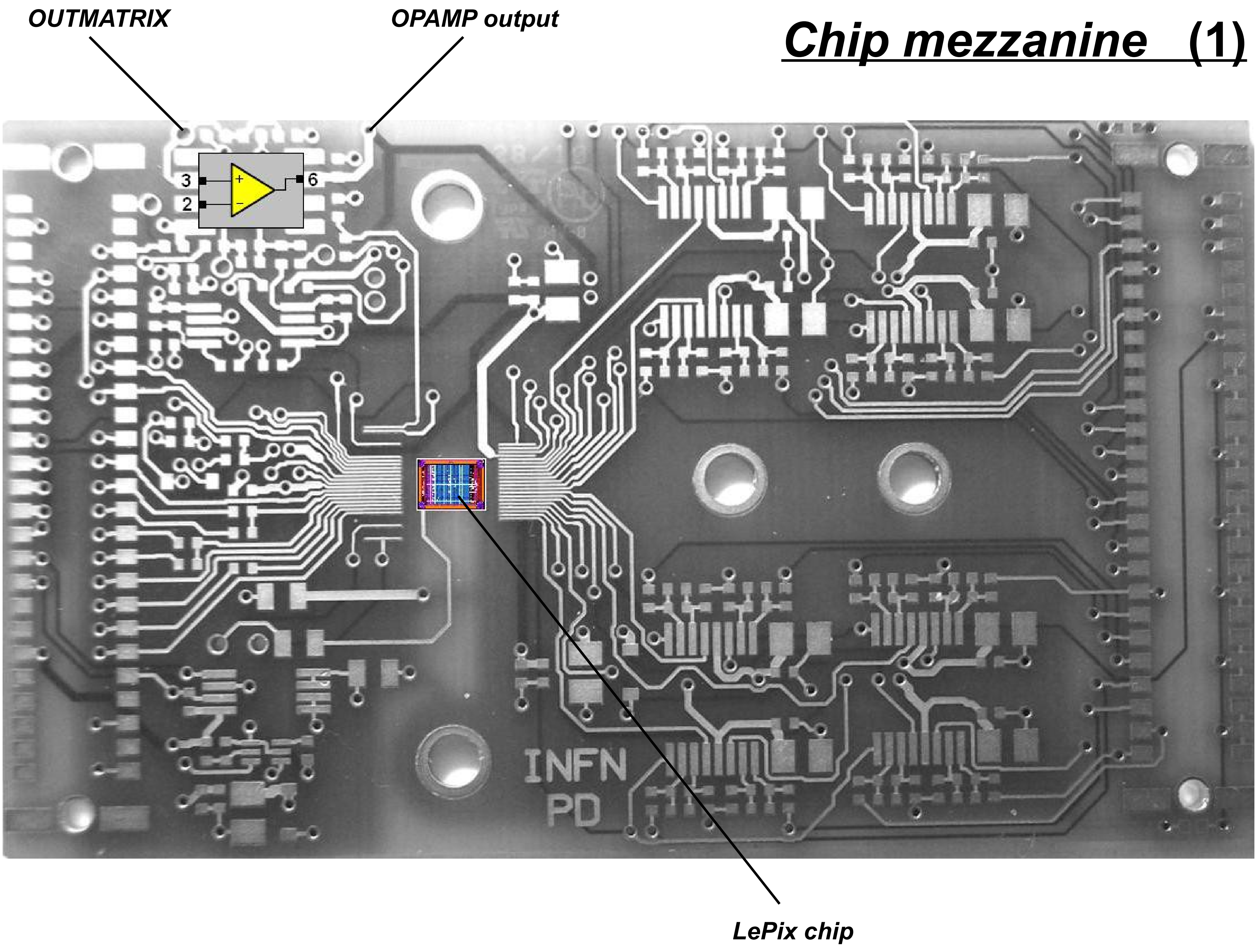


non inverting amplifier

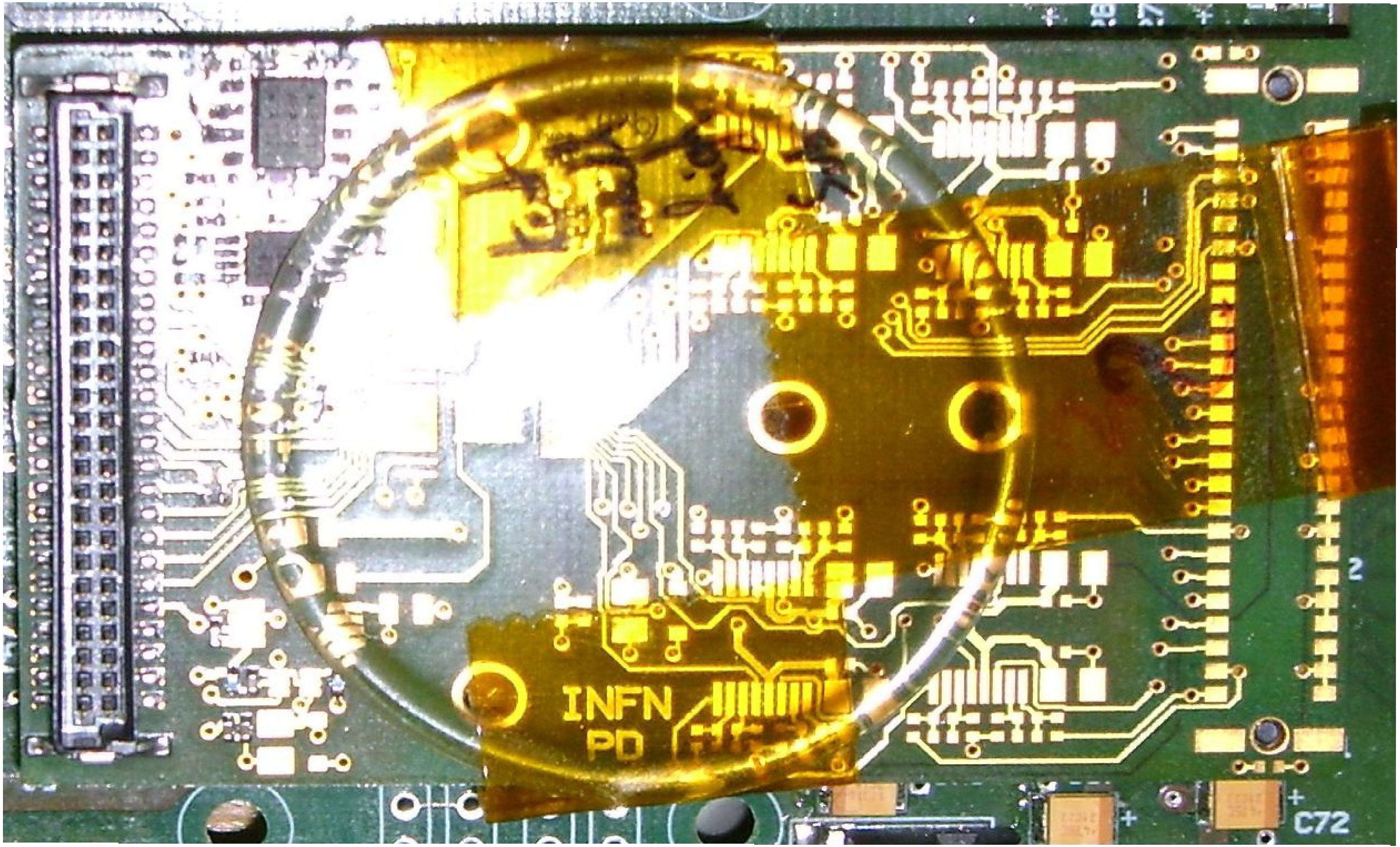
(Av = 1 + R2/R1)



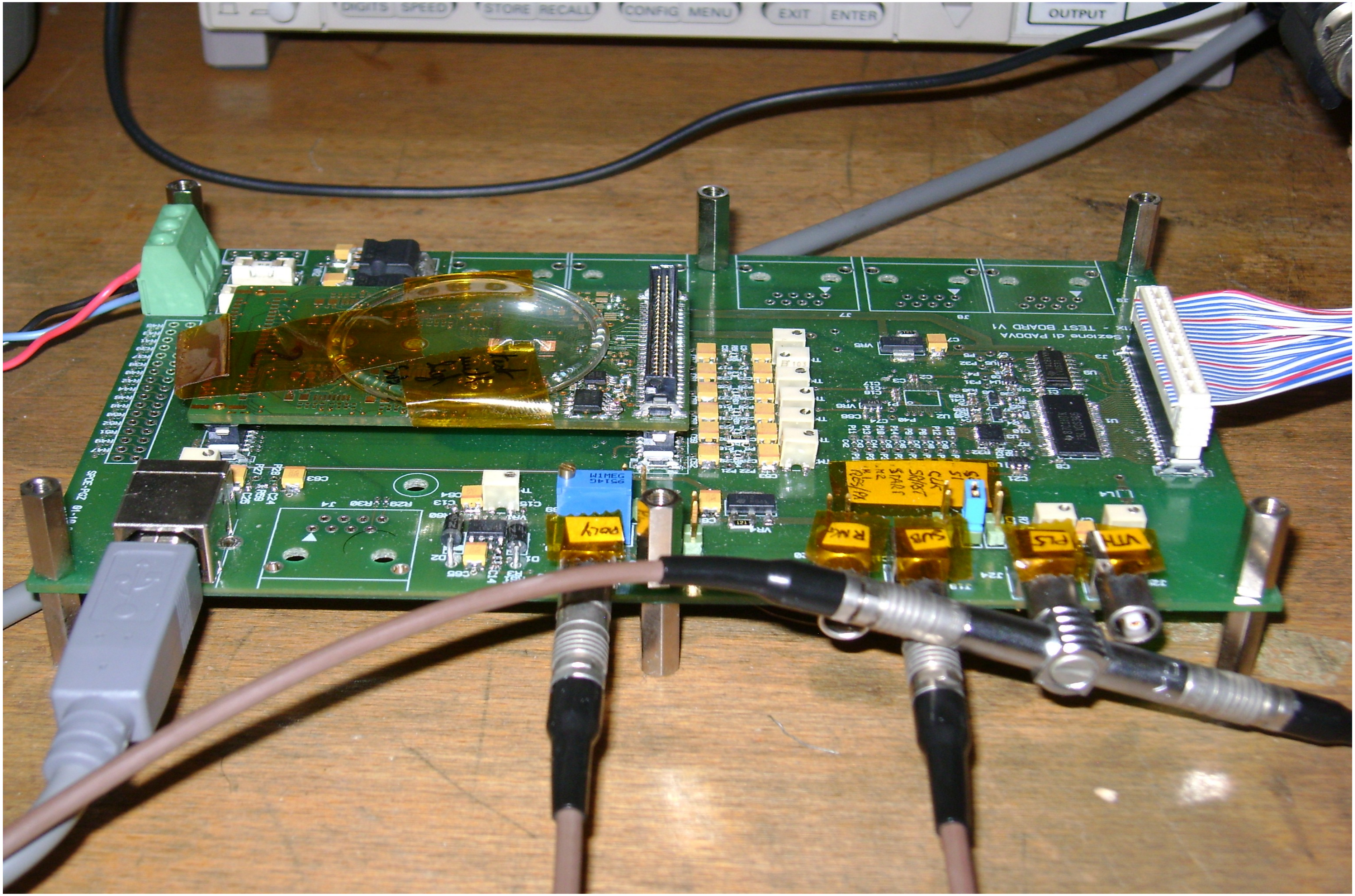
Chip mezzanine (1)



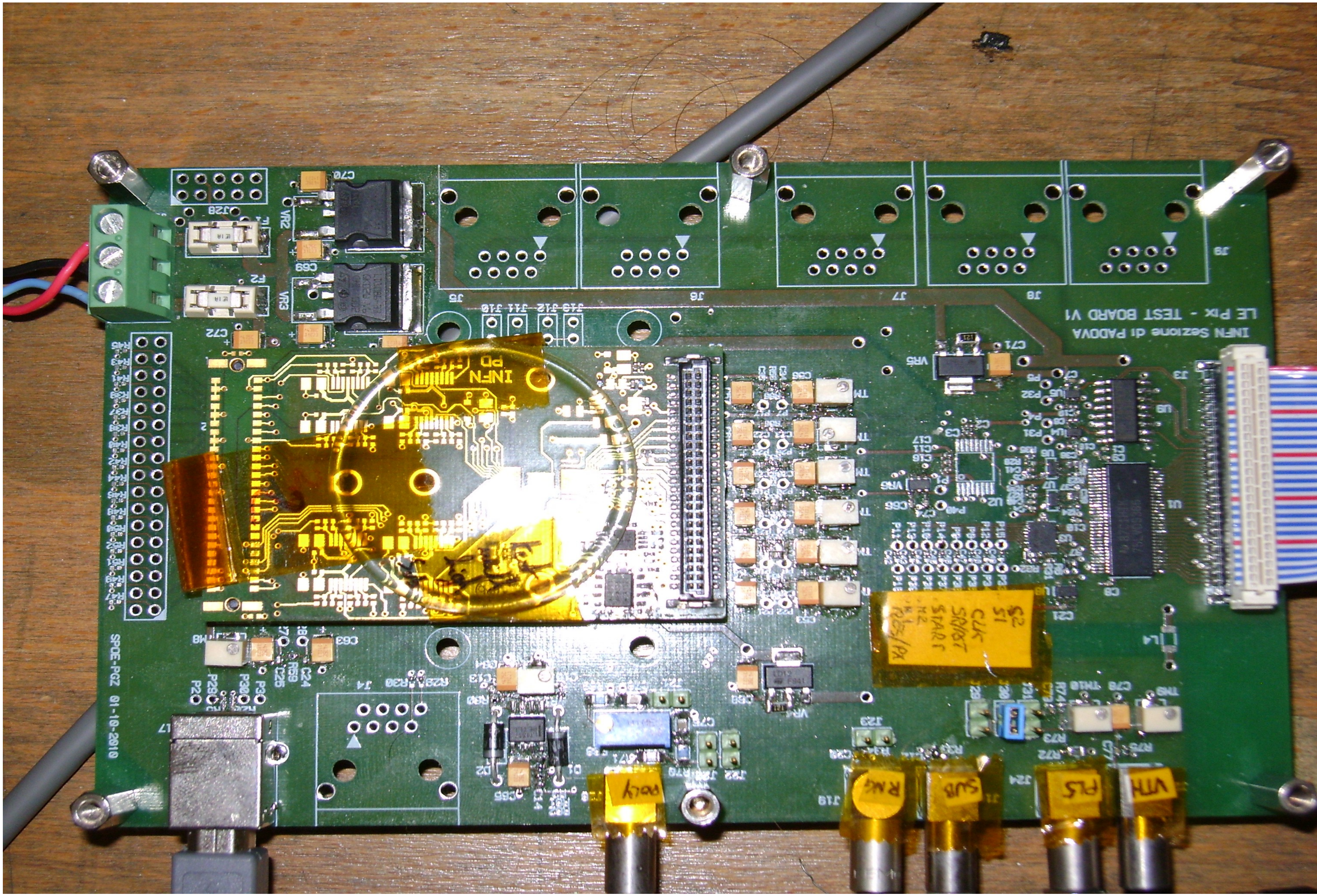
Chip mezzanine (2)



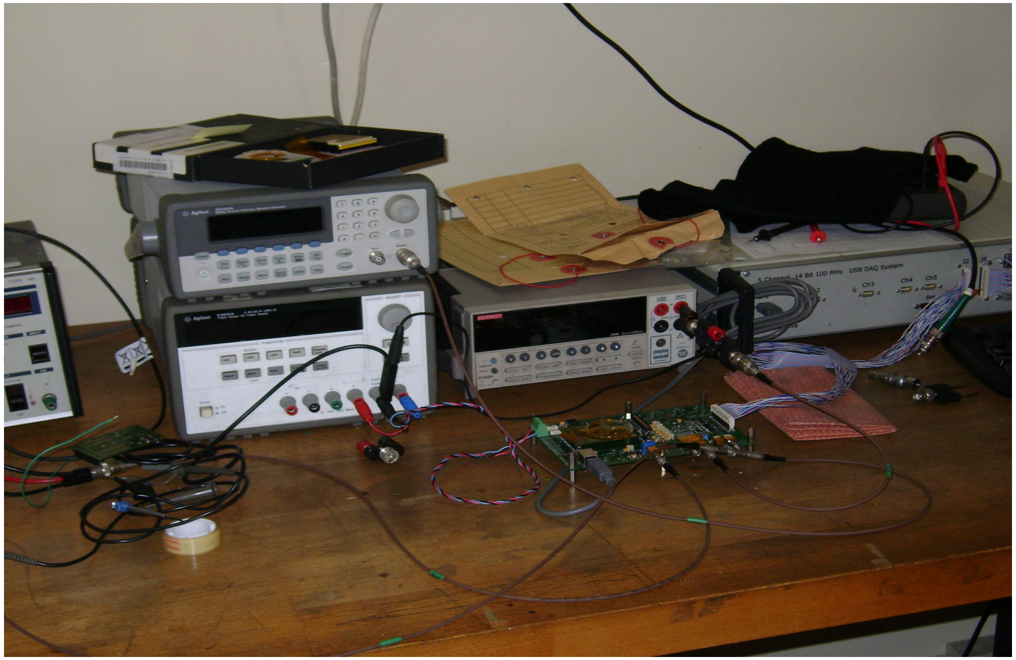
Test PCB (1)



<u>Test PCB (2)</u>

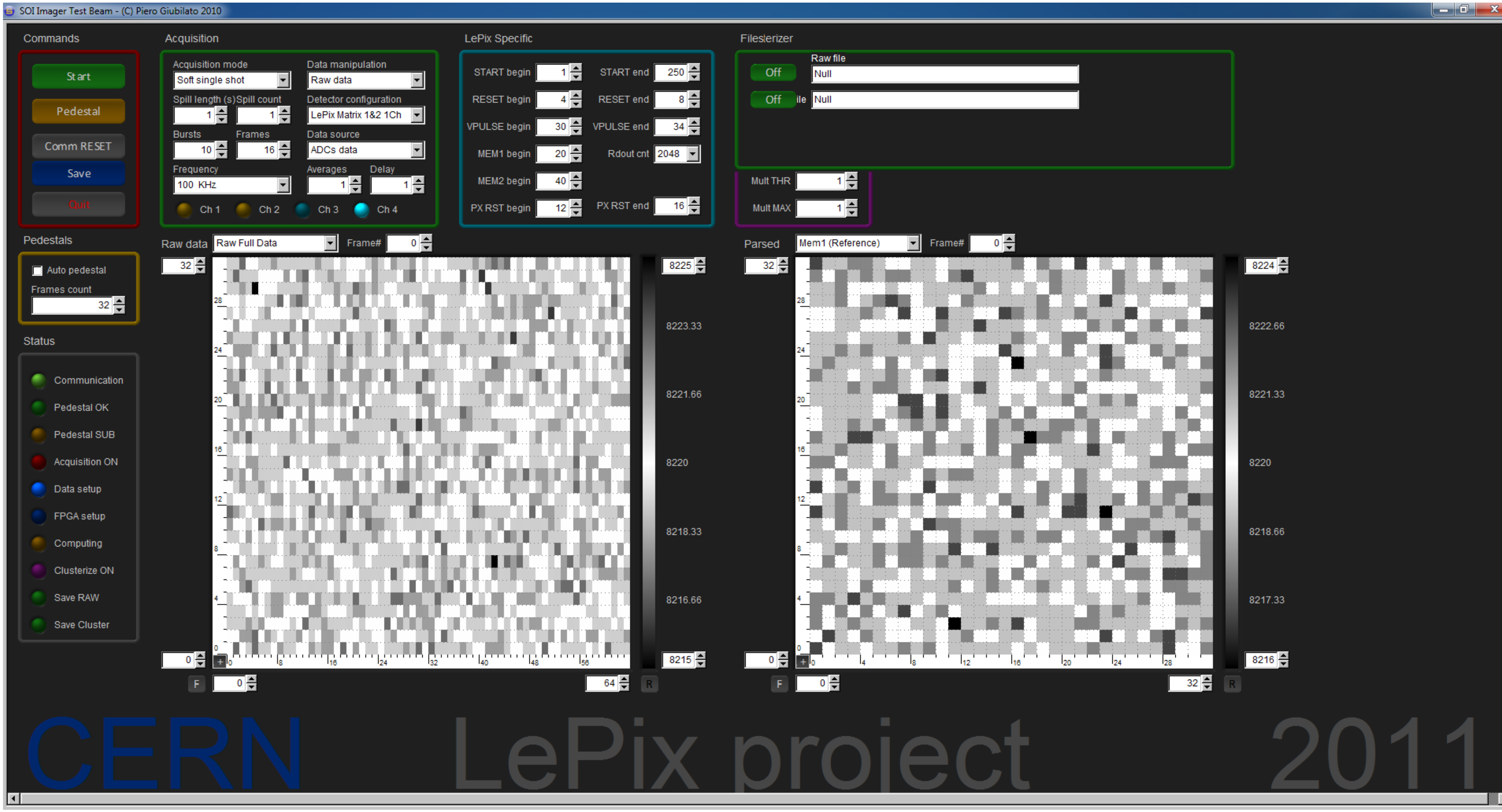


Experimental setup

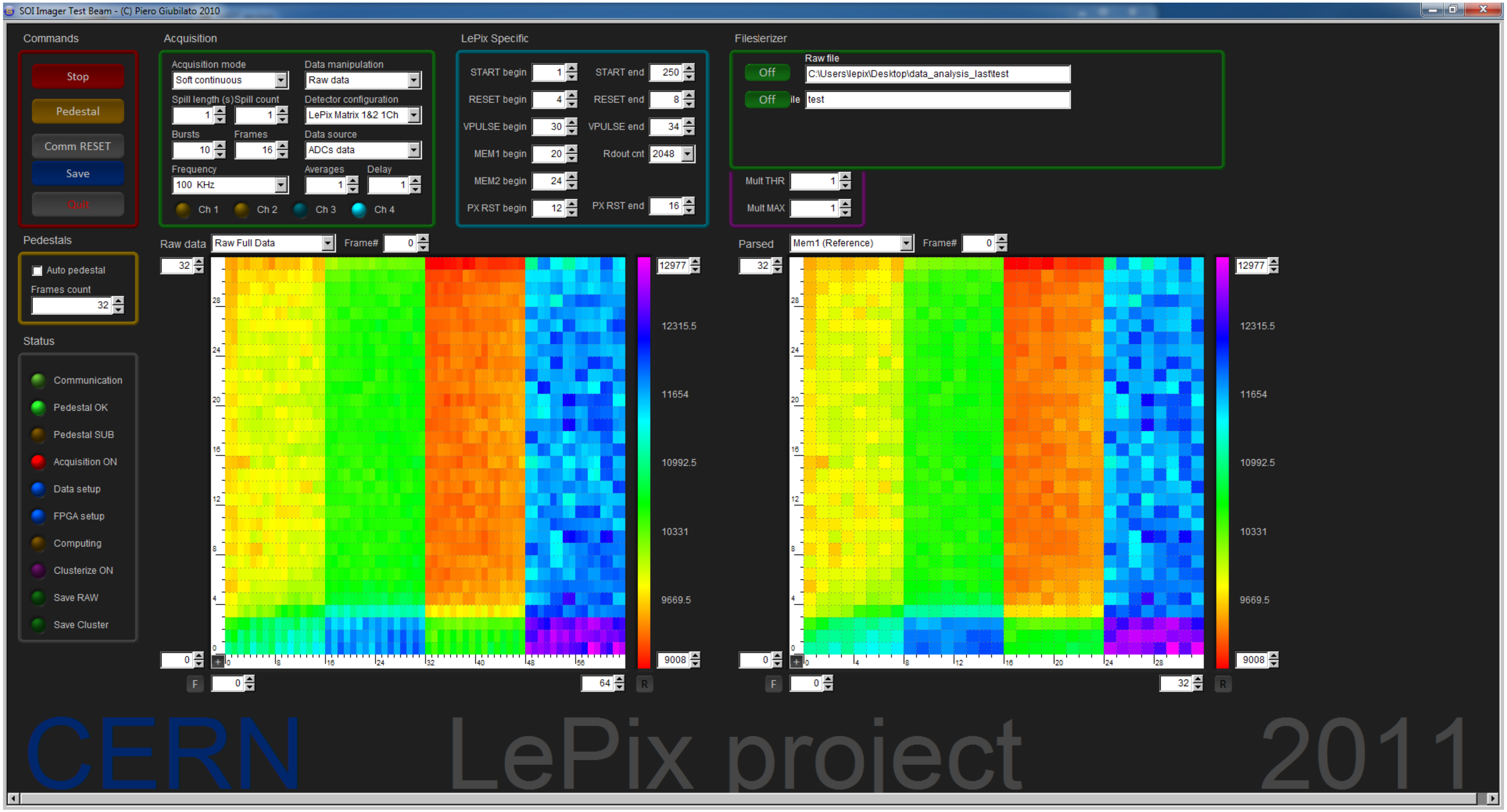


- plug-and-play mezzanine
- test PCB
- power supplies
  - test PCB biasing (± 5 V)
  - sensor depletion voltage (max. -30 V)
  - parasitic transistors
- pulse generator
- digital oscilloscope
- DAQ (14-bit ADC with USB interface)
- computer with acquisition interface

DAQ interface (1)

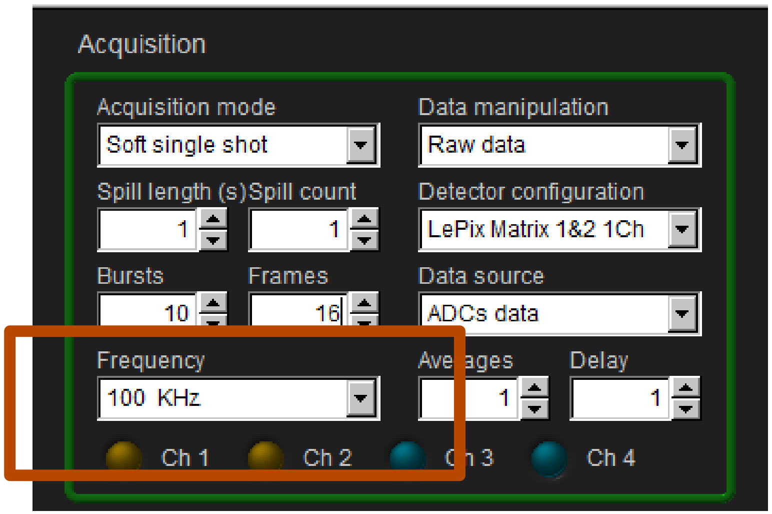


DAQ interface (2)

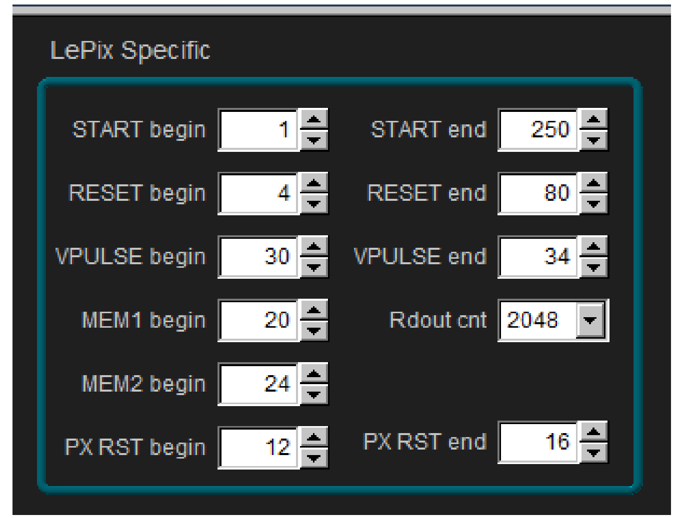


Control signals – DAQ interface

The ***timing*** for digital control signals is set from DAQ interface



CLK



START

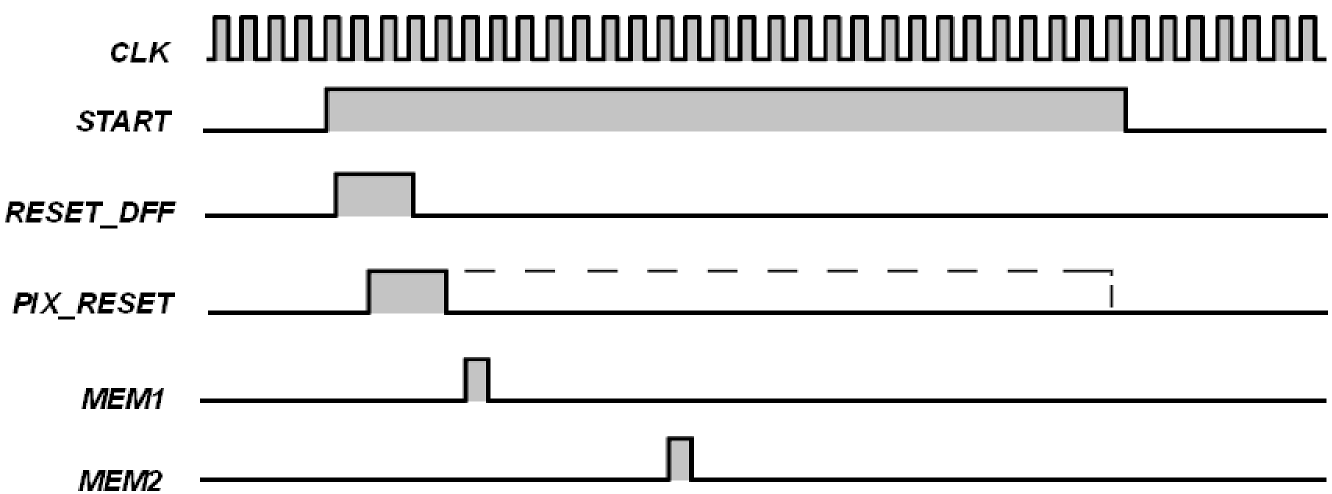
RESET_DFF

MEM1

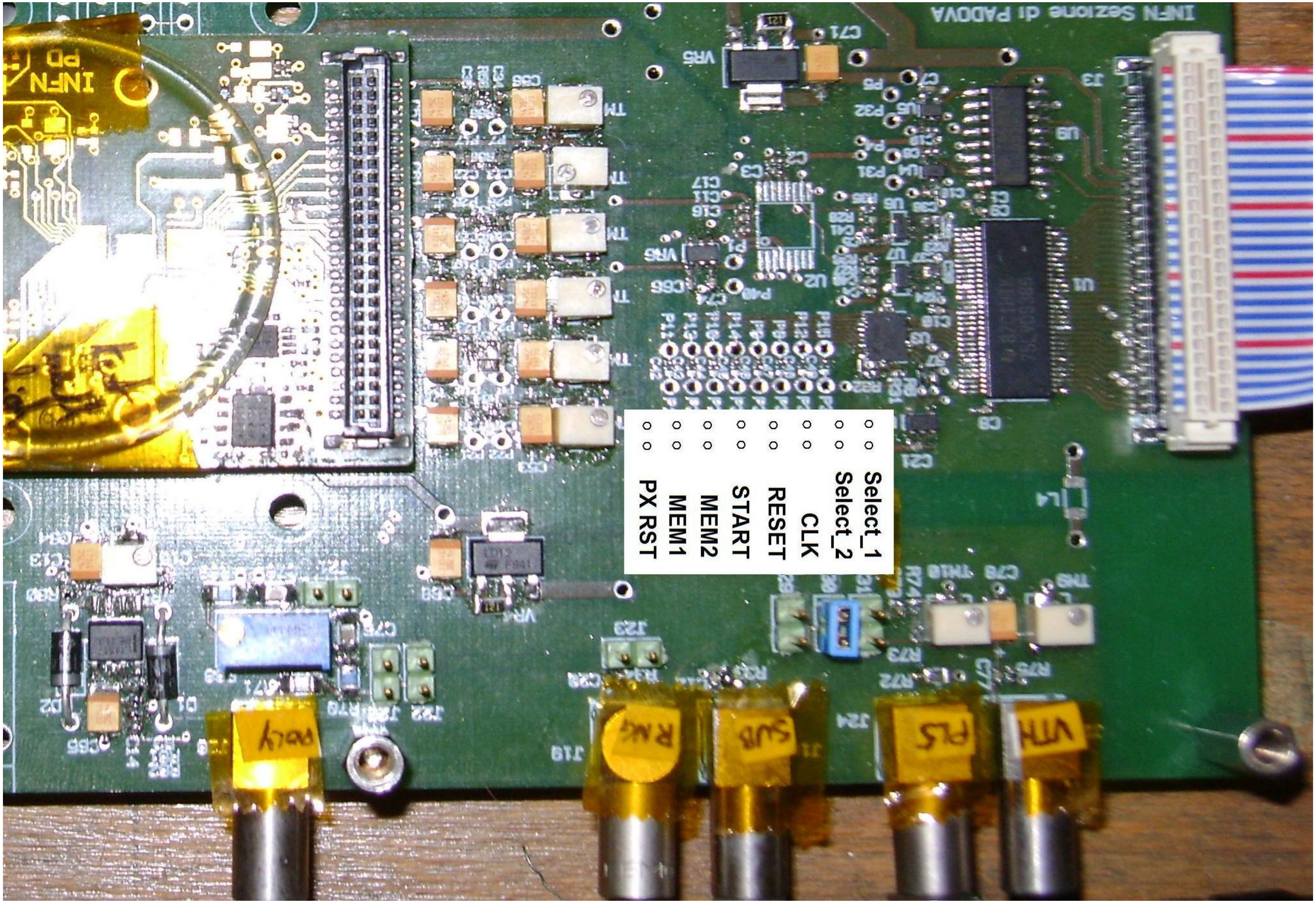
MEM2

PIX_RESET

(start/stop are defined in term of n = n clock cycles)



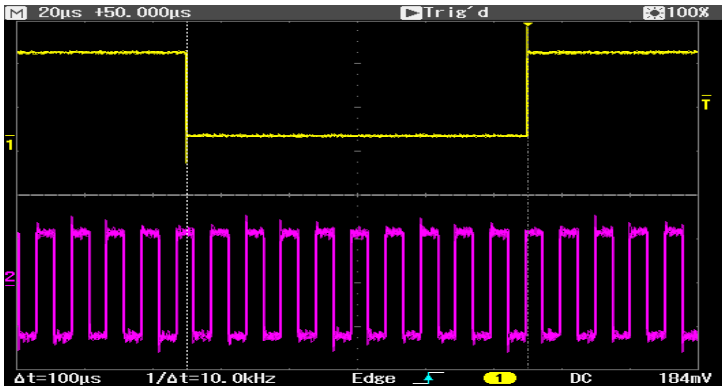
Control signals on the test PCB



Control signals at the oscilloscope

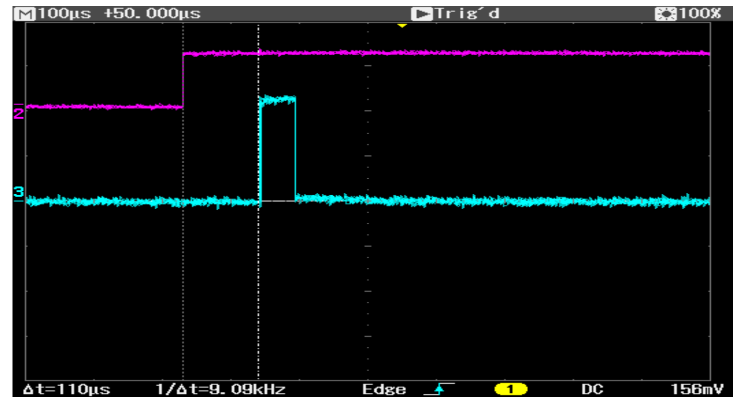
Getting started

Set a right timing for the control signal (check it out using the oscilloscope!)



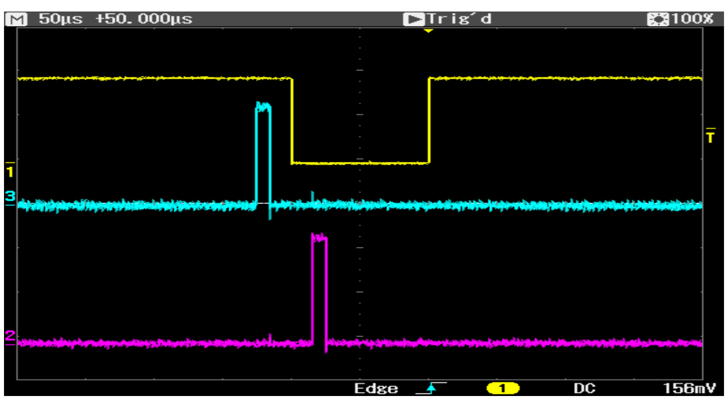
Vpulse

CLK



START

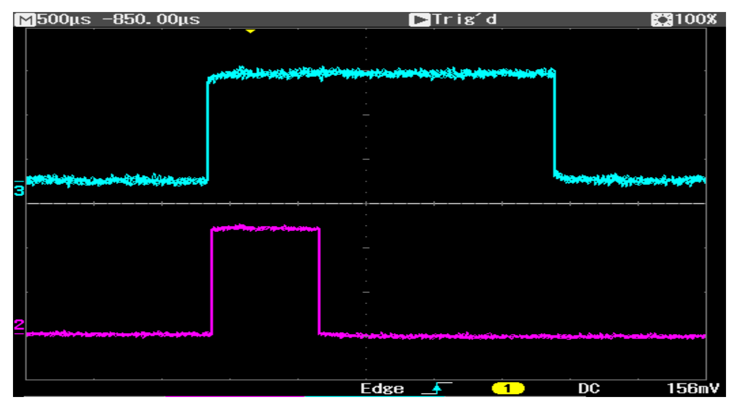
PIX_RESET



Vpulse

MEM1

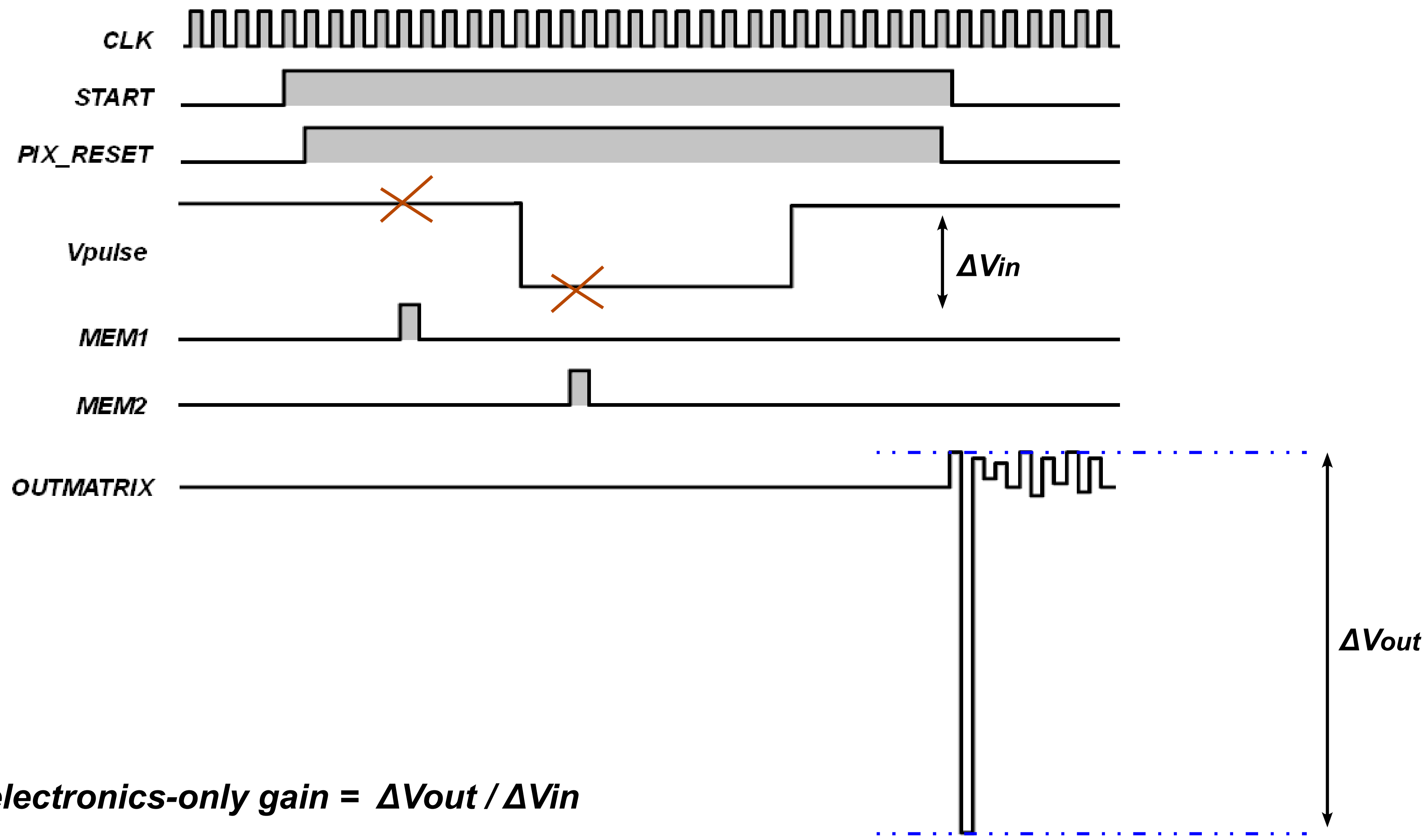
MEM2



START

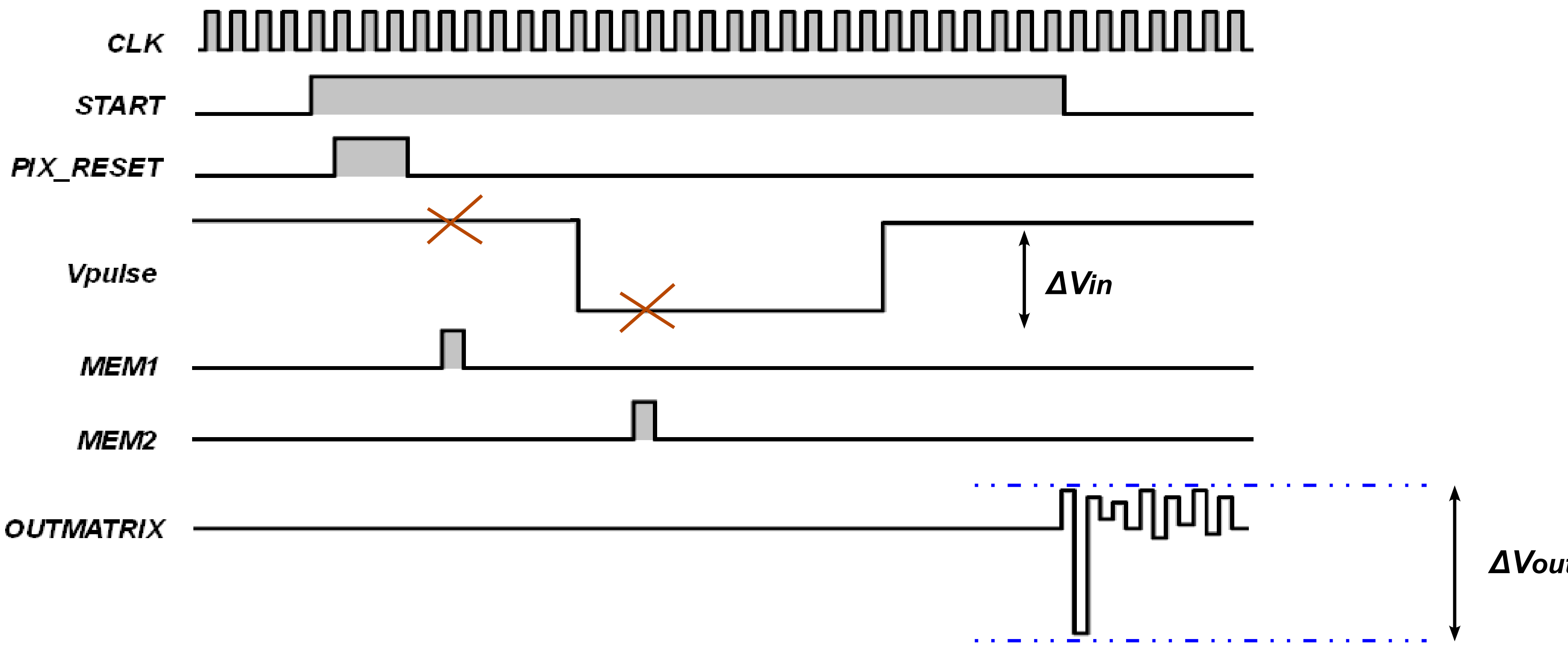
DFF_RESET

Test pulse measurements (1)



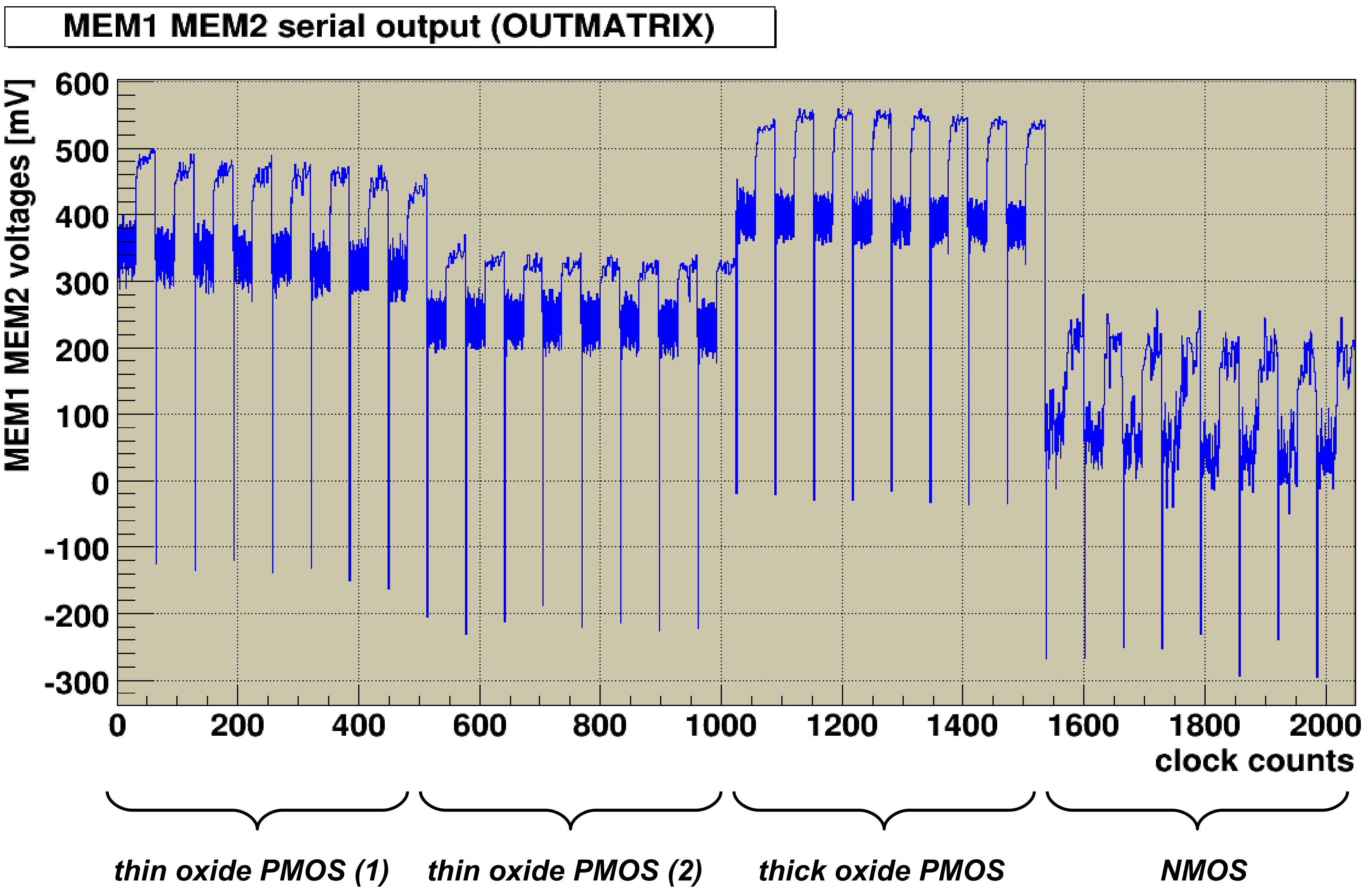
electronics-only gain = ΔVout / ΔVin

Test pulse measurements (2)

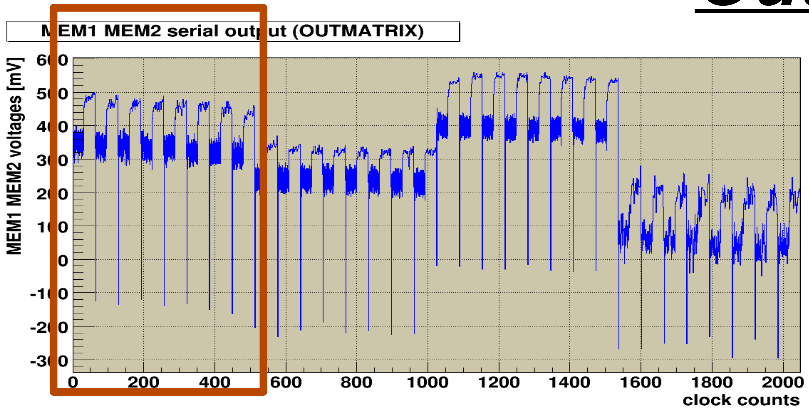


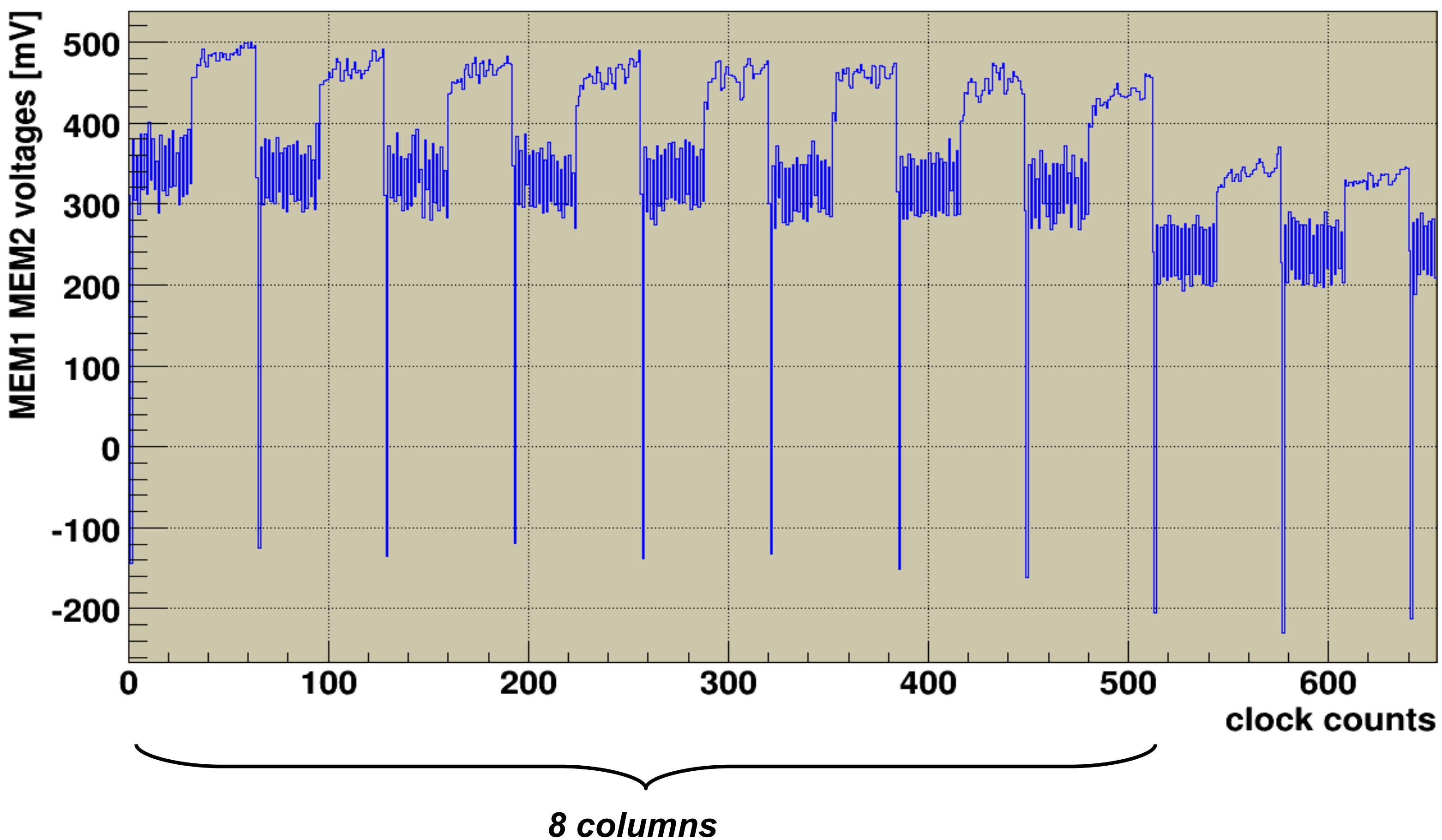
total gain (sensor + electronics) = ΔVout / ΔVin

Output waveform (OUTMATRIX)   (1)

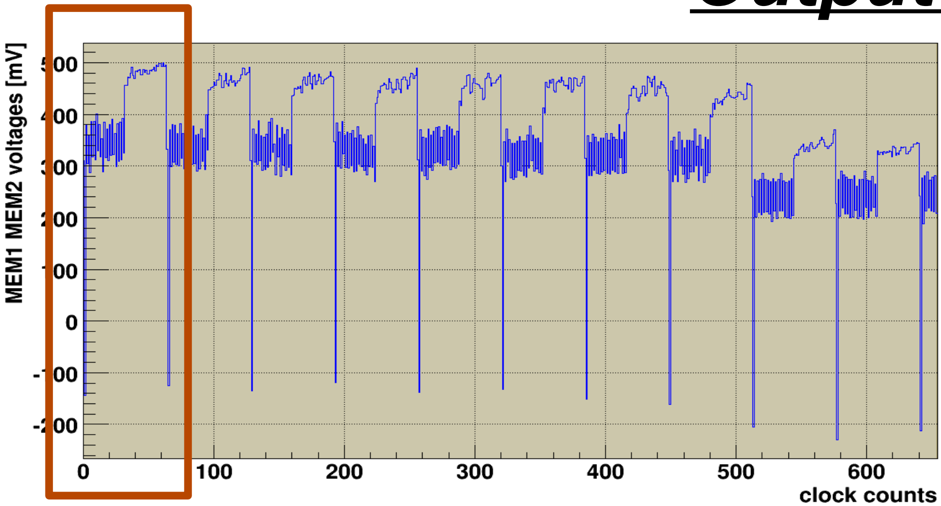


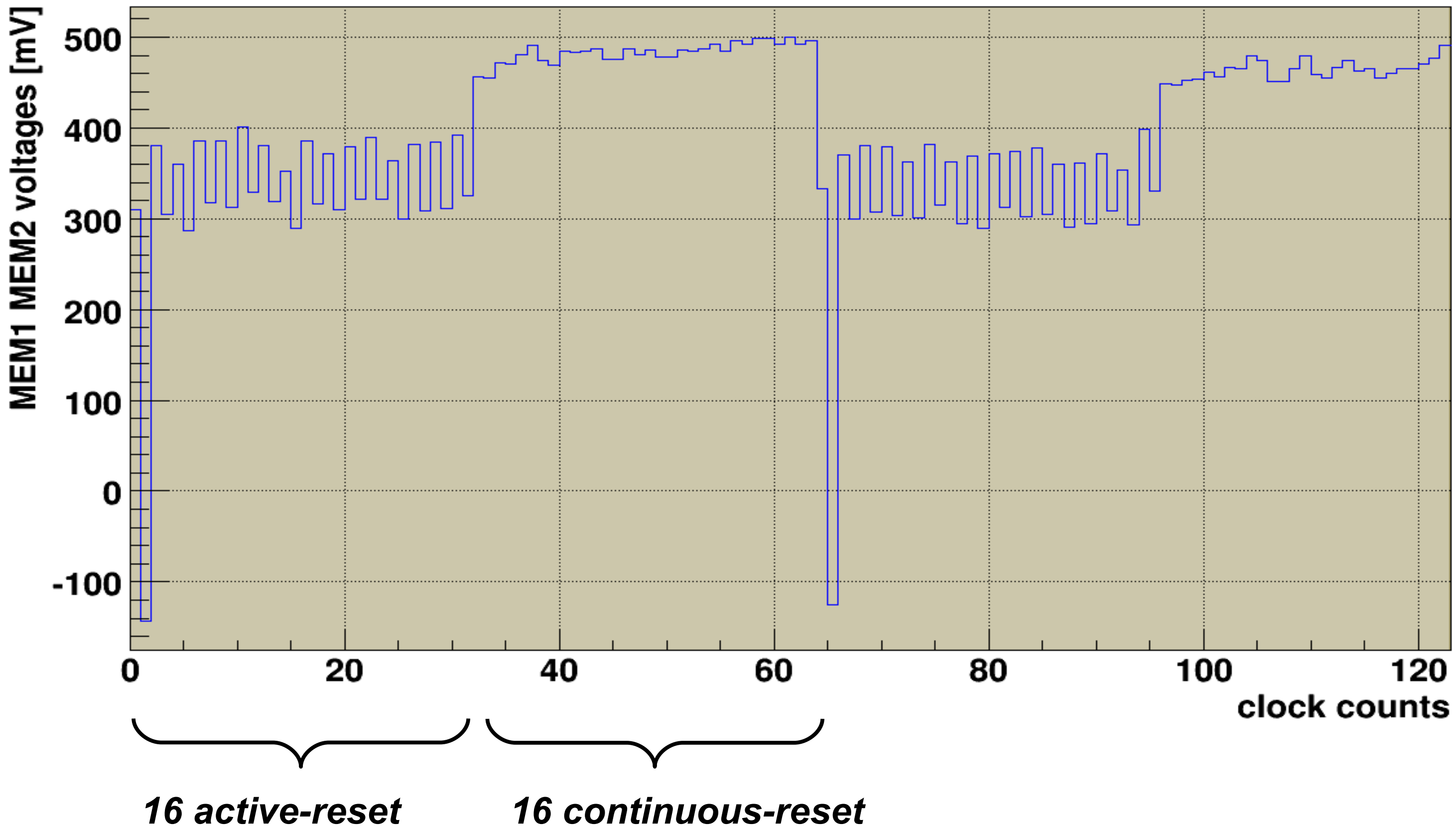
Output waveform (OUTMATRIX)   (2)



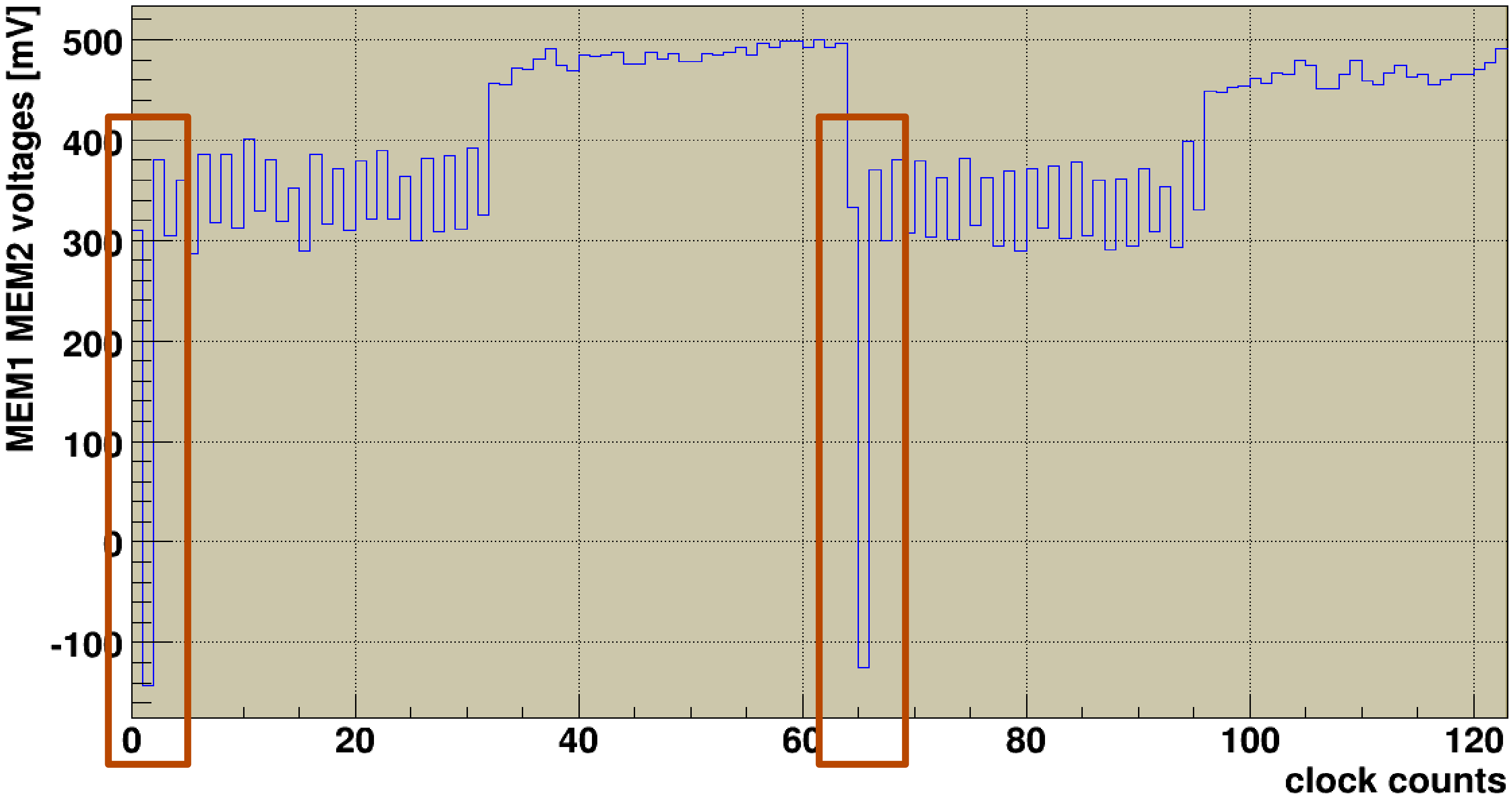


Output waveform (OUTMATRIX) (3)





Output waveform (OUTMATRIX)   (4)



pulsed pixel

pulsed pixel

Lab measurements (1)

Electronics gain measurements

Measure *ΔVout* at the oscilloscope for the first pulsed pixel by applying ***test pulses with different amplitudes*** *ΔVin*

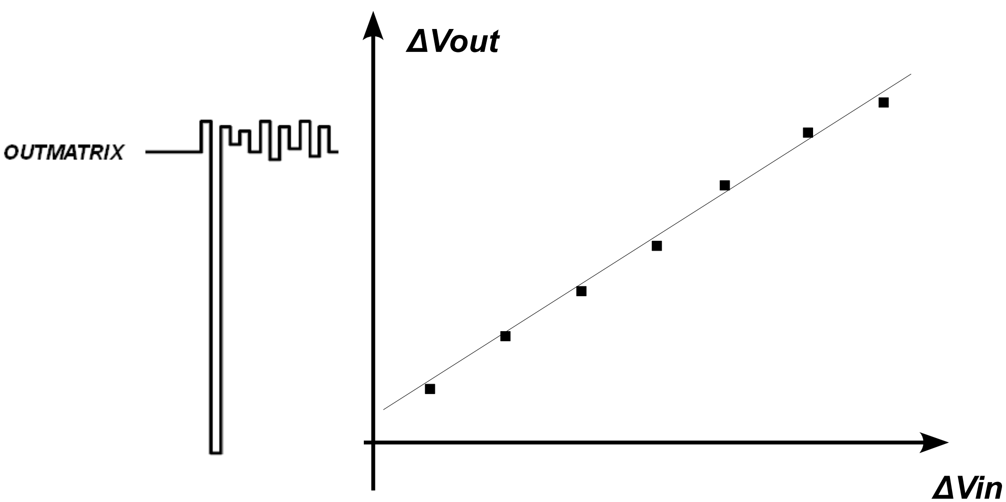
- excluding the sensor from read-out (***PIX_RESET*** always on) → ***electronics-only gain***
- including the sensor capacitance → ***sensor + electronics gain***

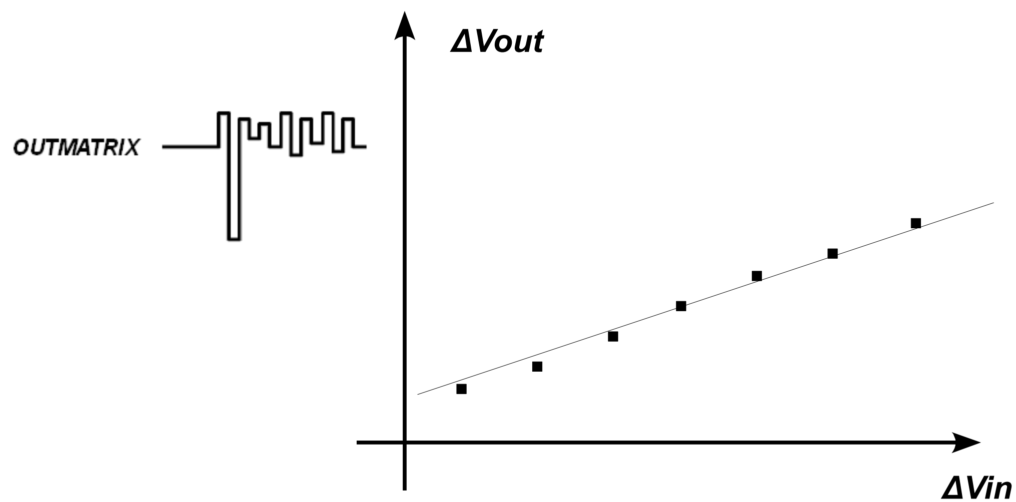
electronics-only (PIX_RESET always ON)

ΔVin	*ΔVout*
100 mV	...
200 mV	...
...	...

sensor + electronics

ΔVin	*ΔVout*
100 mV	...
200 mV	...
...	...

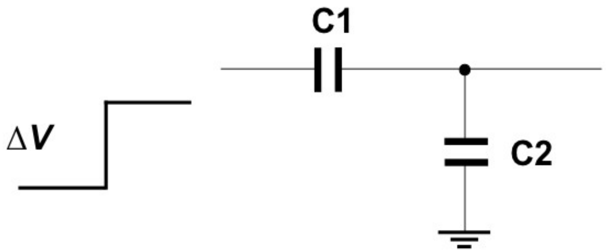




read-out voltage gain = ΔVout / Δvin → ***liner fit slope***

Lab measurements (2)

Refresh



$$V' = V_0 + \frac{C1}{C1 + C2} \Delta V$$

capacitive divider formula

Sensor capacitance estimation

An estimation of the pixel depletion capacitance can be obtained from electronics gain measurements:

total gain = (electronics-only gain) x (capacitive divider ratio)

from linear fits

$$\left(\frac{C_{test}}{C_{pix} + C_{test}} \right)$$

$$C_{test} = 1 \text{ fF } (10\%)$$

(from specs)

Make a comparison with capacitance values obtained for silicon strips…