

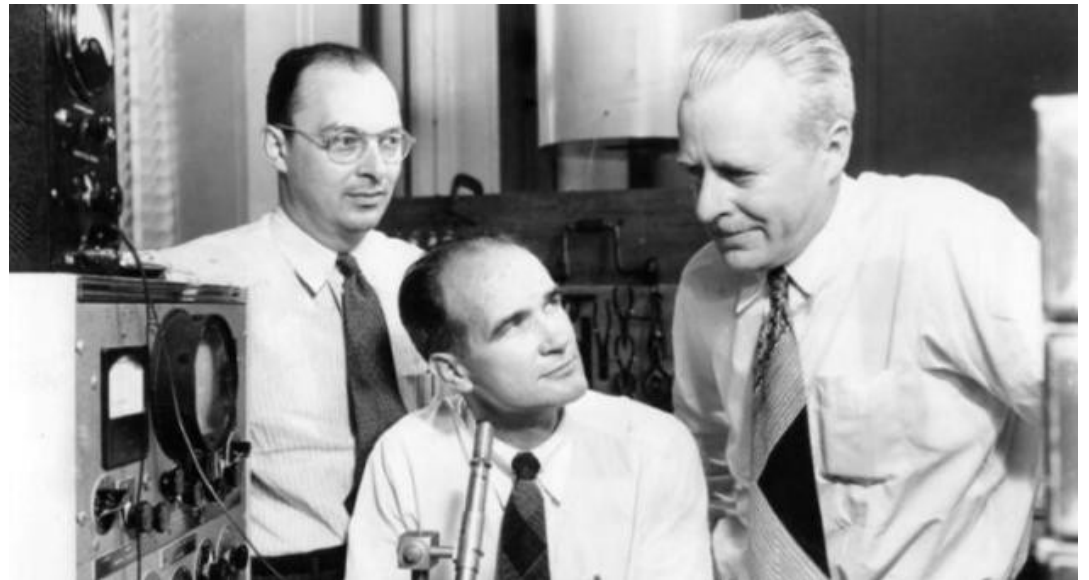
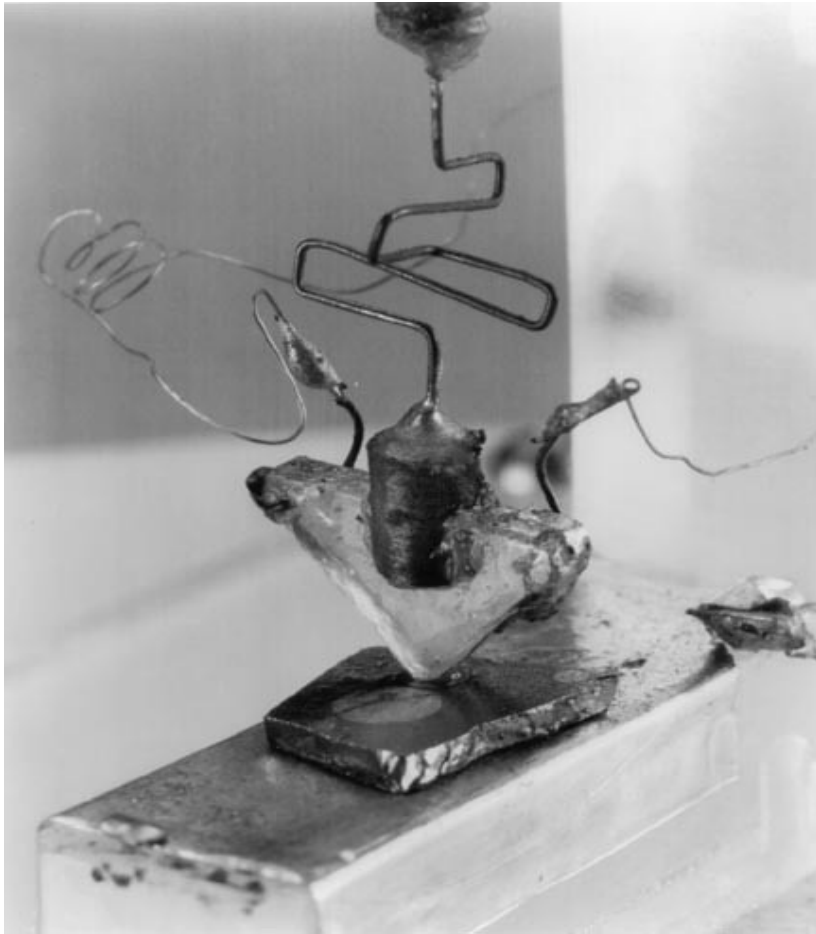
Esperimentazioni II
Traccia delle esercitazioni PSpice

L. Pacher
pacher@to.infn.it

Outline

- the Bipolar Junction Transistor (BJT), look at the blackboard...
- basic usage of PSpice 'on fly'
- lab. experience #8 - BJT characteristic curves
- lab. experience #9 - NPN common-emitter amplifier

The first transistor (1947)



J. Bardeen

W. Shockley

W. Brattain

1956 Nobel prize in Physics

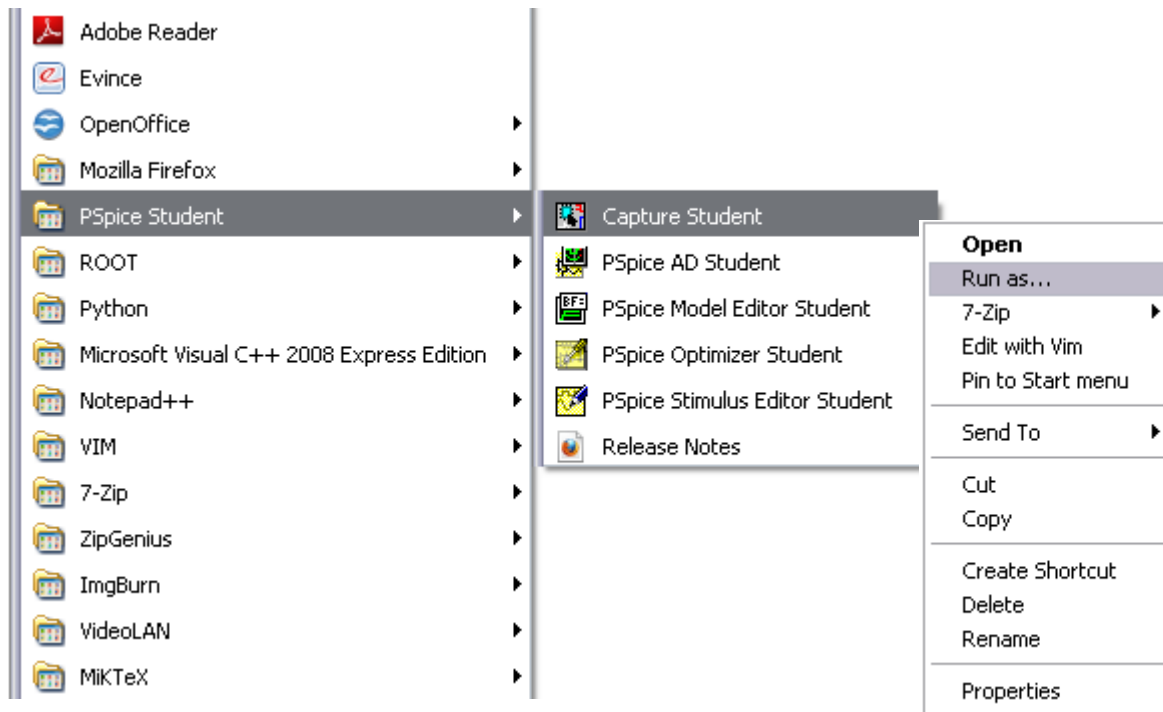
*“for their researches on semiconductors
and their discovery of the transistor effect”*

Uhm....

SPICE and PSpice

- Simulation Program with Integrated Circuits Emphasis, **SPICE**
- '*schematic*' is a meaningless word for a computer, just a human graphical visualization of the circuit
- a sort of interpreted '*markup and programming language*' with its own syntax, a plain text input file and another plain text output file
- the description of a circuit using the SPICE language is called *netlist*
- *SPICE file = netlist + electrical models + analysis directives*
- netlist and analysis directives are now *automatically generated* using *graphical interfaces*
- Personal **SPICE**, **PSpice** is commercial graphical front-end for personal computers running MS Windows operating systems
- the *student version* is free, of course with some limitations
- installation details are in the backup section

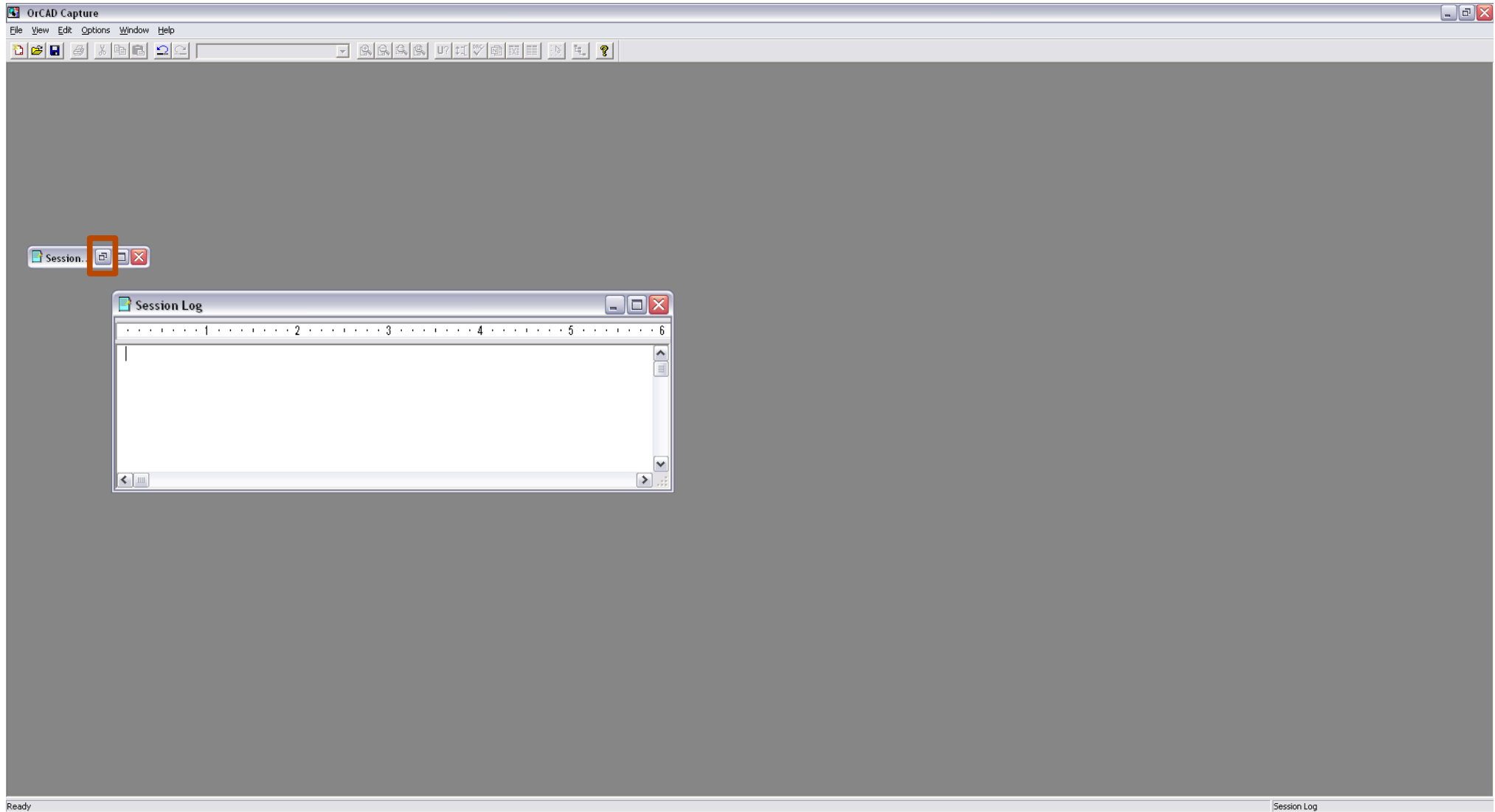
PSpice student



*Be sure to always run Capture with **high privileges!** Pspice simulation files require some (not well defined...) write privileges*

- ***Capture*** - schematic entry tool
- ***PSpice A/D*** - analog, digital and mixed-signals circuit simulator
- ***PSpice Model Editor*** - edit plain text SPICE models or extract models from data sheets
- ***PSpice Stimulus Editor*** – graphical editor for time-based waveforms

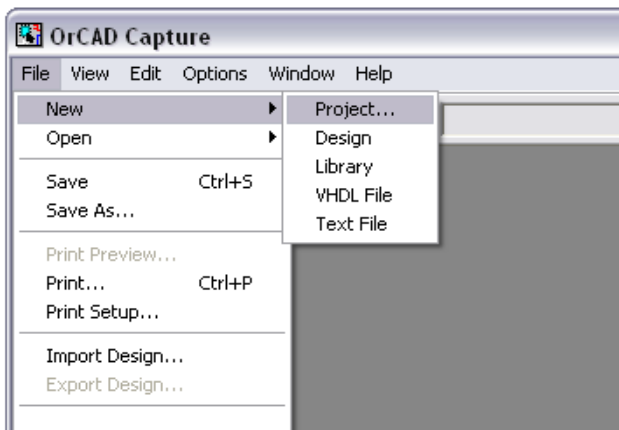
Getting started



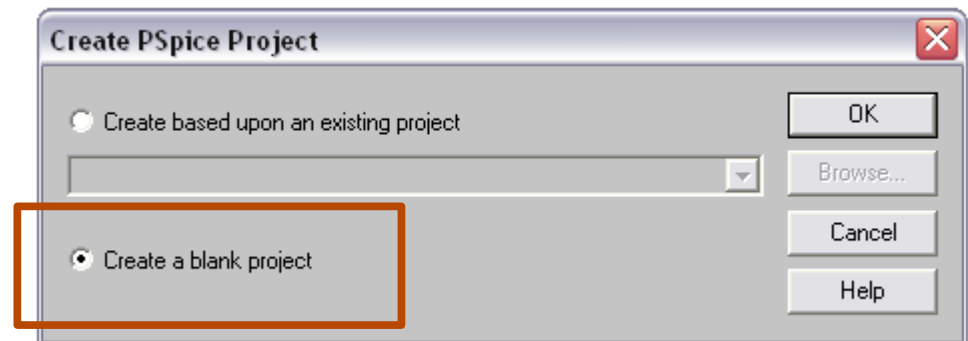
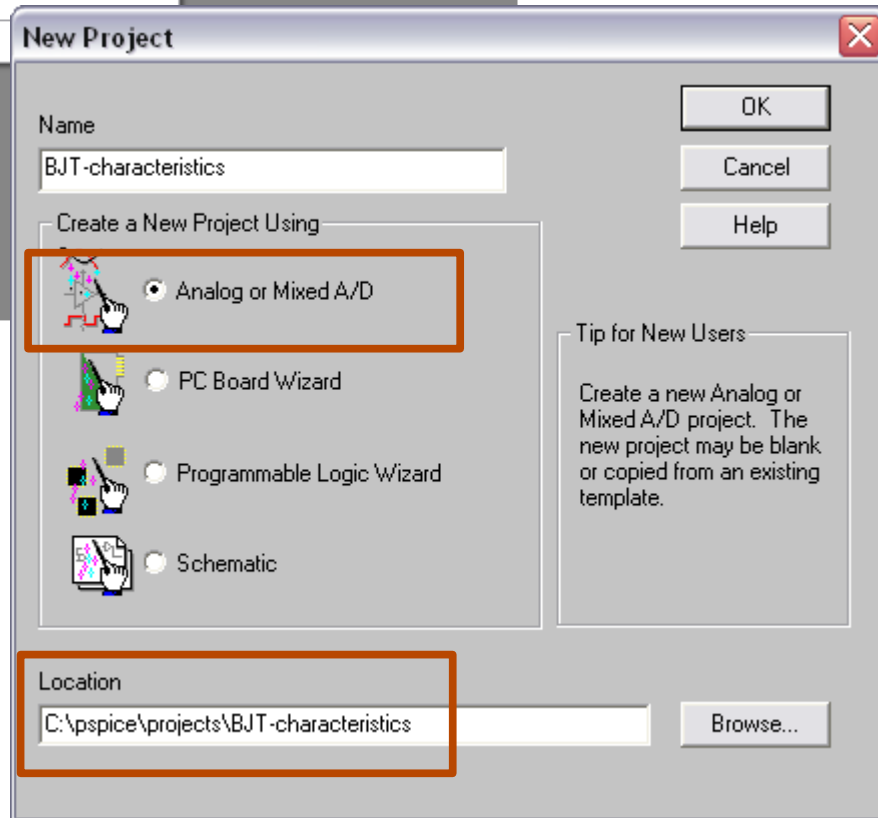
The **Session Log** keeps trace of your work... and highlights possible **errors** !

Create a new project

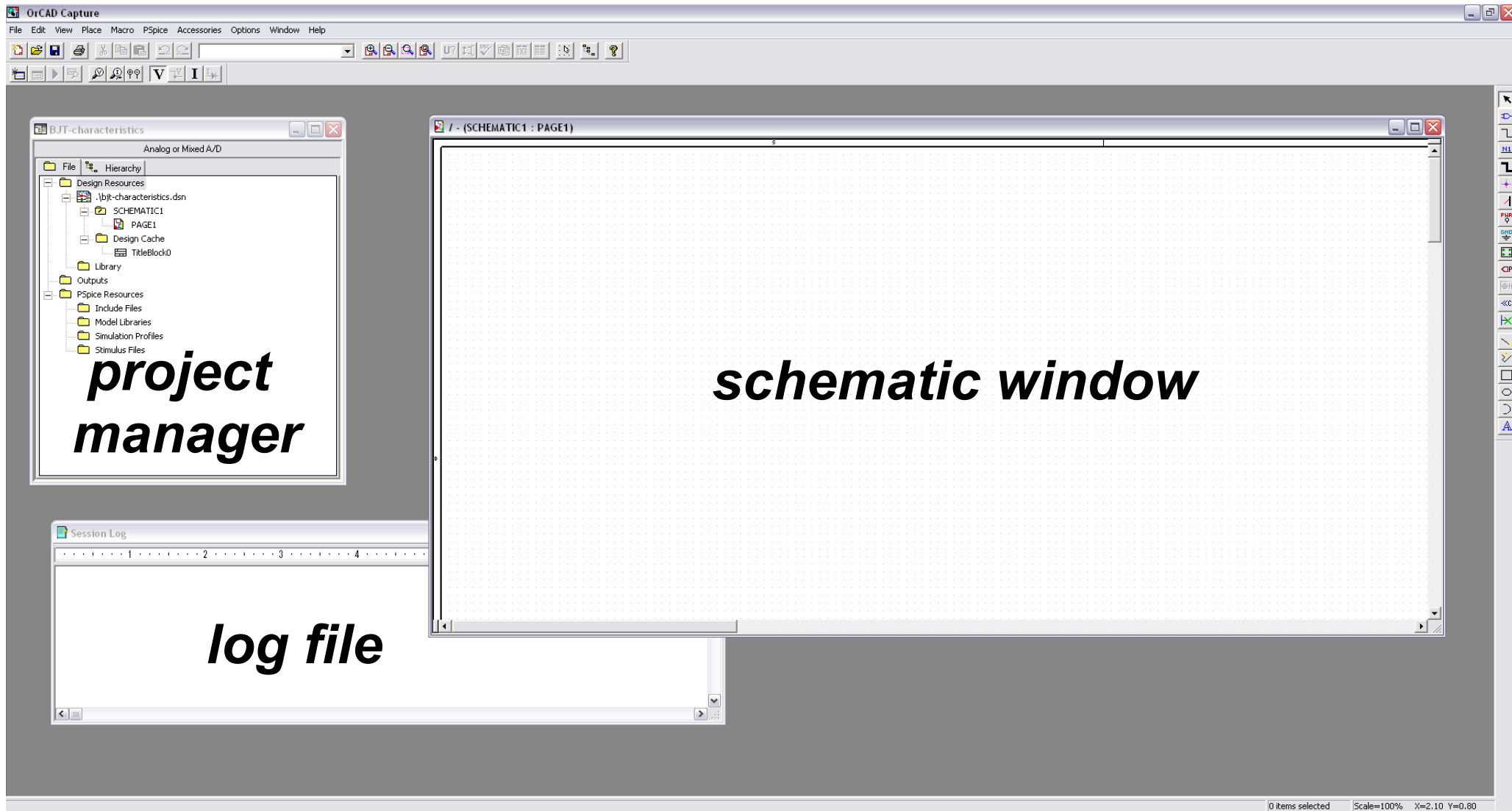
File → New → Project...



- your work is organized into **projects** (.opj main file)
- specify a new folder in C:\pspice\projects with the same name of the project
- simulations with PSpice are available **only** if you choose the **Analog or Mixed A/D** option

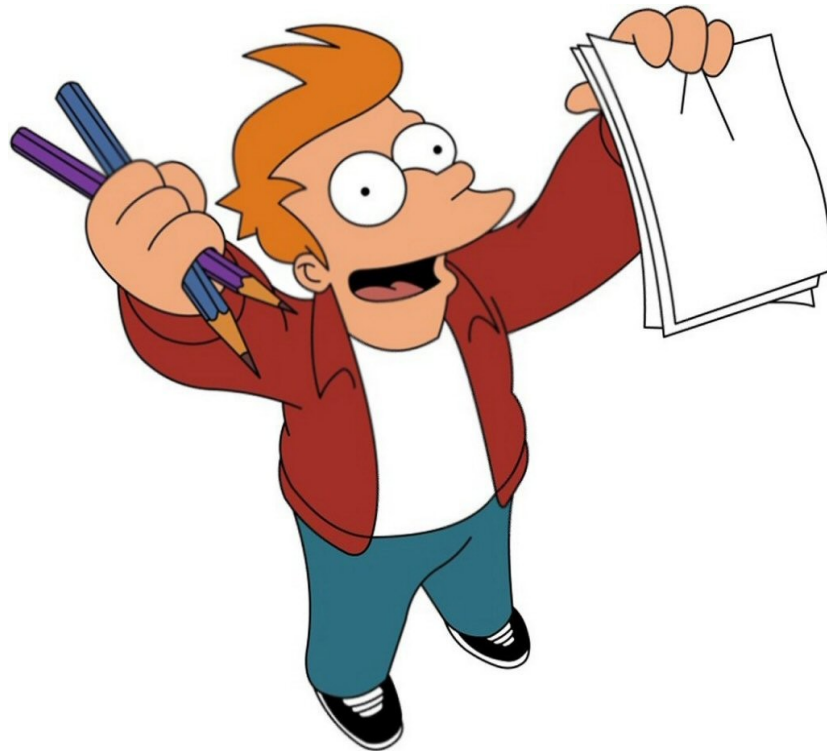


The graphical interface



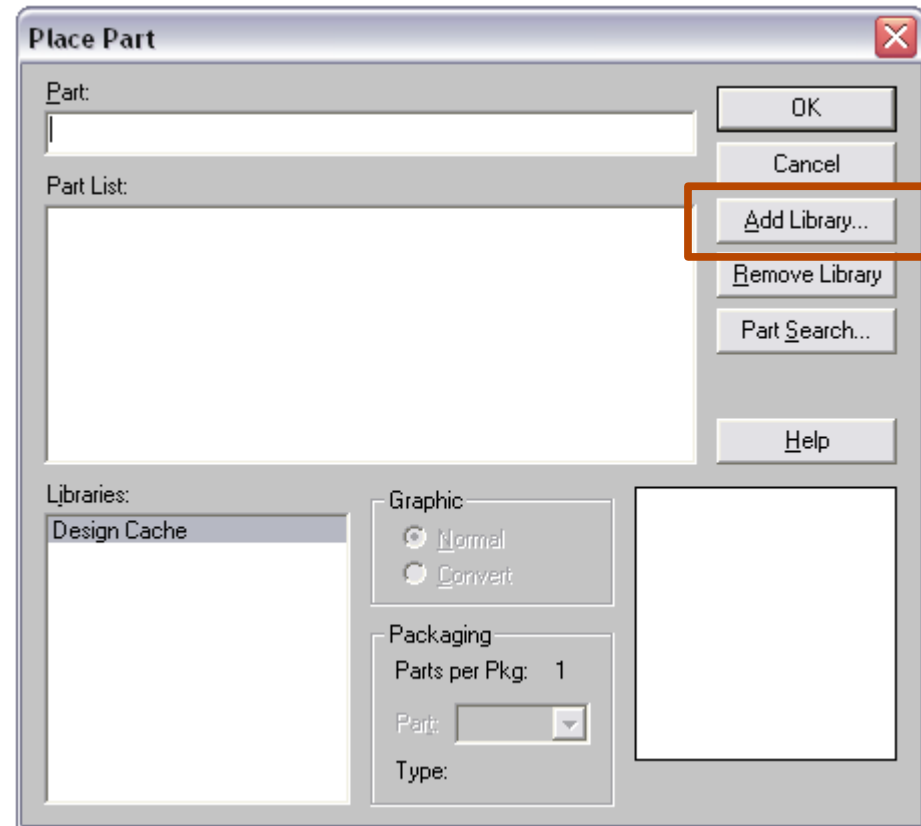
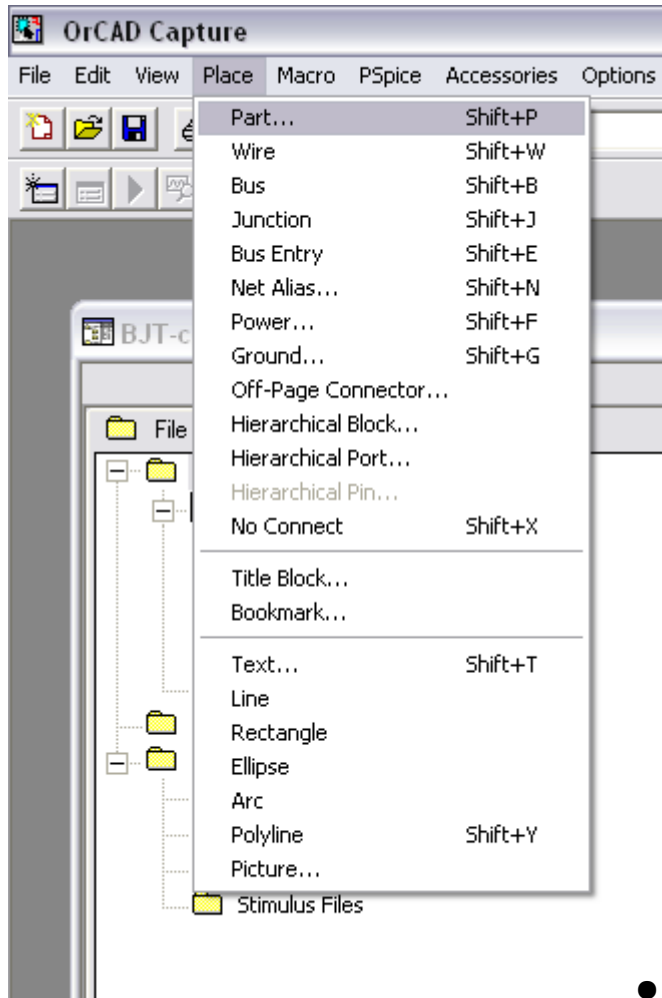
Part I

Schematic entry



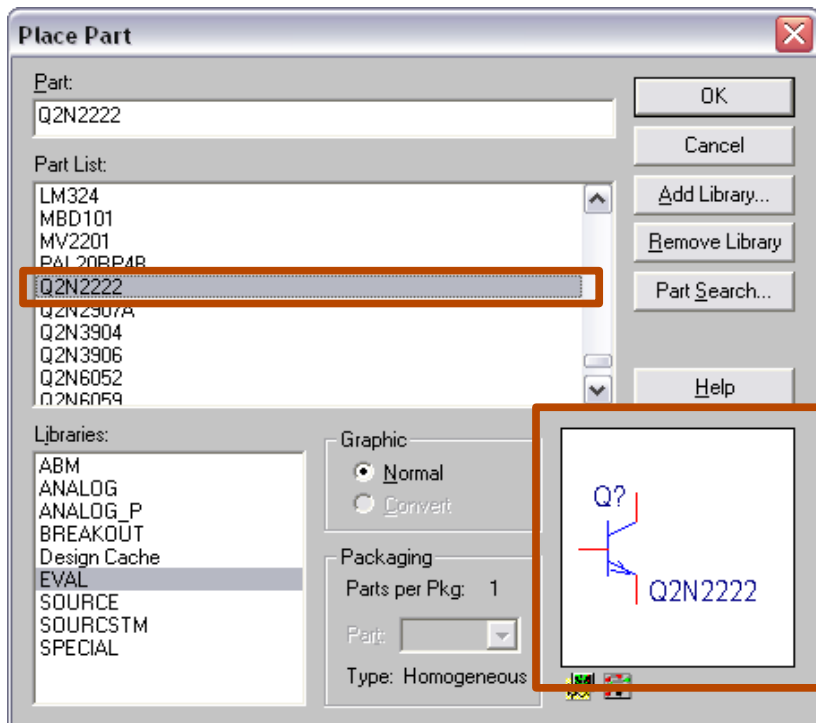
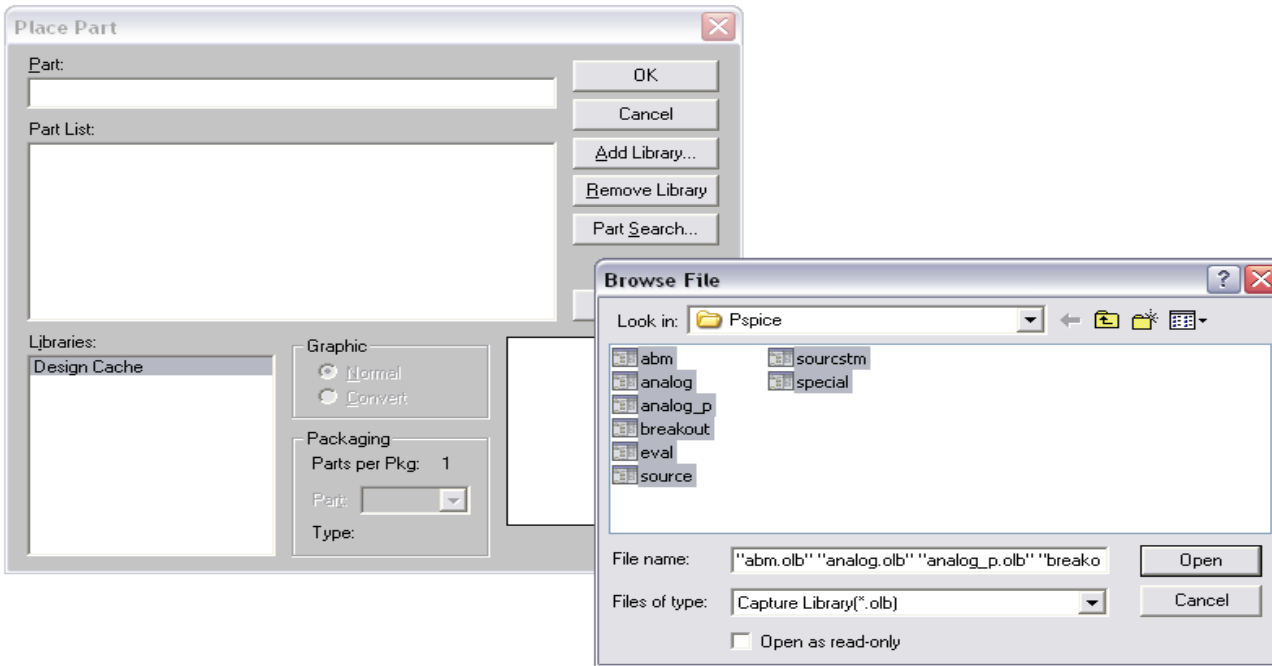
Place components

Place → Part...



- **symbols** of electrical components are organized into **libraries**
- the first time you are using PSpice you have to import the basic libraries

Basic libraries



- **ANALOG** contains ideal R, L, C and controlled voltage/current sources
- **BREAKOUT** contains *ideal semiconductor devices* (transistors, diodes etc.)
- **EVAL** contains a list of *real semiconductor devices* (diodes, transistors, logic gates, OPAMP etc.)
- **SOURCE** contains ideal voltage and current sources

NPN 2N2222

Check the datasheet!

Philips Semiconductors

Product specification

NPN switching transistors

2N2222; 2N2222A

FEATURES

- ∞ High current (max. 800 mA)
- ∞ Low voltage (max. 40 V).

APPLICATIONS

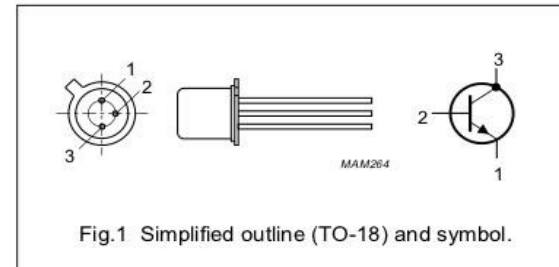
- ∞ Linear amplification and switching.

DESCRIPTION

NPN switching transistor in a TO-18 metal package.
PNP complement: 2N2907A.

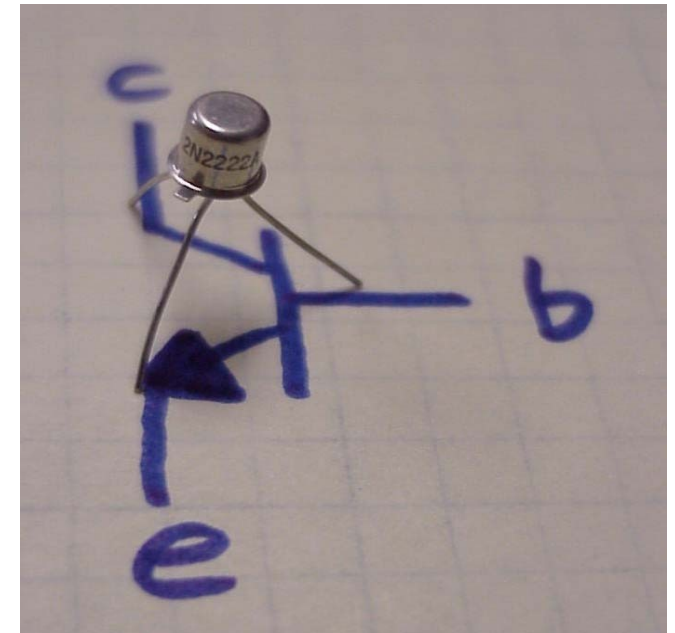
PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector, connected to case



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	2N2222		–	60	V
	2N2222A		–	75	V
V_{CEO}	collector-emitter voltage	open base			
	2N2222		–	30	V
	2N2222A		–	40	V
I_C	collector current (DC)		–	800	mA
P_{tot}	total power dissipation	$T_{amb} = 25 \text{ }^\circ\text{C}$	–	500	mW
h_{FE}	DC current gain	$I_C = 10 \text{ mA}; V_{CE} = 10 \text{ V}$	75	–	
f_T	transition frequency	$I_C = 20 \text{ mA}; V_{CE} = 20 \text{ V}; f = 100 \text{ MHz}$			
	2N2222		250	–	MHz
	2N2222A		300	–	MHz
t_{off}	turn-off time	$I_{Con} = 150 \text{ mA}; I_{Bon} = 15 \text{ mA}; I_{Boff} = -15 \text{ mA}$	–	250	ns



A general-purpose commercial BJT

NPN TIP31

Check the datasheet again!

TIP31, TIP31A, TIP31B, TIP31C NPN SILICON POWER TRANSISTORS

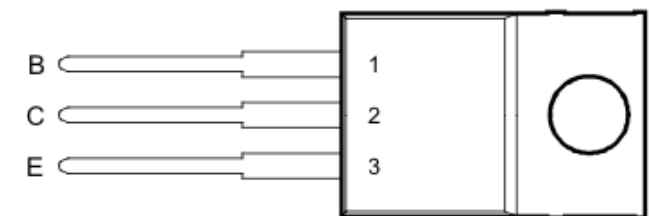
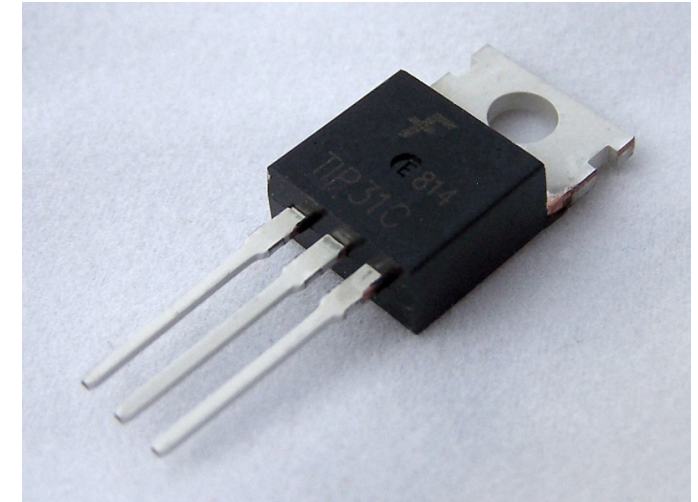
JULY 1968 - REVISED MARCH 1997

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$ Collector-emitter breakdown voltage	$I_C = 30 \text{ mA}$ (see Note 5) $I_B = 0$	TIP31 40 TIP31A 60 TIP31B 80 TIP31C 100			V
I_{CES} Collector-emitter cut-off current	$V_{CE} = 80 \text{ V}$ $V_{CE} = 100 \text{ V}$ $V_{CE} = 120 \text{ V}$ $V_{CE} = 140 \text{ V}$ $V_{BE} = 0$ $V_{BE} = 0$ $V_{BE} = 0$ $V_{BE} = 0$			0.2 0.2 0.2 0.2	mA
I_{CEO} Collector cut-off current	$V_{CE} = 30 \text{ V}$ $V_{CE} = 60 \text{ V}$ $I_B = 0$ $I_B = 0$			0.3 0.3	mA
I_{EBO} Emitter cut-off current	$V_{EB} = 5 \text{ V}$ $I_C = 0$			1	mA
h_{FE} Forward current transfer ratio	$V_{CE} = 4 \text{ V}$ $V_{CE} = 4 \text{ V}$ $I_C = 1 \text{ A}$ $I_C = 3 \text{ A}$ (see Notes 5 and 6)	25 10		50	
$V_{CE(sat)}$ Collector-emitter saturation voltage	$I_B = 375 \text{ mA}$ $I_C = 3 \text{ A}$ (see Notes 5 and 6)			1.2	V
V_{BE} Base-emitter voltage	$V_{CE} = 4 \text{ V}$ $I_C = 3 \text{ A}$ (see Notes 5 and 6)			1.8	V
h_{fe} Small signal forward current transfer ratio	$V_{CE} = 10 \text{ V}$ $I_C = 0.5 \text{ A}$ $f = 1 \text{ kHz}$	20			
$ h_{fe} $ Small signal forward current transfer ratio	$V_{CE} = 10 \text{ V}$ $I_C = 0.5 \text{ A}$ $f = 1 \text{ MHz}$	3			

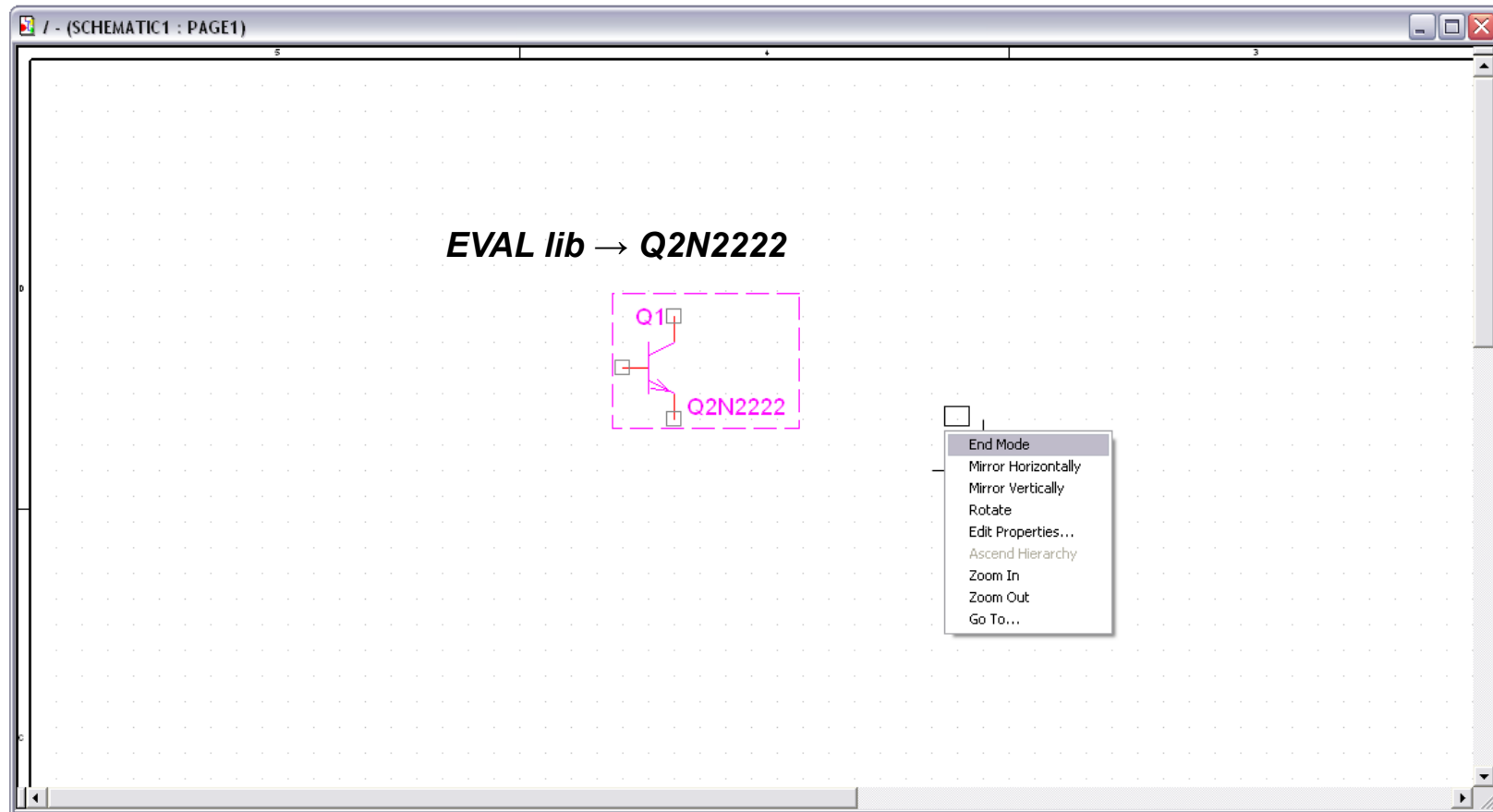
NOTES: 5. These parameters must be measured using pulse techniques, $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters must be measured using voltage-sensing contacts, separate from the current carrying contacts.

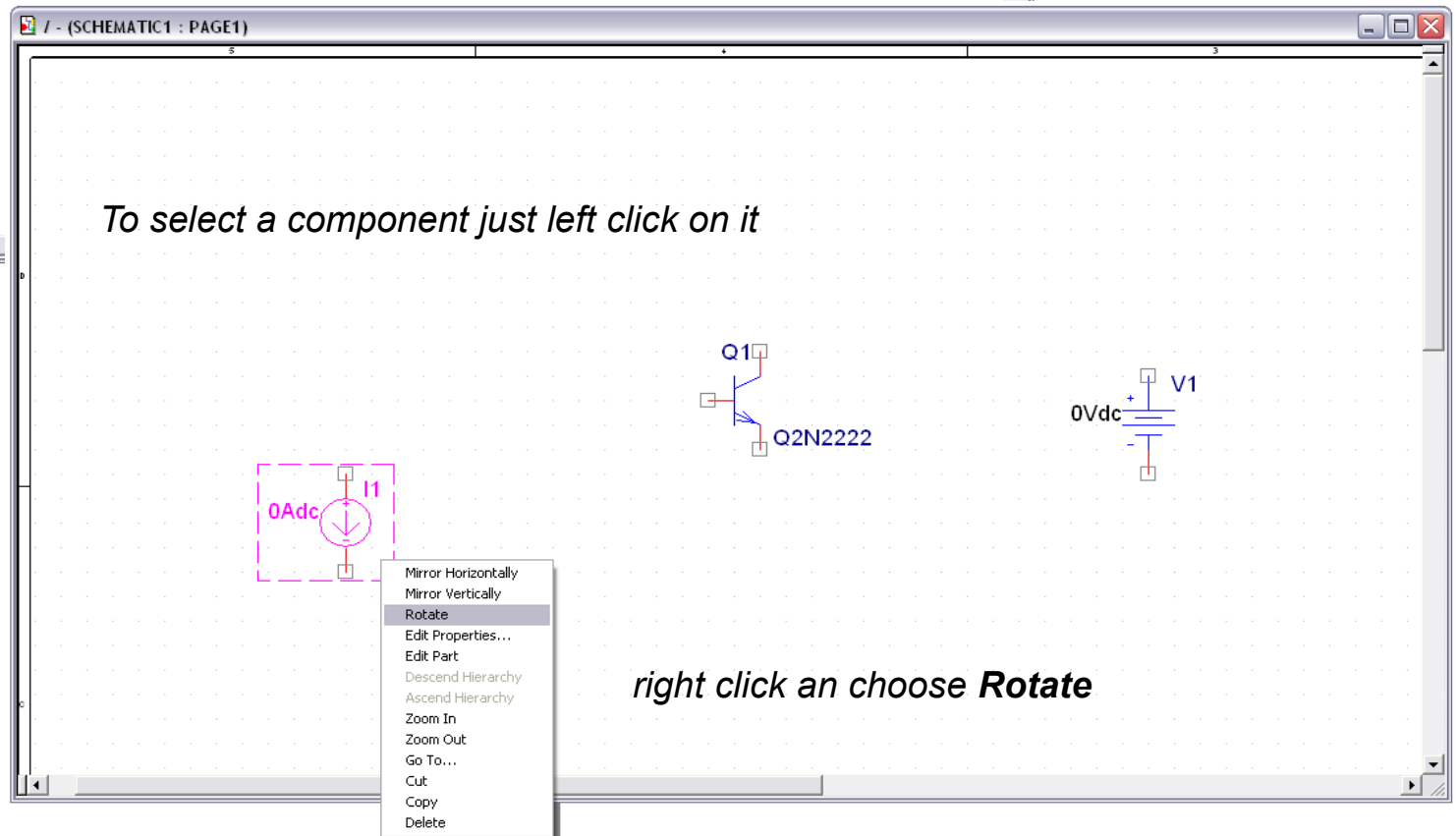
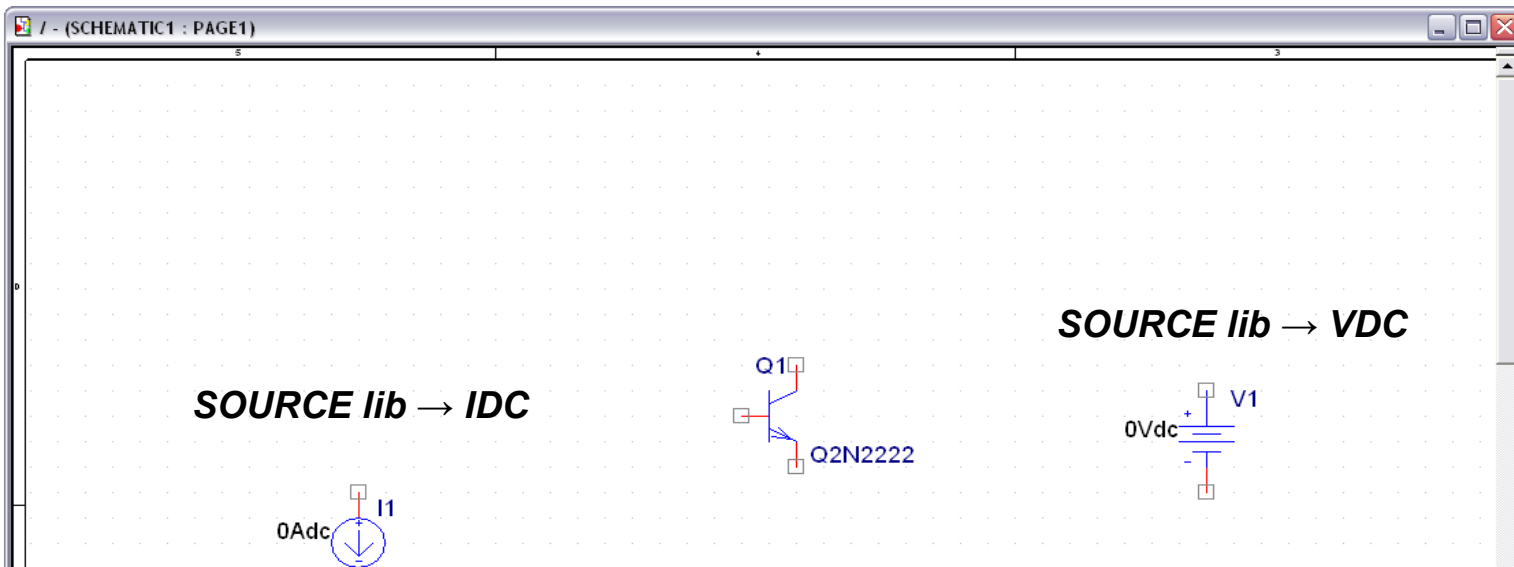


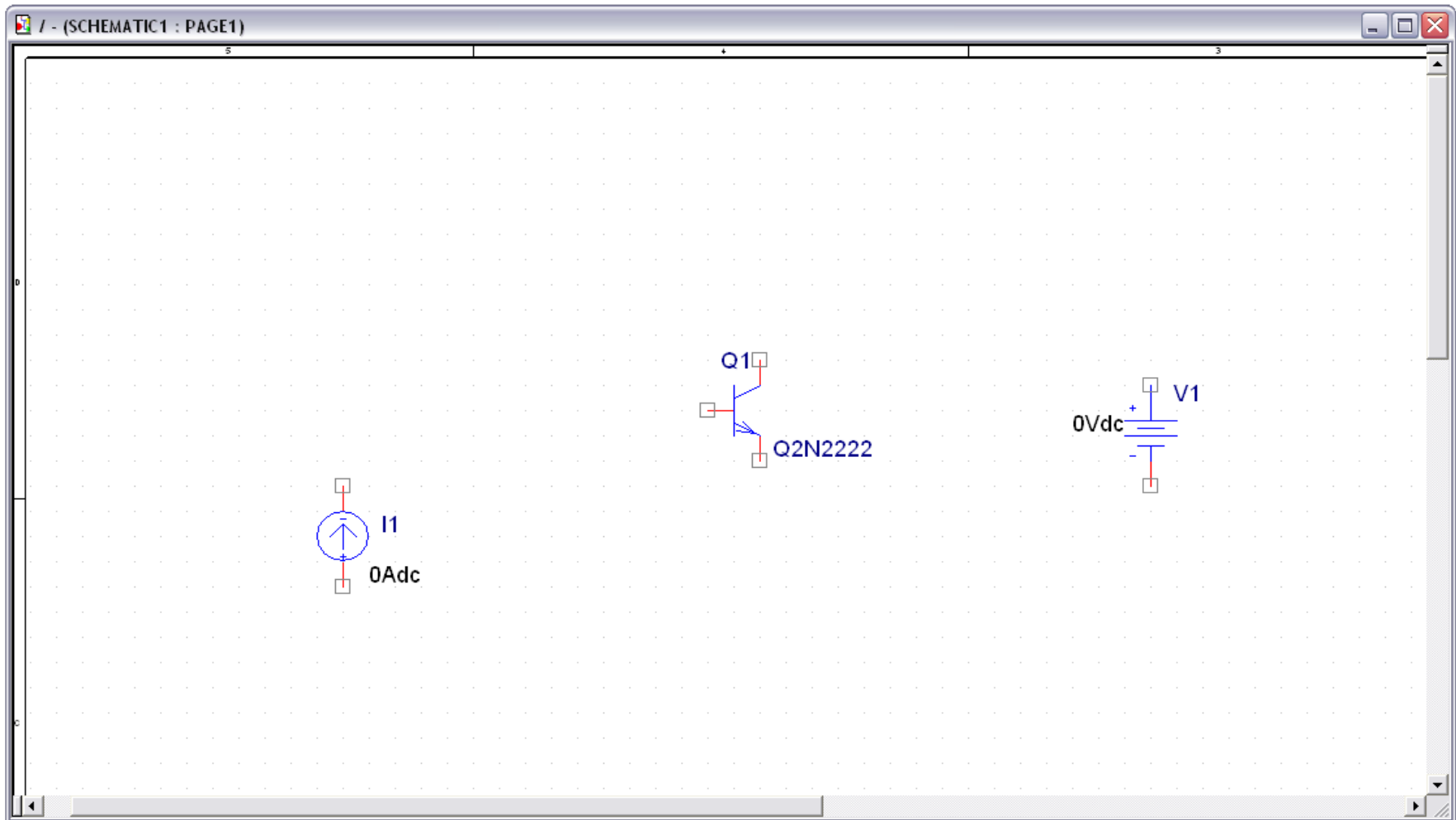
Another general-purpose commercial BJT

This should be the transistor available for your experimental measurements in lab...



You can place multiple instances of the same component, press **ESC** or **right click** → **End Mode** to come back to the select mode



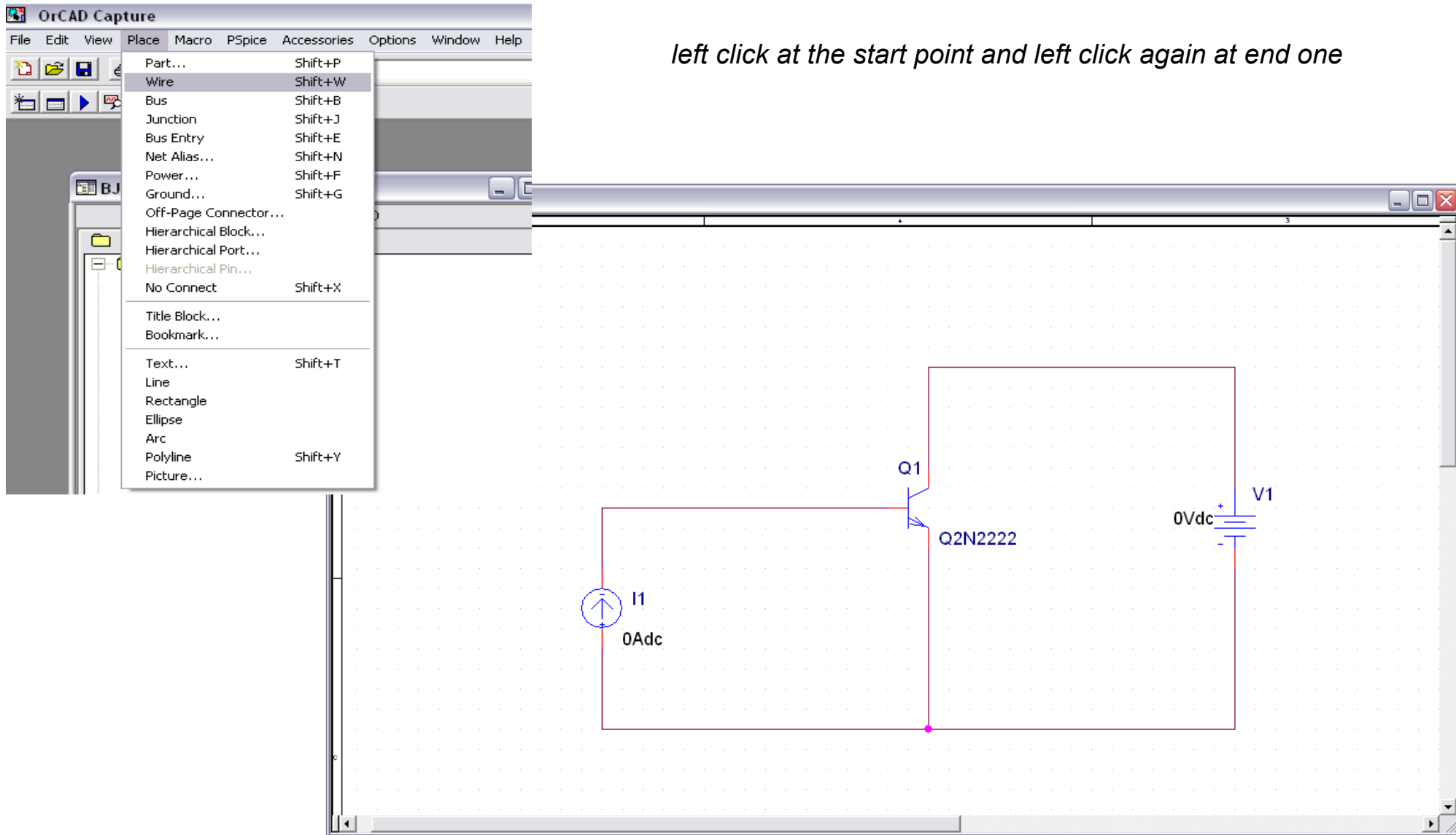


Components are on the table, now we have to make connections...

Make connections

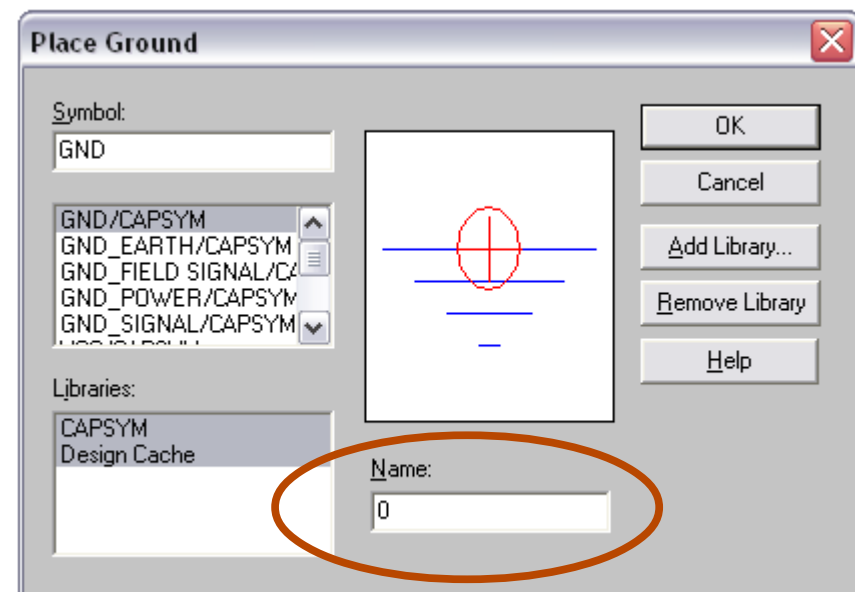
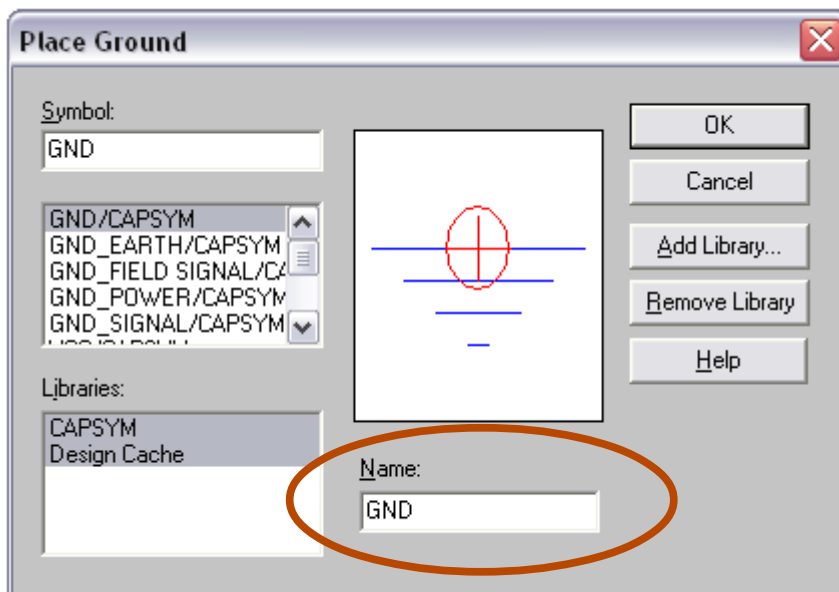
Place → Wire...

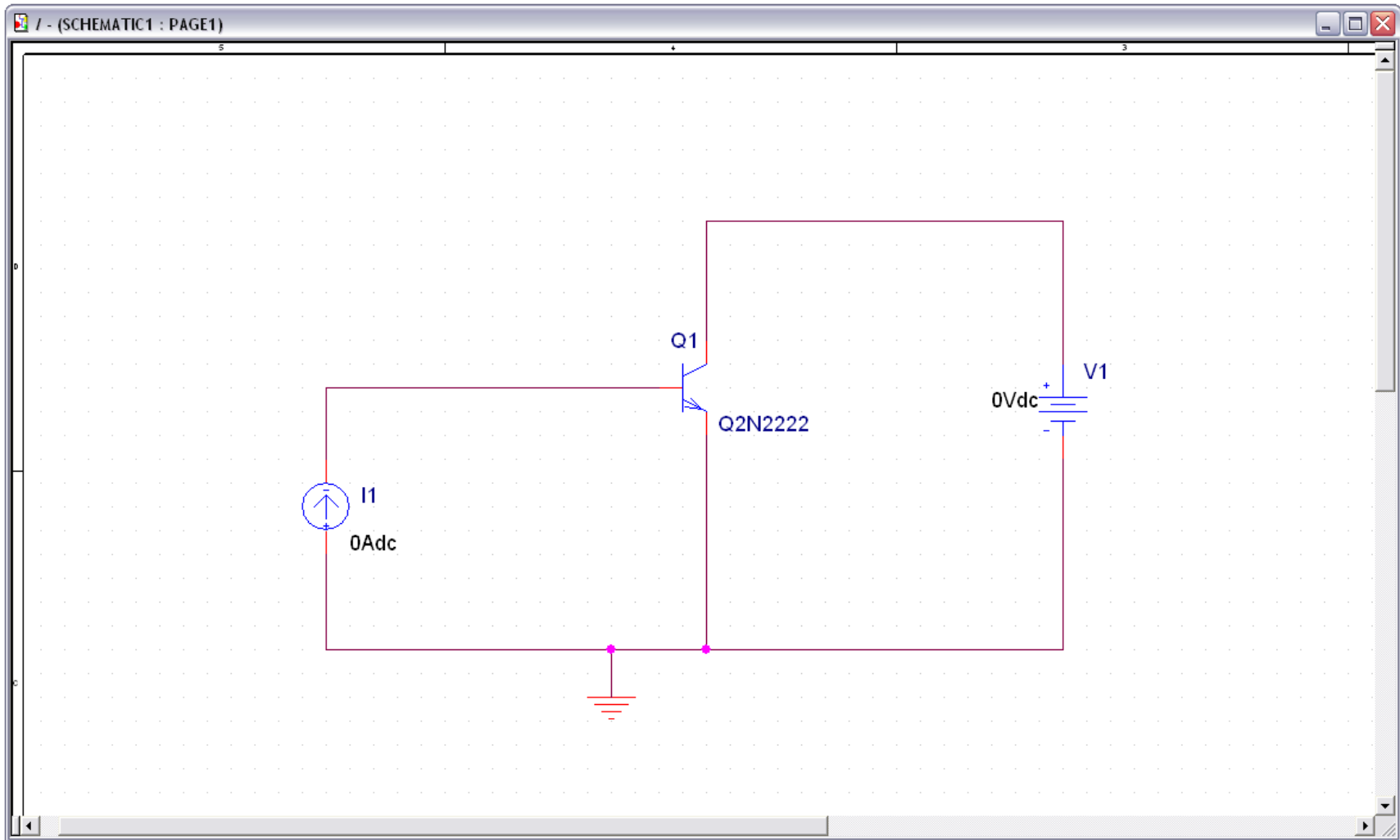
left click at the start point and left click again at end one



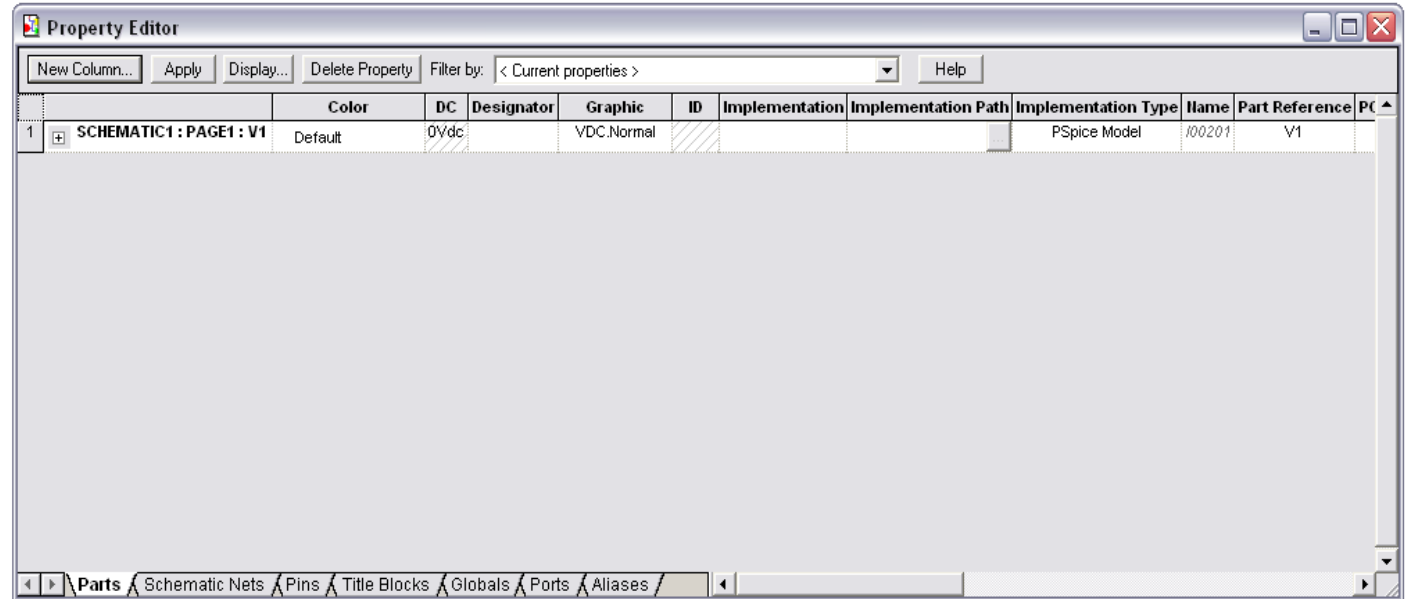
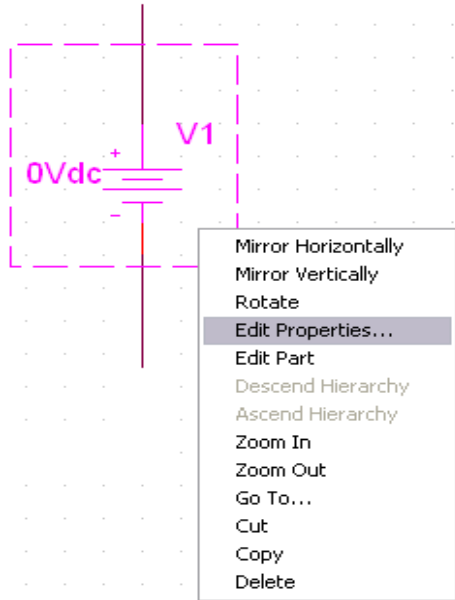
Place grounds

- at least one node **MUST be named 0** for the common reference voltage (*floating-node errors* otherwise)
- **Place** → **Ground...**
- use for instance **CAPSYM /GND** symbol but **change Name into 0 !**

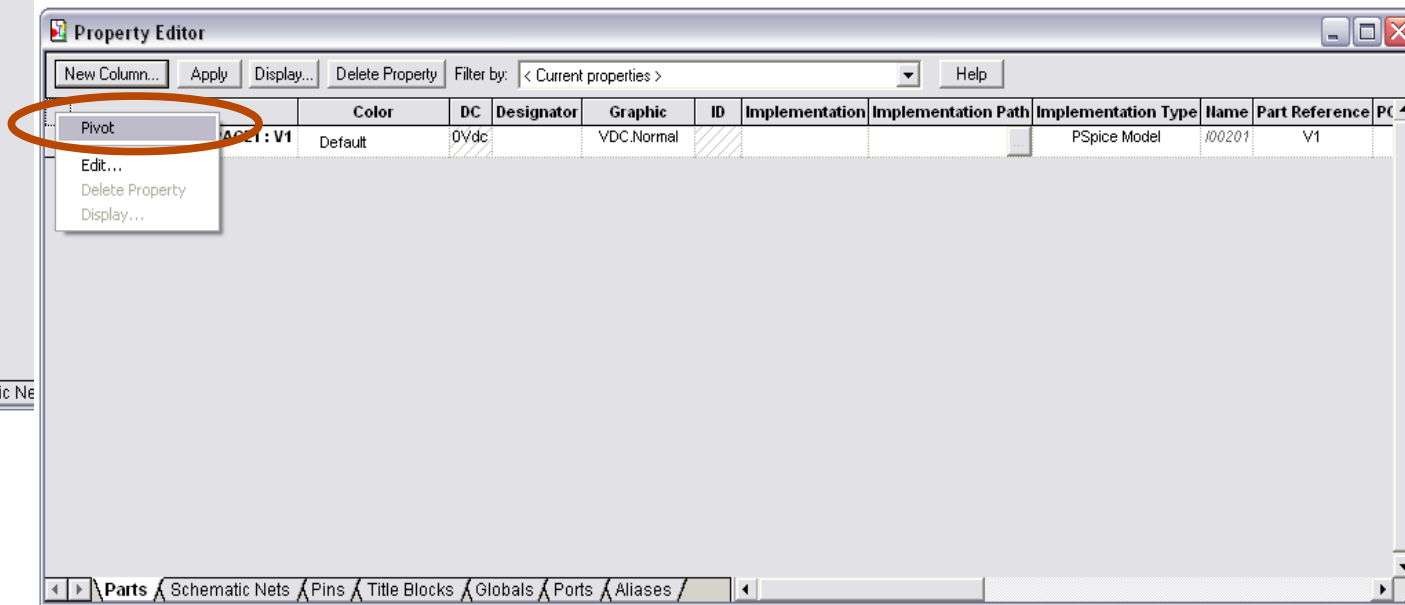
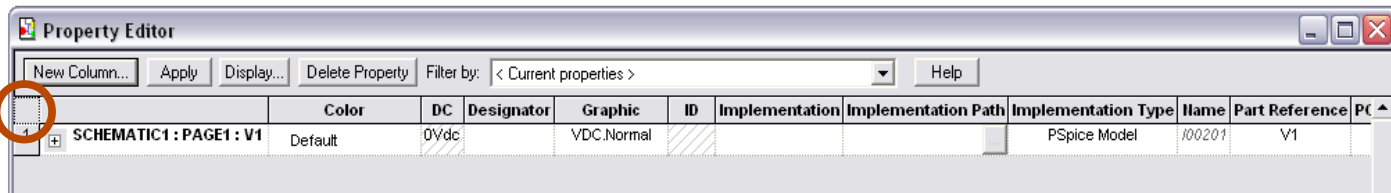




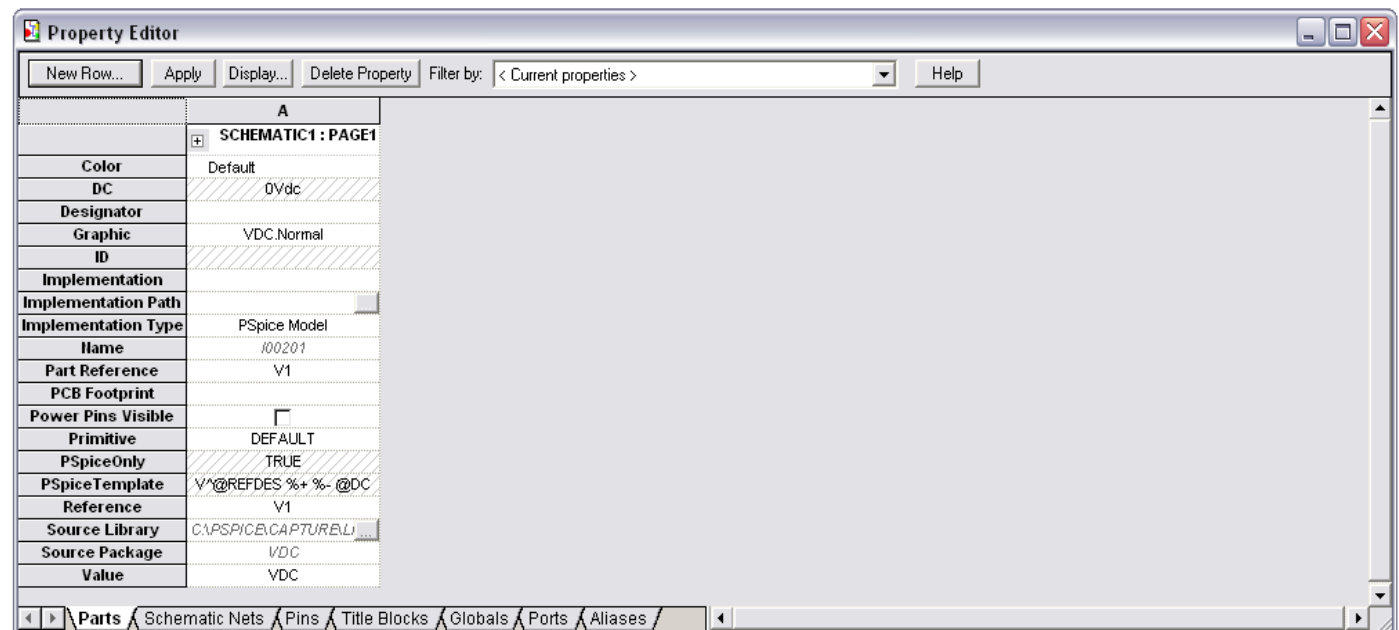
Edit instance properties

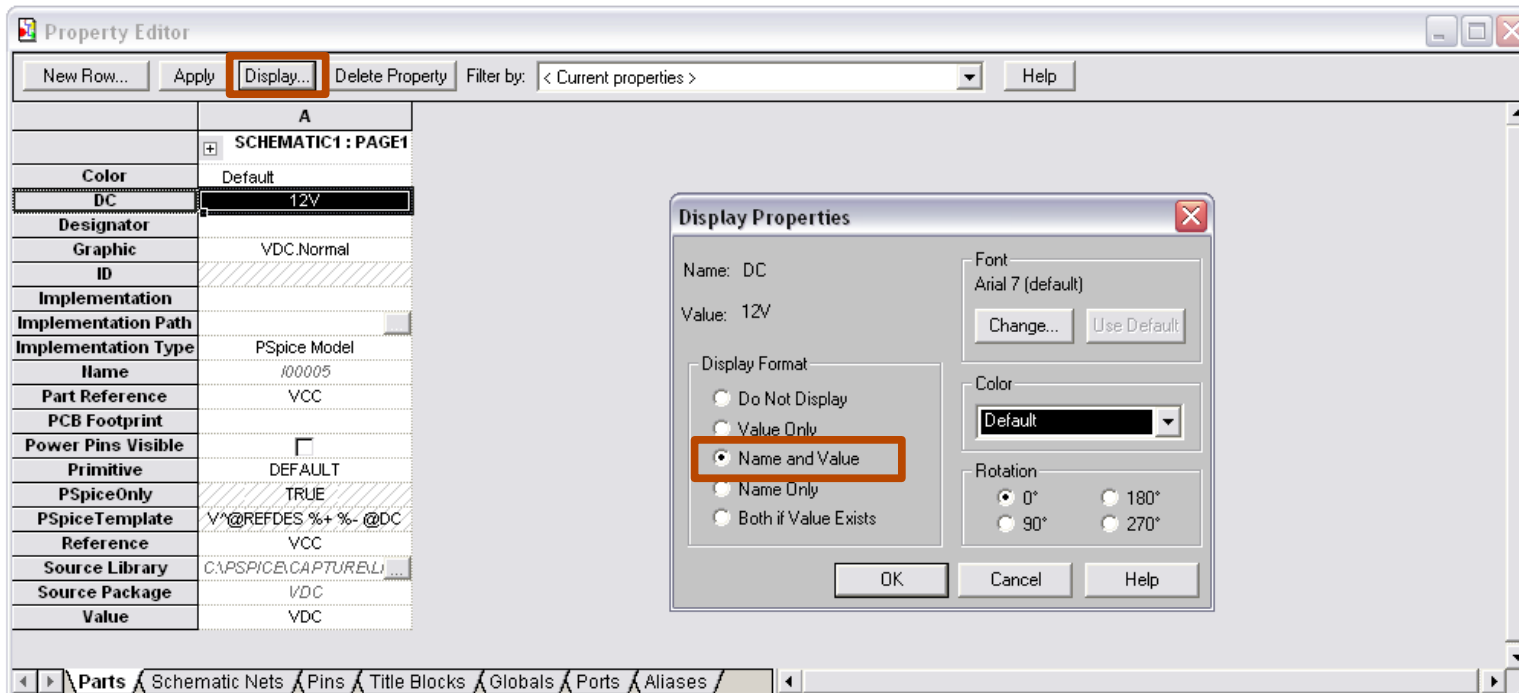
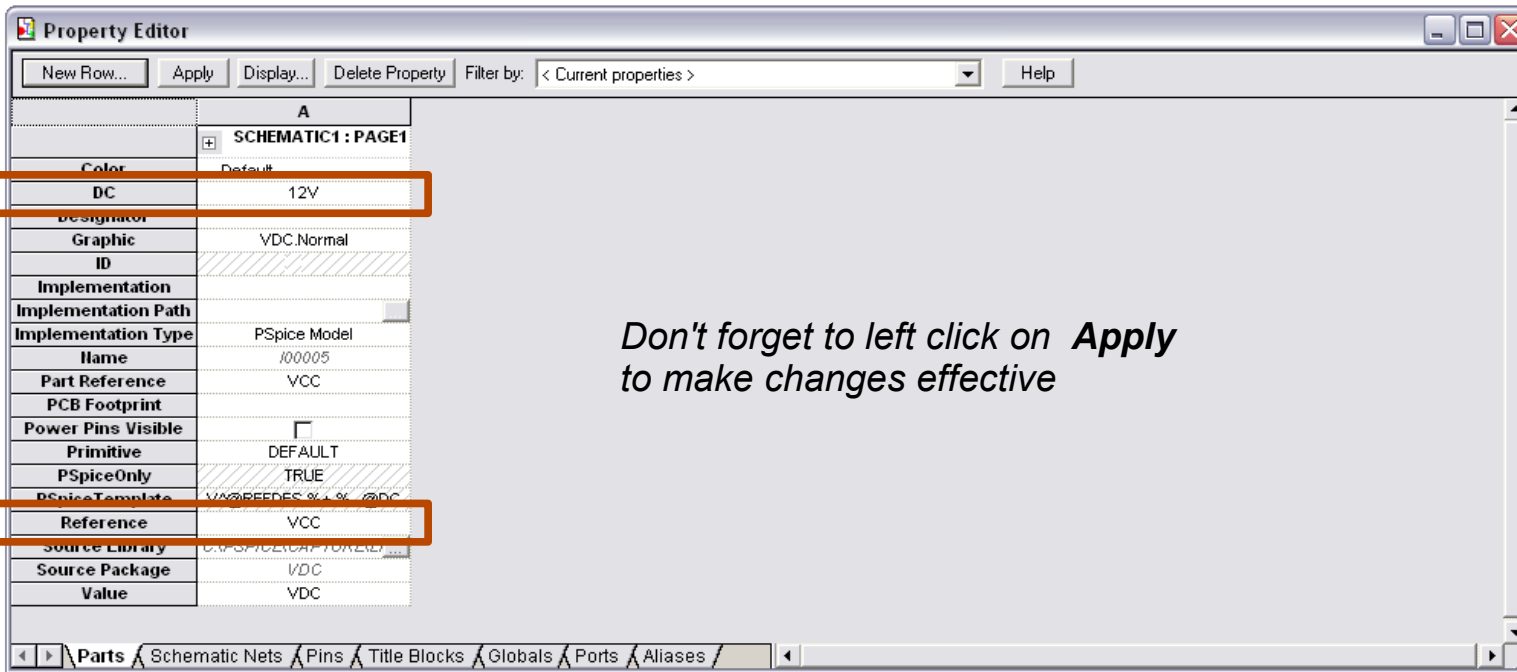


- each component has a set of related **properties** and **parameters**
- a property/parameter has a **name** and a **value**
- some properties names/values are displayed in the schematic, some others by default are shadowed
- left click to select a component, then **right click** → **Edit Properties...**



For a better visualization choose the **Pivot** view (right click on the top-left square in the table)





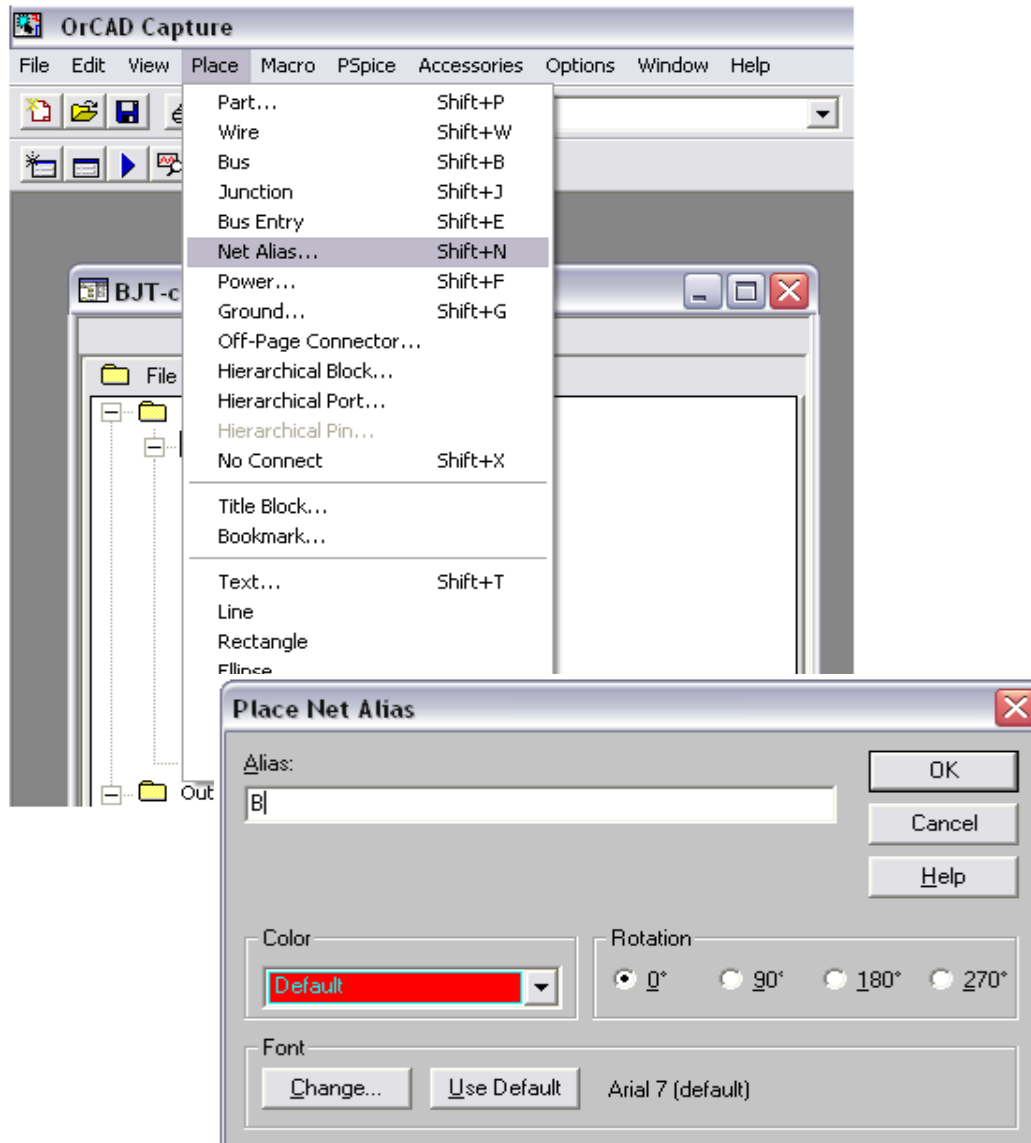
SPICE SI units and prefixes

name	SI	SPICE	C/C++ style
tera	T	T, t	1e12, 1E12
giga	G	G, g	1e9, 1E9
mega	M	MEG, meg	1e6, 1E6
kilo	k	K, k	1e3, 1E3
milli	m	M, m	1e-3, 1E-3
micro	μ	U, u	1e-6, 1E-6
nano	n	N, n	1e-9, 1E-9
pico	p	P, p	1e-12, 1E-12
femto	f	F, f	1e-15, 1E-15

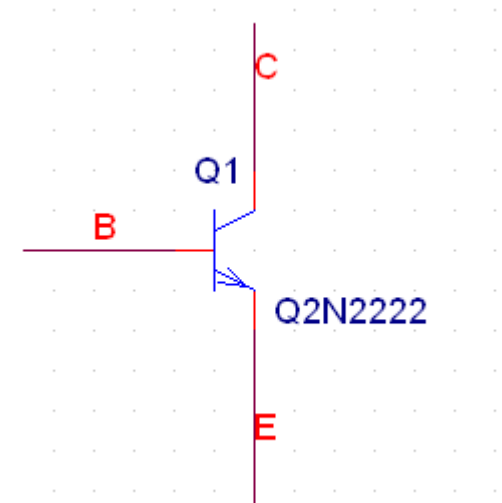
- SPICE is ***not case-sensitive***, upper case and lower case letters are equivalent
- be careful not to use M for mega! 15Mohm are 15 milliohm for SPICE
- ***the unit name can be neglected***, hence 10 and 10V are equivalent for SPICE
- numerical values and prefixes must be typed without spaces, e.g. ***10uF, 10u, 10e-6, 10E-6f***

Naming nets

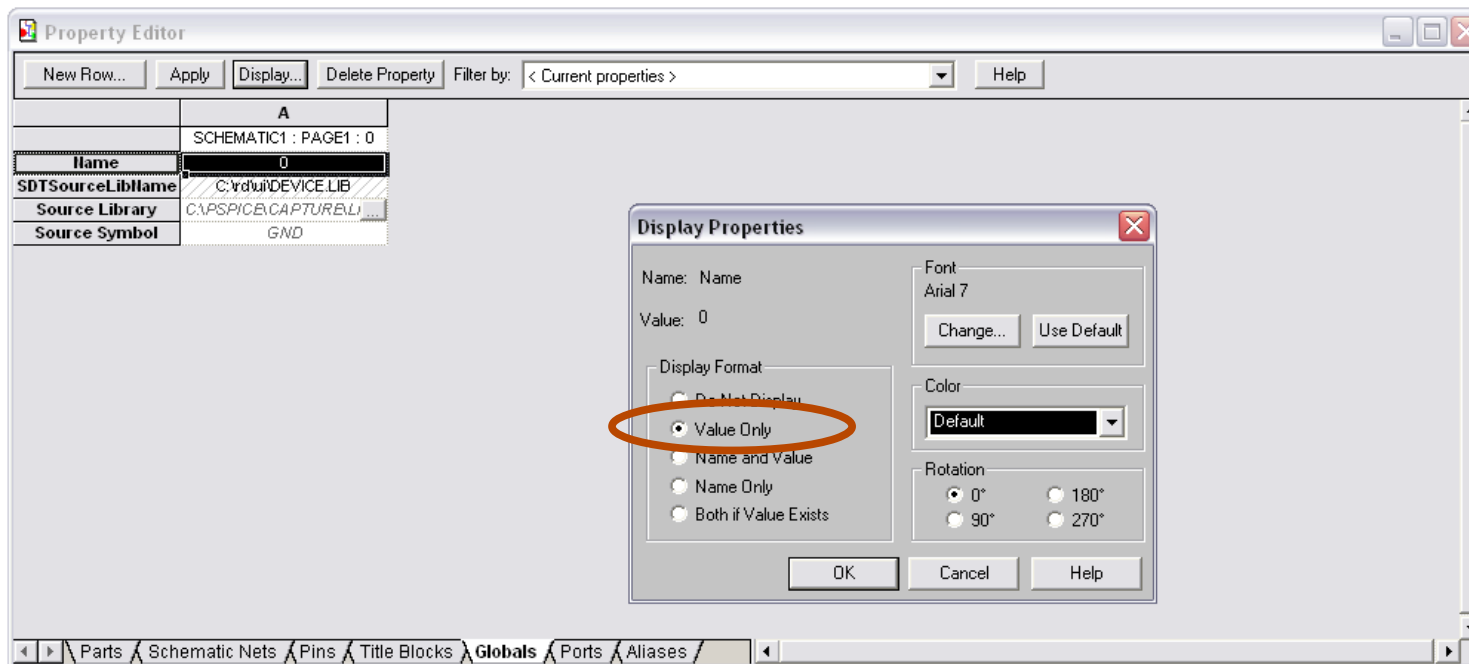
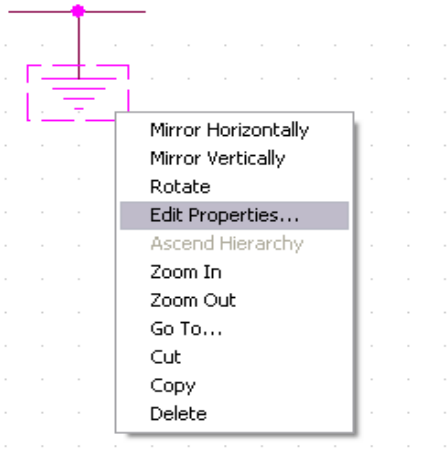
Place → Net Alias...



Give a name (*net alias*) to most significant nodes of the circuit !

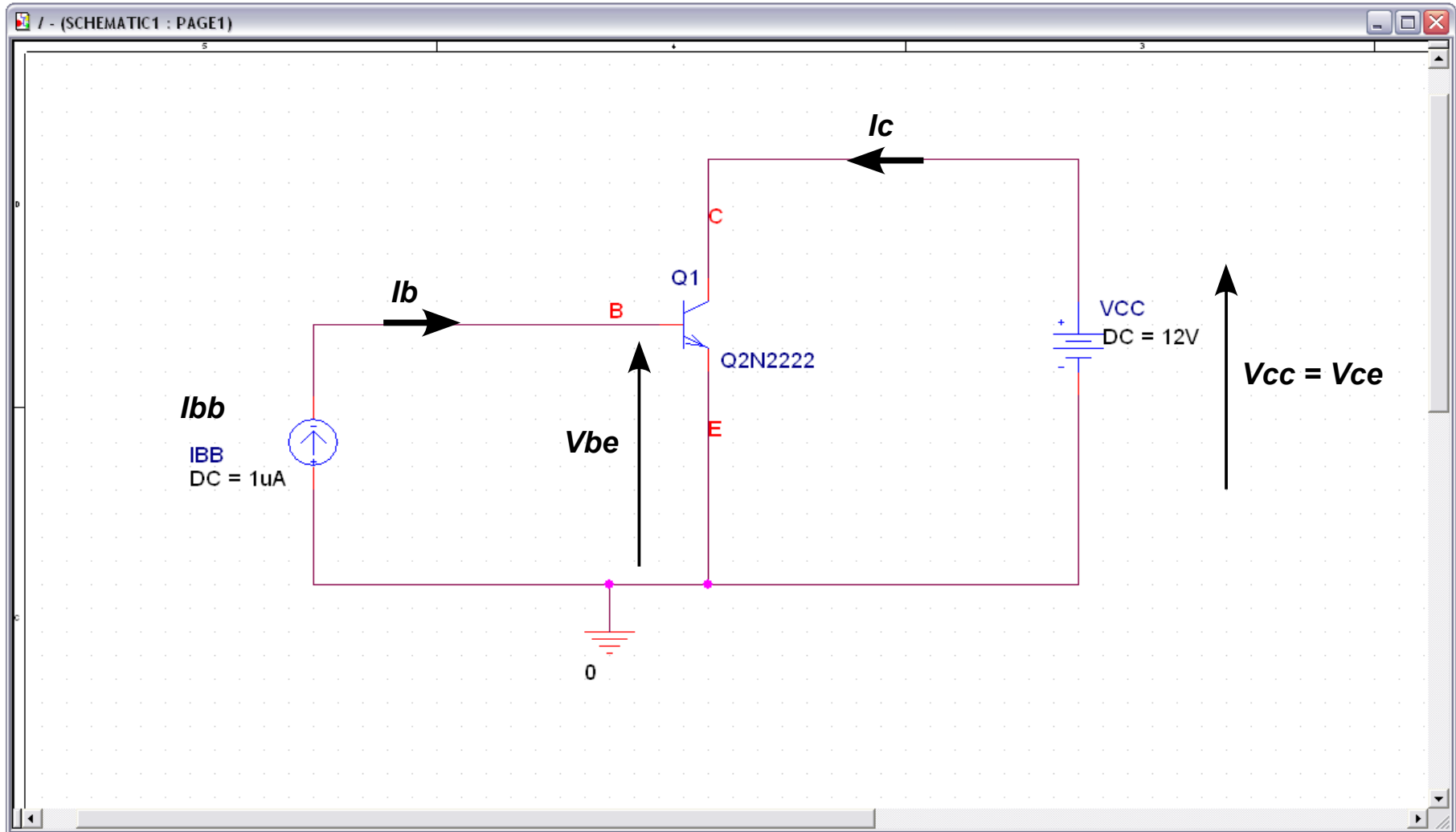


Back to the ground...



Just to remind us that the emitter is tied to zero...

Complete schematic



Useful shortcuts

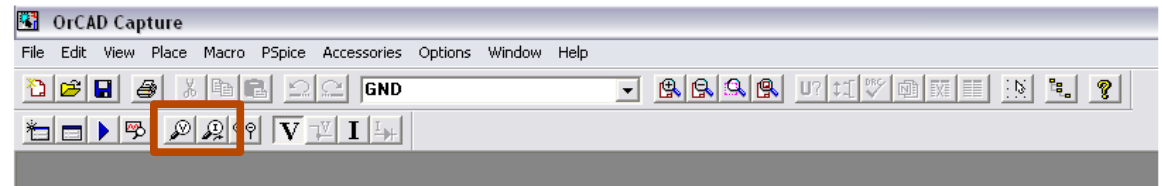
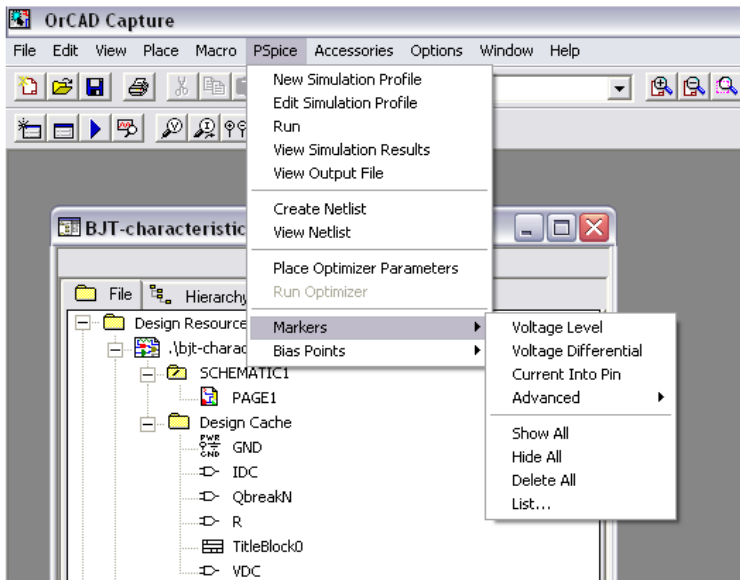
Capture shortcut	description
P	place part
Ctrl + A	add library
G	place ground
F	place power
Ctrl + E	edit component properties
W	place wire
N	place net alias
J	place junction
ESC	end mode
R	rotate component
H / V	mirror horizontally/vertically
T	place text
I / O	zoom in/out
Ctrl + X / Ctrl + V	cut/paste
DEL, CANC	delete component

Part II
Simulations ! (and more theory...)

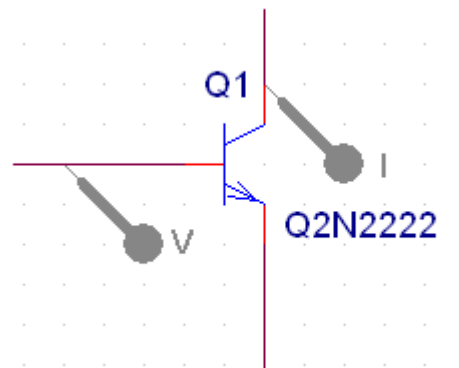


Voltage and current markers

PSpice → Markers → Voltage Level / Current Into Pin

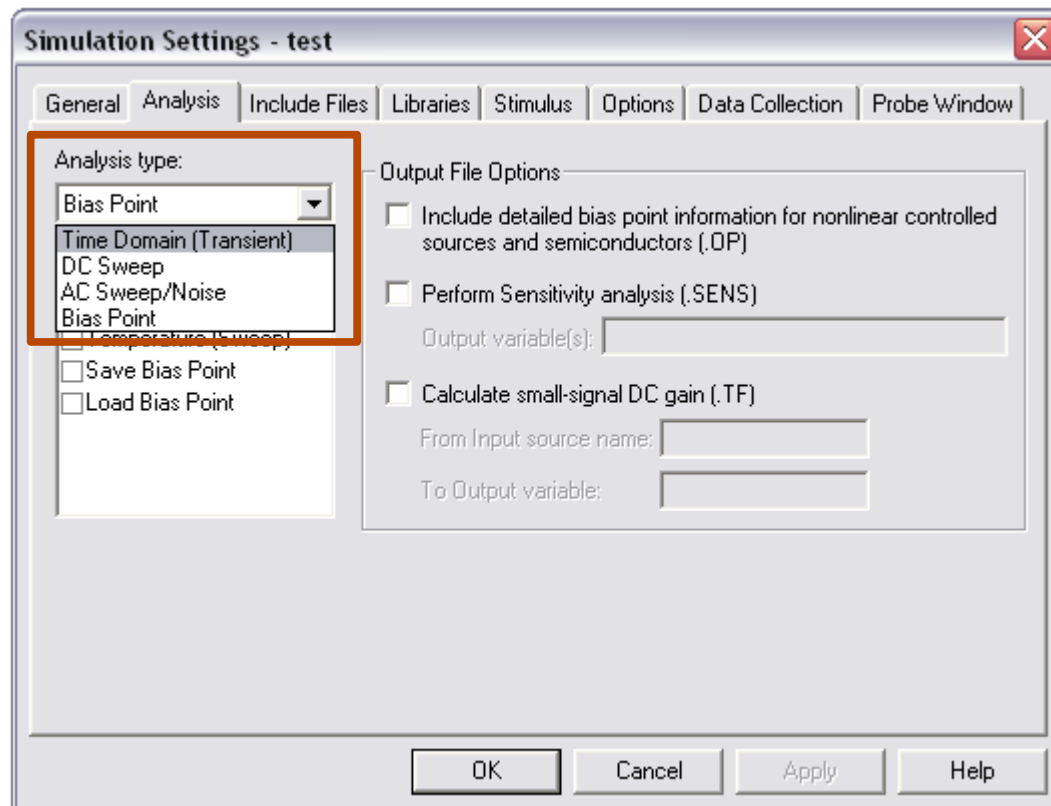
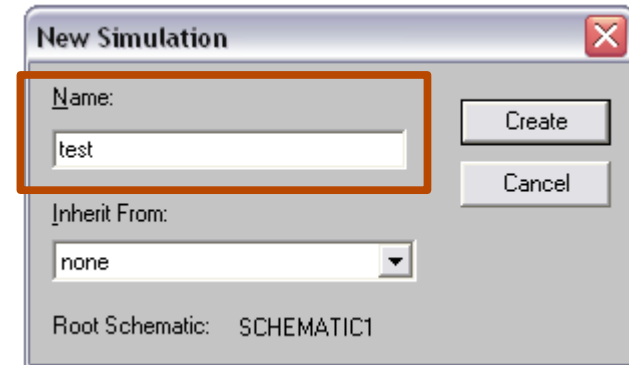
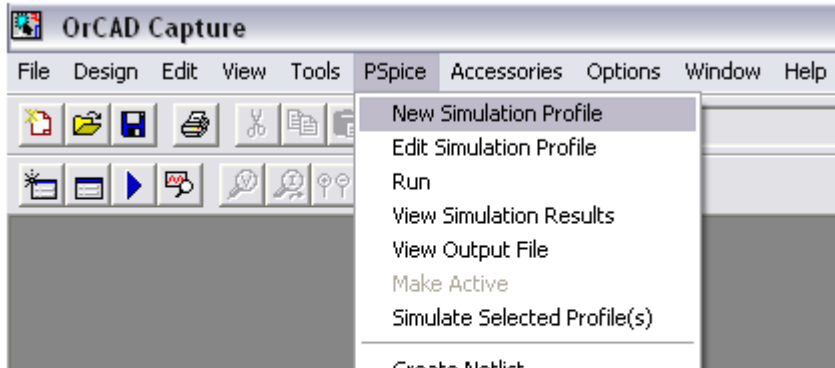


- put **voltage markers** on **wires**
- put **current markers** on **pins**



Simulation profiles

PSpice → New Simulation Profile



- ***transient analysis***
- ***DC sweeps***
- ***frequency (AC) analysis***
- ***bias point***

Bias point

- ***large signal*** DC solution for a particular input voltage/current condition

- ***the time is removed from the circuit***
 - sources with time specifications are set to zero
 - all capacitors are considered open circuits, all inductors shorts
 - DC analysis is a particular case of transient analysis ($dv/dt = 0, di/dt = 0$)

- automatically computed in any other simulation

- simulation results are printed in the text output file and can be visualized in the schematic using ***bias point markers***
 - list of all ***node voltages, currents*** and total ***power dissipation***
 - detailed bias point information for ***semiconductor devices*** (not included by default)

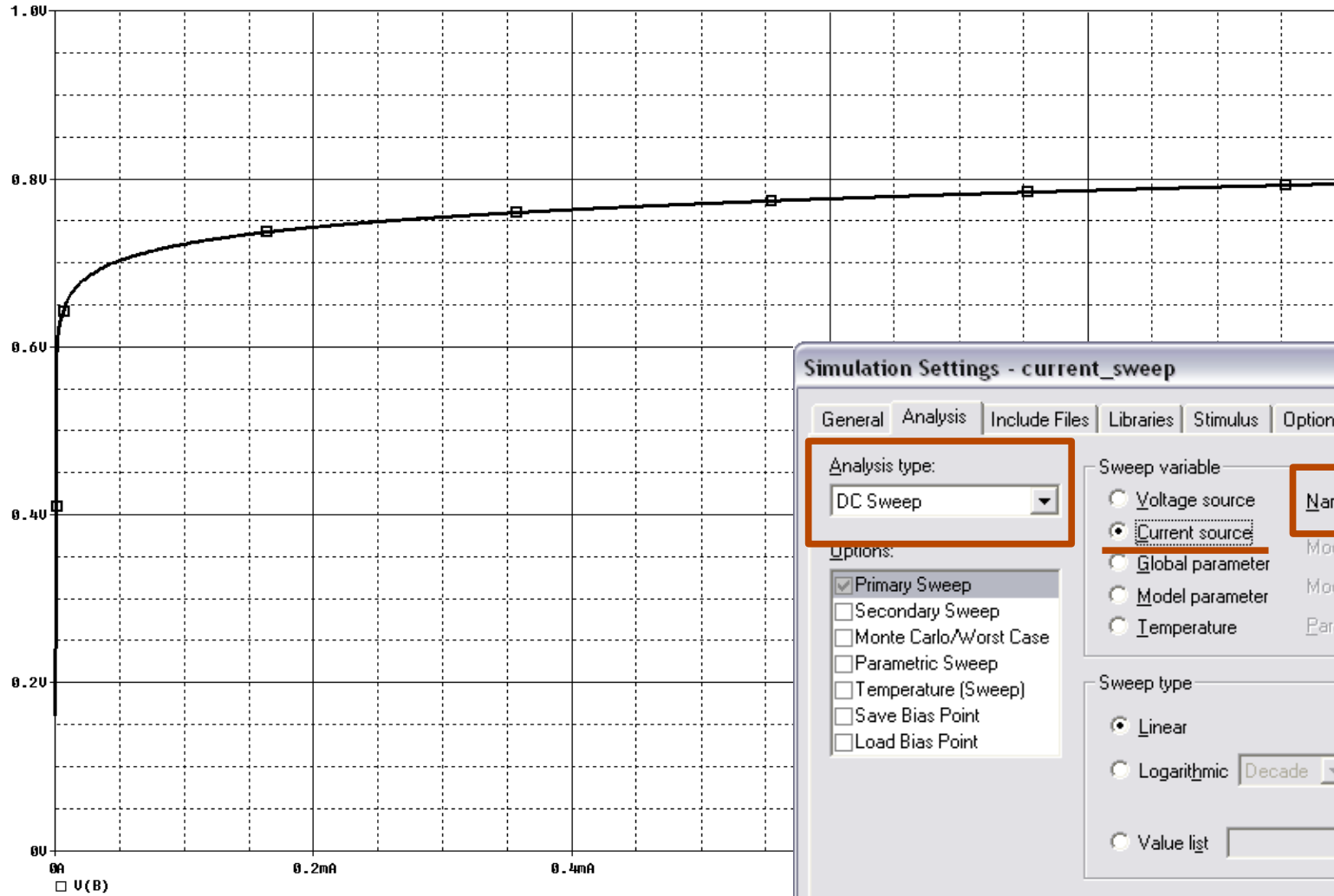
DC sweep

- **large signal steady-state circuit DC response** when sweeping a voltage/current source, a global parameter, a model parameter or the temperature **over a range of values**

- the **bias point** is calculated for each value of the sweep

- **nested DC sweep analysis** can be performed
 - a secondary sweep variable can be selected after a primary sweep value has been specified
 - **curve families** are obtained

V_{be} vs I_{bb} ($V_{ce} = \text{const}$)



The image shows the 'Simulation Settings - current_sweep' dialog box. The 'Analysis type' is set to 'DC Sweep'. The 'Sweep variable' is 'Current source', with the 'Name' field set to 'IBB'. The 'Sweep type' is 'Linear', with 'Start value' set to 0, 'End value' set to 1m, and 'Increment' set to 10u. The 'Options' section is also visible, with 'Primary Sweep' checked.

Simulation Settings - current_sweep

General Analysis Include Files Libraries Stimulus Options Data Collection Probe Window

Analysis type: DC Sweep

Options:

- Primary Sweep
- Secondary Sweep
- Monte Carlo/Worst Case
- Parametric Sweep
- Temperature (Sweep)
- Save Bias Point
- Load Bias Point

Sweep variable:

- Voltage source
- Current source
- Global parameter
- Model parameter
- Temperature

Name: IBB

Model type: [dropdown]

Model name: [text]

Parameter name: [text]

Sweep type:

- Linear
- Logarithmic: Decade [dropdown]
- Value list [text]

Start value: 0

End value: 1m

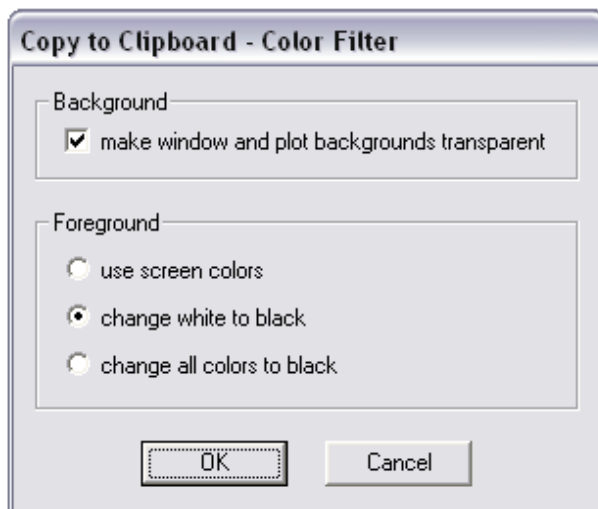
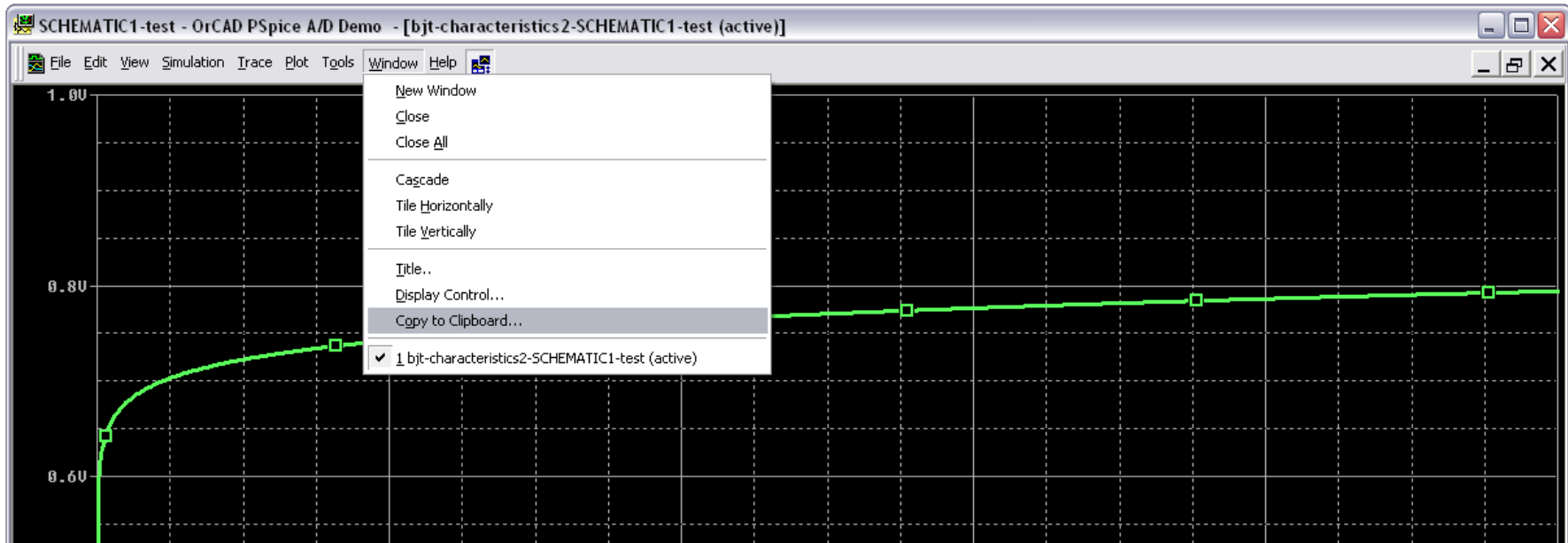
Increment: 10u

OK Cancel Apply Help

Is it in agreement with our expectations ?

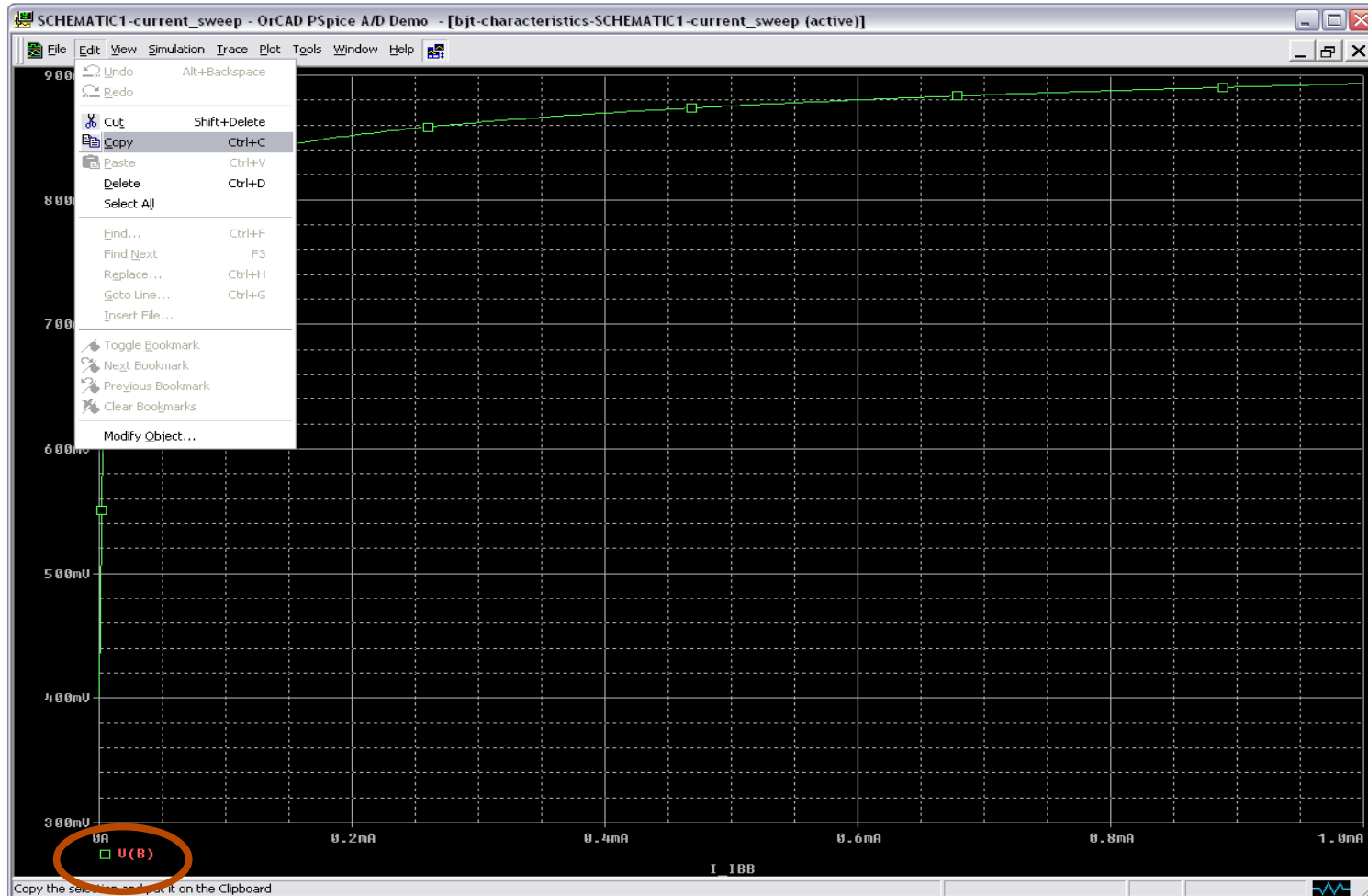
Export the plot image

Window → **Copy to Clipboard...**

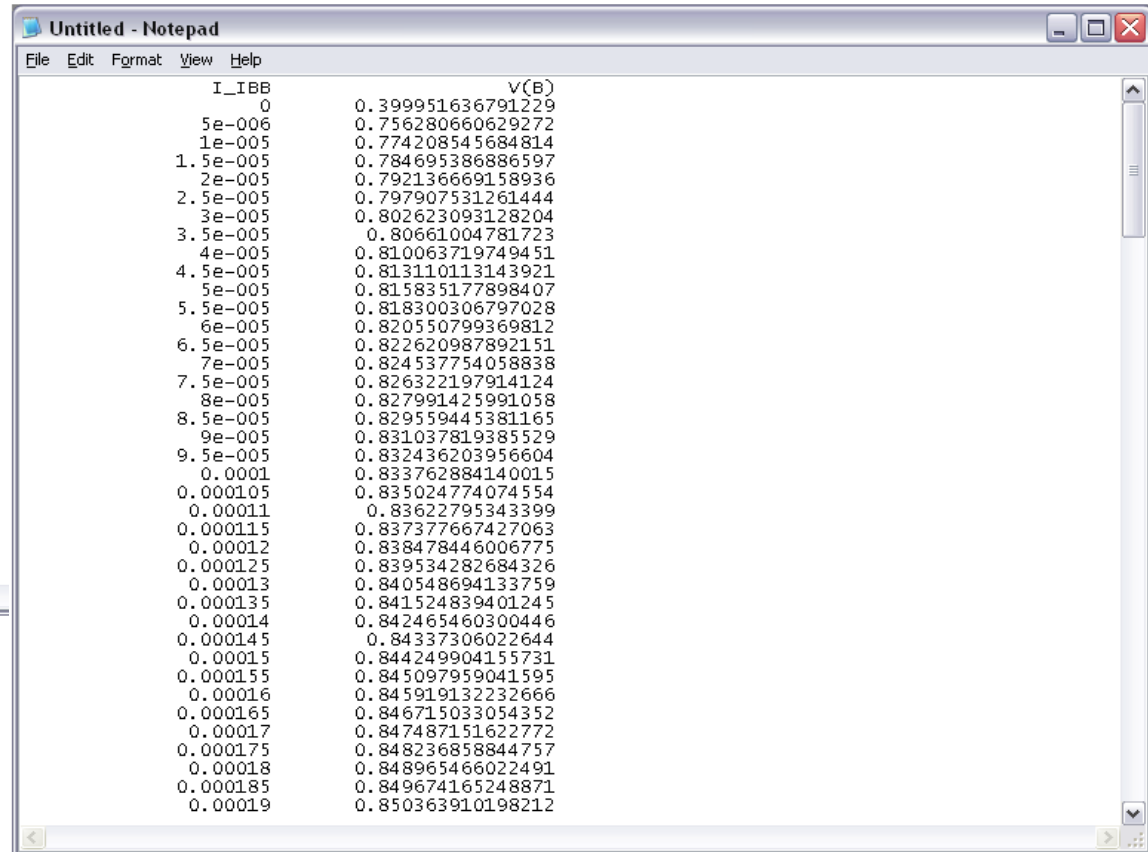
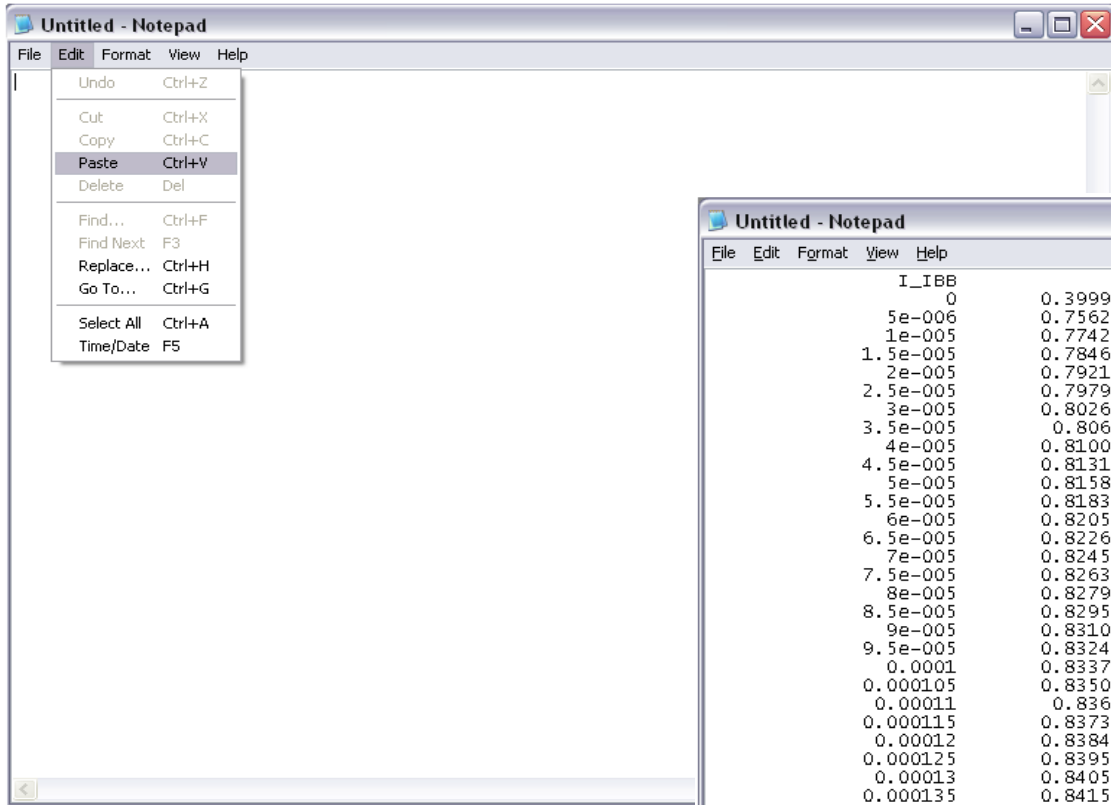


*Choose the color scheme, then open your favorite image editor (**Paint** works fine) and simply do a 'paste' inside it*

Export numerical values

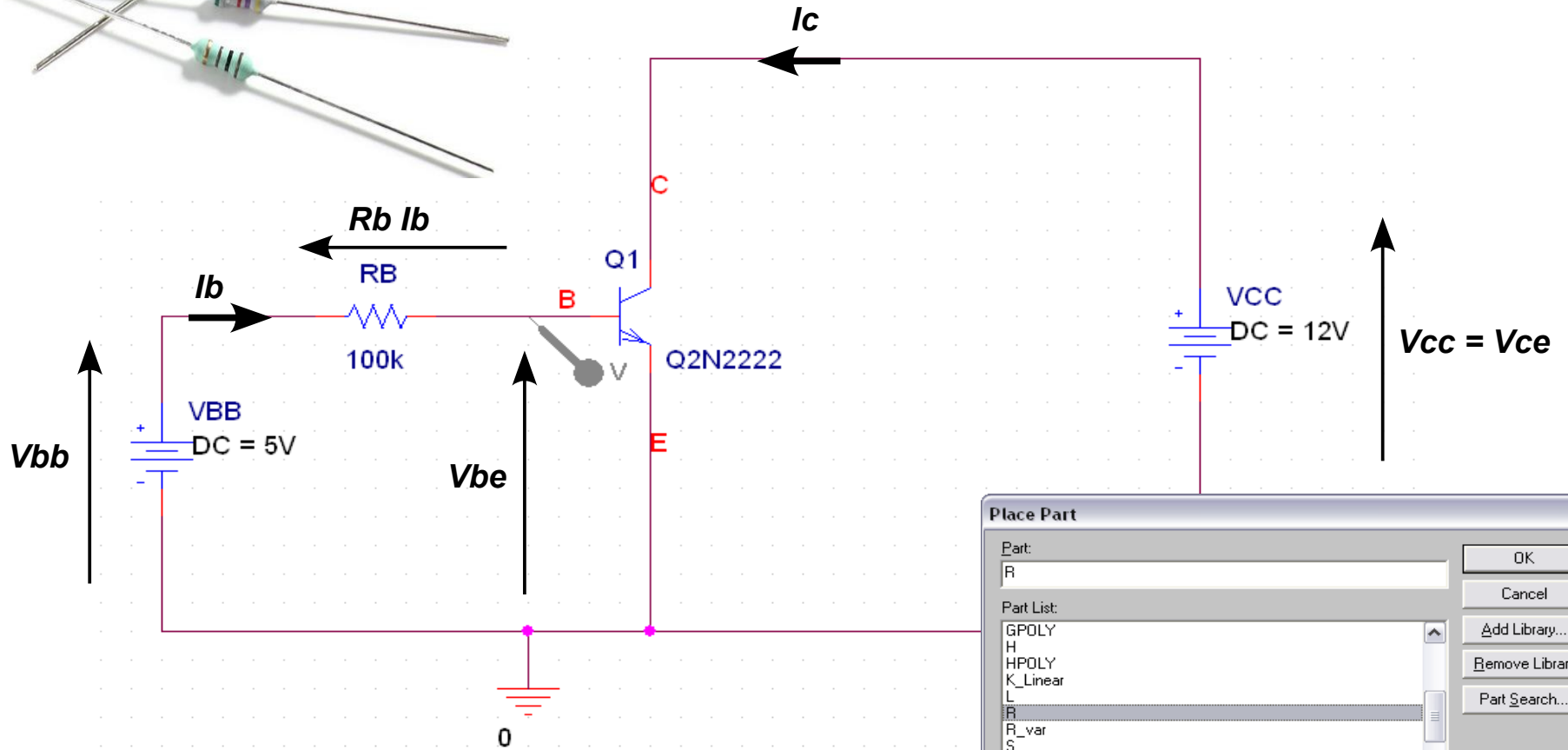
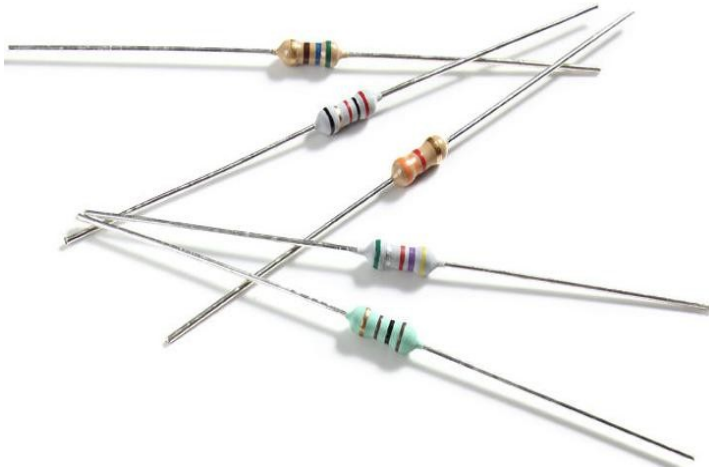


- the waveform can be exported as a set of (x,y) numerical values
- select the waveform name at the bottom-left of the window, then **Edit** → **Copy**



- open a text editor (*Notepad* works fine)
- simply do a 'paste' inside the text editor
- save the file with the *.csv* extension, it can be opened with Excel, Mathematica, ROOT etc.

Welcome to the real world...



This is the circuit you have to deal with in the lab experience #8 !

Place Part

Part: R

Part List:

- GPOLY
- H
- HPOLY
- K_Linear
- L
- R**
- R_var
- S
- T
- TLOSSY

Libraries:

- ABM
- ANALOG
- ANALOG_P
- BREAKOUT
- Design Cache
- EVAL
- SOURCE
- SOURCSTM
- SPECIAL

Graphic:

- Normal
- Convert

Packaging:

Parts per Pkg: 1

Part: [dropdown]

Type: Homogeneous

OK

Cancel

Add Library...

Remove Library

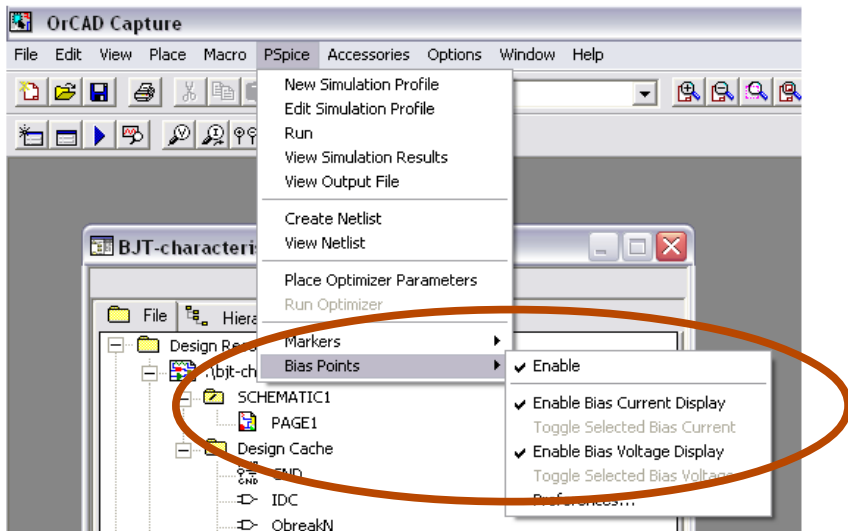
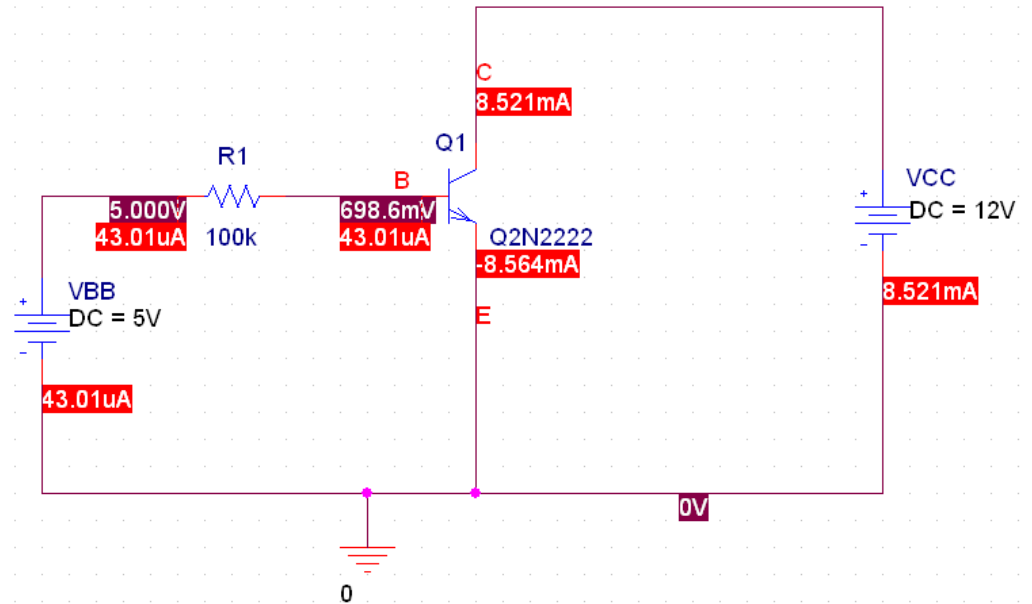
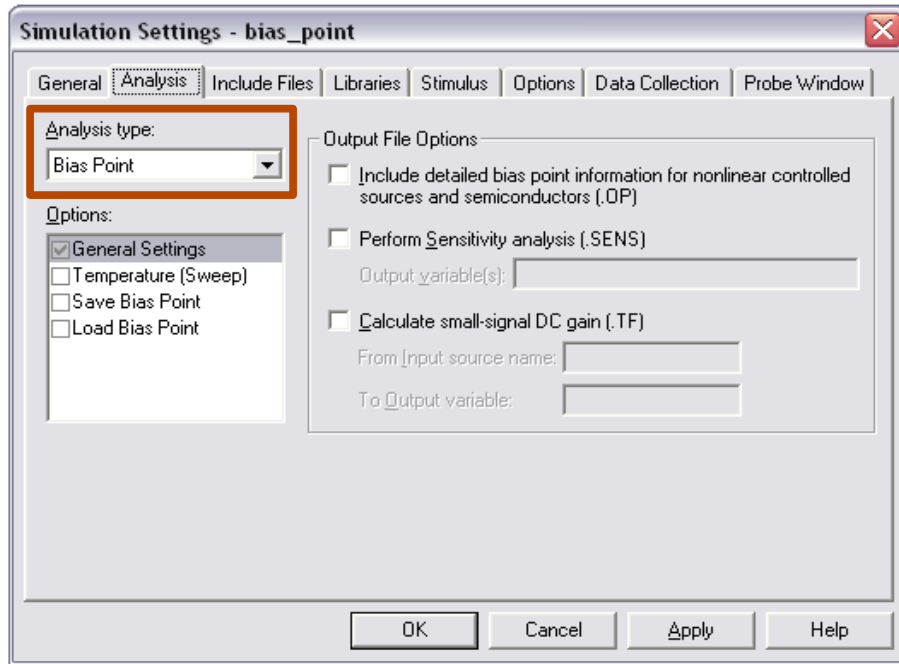
Part Search...

Help

R?

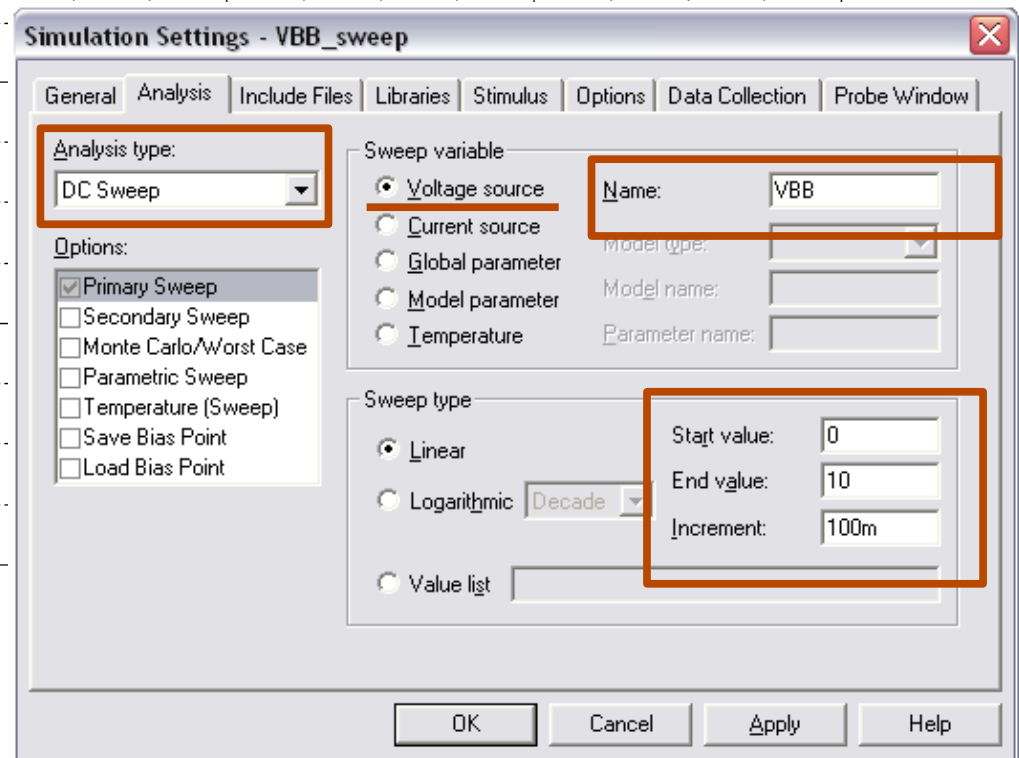
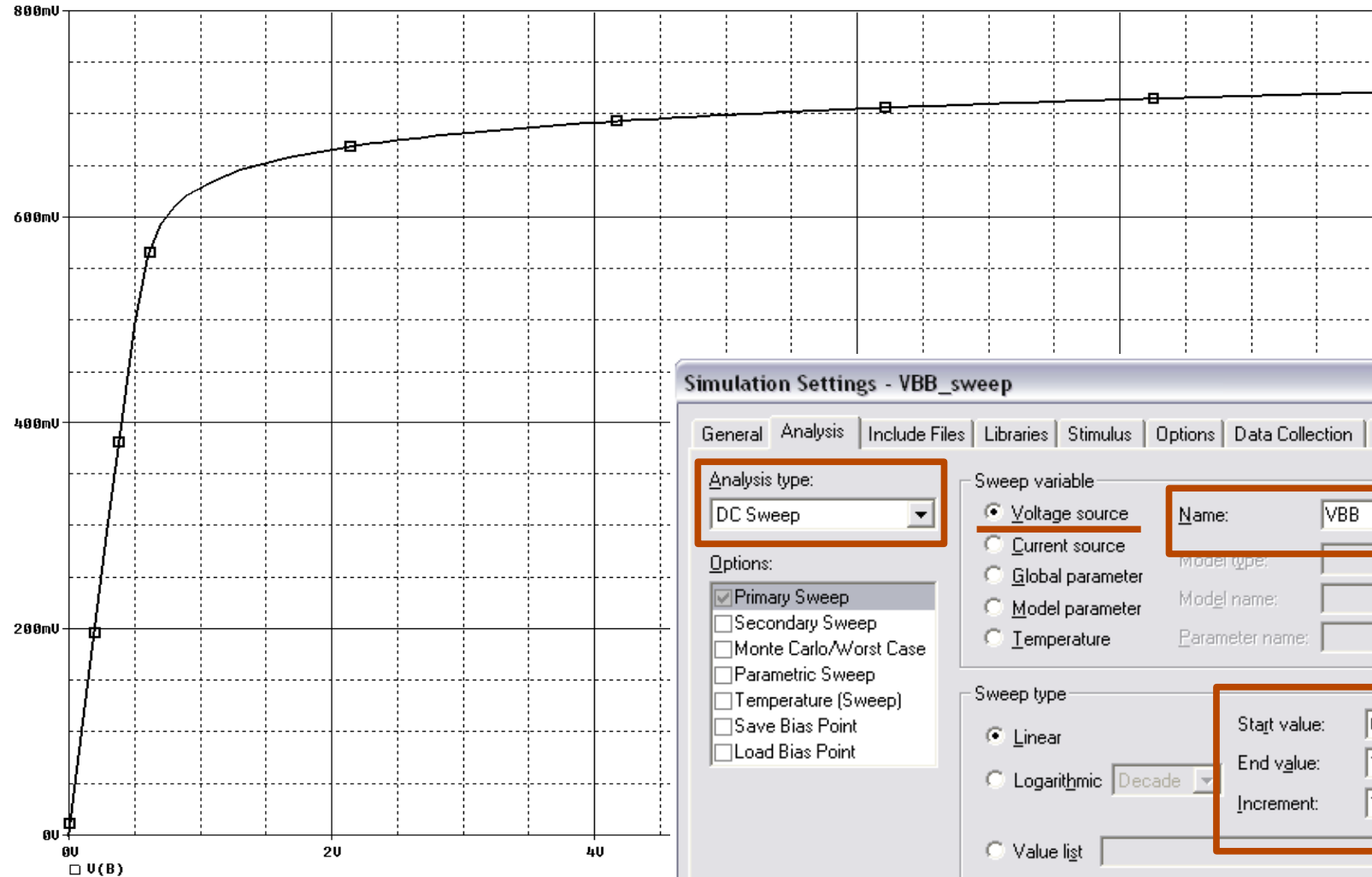
1k

Bias point analysis



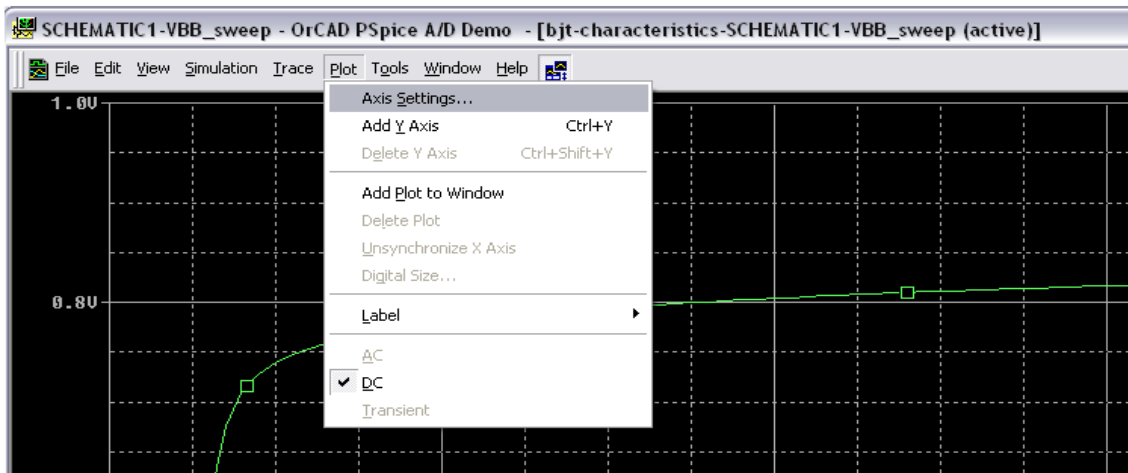
PSpice → Bias Points → Enable Bias Current (Voltage) Display

V_{be} vs V_{bb} ($V_{ce} = \text{const}$)



Vbe vs Ib (Vce = const)

Plot → Axis Settings...



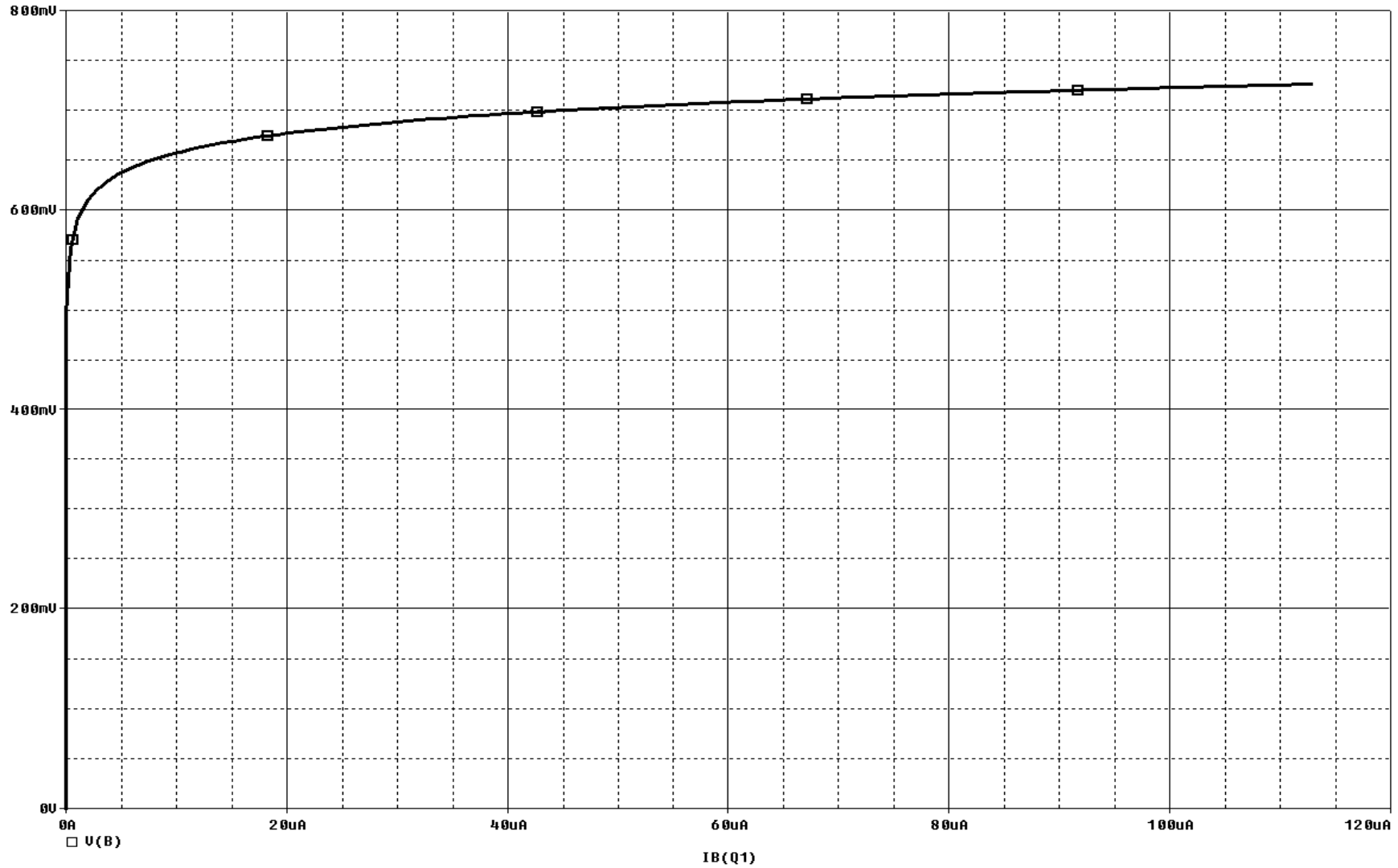
Change the x-axis variable in order to plot Vbe versus the base-current again

The image shows two dialog boxes. The top one is the "Axis Settings" dialog, with the "X Axis" tab selected. The "Data Range" section has "Auto Range" selected. The "Scale" section has "Linear" selected. The "Axis Variable..." button is highlighted with a red box. The bottom dialog is the "X Axis Variable" dialog, showing a list of simulation output variables. The variable "IB(Q1)" is highlighted with a red box. The "Trace Expression" field at the bottom contains "IB(Q1)".

- IB(Q1)
- IC(Q1)
- IE(Q1)

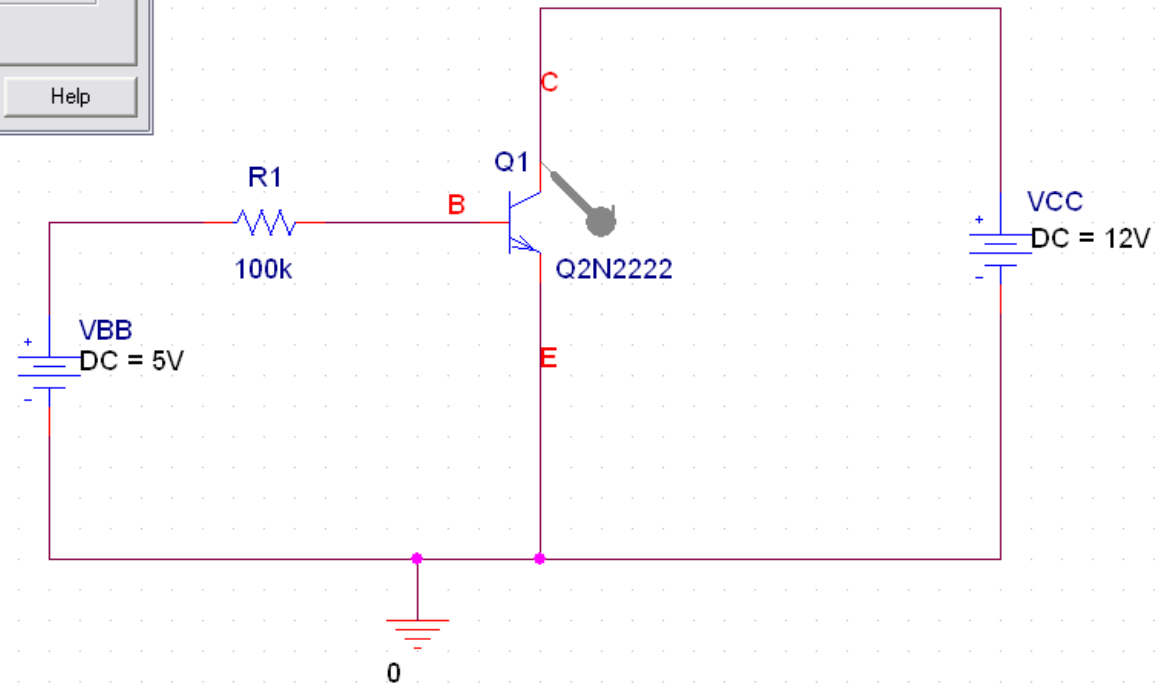
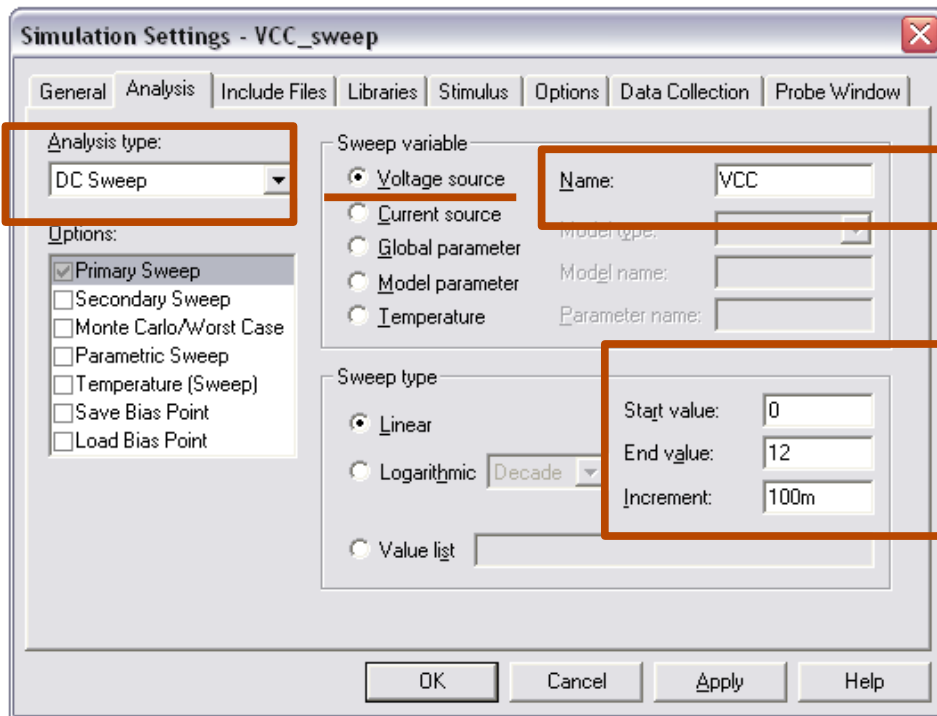
V_{be} vs I_b ($V_{ce} = \text{const}$)

Input characteristic, $V_{be} = f(I_b)$



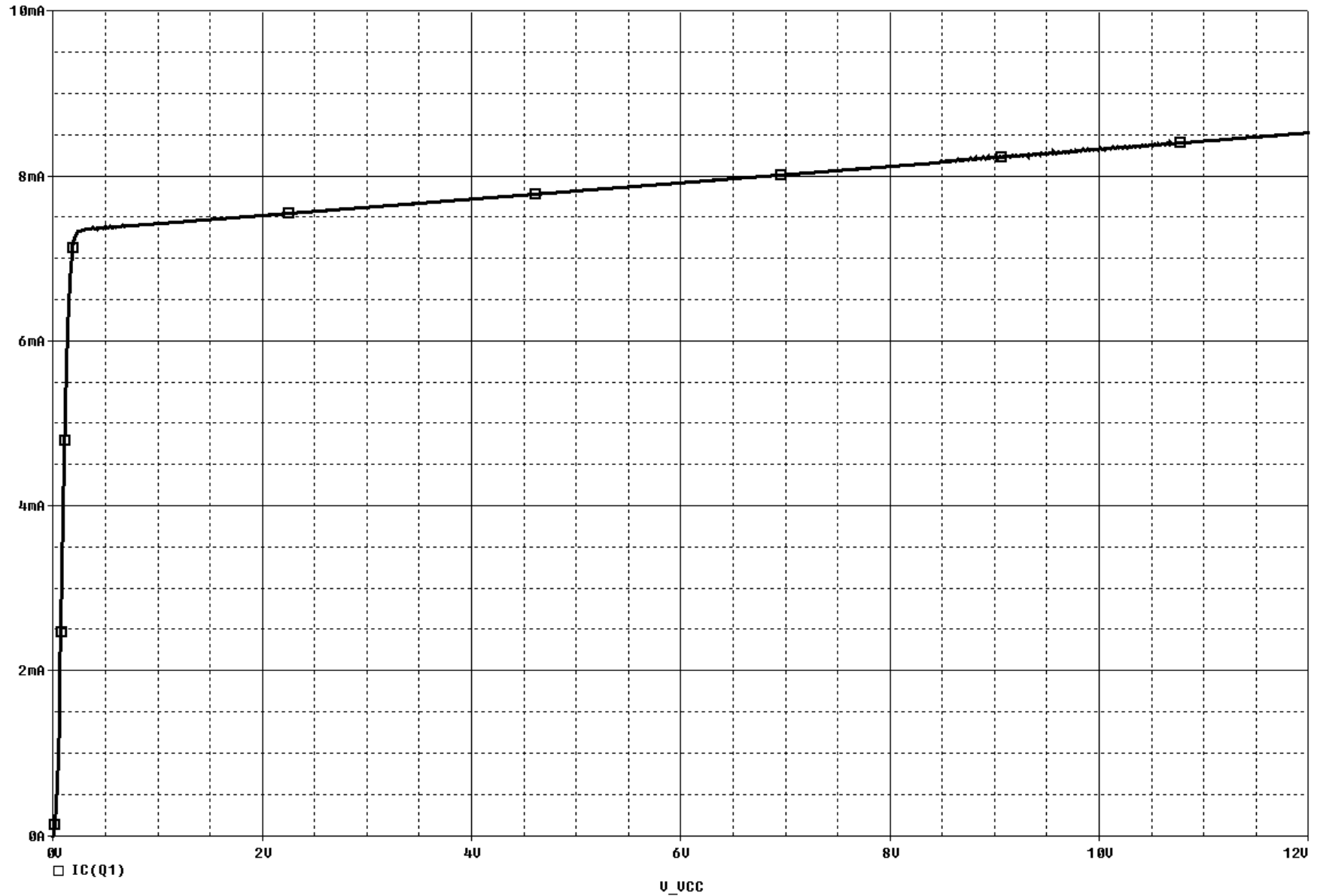
When V_{be} reaches ~ 700 mV the transistor is in full conduction regime !

Ic vs Vce (Vbe = const)

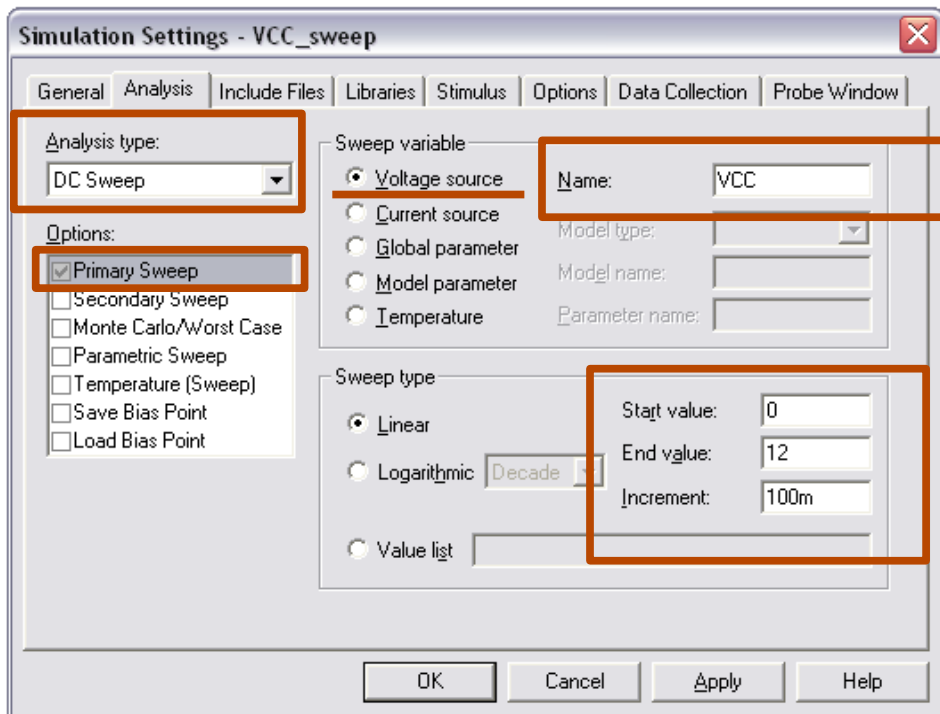


Ic vs Vce (Vbe = const)

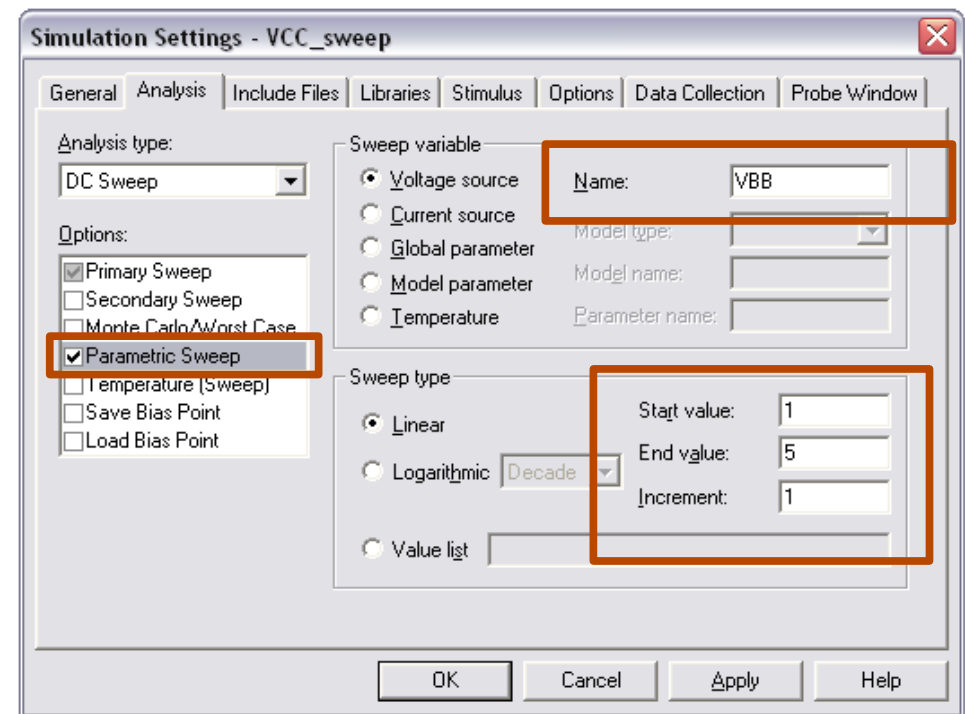
Output characteristic, $I_c = f(V_{ce})$



Nested DC sweeps



Primary sweep by varying V_{cc} for a fixed value of V_{bb} (and therefore of V_{be})

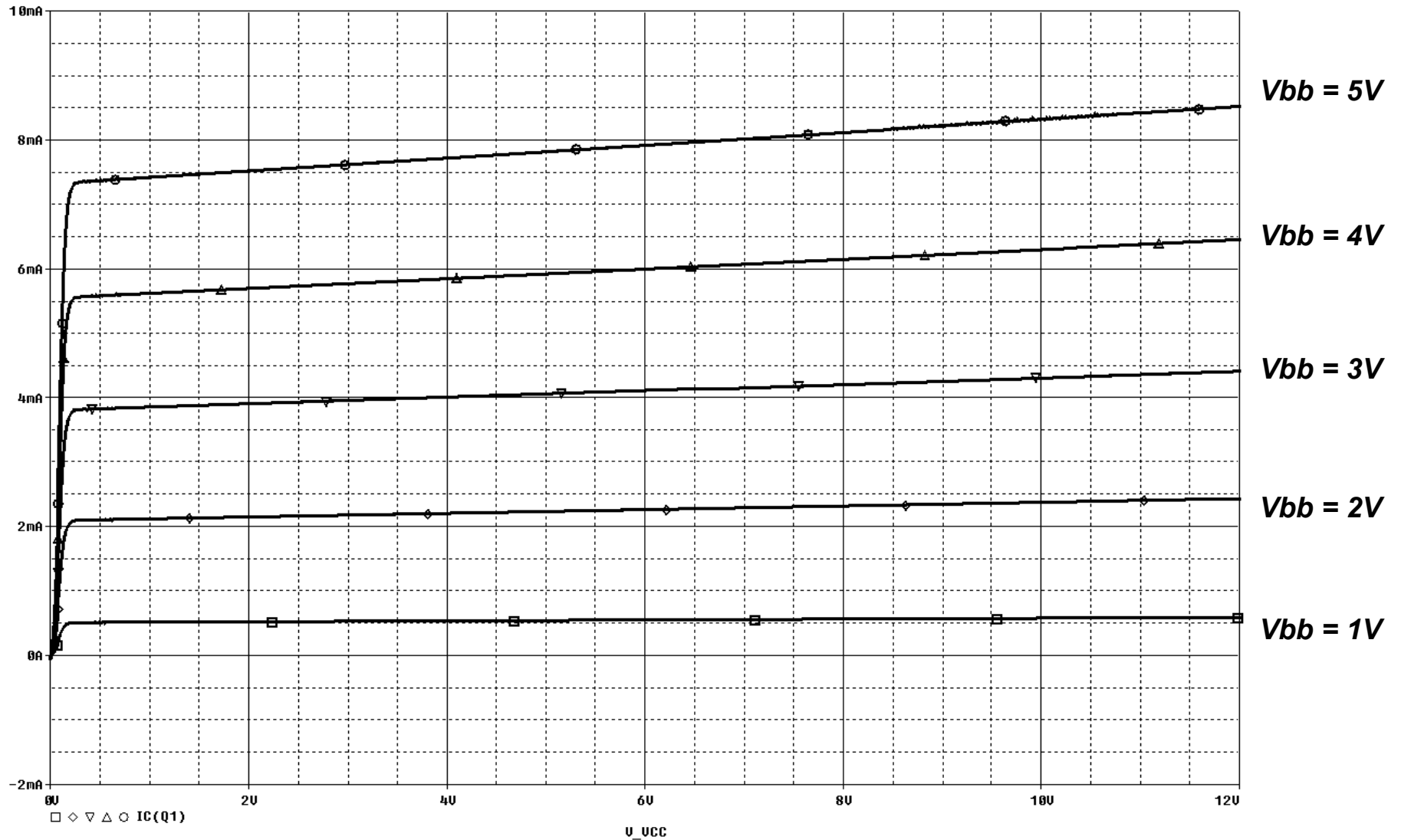


*The primary sweep **is repeated** for different values of V_{bb} (and therefore of V_{be})*

N.B.

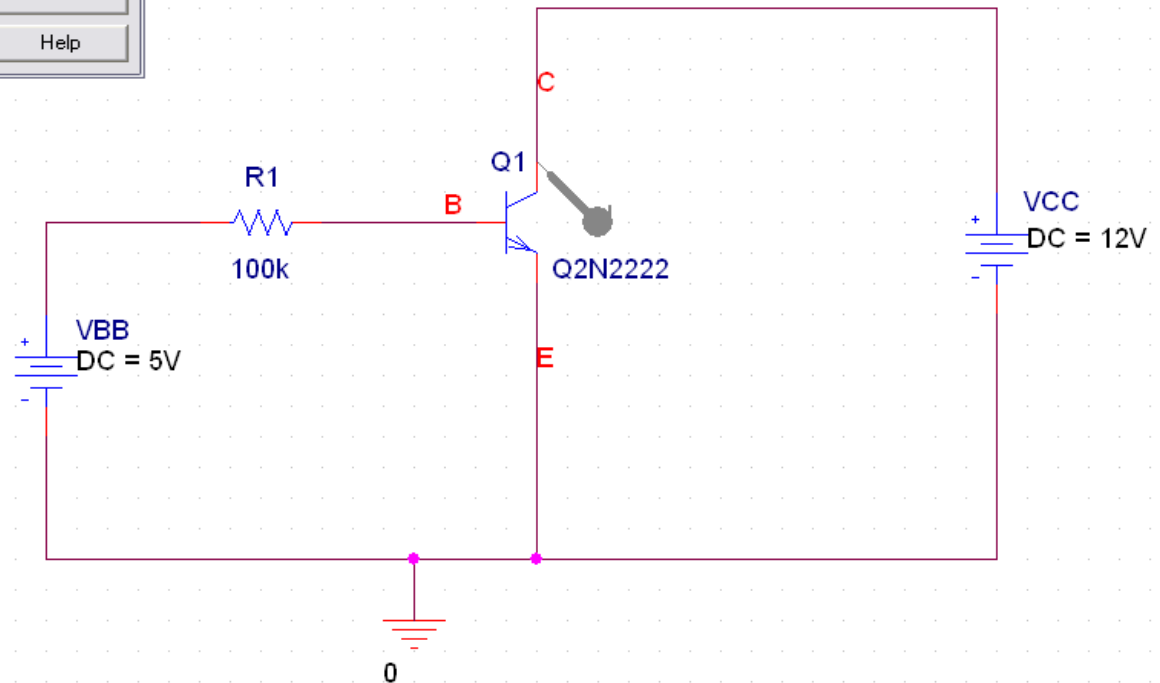
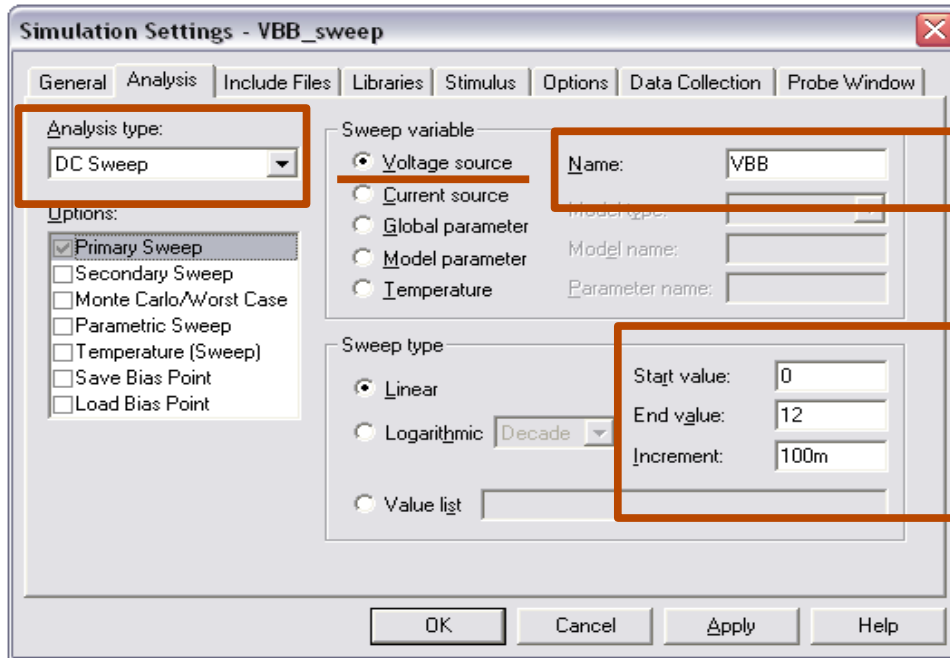
The simulation profile is just one, don't create two different profiles !

Ic vs Vce for different Vbb

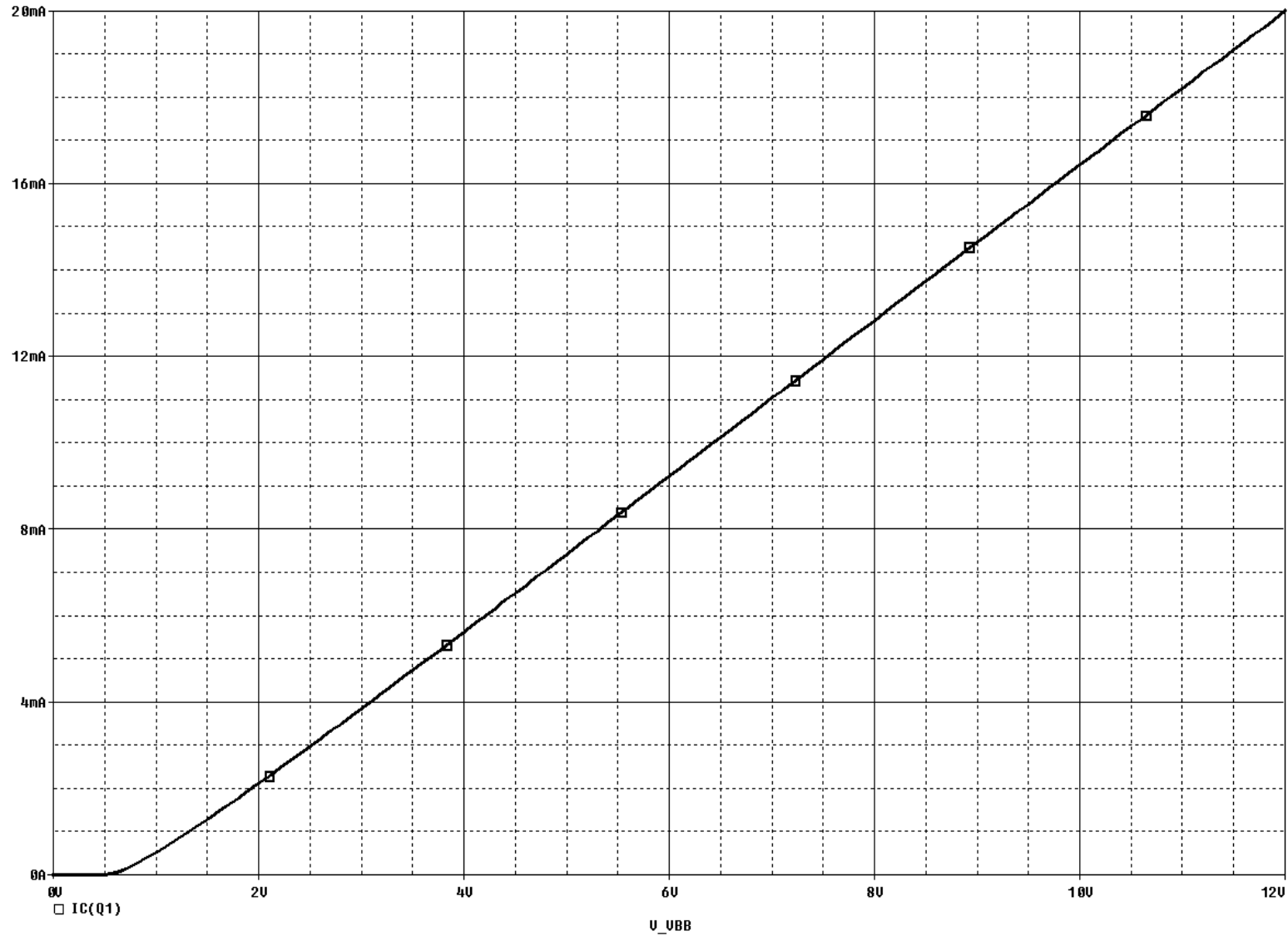


What's happening?

I_c vs V_{bb} ($V_{ce} = \text{const}$)

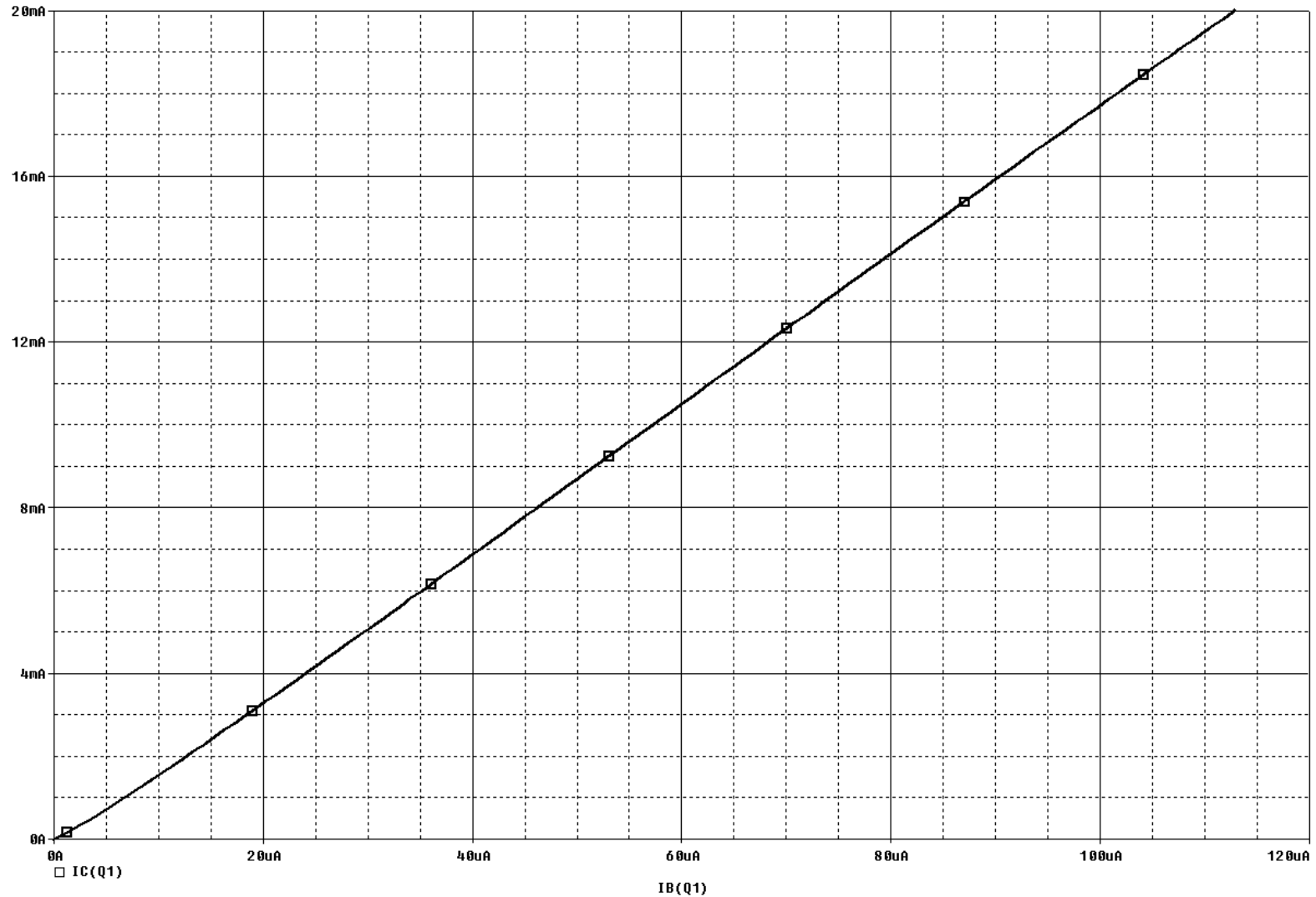


Ic vs Vbb (Vce = const)



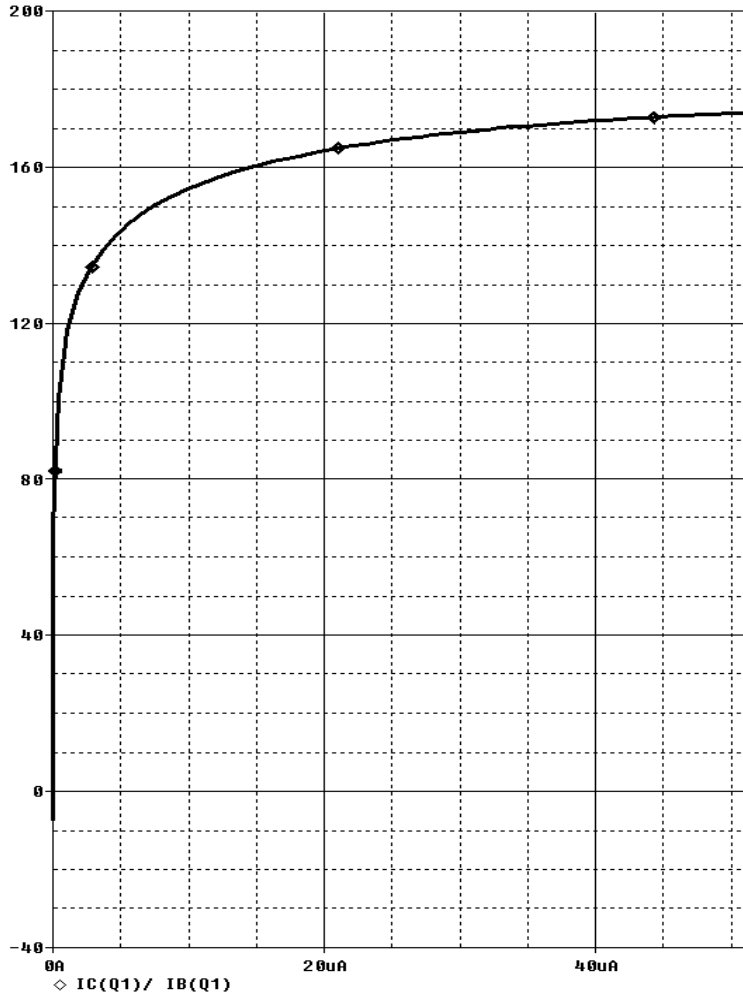
Ic vs Ib (Vce = const)

Change the x-axis variable....



The relationship between I_c and I_b is linear !

$h_{FE} = I_c/I_b$ vs I_b ($V_{ce} = \text{const}$)



Philips Semiconductors

Product specification

NPN switching transistors

2N2222; 2N2222A

FEATURES

- ∞ High current (max. 800 mA)
- ∞ Low voltage (max. 40 V).

APPLICATIONS

- ∞ Linear amplification and switching.

DESCRIPTION

NPN switching transistor in a TO-18 metal package.
PNP complement: 2N2907A.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector, connected to case

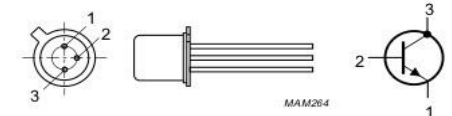
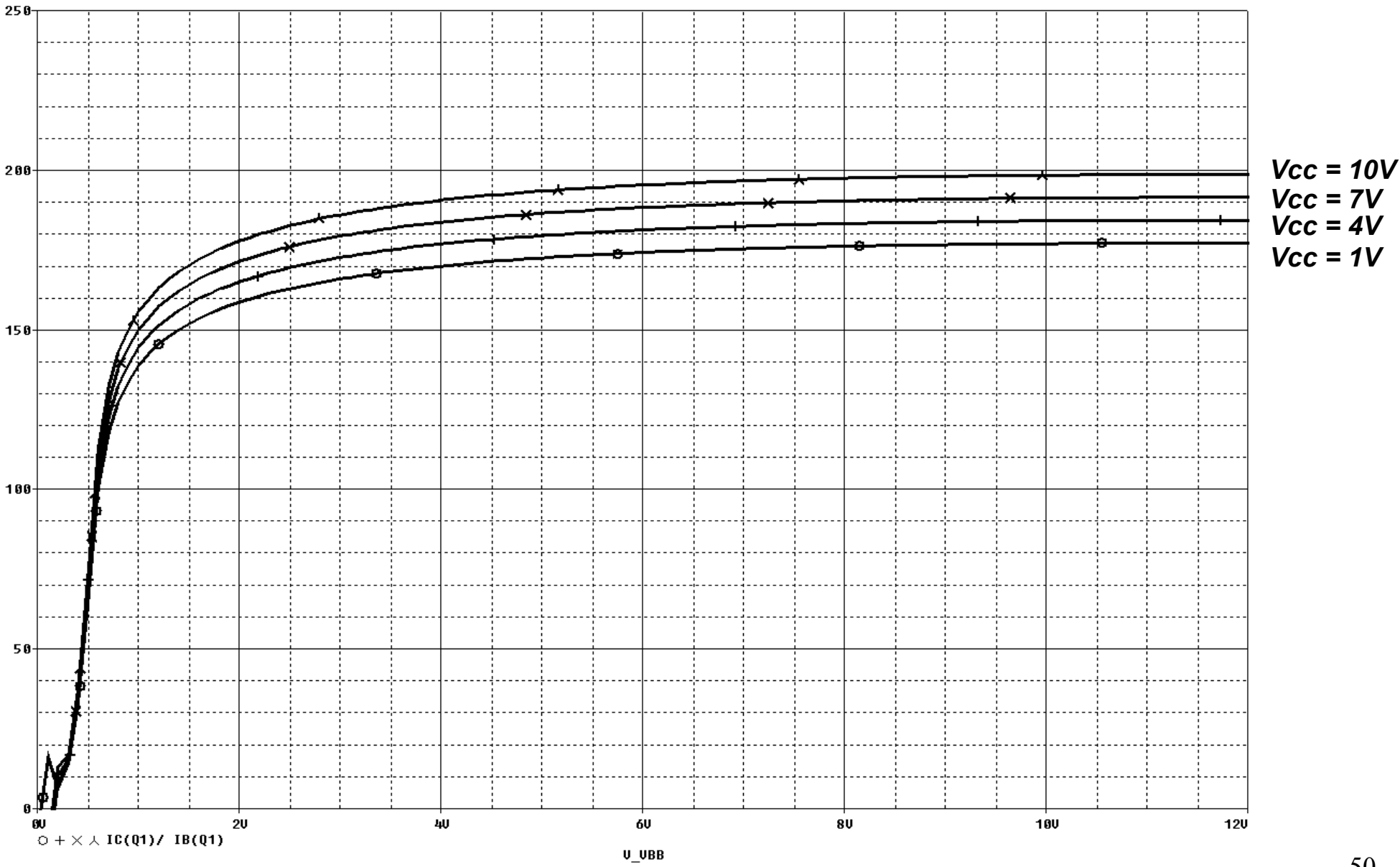


Fig.1 Simplified outline (TO-18) and symbol.

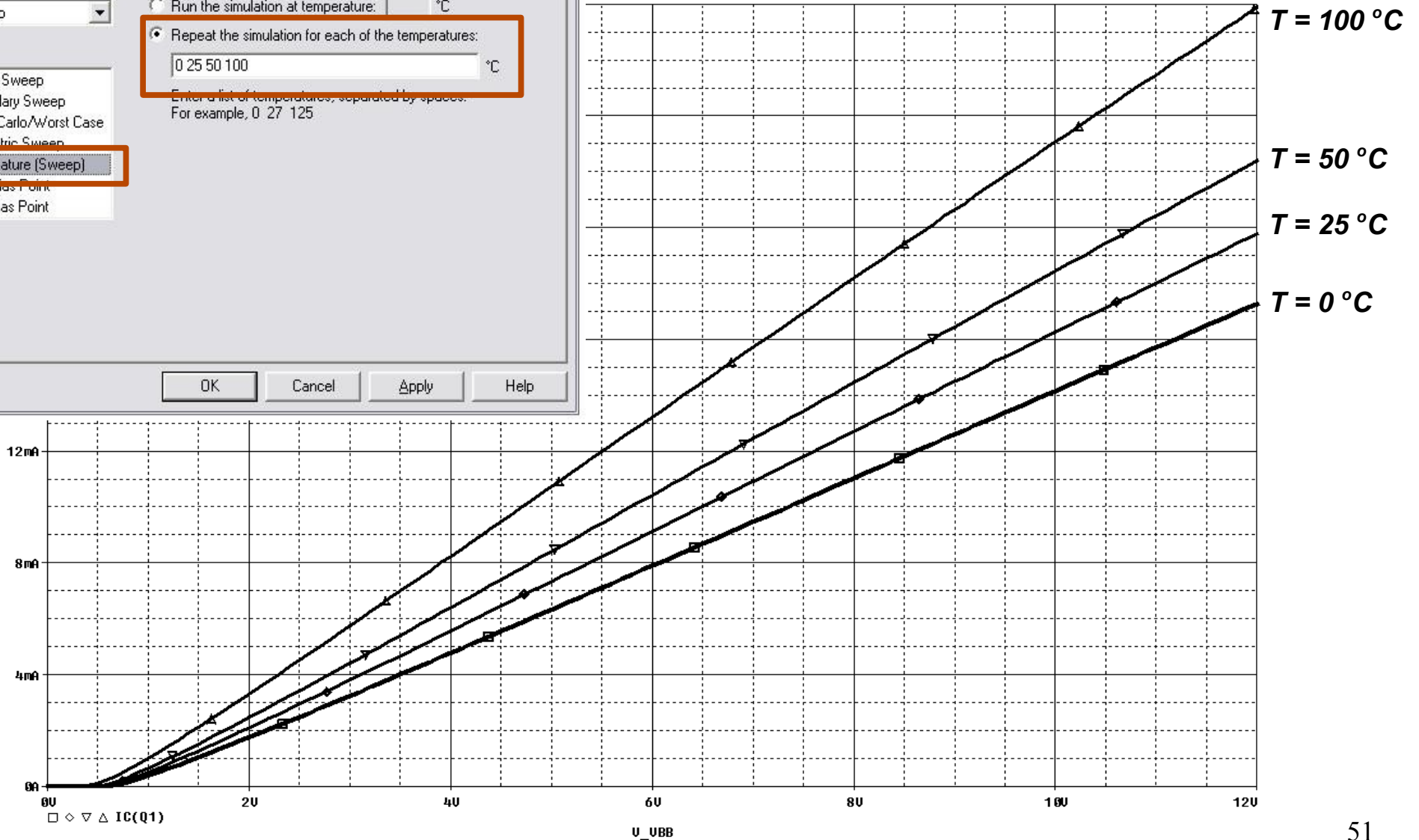
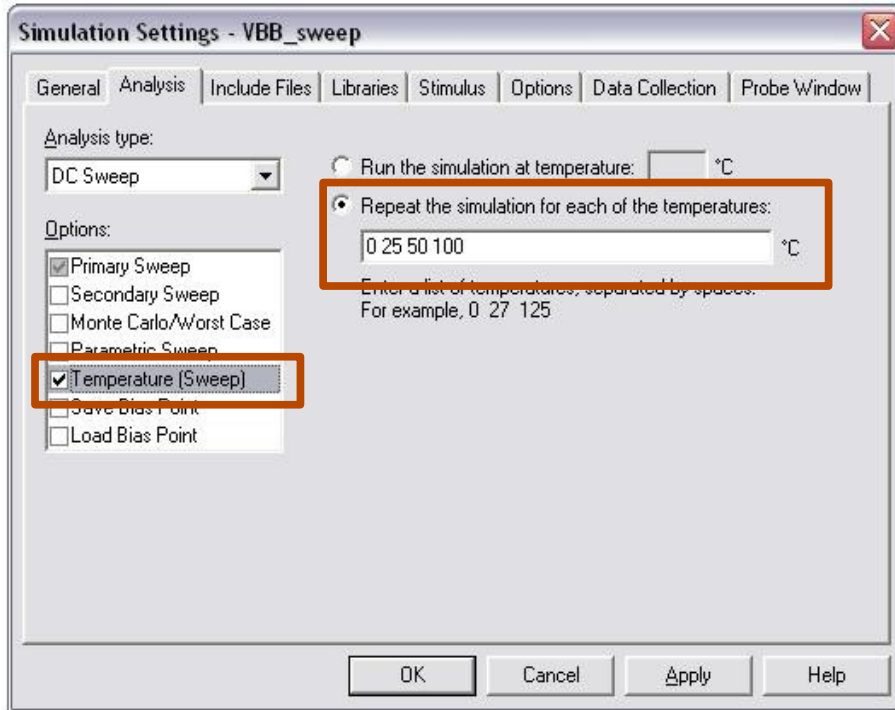
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	—	60	V
	2N2222		—	75	V
	2N2222A		—	75	V
V_{CEO}	collector-emitter voltage	open base	—	30	V
	2N2222		—	40	V
	2N2222A		—	40	V
I_C	collector current (DC)		—	800	mA
P_{tot}	total power dissipation	$T_{amb} = 25^\circ C$	—	500	mW
h_{FE}	DC current gain	$I_C = 10 \text{ mA}; V_{CE} = 10 \text{ V}$	75	—	
f_T	transition frequency	$I_C = 20 \text{ mA}; V_{CE} = 20 \text{ V}; f = 100 \text{ MHz}$	250	—	MHz
	2N2222		300	—	MHz
	2N2222A		300	—	MHz
t_{off}	turn-off time	$I_{Con} = 150 \text{ mA}; I_{Bon} = 15 \text{ mA}; I_{Boff} = -15 \text{ mA}$	—	250	ns

$h_{FE} = I_c/I_b$ vs V_{bb} (V_{ce} sweep)

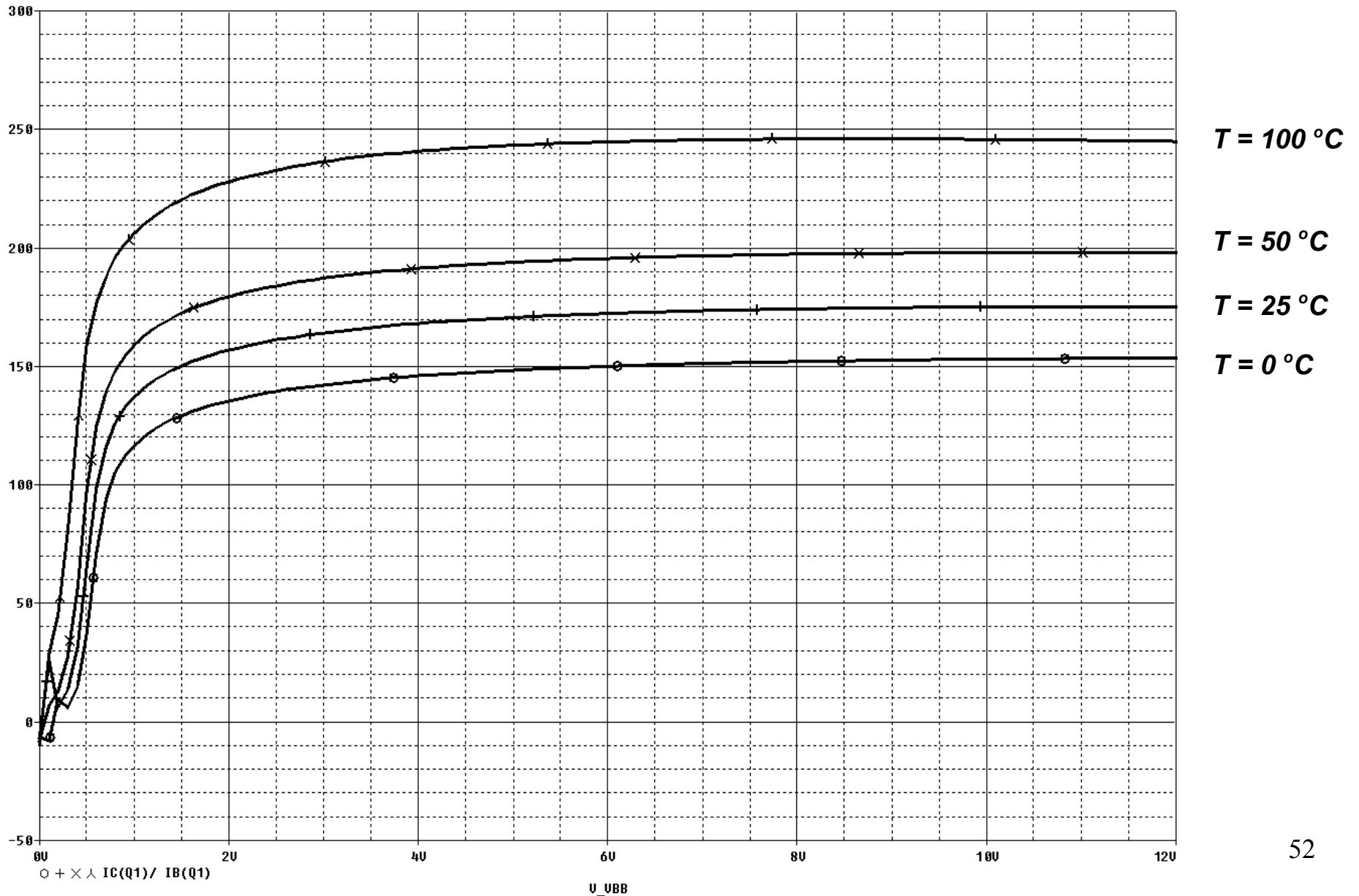


Temperature sweep



Temperature sweep

h_{FE} increases with the temperature... does it make sense?



Lab measurements

- *input characteristics* → I_b vs V_{be} , $V_{ce} = \text{const}$

$V_{ce} = V_{ce1}$		$V_{ce} = V_{ce2}$	
I_b [μA]	V_{be} [mV]	I_b [μA]	V_{be} [mV]
...
...

...
...

- *output characteristics* → I_c vs V_{ce} , $V_{be} = \text{const}$

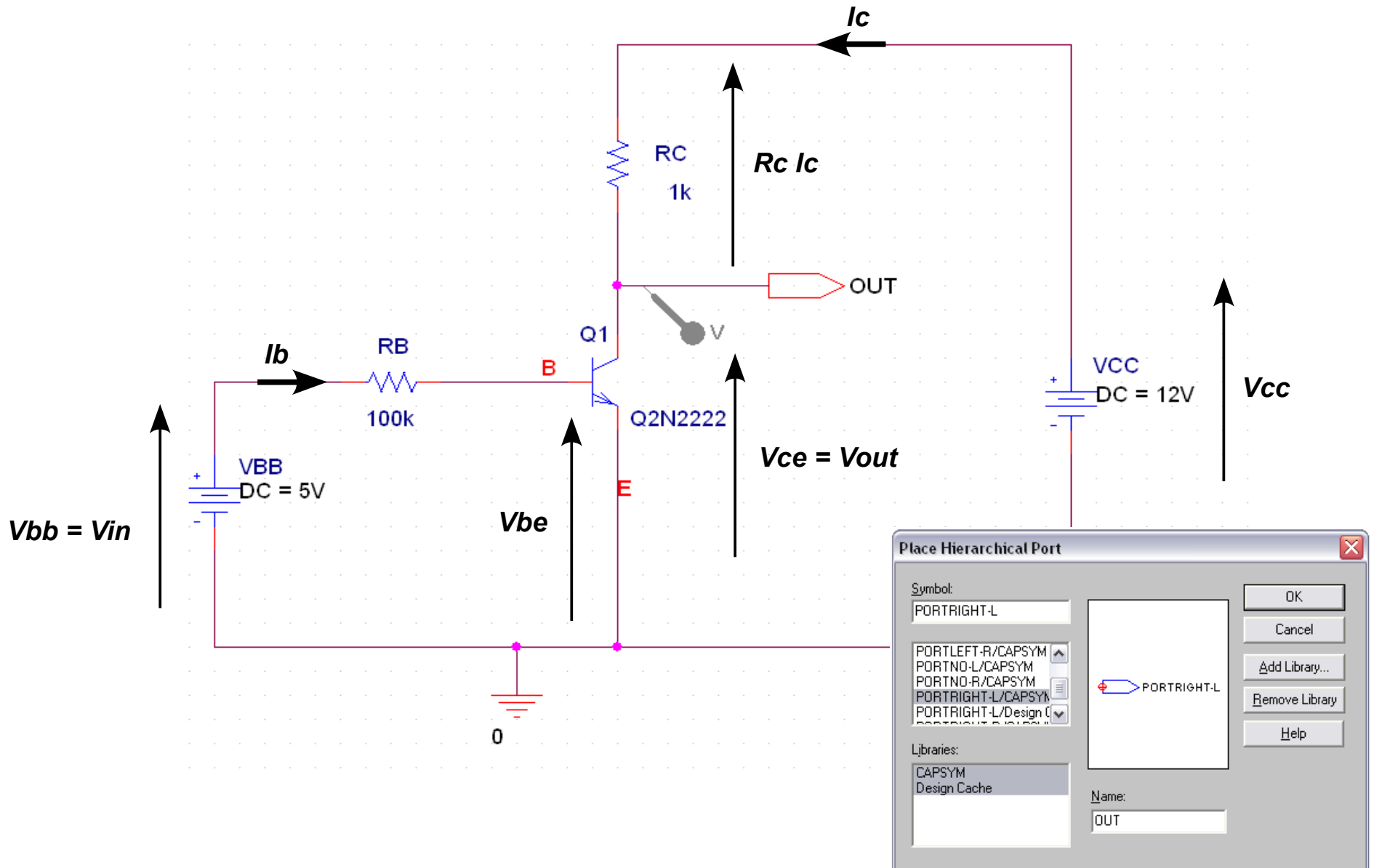
$I_b = I_{b1}$		$I_b = I_{b2}$	
I_c [μA]	V_{ce} [mV]	I_c [μA]	V_{ce} [mV]
...
...

...
...

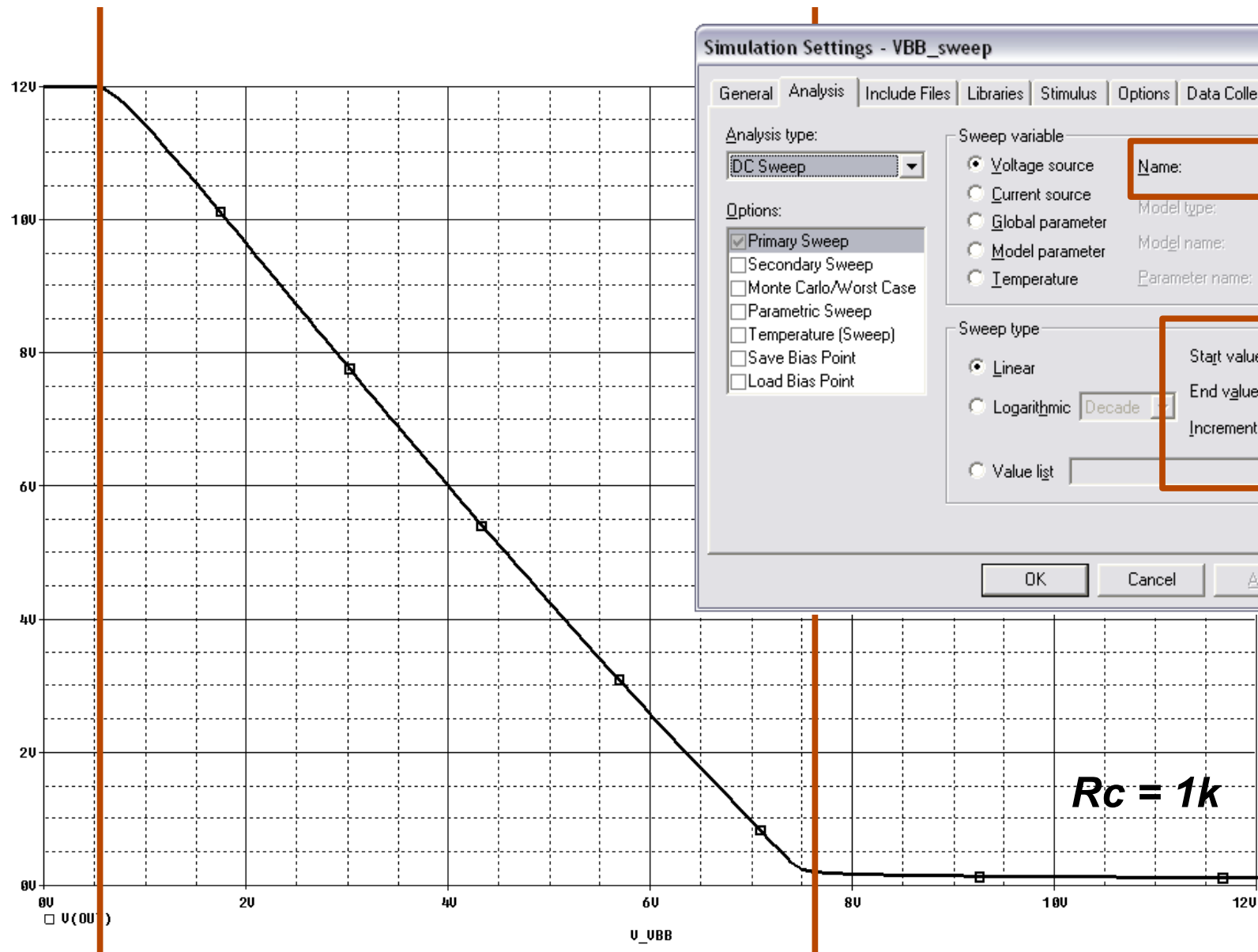
Part III
NPN common-emitter amplifier



NPN common-emitter amplifier

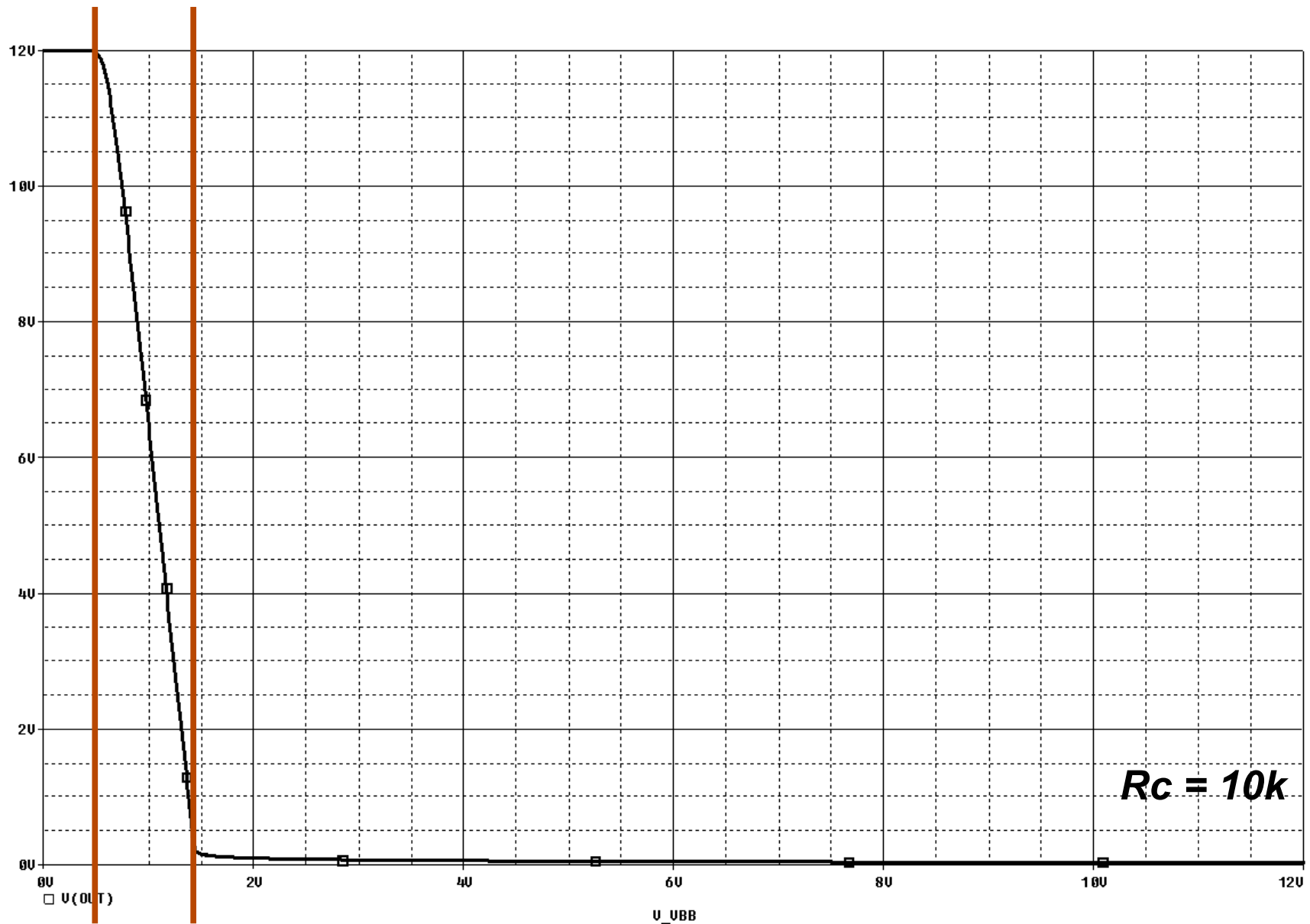


Voltage Transfer Characteristic (VTC)



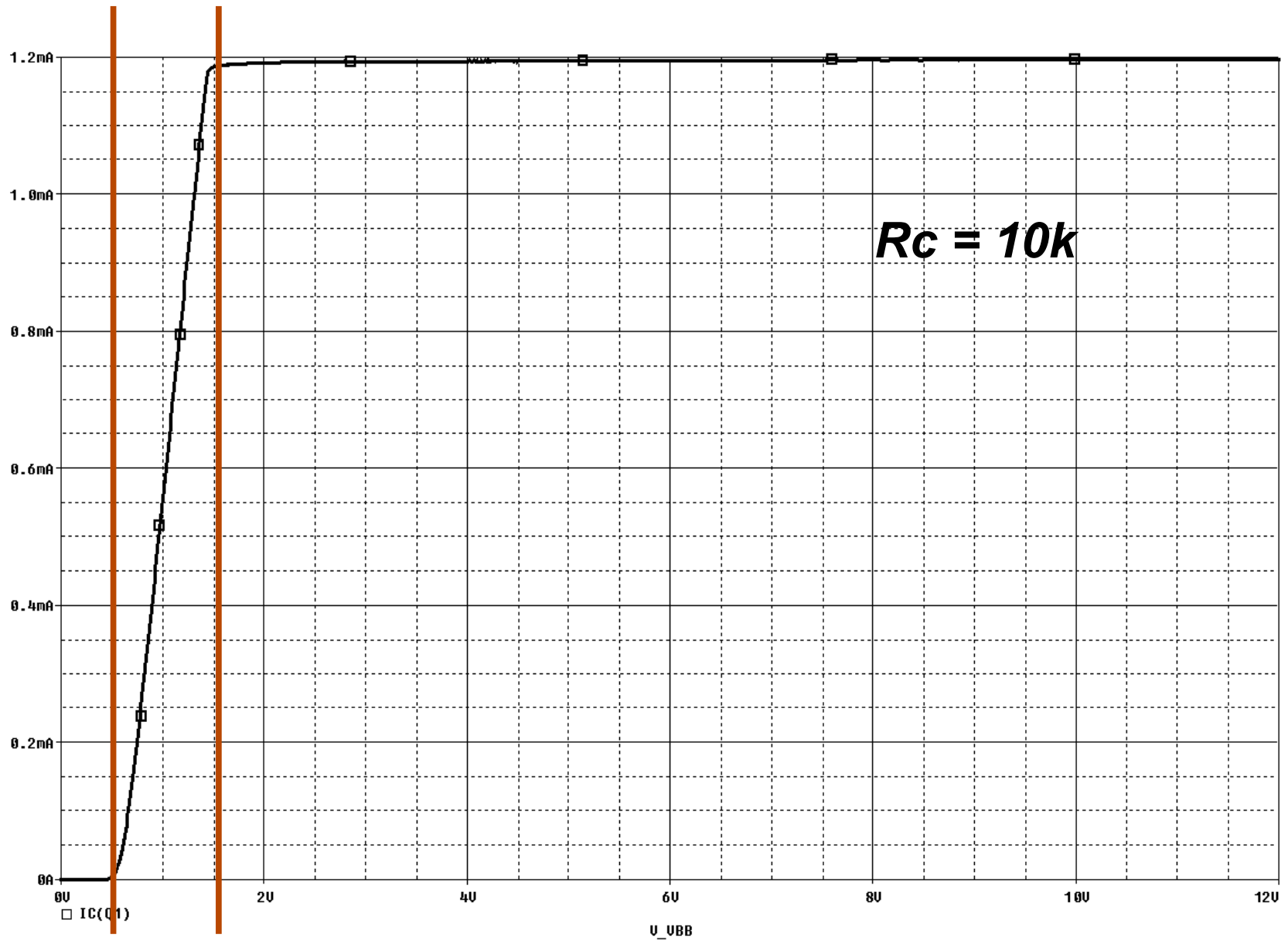
interdiction (cutoff) → active → saturation

Increasing the load



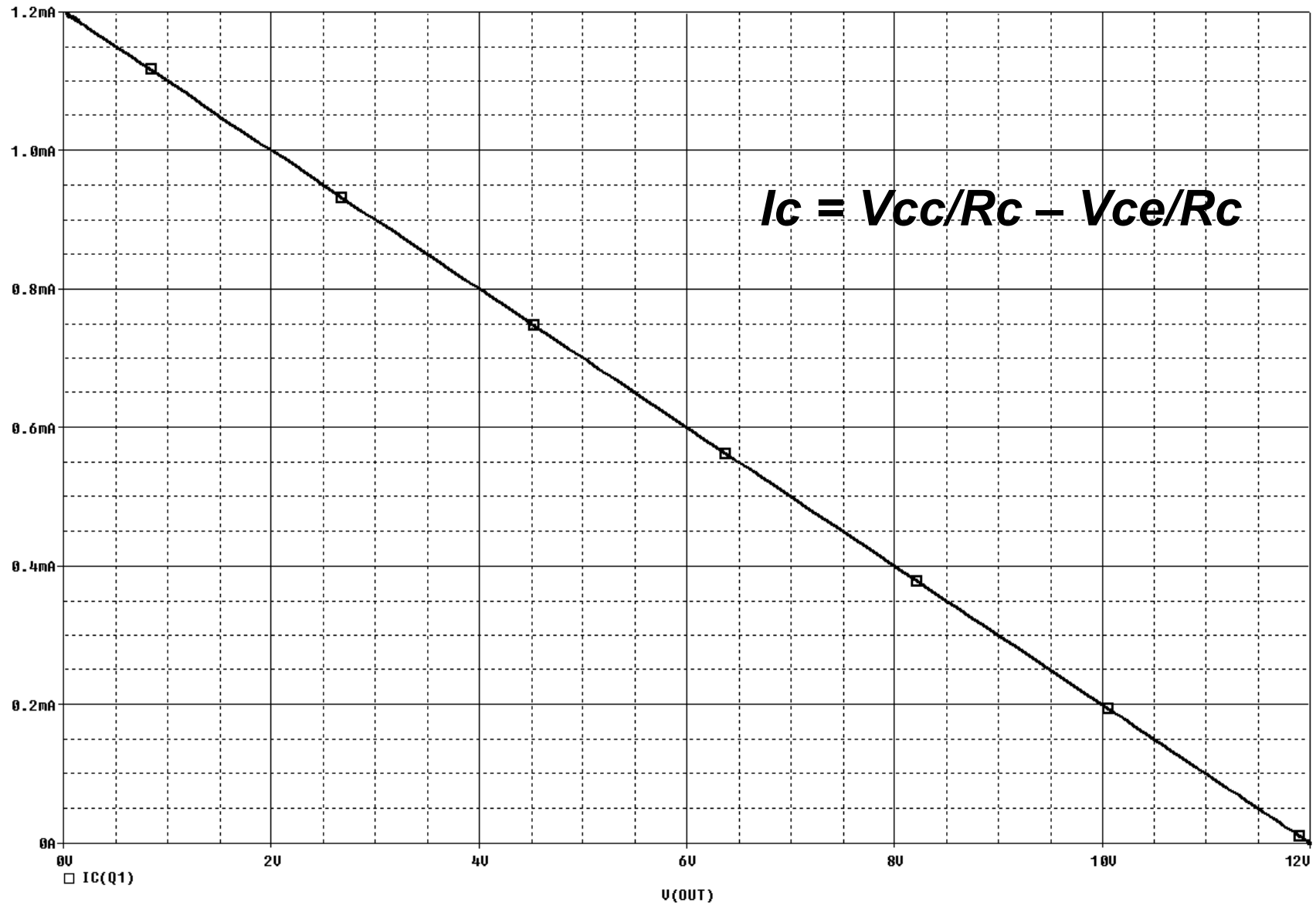
interdiction (cutoff) → active → saturation

I_c vs V_{bb}

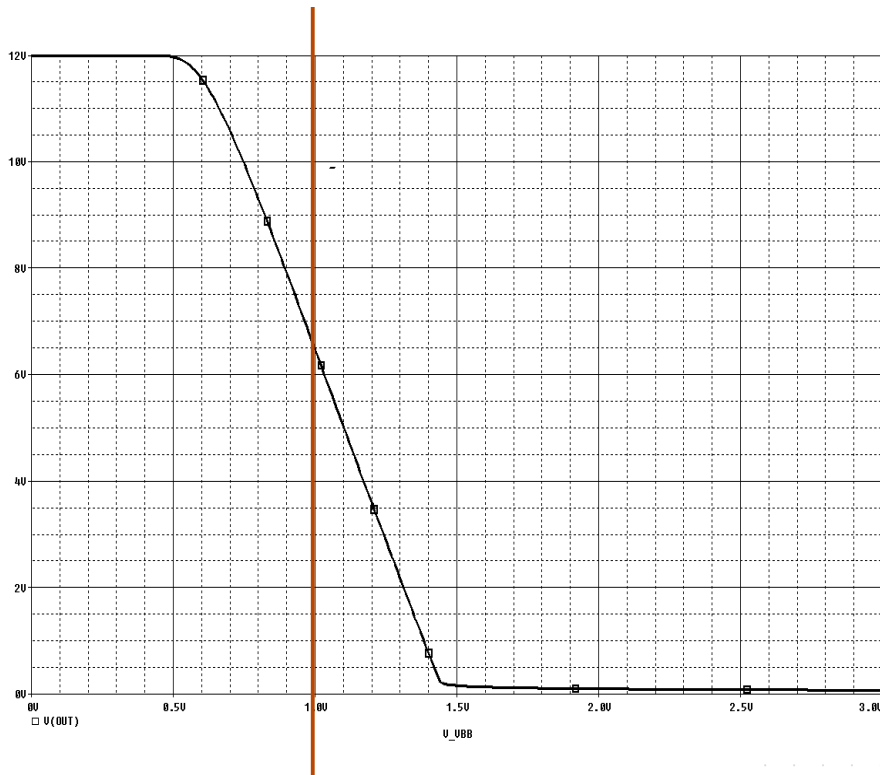


interdiction (cutoff) → active → saturation

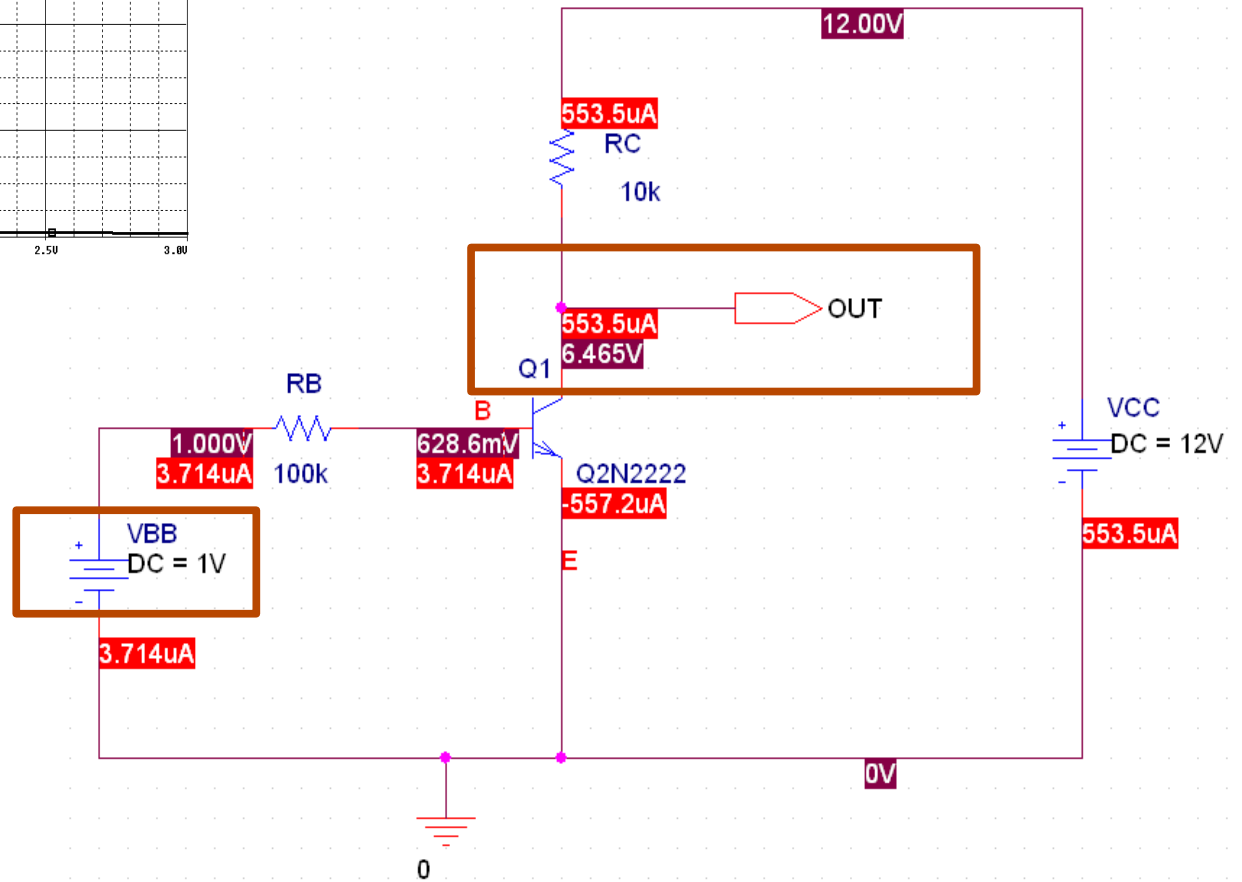
Ic vs Vce... the load line !



DC operating point



$$V_{in,DC} \approx 1V \rightarrow V_{out,DC} = V_{cc}/2 = 6V$$



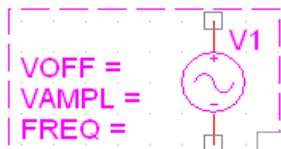
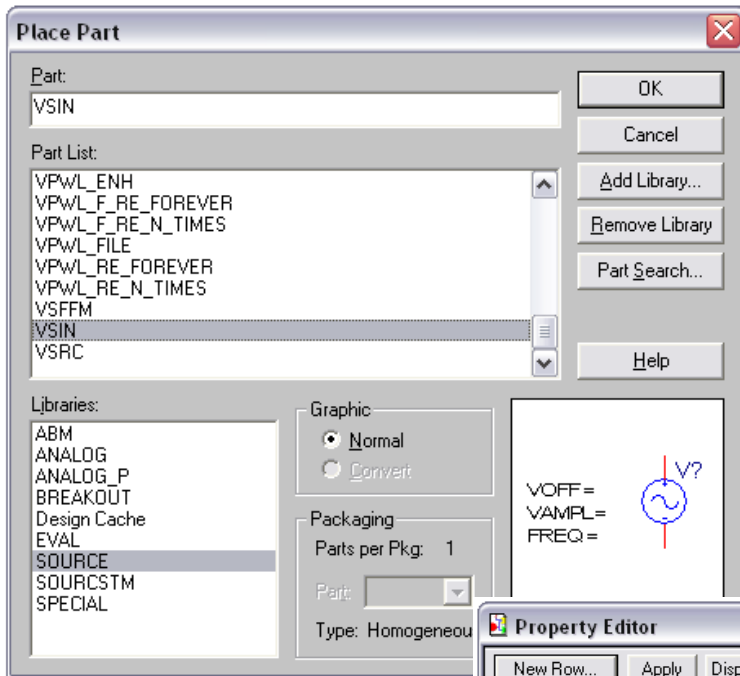
Transient analysis

- **large-signal** response of the circuit to one or more **time-dependent inputs**
 - **numerical integration** of a non linear differential equations system
 - a first DC analysis determines the **initial circuit bias conditions**

- voltages and currents are tracked over time
 - a smaller integration time step increases both the results accuracy and the simulation duration
 - sometimes convergence problems can occur

- you can specify in the simulation settings window the maximum step size in incrementing the time during transient analysis (**numerical integration time-step**)

VSIN source



VOFF =
VAMPL =
FREQ =

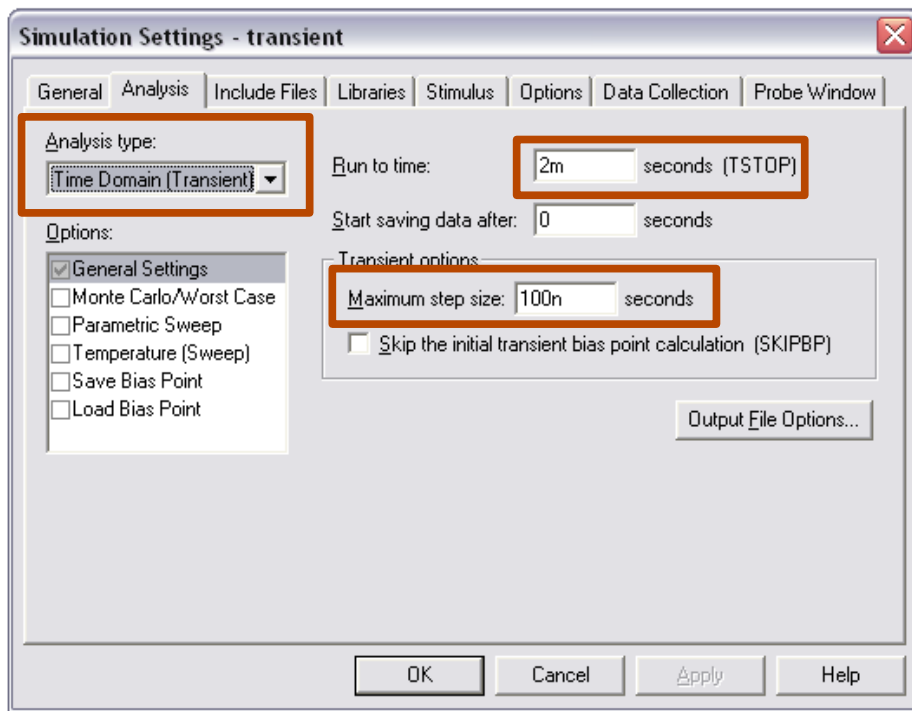
- Mirror Horizontally
- Mirror Vertically
- Rotate
- Edit Properties...
- Edit Part
- Descend Hierarchy
- Ascend Hierarchy
- Zoom In
- Zoom Out
- Go To...
- Cut
- Copy
- Delete

The 'Property Editor' dialog box shows the properties for the selected 'VSIN' part. The 'Filter by' dropdown is set to '< Current properties >'. The table below lists the properties and their values.

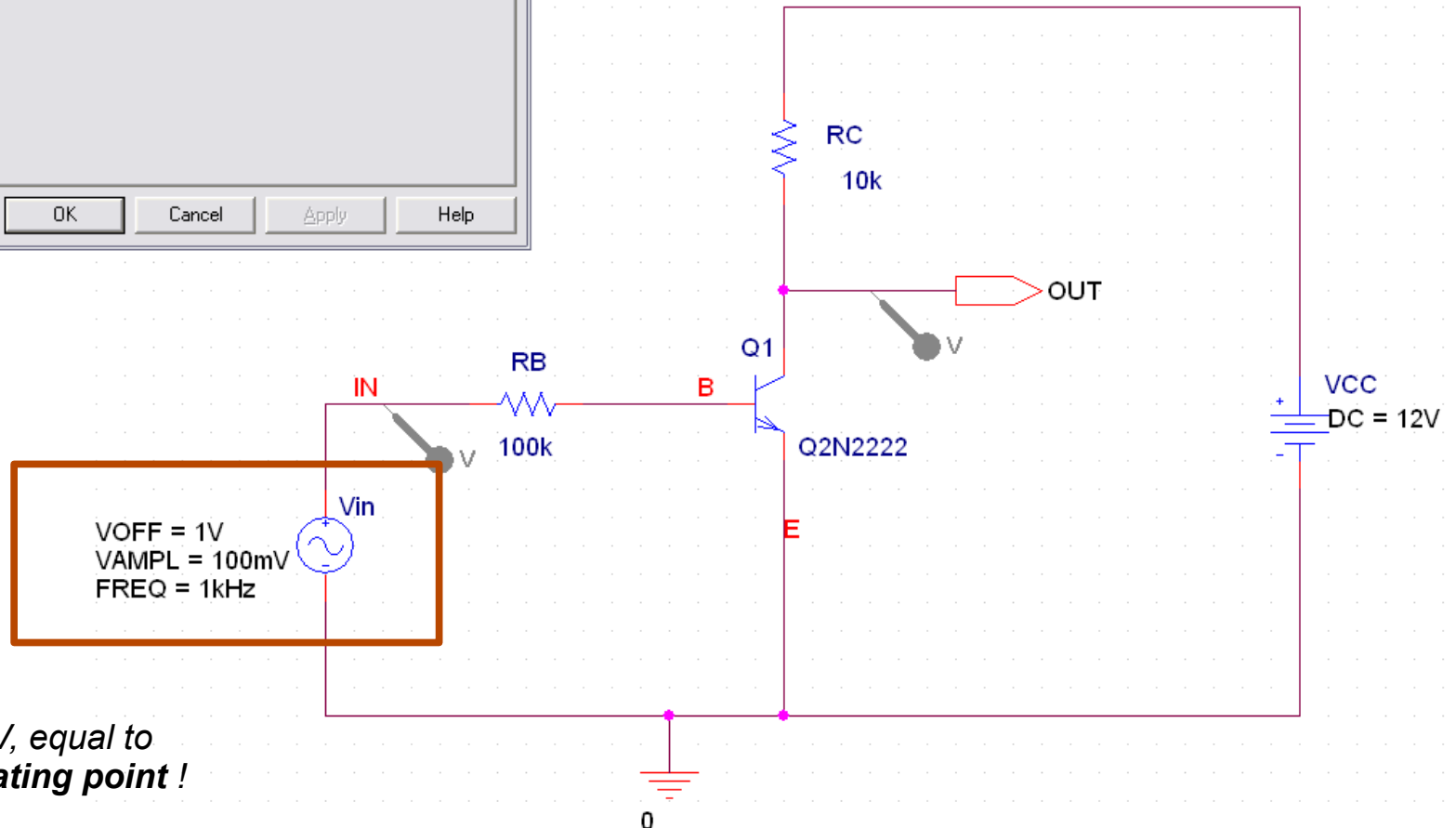
A	
SCHEMATIC1 : PAGE1	
AC	
Color	Default
DC	
Designator	
DF	0
FREQ	
Graphic	VSIN.Normal
ID	
Implementation	
Implementation Path	
Implementation Type	PSpice Model
Name	100759
Part Reference	V1
PCB Footprint	
PHASE	0
Power Pins Visible	<input type="checkbox"/>
Primitive	DEFAULT
PSpiceOnly	TRUE
PSpiceTemplate	V*@REFDES %+ %- ?DCID
Reference	V1
Source Library	C:\PSpice\CAPTURE\LI...
Source Package	VSIN
TD	0
Value	VSIN
VAMPL	
VOFF	

- **DF** → *dump factor*
- **FREQ** → *frequency*
- **PHASE**
- **TD** → *delay*
- **VAMPL** → *amplitude*
- **VOFF** → *DC level*

Transient analysis

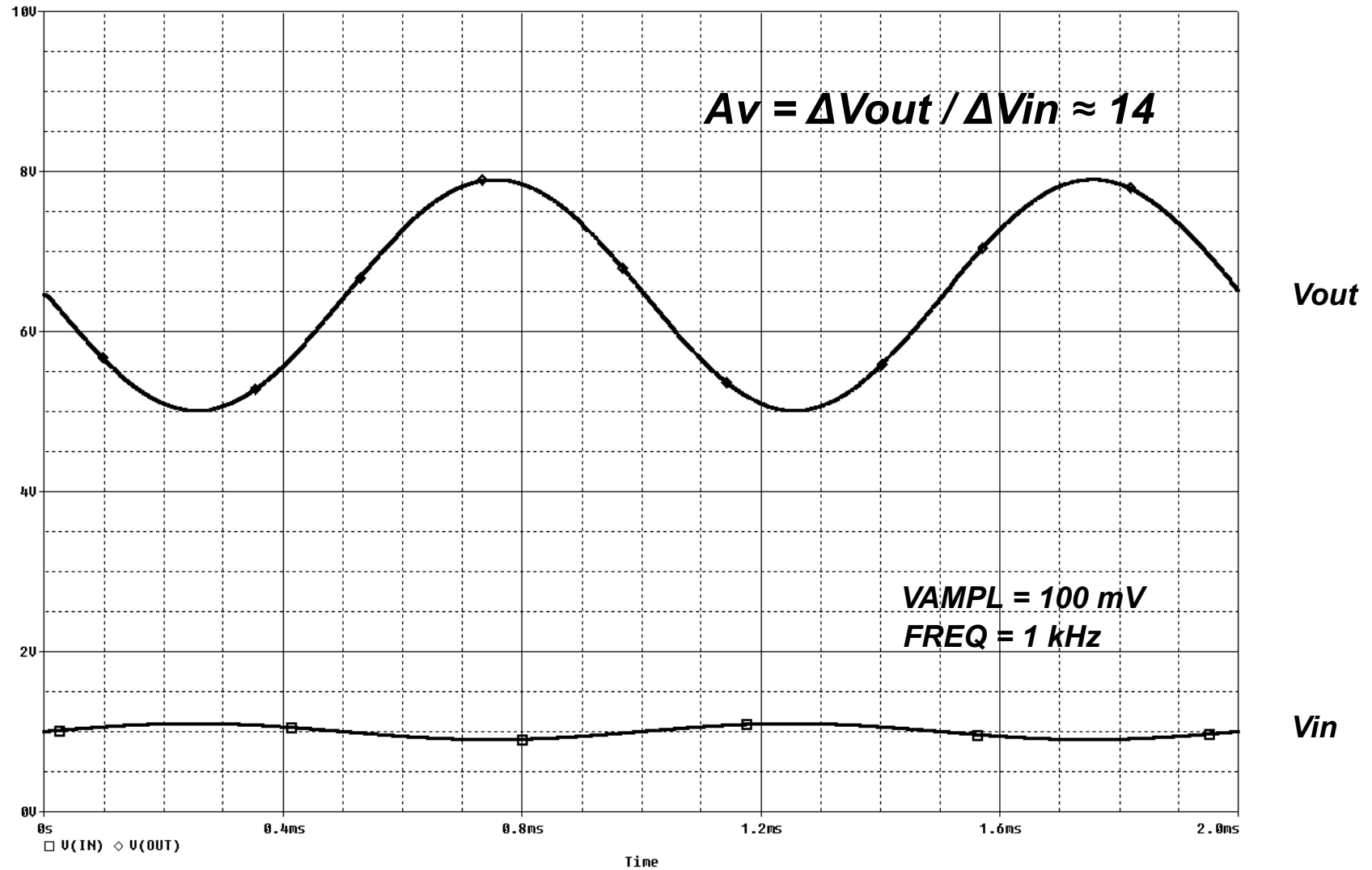


Choose a duration $\sim 2/FREQ$ and an integration time-step of 10-100 ns



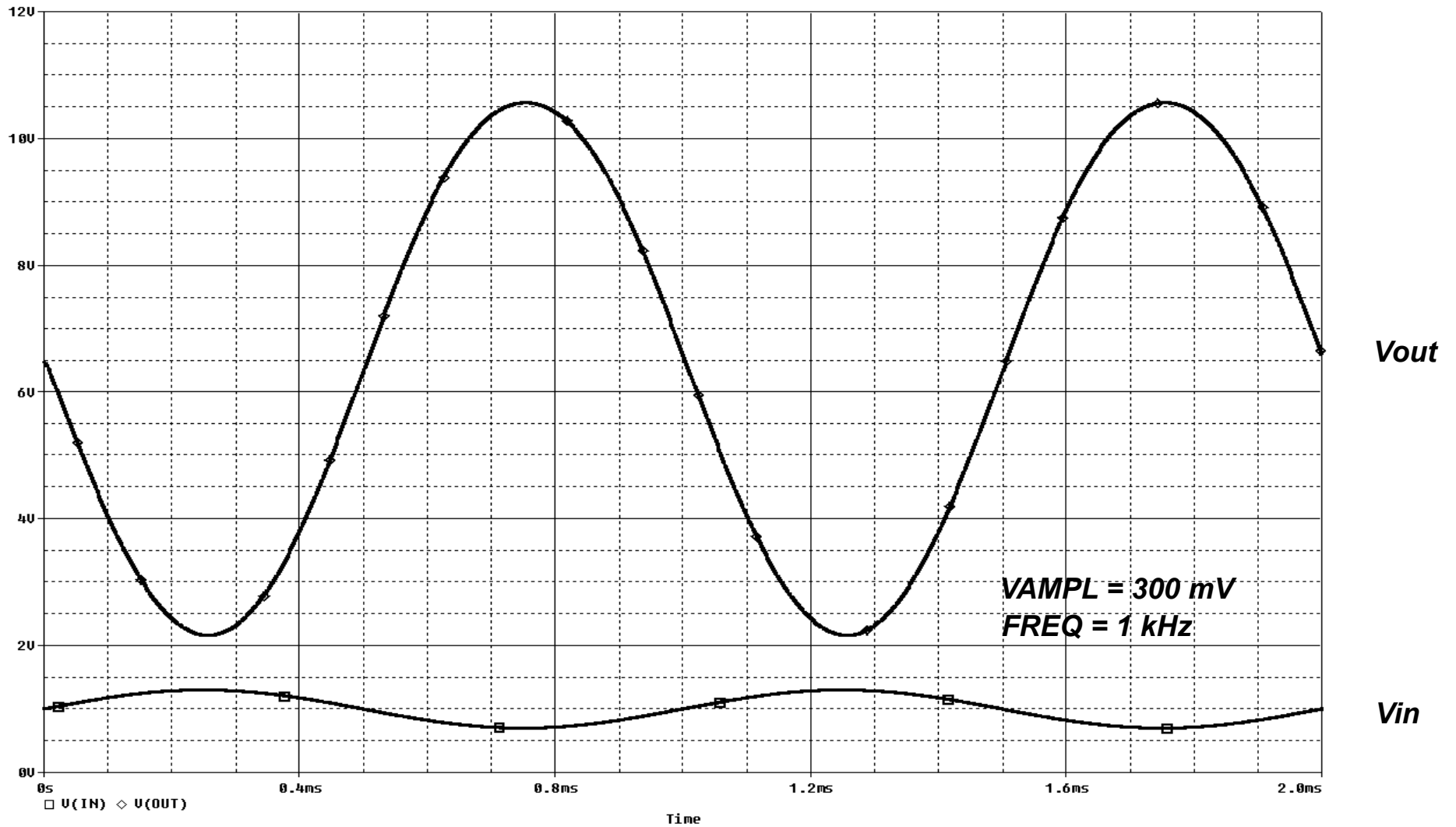
$V_{OFF} = V_{in,dc} = 1V$, equal to the input DC operating point !

Transient analysis

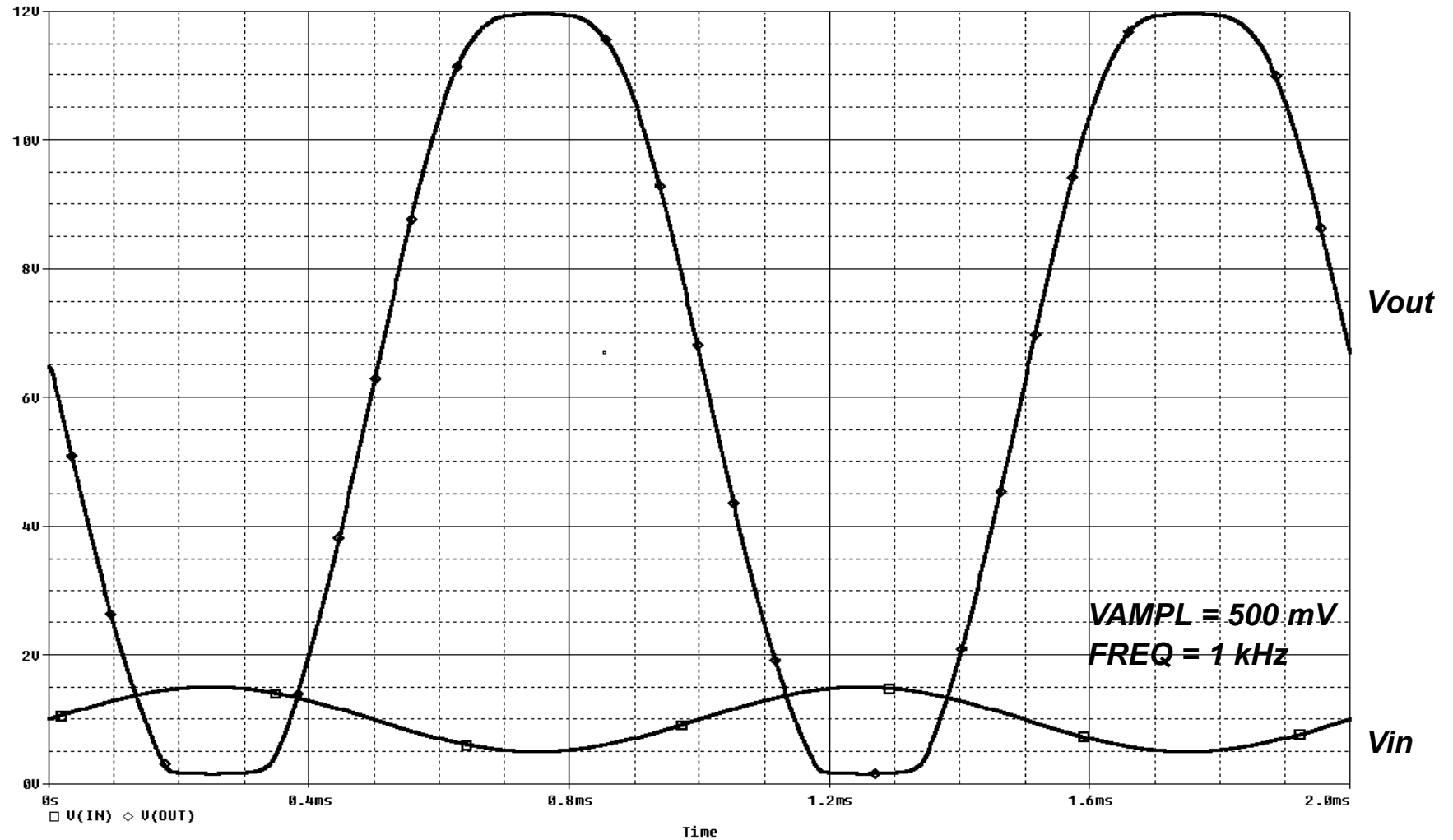


The circuit is an inverting amplifier !

Increasing the amplitude

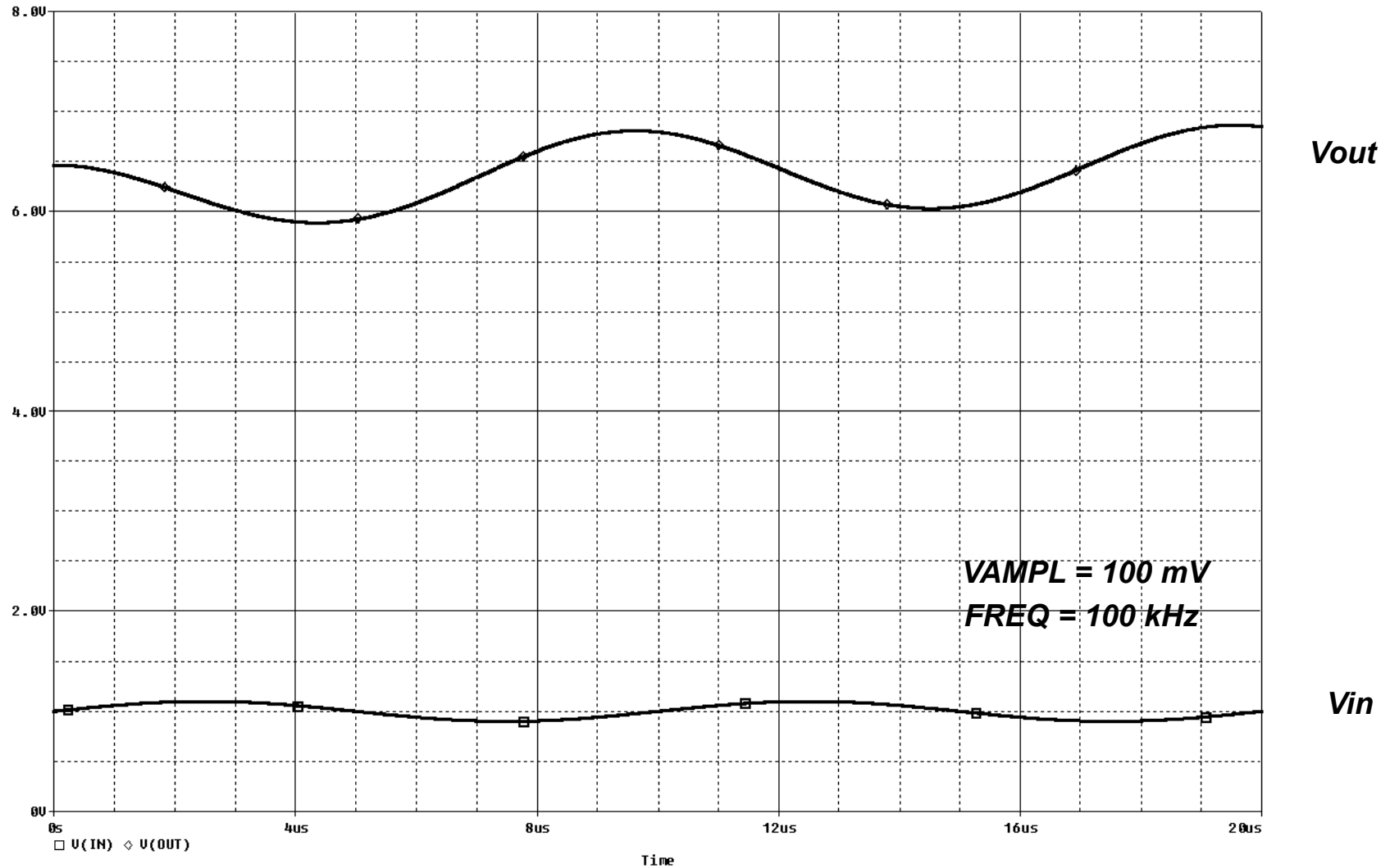


Output saturation



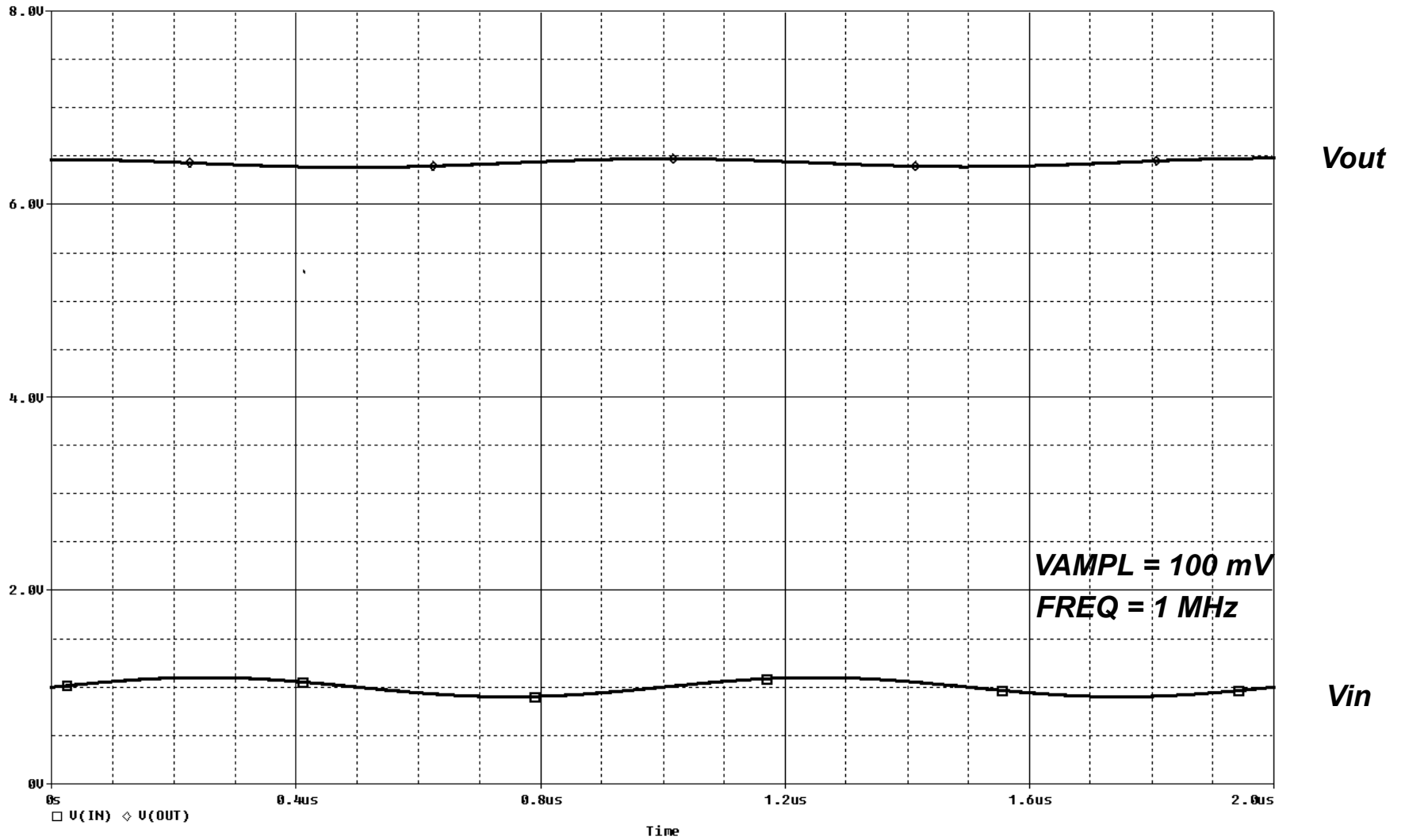
Are you surprised ?

Increasing the frequency



Note that a phase difference exist !

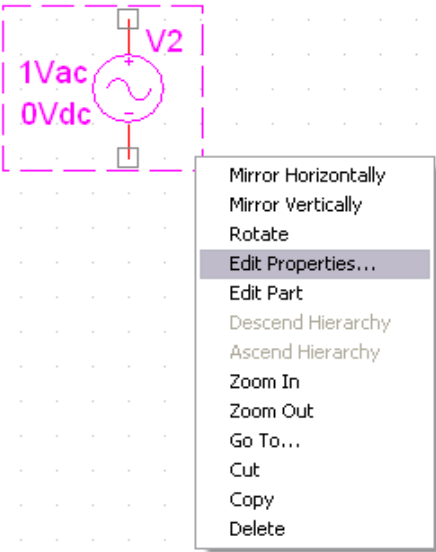
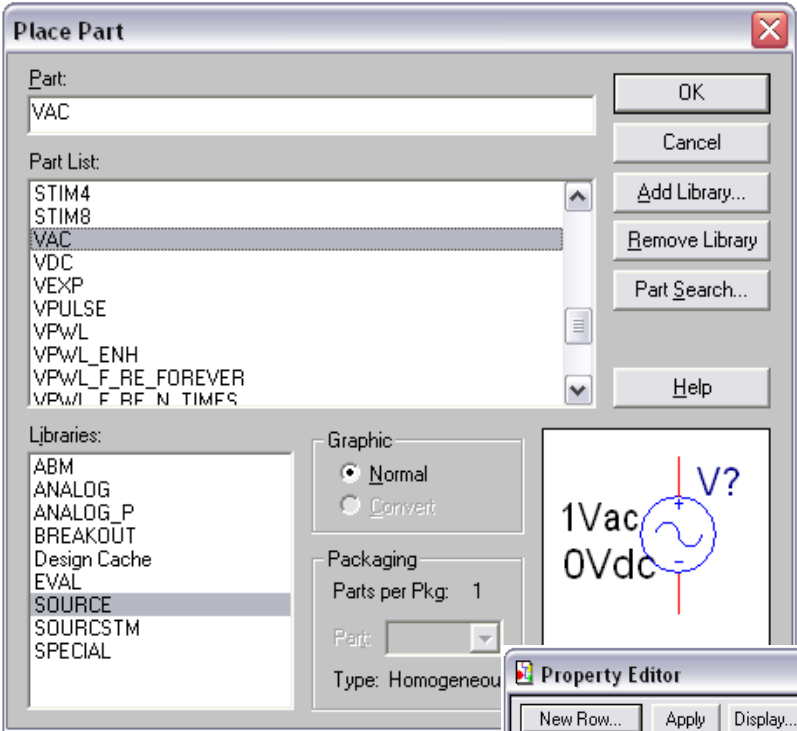
Increasing the frequency



AC analysis

- **small-signal** frequency response of the circuit **linearized** around the bias point by sweeping one or more AC sources over a range of frequencies
 - **non-linear devices** (diodes, transistors etc.) are linearized to determine their AC **small-signal models**
 - all independent voltage and current sources that have **AC specifications** are inputs to the circuit
- outputs include voltages and currents with **magnitude** and **phase**
- the best way to use AC sweep analysis is **to set the source magnitude to one** (e.g. ACMAG = 1V, AC=1A) in this way **the measured output equals the voltage/current gain** (relative to the input source) at that output
- the sweep can be linear, logarithmically by decades or logarithmically by octaves

VAC source

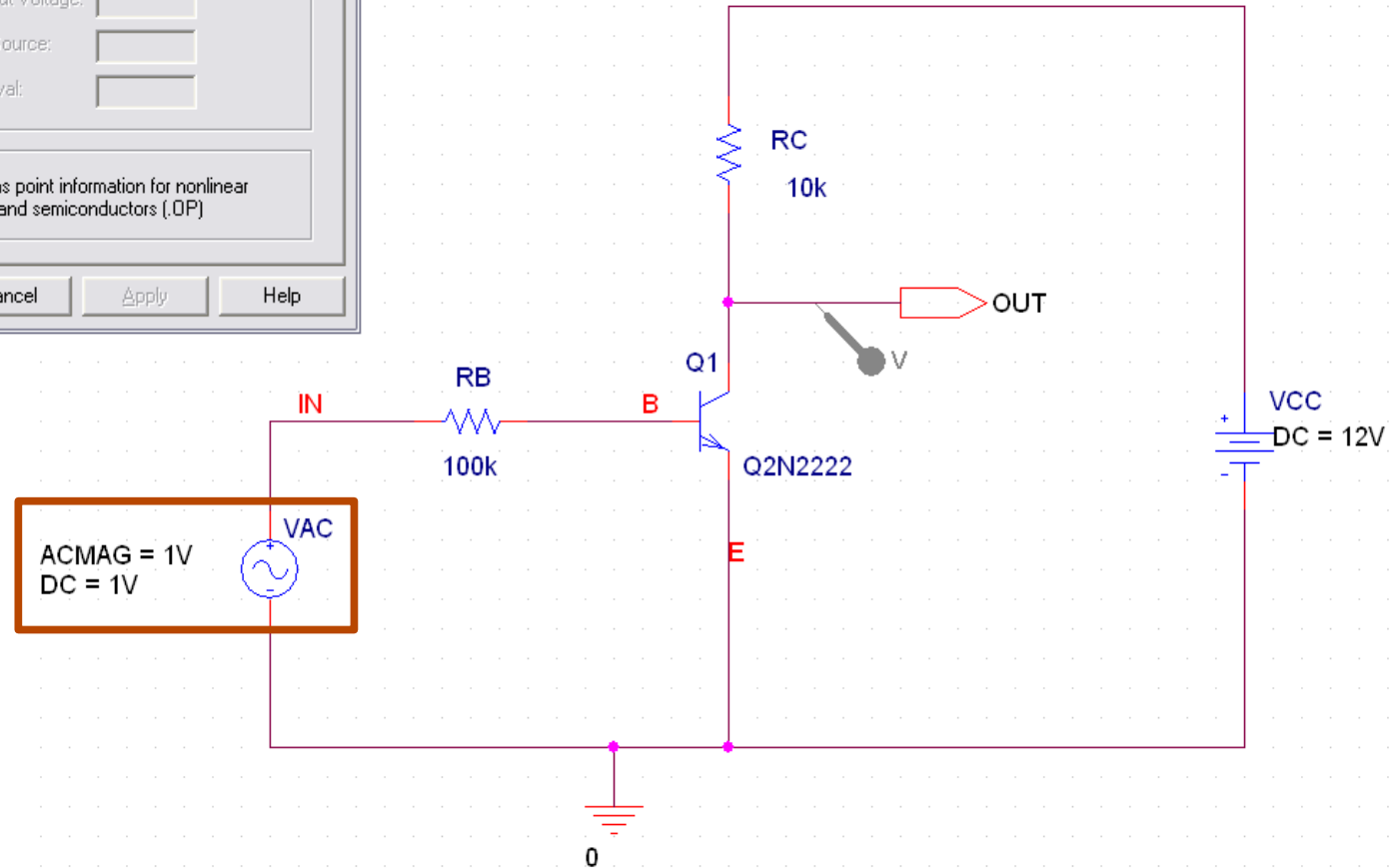
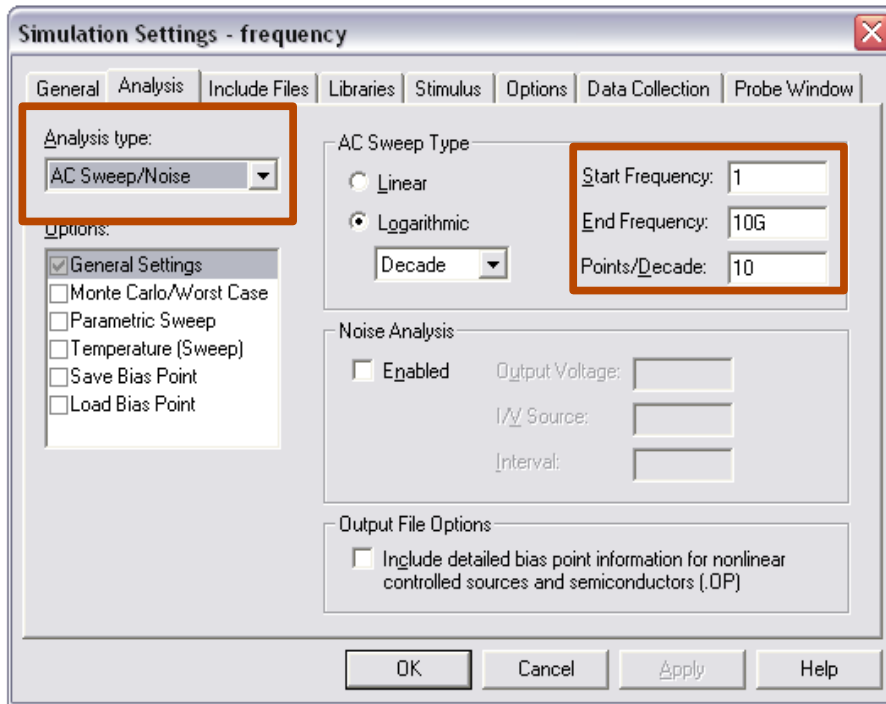


Property Editor

A	
SCHEMATIC1 : PAGE1	
ACMAG	1Vac
ACPHASE	
Color	Default
DC	0Vdc
Designator	
Graphic	VAC.Normal
ID	
Implementation	
Implementation Path	
Implementation Type	PSpice Model
Name	100905
Part Reference	V2
PCB Footprint	
Power Pins Visible	<input type="checkbox"/>
Primitive	DEFAULT
PSpiceOnly	TRUE
PSpiceTemplate	V*@REFDES %+ %- ?DCID
Reference	V2
Source Library	C:\PSPICE\CAPTURE\LI...
Source Package	VAC
Value	VAC

- **ACMAG** → *amplitude*
- **DC** → *DC level (offset)*

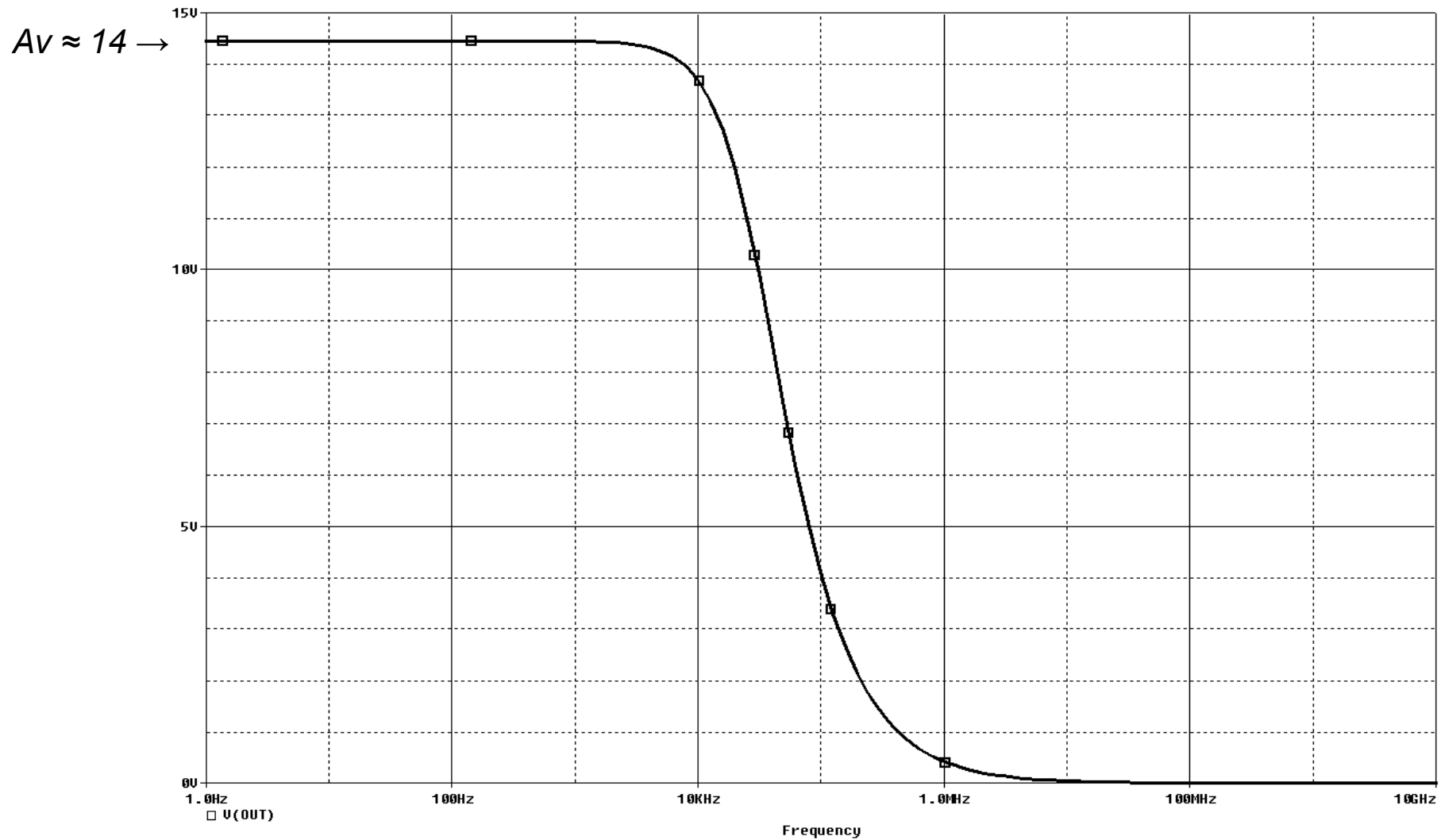
AC analysis



Remind !

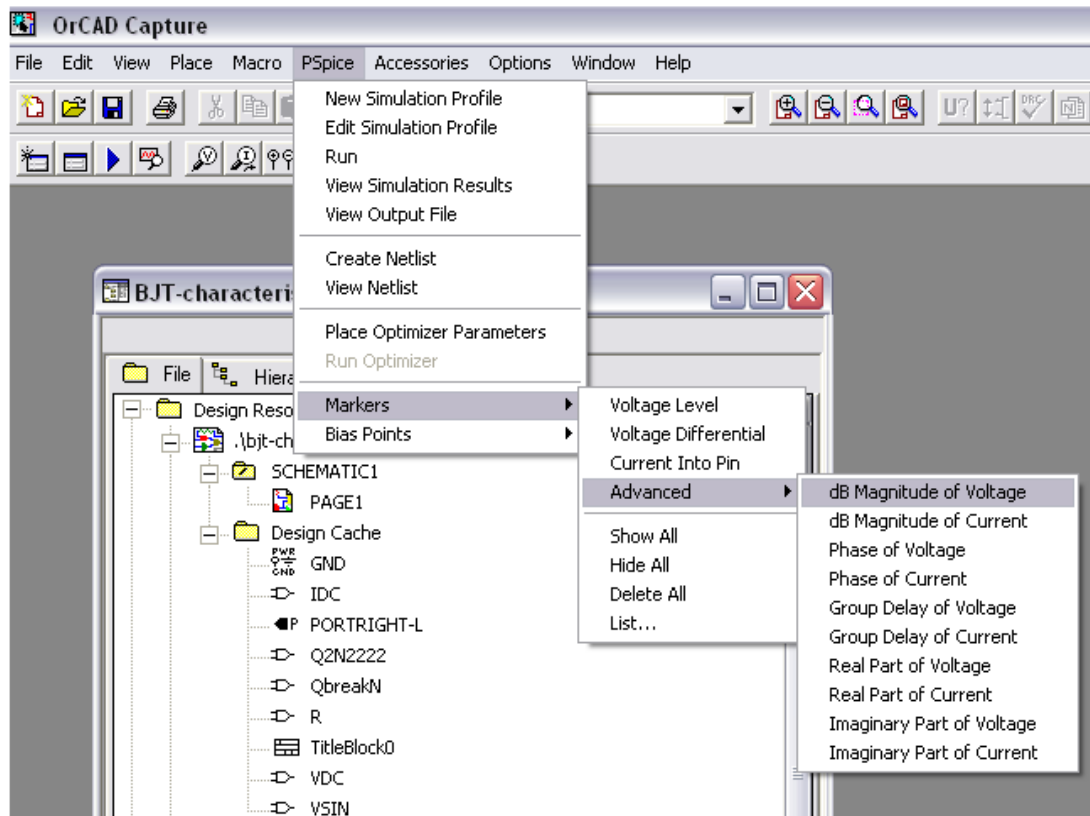
The AC analysis is a **small signal** analysis! The circuit is **linearized** around the DC operating point, hence you can use any ACMAG value! By using ACMAG=1V you immediately obtain **the voltage gain plot** with $V_{out}(f) = V_{out}(f) / 1V$

V_{out}/V_{in} frequency response



*The voltage gain decreases by increasing the signal frequency \rightarrow **low pass filter !***

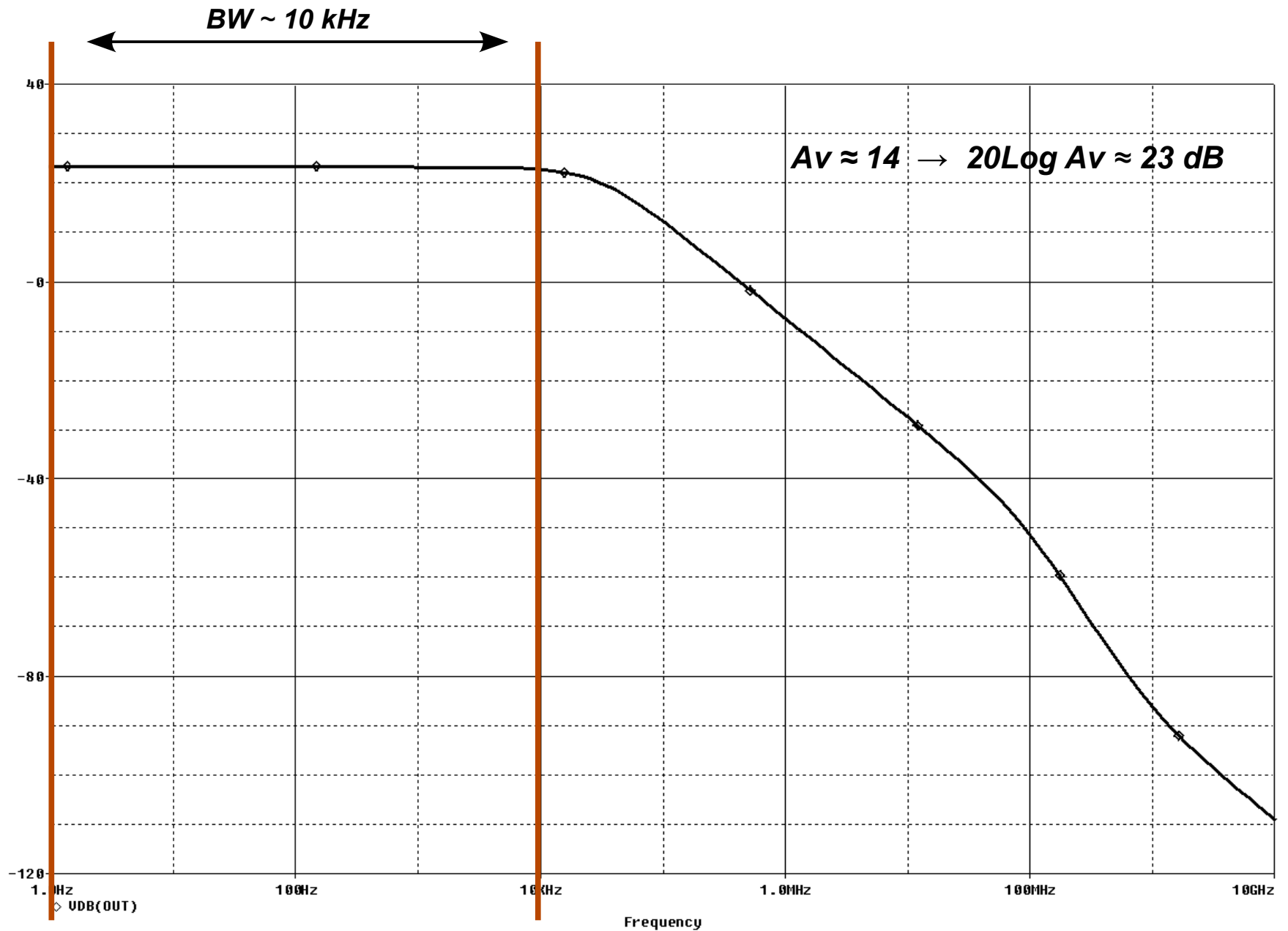
dB voltage gain



*You can plot **dB voltages and currents** and **phases** using special markers*

PSpice → Markers → Advanced → dB Magnitude of Voltage

dB voltage gain



Backup

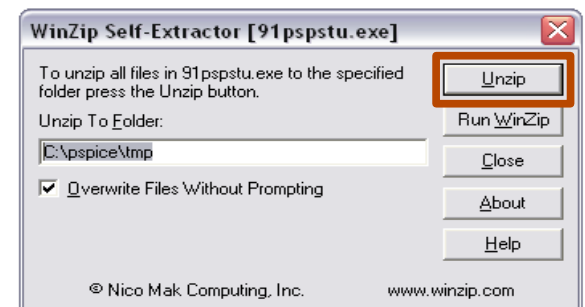
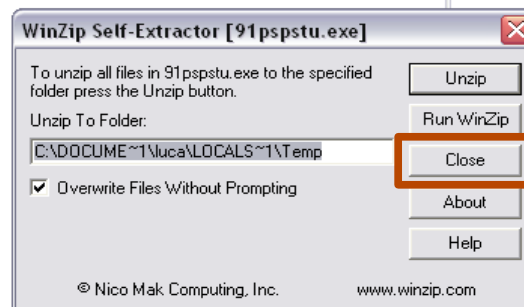
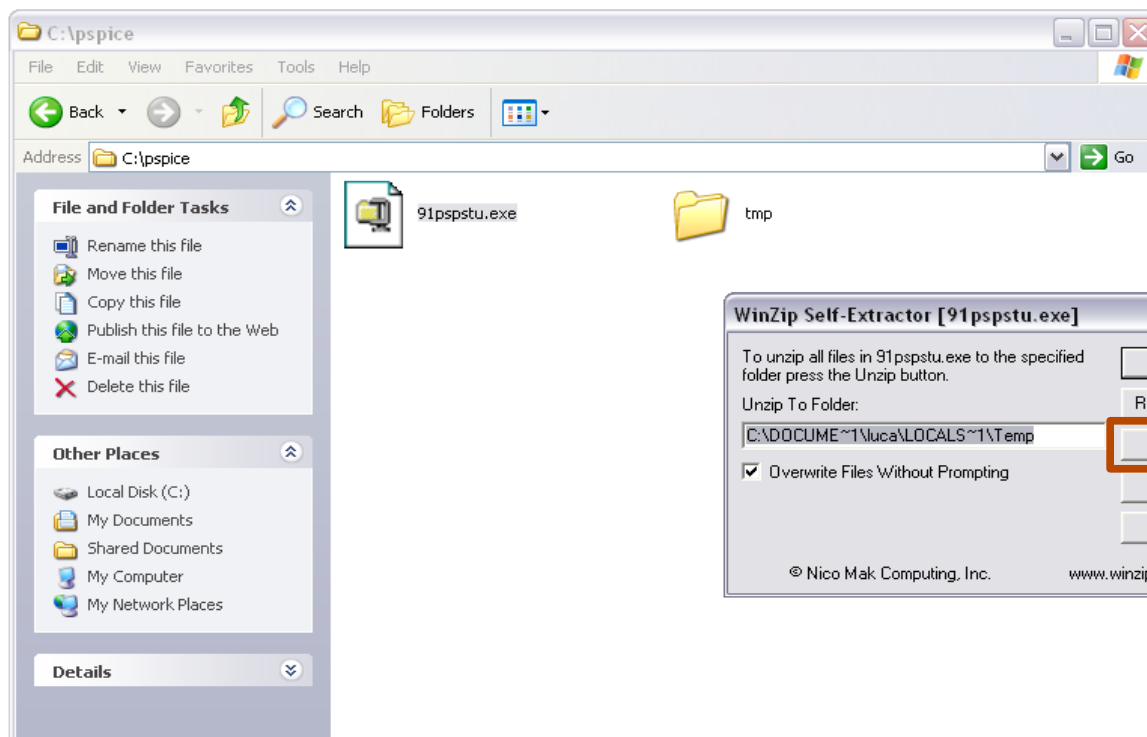
Installation details

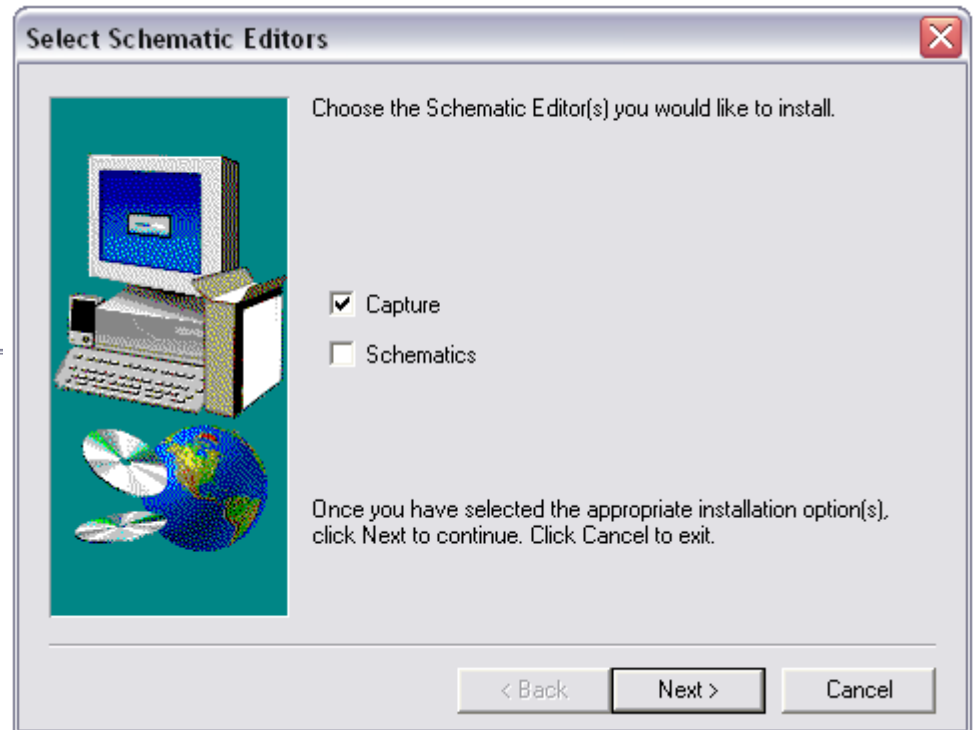
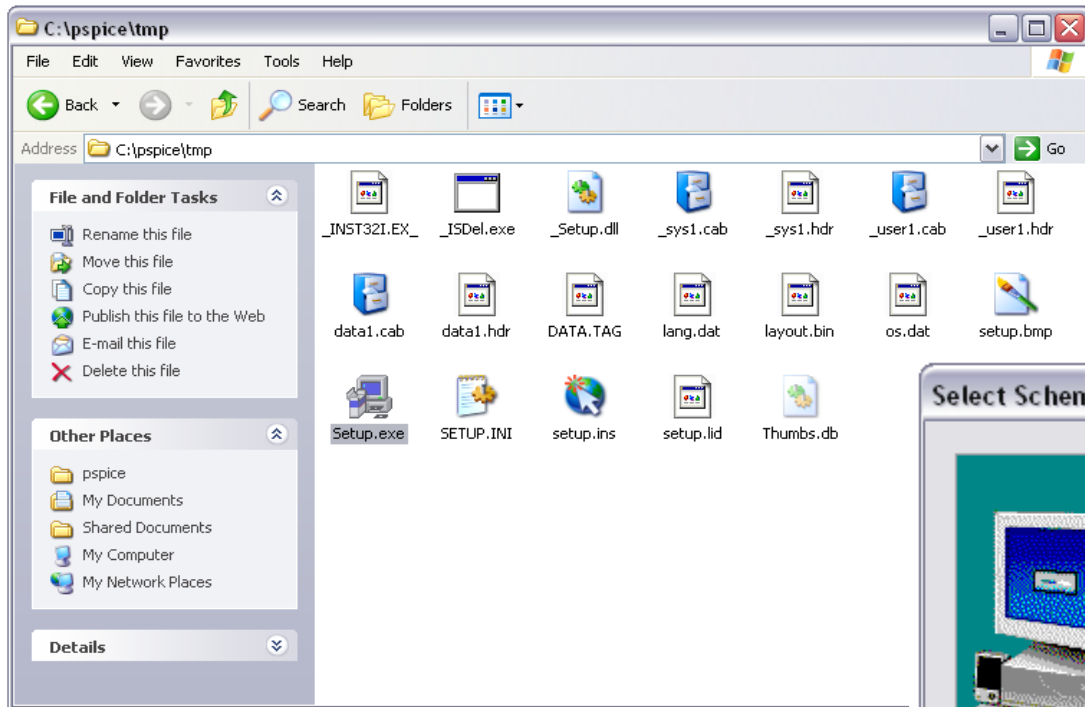
- create a main **installation directory** `C:\pspice`
- download the Windows program executable **91pspstu.exe** (~27 MB) and put it in `C:\pspice`

<http://personalpages.to.infn.it/~pacher/pspice/91pspstu.exe>

www.electronics-lab.com/downloads/schematic/013/index.html

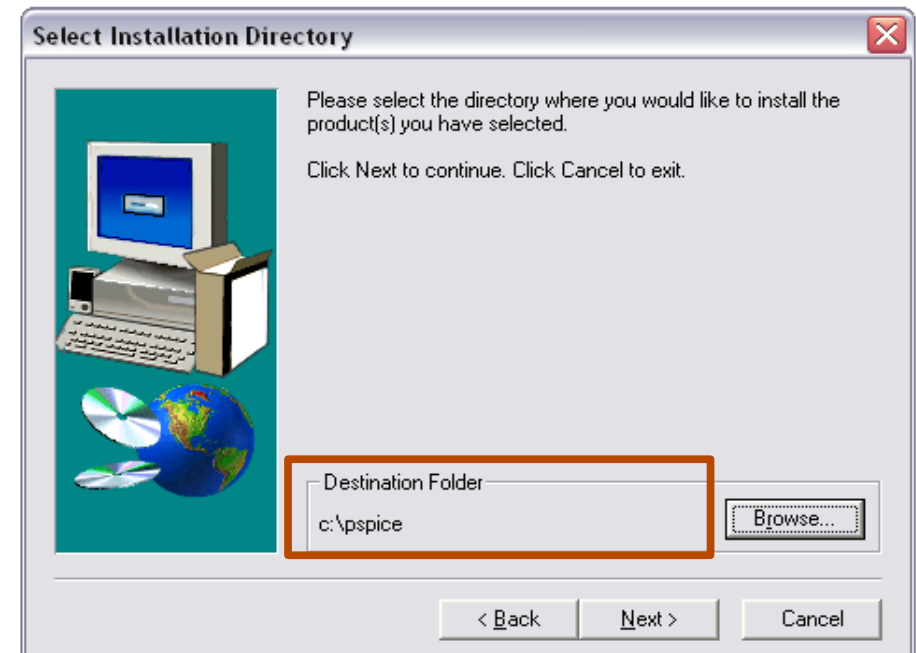
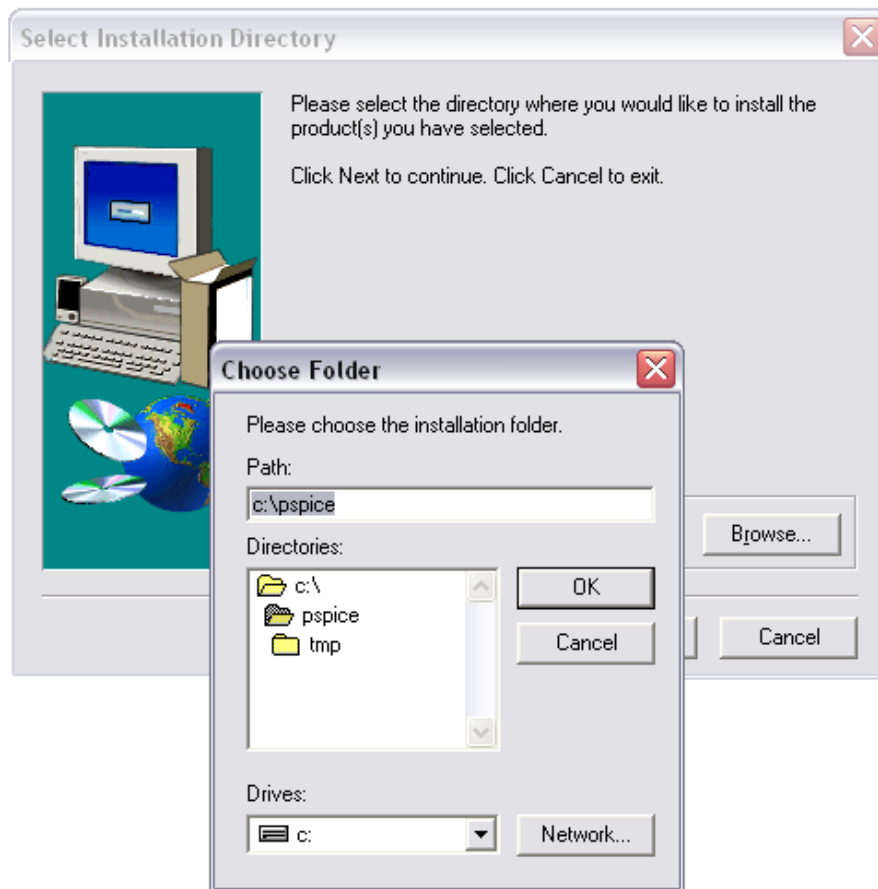
- the executable is a self-extractor compressed file, create a `C:\pspice\tmp` temporary directory for the extracted installation files and launch the 91pspstu.exe executable

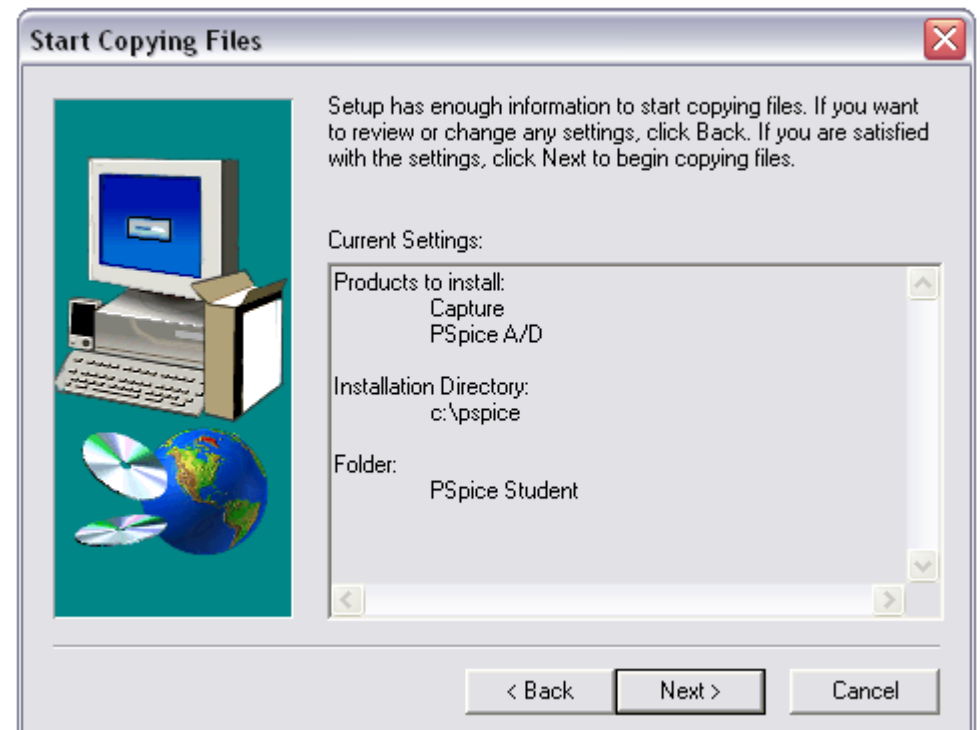
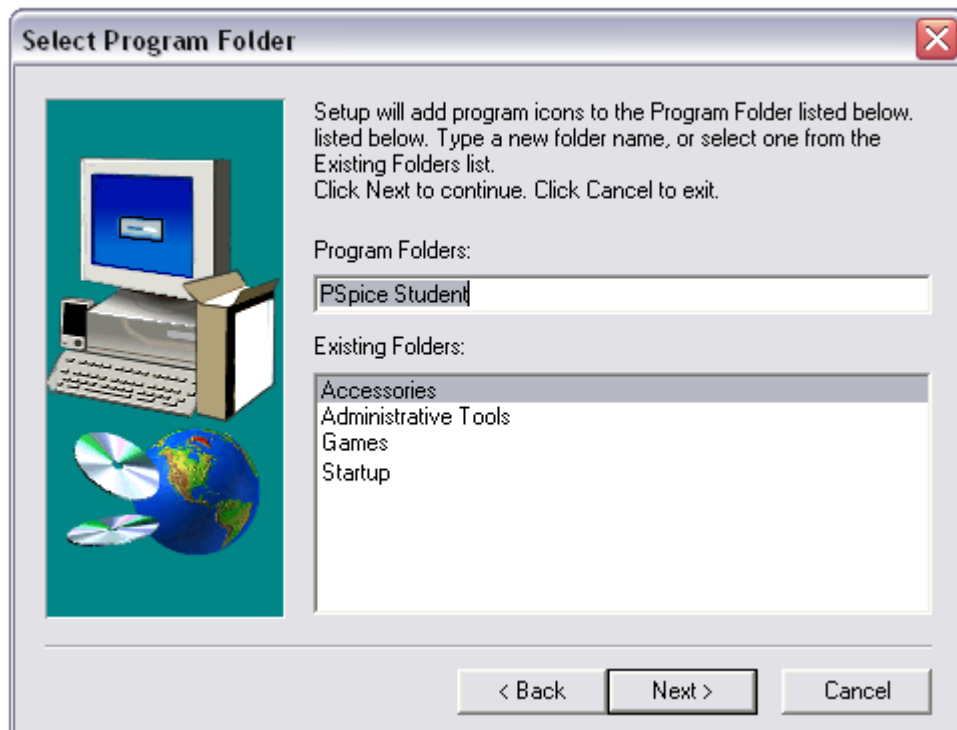


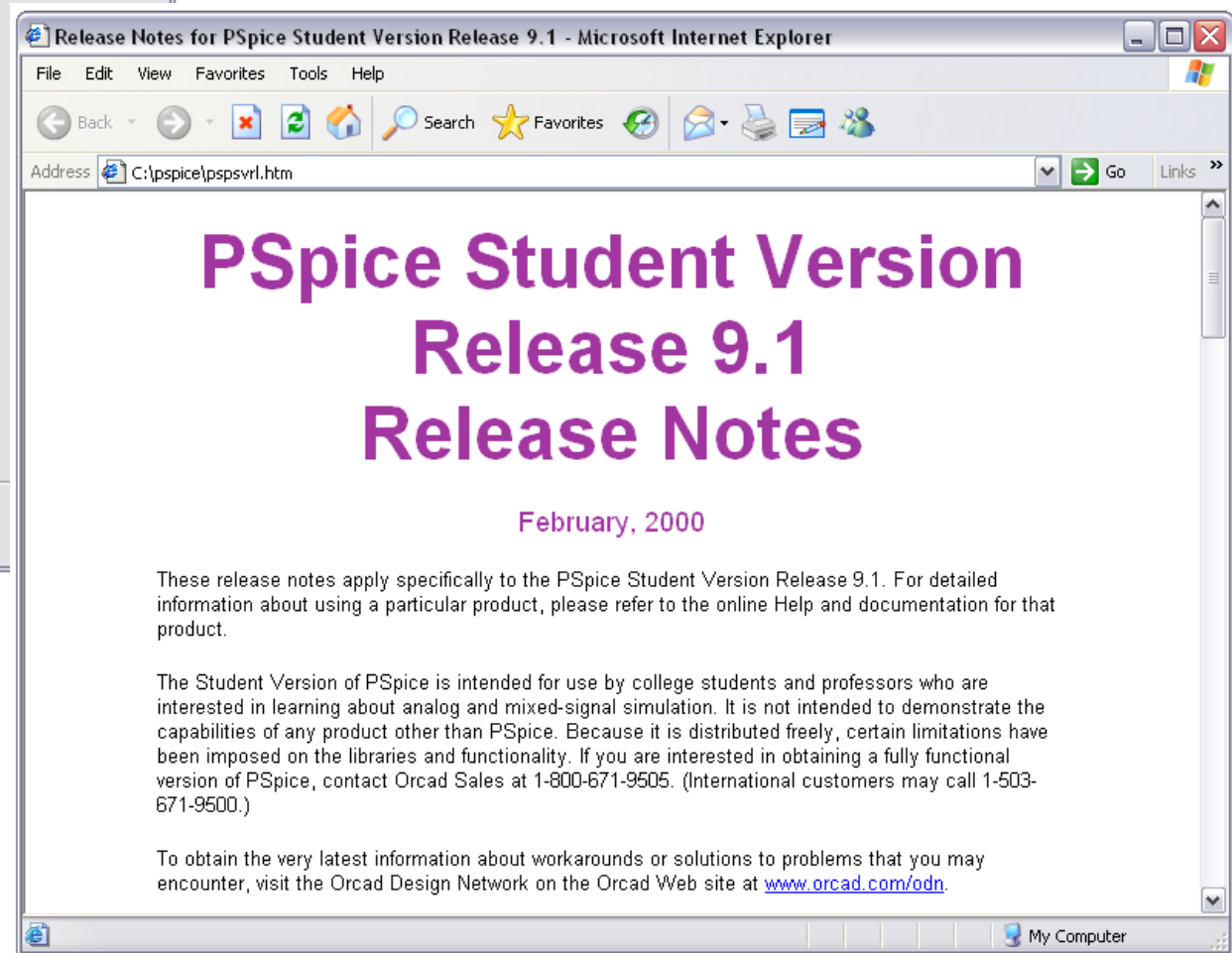
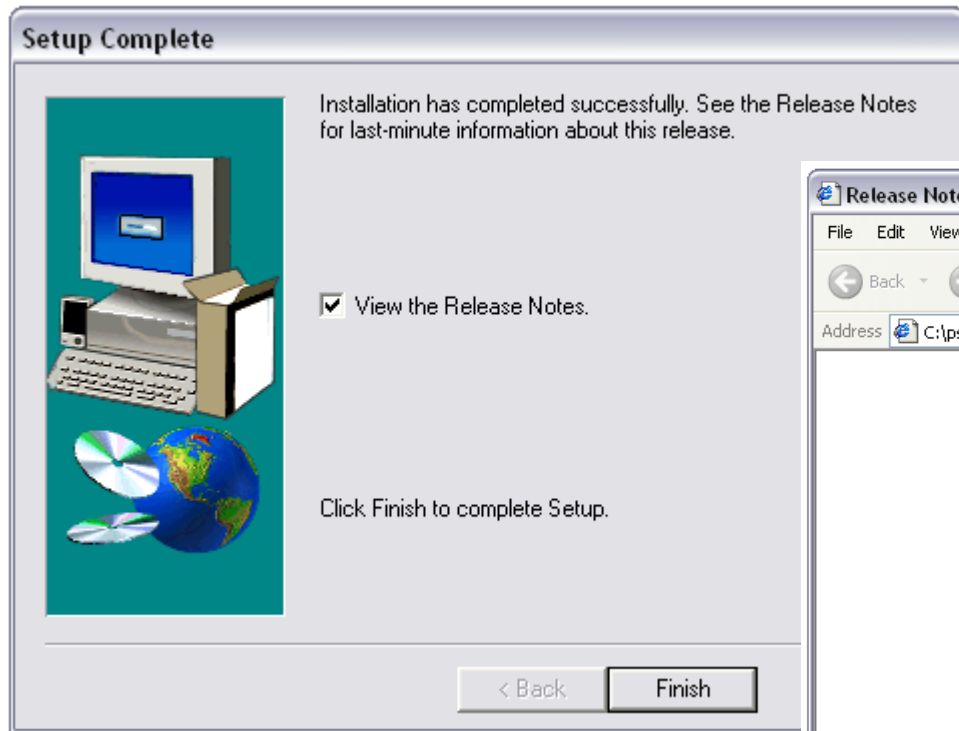


- when the extraction process has finished launch the **Setup.exe** installation program in the temporary directory
- choose **Capture** as schematic entry tool

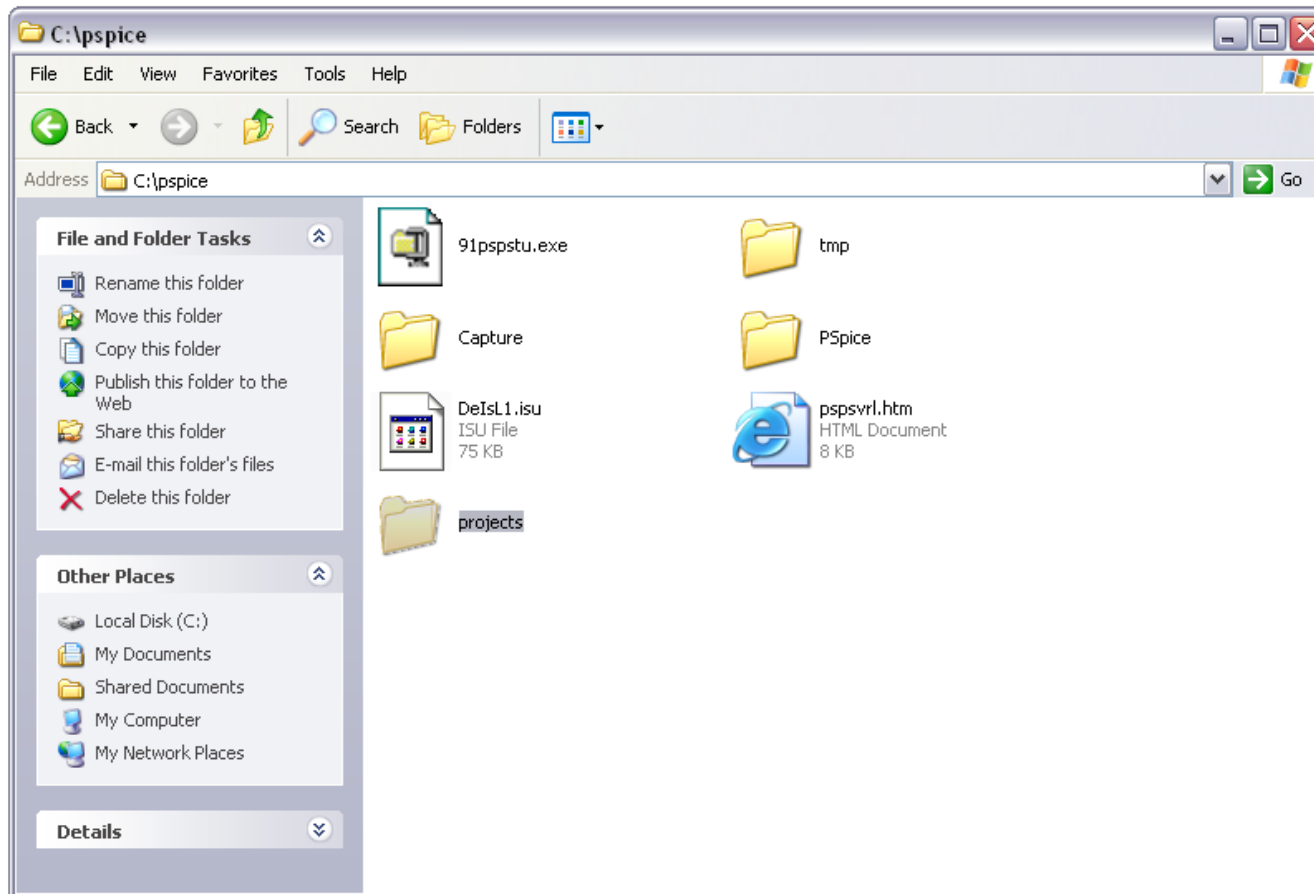
- change the default installation directory path into `C:\pspice`
- this is a safer choice because there are ***no blanks*** in the installation path !







*If you want to learn more about this student version of PSpice (e.g. limits in the number of components) read the **Release Notes***



- at the end of the installation process delete the 91pspstu.exe file and the temporary directory
- create a further C:\pspice\projects directory that will contain all your PSPice projects