Development of timing sensors and Front-End electronics for CMS TOTEM-Precision Proton Spectrometer

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PhD School in Physics and Astrophysics - XXX Cycle 2nd year seminar

Outline

Introduction

- Timing for CT-PPS
- Timing with silicon detectors
- Ultra Fast Silicon Detectors

Front-End electronics for UFSD

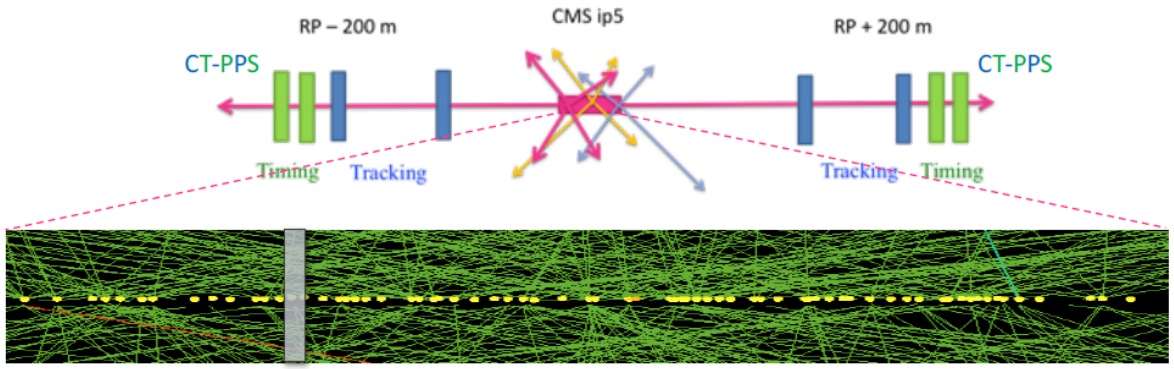
- TOFFEE

Sensor development

- FBK 275 um UFSD
- FBK 50 um UFSD

Timing for CT-PPS

The CMS TOTEM Precision Proton Spectrometer is a 2-arm forward spectrometer located at 200 m from the main interaction point of the CMS experiment at CERN



In the High Luminosity - LHC environment the reconstruction of the time information will be a fundamental tool due to pile-up of events (~ 150-200 /bunch crossing, ~ 150 ps RMS time between vertexes)

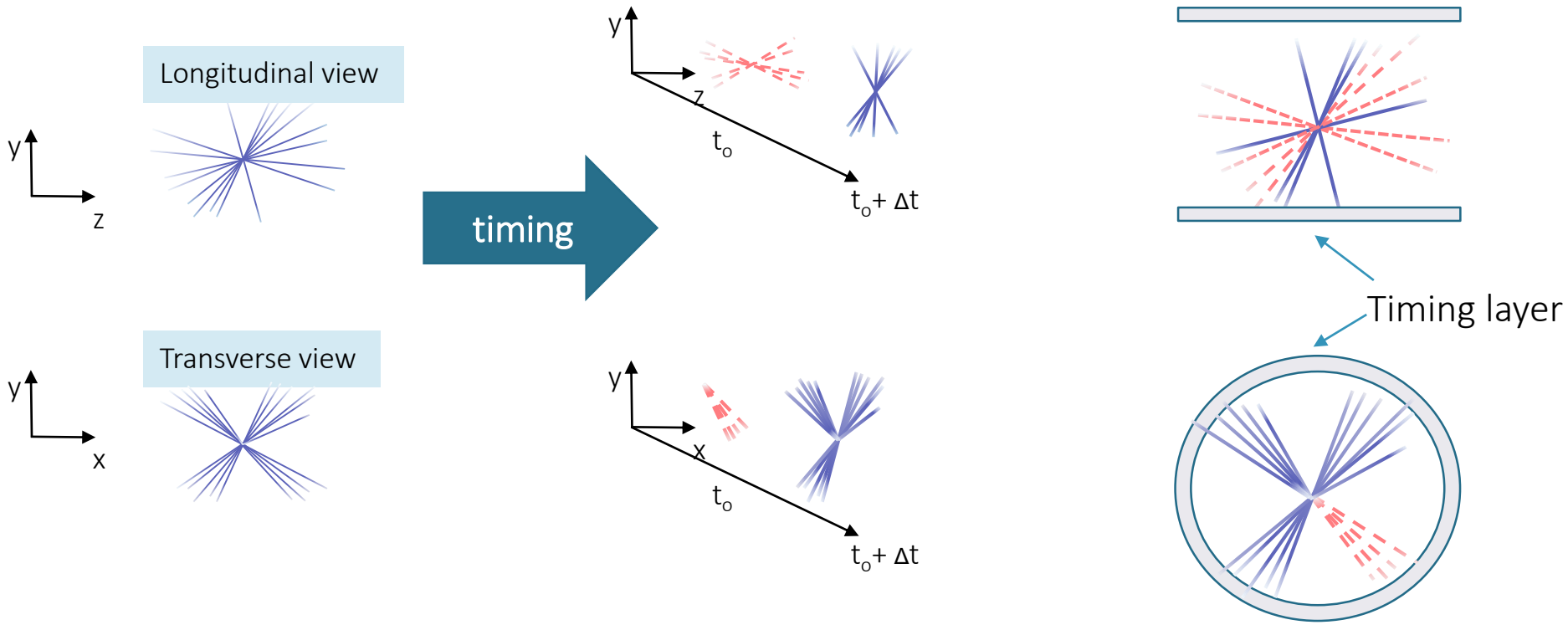
The reconstruction of time information allows to **distinguish different overlapping events**

The «z by timing» coordinate will be calculated according to $\Delta z = c\,\Delta(t_1-t_2)/2$

➡ **We plan to reconstruct the time information with σ_t ~20 ps**
i.e. z position with an accuracy of ~ 4 mm

Timing in event reconstruction

Timing allows to resolve different events otherwise undistinguishable by adding an extra dimension



Time resolution

In a sensor + readout system the time is set when the signal crosses the comparator threshold

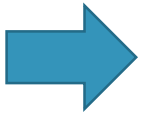
The timing capabilities are determined by the characteristics of the signal at the output of the preamplifier and by the TDC binning.

$$\sigma_t^2 = \left(\frac{N}{\frac{dV}{dt}}\right)^2 + \left(\frac{\delta_{Bin}}{\sqrt{12}}\right)^2 + \sigma^2_{Time\ Walk}$$

Noise and steepness of the signal

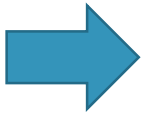
TDC contribution

Sensor signal shape variations due to non homogeneous energy deposition (Landau fluctuations)



Required:

- Noise minimization
- Large and uniform signals
- Short rise time



FAST SENSOR + FAST READOUT

Timing with silicon detectors (I)

- Standard silicon detectors can be used in timing applications with an appropriate geometry
- Silicon detectors benefits include low material budget, low cost, good radiation tolerance, easy electrodes segmentation
- Currently, the GiGaTracker of the NA62 experiment employs a track-timing detector having a time resolution of $\sigma_t \sim$ 150 ps
- Standard silicon sensors can achieve good time resolutions. However, it is difficult to reach resolutions better than $\sigma_t \sim$ 80–100 ps given their small signal.
- The aim is to design a silicon detector for timing, with signals $\sim$ 10 times higher than a standard one

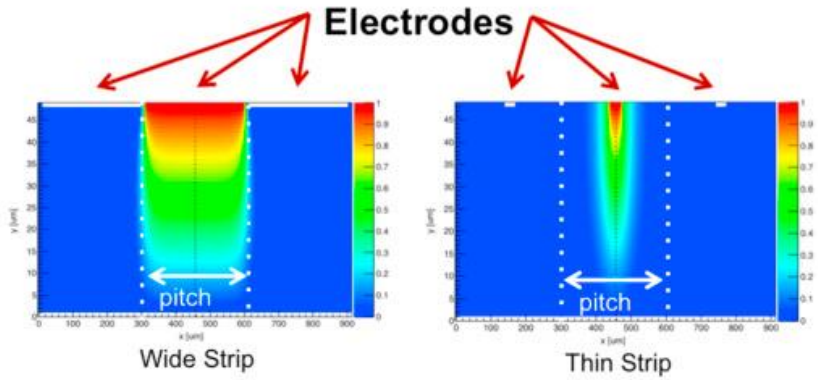
Timing with silicon detectors (II)

- A Minimum Ionizing Particle (MIP) in a standard silicon detector produces ~ 80 e-h pairs/um
- The signal of a silicon detector is produced by charge carriers drifting through the bulk and is defined as the induced current on the electrodes
- The instant induced current on a single electrode is modeled by **Shockley-Ramo's theorem**

$$I_i \propto q\, v\, E_w$$

drift velocity — Weighting field

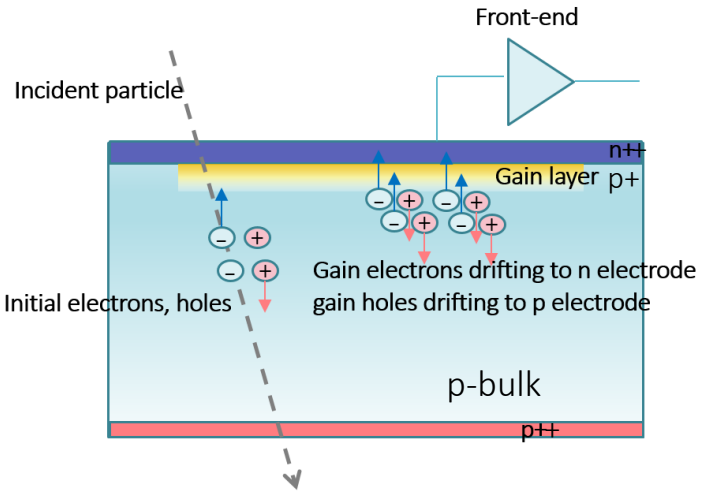
- The key for good timing is the uniformity of the signals
  → drift velocity and weighting field need to be as uniform as possible
  → parallel plate geometry: **strip implant ~ strip pitch ≫ thickness**

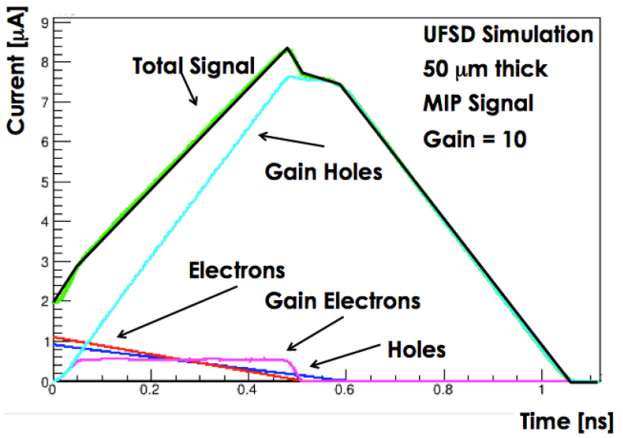


- By **reducing the sensor thickness** it is possible to reduce the drift time (shorter signal), but the number of charge carriers is not high enough to have a good slew rate dV/dt
  → **use avalanche multiplication to increase the signal amplitude**

Ultra Fast Silicon Detectors

- UFSD have been designed to minimise the $N/\frac{dV}{dt}$ term
- They have a particular signal shape due to **charge multiplication**
- To achieve charge multiplication **ΔE= 300 kV/cm** is necessary
  → possible by adding a p doping layer internal to the sensor: gain layer
- Electrons multiply when crossing the gain layer generating **additional electrons and holes** (electrons have higher ionization coefficient than holes)
- The main part of the signal is **produced by gain holes** drifting to p electrode
- UFSD have **low gain** (~ 10): low shot noise, milder electric fields, possible electrode segmentation, behavior similar to standard silicon detectors
- Currently produced by CNM (Barcelona) and FBK (Trento)





UFSD – slew rate and thickness

The shape of the signal depends on the sensor thickness:

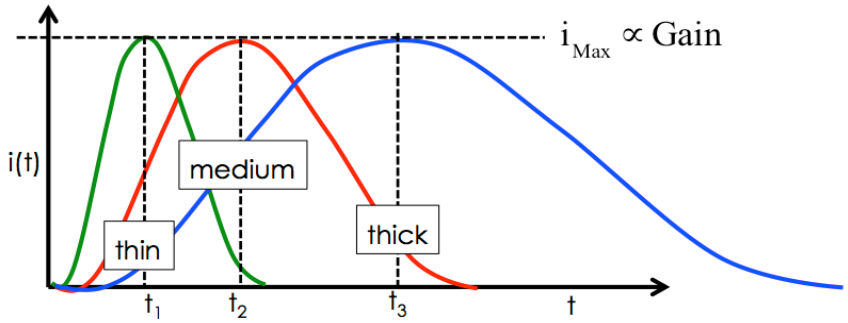
- **Amplitude** depends on the **gain value**
- **Length** depends on sensor **thickness**

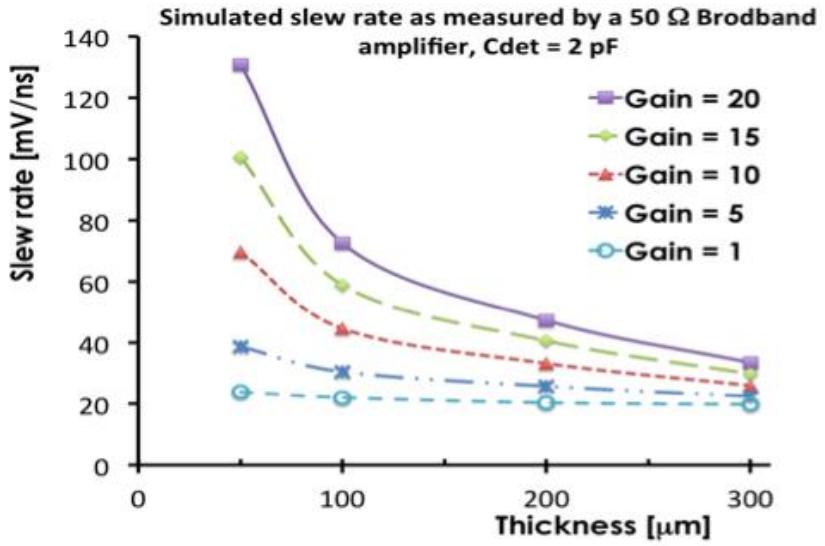
For a fixed gain:

- Amplitude = constant
- Rise time decreases ~ **1/thickness**

Slew rate:

- Increases with gain
- Increases ~ **1/thickness**

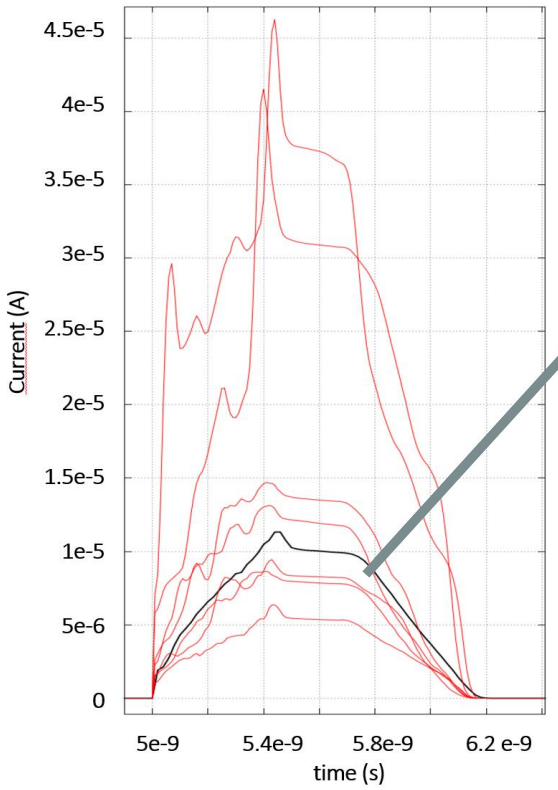


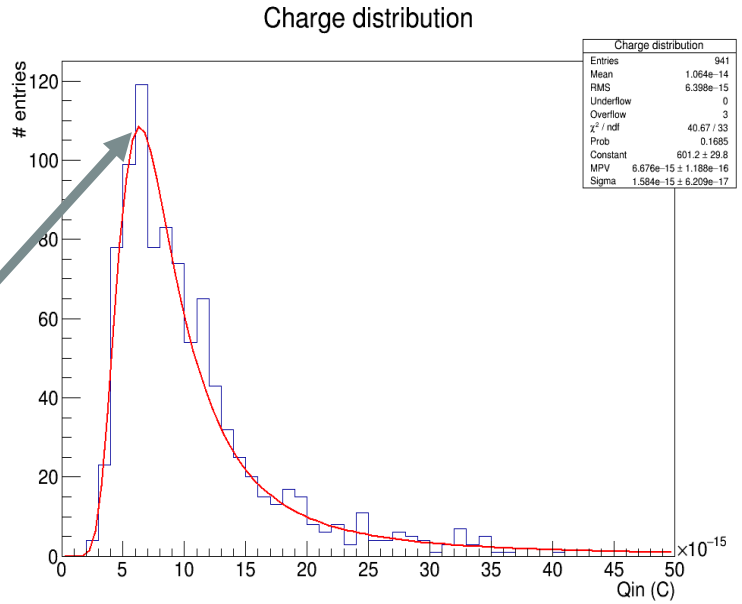


The key for a fast sensor is then:

- thin bulk
- charge multiplication

50 um UFSD signals



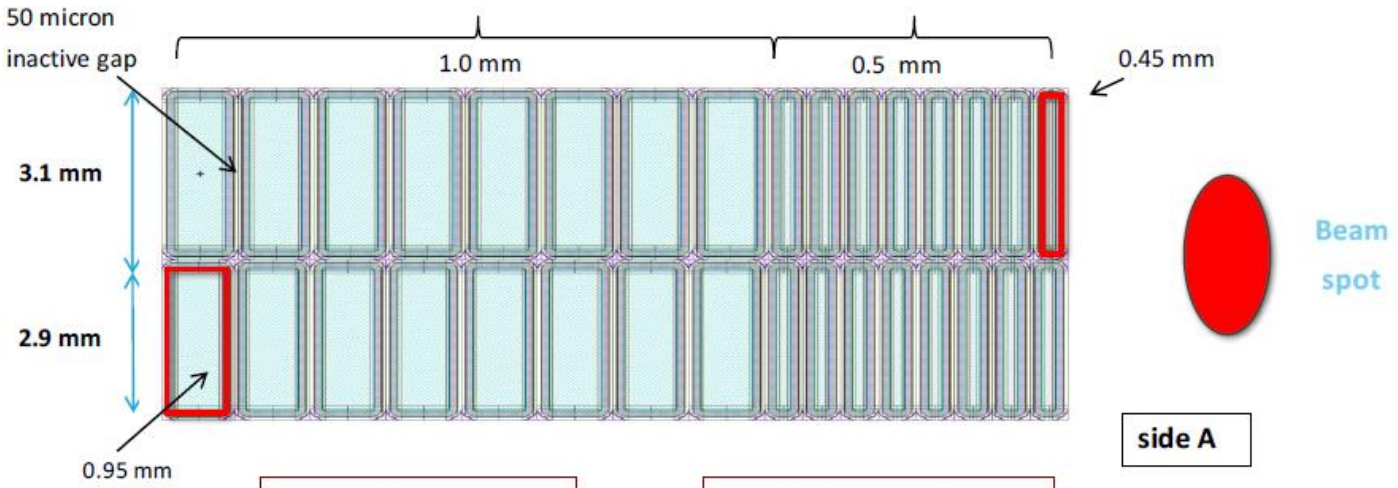


Typical 50 um, gain 15 UFSD MIP signal
charge ~ 8 fC
signal length ~ 1.2 ns

UFSD are fast sensors providing steep signals

→ a fast readout electronics is needed to reach the best time resolution

UFSD geometry for CT-PPS (CNM production)



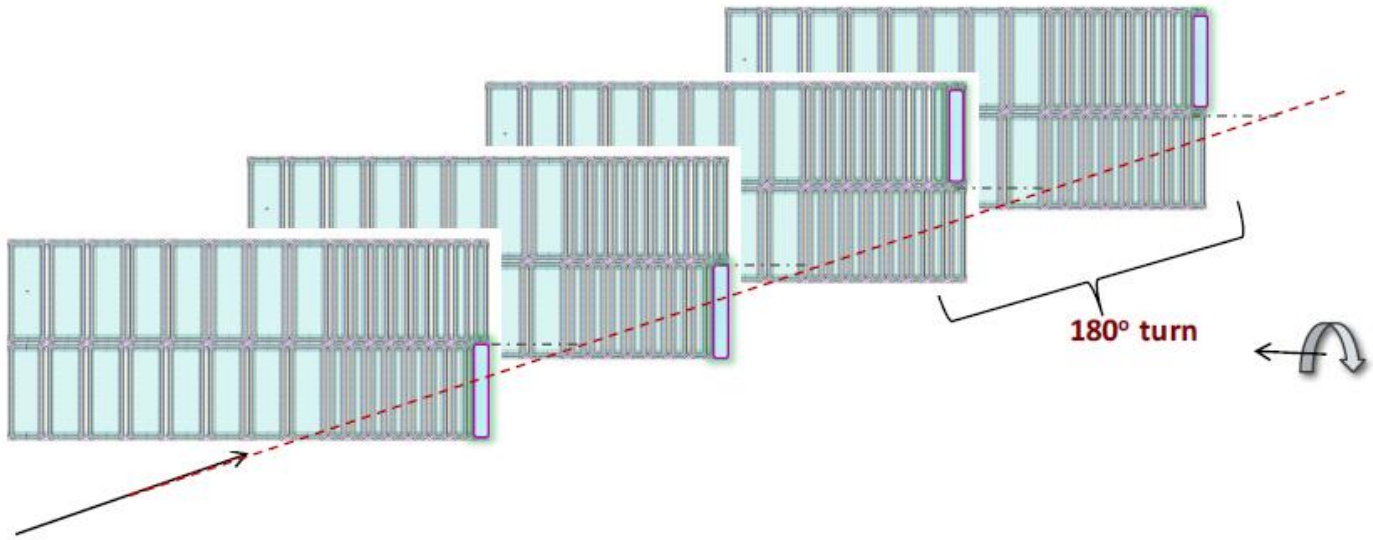
Asymmetric design
Area = 12mm x 6mm
Thickness = 50 um
# of channels = 32 Gain ~ 15
Slim edge of ~200 µm on side A

Expected time resolution: ~30 ps

The signal from each pad will be detected by a **DC-coupled front-end** mounted close to the detector module inside PPS roman pot (RP)

Layout of detector planes

4 (6) planes per station (qualitative sketch):



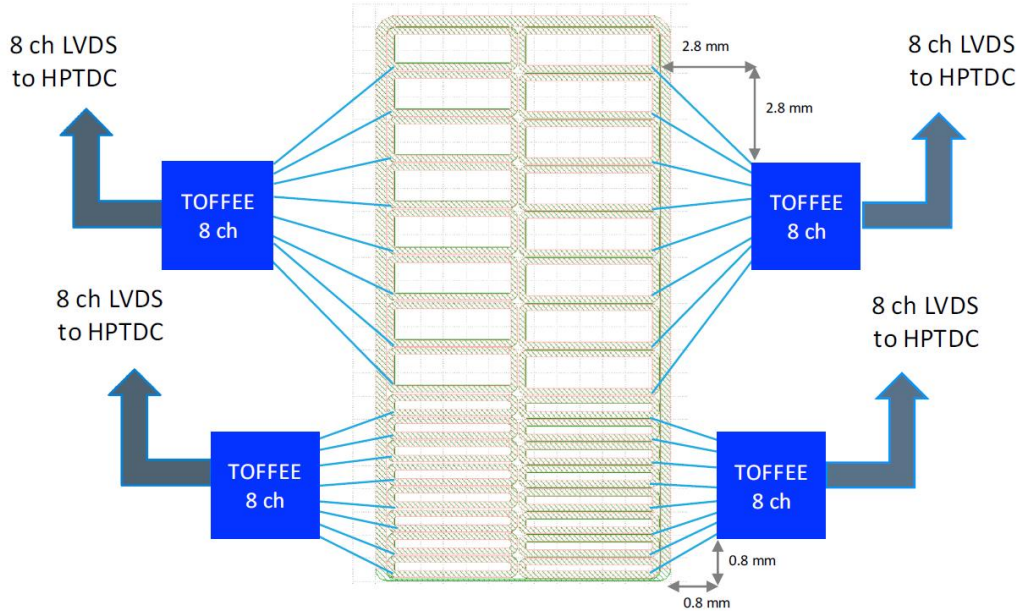
No cracks aligned:
2 (3) planes facing the beam
2 (3) turned by 180°

TOFFEE - overview

TOFFEE (Time Of Flight Front End Electronics) is designed in UMC 110 nm CMOS technology in collaboration with LIP (Lisbon)

The ASIC has 8 channels, each channel consists of:

- Trans-Impedance Amplifier
- Single threshold discriminator
- Delay line to stretch discriminator output: High Precision TDC (HPTDC) reads pulses wider than 5ns
- LVDS driver for HPTDC interfacing



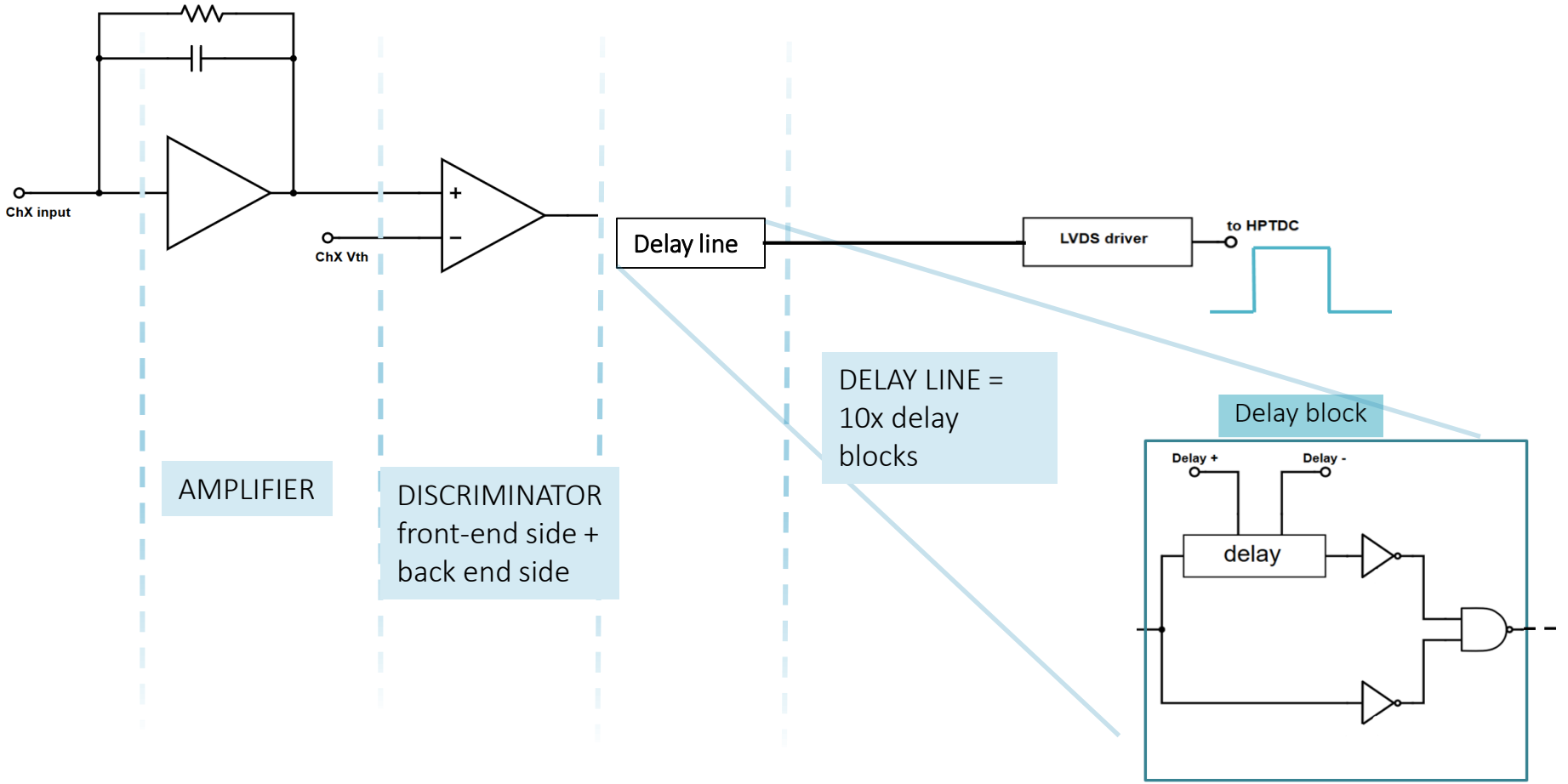
It is optimized for a sensor capacitance of 5-10 pF and an input charge between 3 fC and 30 fC

The output is sent out of the roman pot to the existing HPTDC board through LVDS links (32 pairs per detector module)

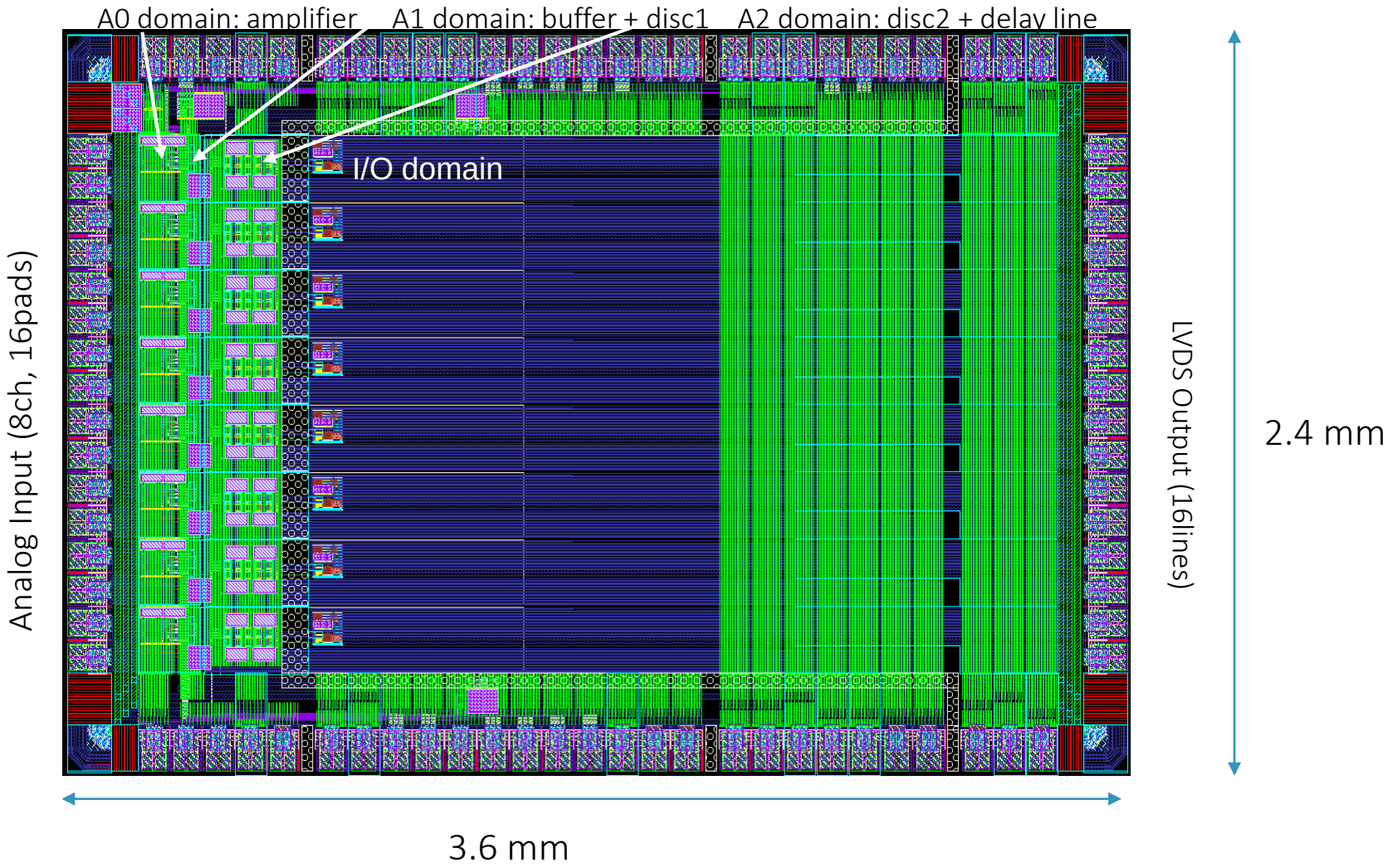
To read out a CT-PPS UFSD minimizing wire-bond length → 4 TOFFEEs

The chip has been submitted to foundry in May 2016, tests started in October 2016

TOFFEE – signal processing chain



TOFFEE – layout



TOFFEE – specifications

Linear dynamic range: 3fC -30fC

Preamplifier gain: ~ 7 mV/fC

GBW: 14 GHz

RMS noise at Cdet= 6 pF: 800 uV

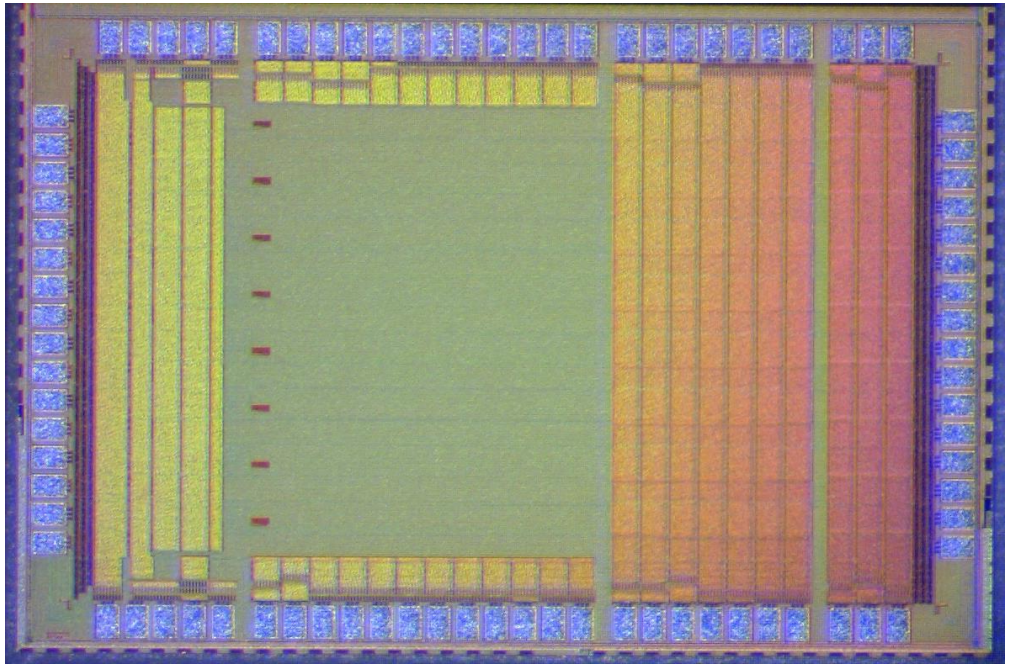
Discriminator output width: 2 – 14 ns

Delay line: adding 5 ns offset to discriminator signal width

Power consumption: 18mW per channel

AVDD: 1.2V

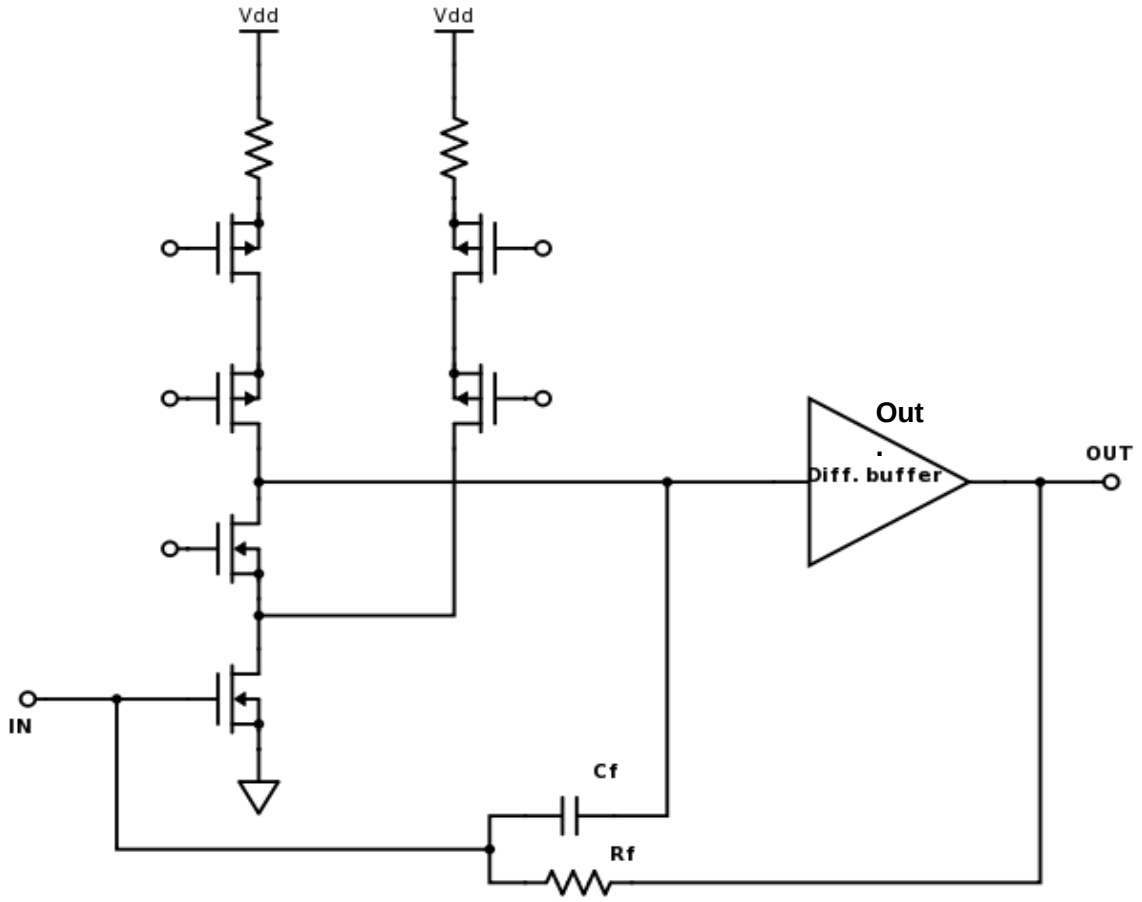
DVDD IO: 2.5V



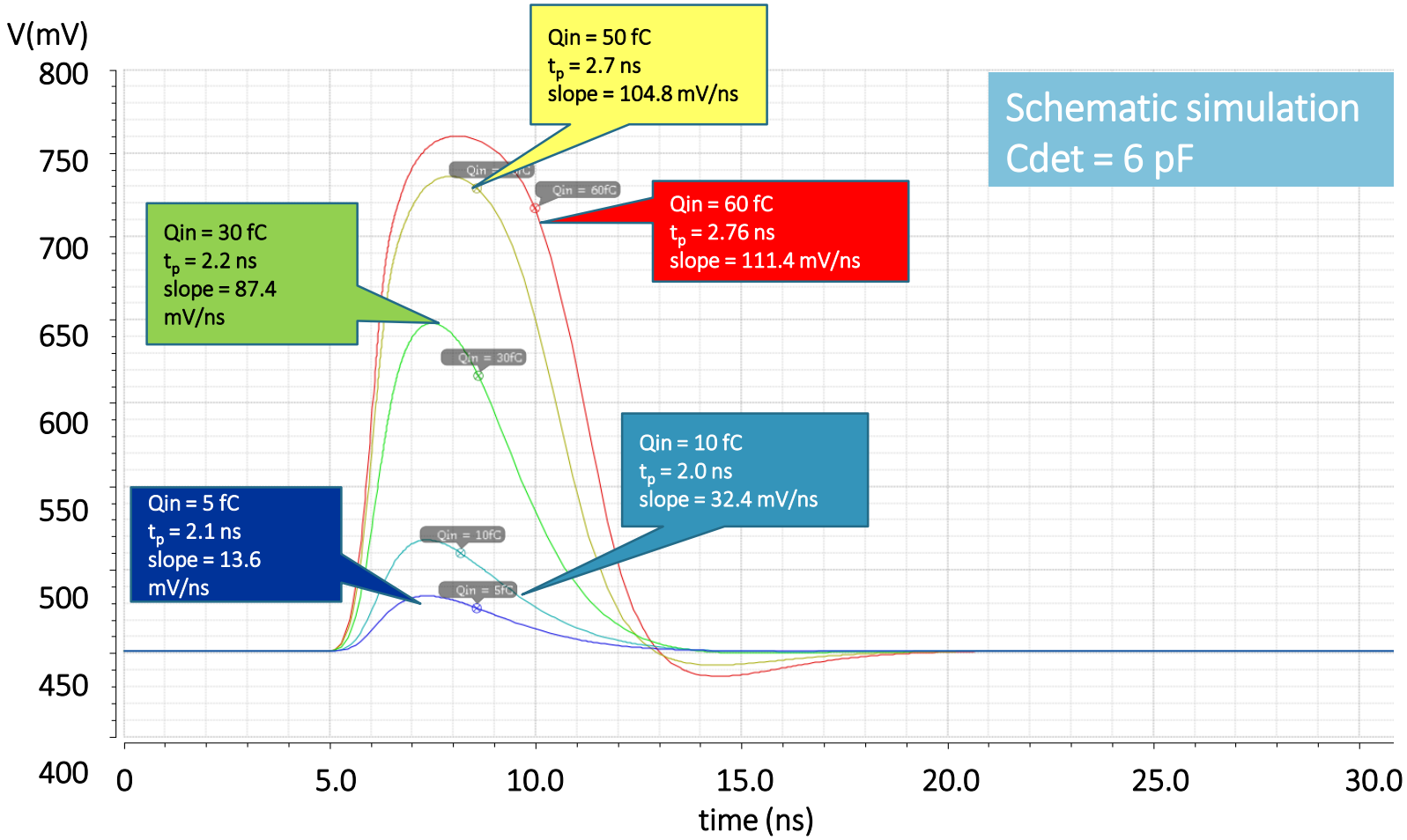
Expected dose at CT-PPS roman pot: NIEL ~ 7 *10^{14} n_{eq}/cm^2 , TID ~ 80 Mrad

Preamplifier architecture

- Cascode amplifier with split current sources
- Right branch injects high current in the input transistor
- Resistors for noise shielding
- Output buffer for load driving



Preamplifier signal (I)



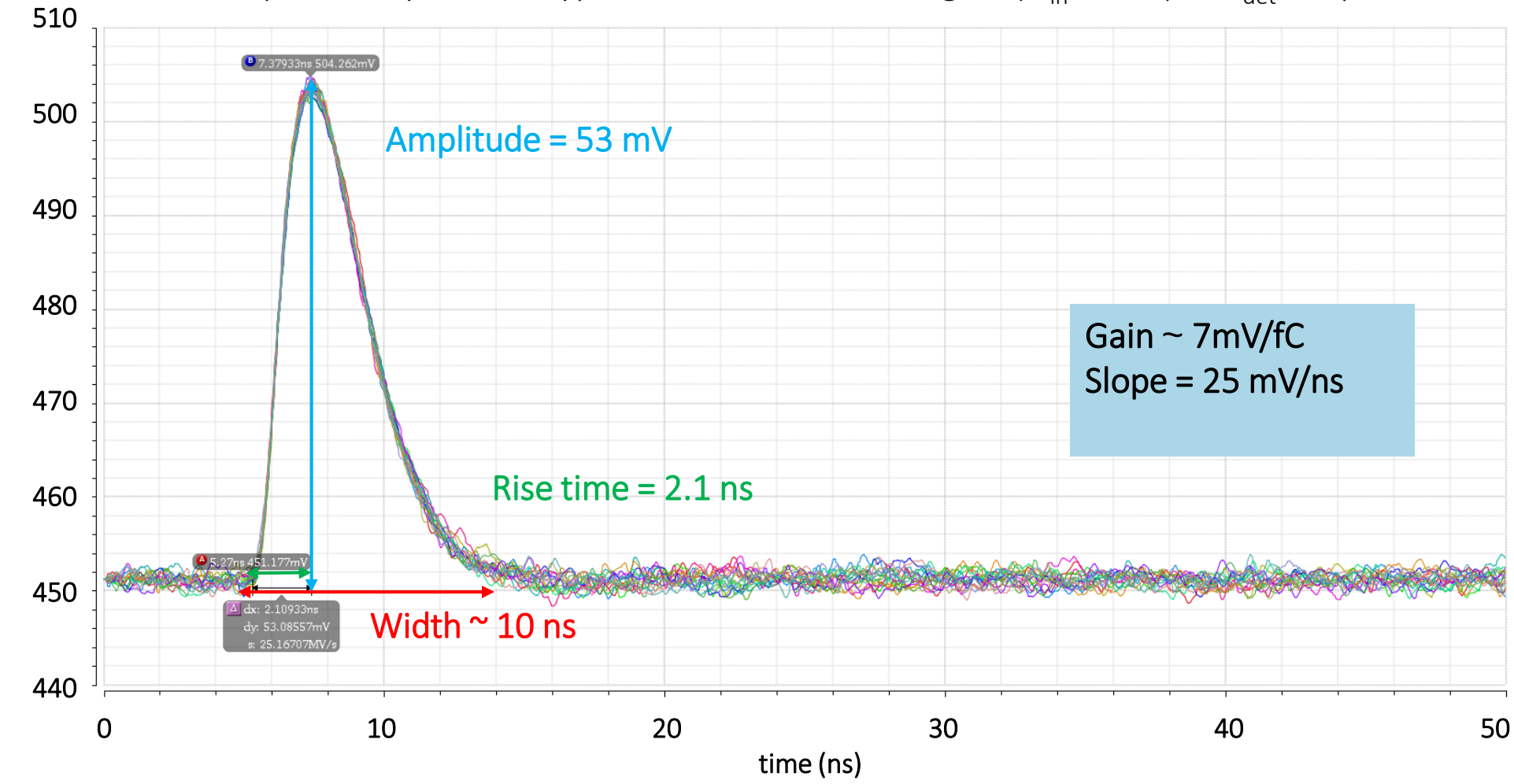
The preamplifier signal has

- **fast rise time**: ~ 2 ns schematic, < 3 ns postlayout
- **high slope**

Requires high GBW amplifier (main power contribution)

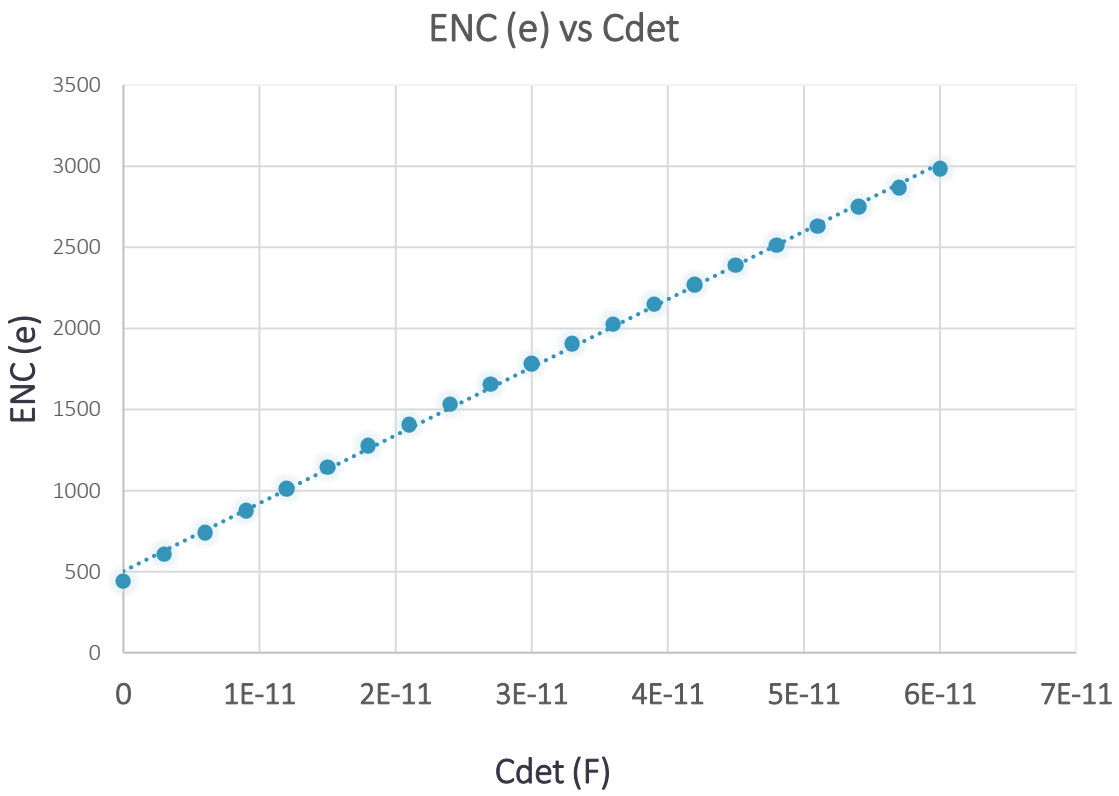
Preamplifier signal (II)

Preamplifier response to typical 50 um UFSD MIP signal (Q_{in} = 8 fC) at C_{det} = 6 pF. Transient noise simulation

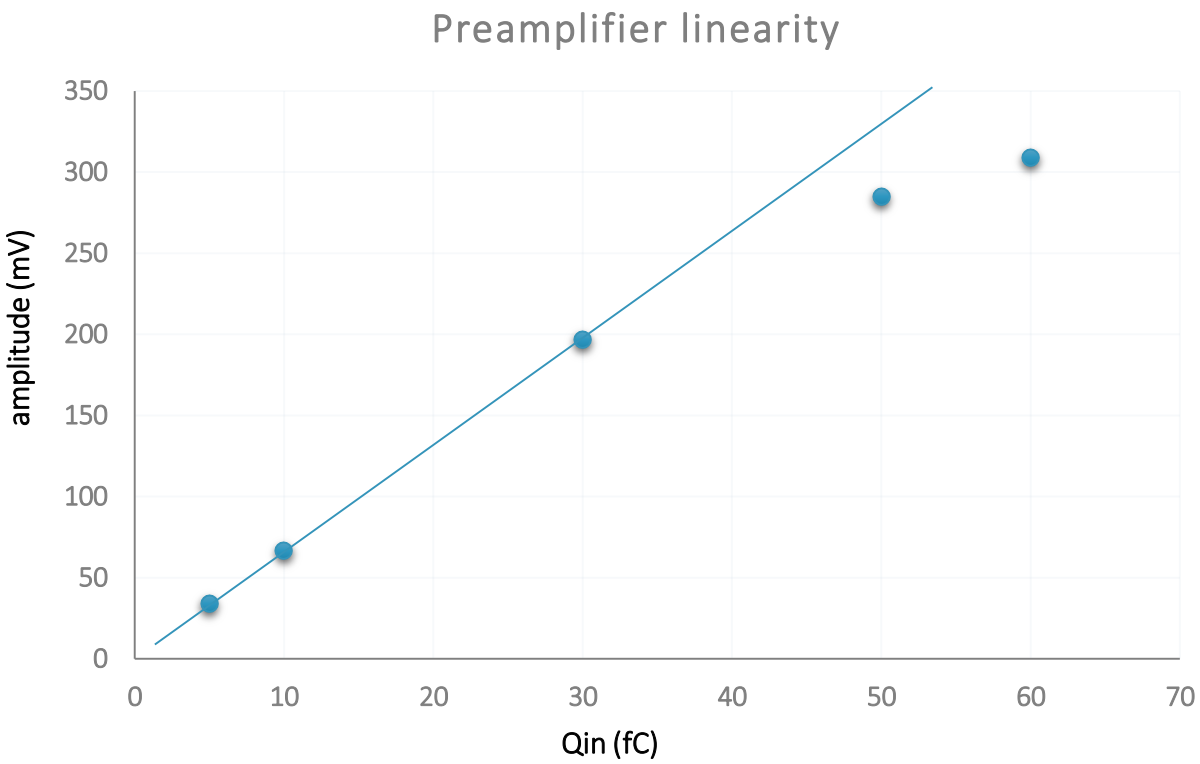


Preamp noise curve and linearity

Simulated amplifier output noise as a function of detector capacitance



Preamplifier gain linearity as a function of input charge



TOFFEE – simulated time resolution

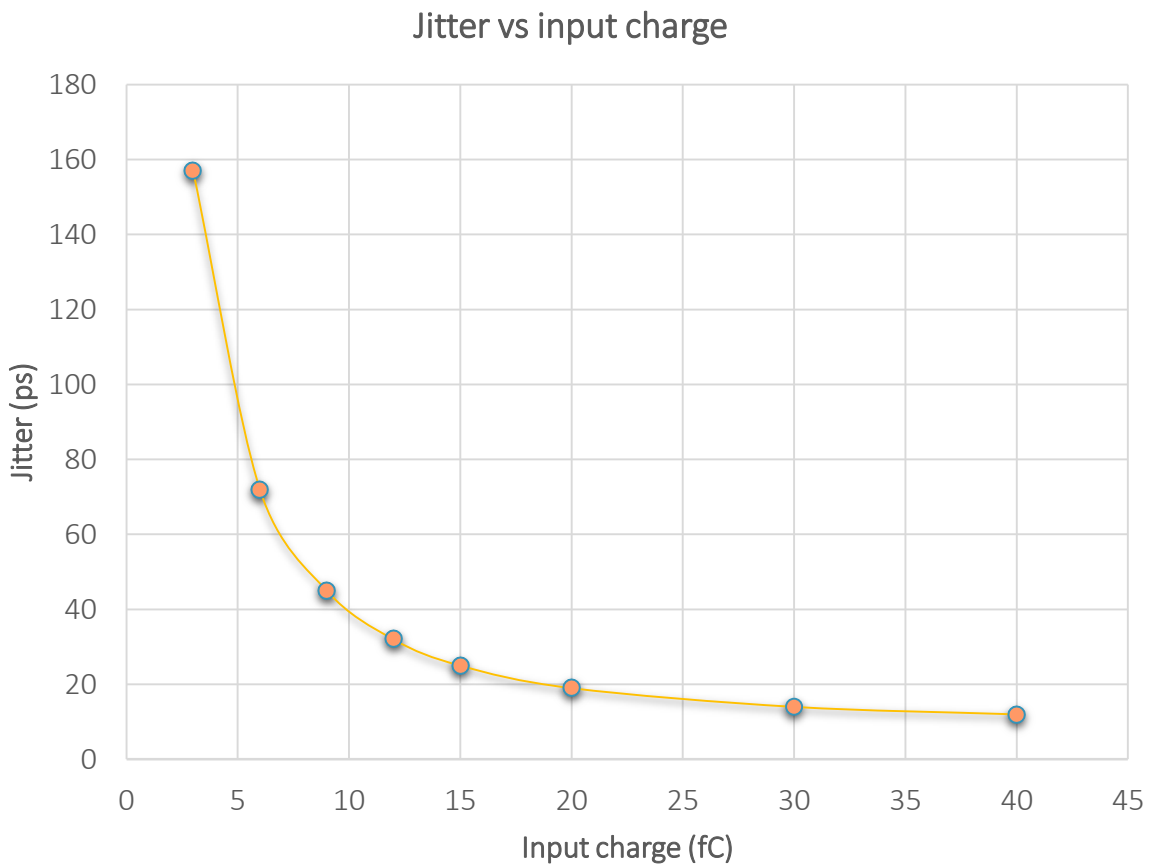
Jitter estimation as a function of input charge from post layout simulations

A time resolution of **~ 45 ps** is expected for 1 **single detector + readout module** for a MIP signal (~ 8 fC)

Time resolution can be further improved by putting more planes in parallel, e.g. for 4 planes

$$\sigma_t = \frac{jitter}{\sqrt{N\ planes}}$$

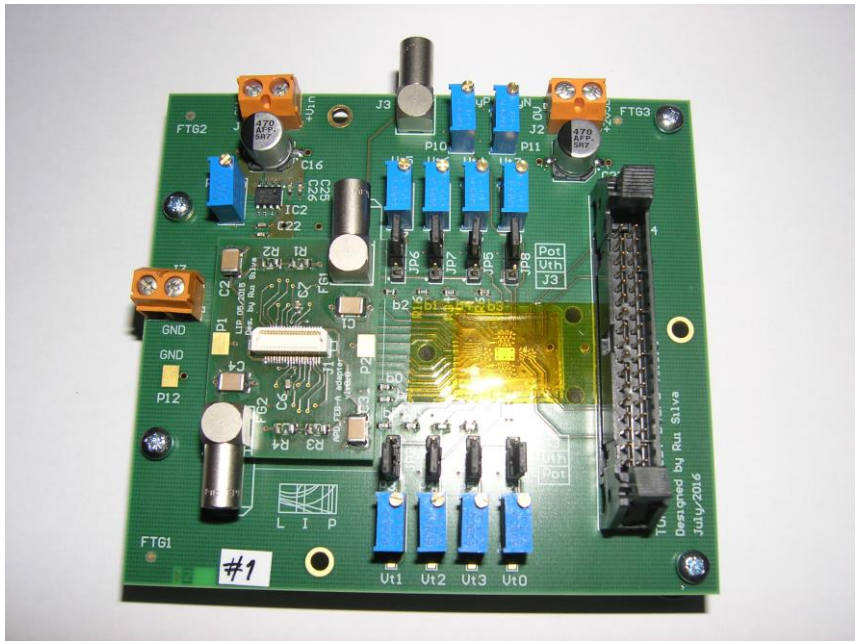
~ 22 ps



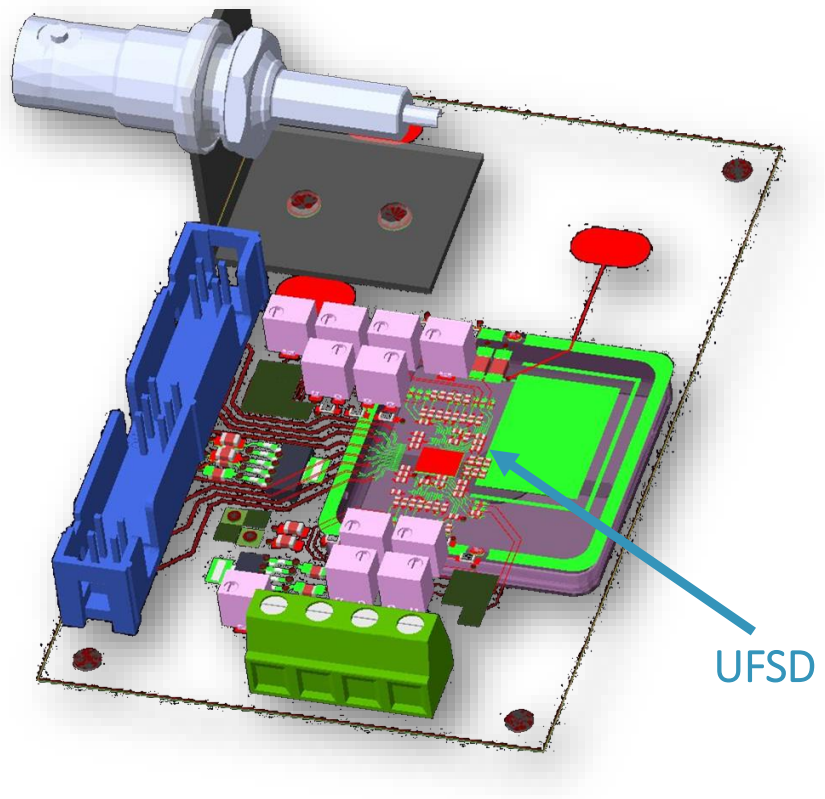
TOFFEE test boards

TOFFEE tests started in October. Two dedicated boards have been designed:

- **LIP board** (by R. Silva): TOFFEE + RMD APDs → tested
- **Turin board** (by M. Mignone): TOFFEE + CT-PPS UFSD → available Dec. 2016

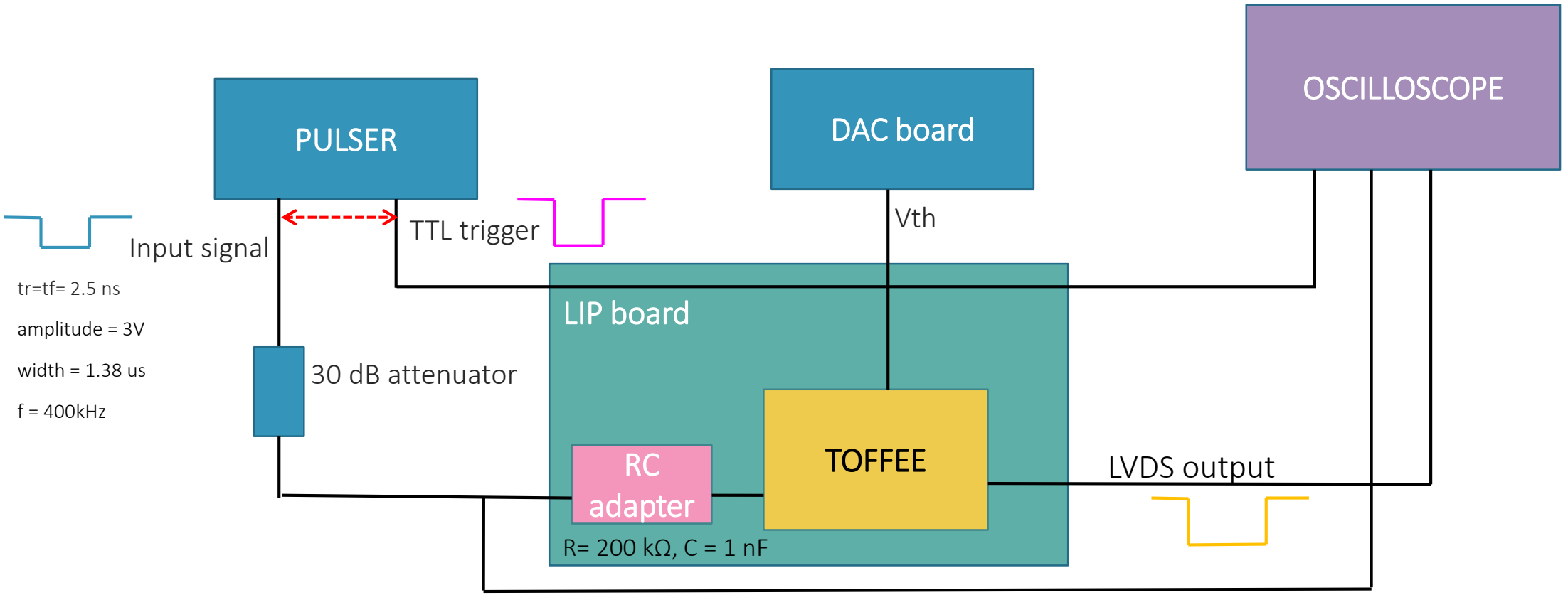


LIP board for TOFFEE + APD adapter



Turin board+ UFSD

Tests with external pulse - setup



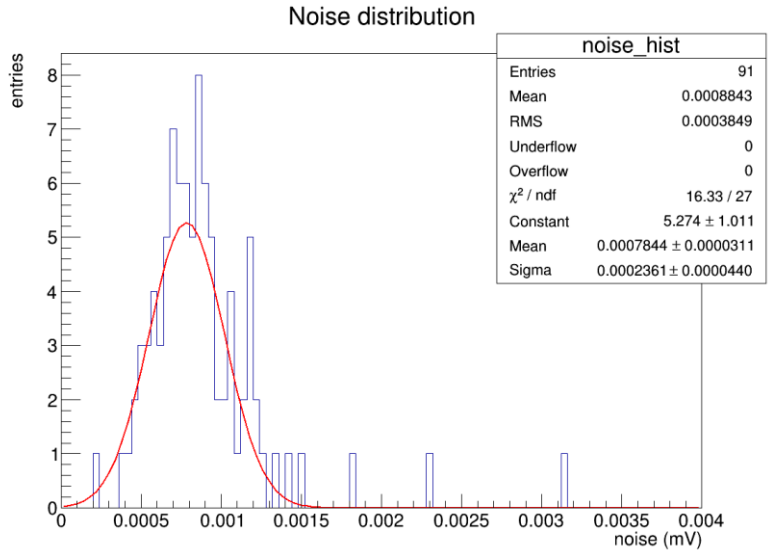
Tests with external pulse – threshold scan

- LVDS output is read by a differential probe connected to oscilloscope
- The time of arrival of the LVDS output with respect to test pulse is measured
- By scanning the threshold voltage it is possible to track the shape and amplitude of the signal at the preamplifier output and
- The amplitude is determined as the threshold voltage value at which the discriminator does not trigger anymore
- Measured signal slew rate dV/dt

$$SR = \frac{V_{th2} - V_{th1}}{mean_2 - mean_1} = 28.6 \text{ mV/ns}$$

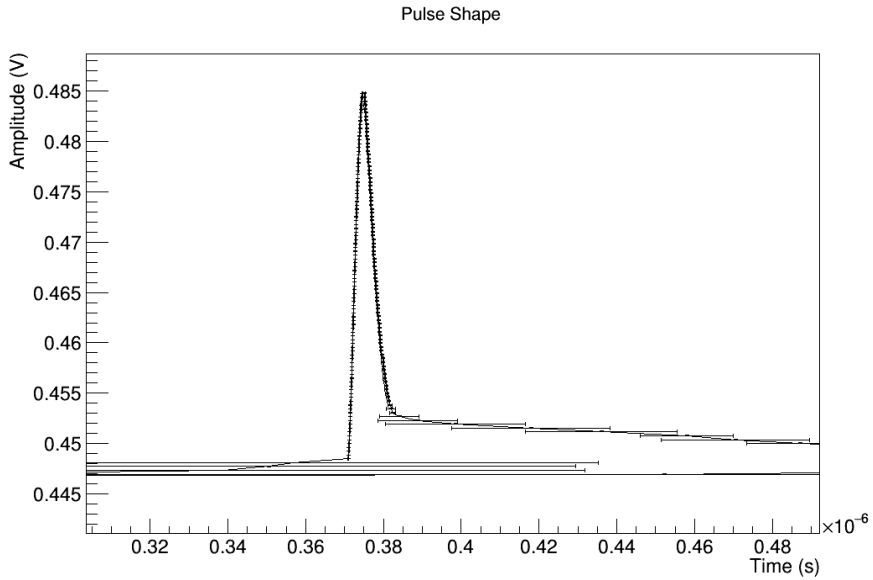
- Measured TOFFEE + pulser jitter σ = 38 ps
- Evaluated noise $Noise = SR \cdot \sigma$ = 0.80 mV

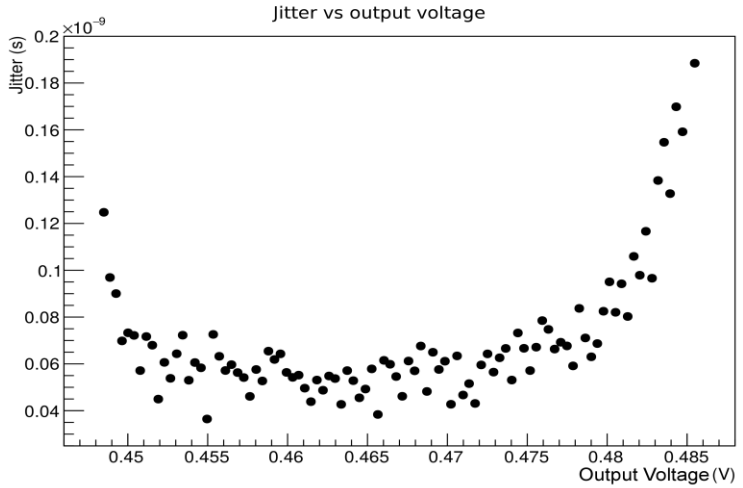
All values are consistent with simulations



Tests with external pulse – signal reconstruction

- Preamplifier signal pulse shape has been reconstructed from the analysis of ToA (Time of Arrival) and ToT (Time over Threshold)
- A positive pulse is sent to TOFFEE input through 30 dB attenuator and RC filter (R= 200 kΩ, C= 1 pF)
- pulse amplitude = 1.2 V, width = 1 us, frequency = 100 kHz, $t_r = t_f$ = 2.5 ns → total charge ~ 40 fC
- ToA = delay time between trigger signal and LVDS switching
- ToT = width of first detected LVDS pulse in the oscilloscope recording window
- Through threshold scan it is possible to track the pulse shape and the time resolution of rising and falling edges
- Jitter is evaluated from ToA distribution σ



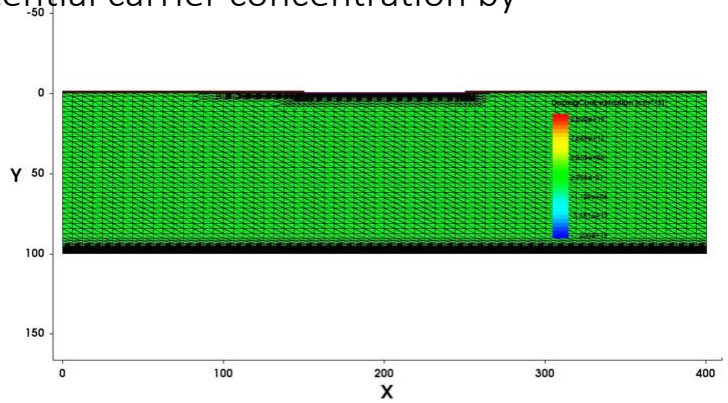


Sensors development

- UFSD design is also conducted by Fondazione Bruno Kessler (FBK) and Trento University
- INFN Torino's collaboration with FBK and Trento University started in 2014
- I am contributing to UFSD development performing **sensor simulations**
- Simulations are carried out with the TCAD software **Synopsys Sentaurus**, incorporating FBK technology parameters.
- TCAD solves **Poisson and Continuity equations** numerically and extracts the Electrostatic potential carrier concentration by discretizing the device with a grid (mesh).

  → electrical simulations (leakage current, breakdown voltage)

  → dynamic simulations (charge collection and gain)



- Sensors from the first FBK UFSD production (completed March 2016) feature a 275 um bulk thickness
- Studies on 50 um thick structures performed, devices are ready to be processed

275 um production

Studies on 275 um thick sensors involved:

- Electrical simulations to predict the electrical characteristics of the devices (2D)

  → leakage current and breakdown voltage evaluation

- Dynamic simulations, optical/heavy ion (2D with cylindrical geometry)

  → Charge collection and signal shape evaluation

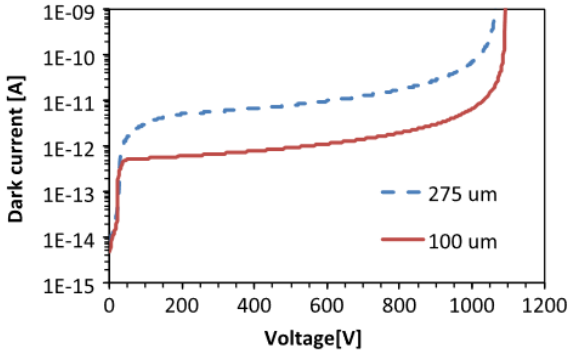
  → Gain behavior with bias voltage

  → Analysis on ndeep and pstop size (dead space between electrodes)

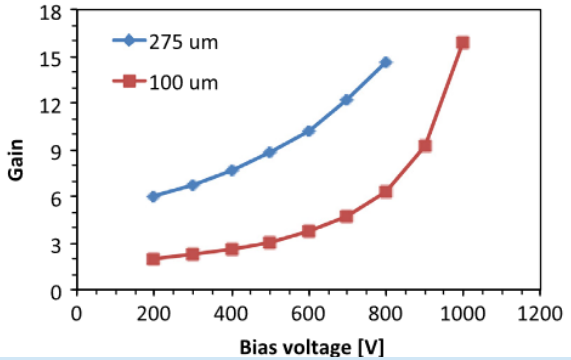
  → AC-coupled structure simulation: (AC pad size and signal study)

275 um simulations (I)

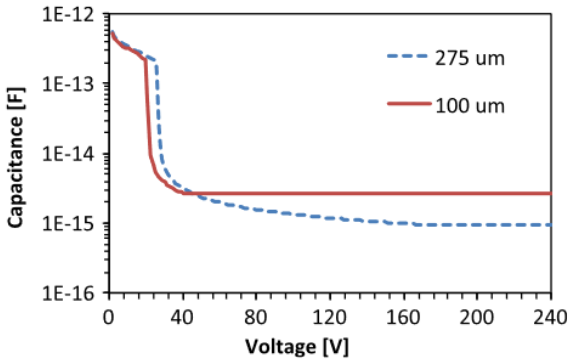
Electrical and dynamic simulations, 275 um bulk thickness compared with 100 um



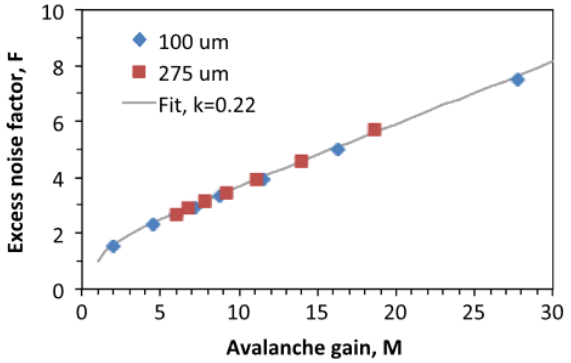
Leakage current as a function of bias voltage



Gain as a function of reverse voltage, response to a MIP



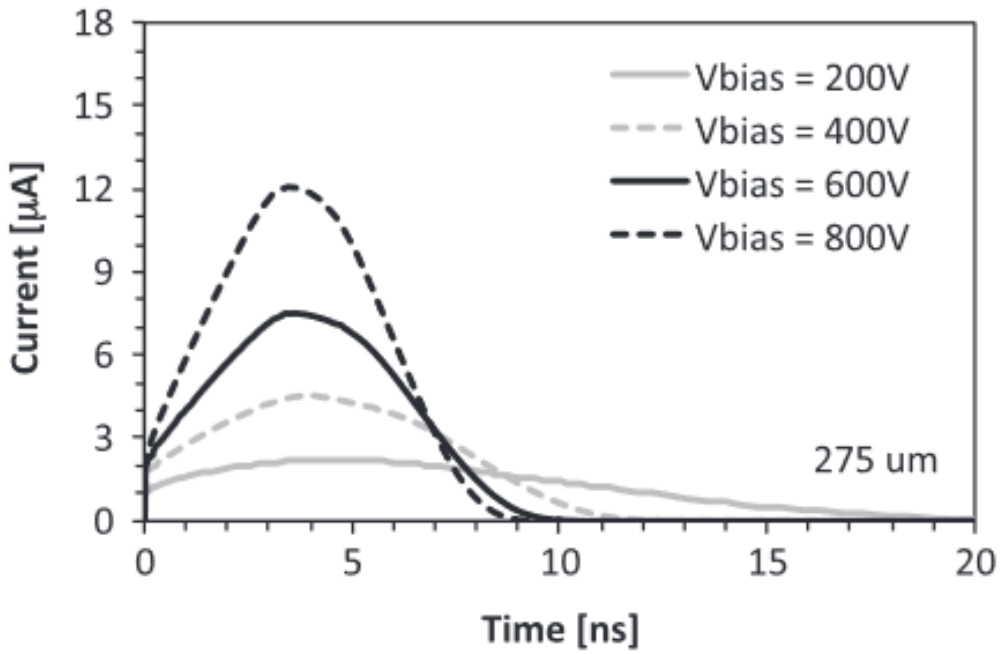
Capacitance as a function of bias voltage

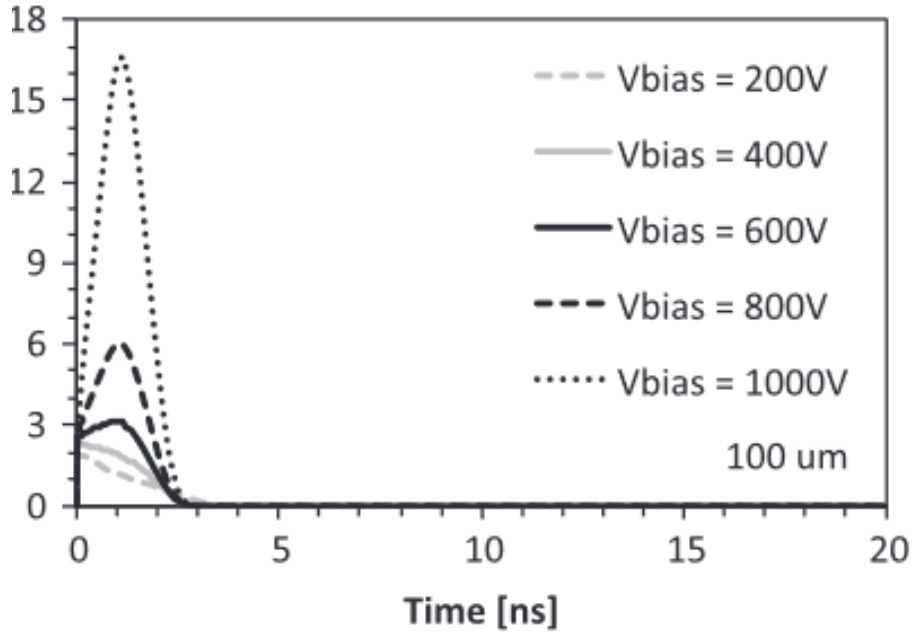


Excess noise factor as a function of gain calculated analytically according to $F = M \cdot k + \left(1 - \frac{1}{M}\right) \cdot (1 - k)$, k=0.22

275 um simulations (II)

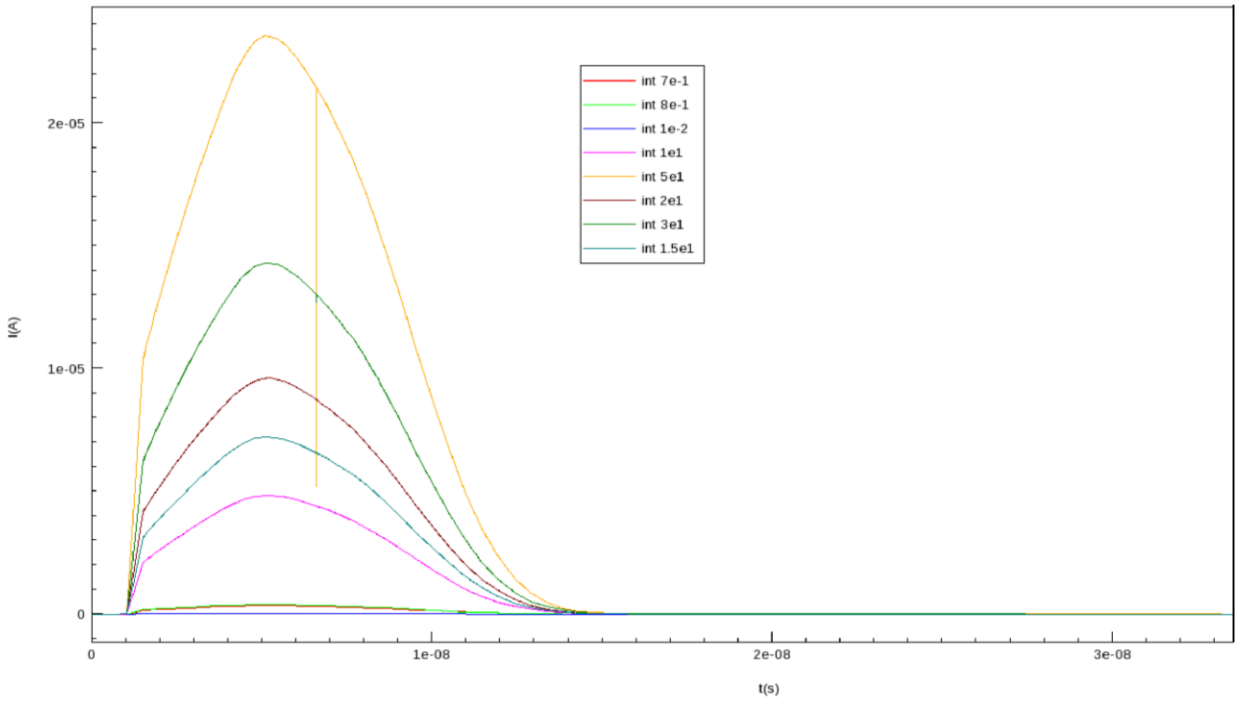
Current signals as a function of time at different voltages, 275 um and 100 um thick devices comparison



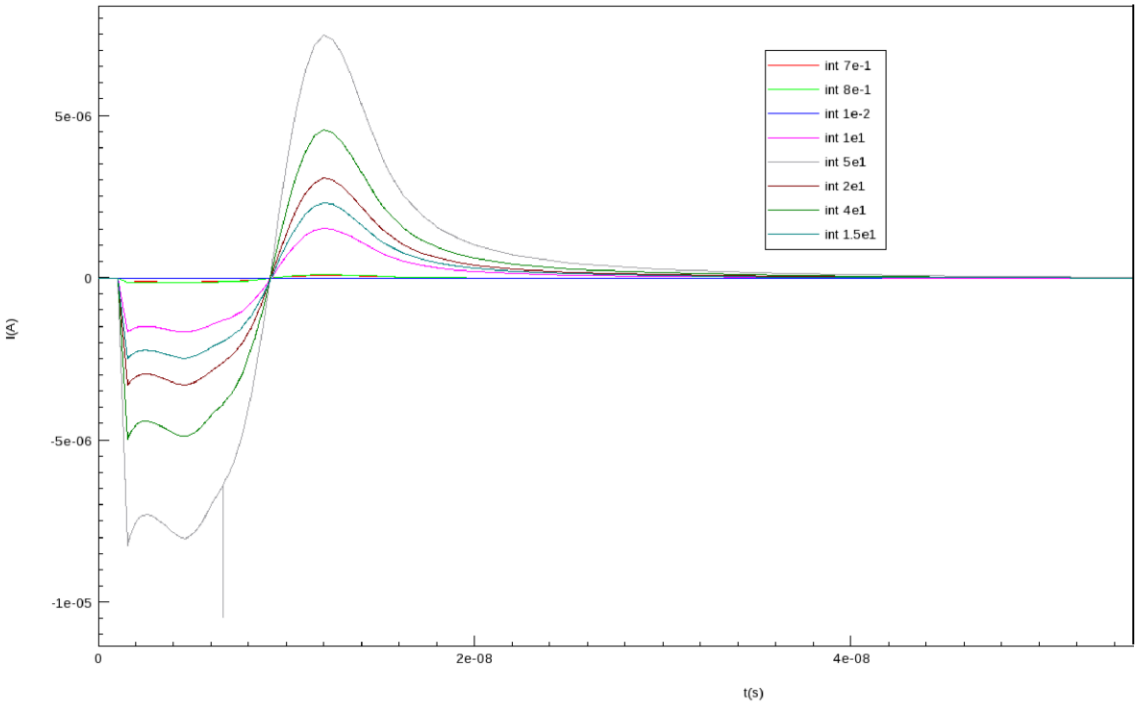


275 um simulations (III) – AC coupling

Current from pad hit by light → signal



Current from neighbouring pad → no resulting signal



50 um production

Studies on 50 um thick sensors:

- Tuning of gain layer doping for a reduced bulk thickness

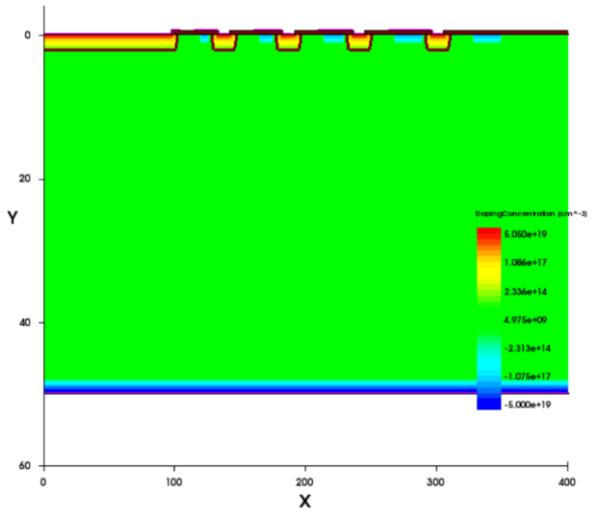
  → Gain curves and breakdown voltage evaluation

- Analysis on ndeep and pstop size for dead area minimization

  → Gain scan along x coordinate

- Low temperature simulations: analysis of gain behavior at various temperatures using different avalanche models implemented in Sentaurus (Van Overstraeten/ De Man, Okuto)

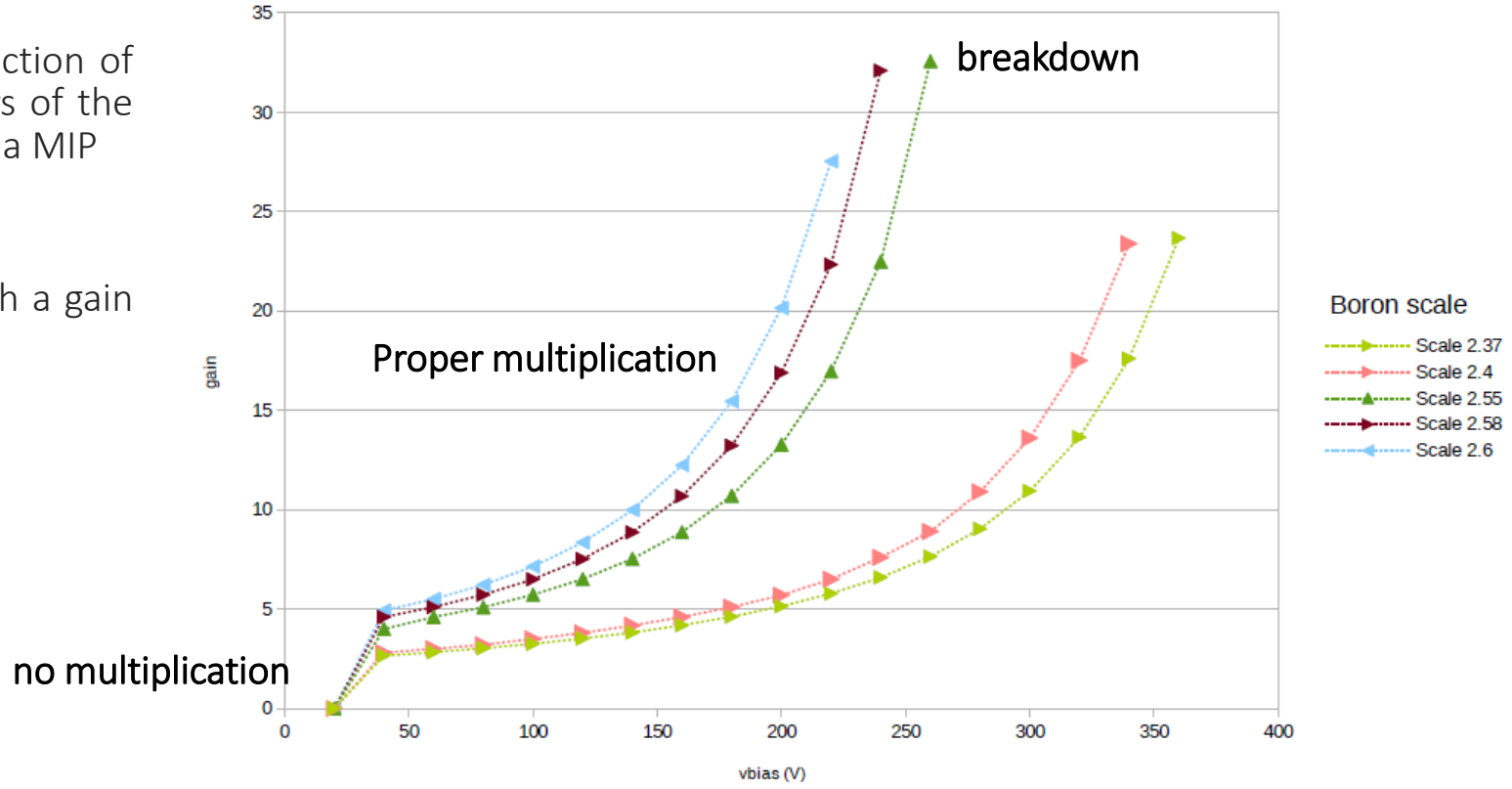
Guardring study for 50 um thick devices



50 um – gain curves

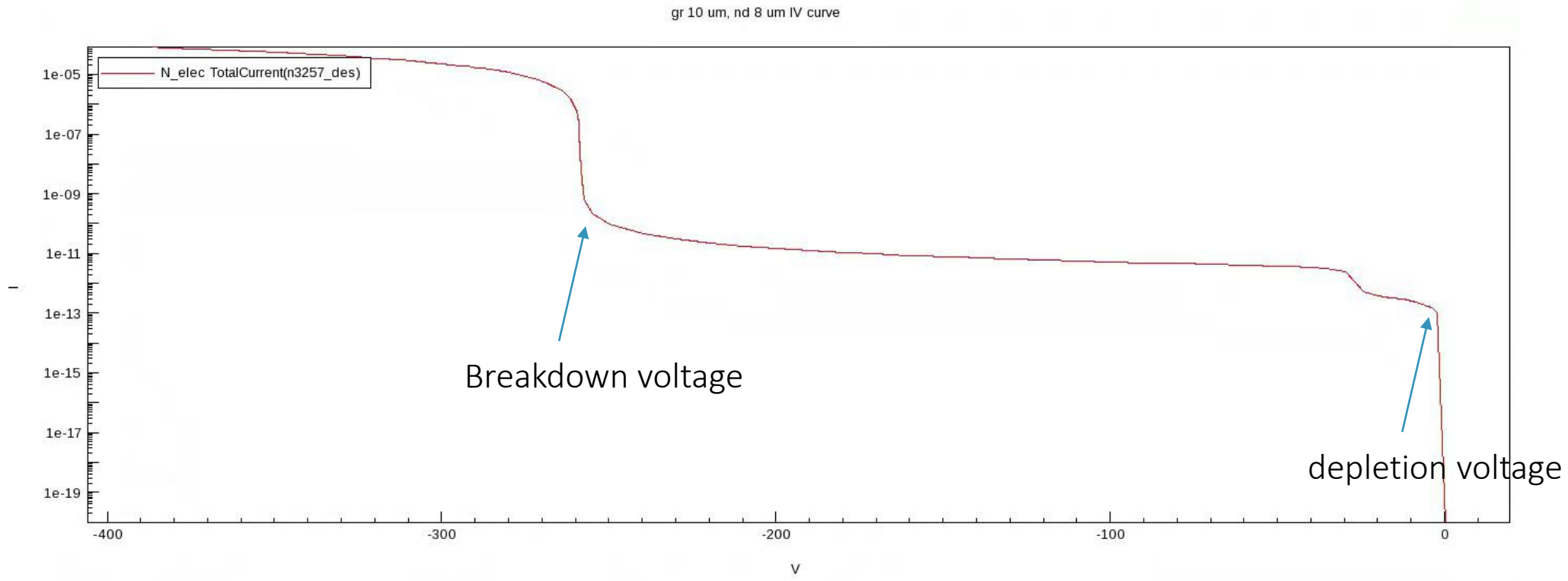
Extraction of the gain value as a function of bias voltage for different scale factors of the gain layer doping profile, response to a MIP

→ the goal is to obtain a device with a gain of ~ 15 between 150 and 200 V



50 um – IV curve

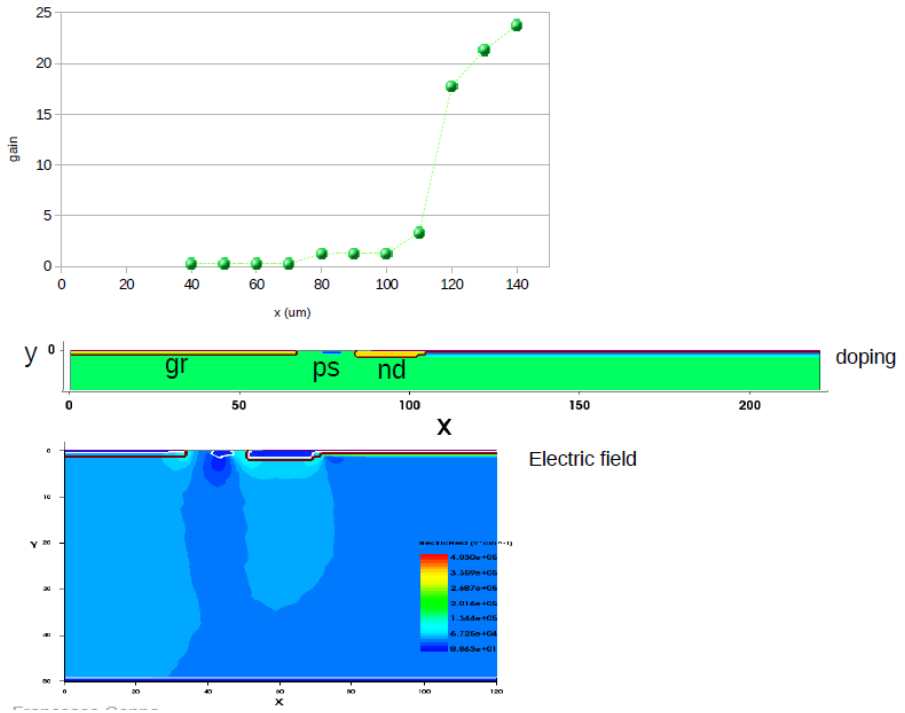
Dark current as a function of bias voltage for a 50 um thick device



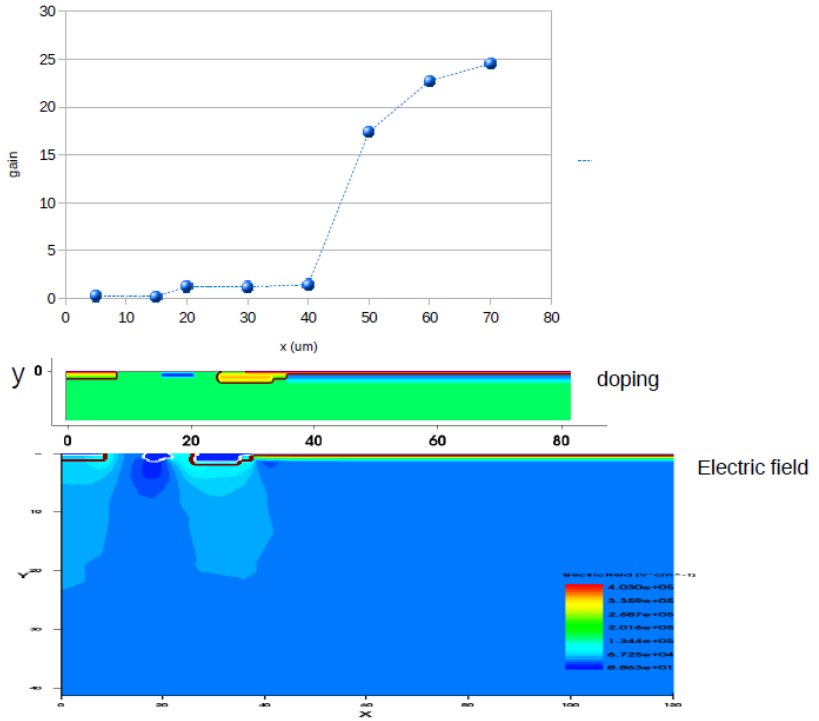
50 um – gain scan along x

Extraction of gain value along x coordinate to study the effectiveness and size of ndeep/pstop implants (dead area between electrodes)

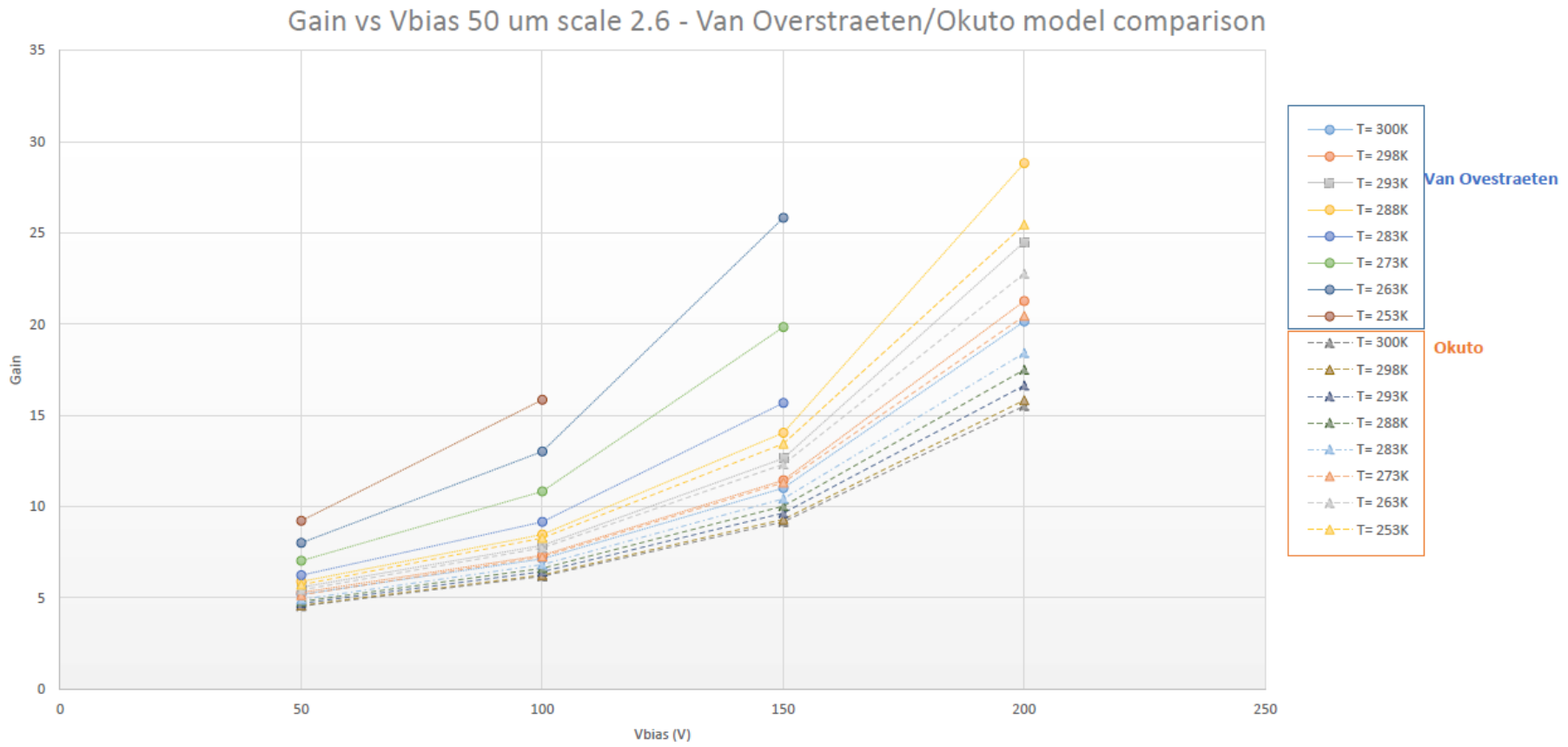
Maximum guardring/ndeep size



Minimum guardring/ndeep size



50 um – low temperature simulations



Conclusions and future plans

- UFSD are good candidates to be used as timing detectors for the CT-PPS spectrometer
- The expected time resolution for a 50 um thick UFSD is ~ 30 ps (indeed confirmed by beam tests performed in August 2016)
- The TOFFEE ASIC has been designed as custom front-end for UFSD with CT-PPS geometry
- TOFFEE + UFSD simulated time resolution is ~ 45 ps for a MIP signal for a single module (4 modules: ~ 22 ps)
- Tests on TOFFEE started in October 2016 with a custom readout board (by LIP) and a test pulse. Simulated noise and time resolution have been confirmed
- Tests on TOFFEE with UFSD sensors will be performed in January 2017

- FBK 275 um thick UFSDs have been produced and tested
- The design of FBK 50 um thick sensors has been completed. Devices will be produced in the next months

- Beam tests with the full TOFFEE + UFSD system are scheduled for May/June 2017
- Assembling and mounting of detectors + front-end is planned for winter 2017
- An improved TOFFEE version with analog outputs and TDC is also foreseen