University of Turin

Faculty of Mathematical, Physics and Natural Sciences

Physics degree thesis

LePix: monolithic pixel detector for LHC tracking systems

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Outline

- ***Background***
  - ***LHC upgrades scenarios***
  - ***hybrid and monolithic architectures for pixel detectors***
- ***The LePix project***
  - ***basic sensor concept***
  - ***the first 90 nm LePix submission***
- ***Measurements and results***
- ***Conclusions***

LHC upgrades scenarios

- first 2010-2012 physics run
  - nowaday LHC operating conditions: $\sqrt{s}$ = 7 TeV, luminosity ~ 3 x 10^{33} cm $^{-2}$ s $^{-1}$, 50 ns bunch crossing
  - operating conditions for 2012 are under consideration both for $\sqrt{s}$ and for the bunch spacing

- first long shutdown in 2013 (**LS1**)

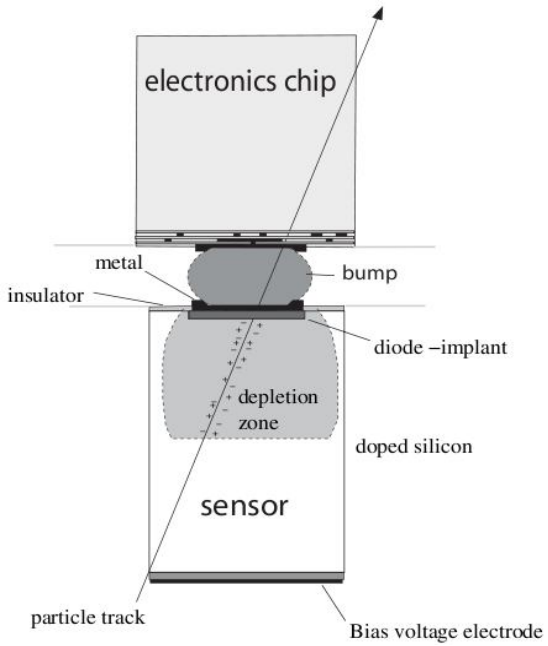
- second long shutdown in 2017 (**LS2**)

- third long shutdown in 2021 (**LS3**) → **Super-LHC (sLHC)**
  - luminosity up to 10^{35} cm $^{-2}$ s $^{-1}$
  - replacement of the entire ALICE, ATLAS and CMS tracking systems
  - more layers equipped with sensors featuring high granularity, speed and adequate radiation hardness also in tracker regions at present instrumented with conventional silicon strip detectors

first R&D programs must start now in order to be ready for ~ 2020 (each project requires a typical man-power of 5 ÷10 man-years)

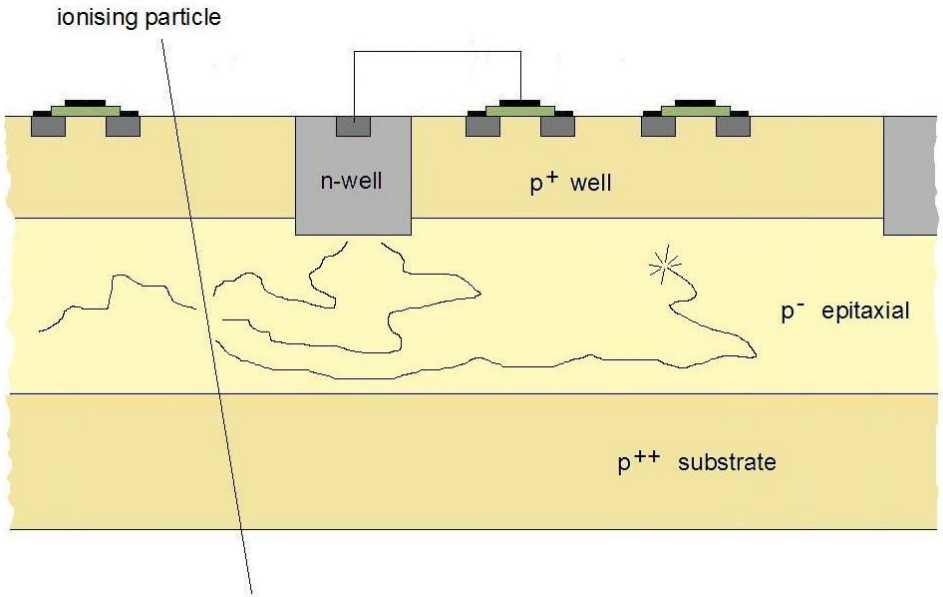
Hybrid vs. monolithic

hybrid pixel detectors



- ***bump bonding*** technique → expensive
- charge collection ***by drift*** → speed & RH
- material budget ~ 300 μm
- power consumption ~ 250 mW/cm^2
- cost can be afforded in the innermost 2 ÷ 3 layers of a collider tracking system covering ~ m^2

Monolithic Active Pixel Sensors (MAPS)



- detector & read-out electronics ***on the same piece of silicon***
- charge collection ***by diffusion*** (~ 100 ns) → ***no reverse bias***
- low material budget ~ 10 ÷ 30 μm
- low power consumption (a few tens of mW/cm^2)
- standard CMOS technologies → ***low production cost***

The LePix project

- a long-term *R&D* project potentially suitable for ~ 2021 LHC trackers upgrades and for future HEP experiments

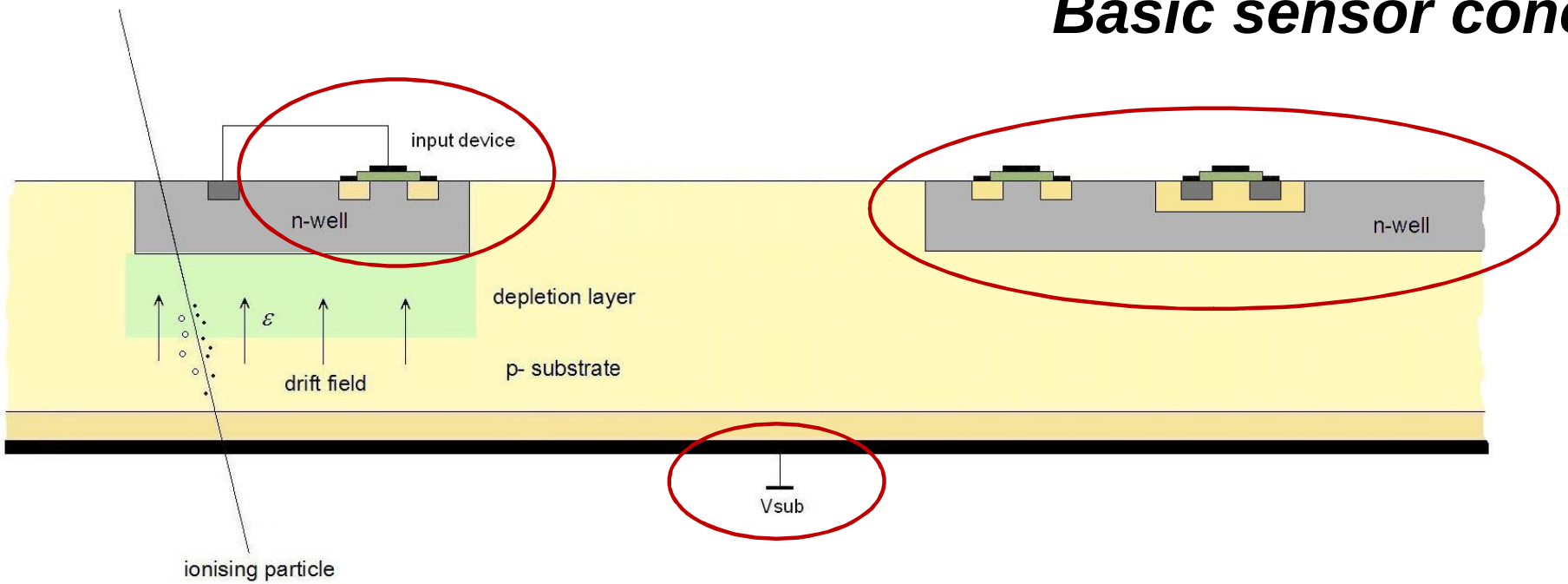
- the project explores the possibility of implementing ***monolithic pixel detectors in very deep submicron CMOS technologies***

- the goal is ***to combine advantages of MAPS and hybrid pixel detectors architectures***

  - MAPS exhibit low power consumption and low material budget, integrating the sensor and its read-out electronics on the same substrate according to the monolithic approach

  - in hybrid pixel detectors the charge collection by drift ensures speed and adequate radiation tolerance

Basic sensor concept



- the key difference with respect to traditional MAPS is the ***reverse-biased substrate***
  - charge collection ***by drift*** → speed and radiation tolerance

- ***high resistivity*** (≥ 100 Ω cm) wafers → depletion layers of 10 ÷ 40 μm by applying moderate reverse biases (50 ÷ 100 V)

- possibility offered by the foundry of porting ***standard CMOS processes*** on high resistivity wafers
  - the remaining electronics is built in a dedicated *n*-well of ***low resistivity*** (~ 1 ÷ 2 Ω cm) at the border of the sensitive region
  - the *n*-well must be insulated from the reverse-biased substrate in order to avoid breakdown → ***non standard*** and ***aggressive*** layout (special masks, protection structures, etc.)

Prototyping strategy

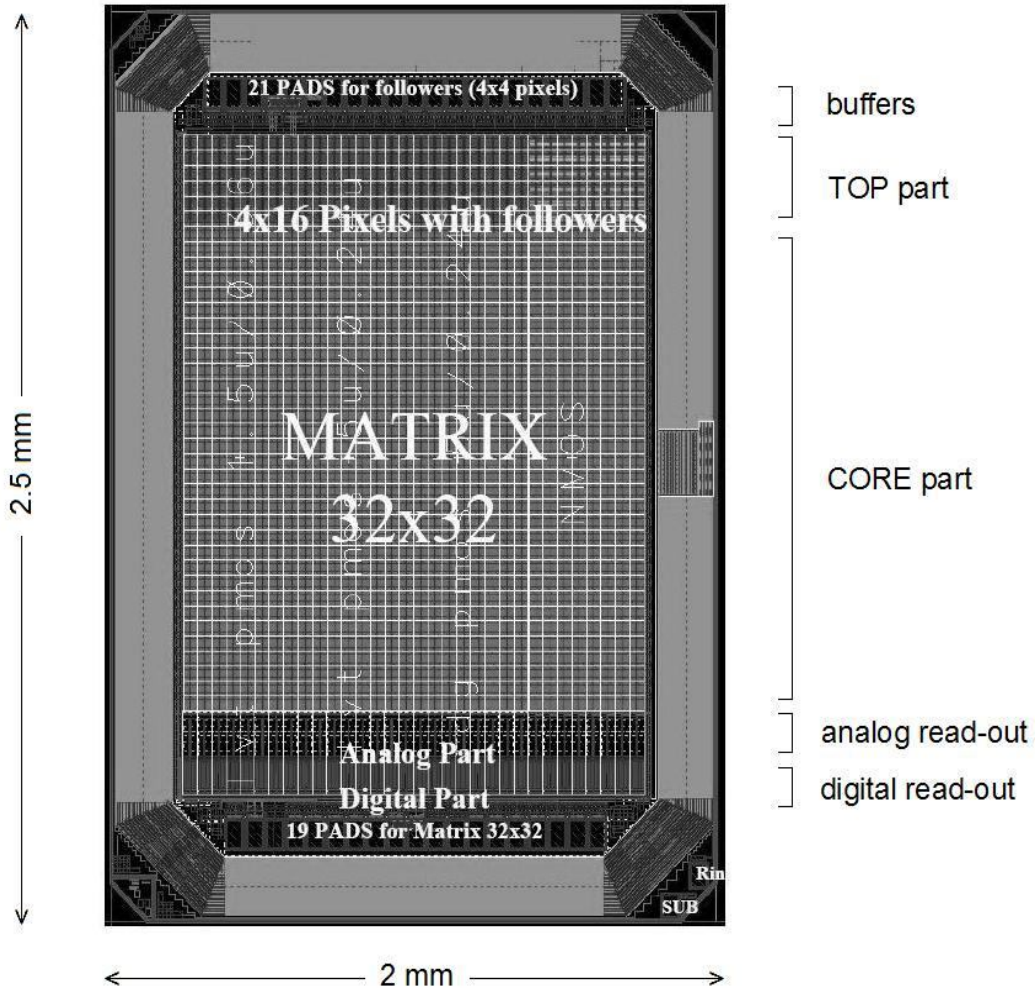
- first LePix submission in standard CMOS **90 nm** technology (March 2010)

- breakdown and transistor test structures, a large diode for radiation tolerance measurements and **4 test pixel matrices** have been submitted with the foundry
  - a ***layout problem*** arised during first tests performed at CERN in summer 2010 (see later)
  - structures submitted on ***standard resistivity wafers*** only

- a prototype of the LePix digital circuitry has not yet been implemented
  - matrices instrumented with some few simplified read-out schemes

- according to measurements and results presented in this work our description is only focused on pixel matrices, in which detecting elements and read-out electronics are integrated on the same piece of silicon

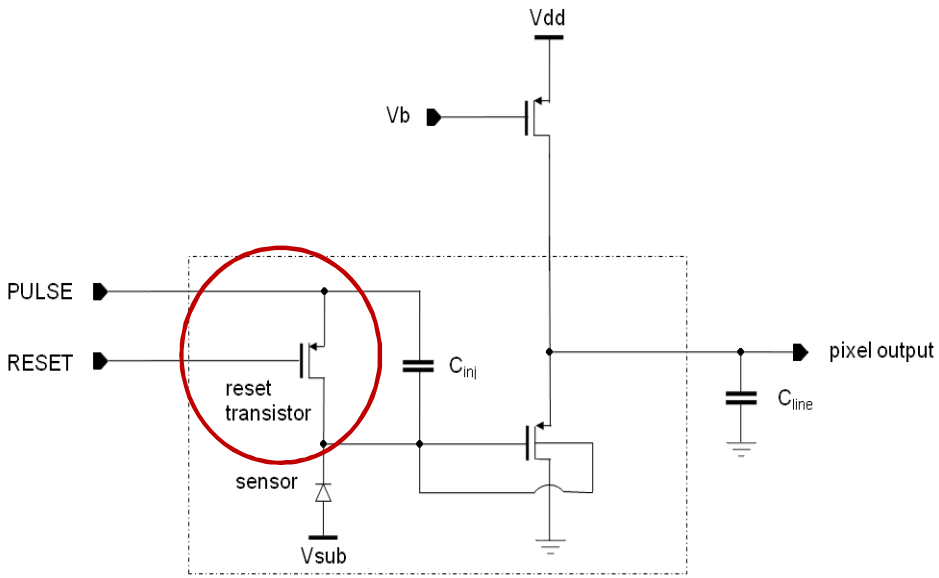
Matrix overall layout



- the sensitive area, the analog read-out and a bare minimum standard digital circuitry are ***integrated on the same chip*** (2 mm x 2.5 mm)
- a guard ring structure (200 µm around the matrix) ensures a uniform depletion layer
- 2 asymmetric regions
  - **TOP part** - 6 rows x 32 columns
  - **CORE part** - 32 rows x 32 columns
- same segmentation and structure, ***different read-out schemes***
  - matrix 1 - 2 → analog serial read-out
  - matrix 3 - 4 → binary serial-read-out

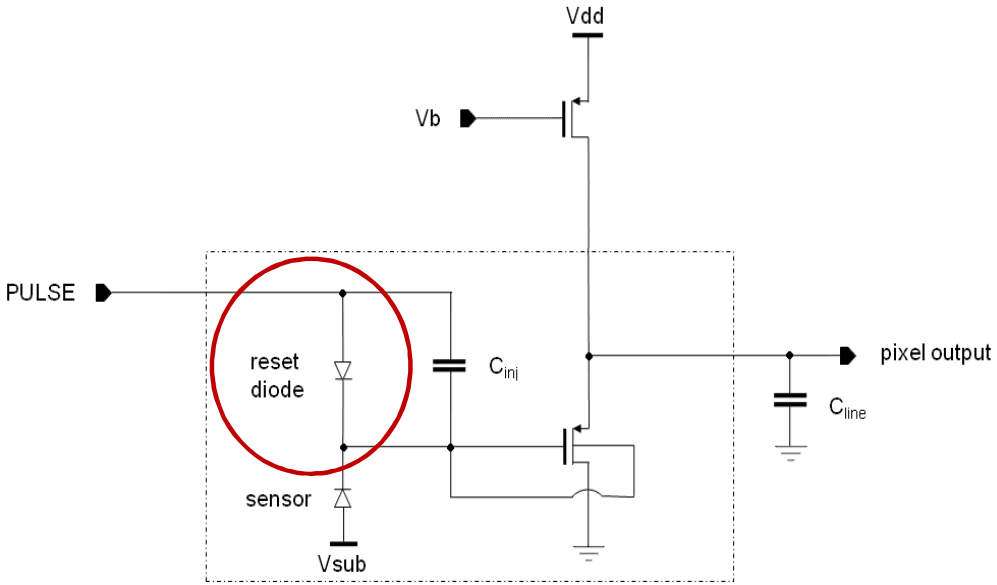
Reset schemes & test pulse

- each sensor needs to discharge the parasitic capacitance after a particle hit has been detected
  - ➢ 2 discharge schemes implemented → ***active-reset*** and ***continuous-reset***
- 3 rows in each matrix can be ***electrically pulsed*** by applying a voltage step (test pulse) over a ***injection capacitor***



active-reset (6 rows TOP part + 16 rows CORE part)

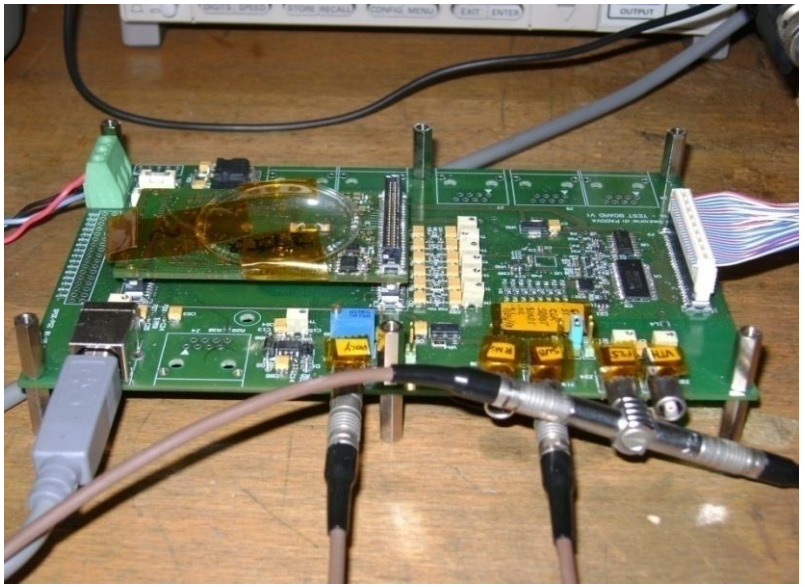
A PMOS reset transistor is employed to reset the sensor. The gate is driven by a digital voltage pulse PIX_RESET and a weak-inversion current discharges the pixel capacitance. Depending on the duration of the PIX_RESET signal the reset transistor can behave like a switch or a linear resistor.



continuous-reset (16 rows CORE part)

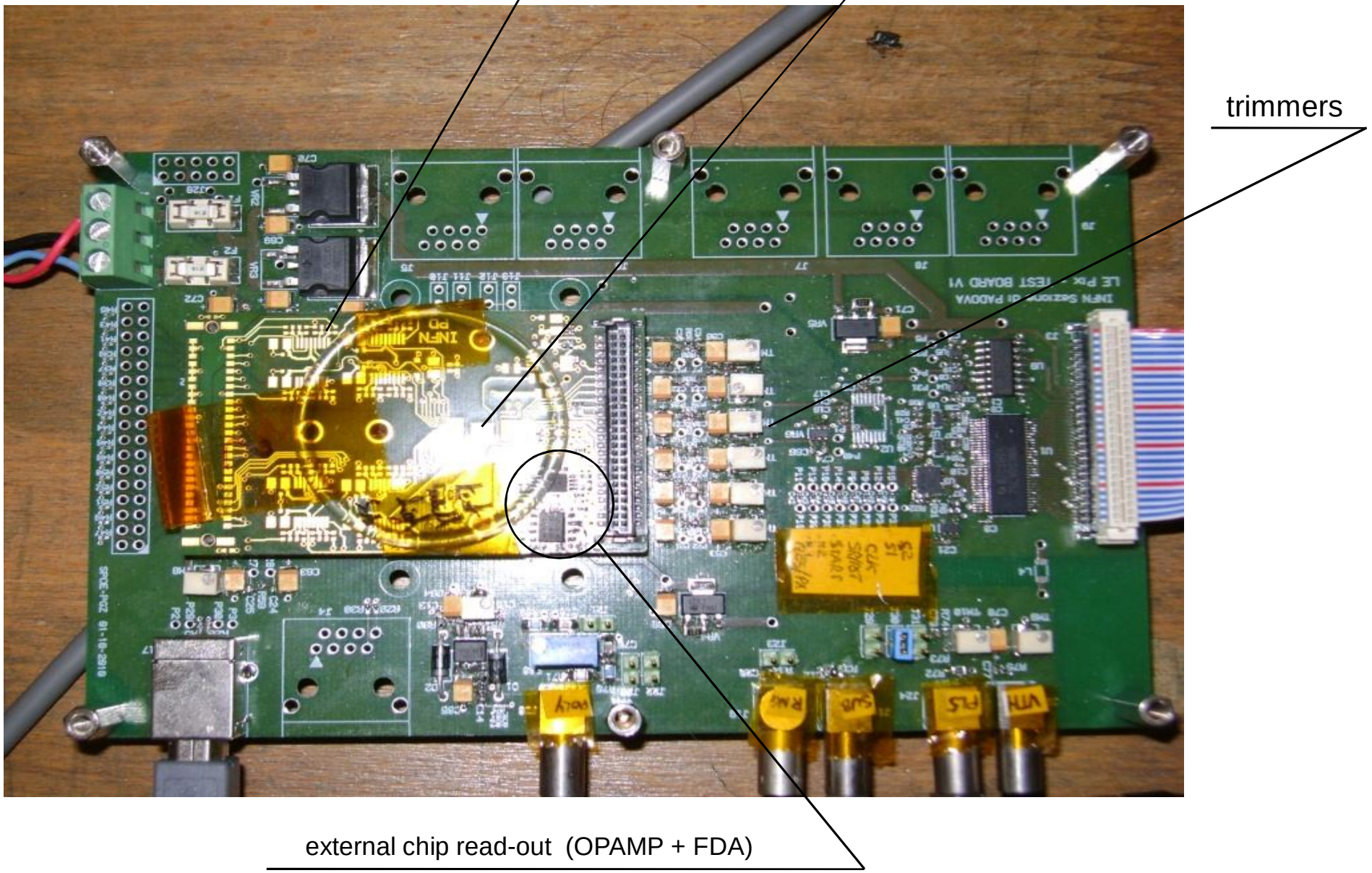
Continuous-reset pixels discharge the sensor capacitance through a diode (connected to a reference DC voltage) which absorbs the leakage current from the pixel.

A plug-and-play setup



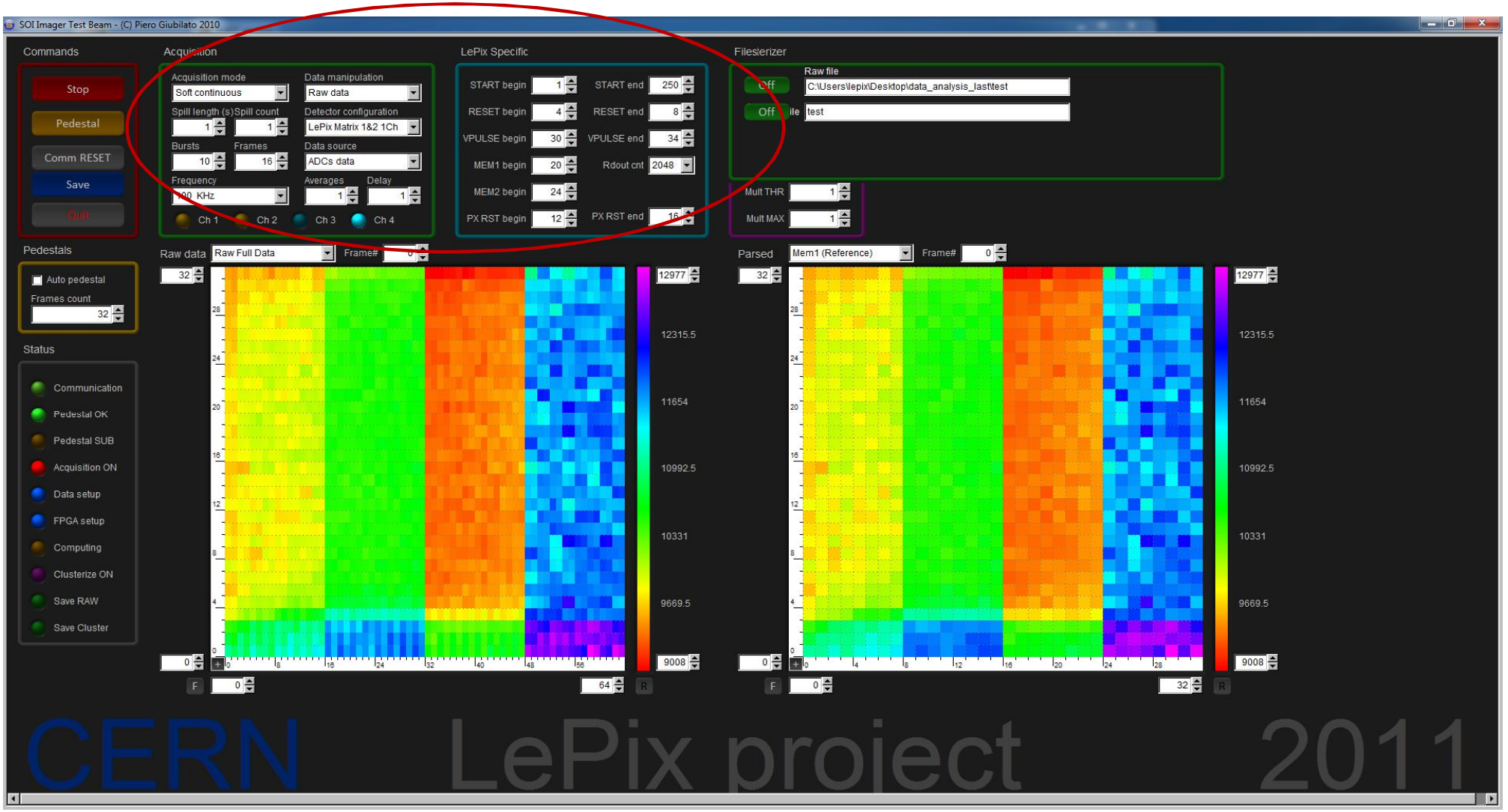
- the chip is wire-bonded onto a mezzanine, which provides mechanical support, output test points and a bare minimum standard circuitry
- main test PCB (bias trimmers, further output test points, signals, power)
- DAQ with FPGA and 14 bit ADC
- a simple USB cable from DAQ to the acquisition PC (Windows 7 OS)

Test PCB



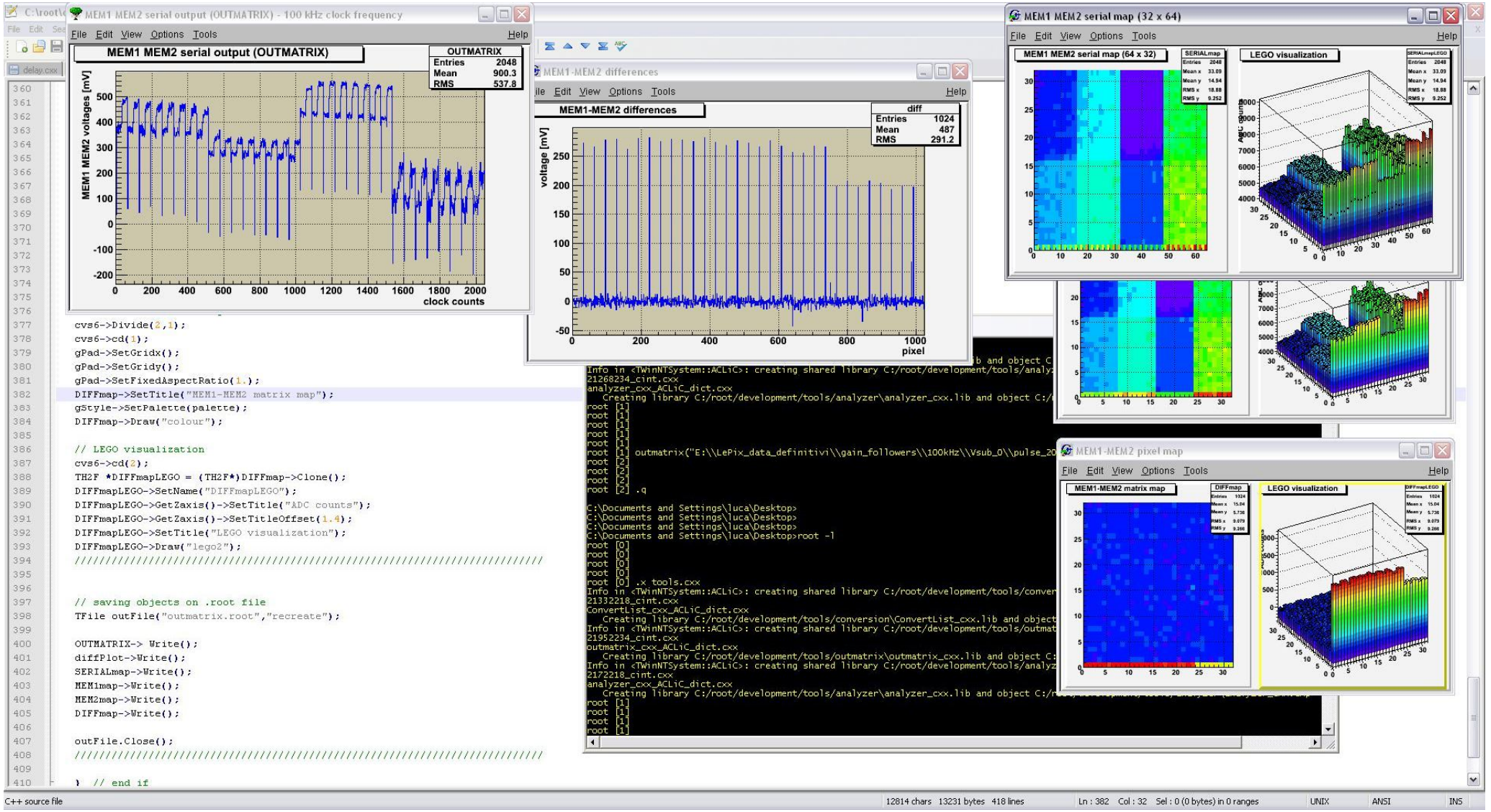
Acquisition interface

- ROOT 5.26 acquisition interface built with Visual C++ 2010
- on-line reconstruction of the CORE part pixel-map (1024 pixels)
- CLOCK frequency + timing for acquisition digital signals
- binary output files containing ADC integers → off-line data analysis



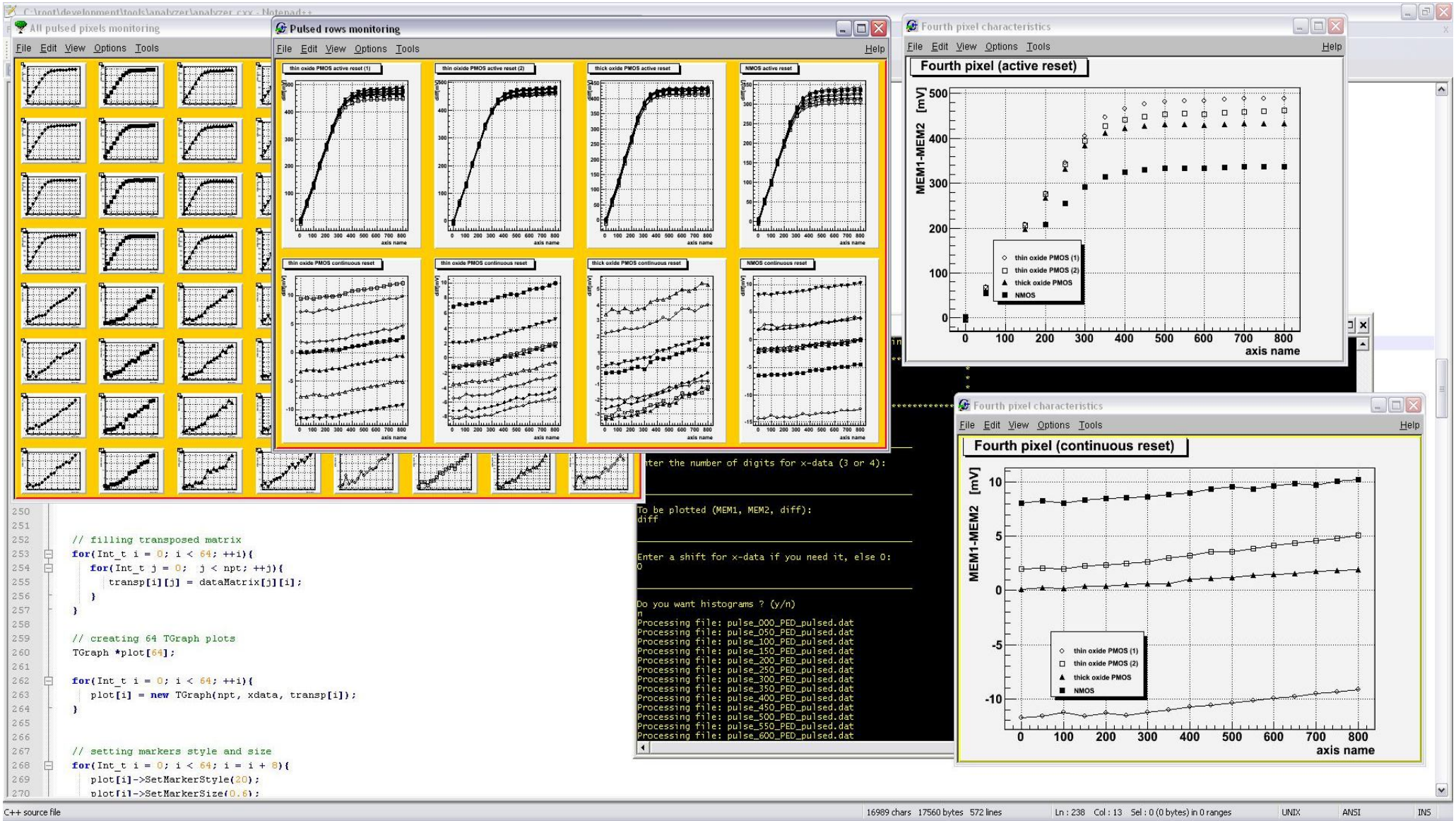
Off-line software (1)

- off-line matrix ***serial output*** and ***pixel-map*** reconstruction



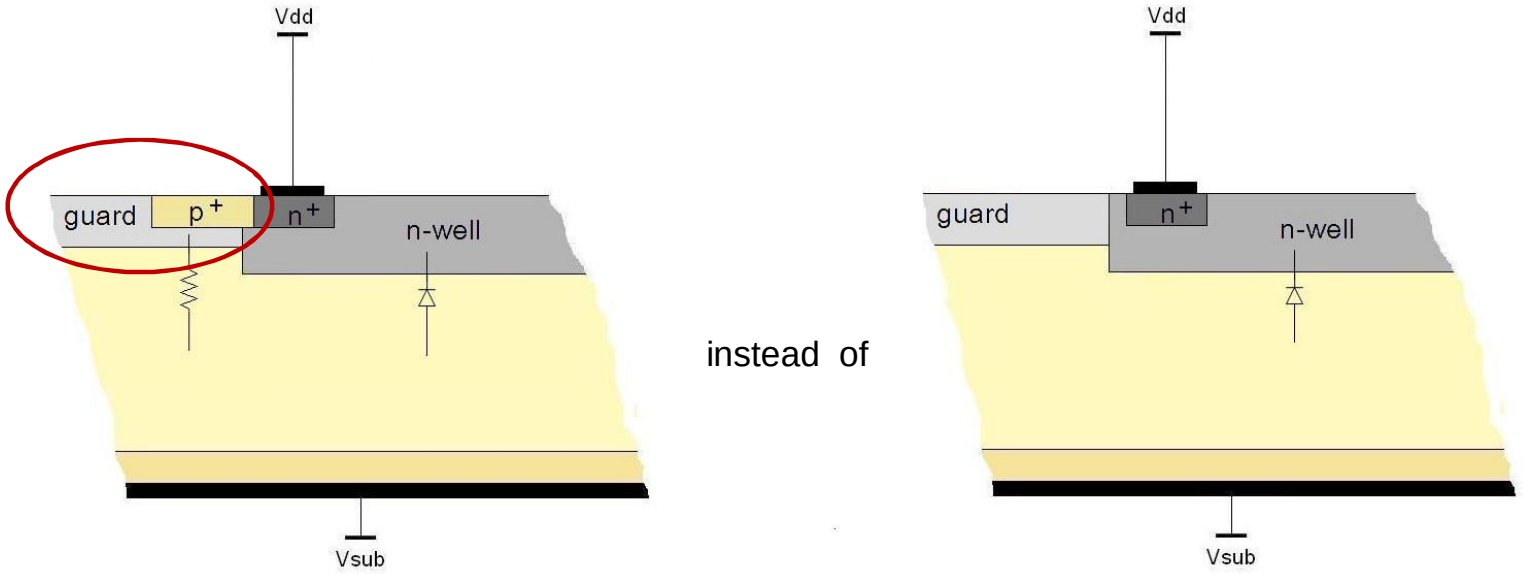
Off-line software (2)

- off-line extraction of ***pixel characteristics*** → output voltages as a function of a certain parameter under consideration (e.g. PULSE amplitude)

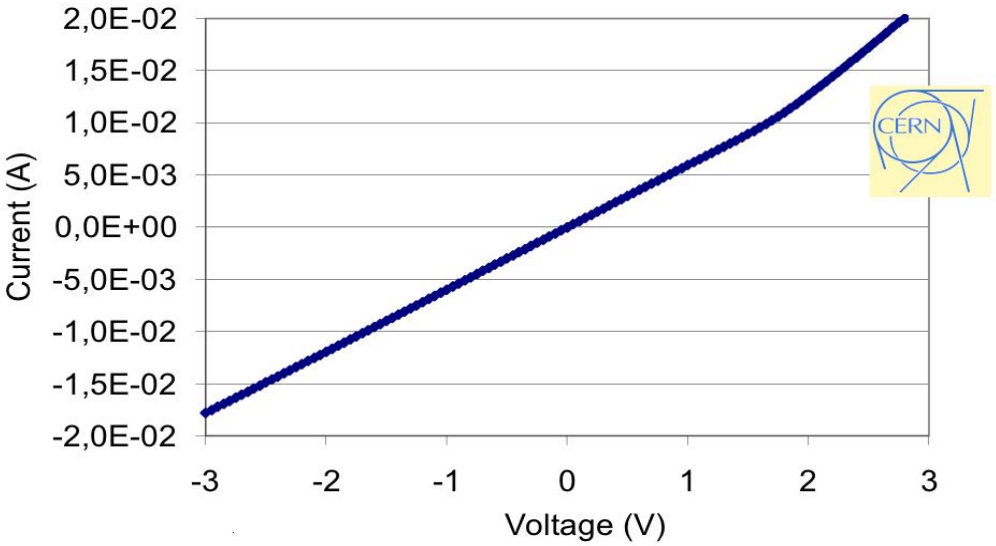


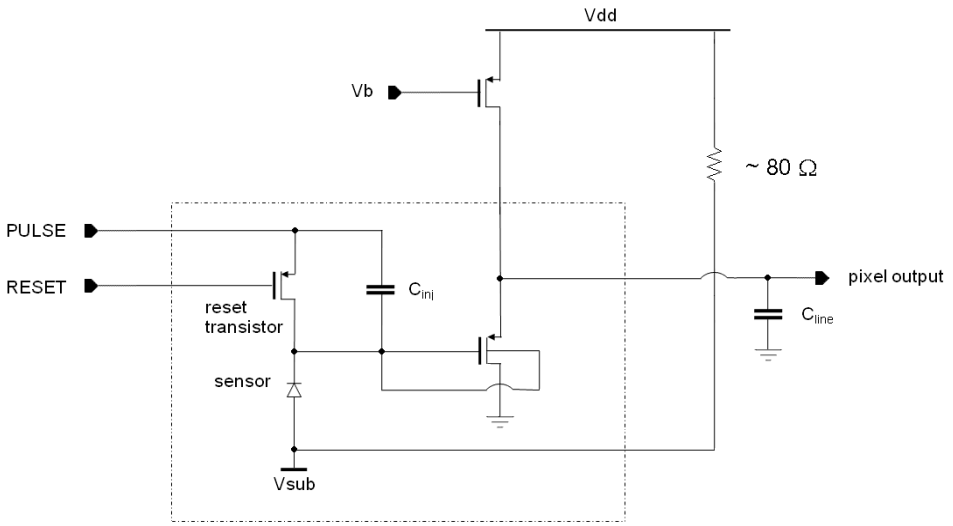
Layout issue

- ***pattern density rules*** in very deep submicron technologies are very restrictive
- LePix requires a really ***non standard*** and ***aggressive*** layout
- beside standard masks provided by the foundry several ***custom masks*** were needed to be drawn in order to better insulate the electronics from the reverse-biased substrate
  - ➢ due to a mismatch with the foundry one of these special masks has been misinterpreted
  - ➢ all matrices of the first submission on standard resistivity received a systematic p^+ implant in the external guard ring → ***layout issue***



Matrix short





$$V_G = \frac{C_{inj}}{C_{pix} + C_{inj}} V_{PULSE}$$

- linear behaviour discovered with first matrix breakdown tests @ *CERN*
  - the p^+ implant introduces a ***resistive path***
  - *mA* currents through the resistive path vs. typical substrate leakage currents ~ *nA*
  - the lot on high resistivity immediately put on hold, requiring adequate corrections

$$C_{pix} >> C_{inj}$$

- nominal reverse biases are forbidden → - 5 V is enough to ***damage the chip***
  - ***the chip substrate can not be depleted*** → no particle hits can be detected
  - tests and measurements can be performed only on the read-out electronics, excluding the sensor
  - only active-reset pixels can be excluded

Measurements and results

- breakdown voltage > 30 V close to expectations + radiation tolerance @ *CERN*
  (but a systematic characterization of the read-out electronics embedded in the sensors has not been performed)

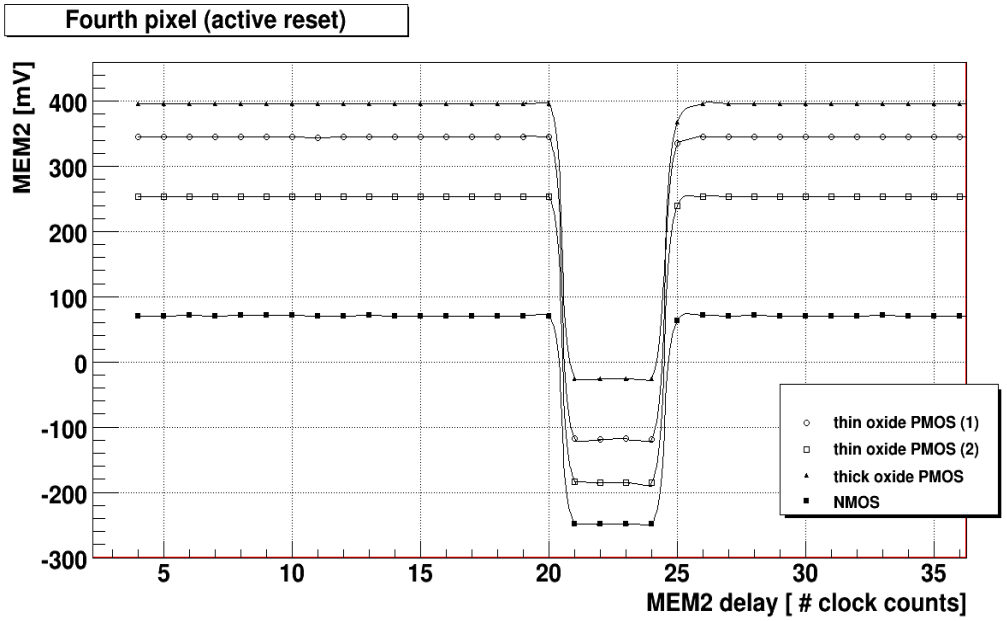
- setup validation (***external-chip read-out with OPAMP + FDA + ADC***)
  - setup linearity (DC characteristics + voltage gain)
  - noise

- matrix 1-2 CORE part characterization (***MAPS-like double sample analog serial read-out***)
  - matrix output
  - source followers (SFs) characterizations → measurements ***at the transistor level***, validating the 90 nm LePix electronics
  - estimation of the pixel capacitance

- matrix 3-4 CORE part characterization (***binary serial read-out based on PREAMP + DISC***)
  - matrix output
  - threshold scan and thermal noise
  - PREAMPs and DISCs homogeneity
  - bias characteristics

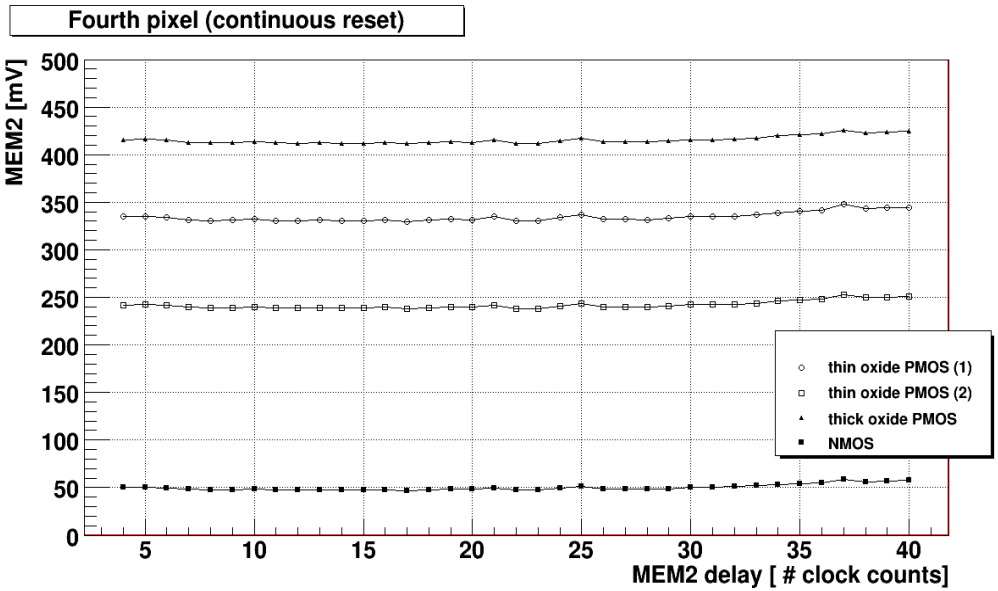
  ⎫ discussed

PULSE reconstruction in matrix 1-2



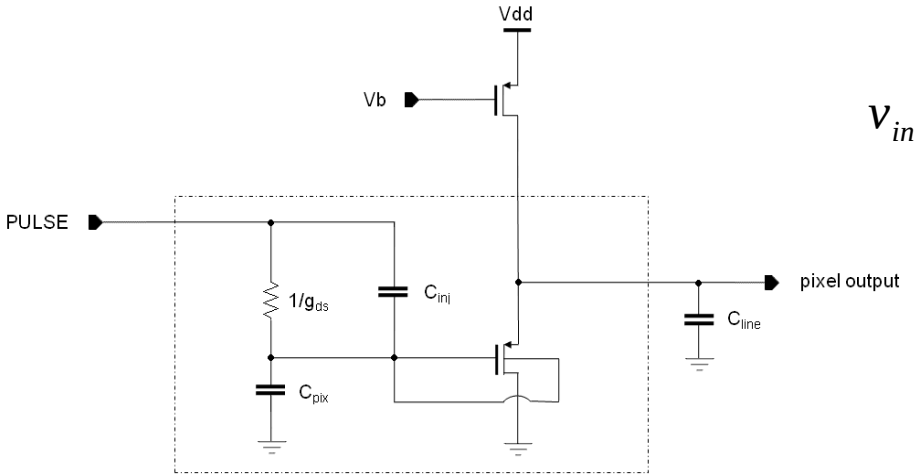
A direct proof of the severe constraint introduced by the short in the guard …

*… due to the **large capacitance of the not depleted sensor** only input transistors of the active-reset pulsed row received the PULSE !*

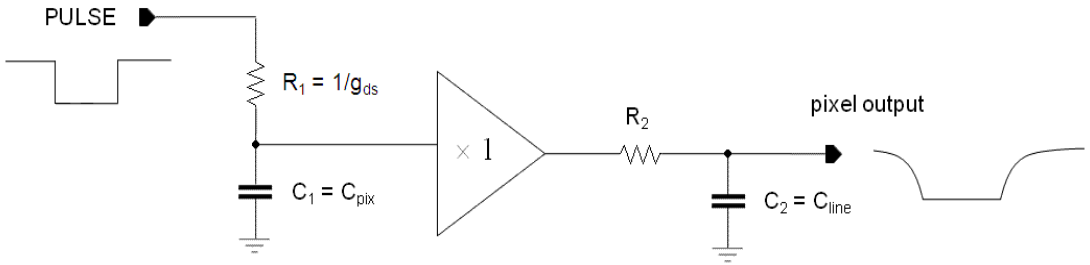


$$C_{pix} >> C_{inj}$$

Estimation of the pixel capacitance in matrix 1-2

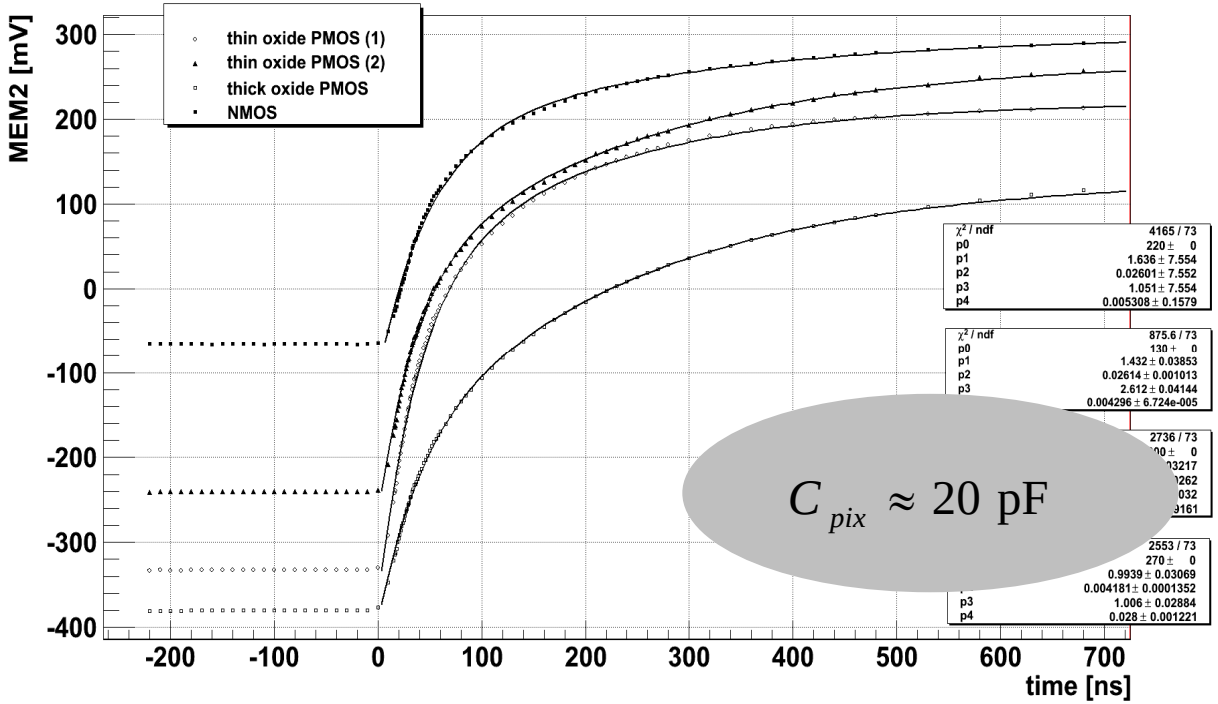


$$v_{in}(t) = k\,u(t)$$



Although the external PULSE is a signal with sharp rising and falling edges the output waveform is expected to have ***smooth transitions due to parasitic capacitances***

- two integrations performed by ***2 buffered RC low-pass filters***
- fine scan of the PULSE rising and falling edges, fitting experimental data with the predictable function (Laplace theory)



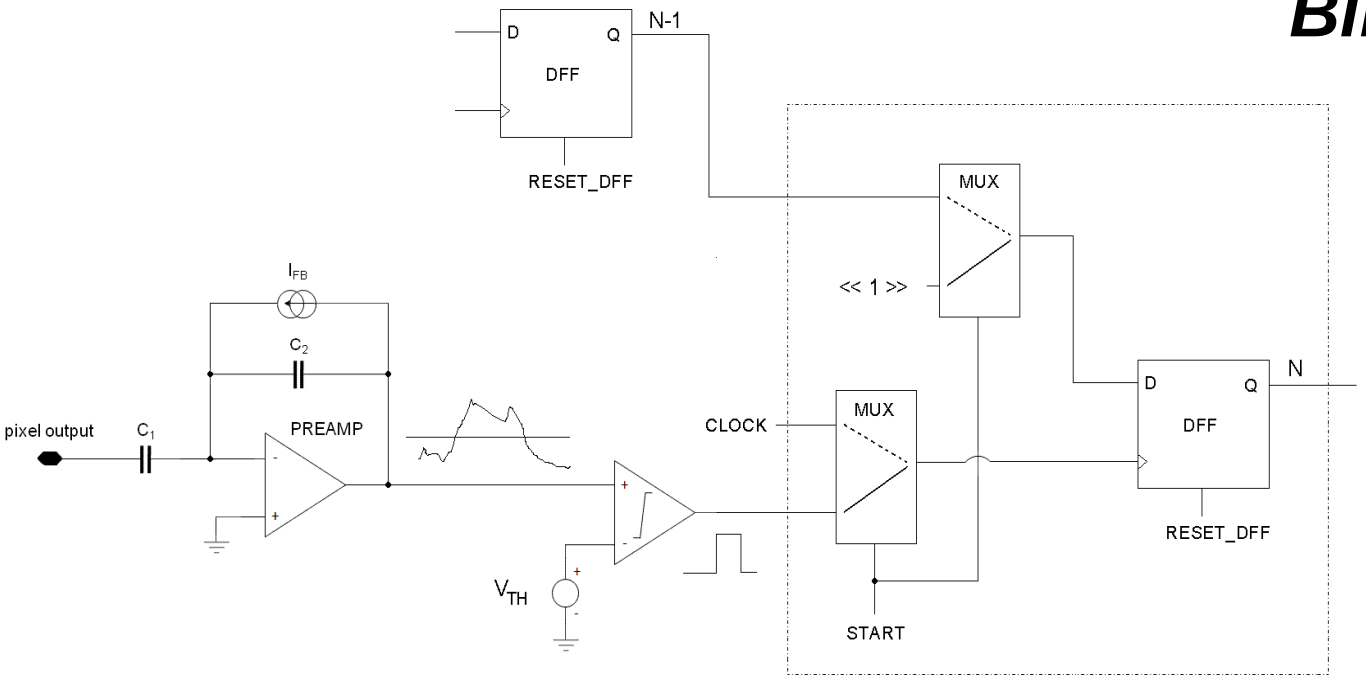
Simplified fitting function :

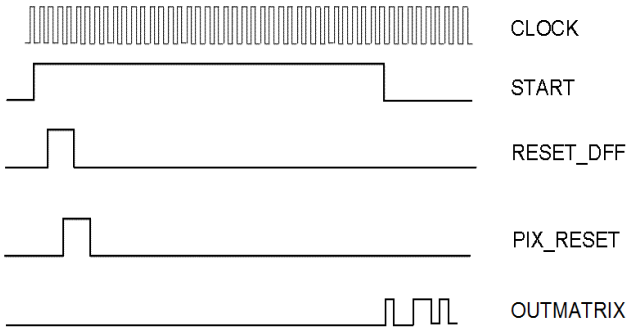
$$v_{out}(t) = k\left(1 - a\,e^{-b\,t} - c\,e^{-d\,t}\right)$$

$\tau_1 \approx 200$ ns $\qquad \tau_2 \approx 38$ ns

Matrix 3-4 CORE part characterization

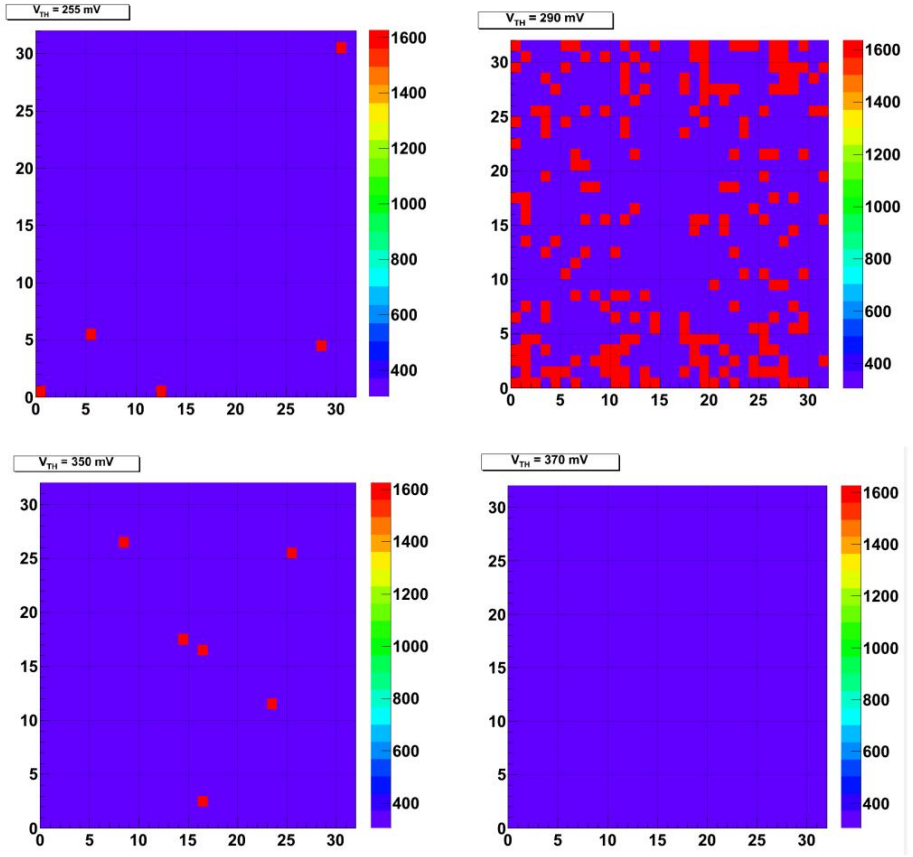
Binary serial read-out

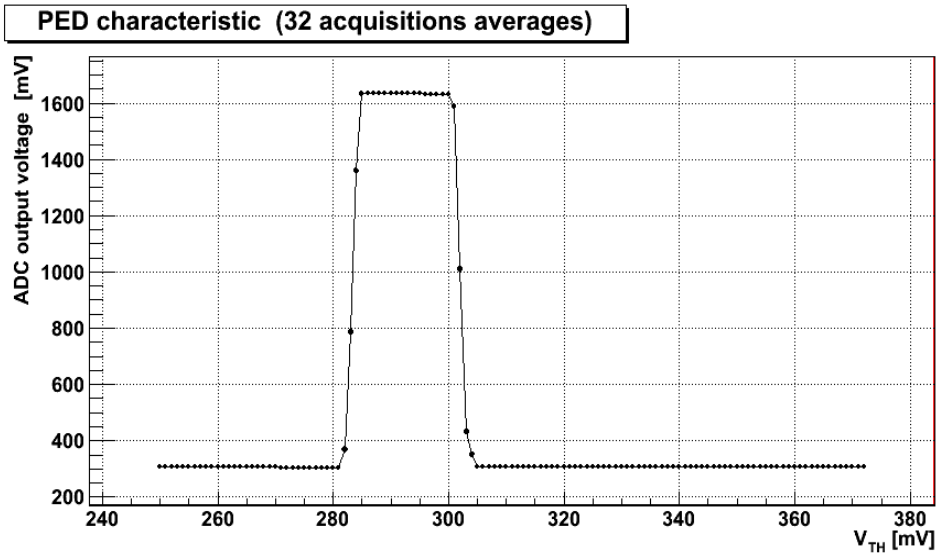




- input transistor in SF configuration AC coupled to a voltage amplifier (PREAMP) followed by a comparator (DISC)
- no support for ToT available
- ***parallel analog read-out*** of the CORE part towards the periphery of the matrix + ***serial digital read-out***
- 2 multiplexers (MUX) and a D-Flip/Flop (DFF) for each pixel
- 1024 DFFs configured as a shift register → ***binary serial read-out***
  - if a *transition* occurs the DISC produces a digital output pulse, providing a clock rising edge for the DFF
  - the output is a sequence of **1024 *logic values*** 1/0 fed to the ADC through the external-chip read-out chain

Threshold scan

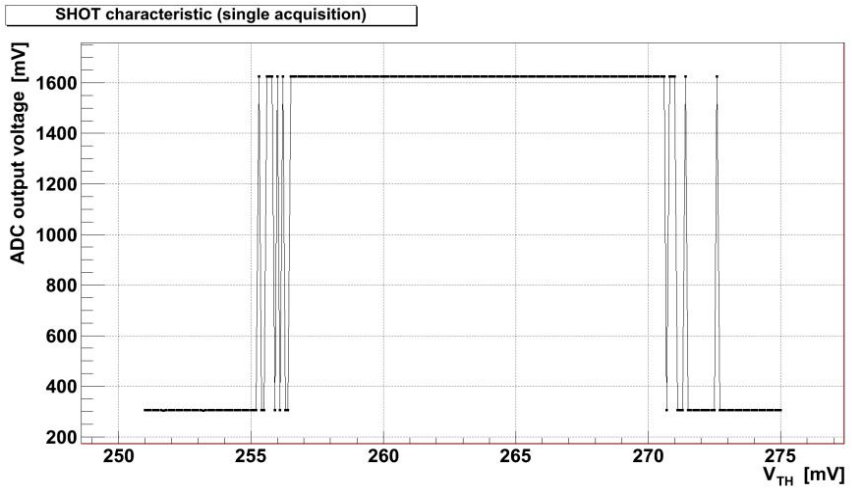


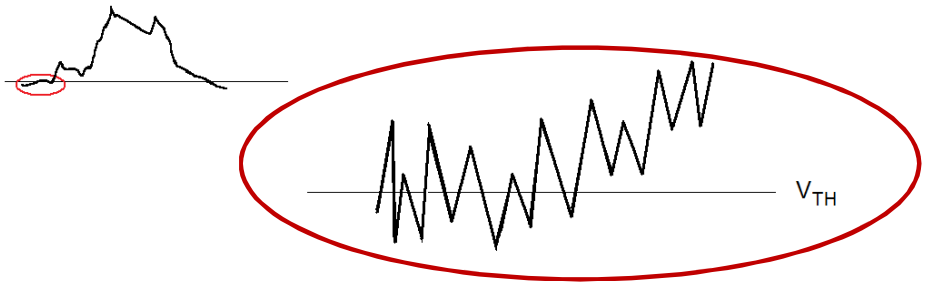


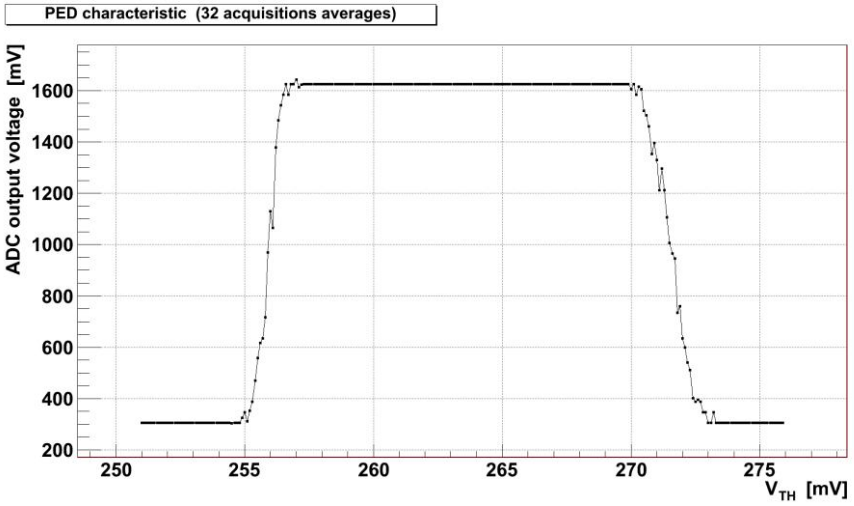
A representative PED characteristic (i.e. DFF output vs. V_{TH}).
Something interesting occurs in rising and falling edges…

- despite no particle hits can be measured, the front-end electronics register some transitions by varying the threshold voltage
- ***DFF outputs as a function of the DISC threshold voltage V_{TH}***
  - each DFF produces a 1 in the 250 to 370 mV threshold range
  - if V_{TH} is too low or exceeds a certain maximum value all DFF ouputs become 0
  - a parasitic signal is superimposed to the baseline → some ***noise*** affects DISC inputs

Edges fine threshold scan



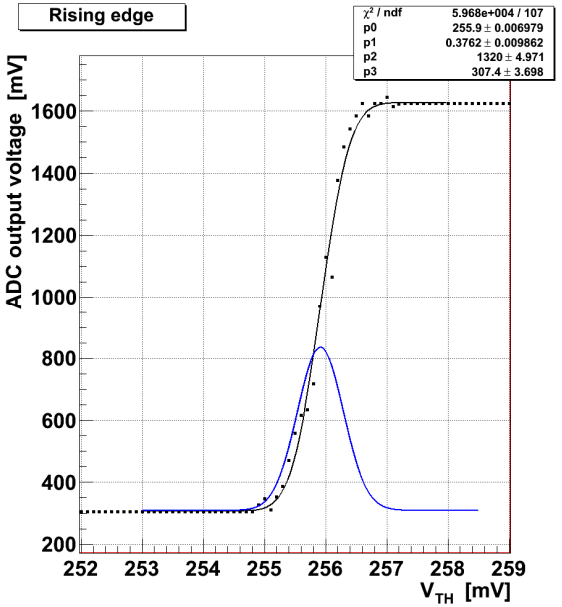


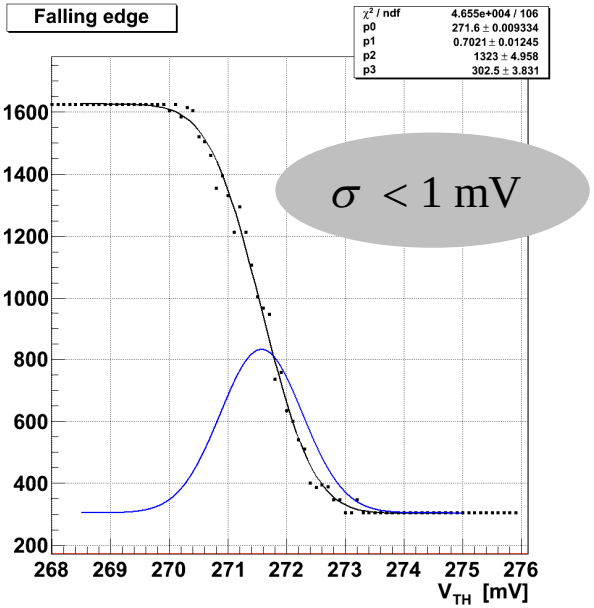


Some ***thermal noise*** *superimposes to the main parasitic signal*

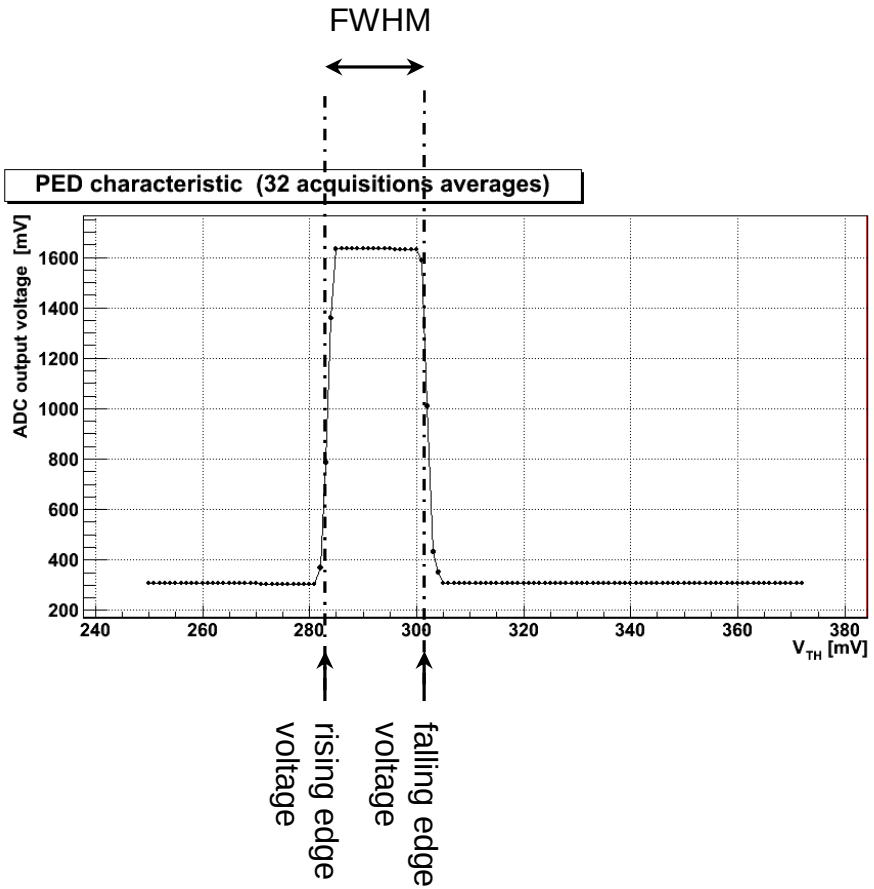
- rising and falling edges SHOT values are indeterminated
- PED values are averages of one by one logic values, resulting at the end in no more logic values

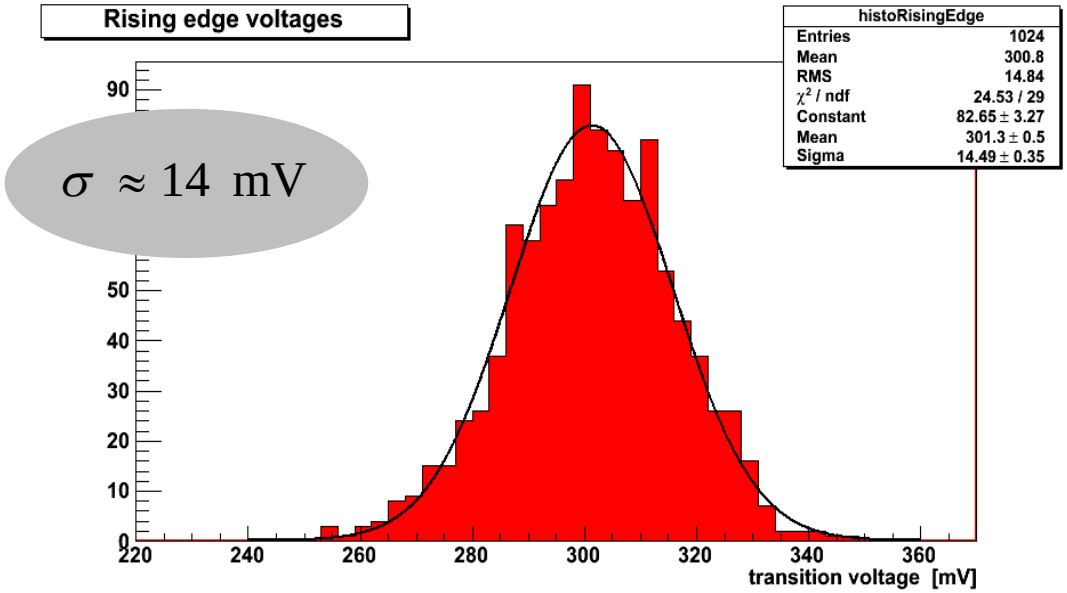
A measurement of thermal voltage fluctuations is obtained by fitting edges with 2 sigmoids





Thresholds (dis)homogeneity



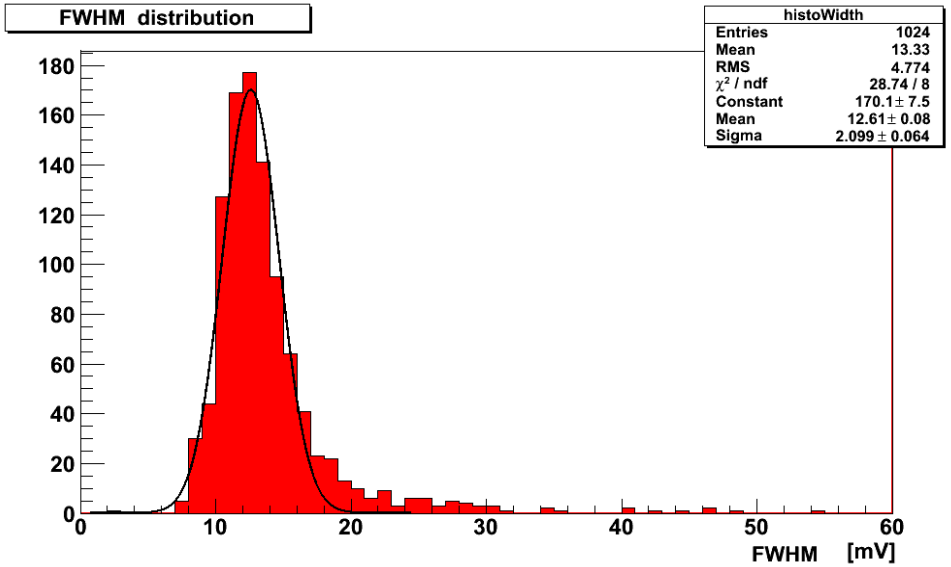


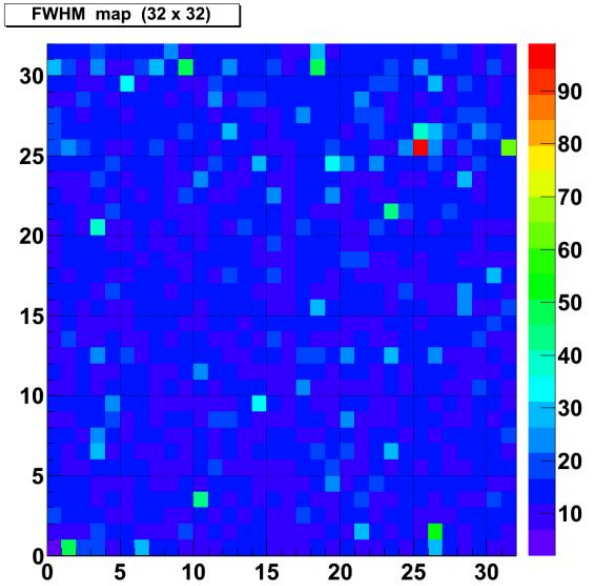
The set of 1024 DFF outputs shows different edge transition voltages

- the spread of the distribution quantify the DISC ***thresholds dishomogeneity***
- a Standard Deviation of 14 mV is quite large with respect to the nominal threshold (20 mV above the baseline)
- this dishomogeneity confirms difficulties introduced by the LePix aggressive and non standard layout, necessary to meet the tigh area requirements (e.g. mismatches at the transistor level in DISC devices)

noise amplitude ~ 10 ÷ 18 mV
(Gaussian spread)

FWHM distribution

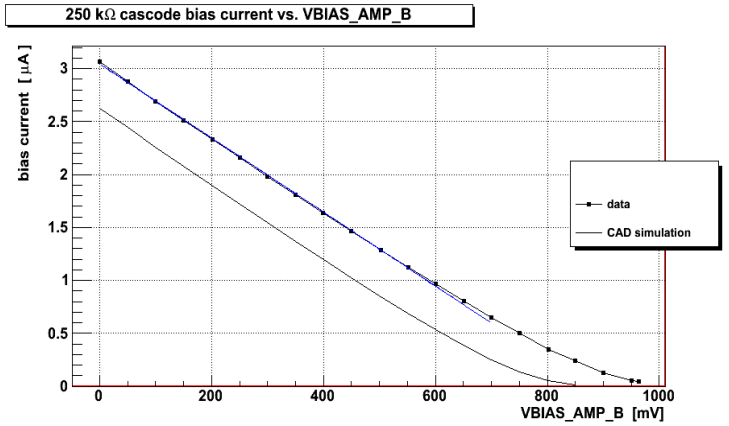


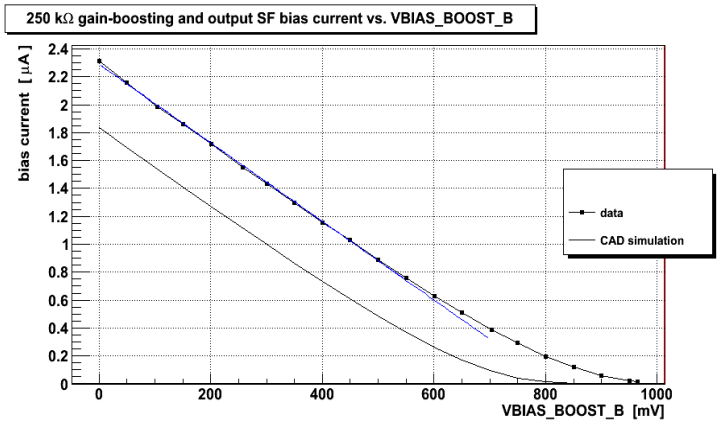


DISCs which lead to a FWHM > 20 mV
are scattered randomly.
No evidence of a systematic clusterization.

- the FWHM of a PED characteristic represents the ***noise amplitude***
- the set of 1024 DFF outputs shows different FWHM
  - Gaussian trend followed by an excess of devices (~10%) affected by a larger noise (FWHM > 18 ÷ 20 mV)
  - if the noise is injected before the PREAMP stage, a certain Gaussian spread can be attributed to a ***dishomogeneity in the PREAMP voltage gains***
  - the FWHM map does not show a systematic clusterization of devices affected by a larger noise
    → ***no coupling between analog and digital lines***

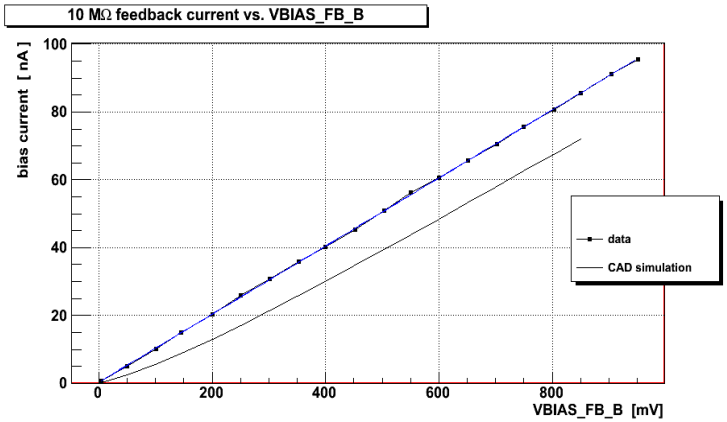
Bias characteristics vs. CAD simulations

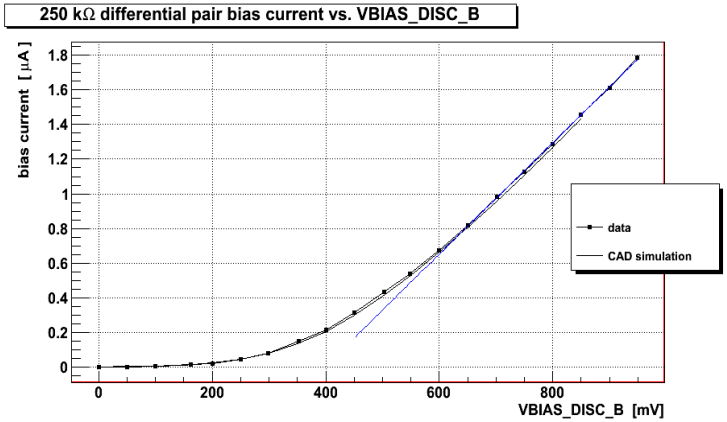




PREAMP

PREAMP





DISC

- devices requires some ***bias currents*** that must be regulated externally → ***trimmers*** placed on the external test PCB
- ***measured bias currents versus trimmer output voltages***
- data compared with theoretical values predicted by ***DC simulations***
- proper bias voltages must be choosen within the linear regions

some differences between data & simulations → non standard layout

Conclusions

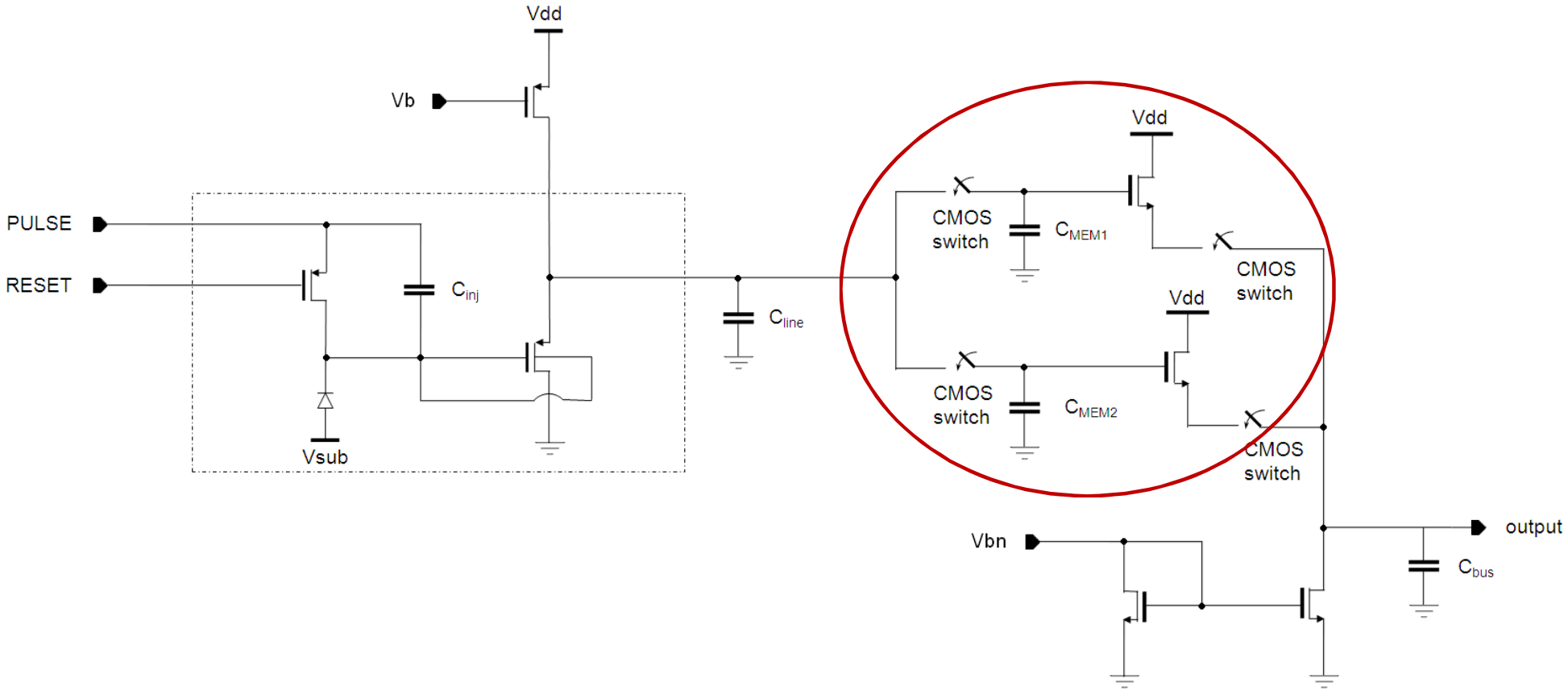
- the LePix project explores the possibility of implementing monolithic pixel detectors in very deep submicron CMOS technologies with performance adequate for the LHC upgrades and for future HEP experiments
- at present both the ALICE and CMS collaborations have been shown an interest for the project
- within the LePix collaboration the INFN has been an important reference point
  - design of matrices 3-4 analog read-out (Turin)
  - experimental setup and acquisition software (Padova)
- this thesis has been devoted to the ***characterization of the matrix prototypes of the first Lepix submission*** in standard 90 nm CMOS technology, exploiting the experimental setup available in Turin
  - setup commissioning and validation of the acquisition software
  - development of the software for the off-line data analysis
- pratical design and implementation of the LePix sensor layout are challenging and the first submission with the foundry has shown that the excercise is not easy → discovered a ***layout problem***
  - lot on high resistivity put on hold, requiring adequate corrections
  - ***severe limitations for the characterization of the detector***, imposing the pixels exclusion
  - validation of the read-out electronics implemented in first matrix prototypes
- after corrections tests structures on high resistivity substrates have been submitted and they are expected back from the foundry in October 2011 → ***tests performed on new prototypes will define the actual LePix capabilities***

Thank you
for your attention !

Backup slides

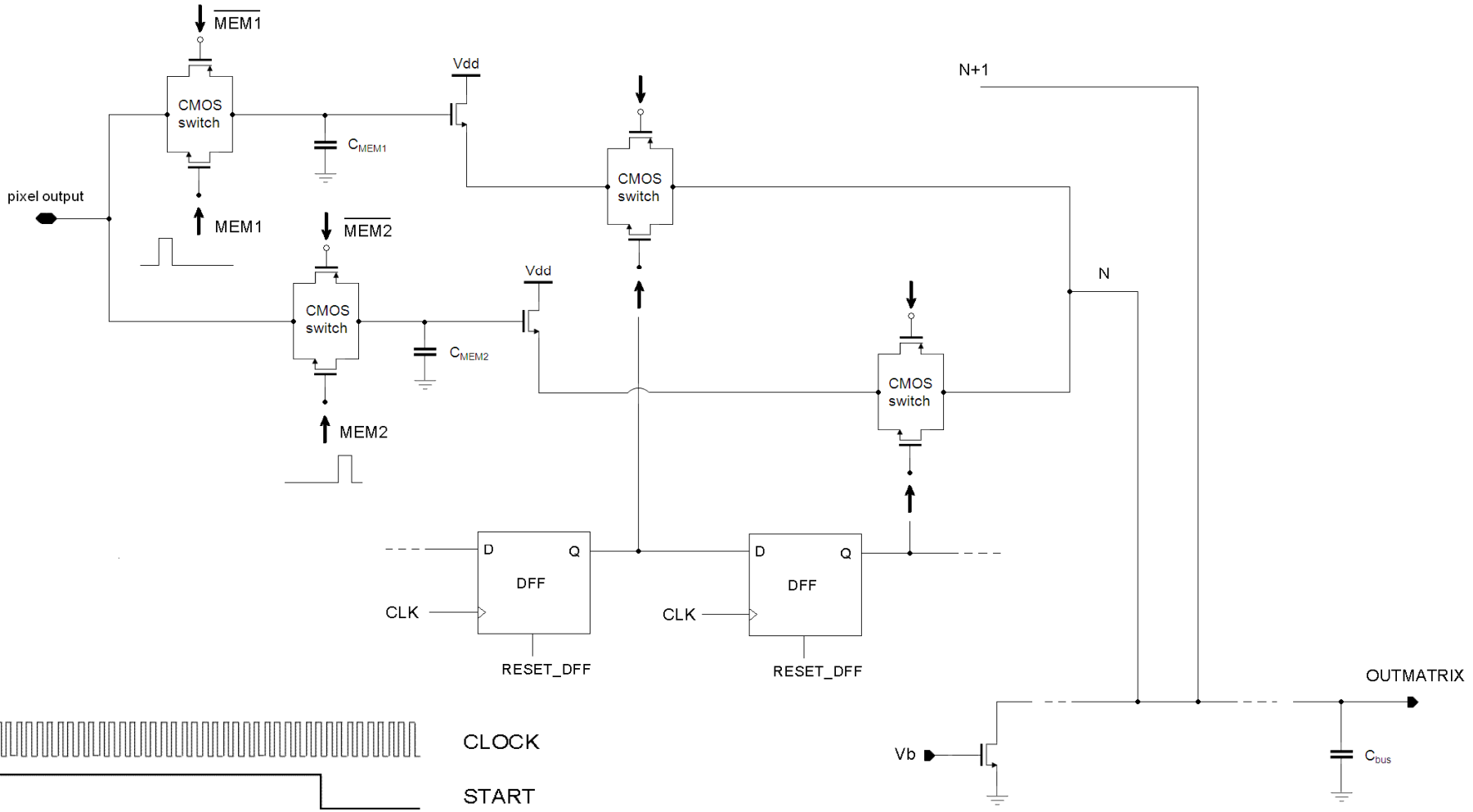
Matrix 1-2 CORE part characterization

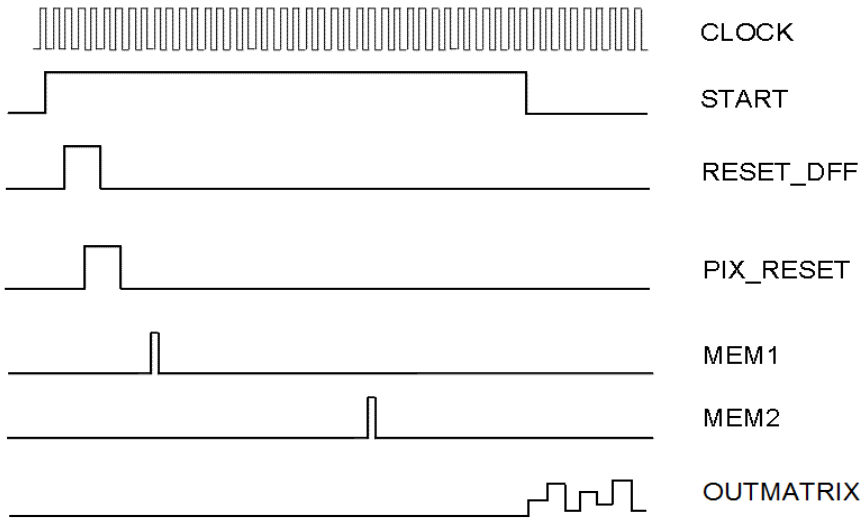
Double sample analog read-out



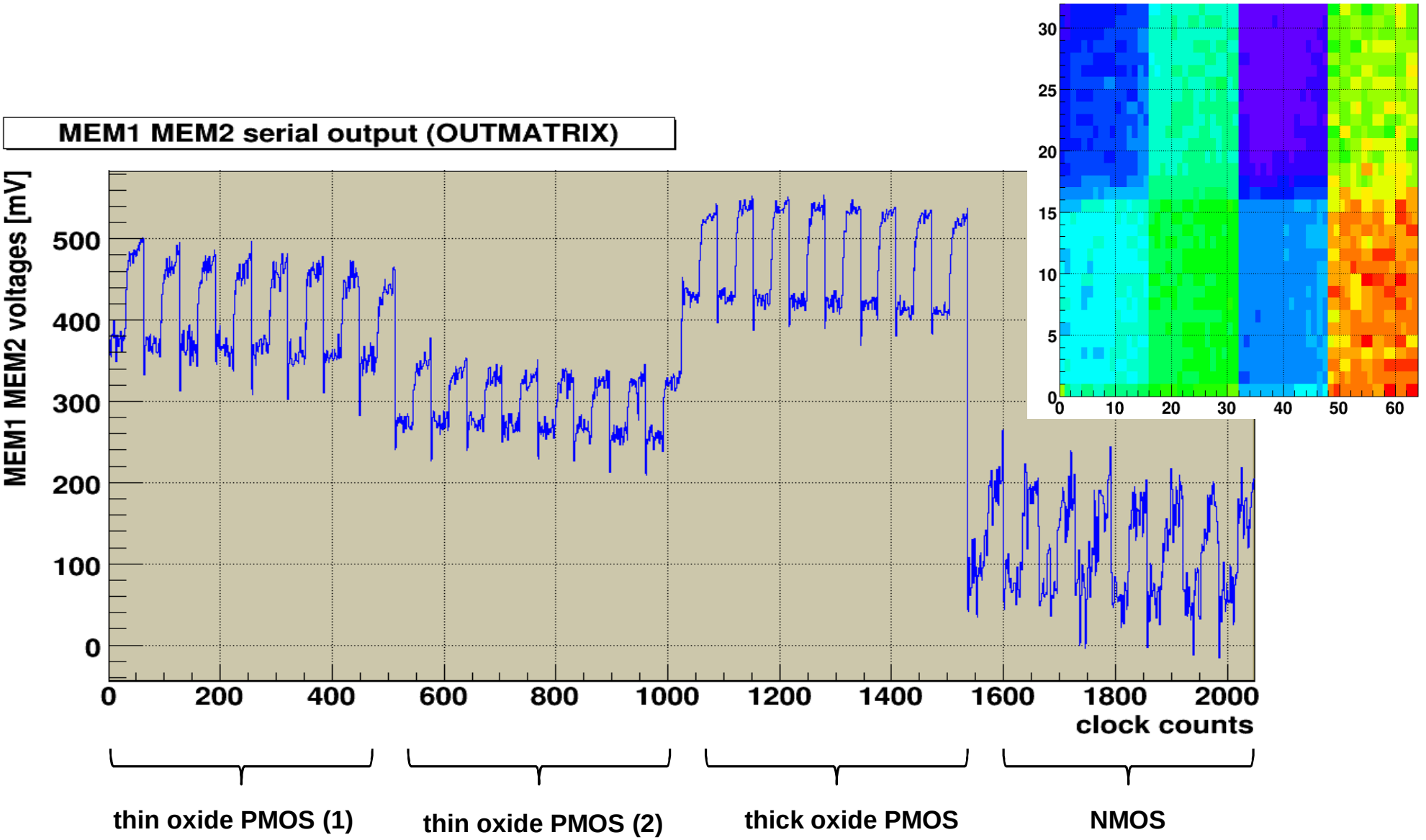
Two analog values are stored for each pixel (**double sample**), the difference between these two voltages corresponds to the signal collected by the sensor.

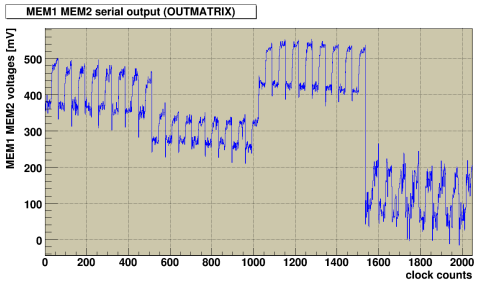
- this is an ***extremely simple read-out scheme***, designed to optimize the sensor characterization (very similar to traditional serial MAPS)


MEM1
CMOS switch
Vdd
N+1
C_{MEM1}
pixel output
MEM1
MEM2
CMOS switch
Vdd
CMOS switch
N
C_{MEM2}
CMOS switch
MEM2
D
Q
DFF
CLK
RESET_DFF
D
Q
DFF
CLK
RESET_DFF
OUTMATRIX
Vb
C_{bus}

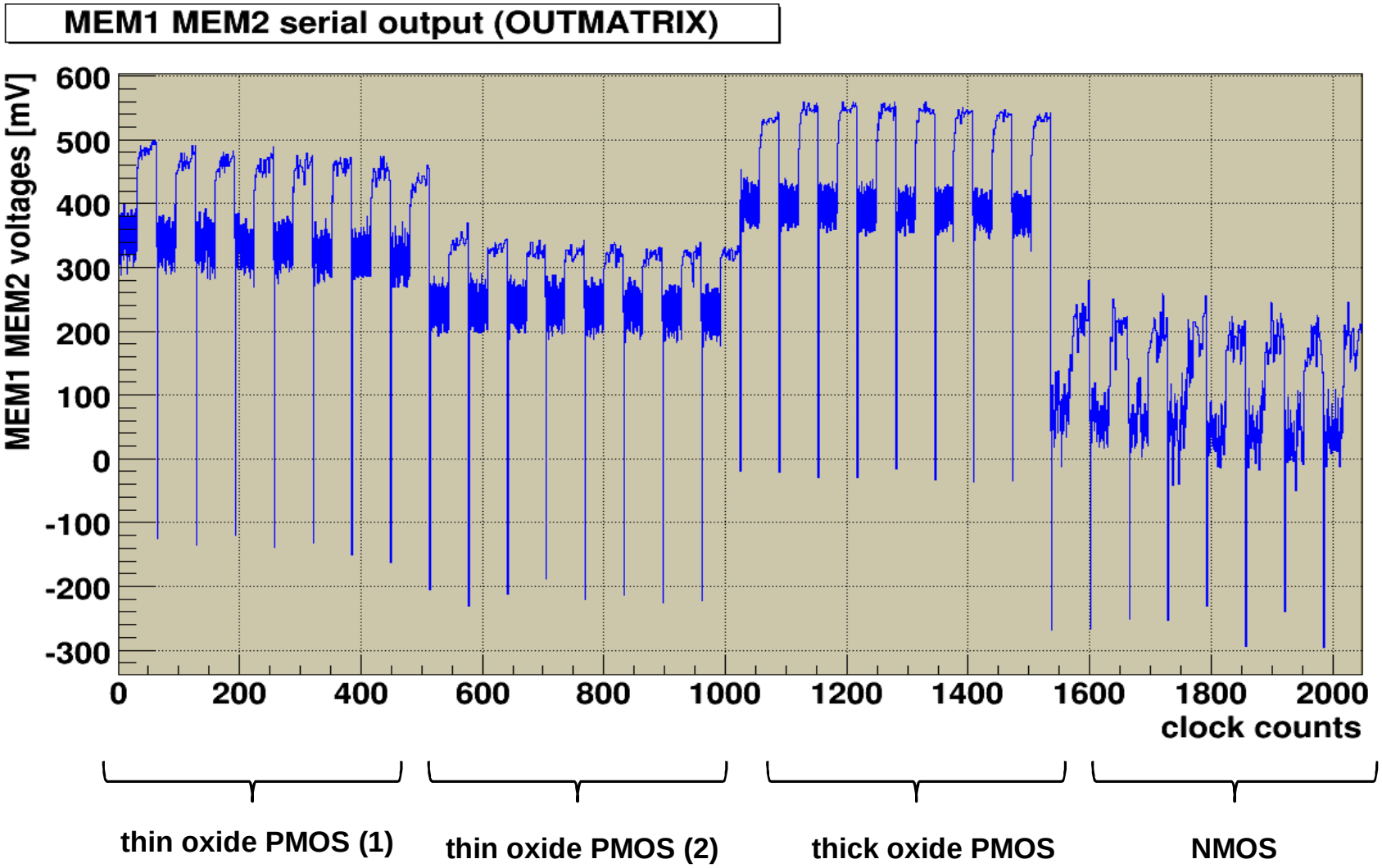

CLOCK
START
RESET_DFF
PIX_RESET
MEM1
MEM2
OUTMATRIX

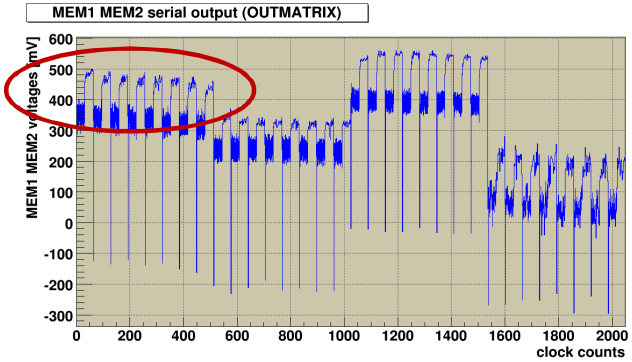
Matrix output no PULSE



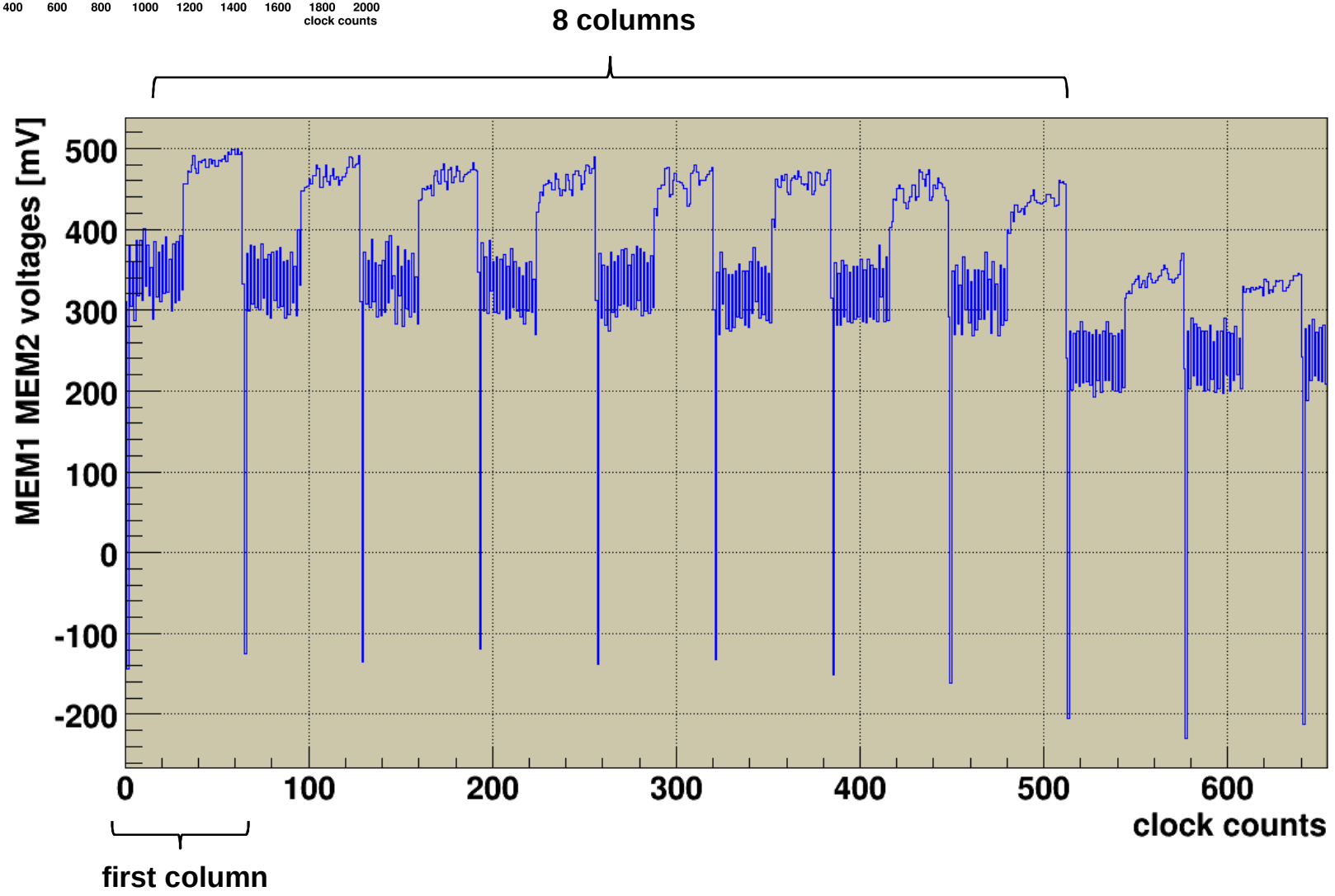


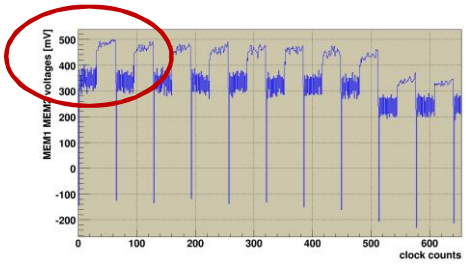
Matrix output with PULSE





Waveform structure (1)





Waveform structure (2)

16 continuous-reset

MEM1 MEM2 voltages [mV]

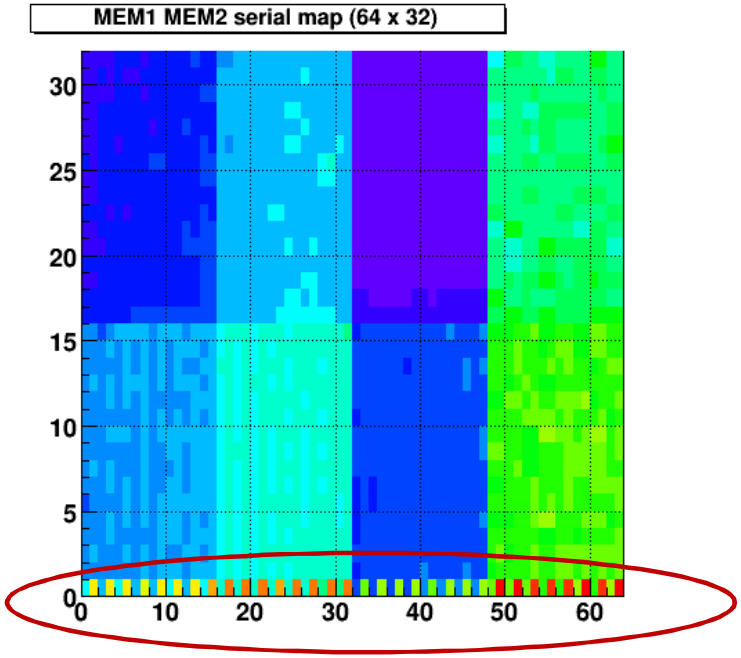
pulsed pixel

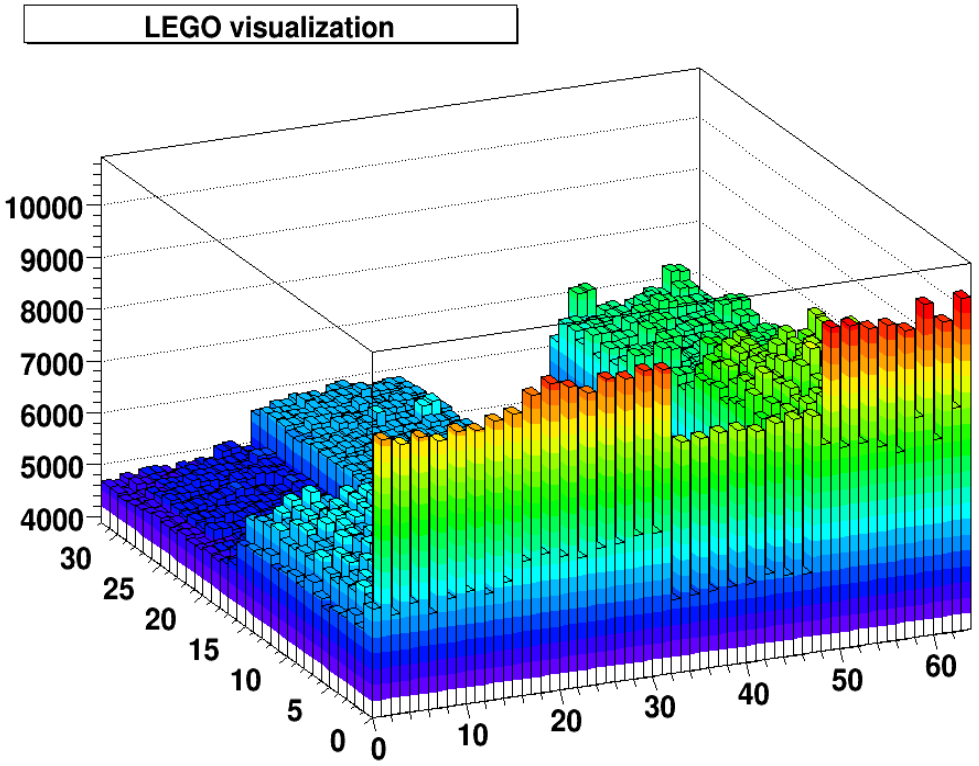
pulsed pixel

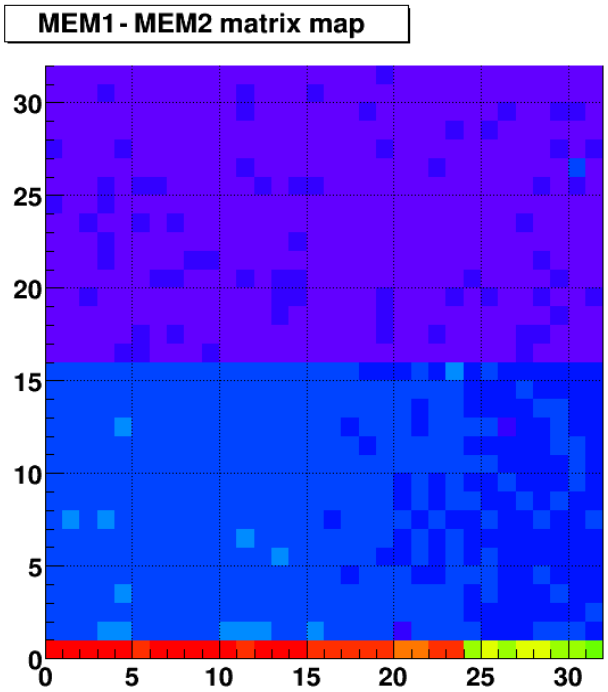
clock counts

16 active-reset

Pulsed rows

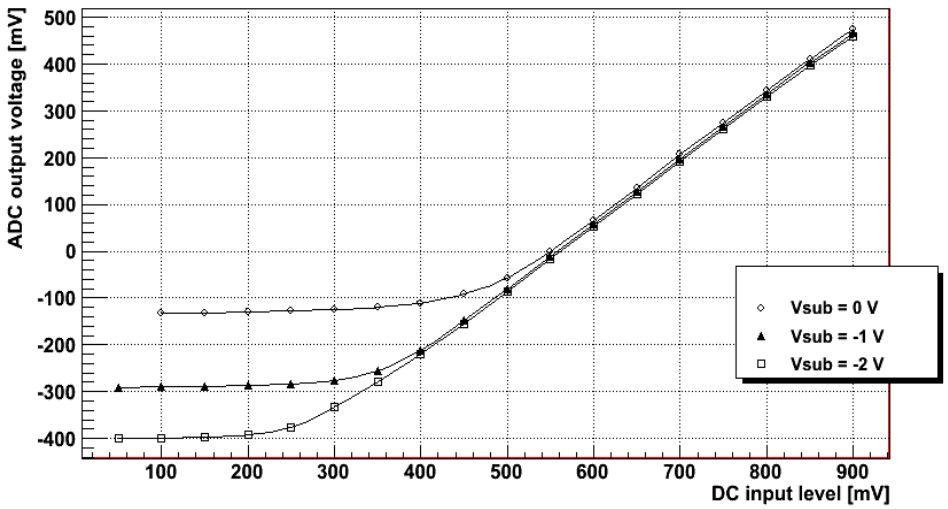

MEM1 MEM2 serial map (64 x 32)
30
25
20
15
10
5
0
0
10
20
30
40
50
60


LEGO visualization
10000
9000
8000
7000
6000
5000
4000
30
25
20
15
10
5
0
0
10
20
30
40
50
60

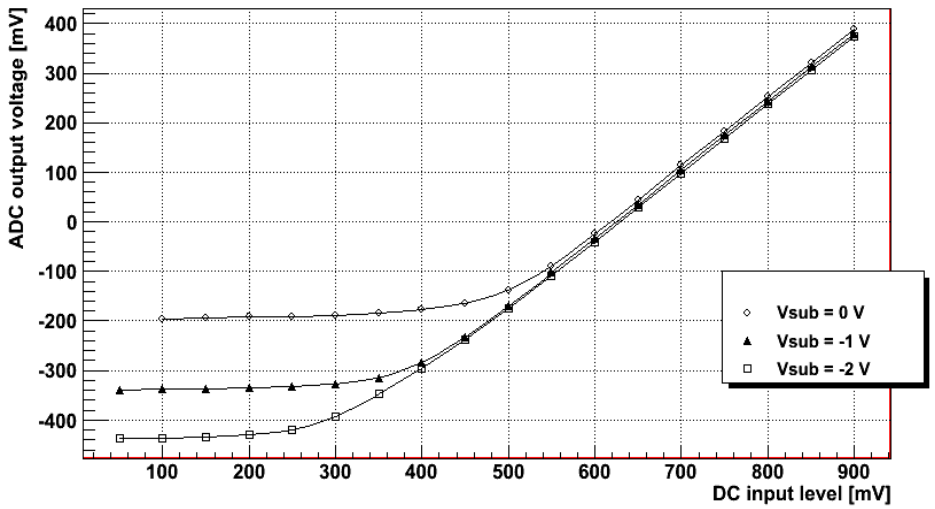

MEM1 - MEM2 matrix map
30
25
20
15
10
5
0
0
5
10
15
20
25
30

SFs DC analysis

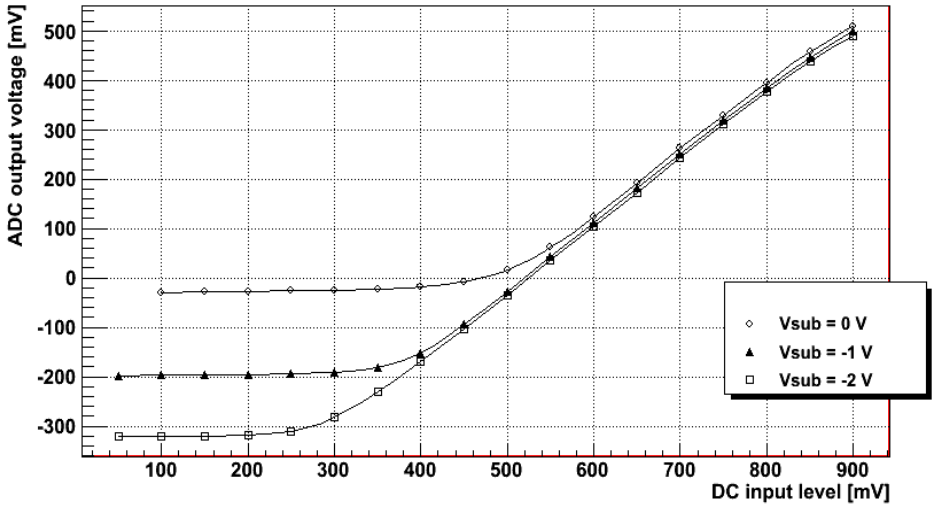
Active reset thin oxide PMOS (1)



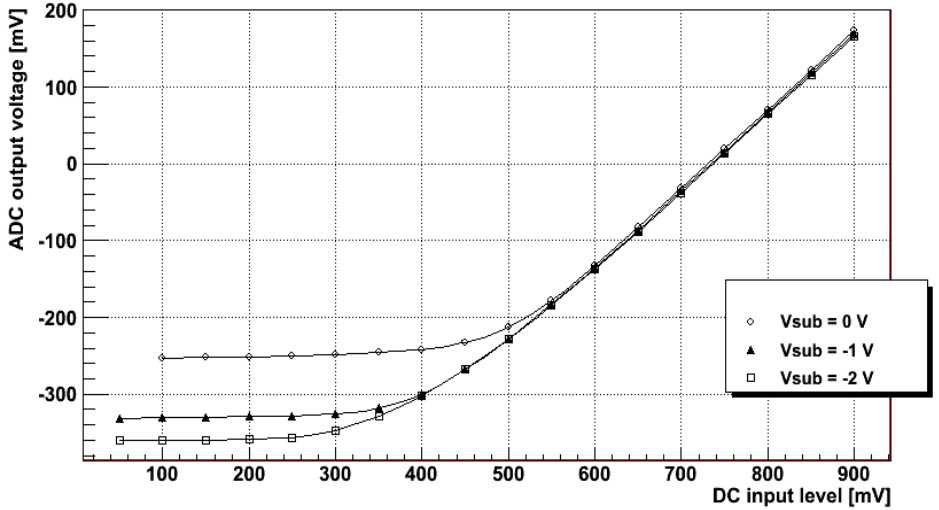
Active reset thin oxide PMOS (2)



Active reset thick oxide PMOS

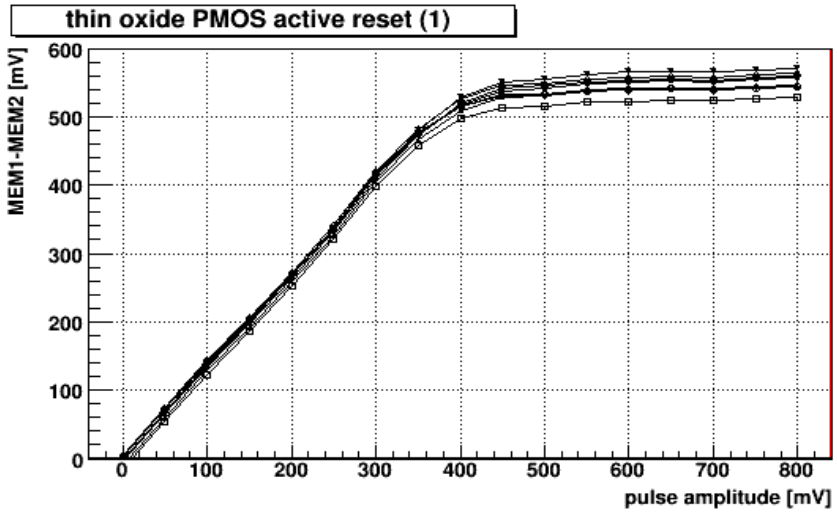


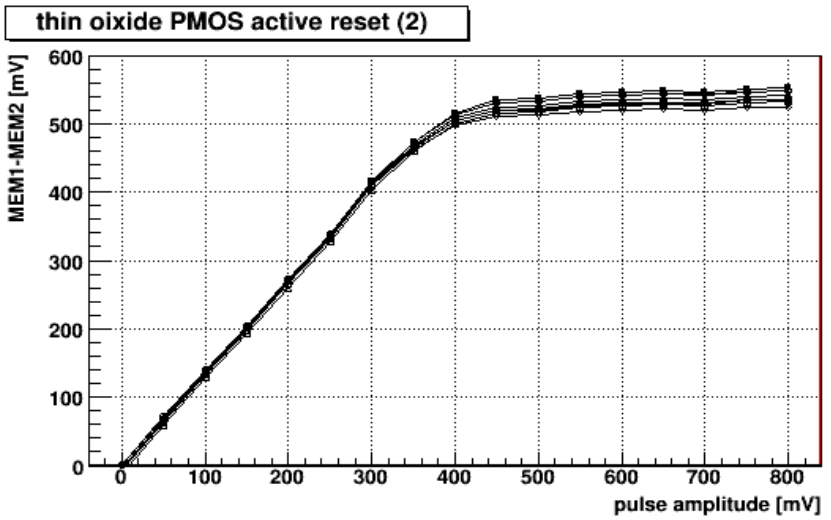
Active reset NMOS

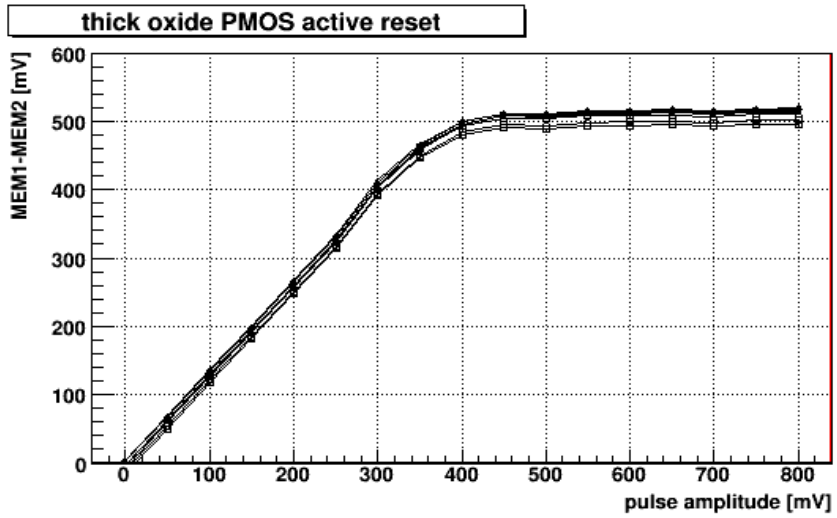


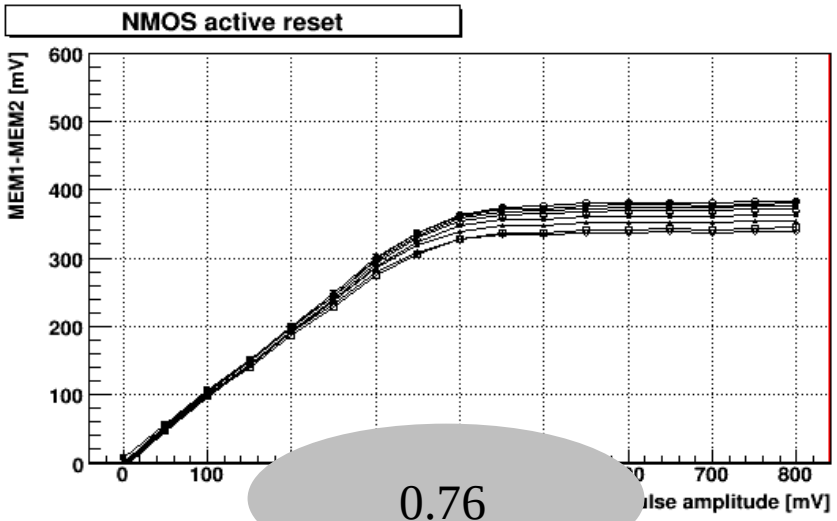
$0.87 \div 0.89$

SFs gain (active-reset)





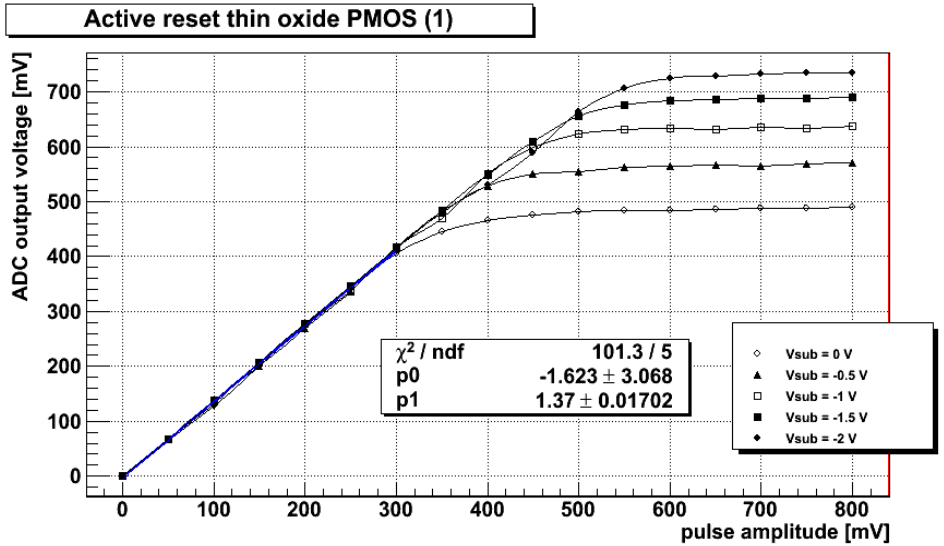


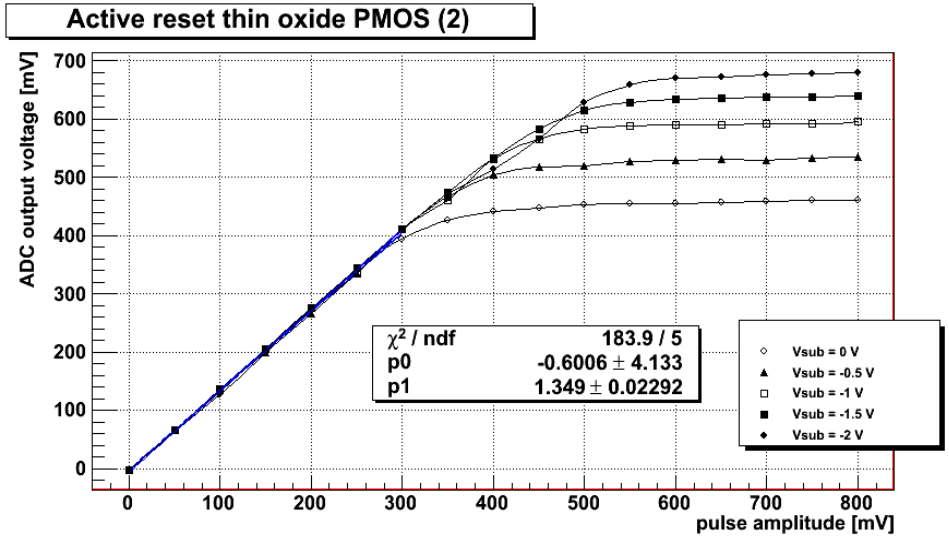


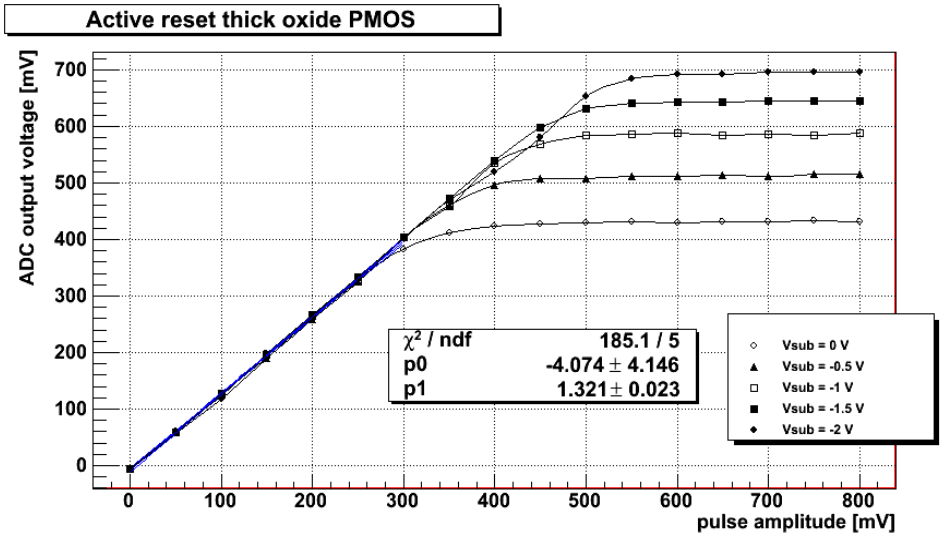
0.76

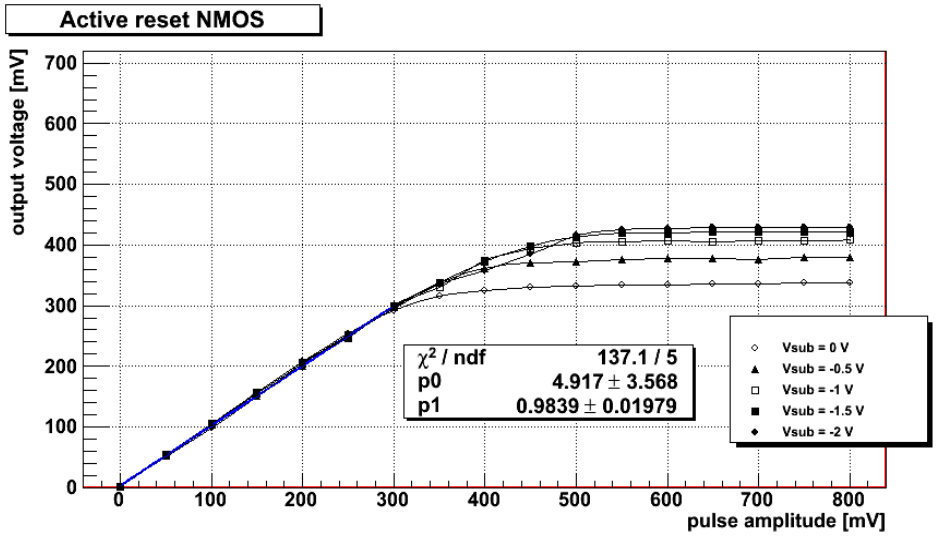
SFs gain vs. reverse bias

f = 100 kHz





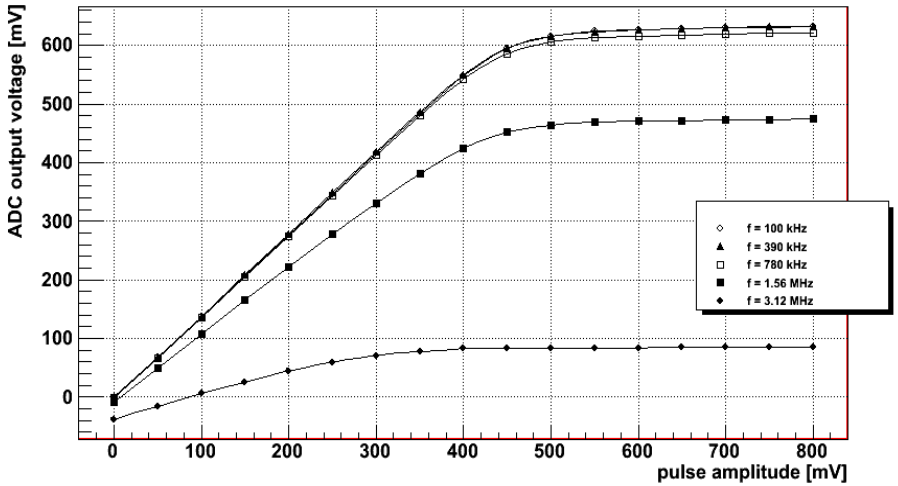




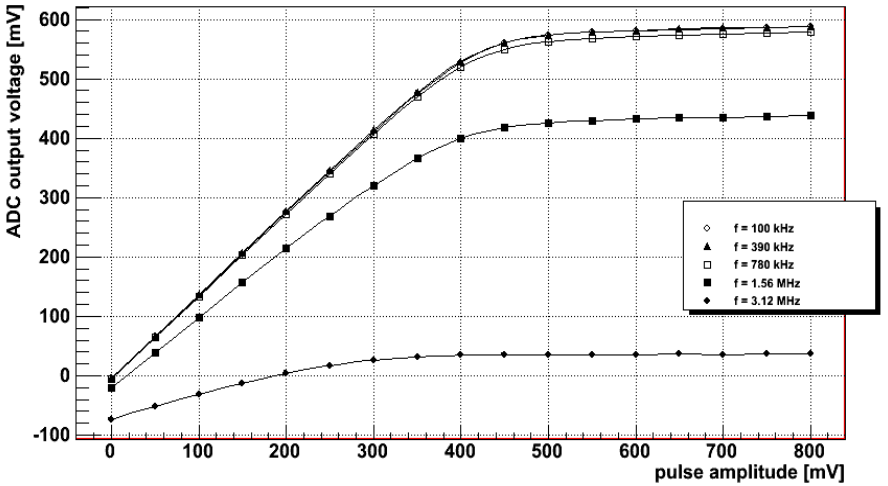
SFs gain vs. frequency

Vsub = -1 V

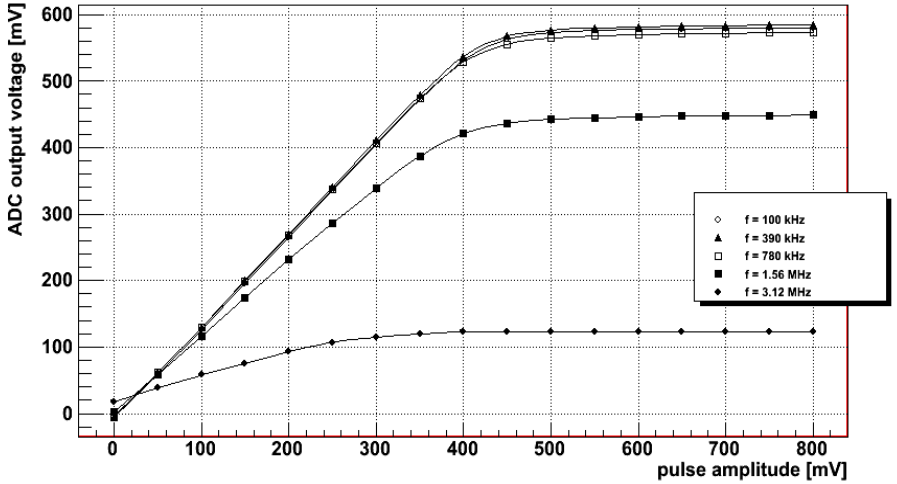
Active reset thin oxide PMOS (1)



Active reset thin oxide PMOS (2)



Active reset thick oxide PMOS



Active reset NMOS