Letter of Intent for RD Collaboration Proposal
Development of pixel readout integrated circuits for extreme rate and radiation

Eckhard Elsen, Chair
LHC Experiments Committee

Feb. 26, 2013

Dear Dr. Elsen,

We intend to submit to the LHCC a proposal for a new CERN RD collaboration to address the major challenges of developing a next generation of pixel readout chips for use at the High Luminosity LHC.

The present hybrid pixel detectors in operation at the LHC represent a major achievement. They deployed a new technology on an unprecedented scale and their success firmly established pixel tracking as indispensable for future HEP experiments. However, extrapolation of hybrid pixel technology to the HL-LHC presents major challenges on several fronts. We propose a new RD collaboration specifically focused on the development of pixel readout Integrated Circuits (IC). The IC challenges include: smaller pixels to resolve tracks in boosted jets, much higher hit rates ($1 GHz/cm^2$), unprecedented radiation levels (10 MGy), much higher output bandwidth, and large IC format with low power consumption in order to instrument large areas while keeping mass low. The IC design communities from ATLAS and CMS have independently reached similar conclusions, and held a joint workshop in November 2012 (http://indico.cern.ch/conferenceDisplay.py?confId=208595). The motivation for a dedicated RD collaboration emerged from this workshop as the most efficient way to resolve the challenges identified. A consensus was reached that this collaboration must be narrowly focused in order to be effective. We note there is presently no plan for ATLAS and CMS to use the same physical IC. This is fully consistent with collaborating on a common RD proposal, because most of the development, test and qualification effort needed is independent of the specific implementation of the final IC's.

In addition to 10 MGy total dose tolerance (driven by the innermost layers), a very high level of fault tolerance to radiation induced single event upsets is needed. These radiation qualification requirements are an order of magnitude larger than for other detectors at HL-LHC. The $1 GHz/cm^2$ hit processing requirement with low power consumption can only be addressed by using the most advanced IC processes we can access (and afford). Studies by several groups have converged on 65nm CMOS as the presently favored technology. A large format pixel IC in 65nm will contain ~500 million transistors, which is more than any single core computer processor ever had (only multi-core processors broke the 1 billion transistor barrier). An IC of this magnitude would need a very large design effort even without considering the extreme radiation tolerance requirement. Such an ambitious goal can only be achieved within our community by pooling resources across experiments and across countries into one focused collaboration. Prototyping in 65nm will also be costly. Through this collaboration we will share submissions to make the best use of limited funding. At CERN further synergy is established with CLIC detector development of a high density pixel IC in 65nm.

We aim to submit a detailed proposal in May 2013. Currently the following institutes have expressed interest in joining: from ATLAS: Bonn, CPPM, LBNL, NIKHEF, New Mexico, UC Santa Cruz; from CMS: CERN, Fermilab, Padova, Perugia, Pisa, PSI, Torino. The anticipated duration of this R&D program is 3 years, after which the experiments will implement final designs and begin fabrication.

Sincerely,

Jorgen Christiansen (CERN, CMS)
Maurice Garcia-Sciveres (LBNL, ATLAS)