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The NA62 experiment: Gigatracker readout architecture

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Overview

The NA62 experiment at CERN SPS aims to collect 80 $K^+ \to \pi^+ \nu\bar{\nu}$ events, in order to obtain a direct measurement of the CKM matrix parameter V_{td}.
A crucial detector of the NA62 experiment is the beam spectrometer named Gigatracker. It consists of three stations of hybrid silicon pixels sensors with an overall 150 ps (rms) time resolution and 100 μm (rms) space resolution. In addition the system will operate under a high radiation environment due to the high density of particles (up to 1.5 MHz/mm^2 in the centre corresponding to 0.8 - 1 GHz in total). The time resolution requirement is very challenging and none of the existing systems has such a capability. To achieve this goal the readout electronics must compensate the discriminator time-walk and the dead time should be below 1%. In order to evaluate the best solution, two readout Application Specific Integrated Circuit (ASIC) designs have been developed. One is based on the constant-fraction discriminator technique and the other one is based on the use of a time-over-threshold circuit. The first one is the object of this thesis and it is widely described in this work.
The layout of the thesis is the following: chapter 1 is a short introduction to the kaon physics and the interest in the mainframe of the Standard Model. The second chapter is dedicated to an overall overview of the physics motivations of the experiment NA62. The chapter 3 contains a description of the NA62 detector, with more details on the Gigatracker system. Chapter 4 is dedicated to the electronics readout of the Gigatracker, with the description of the possible architectures under development. Two ASIC prototypes, which have been submitted in 2009, are presented. More details are given for the in pixel TDC architecture, which it is the object of this work. Finally in chapter 5 the preliminary results on the P-TDC demonstrator ASIC are reported.

Chapter 1

Introduction

Since their discovery by the cosmic radiation [1], K mesons played a very important role in the field of high energy particle physics. In the early 1950s, with the advent of particles accelerators, kaons were studied in details.

A. Pais introduced the *strangeness* [2] to explain the fact that these particles are easily created by strong collisions, but their decay time is much longer than expected by the strong interaction (10^{-10} seconds instead of the expected 10^{-23}). It was thus assigned to each particle type an additive quantum number, S, assuming to be conserved by the strong interactions operating in the production, but violated by the weak interactions at the decay. Moreover antiparticle had to have strangeness opposite to the corresponding particle.

Furthermore it appeared that two types of neutral mesons with opposite strangeness were necessary to cope with the observed reactions at the production stage. The two types of neutral mesons were indicated respectively as K^0 with S=+1, and $\overline{K}^0$ with S=-1. It was then observed that both K^0 and $\overline{K}^0$ could decay, among a large variety of channels, by weak interaction, thus violating the strangeness, into 2 pions, $\pi^+ \pi^-$ and $\pi^0 \pi^0$, or 3 pions, $\pi^0 \pi^0 \pi^0$ and $\pi^+ \pi^- \pi^0$. The decays show two distinct lifetimes: 5.4 x 10^{-8} sec (long-lived) and 8.6 x 10^{-11} sec (short-lived).

From the above experimental observations, Gell-Mann and Pais [3] concluded that neutral kaon states of definite mass (K^0 and $\overline{K}^0$) and neutral kaon states of definite lifetime (K_1: short-lived and K_2: long-lived) could be related by the following relationship:

$$|K_1> \equiv \frac{|K^0> + |\overline{K}^0>}{\sqrt{2}}, \qquad |K_2> \equiv \frac{|K^0> - |\overline{K}^0>}{\sqrt{2}}$$

and $$|K^0> \equiv \frac{|K_1> + |K_2>}{\sqrt{2}}, \qquad |\overline{K}^0> \equiv \frac{|K_1> - |K_2>}{\sqrt{2}}$$

where $K_1 \rightarrow \pi\,\pi$ is allowed and $K_2 \rightarrow \pi\,\pi$ is not permitted. K_2 could decay into 3π. K_1 and K_2 are not expected to have the same decay constant and in fact K_2, which has been observed in 1956 [4], has a lifetime much longer. This is expected due to the phase space volume which is largely different between the 2-pions and 3-pions decays.

The decays of kaons have been fundamental to understand that weak interactions did not conserve parity (P) and charge-conjugation (C).

Following the historical development, it was believed that the eigenvalue of the operator CP has to be conserved, though both separately P and C were not. Based on the decay final states (2 and 3π) of short and long-lived states it was natural assign CP = +1 to K_1 and CP=-1 to K_2. Thus $CP|K_1\rangle = +|K_1\rangle$ and $CP|K_2\rangle = -|K_2\rangle$.

With these assignments and applying CP to K^0 and $\overline{K}^0$, one obtains: $CP\,|K^0> = |\overline{K}^0>$ and $CP\,|\overline{K}^0> = |K^0>$.

In 1964 Christenson, Cronin, Fritch and Turlay studied the decay of the long-lived kaon and detected a substantial probability of decay into two pions. This observation led to the conclusion that CP is violated in weak decays [5]. They measured for the first time the following decay modes ratio:

$$\frac{K_L \rightarrow \pi^+\pi^-}{K_L \rightarrow \text{all charged modes}} = (2.0 \pm 0.4)\times 10^{-3}$$

CP violation implies that T symmetry is broken because of the CPT theorem elaborated in 1954 [6] [7]. This fact has been observed in fundamental interactions that have a privileged time direction, where it was expected to

be invariant under time reversal symmetry (T). In 1967 Sakharov connected this asymmetry with the matter-antimatter asymmetry in the Universe [8] basing his theory on the CP violation observed in kaons decays.

Several explanations to account for the CP violation have been attempted.

It was however evident that the K_1 and K_2, states with definite CP eigenvalue, could not be longer interpreted as *short-lived* and *long-lived* particles. To represent these latter states one needs to introduce K_S and K_L. In a world where CP was conserved $K_S = K_1$ and $K_L = K_2$. In this non-conserving CP world the above equation do not hold, and are modified into:

$$|K_S> \equiv \frac{|K_1> + \varepsilon |K_2>}{(1+|\varepsilon|^2)^{1/2}} \qquad \text{and} \qquad |K_L> \equiv \frac{|K_2> + \varepsilon |K_1>}{(1+|\varepsilon|^2)^{1/2}}$$

where ε, which represents the amount of K_2 (K_1) states in the K_S (K_L), ought to be small ($\sim 10^{-3}$). Even if the CP was conserved in the decay, we would observe a CP-noninvariant component ε.

Without entering in more details, this picture would have required:

$$\varepsilon = \eta_{+-} = \eta_{00} \qquad \text{where} \quad \eta_{+-} = \frac{amplitude K_L \to \pi^+\pi^-}{amplitude K_S \to \pi^+\pi^-}$$

$$\text{and} \qquad \eta_{00} = \frac{amplitude K_L \to \pi^0\pi^0}{amplitude K_S \to \pi^0\pi^0}.$$

It was thus clear that only by establishing a deviation between η_{00} and η_{+-} one could prove the CP-nonconservation of the decay (or direct CP violation). Observables are usually parameterized as follows.

$\eta_{+-} = \varepsilon + \varepsilon'$ and $\eta_{00} = \varepsilon - 2\varepsilon'$

In the recent years several measurements have been performed on the CP-violating ratio *Re*(□'/□): a deviation from zero would have indicated a direct CP violation. Furthermore, this parameter is strictly related to the elements of the Cabibbo-Kobayashi-Maskawa V^{CKM} matrix [9] and can put a constraint on it.

In the middle of 1980's the NA31 experiment at CERN and E731 at Fermilab performed the first measurement on the *Re*(□'/□) parameter, measuring simultaneously K_L and K_S decays:

$$R \equiv \frac{\Gamma(K_L \to \pi^0\pi^0)/\Gamma(K_S \to \pi^0\pi^0)}{\Gamma(K_L \to \pi^+\pi^-)/\Gamma(K_S \to \pi^+\pi^-)} \cong 1 - 6\,\mathrm{Re}(\varepsilon'/\varepsilon)$$

NA31 measured (23 ± 6.5)□10^{-4} [10], showing the evidence of direct CP violation, while E731 measured (7.4 ± 5.9)□10^{-4} .

After that, new experiments have been constructed in 1990's at CERN (NA48) and Fermilab (KTeV) to measure *Re*(□'/□) with a precision of (1~ 2)□10^{-4}, collecting the following results:

- NA48 (14.7 ± 2.2)□10^{-4} [11]
- KTeV (19.2 ± 2.1)□10^{-4} [12]

In the following years the NA48 experiment also studied other rare decays of K_S (in 2002 under the name of NA48/1) and K^+ K^- (in 2003-2008 under the name of NA48/2) and the KTeV experiment completed this research program on the rare decays of kaons with the study of K_L (2008).

Other important studies performed on the K^+ decays have been done at Brookhaven AGS by the experiments E787 and E949. They collected in total seven events of the rare decay $K^+ \to \pi^+ \nu\bar{\nu}$ measuring a branching ratio of $(1.73^{+1.15}_{-1.05}) \times 10^{-10}$ [13], in accordance with the Standard Model (SM) prediction of $(0.85 \pm 0.07) \times 10^{-10}$ [14]. These rare kaons modes offer a big opportunity to study the Standard Model and allow a clean determination of the important parameter V_{td} of the CKM matrix. For this a new experiment (called NA62) is under construction at CERN Super Proton Synchrotron (SPS) with the goal of collecting at least 80 $K^+ \to \pi^+ \nu\bar{\nu}$ events.

Chapter 2

Physical motivations

The research program of the NA62 experiment at CERN SPS is to measure the Branching Ratio by accumulating a statistics of 80 $K^+ \to \pi^+ \upsilon\bar{\upsilon}$ events or more, with a signal to background ratio of (*S/B*) 10:1, in two years of data taking [15].

2.1 The $K^+ \to \pi^+ \upsilon\bar{\upsilon}$ decay and the Standard Model

The study of the rare decays $K^+ \to \pi^+ \upsilon\bar{\upsilon}$ and $K_L \to \pi^0 \upsilon\bar{\upsilon}$ can give important information on the Standard Model and the Cabibbo-Kobayashi-Maskawa matrix (CKM) [9], completing the results coming out from the B physics. This process is extremely attractive because their rates (small but not negligible) can be calculated in terms of Cabibbo-Kobayashi-Maskawa CKM angles.

The CKM matrix, which connects the weak eigenstates (*d', s', b'*) and the corresponding strong eigenstates, describes the probability of transition between quarks and is defined as follows:

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \begin{pmatrix} d \\ s \\ b \end{pmatrix} \equiv \hat{V}_{CKM} \begin{pmatrix} d \\ s \\ b \end{pmatrix}$$

There are several parameterizations of the CKM matrix in literature, but for present discussion it's convenient to use the Wolfenstein parameterization [16], where the basic parameters are:

$$\lambda, \qquad A = \frac{|V_{cb}|}{\lambda^2}, \qquad \bar{\rho} = \rho(1 - \frac{\lambda^2}{2}), \qquad \bar{\eta} = \eta(1 - \frac{\lambda^2}{2})$$

In this parameterization each element of the CKM matrix is expanded as a power series in the small parameter $\lambda = |V_{us}| \approx 0.22$.

$$\hat{V}_{CKM} = \begin{pmatrix} 1-\frac{\lambda^2}{2} & \lambda & A\lambda^3(\rho - i\eta) \\ -\lambda & 1-\frac{\lambda^2}{2} & A\lambda^2 \\ A\lambda^3(1-\rho-i\eta) & -A\lambda^2 & 1 \end{pmatrix} + O(\lambda^4)$$

Because of the smallness of λ and the fact the expansion parameter is λ^2, it's normally sufficient to consider only the first few terms in the expansion. The diagonal elements are close to unity, $|V_{cd}|$ and $|V_{us}|$ of the order 0.2, the elements $|V_{cb}|$ and $|V_{ts}|$ of the order $4\ 10^{-2}$, $|V_{ub}|$ and $|V_{td}|$ of the order $5\ 10^{-3}$. The constraints of unitarity for the CKM matrix can be written as follows:

$\sum_k |V_{ik}|^2 = 1$ for the diagonal elements

$\sum_k V_{ik} V_{jk}^* = 0$ for the other elements

This implies a set of equations, but for the present purpose we can use:

$$V_{us}^* V_{ud} + V_{cs}^* V_{cd} + V_{ts}^* V_{td} = 0$$

which identifies a unitarity triangle on the complex plane (ρ,η).

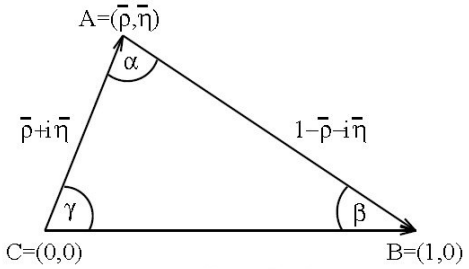

Fig.2.1 *Unitarity triangle*

At the quark level, in the Standard Model, the two decays $K^+ \to \pi^+ \upsilon\bar{\upsilon}$ and $K_L \to \pi^0 \upsilon\bar{\upsilon}$ come from the $s \to d\nu\bar{\nu}$ process and they are described by the Z_0 penguin and the box diagram with a double W exchange.

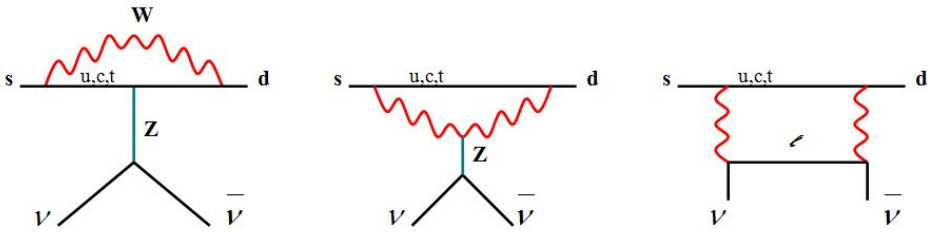

Fig.2.2 *Rare K decays in the Standard Model.*

The active GIM mechanism implies on the decay amplitude the approximation $A_q \approx \frac{m_q^2}{M_W^2} V_{qs}^* V_{qd}$ (where q are the *up*, *charm* or *top* quarks, u, c, t). For the mass values and the CKM elements involved, it's clear that the up-quark contribution is always negligible, while the top-quark dominates the process (the charm-quark has a smaller contribution in the decay $K^+ \to \pi^+ \upsilon\bar{\upsilon}$). Since this is a short-distance process it can be described by a Fermi-like coupling with the following effective Hamiltonian:

$$\mathrm{H}_{eff} = \sum_{l=e,\mu,\tau} \frac{G_l}{\sqrt{2}} (\bar{s}d)_{V-A} (\overline{\upsilon_l} \nu_l)_{V-A}$$

where G_l , the effective coupling constant, is the sum of two elements, arising from the top-quark and the charm-quark:

$$G_l = \frac{\alpha\, G_F}{2\,\pi \sin^2 \Theta_W} [\, V_{ts}^* V_{td} X(x_t) + V_{cs}^* V_{cd} X_{NL}^l \,]$$

where $x_t = \frac{m_t^2}{M_W^2}$. The coefficients $X(x_t)$ and X_{NL}^l, which encode the top and the charm-quark contributions, are calculated at NLO level [17, 18, 19]. The top-quark part is precisely computed, with a small error arising from the uncertainty of the top-quark mass. The smaller part of the charm-quark has the largest theoretical uncertainty, which cause an error of ~5-7% on the determination of V_{td}. With the given definitions the branching fraction of $K^+ \to \pi^+ \upsilon\bar{\upsilon}$ and $K_L \to \pi^0 \upsilon\bar{\upsilon}$ can be written as:

$$BR(K^+ \to \pi^+ \upsilon\bar{\upsilon}) = 6 r_{k^+} BR(K^+ \to \pi^0 e^+ \upsilon) \frac{|G_l|^2}{G_F^2 |V_{us}|^2}$$

$$BR(K^0 \to \pi^0 \upsilon\bar{\upsilon}) = 6 \frac{\tau_{K_L}}{\tau_{K^+}} r_{K_L} BR(K^+ \to \pi^0 e^+ \upsilon) \frac{(\mathrm{Im} G_l)^2}{G_F^2 |V_{us}|^2}$$

The measurement of both branching ratios would provide two independent elements on the unitarity triangle. $BR(K^+ \to \pi^+ \upsilon\bar{\upsilon})$ defines an ellipse in the $\bar{\rho} - \bar{\eta}$ plane (the charm-quark contribution to G_l, which depends on V_{cs} and V_{cd}, is a real number) and $BR(K_L \to \pi^0 \upsilon\bar{\upsilon})$ a vertical line (the height of the unitarity triangle).

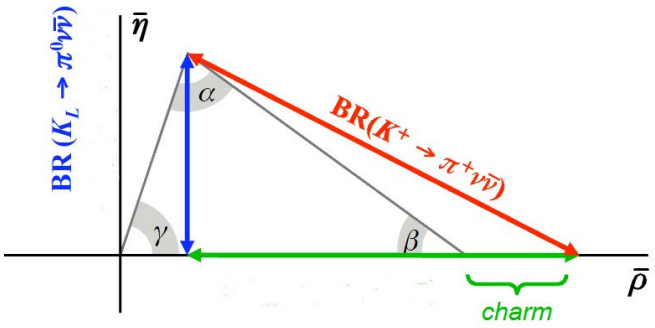

Fig.2.3 *Unitarity triangle and rare K decays.*

Since in the described approximations $V_{ts} = -V_{cb}$ (and the latter is well extracted from *B* decays [20]), the measurement of the two branching ratios for the two kaon decays, will provide a direct measurement of the G_l coupling constant and thus the determination of the V_{td} parameter. In addition combing these measurements with the existing data on the β angle and the $B^0 \bar{B}^0$ oscillations, it will perform an exhaustive test on the Standard Model (for a detailed review of the CKM matrix and the rare kaon decays, please refer to [21] and [22]).

At the present the theoretical predictions for the two branching ratios within the Standard Model are:

$$K^+ \to \pi^+ \upsilon\bar{\upsilon} = (0.85 \pm 0.07) \times 10^{-10} \quad [14]$$

$$K_L \to \pi^0 \upsilon\bar{\upsilon} = (3.0 \pm 0.6) \times 10^{-11} \text{ [22]}$$

Preliminary experimental results for the K^+ decay are given by the E787 and E949 collaborations at Brookhaven National Laboratory:

$$BR(K^+ \to \pi^+ \upsilon\bar{\upsilon}) = (1.73^{+1.15}_{-1.05}) \times 10^{-10}$$

(which are based on seven events in the entire E787+E949 data sample [13]).

For the K_L decay un upper limit has been set by the experiment E391a at KEK 12-GeV proton synchrotron [23]:

$$K_L \to \pi^0 \upsilon\bar{\upsilon} < 6.7 \times 10^{-8} \text{ (90\% C.L.)}$$

In this general framework the NA62 experiment will play an important role in the following years, completing these results.

2.1 Other physics opportunities

The new experimental setup for the NA62 experiment will provide an excellent resolution on the photon energy that will allow the study of radiative kaon decays with a precision never reached before. In addition the experimental apparatus can be used for many measurements on others rare kaon decays.

Moreover the study of rare kaon decays can give important inputs for physics beyond the Standard Model. The $BR(K^+ \to \pi^+ \upsilon\bar{\upsilon})$ measured at Brookhaven seems to be larger than the predicted value within the Standard Model. A possible interpretation of this result can be found in the supersymmetric models, replacing the W boson with new particles like *charged Higgs*, *charginos* and *stops*. Possible scenarios of new physics contributions in the $s \to d\bar{\nu}\nu$ amplitude and in $B\bar{B}^0$ mixing are described in [24].

2.2 Principle of the experiment

The goal of the experiment is to collect at least 80 $K^+ \to \pi^+ \nu\bar{\nu}$ events in two years with a signal to background ratio S/B=10:1. Considering the impossibility to measure the two neutrinos in the final state, the experiment requires an adequate strategy to optimize the kinematic measurements and the veto system. The main source of background, arising from the two body decays, mainly $K^+ \to \pi^+\pi^0$ and $K^+ \to \mu^+\nu$, which have branching ratios 10^{10} times larger than the expected signal, must be suppressed. Also, the reconstruction of the two-body kinematics, can be done only with a precise photon detection in conjunction with a good Particle Identification (PID). In addition also the three-body decays give a contribution to the background and they must be taken in account. The following table shows the K^+ decay modes that can contribute to the background and the rejection handles.

Decay mode	Branching ratio	Background rejection
$K^+ \to \mu^+\nu$	63% (called $K_{\mu 2}$)	μ PID, two-body kinematics
$K^+ \to \pi^+\pi^0$	21%	Photon veto, two-body kinematics
$K^+ \to \pi^+\pi^+\pi^-$	6%	Charged particle veto, kinematics
$K^+ \to \pi^+\pi^0\pi^0$	2%	Photon veto, kinematics
$K^+ \to \pi^0\mu^+\nu$	3% (called $K^+_{\mu 3}$)	Photon veto, μ PID
$K^+ \to \pi^0 e^+\nu$	5% (called K^+_{e3})	Photon veto, E/p

Table 2.1 *K^+ decay modes and rejection criteria.*

The kinematic of the decay under study can be represented as follows.

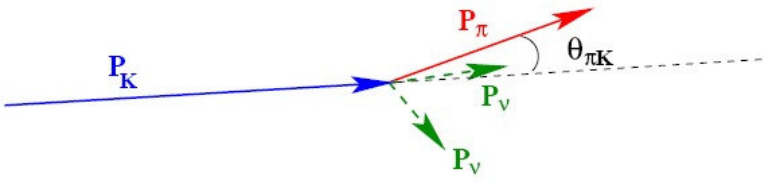

Fig. 2.4 *Kinematics of $K^+ \to \pi^+\nu\bar{\nu}$.*

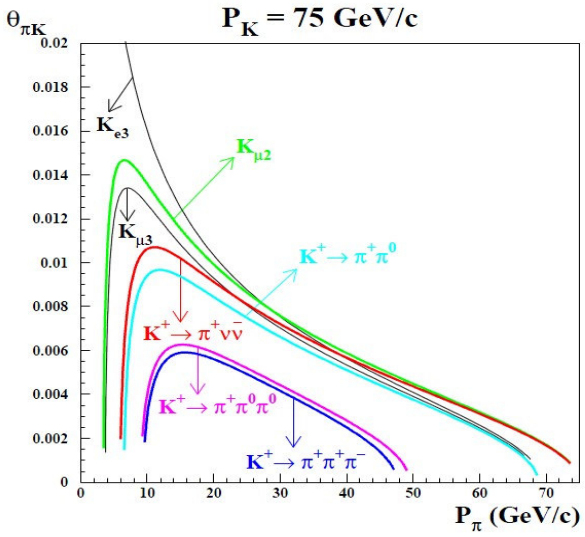

Fig. 2.5 Angle-*momentum relation for* K^+ *decays.*

The measurable quantities are: the momentum of the incoming K^+ (P_K), the momentum of the outgoing π^+ (P_π), and the angle between them ($\theta_{\pi K}$). In order to separate the signal from the background, two acceptance regions can be defined. Under the hypothesis that the charged final state is a pion and the angle $\theta_{\pi K}$ is small one can define the squared missing mass, m^2_{miss}, as:

$$m^2_{miss} \cong m^2_K(1-\frac{|P_\pi|}{|P_K|}) + m^2_\pi(1-\frac{|P_K|}{|P_\pi|}) - |P_K||P_\pi|\theta^2_{\pi K}$$

Assuming $P_K = 75\ GeV$ /c, corresponding of the central value of the beam momentum at the CERN SPS, m^2_{miss} distributions for the signal and for the other most probable K^+ decays are somewhat in overlapping regions. In particular the squared missing mass of $K^+ \to \pi^+\pi^0$ has a fixed value of $m^2_{miss} = m^2_{\pi^0}$ (represented by a line) which is in the signal region. To cut out the 2-pion decays, the acceptance area must be divided in two regions (where Δm depends on the m^2_{miss} resolution):

- Region I: $0 < m^2_{miss} < m^2_{\pi^0} - (\Delta m)^2$

- Region II: $m_{\pi^0}^2 + (\Delta m)^2 < m_{miss}^2 < \min[m_{miss}^2(\pi^+\pi^+\pi^-)]$

The definition of Region II also rejects the three body decay $K^+ \to \pi^+\pi^+\pi^-$ (see Fig. 2.6).

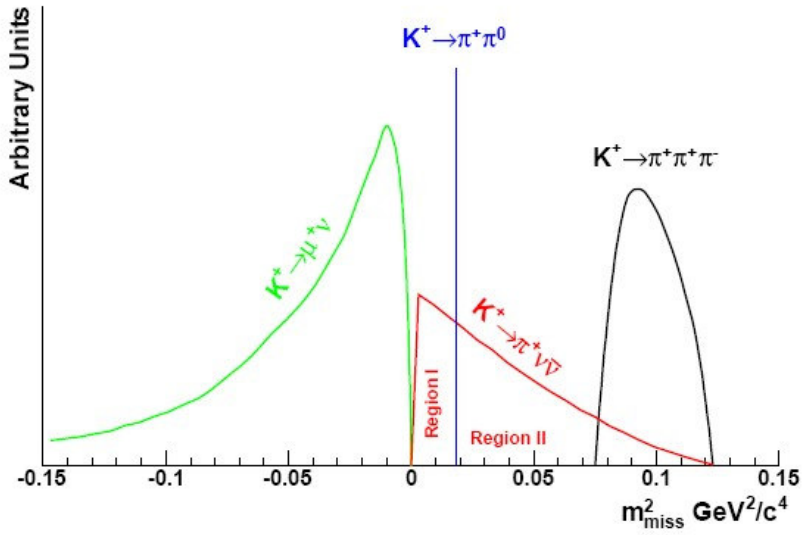

Fig. 2.6 *Squared missing mass distributions.*

Simulations show that to reach $S/B \geq 10$ it is necessary to fix the squared missing mass resolution at $(\Delta m)^2 \approx 8\times10^{-3} GeV^2/c^4$ [15]. This value puts the constraints on the required performance of the two spectrometers which take part of the NA62 detector (refer to Chapter 3 for details). Also, to suppress the background arising from most probable K^+ decays, the detector should provide an efficient γ detection to reject π^0 decays. Finally π^- and μ^+ can be suppressed respectively with the wrong-charge deflection and particle identification, as explained in detail in the next chapter.

Chapter 3

Experimental apparatus

NA62 is a fixed target experiment making use of the proton beam of the CERN SPS to produce the K^+ flux. The following picture is the section view of the entire detector, where the proton beam comes from the left. In this chapter it will be given a description of each sub-detector, focusing more on the Gigatracker system which is the object of the present work.

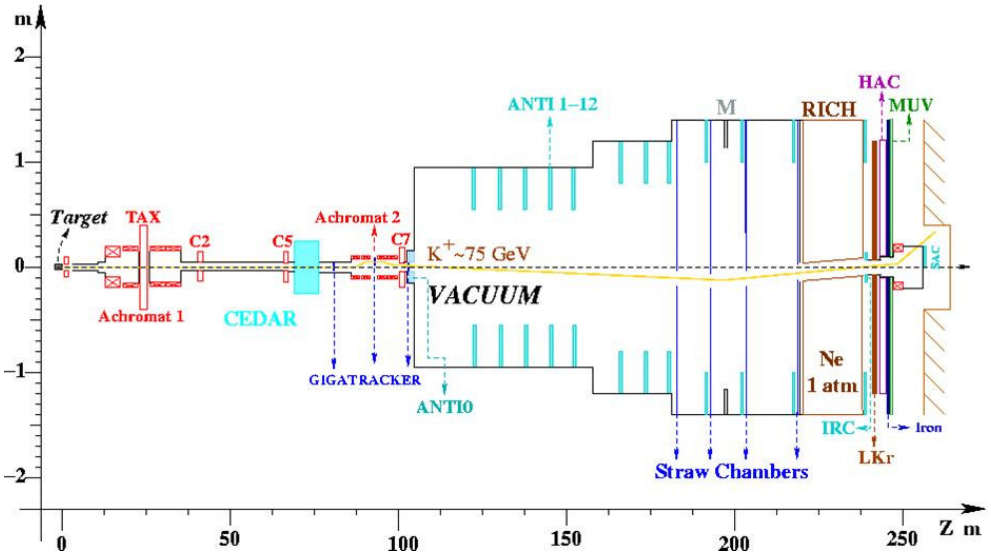

Fig. 3.1 *Detector view.*

To better understand Fig. 3.1 refer to the acronyms list below:

- CEDAR: Cherenkov Differential counter with Achromatic Ring focus
- GIGATRACKER: silicon pixel detectors for momentum and time measurements

- ANTI: Anti-counters (Large Angle photon Veto)
- RICH: Ring Imaging Cherenkov detector
- LKr: Liquid Krypton calorimeter
- IRC: Intermediate Ring Calorimeter (photon veto)
- SAC: Small Angle Calorimeter (photon veto)
- HAC: the NA48 Hadronic Calorimeter (muon veto)
- MUV: MUon Veto system

3.1 The beam for the experiment

The charged kaon beam for the experiment is derived from the primary proton beam at 400 GeV/c of the SPS colliding a beryllium target. The high energy of the primary beam gives some advantages. With the use of an empirical formula [25] can be calculated that the maximum K^+ production, per primary proton of fixed momentum p_0, occurs for $p_K \approx 0.35\, p_0$ (0.23 for K^-). In addition K^+ (K^-) production increases as p_K^2 (and so as p_0^2). It can be calculated that the maximum number of K^+ decays, in the defined length range constrained by the detector geometry, is maximum when $p_K \approx 0.23\, p_0$ (0.15 for K^-) and it increases as p_K (and therefore as p_0). Moreover, at high energy, detectors like calorimeters, photon veto counters and muon detectors, have better performances in terms of acceptance, resolution, and efficiency. The choice of a positive kaon beam is motivated by the ratio of the production rates: $K^+/K^- \approx 2.1$ (per 400 GeV/c proton beam).

A kaon momentum of 75 GeV/c has been chosen as central value. This is a compromise of the parameters listed in table 3.1. The number of produced K^+ and the percentage in the beam increases with the momentum, but there are other aspects to take into consideration: the distance of the decay region (102 m from the target), the length of decay region itself, 50 m, and the detector acceptance: particles near the beam pipe can not be detected. The kaon fluxes listed in table 3.1 are the results of the combinations between

measured particle rates and the estimation made with the use of an empirical formula [25].

p_K [GeV/c]		60	**75**	120
Fluxes at production:	p x 10^6	89	171	550
(10^{12} incident proton per s)	K^+ x 10^6	40	53	71
	π^+ x 10^6	353	532	825
	Total x 10^6	482	756	1446
Survival factor over 102 m	K^+	0,797	0,834	0,893
	π^+	0,970	0,976	0,985
Fluxes at 102 m from target:	p x 10^6	89	173	550
(10^{12} incident proton per s)	K^+ x 10^6	32	45	63
	π^+ x 10^6	343	525	813
	Total x 10^6	464	743	1426
Decays in 60 m fiducial length:	K^+ x 10^6	3,9	**4,5**	4,1
(10^{12} incident proton per s)	π^+ x 10^6	6,1	7,4	7,2
K^+ decays / π^+ decays in 60 m		**0,64**	0,61	0,57
K^+ decays in 60 m / total hadron flux x 10^{-3}		**8,4**	6,1	2,9
$K^+ \to \pi^+ \nu\bar{\nu}$ acceptance (Region I, no p_π cut)		0,08	**0,11**	**0,11**
Accepted $K^+ \to \pi^+ \nu\bar{\nu}$ / 10^{12} proton per s x10^6xB.R.		0,31	**0,50**	0,45
Accepted $K^+ \to \pi^+ \nu\bar{\nu}$ / π^+ decays in 60 m x B.R.		0,052	**0,067**	0,062
Accepted $K^+ \to \pi^+ \nu\bar{\nu}$ /total hadron flux x10^{-3}xB.R.		**0,67**	**0,67**	0,31

Table 3.1 *K^+ production and decay parameters for different p_k values.*

The primary proton beam used to produce the K^+ beam, previously has served the experiments NA48 [26] and NA48/2 [27] to produce the K^0_L and the K^+ K^- beams. The extracted 400 GeV/c proton beam from the SPS North Area is split into three branches hitting targets T2, T4 and T6. At the target station T4 a system of magnets provides the transport of protons that have not interacted, up to the experimental cavern ECN3. For a detailed overview of the beam layout refer to [28].

For the extraction of the secondary hadron beam it is planned to reuse the existing target station T10 and to install the new beam along the existing K12 beam line. At T10 the primary protons are focused with zero angle over the beryllium target, which is suspended between aluminium foils and cooled by forced convection. The K^+ momentum selection and positron suppression are performed by a system of quadrupoles and motorized beam collimators (TAX). A listing of the layout and geometry of the new K^+ beam for the NA62 experiment can be found in the *BEATCH* file attached in [28].

3.1.1 K^+ tagging

The secondary beam it is not a pure K^+ beam but many other particle types cause the increment of the flux in the upstream detectors up to 17 times larger than the useful one. For this reason the K^+ particles in the secondary beam must be identified with respect to pions and protons components by the differential Cerenkov counter (CEDAR). The detector is housed in a steel pressure vessel of 558 mm diameter, filled with hydrogen gas [28] at a pressure of about 4 bar.

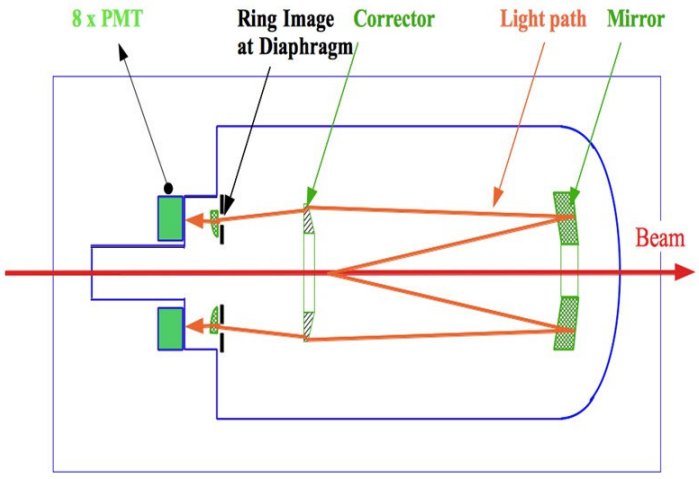

Fig. 3.2 *CEDAR detector.*

The Cerenkov angle of the light produced by the particles traversing the vessel is function of their masses. The light is reflected by a spherical mirror

and detected by eight photomultipliers. The coincidence of at least six of them detects the passage of a particle. Trimming the pressure of the gas it is possible to transmit through the diaphragm only the light produced by a K^+ particle at a given angle, whilst light associated to protons and pions will be stopped. The rate in the detector is limited to 50 MHz, which corresponds to the kaon rate in the beam.

Finally, to increase the efficiency of the light collection, a system of corrector lenses redirect the light rays to the diaphragm with the same radius independently on the wavelength and point of emission.

NA62 will use un update version of the *West CEDAR* built for the SPS secondary beams [29]. The main requirements are listed in table 3.2.

Time resolution	< 100 ps
Number of photons per Kaon	100
Kaon rate	50 MHz
Rate per photomultiplier	3 MHz
Efficiency	> 95%

Table 3.2 *CEDAR main parameters.*

The existing CEDAR must be adapted in order to meet the NA62 specifications. In particular new photodetectors and readout electronics are needed to manage the high kaon rate. As consequence also the light transport system must be re-designed [28]. At the moment the choice of the photodetector is based on a conventional vacuum photomultiplier tube with quartz window (Hamamatsu R7400P).

3.1.2 Beam tracking and momentum measurement

The beam tracking system consists of three stations of silicon pixels detectors, installed in vacuum over the beam line, named Gigatracker. It will be described in detail in section 3.3. Of relevance for the beam is the deflecting system. A pair of quadrupoles match the beam through the three

stations of the Gigatracker and limits the beam size at the downstream detectors. Between the GTK1 and the GTK3 is placed an "achromat" composed of four dipole magnets, vertically deflecting the beam. The yokes of the first three magnets are installed below the beam (down) whereas the fourth is placed above (Up).

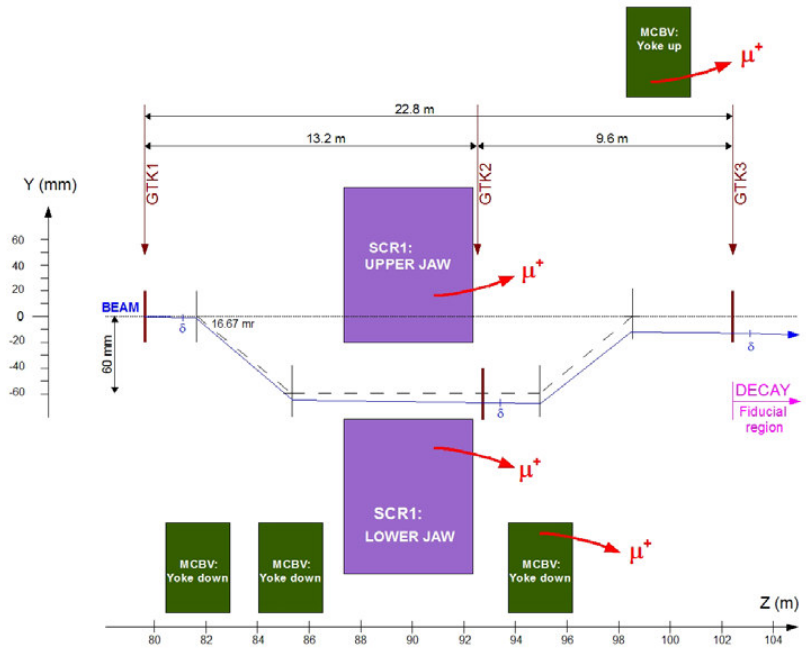

Fig. 3.3 *Schematic layout of the beam tracking and momentum measurement system.*

The effect of the resulting magnetic field is the defocusing action on the μ^+, produced by the iron collimator SCRAPED 1 (SCR1). The lower jaw, placed 20 mm below the beam, deflects away the μ^+ of momenta < 55 GeV/c, which are travelling along the K^+ and π^+ beam at 75 GeV/c. Moreover the upper jaw stops the undeviated particles assuring that no neutrals (K^0_L and neutrons) or negative charged (π^- and K^-) can be transmitted through the downstream detectors. The amount of displacement along the vertical axis of the GTK2 station respect the other two stations

(following the 75 GeV/c beam path) provides the momentum measurement with a resolution of ~ 0,2 %.

3.1.3 Decay region

The decay fiducial region is contained in the first 60 m of the evacuated tank located immediately after the Gigatracker station 3. Then the beam is transported to the downstream detectors through a thin aluminium window traversed by the beam tube (of diameter ~155 mm).

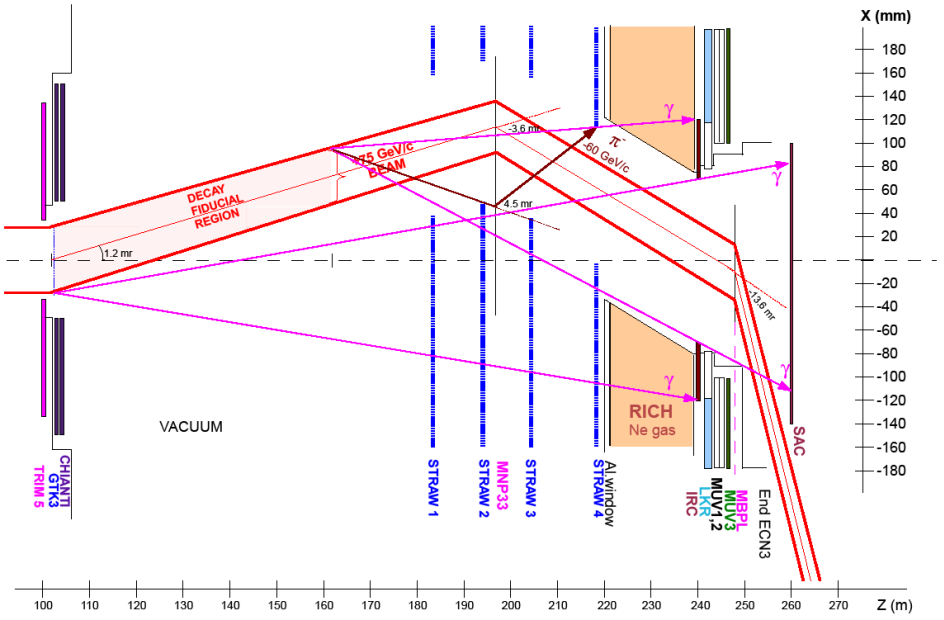

Fig. 3.4 *Vacuum tank and decay fiducial region.*

The detectors installed in the vacuum tank are described in the next sections. But concerning the beam it is important to spend a few words about the single magnetic spectrometer, which is composed by four straw-tubes chambers covering the whole acceptance area except ±60 mm around the beam path. Between the four chamber is installed the dipole magnet MNP33 which deflect the 75 GeV/c beam by –3.6 mrad in order to focus the beam to the undeviated axis at the beginning of the LKr calorimeter. Besides tagging the π^+ candidates from the K^+ decays, the spectrometer detects the π^-

originating from the K^+_{e4} decays ($K^+ \to \pi^+\pi^- e^+\nu$), with momentum up to 60 GeV/c, deflected by the magnet by +4.5 mrad.

At the exit of the LKr calorimeter a pair of filament scintillators provides a further position measurement. The beam is finally deviated by -13.6 mrad to avoid the interaction with the Small Angle Calorimeter (SAC) and then dumped in concrete blocks placed at the end of the cavern ECN3.

3.2 Detector overview

As described in section 2.2 the rate of decay $K^+ \to \pi^+ \upsilon\bar{\upsilon}$ is 10^{10} times lower than the background sources (table 2.1). Therefore an accurate particle identification, a robust photon vetoes system in conjunction with the muon rejection are mandatory for the NA62 detector. Besides that the detector requires a high resolution timing to support the high rate of particles (~800 MHz at the Gigatracker).

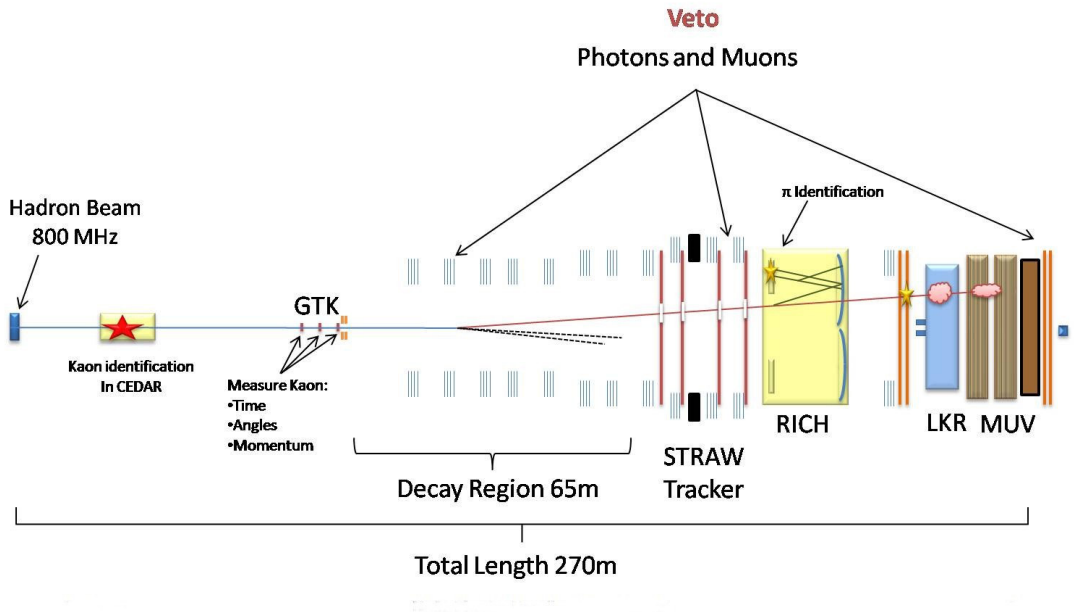

Fig. 3.5 *Detector elements and their function.*

The squared missing mass defined in 2.2 is related to the K^+ and π^+ momenta and defines the acceptance regions for the signal, Region I: $0 < m^2_{miss} < 0.01\ GeV^2/c^4$ and Region II: $0.026 < m^2_{miss} < 0.068\ GeV^2/c^4$.

The 92% of background sources are suppressed by this kinematics selection. The remaining 8% must be rejected by the vetoes systems and the particle identification.

First of all the kaon identification is performed in the CEDAR (section 3.1.1). Then, to reconstruct the squared missing mass, the Gigatracker system provides the measurement of P_{K^+} in conjunction with time and coordinates measurements of all the beam particles before the decay region. In the vacuum tank, the Straw Tracker (Magnetic Spectrometer) performs the measurement, momentum and position, of the charged particles from the K^+ decay. In addition, in the vacuum tank, π^- are suppressed for wrong-charge deflection (Fig. 3.4).

One of the main sources of background (BR: 63.4%) is the decay $K^+ \to \mu^+\nu$ ($K_{\mu 2}$). The required rejection factor of 10^{-12} is reached by the kinematics selection, the muon veto system (MUV) and particle identification performed by the RICH detector. The latter performs the separation between μ and π candidates.

Another important source of background (BR: 20.9%) is the decay $K^+ \to \pi^+\pi^0$ ($K_{\pi 2}$). The required rejection factor of 10^{-12} is achieved by the photon veto system which is composed of three different calorimeters covering different acceptance angles:

- Large Angle (LAV): 10 mrad < acceptance <5 0 mrad
- Medium Angle (Liquid Krypton): 1 mrad < acceptance < 10 mrad
- Small Angle (IRC, SAC): acceptance < 1 mrad.

A further background source can arise from the inelastic interactions in the beam collimators or in the GTK3 station, where the beam particles can generate pions and other particles at a small angle and reaching the Straw Tracker. If no other particles are detected a false K^+ decay can be assumed; in fact it would mimic a K^+ particle decaying into a pion with no other particles. The Charged ANTI (CHANTI) detector tags the inelastic interaction vetoing the charged particles produced at a large angle. This

system of scintillators is placed immediately after the GTK3 station. In addition it provides a further beam halo monitoring and muon halo tagging.
In the following sections is given a detailed description of each sub-detector.

3.3 The Gigatracker

3.3.1 System architecture and requirements

The Gigatracker (GTK) is one of the key elements for the NA62 experiment. It has to provide a precise time, angle, and momentum measurement of all the incoming particles in the 75 GeV/c beam.
The GTK is composed of three stations of hybrid silicon pixels sensors mounted around four dipole magnets.

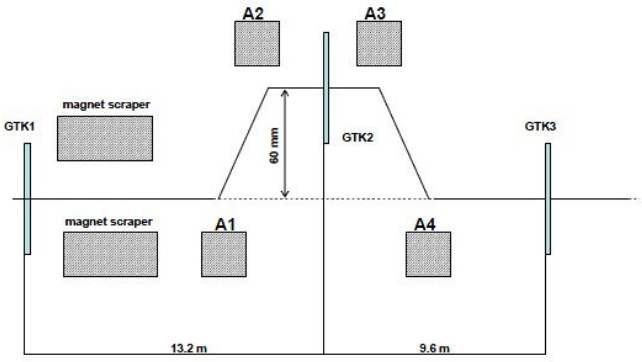

Fig. 3.6 *Schematic layout of the Gigatracker.*

The distance between GTK1 and GTK2 is 13,2 m, between GTK2 and GTK3 is 9,6 m. To cope with the vertical bending of the beam at the achromat the GTK2 is displaced vertically by 60 mm. Each station covers an area of 60 x 27 mm, matching the expected beam dimension, and each pixel is 300 x 300 μm. The readout is accomplished with a set of ten Application Specific Integrated Circuit (ASIC) chips (see Chapter 4 for details), which are bump bonded to the sensor and organized into two rows of five chip each. Being placed to match the beam, the Gigatracker (GTK) is exposed to a very high and not uniform beam rate, which ranges between

~0.8 and 1 GHz, with a peak of intensity around the centre of 1.5 MHz/mm^2. Thus the GTK has to operate in a strong radiation environment. In order to minimize the hadronic interactions and the beam defocusing it has to operate in vacuum and the amount of crossed material must be minimum.

GTK information in conjunction with the Straw Tracker measurements will provide the momenta and angle of the incoming and outgoing particles in order to reconstruct the squared missing mass. Several simulations were performed to fix the required the GTK resolution [28]. Taking into account the expected Straw resolution it has been found that the GTK must be able to measure the momentum with a resolution $\sigma(P_K)/P_K$ equal to 0,2 % and the direction with a resolution of 16 μrad [30].

Due to the high rate, to match the tracks between the GTK and the downstream spectrometer (Straw Tracker) the time resolution must be < 200 ps (rms) per station on the single hit corresponding to ~150 ps for a track.

Even with the required time resolution (150 ps) it is expected that a large number of events will suffer of multiple-tracks overlapping.

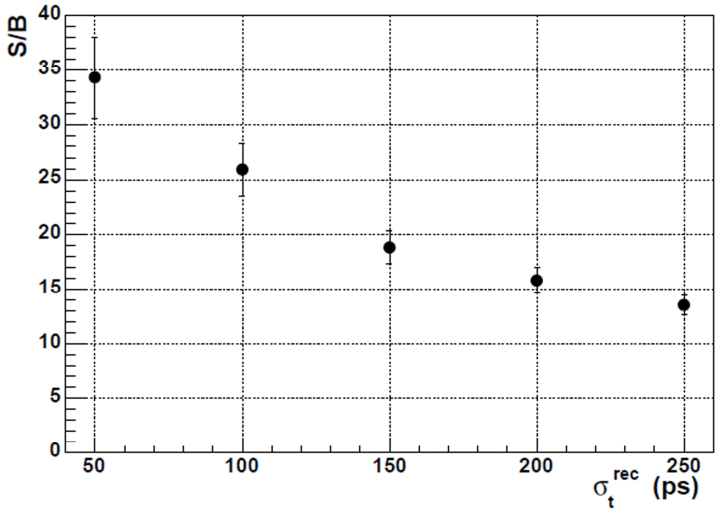

Fig. 3.7 S/*B ratio and Gigatracker reconstructed time resolution.*

However, when considering the overall event reconstruction more constraints can be applied to reject the fake overlapping tracks.

To study the track selection procedure, full events were simulated with *GEANT4* . The Monte Carlo showed that in case of a single track in the Gigatracker, the ratio of signal (S) with respect to background events (B) due to $K^+ \rightarrow \pi^+ \pi^0$, S/B, is ~100, when assuming an event signal acceptance of 10% and a π^0 rejection efficiency of 2×10^{-8}. In case of events with two tracks, the fake track can be rejected using the Closest Distance of Approach (CDA) algorithm. The computation determines the consistency of the two tracks, incoming and outgoing, as converging to a single point. Considering 800 MHz of particles rate, if the time resolution of the GTK is σ_t= 150 ps rms, within $\pm 2\ \sigma_t$ the number of events with more than one track in the GTK is around the 36% and in the ~ 3% of them the matching between the incoming K and the outgoing π^+ is incorrect. The wrong track can be rejected if the CDA is greater than a certain limit, which basically depends on the angular resolution. Because of the multiple tracks in the GTK and the beam divergence, the S/B ratio decreases rapidly and this requires a very good time resolution in the GTK. In fig. 3.7 it is shown the impact of the time resolution on the S/B ratio[1]. The required spatial resolution is less critical and it is set to 100 μm (rms). This value is obtained with a pixel size of 300 x 300 μm.

The time resolution of 150 ps is quite an ambitious value and at the moment no other pixels systems has such a capability. Just for comparison, pixels systems of the experiments at CERN LHC have a spatial resolution between 12 and 18 μm, while the time resolution is more relaxed due to the bunch crossing time of 25 ns [31],[32],[33]. Another important R&D project on

[1] The ratio quoted in fig. 3.7 was obtained by assuming that the time resolution of the beam tracker was improved by 40% with an extra detector following the GigaTracKer.

pixel detectors at CERN is the Timepix ASIC [34], which is an evolution of the Medipix chip [35]. In this case the time resolution is in the order of 10 ns [36].

Another challenging parameter is the high particles rate. The maximum beam intensity in the central area of the detector is expected to be 1,5 MHz/cm^2. The fluence in the central area of the detector for the expected 100 days run time per year is 2x10^{14} 1MeV neutron equivalent per cm^2. This value is very high and comparable with the working conditions of the inner layers of the LHC trackers in 10 years of operation. This requires the sensor and the readout electronics to have a robust radiation tolerance and to replace the Gigatracker stations every 60 days of data taking, which is the typical annual period expected to be granted to NA62. Moreover, to reduce the leakage in the silicon sensor, the Gigatracker must be cooled at 5^o C or below. This request limits the power dissipated by the ASIC chips to be lower than 2W/cm^2.

Another important issue is the material budget. The upper limit, which has been set to 0,5% X_0, imposes the thickness of the sensor and the readout ASIC to be respectively 200 μm and 100 μm. The table below summarizes the main parameters of the Gigatracker system.

Number of stations	3
Number of pixels per station	18000
Number of readout chips per station	5 columns x 2 rows
Number of pixels per chip	1800
Size of pixels	300 μm x 300 μm
Thickness of sensor	200 μm
Thickness of readout chip	100 μm
Time resolution of GTK (rms)	150 ps
Time resolution of one station (rms)	200 ps
Input dynamic range	5000 – 60000 electrons

Particle rate per station	800 MHz
Average particle intensity per station	0,5 MHz/mm^2
Design particle rate per chip	130 MHz
Dead time due to readout	1% (2% in beam centre)
Time stamp resolution per station (rms)	< 200 ps
Total dose in 1 year	10^5 Gy
Material budget	0,5 % X_0 per station
Power dissipation per station	< 2W/cm^2 , 32W
Operating temperature vacuum	< 0^o C

Table 3.3 *Gigatracker parameters.*

3.3.2 The sensor

The silicon sensor is based on the p-in-n planar technology. Comparing the existing technologies for silicon hybrid pixels sensors the choice had to be made between planar and 3D detectors. While the latter one is very promising for the future, the starting time of NA62, foreseen for 2012, imposes the use of a mature technology as the planar one is. Finally the p-in-n technology has been choosen due to the simpler processing procedure and the relatively low cost compared to other possible solution such as underdepleated n-in-n).

The sensor must satisfy two main requirements: to have a very low material budget (< 0.5% X_0 per station) and a sufficient large signal to provide the required time resolution. The 200 μm thickness is a good compromise between the material budget and the charge yield (~15000 e^-). Moreover the sensor should operates at high over-depletion with the bias voltage of 500 V. To ensure a stable operation a multi-guard ring (12) structure has been developed

The overall time resolution is strongly dependent on the charge collection efficiency, speed, and on the capacitance of the sensor. These values degrade under radiation. Also the leakage current increases and the depletion voltage changes. In order to study these effects different p-in-n

diodes were irradiated to fluences between 10^{12} and 2×10^{14} 1 MeV n eq cm^{-2} [37]. Some of the results are reported in table 3.4 and set the limit of 60 working days per station before their substitution. During the NA62 data taking a sufficient precise measurement (better than 100 nA of precision) of the leakage current will indicate the overall status of the detector.

A first prototype of the p-in-n sensor has been realized at the end of 2009 on a 4" wafer. The substrate is n-type (phosphorous doped) with a resistivity of about 4-8 kΩcm the thickness of (200±10) μm and the pixel size 300x300μm. The wafer contains different sensor geometries: one full-size sensor (18000 pixels), 3 single chip sensors (1800 pixels) and sensors for readout chips prototypes (see Chapter 4)

Irradiation level	initial	$5x10^{14}$	$9x10^{14}$
Coupling type amplifier	DC		
Readout pixel implant	n		
Pixel pitch	300 μm		
Sensor thickness	200 μm		
Capacitance of pixel to all neighbor pixels	50 fF		
Capacitance of pixels to backplane	30 fF	40 fF	48 fF
Extra bump capacitance	20 fF		
Max leakage current per pixel for shot noise	0,5 nA	50 nA	200 nA
Charge collection efficiency (at 500 V)	1	0,6	0,45
Collected charge (at 500 V)	16000 e^-	9600 e^-	7000 e^-
Charge collection time	< 5 ns		

Table 3.4 *Irradiation results.*

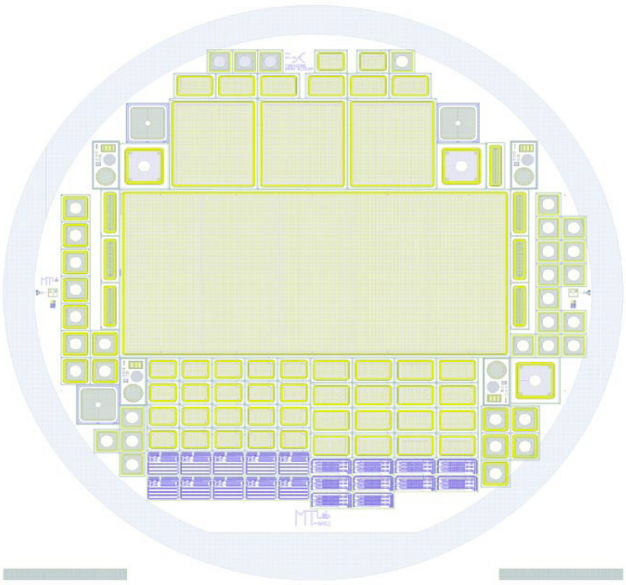

Fig. 3.8 4” wafer layout.

Two rows of five readout chips are connected to the sensor through bump bonding: each pixel cell is bump bonded to the corresponding read-out channel. The bump pads have an octagonal shape and the size is 26 µm. Within the pixel, the pad is located 50 µm from the pixel edge. The bump pads have a mirroring position with their neighboring columns. The pixel size in the interchip region is enlarged (300x400 µm) in order to maintain the full sensitive area. Also the guard rings must be connected to the frontend chips by bump bonding.

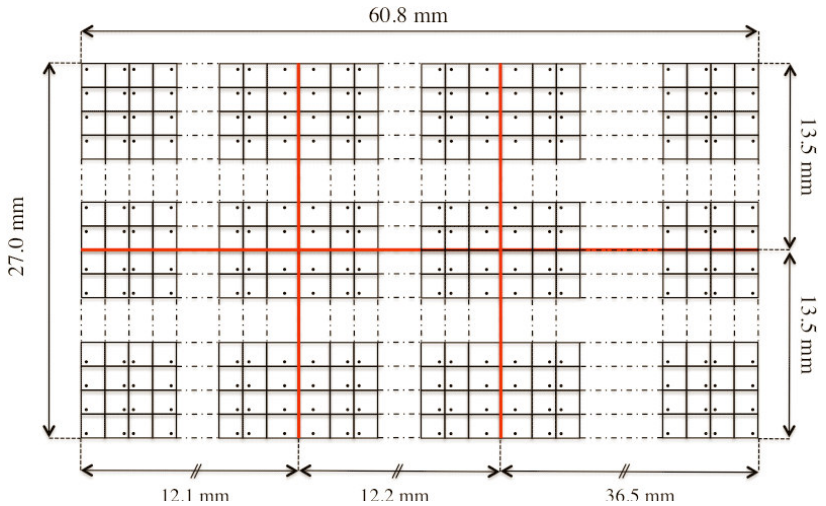

Fig. 3.9 *Schematic layout of the bump bonding position.*

3.3.3 Cooling and mechanics

The detector module is supported by a carbon fiber structure as showed in the picture above.

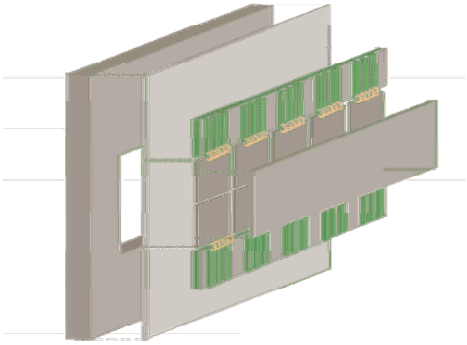

Fig. 3.10 *The Gigatracker supporting system.*

In order to minimize the material budget in the beam area, all the mechanical connections must be done at least 10 mm outside the beam.

The cooling system must provide a uniform working temperature of 5^{o} C or less. The total power dissipated should be less than 32 W corresponding to 2 W/cm^2. In addition the system is operated in vacuum. At the moment, to reach these requirements, there are two possible solutions under development: a micro-channel structure and a vessel with mylar walls.

The micro-channel cooling option consists of two silicon plates. The upper one (cover) contains holes for inlet and outlet and it is glued to the second wafer which contains the micro-channels for the coolant passage. The sensor and the readout chips are clamped between the two silicon plates, through the two red metal blocks, as showed above.

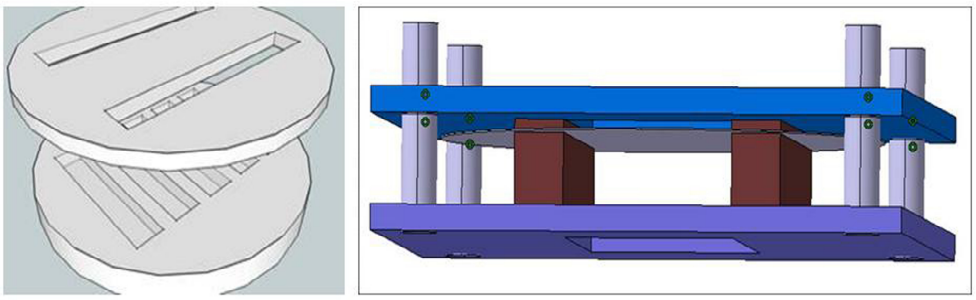

Fig. 3.11 *The micro-channel clamp concept.*

The two metal blocks contains grooves to feed the micro-channels located in lower silicon plate. One should remark that the clamp solution is still under scrutiny and other possibilities are under consideration.

Choosing a channel dimension of 50x50 μm and etching the silicon plates in the beam area it is possible to maintain a total material budget of 0,45% X_0.

A base solution for the coolant gas is C_6F_{14},which is radiation hard, thermally and chemically stable as confirmed in the CMS and ATLAS trackers.

The expected pressure of the fluid in the micro-channels is 12 bar while the operation temperature between -20° C and -30° C. The advantage of using this technique is the lower thermal stress (smaller ΔT between readout chips and coolant) and a better temperature uniformity.

The second option under study for the Gigatracker cooling system is based on the use of a vessel with mylar walls, inserted in the vacuum beam, housing the sensor and the readout chips. A flux of nitrogen at 100° K and 25 m^3/h is expected to be sufficient to keep the temperature of the module at < 5° C with the required uniformity.

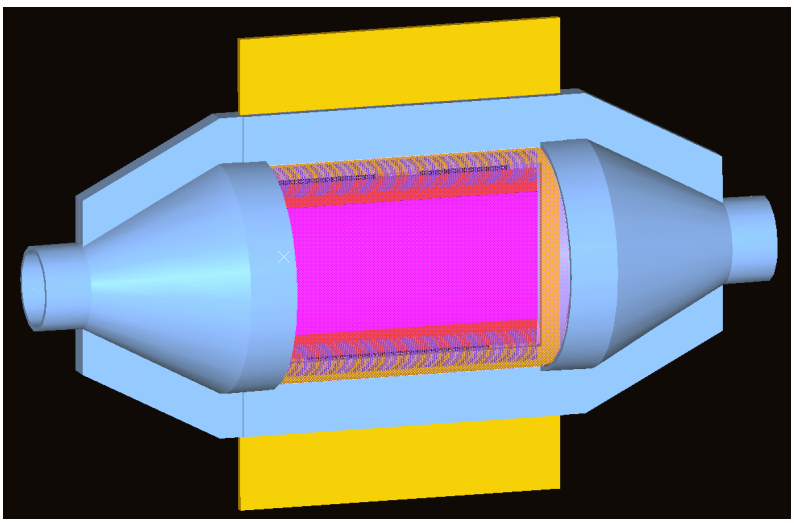

Fig. 3.12 *The GTK cooling vessel. The beam is orthogonal to the picture.*

In this configuration the sensor is connected to a printed circuit board (PCB) (yellow in Fig. 3.12), which provides all the electrical connections to the external system. The detector is thermally decoupled form the PCB and the support must compensate the different thermal expansion coefficients of the materials. Simulations and thermal analysis showed a good uniformity with a maximum temperature of 4^{o} C.

3.4 Magnetic spectrometer

The downstream Magnetic Spectrometer, which is mainly based on the Straw Tracker, is essential to measure the momentum of the outgoing π^{+}. The whole NA62 experiment will succeed only if the K^{+} and π^{+} momenta and angles will be measured with great accuracy, i.e. $\Delta p/p \sim 0.1\%$ and $\Delta\alpha/\alpha \sim 10^{-7}$ rad. This implies the minimization of the amount of material crossed by the particles. It means that every straw station has a limit of 0,1% of X_0. In addition, to reduce the multiple scattering of the outgoing pions, the tracker must operate in vacuum and so it will be installed in the decay region. The proposed design is partially based on the straw detectors used in ATLAS and COMPASS.

The Magnetic Spectrometer consists of a single dipole magnet with four straw chambers, each one made of four views (x,y,u,v), as showed in Fig. 3.14 [38]. Each view is rotated with respect to the following by 45 degrees.

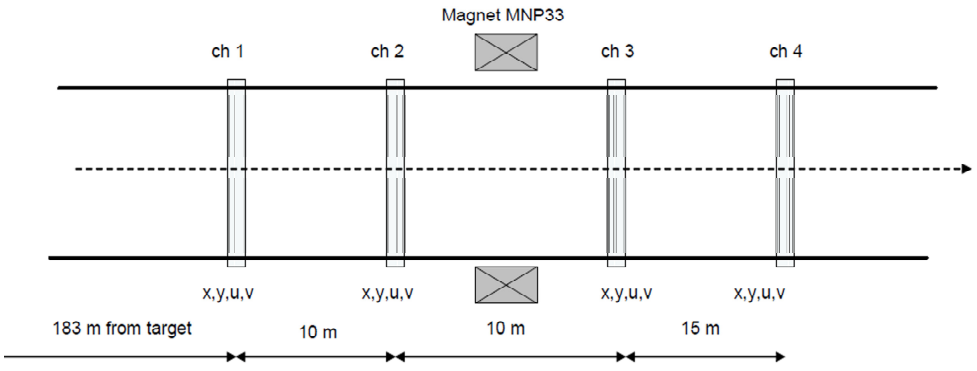

Fig. 3.13 *The Straw Tracker layout.*

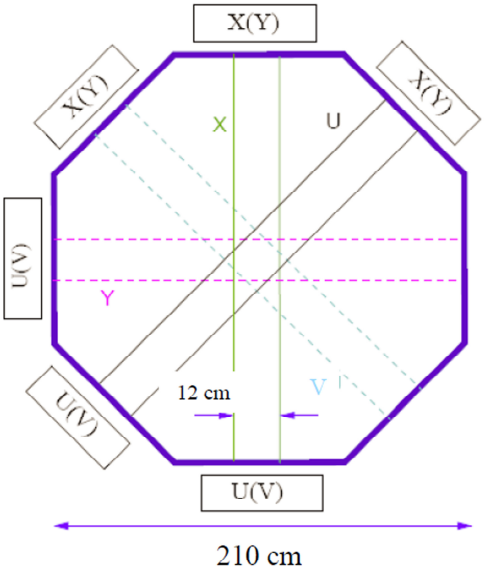

Fig. 3.14 *Schematic layout of the four view chamber.*

Finally each view consists of four staggered planes to increase the point resolution beside solving the left-right ambiguity in reconstructing the pion track (Fig. 3.15). Each view contains a total of ~500 straws . The detector gas is a mixture of CO_2 (80%), Isobutan C_4H_{10} (10%), CF_4 (10%) and it has been used in the 2007 test beam.

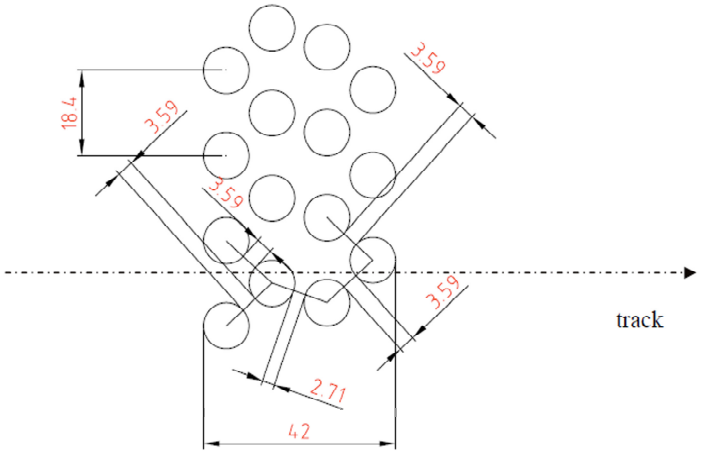

Fig. 3.15 *Straw staggered layers.*

For the 2007 test it was constructed a small prototype of 48 straws. The measured spatial resolution it is equal to 60 μm [39].

3.5 Photon vetoes system

As showed in table 2.1 and Fig. 2.6, the dominant background in the kinematical region of interest, arises from the decay $K^+ \to \pi^+\pi^o$. The suppression can be performed by the π^0 rejection with an overall inefficiency of ~ 10^{-8} or smaller. MC simulations showed that with a photon vetoes coverage of 50 mrad, only 1.6% of $K^+ \to \pi^+\pi^o$ events have one photon outside the acceptance[15], whilst the remaining have both within.

Due to the detector geometry, the maximum efficiency can be achieved partitioning the photon vetoes system in three sub-detectors (Fig. 3.1):

- Large angle vetoes (LAV or ANTI counters 1-12 in Fig. 3.1), covering the angles between 8,5 mrad and 50 mrad
- Liquid Krypton Calorimeter (LKr) covering the angles between 1 and 8,5 mrad
- Small angles vetoes, covering the region near zero degrees and the zone around the inner part of the RICH and LKr

Simulations on the kinematics of $K^+ \to \pi^+\pi^o$, based on GEANT4, were combined to experimental results (done by E787, ES147, ES171 [40]) and theoretical predictions based on the CKM proposal [41], to calculate the average photon detection inefficiency. Applying a cut on the pion momentum between 15 and 35 GeV the fraction of π^+ π^0 with two photons in the LKr acceptance is 82%. In the remaining 18% of events, the photon with high energy hits the LKr while the one with lower energy has 98.9% probability to end in the ANTI counters (LAV) [42]. The overall inefficiency of the system to detect a π^0 is reported in the following table. Measurements were performed on the LAV and the LKr, while the parameterization Optimistic or Realistic refers to the parameters used in simulations as reported in the proposal [15].

	Average inefficiency	Fraction of ineff. events
Realistic choice		
Without pion momentum cut	$1{,}0\ 10^{-7}$	1%
With pion momentum cut	$2{,}8\ 10^{-8}$	0,8%
Optimistic choice		
Without pion momentum cut	$0{,}9\ 10^{-8}$	0.89%
With pion momentum cut	$2{,}2\ 10^{-9}$	0,2%
Using the results of the tests		
Without pion momentum cut	$1{,}6\ 10^{-7}$	0,89%
With pion momentum cut	$1{,}7\ 10^{-8}$	0,2%

Table 3.*5 Total average inefficiencies.*

3.5.1 LAV

The Large Angle photon Veto detector (or ANTI counter) consists of a set of rings around the decay tank. It has been optimized to detect photons with energy E>100 MeV, inefficiency lower than 10^{-4} and a timing resolution lower than 1 ns. The acceptance covers the angles from15 to 50 mrad.

The NA62 proposal [15] presented two possible solutions to build such a detector. The first one is based on a prototype that was build for the now cancelled CKM experiment at Fermilab. It consists of sandwiches of lead sheets and scintillating tiles, with Wave-Length Shifting (WLS) optical fibers readout. Sixteen of these modules forms the veto counter. The second one (lead-fiber prototype) is based on a lead structure (two 0,5 mm tick lead foils) with embedded scintillating fibers, as already used in the KLOE experiment and known as “spaghetti calorimeter” [43]. The fibers are arranged orthogonally to the particles direction.

In addition have been considered lead glass modules of the OPAL experiment [44] which were kindly made available from the same collaboration.

A lead-fiber prototype was assembled in Frascati in 2006. It consisted of one U-shaped module with inner radius 60 cm and length 310 cm, which are similar in dimension to the final upstream veto stations. In order to compare the built prototype to the other two options, the CKM prototype was asked in loan as well as a few lead glass counters from OPAL. The three options have been tested and compared during a test held in Frascati in 2007. The test results showed comparable performances, with an overall inefficiencies between 10^{-4} and 10^{-6}, for energies between 203 MeV and 483 MeV. Thus the final choice was the less expensive option: the OPAL lead glass modules.

One single lead glass module is a truncated pyramid of SF57 glass 37 cm long. The light is collected on top by a photomultiplier (Hamamatsu R2238). The full module will have internal radius of 53 cm and it will be composed of 32 layers, each one 5 degrees shifted in order to have a total hermeticity with three blocks (20 X_0). The design of the module is presented in the picture of Fig. 3.16.

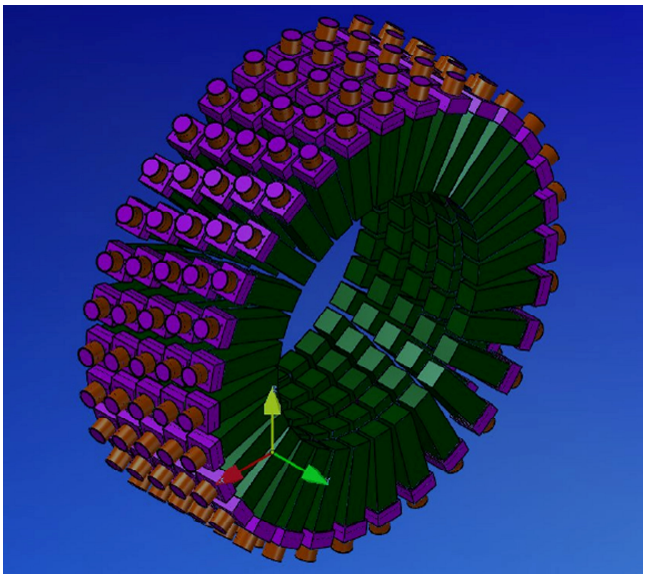

Fig. 3.16 *The lead glass module design.*

3.5.2 LKr

The Liquid Krypton Calorimeter (LKr) was used in the NA48 experiment and was characterized by very good performance [45]. In NA62 it will be

used to cover the intermediate region namely from 1 to 8,5 mrad. In this region the photon detection inefficiency has to be 10^{-5} for photons with energy above 1 GeV and better than 10^{-5} for energy above 35 GeV. Two tests have been performed in 2004 and 2006 in order to measure the LKr inefficiency. The first one collected $K^+ \to \pi^+\pi^0$ decays during a special run of NA48/2 (2004). About 7,33 10^5 events were selected and analyzed [42]. The event selection required a single outgoing track leading to a missing mass compatible with the π^0. The LKr cluster associated to a minimum energy was assumed to be the softer photon from the π^0. It was then predicted position and energy of the harder second photon. Though the number of collected events was not sufficient to properly measure the photon inefficiency, the measurement could only indicate an upper limit on the inefficiency at $E_\gamma > 10GeV$: $\eta_{lkR} < 0{,}9\,10^{-5}$.

The test performed in 2006, still with the NA48 apparatus, used a beam of electrons with momentum 25 GeV/c. Briefly the electrons interacting with the upstream drift chamber radiated bremsstrahlung photons. The electron was left with an energy equal to the difference between the beam energy, 25 GeV, and the energy of the radiated photon. The actual electron energy and direction were measured with the spectrometer. Position and energy of the photon could then be predicted at the LKR. . The overall measured inefficiency partially confirmed the 2004 test. Results are reported in table 3.6

E_γ(GeV)	Inefficiency
2,5 – 5,5	$< 10^{-3}$
5,5 – 7,5	$< 10^{-4}$
7,5 - 10	$< 5\ 10^{-5}$
> 10	$< 8\ 10^{-6}$

Table 3.6 *LKr measured inefficiency.*

However the expected signal rate in the LKr will be much larger than in NA48 and furthermore the read-out inefficiency could jeopardize the intrinsic detector efficiency. These simple considerations suggested the replacement of the LKr readout electronics. In NA48 it was done with FASTBUS modules which now are obsolete. A possible solution is to use a generalised version of the ALICE TPC readout developed at CERN.

In addition also the cryogenics slow control must be replaced due to software obsolescence.

3.5.3 Small angle vetoes

There are two types of small angle vetoes: Intermediate Ring Calorimeter (IRC) covering the beam tube between the LKr and the RICH, and the Small Angle Calorimeter (SAC) placed after the Muon Veto system and covering the region near zero degrees. Both detectors will be built using the "shashlyk" technique [46], which consists of sandwich of lead scintillators and Wave Length Shifting (WLS) fibers collecting the light.

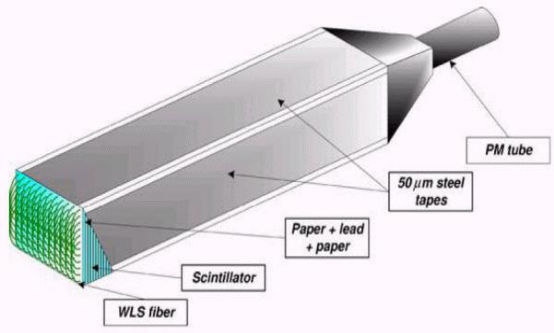

Fig. 3.17 *The shashlyk concept.*

The two detectors must be at least 16 X_0 deep in order to keep the inefficiency below 10^{-7} at the involved energies.

A first prototype of the SAC was tested in 2006 during the P326 run, using the 25 GeV electron beam and collecting 10^7 data [42]. It consists of 70 lead plates 1,5 mm tick, with scintillator plates in between for a total of 16 X_0. The active area is about 20 cm x 20 cm and the light is collected by 480 WLS fibers. The data analysis of the taken data is ongoing.

3.6 Charged ANTI counter (CHANTI)

In addition the veto system foresees six rings anticounters after the last Gigatracker station (GTK3) in order to detected the charged particles produced in the collimator, acting as a "guard ring" to reduce the background (ANTI0 in Fig. 3.1). In fact pions, or other charged particles produced in the GTK3 at small angles, can reach the Straw Tracker and mimic a kaon decay in the fiducial region [28].

The design of the anticounter is not finalized. However a possible solution relies on scintillator tiles read with WLS fibers connected to photomultiplier.

3.7 Ring Imaging Cherenkov counters (RICH)

The rejection of background arising from the $K^+ \to \mu^+ \nu$ decay ($K_{\mu 2}$) requires the identifications of muons, which is mostly performed by the MUV detectors (refer to 3.7) with a ratio of 10^5. In addition the RICH detector will improve the separation of μ^+ from π^+ with momentum between 15 and 35 GeV/c, providing a further muon suppression of 10^2. Furthermore the RICH provides the measurement of the π^+ crossing time with a resolution of 100 ps forming the level0 trigger for charged particles [47].

The detector is placed between the last Straw Chamber and the LKr (Fig. 3.1). It consists of a vessel 18 m long and 2,5 m large around the beam pipe. The vessel is filled with neon gas at the atmospheric pressure. When a charged particle of velocity β crosses the gas volume, with index of refraction n, emits a cone of radiation with angle θ_c with respect to the particle trajectory: $\cos\theta_c = \frac{1}{n\,\beta}$. The momentum threshold for a charged particle of mass m to emit Cherenkov radiation is related to the index n by the equation : $p_t = \frac{m}{\sqrt{n^2 - 1}}$. The neon gas has the right index of refraction to guarantee the maximum efficiency for a 15 GeV/c pion.

At the end of the cylindrical vessel a mosaic of mirrors reflect the Cherenkov light onto the upstream end of the vessel, where the photomultiplier for the light collection are located.

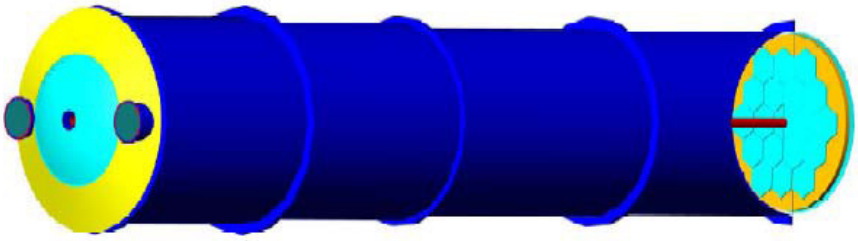

Fig. 3.18 *Schematic view of the RICH vessel. The downstream section shows the mirrors and beam pipe.*

If the momentum p of the particle is measured by some other detector (i.e. Straw Tracker) the mass can be derived from the Cherenkov angle, which is measured by the radius of light collected by the photomultipliers, as showed above.

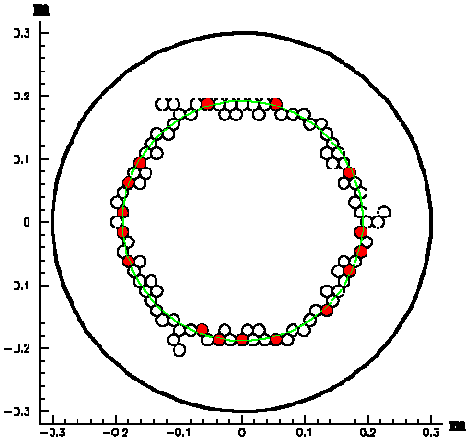

Fig. 3.19 *Light emitted by a pion collected on PMTs (in red the hit ones). Particles with different masses will hit PMTs forming figures with different radius.*

A first prototype of the RICH detector was built and tested in 2007, reaching the timing resolution of 65 ps [48].

3.8 Muon vetoes (MUV)

The rejection of decays containing muons ($K_{\mu 2}$ over the others) is mandatory for the outcome of the experiment. The target of the MUV system is to provide muon suppression of 10^5.

A large part of the rejection is performed requiring two conditions on the track:

a) not to deposit of a significant energy in the calorimeters;
b) to traverse a sufficiently thick layer of iron.

However, in order to achieve the full required rejection power, also muons that undergo catastrophic bremsstrahlung or direct pair have to be identified. To reject these rare events, the MUV system is required to present a sufficient longitudinal segmentation.

In addition in the region of the MUV system, a magnet should deflect the charged particles in order to avoid the collision with the Small Angle Calorimeter. The MUV system consists of three different parts: MUV1, MUV2 and MUV3 in the order of their position along the beam axis. The first two, placed after the LKr, are hadronic calorimeters for measurements of energies deposited by particles to distinguish hadronic from electromagnetic showers. While MUV2 is the old Hadronic Calorimeter of NA48 (HAC), MUV1 is a new module. Both of them are sampling calorimeters, with 24 (MUV1) or 22 (MUV2) planes of scintillator strips oriented alternating vertical and horizontal direction. The design of MUV3 is under development.

Chapter 4

The Gigatracker readout electronics

As described in section 3.3 the Gigatracker requirements are very challenging in terms of timing resolution (150 ps rms), particles rate (800 MHz), material budget and radiation exposure. All these aspects present difficulties for the design of the pixel readout chip.

4.1 Chip specifications

The readout will be performed by ten readout chips bump bonded on the sensor. As showed in the following picture they are organized in two rows of five chips.

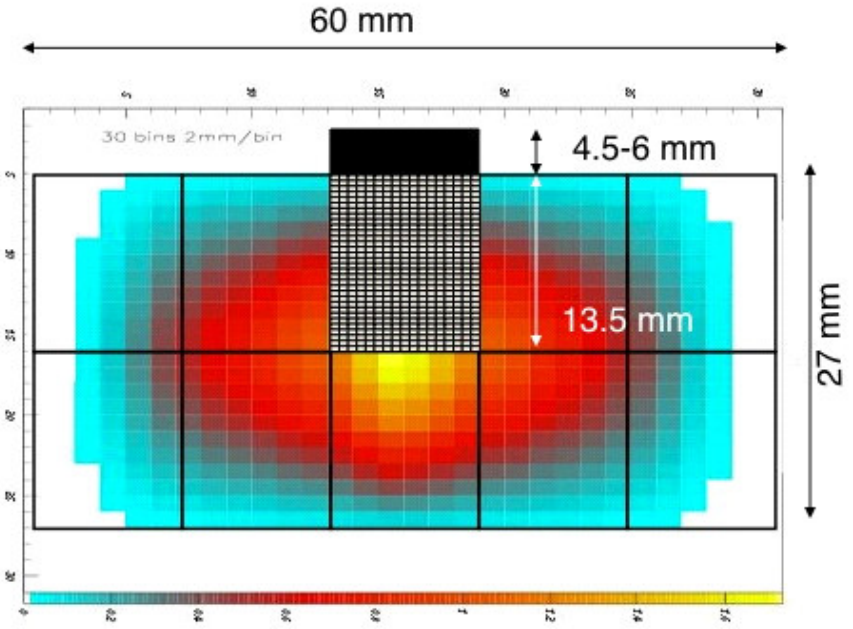

Fig. 4.1 GTK Readout chips.

Each readout chip has to cover an area of 13,5 x 12 mm, where the active pixel matrix is organized in 45 rows x 40 columns of pixels for a total of 1800 pixels. Fig. 4.1 also reports the expected particles rates in the different regions of the sensor, where the peak rate per pixel in the centre of the beam it is expected to be 140 kHz, while the average rate per pixel in the whole GTK station is 44 kHz.

If every hit is encoded into a 32-bit word the data throughput will reach the considerable value of 4,2 Gb/s per chip, which means 4,8 Gb/s considering a serial transmission with a 8b/10b encoding. At this rate the use of high speed differential signal is mandatory and a trigger less readout will be adopted.

A further constraint on the readout chips come from the external pad positions. As shown in Fig. 4.1 the chips, in order to cover the total active area, have only one side which is accessible from the external without interference, thus the number of electrical connections must be limited as much as possible.

Also power consumption is an issue while the cooling system puts a limit on the overall dissipation in the GTK station of $2W/cm^2$. In addition the chips have to operate in a strong radiation environment, where the expected total dose in one year is 10^5 Gy. The detailed list of the specifications of the GTK readout chip has reported in the following Table 4.1 [28].

The GTK pixel readout chip will be implemented using the CMOS 130 nm technology. Several studies on this technology showed that it should be sufficiently radiation hard for the expected total dose from kaons and pions with a background of neutrons. However the dose is not uniform in the three stations or in the centre or periphery of each chip. This will cause a different response from pixels located in different positions that can be adjusted by trimming the discriminator threshold on each pixel.

Architecture/geometry	
Chip active area	13,5 x 12 mm
Chip size	19,5 x 12 mm
Number of pixels per chip	1800
Pixel size	300 x 300 μm
Thickness of readout chip	100 μm
Pixel analogue frontend	
Input dynamic range	5000 – 60000 e^-
Electronic noise in pixel input with sensor	200 e^- rms
Analogue shaping time	4 ns
Time resolution of the discriminator	100 ps rms
Discriminator column spread after trimming	100 ps rms
Discriminator chip spread before trimming	150 ps rms
Discriminator time walk after correction	80 ps rms
Trim DAC resolution	8 bits
Overload detection threshold	60000 e^-
Double single pixel pulse resolution	100 ns
Max recovery time for 2 fC signal following a 80 fC signal	2 μs
Max dark current per pixel tolerance	1 μA
Power dissipation per pixel	1 mW max
TDC	
TDC time precision	100 ps
Data rates	
Beam rate	800 MHz
Average centre chip hit rate	132 MHz
Avg. particle rate per pixel in station	44 kHz
Avg. particle rate per pixel in centre chip	73 kHz
Peak rate per pixel / beam centre	140 kHz
Centre chip data rate (32 bit per hit)	4,2 Gb/s
Avg. centre column rate	3,3 MHz
Serializer data rate	4,8 Gb/s
Master clock frequency	160 Mhz / 320 Mhz DLL
Readout efficiency	99% (98% in beam centre)
Radiation	
Average total dose in one year	2 10^{14} p-k/cm^2, 10^5 Gy
Max pixel timing mismatch after radiation	200 ps
Off chip trigger	
Number of levels	1 (L0)
Latency	> 1 ms
Trigger window	75 ns

Table 4.*1 Readout chip specifications.*

4.2 Time walk compensation

With the expected input dynamic range the time walk compensation is mandatory in order to reach the target time resolution. The techniques typically used are the Time Over Threshold (TOT) or the Constant Fraction Discriminator (CFD).

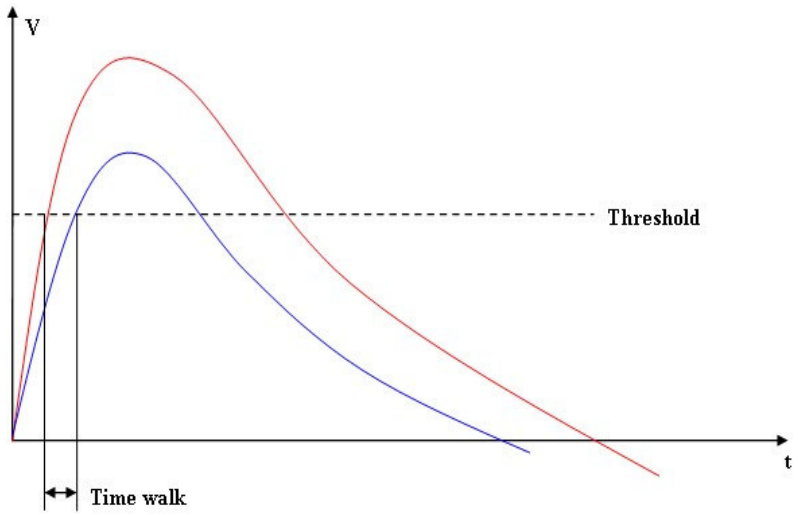

Fig. 4.2 *Time walk definition. Signals with different amplitudes are detected at different times.*

The TOT technique consists in the use of a preamplifier where the output signal width is proportional to the input signal amplitude. The time walk correction is based on an algorithm derived from the correlation between the pulse width and the experienced time walk that can be measured injecting signals with known amplitude. The TOT solution requires the time measurement of both rising and falling edge of the input signal, increasing the amount of data to handle.

In the CFD filter one portion of the input signal (~20%) is inverted, while the signal is delayed by a fixed time. The two signals are then combined to give a bipolar signal with a zero crossing point. This point (t_{cfd}) is detected and virtually independent on the input signal amplitude:

$$t_{cfd} = \frac{t_d}{1-f} \text{ where } t_d = \text{delayed time; } f = \text{fraction of signal;}$$

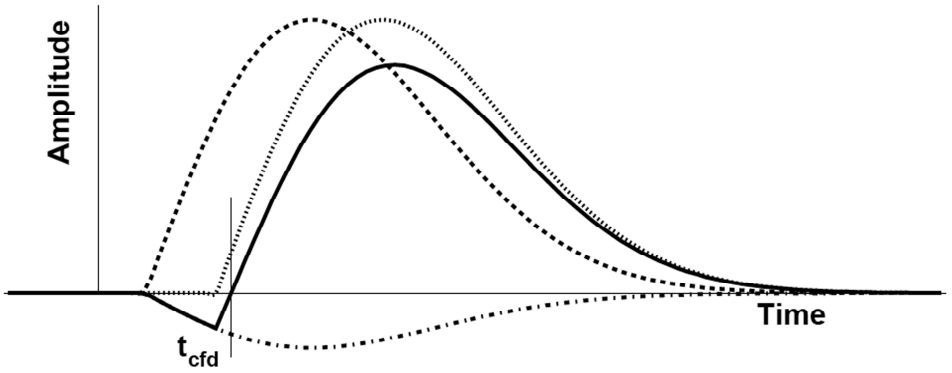

Fig. 4.3 *The Constant Fraction Discriminator principle. The input pulse is represented by the dashed line. It is delayed (dotted), attenuated and inverted (dashed-dotted line), then summed to give the bipolar pulse*.

In the CFD the choice of the delay time and the fraction of signal of the inverted part are crucial parameters. Therefore the circuit is more complex than the ToT architecture. For the GTK readout chips both the two techniques (TOT and CFD) seem to be promising so they are both under investigation and two ASICs prototypes have been developed (see sections 4.5 and 4.6).

4.3 The time measurement

In the GTK readout chip the coarse time information will be provided by a clock counter that will serve as a reference. The issue of the precise time resolution can be dealt with a Time to Digital Converter (TDC), which has to provide the precise time measurement with respect to the time reference. There are many techniques to implement such a device, but for the GTK readout two options are ongoing: a Delay Locked Loop (DLL) based TDC and a Time to Amplitude Converter followed by a dual slope Wilkinson ADC. While the first is a fast circuit and can be adopted only in the case of sharing the same TDC between a group of pixels, the second one has the advantage to follow an analogue approach. This technique infers less electronic noise and can be realized in a relative small area, thus, in

principle, it can be implemented on each pixel cell. The two different approaches have been implemented in the two chips prototype, described in sections 4.5 and 4.6.

The principle of a DLL based TDC is sketched in Fig. 4.4. A chain of well calibrated delay elements, voltage controlled by the charge pump, generates a bunch of clock signals that are used to clock the hit register, which samples the input signal. So the hit register latches the time position of the input signal. The digital information is then generated encoding the hit register content.

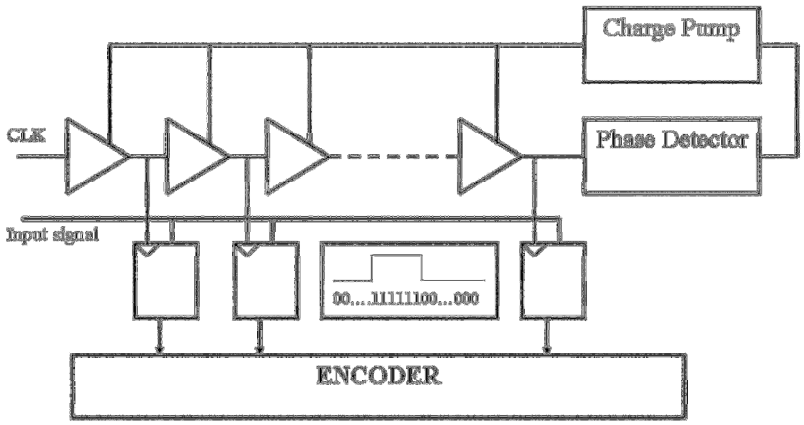

Fig. 4.4 *The DLL based TDC principle*.

In the second option, the Time to Amplitude Converter followed by the Wilkinson ADC, the time interval to be measured is converted into a voltage amplitude, by charging a capacitor with a constant current. The peak voltage is then proportional to the charging time, which is defined by the start and stop conditions of the time window to measure. Then the capacitor is discharged linearly with a longer time that can be measured by a clock counter (dual slope Wilkinson ADC). The length of the discharging ramp is proportional to the input amplitude and finally to the charging time window. The behavior of this circuit is showed in detail in section 4.6.4.3.

4.4 Off-detector readout electronics

The off-detector readout system is responsible of the interface between the on-detector electronics, the Data Acquisition system (DAQ), the NA62 trigger and the slow control (DCS, Detector Control System).

The foreseen data throughput from one readout chip is expected at around 5 Gb/s, requiring at least two or four optical fibers (depending on the serializer speed of the readout system) to assure the data transmission. The task performed by the GTK Readout Boards (ROB) is to store the raw data until the L0 trigger arrival, which has a latency of at least 1 ms. Then the ROB selects the data to send to the DAQ system, in a time window of 75 ns around the event addressed by the trigger. The expected data rate at the ROB output is 75 MB/s per GTK chip. In addition the off-detector readout will monitor the detector status (temperature, electronics configuration and status) and pass these information to the DCS system. The configuration must be sent individually to each chip, within the clock signal which requires a very low jitter (< 20 ps). In total the number of serial connections will be 60 (or 120).

At present, it has been decided to use the TTCrx chip [49] to receive the trigger signals. In addition a throttle signal will be used to slow down the trigger rates in case of problems with the buffer occupancy.

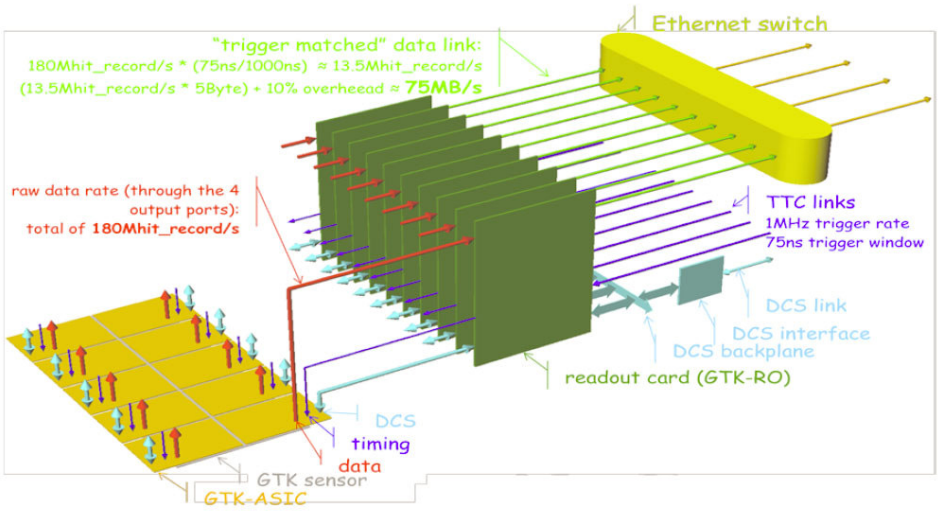

Fig. 4.5 *Off detector readout electronics* [28].

4.5 The End of Column TDC prototype

During 2009 a prototype of the GTK readout chip, with a DLL based TDC at the End of Column (EOC), and a time walk compensation realized by the Time Over Threshold discriminator (TOT), has been submitted by the CERN group of the collaboration. The chip is implemented in CMOS 130 nm technology. It is described in the next sections, and preliminary results are showed.

4.5.1 Global architecture

In the EOC TDC option the pixel cell contains only the analogue electronics: the preamplifier, the TOT discriminator and a line driver which sends the discriminated signal to the EOC circuitry. Here is hosted a DLL based TDC, tagging the rising edge and the falling edge of the discriminated signal, with a time precision of 100 ps. In addition a coarse measure of time is performed by clock counters, and the time tag is extended up to 12,8 μs.

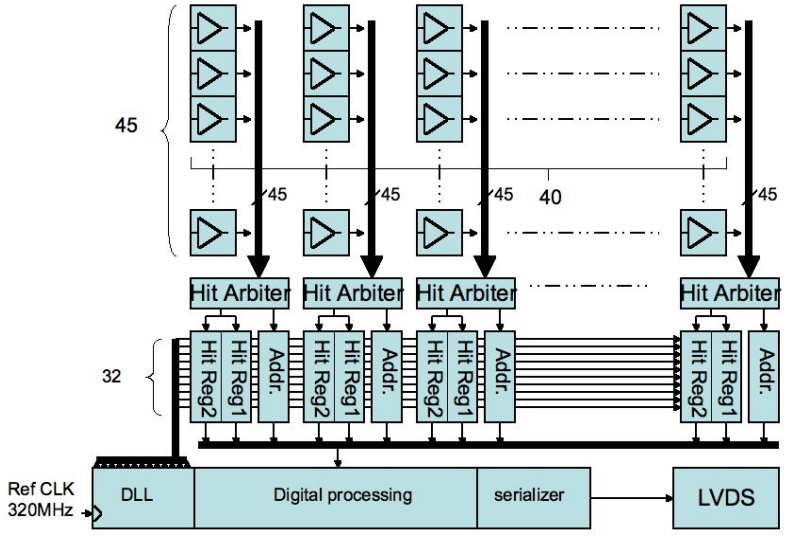

Fig. 4.6. The *EOC architecture block diagram.*

The first idea was to share the transmission lines between a group of pixels [50], [51]. After many simulations that showed to have a high risk of hit inefficiency, it has been decided to use a single line for each pixel.

In order to minimize the amount of TDC hit registers, a single register serves a group of 5 pixels, with the use of a combinatorial Hit Arbiter circuit. Simulations showed that for the worst case (centre of column) the hit efficiency is still 99,5%. The time words and the pixels addresses are stored in a FIFO before to send them out of the chip via a serial transmission. The time walk compensation is performed off line using the two time tags (rising edge and falling edge) per hit. In this architecture no clock signals are propagated to the pixel matrix, which hosts only the analogue electronics. All the digital circuitry is concentrated in the EOC periphery.

4.5.2 The EOC analogue pixel front end

The pixel cells hosts in total seven components: a trans-impedance preamplifier, a differential post amplifier, two stages of the ToT discriminator (the second one with hysteresis), a dynamic asynchronous latch, the line current driver with pre-emphasis and the coplanar transmission line [52].

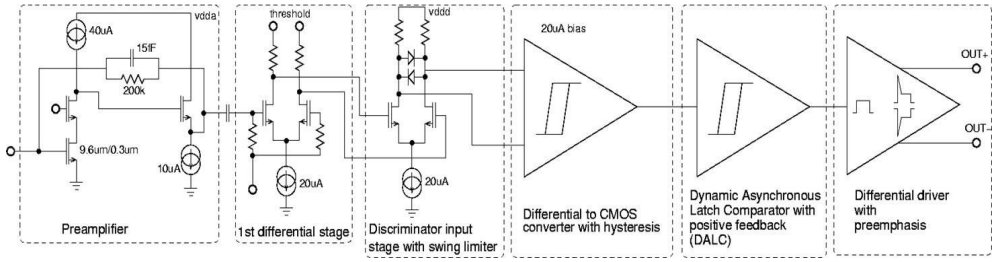

Fig. 4.7 *Block diagram of the EOC pixel cell (without the transmission line).*

The preamplifier has a cascode stage with an NMOS input transistor of dimensions 9.6 µm x 300 nm (WxL) with a simple RC feedback. The pulse gain is 30 mV/fC. The dimensions of the input transistor are optimized for a detector capacitance of 250 fF. The low value of the input capacitance allows the use of a simple cascode stage offering very high bandwidth (1 GHz gain bandwidth product) at very affordable power consumption (60 µW). The open loop gain is about of 45 dB and the input impedance of the preamplifier is in the range of 1 to 2 kohm for 1 GHz bandwidth, which is low enough to provide the required charge collection from the detector.

Crosstalk between neighboring pixels is expected to be less than 4 %. The first differential stage translates the external differential threshold voltage for the comparator. The fully differential structure of the comparator provides very good rejection of common mode noise arising from the digital power supply. The entire preamplifier-shaper circuit has a gain of 70 mV/fC. The overall shaping function of the preamplifier and shaper has a peaking time of 5,5 ns and it behaves like CR-RC3 circuit. The following three stages of the comparator, which prepare the signal for the transmission line, have high sensitivity and very high speed performances at a reasonable power (50 μW). The time jitter (transient noise simulation) of the full front end was simulated with 3 fC of input signal and it is in the order of 30 ps RMS, which agrees with the predicted Equivalent Noise Charge (ENC) values, as shown below.

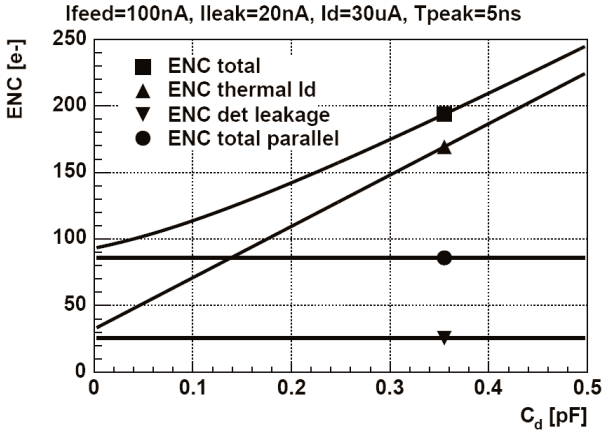

Fig. 4.8 *Noise analysis for the 130 nm technology*.

These simulation results show that for a detector capacitance of 250 fF the predicted ENC will be below 200e^-. Further simulations were performed to evaluate the time walk and time over threshold behavior with the same detector capacitance. The results show that the expected time walk correction is 2,1 ns for an injected charge of 5,25 fC. The TOT pulse width can vary from 8,45 ns, for an injected charge of 1 fC, to a maximum of 14,4 ns for a maximum injected charge of 5 fC [28].

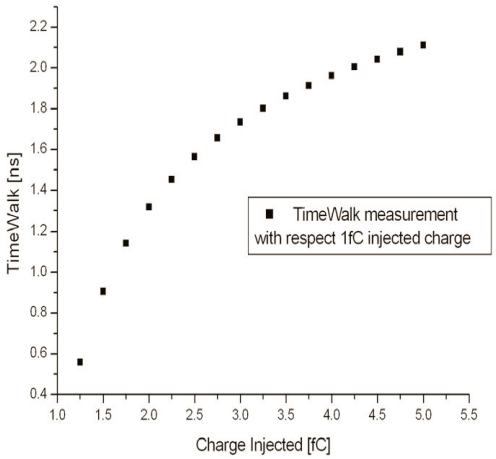

Fig. 4.9 *Time walk correction vs. injected charge*.

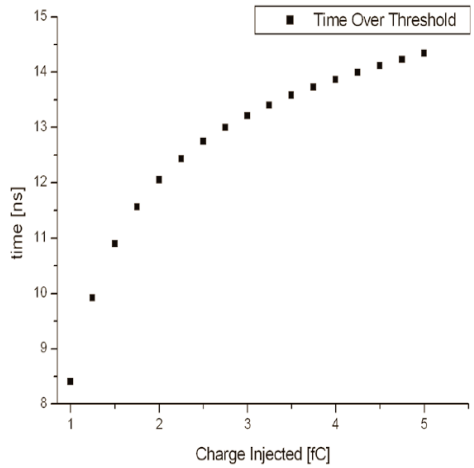

Fig. 4.10 *Simulated pulse of the TOT discriminator.*

4.5.3 The transmission line

In order to preserve the time jitter at a low level, the TOT signal must be propagated to the end of column TDC preserving both the rising edge and the falling edge. Due to the fact that a traditional CMOS inverter introduces a delay which depends on the input capacitance (proportional to the length

of the transmission wire) it can not be used as a receiver. Furthermore the large voltage swing limits the transmission speed.

The transmission lines are coplanar waveguides where signal components of different frequency are transmitted at the same speed. The differential voltage swing is 240 mV driven in current in the pixel cell, in order to guarantee at the receiver the same signal amplitude, independently from the pixel distance and from the resistance of the transmission line. The 13,5 mm long transmission line (the longest one) can slow down the signal edge during the transmission up to 5 ns. To avoid this effect in the pixel cell is performed a pre-emphasis of the current signal, and this allow to have a signal with a rising edge of 1 ns at the receiver input, also for the farthest pixels.

The transmission receiver consists of two blocks: a differential to CMOS converter with hysteresis and a dynamic asynchronous latch comparator (DALC). The DALC does not consume static power and thanks to a positive feedback generates signals with fast transitions. The difficulties of the receiver circuit arise from the very low voltage swing in the input with the high frequency (1 GHz) operations required.

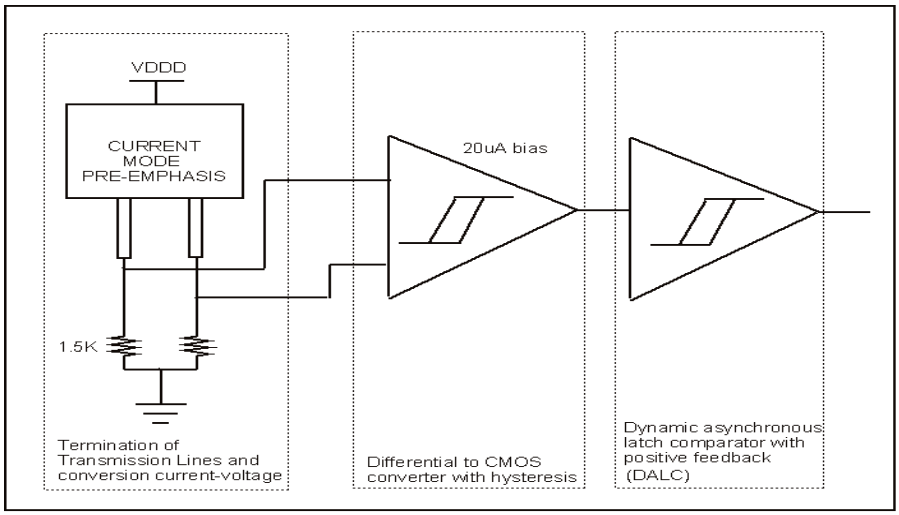

Fig. 4.11 *Transmission line: the receiver block diagram.*

The input stage of the receiver is a circuit that senses the differential current and it is implemented with a differential common gate cascode stage. The output of the first stage is sensed with a broadband differential to single-ended amplifier. The output is converted into a fast digital CMOS level signal by a dynamic asynchronous positive feedback latch comparator stage, which can generate pulses edges of 50 ps to drive the TDC inputs.

4.5.4 The End of Column logic

In the EOC architecture the fine time measurement is performed by a DLL based TDC, where the delay chain consists of 32 buffers connected in series. The circuit is based on previous developments done both in 0,25 µm and 0,13 µm CMOS technology.

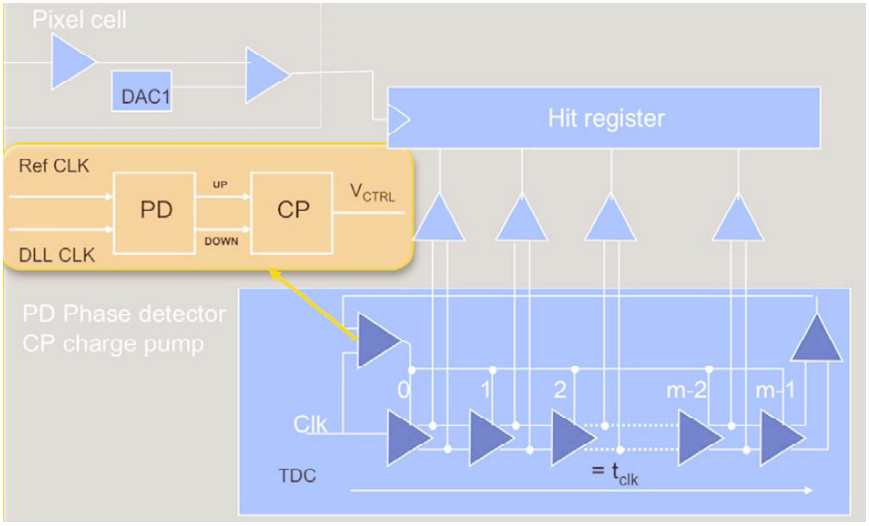

Fig. 4.12 *The EOC TDC.*

The reference clock feeds the delay chain, where the delay of each element is controlled in voltage. At the end of the chain the phase of the input clock is compared with the one of the signal coming from the delay chain. If the phase difference is positive (signal too slow) the circuit gives a voltage pulse in order to increase the speed of the chain. If the phase difference is negative it decreases the voltage to have a longer delay. Once the DLL is locked there is no phase difference and one clock period is exactly segmented by the number of buffers in chain. When the hit arrives the state

of these buffers is latched in the hit register to give the fine time information, while the coarse time is obtained by latching a clock counter.
The EOC TDC works with a reference clock of 320 MHz. Since the delay chains contains 32 buffers, the TDC time bin is 98 ps. In order to reduce the amount of registers, it was decided to use only one register every 5 pixels. In total for a 45-pixels column there are 9 rising edge registers and 9 falling edge registers. Many simulations showed that it is still possible to keep an efficiency of 99,5% with this configuration. In the rare case of simultaneous hits in the same register, an arbiter circuit flags the ambiguity in the data stream. In order to process the cases of charge sharing between neighbour pixels, the same hit registers do not serve consecutive pixels, but the connections are organized like it is shown in the following figure (4.13).

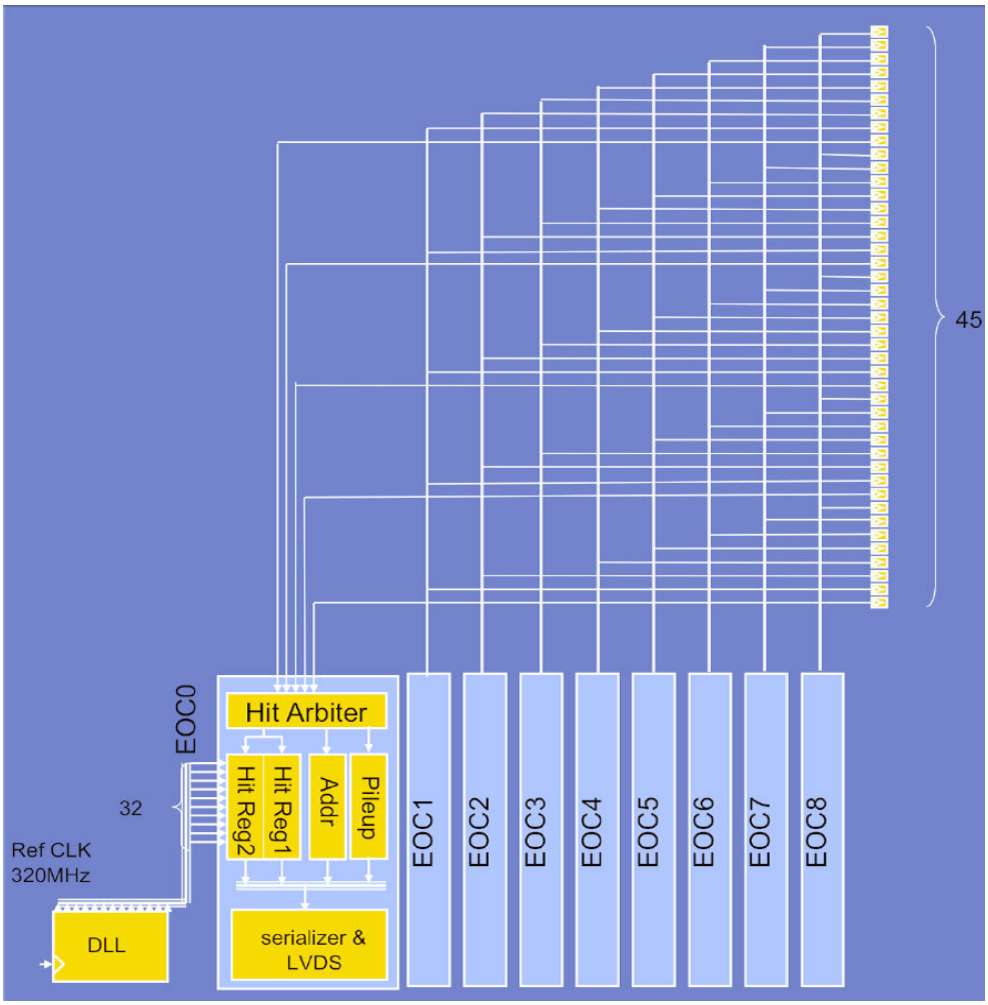

Fig. 4.13 *The 45 pixels column readout.*

Since the time walk compensation is performed by the TOT discriminator, the rising edge of the signal gives the information of the arrival time, while the falling edge is related to the signal amplitude and it is used to correct the time walk. In addition to the time of the leading edge a synchronous clock counter is latched to add the coarse time information. The digital word, which contains the two time stamps and the pixel address, is stored in a FIFO before it is serialized and sent out of the chip.

The GTK readout chip will contain only one (or few at most) DLL: the signals are buffered and distributed via differential drivers to all the hit registers of the 40 columns. The EOC digital logic is placed at the periphery of the chip, where the expected radiation levels are reduced. Thus only a subset of registers needs special protection against the single event upset. In order to fit the end of column readout in the 300 μm column width, the layout it will be very dense and the concentration of digital noise in this area it can be an issue.

4.5.5 End of Column TDC demonstrator

A demonstrator ASIC in CMOS 130 nm technology of the EOC TDC architecture has been developed and realized in 2009. The chip contains one full column of 45 pixels which is folded, in order to avoid a very long and narrow chip geometry. The goal of this prototype is prove that: a) the time walk compensation can be performed by the TOT discriminator; b) the transmission line concept of the analogue signal; c) the time tagging by the DLL based TDC can reach a time resolution better than 200 ps. While the analogue cell, the TDC and the transmission line are developed as in the final chip, the readout of the output buffer has been simplified and it will require further studies.

The 45 pixel column of the demonstrator is connected to 9 hit arbiters using 18 hit registers and one DLL. The reference clock is 320 MHz and also the readout is done at the same speed, through one serial connection for each of

the 9 groups of registers. In order to evaluate the impact of the digital noise on the analogue cell, the readout clock can be switched off.

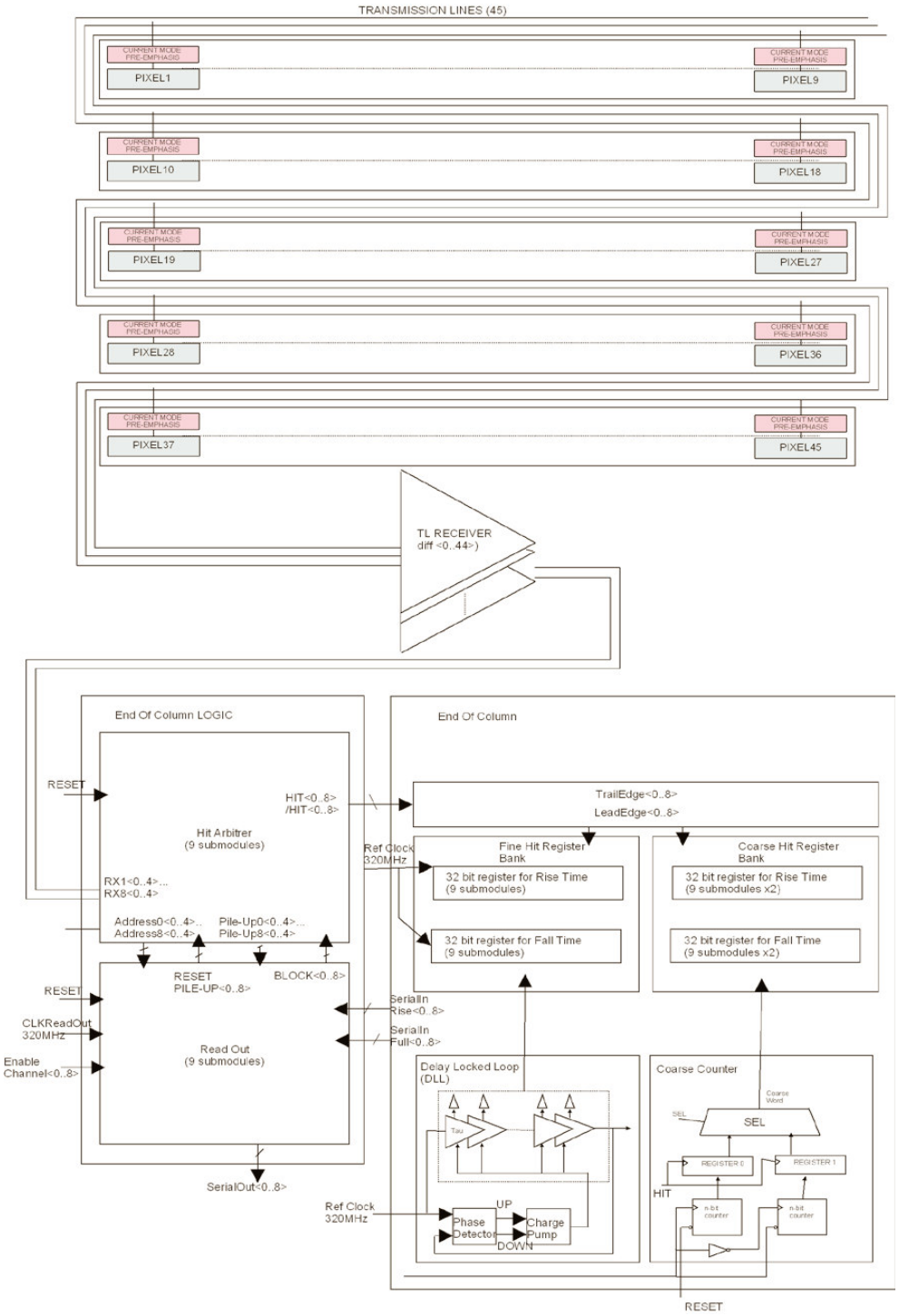

Fig. 4.14 *The demonstrator chip block diagram* [28].

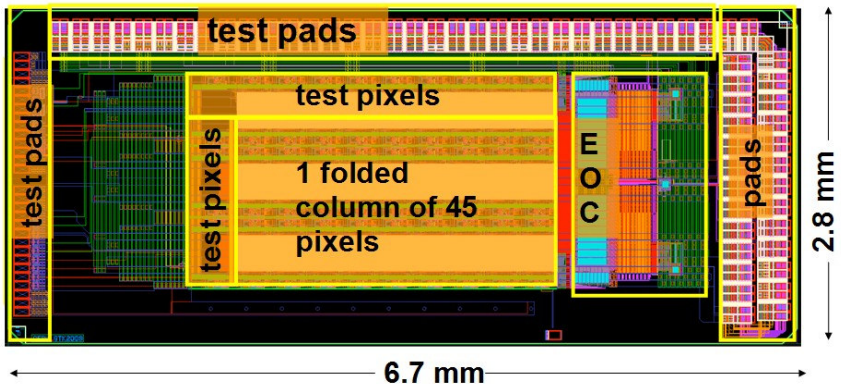

Fig. 4.*15 The EOC prototype layout.*

In addition, in order to qualify the individual blocks, a set of 10 test pixels is connected to a second EOC circuit that operates independently.

In Fig. 4.15 are reported the dimensions and the layout of the EOC prototype as it has been submitted.

4.5.6 Test setup

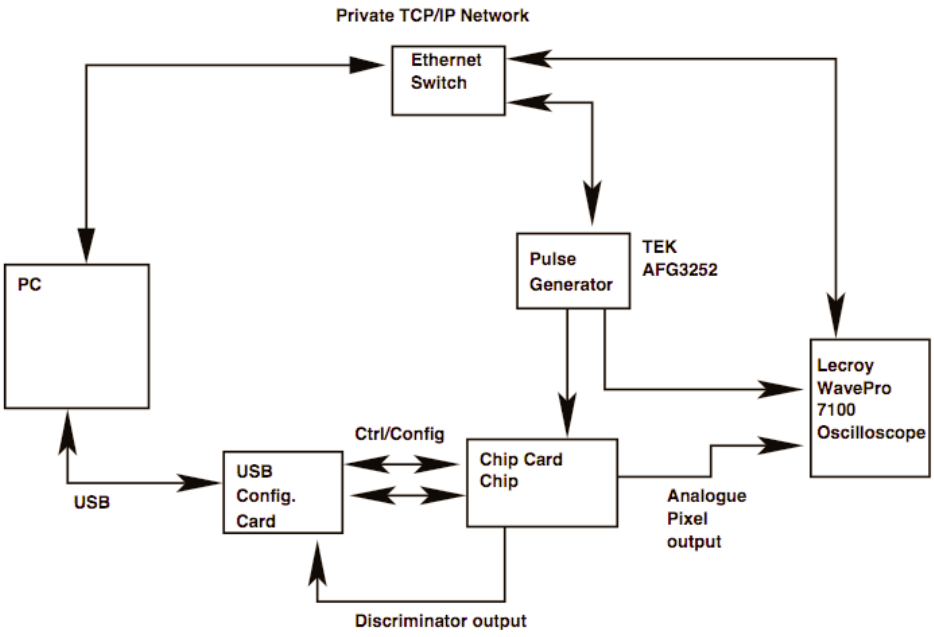

Fig. 4.16 *Analogue measurement test setup.*

The test system is based on an ALTERA Stratix III FPGA development kit. The chip has been wire-bonded to a printed circuit board (sensor card) and connected to the FPGA board. The block diagram in Fig. 4.16 shows the set up for the analogue measurements. In principle the test is done injecting an asynchronous signal to the analogue cell input, and recording the output signals of the pre-amplifier and the discriminator by a digital oscilloscope. The analysis of the time walk and the TDC performances are done offline. The same test boards will also used in laser and beam test.

4.5.7 Preliminary results

The test started at the end of august 2009. The static power consumption is ~8 mA for the 1,2 V analogue bias (which corresponds to 133,3 μA per pixel). The measured value correspond to a situation where mostly of the circuit remains inactive, with the DLL having no input clock applied to generate the delayed signal. The analogue front-end was tested by injecting a charge of 2 fC, by a pulse of amplitude 100 mV and rise time 0,5 ns onto a 20 fF capacitor. Under this condition the analogue output noise is ~ 500 μV rms or 56 e^- ENC which is in agreement with the results of the simulations without detector. For each of the 5 test pixels, it was traced the S-curve (threshold scans curve). An example of the S-curve for pixel no. 10 is shown in Fig. 4.17.

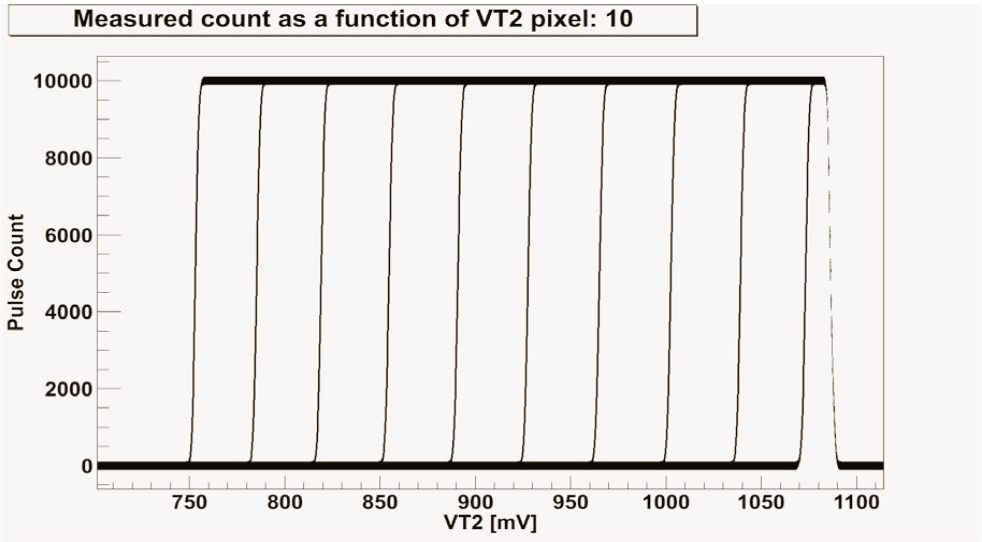

Fig. 4.17. *The S-curve for pixel no. 10* [28].

For a fixed number of input pulses, the output number of pulses is reported on the vertical scale as a function of the input charge. The curves are drawn as a function of the threshold of the differential preamplifier, V_{T1} - V_{T2}. To trace the S-curve V_{T1} was set to 1100 mV. 10000 pulses of fixed amplitude were injected with a repletion period of 1 ms. After each pulse the discriminator output is recorded with the acceptance window of 25 ns. Then the threshold V_{T2} is changed by 300 μV to scan the whole range between 865 and 910 mV. The full procedure has been repeated for different values of input charge, from 0,5 to 5 fC.

Preliminary statistics on the gain for the five test pixels are reported in the following two figures, 4.18 and 4.19. The results have been extracted for an injected charge between 1 and 3 fC, which corresponds to the linear gain region. The mean value of the gain is 67,8 mV/fC, which is in a very good agreement with 70 mV/fC as predicted with the simulation.

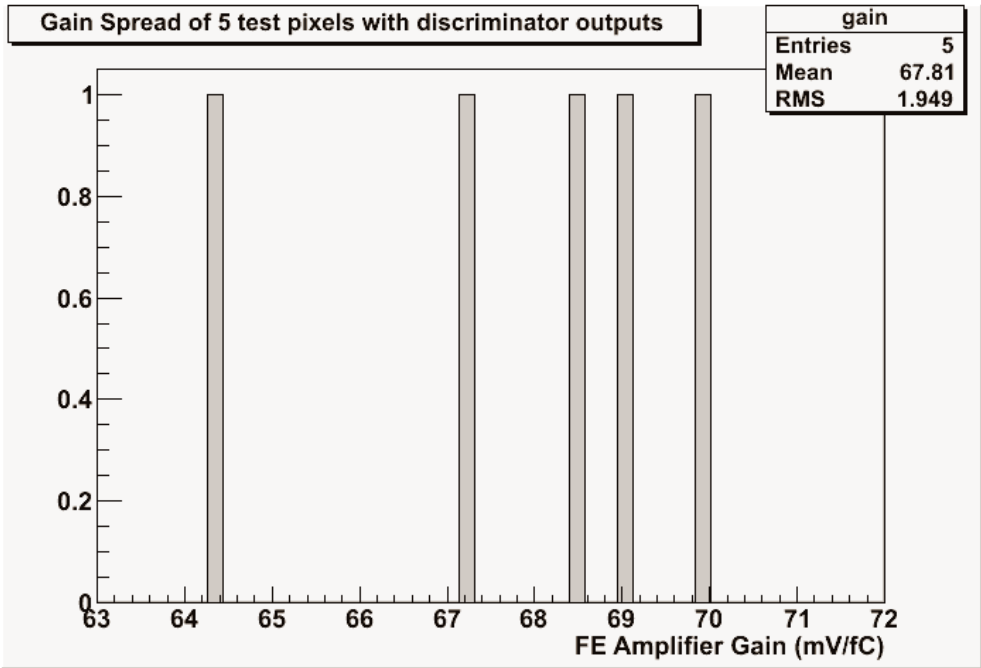

Fig. 4.18. *Gain spread of the 5 test pixels* [28].

The same statistics was collected for the offset of the pre amplifiers output and it is reported in Fig. 4.19. The spread around the mean value of -4 mV can be explained in terms of process variations.

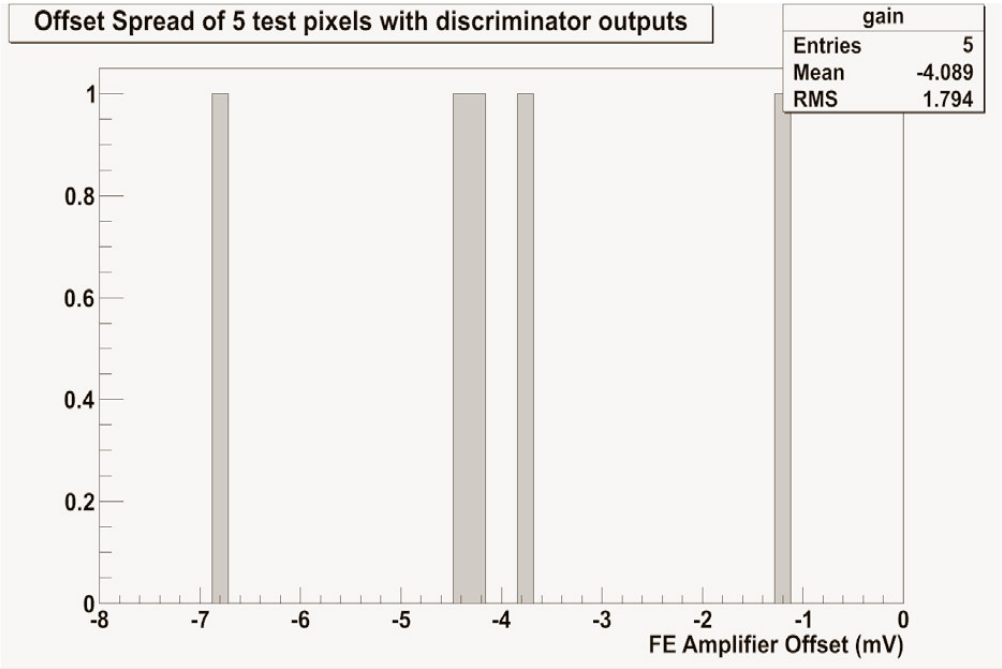

Fig. 4.19. *Offset spread of the 5 test pixels* [28].

To evaluate the jitter and the time walk of the front-end, the acquired data were analyzed off-line. Time walk and jitter values for both the rising edge (T_1) and the falling edge (T_2) are reported in the following figures 4.20 and 4.21.

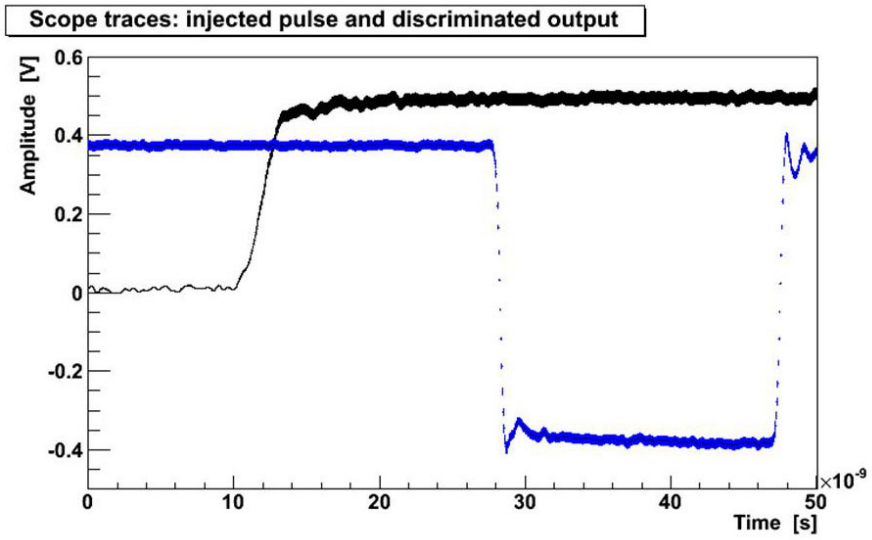

Fig. 4.20 *Injected charge and TOT response.* [53]

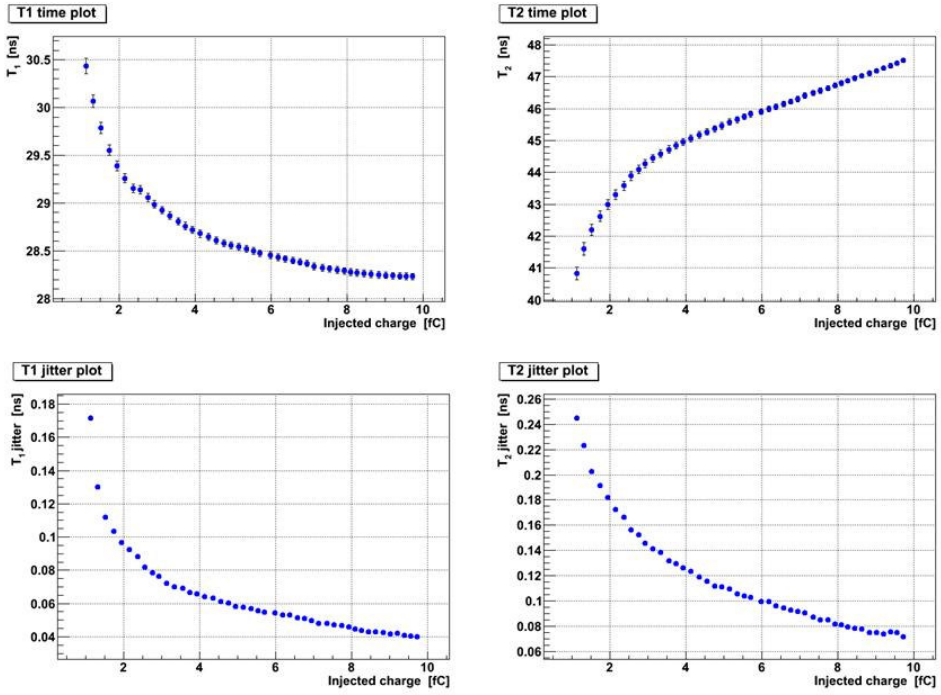

Fig. 4.21 *Time walk (up) and jitter (down) for the leading (T_1) and trailing (T_2) edge of the TOT discriminator.* [53]

Performing the time walk compensation off-line over the Landau distributed input charge a jitter value of 70 ps was obtained which is greater than the simulated 40 ps. At the moment this can be explained with the non optimized test setup.

The TDC tests are ongoing and at the moment the DLL locks at 250 MHz instead of the nominal 320 MHz, giving a time binning of 125 ps. To characterise the behaviour of the TDC many random triggers (28 millions) were sent and histograms of TDC code occurrences were traced. The integral and the differential non linearity are lower than 0,2 LSB and the bin width uniformity is ~0,15 LSB [54].

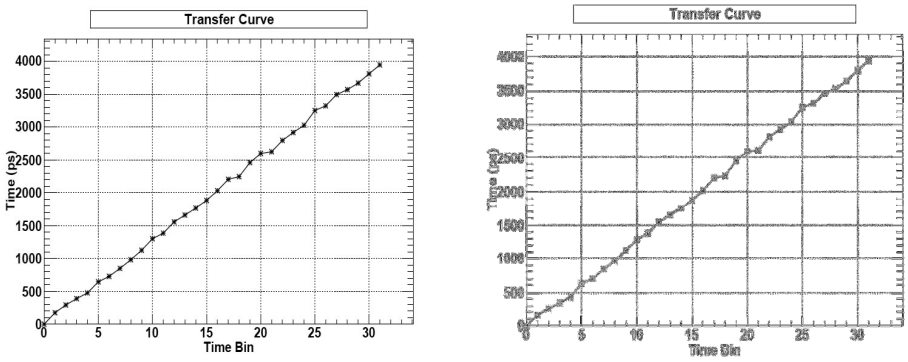

Fig.4.22 *TDC transfer function. Rising edge leading (left) and rising edge trailing (right).*

4.6 TDC per pixel prototype

A different architecture of the GTK readout chip was developed by the Torino group of the NA62 collaboration. The system simulation and the design of a part of the chip have been the part of the subject of the present doctoral thesis. The ASIC is in CMOS 130 nm technology and it has been submitted in 2009. Tests started at the beginning of February 2010.

4.6.1 Global architecture

The basic principle of the TDC per pixel architecture (P-TDC) is to perform the time walk compensation by a constant fraction discriminator filter (CFD) and the fine time measurement by a time to amplitude converter (TAC) based TDC. Thanks to the relative small area occupied by the TAC, it is possible to implement a single TDC for each pixel cell. In this way

most of the digital operations are performed inside the pixel cell, including the time to digital conversion and the multi event buffering. The simplified block diagram of this architecture is presented below.

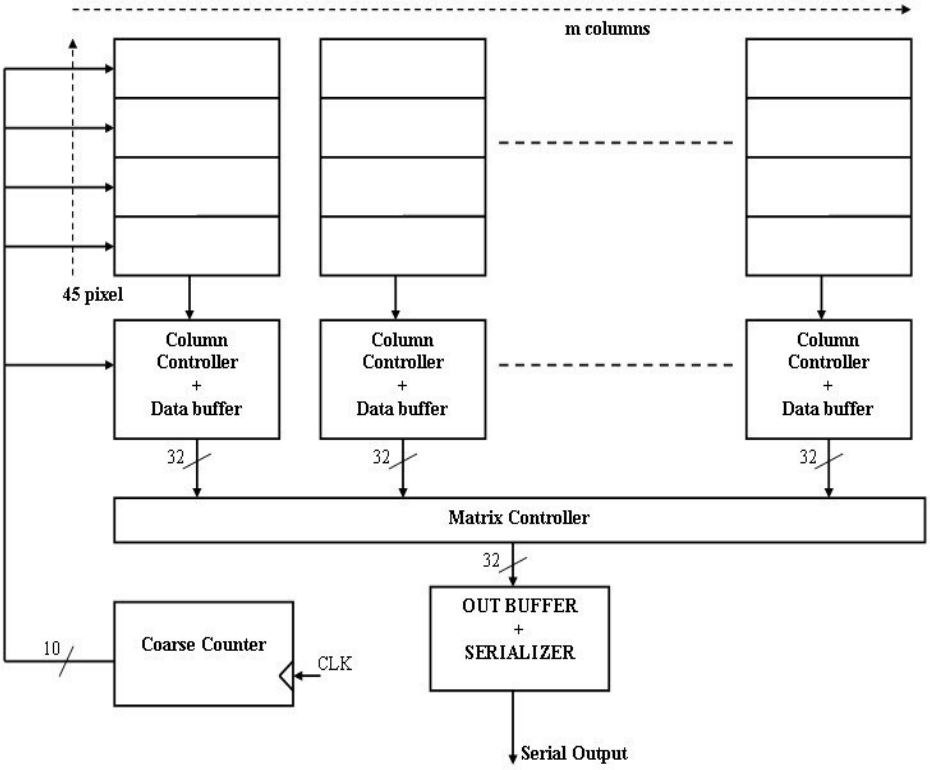

Fig. 4.23 *Simplified block diagram of the P-TDC architecture.*

Since the time conversion is performed on the pixel, it is necessary to propagate the clock signal and the Coarse Counter bus (which is Gray encoded) through the whole chip. In this option only digital signals are exchanged from the pixel matrix to the periphery of the chip. Of course the clock signal, with the frequency of 160 MHz, is the most critical and must be distributed with high precision. For this purpose it is used a dedicated transmission line for each pair of columns. Then each column of 45 pixels is readout by a dedicated controller. A merging block prepares the data for the serializer performing also additional checks. The number of merged columns will depend on the speed of the chosen serializer.

4.6.2 The P-TDC pixel cell

The pixel scheme is depicted in Fig. 4.24. It is based on a pre-amplifier followed by a CFD in order to keep the time resolution against time walk variations. A 10 bits time stamp information, with a time resolution of 6,25 ns (1 clock cycle at 160 MHz) is distributed in parallel to all pixels.

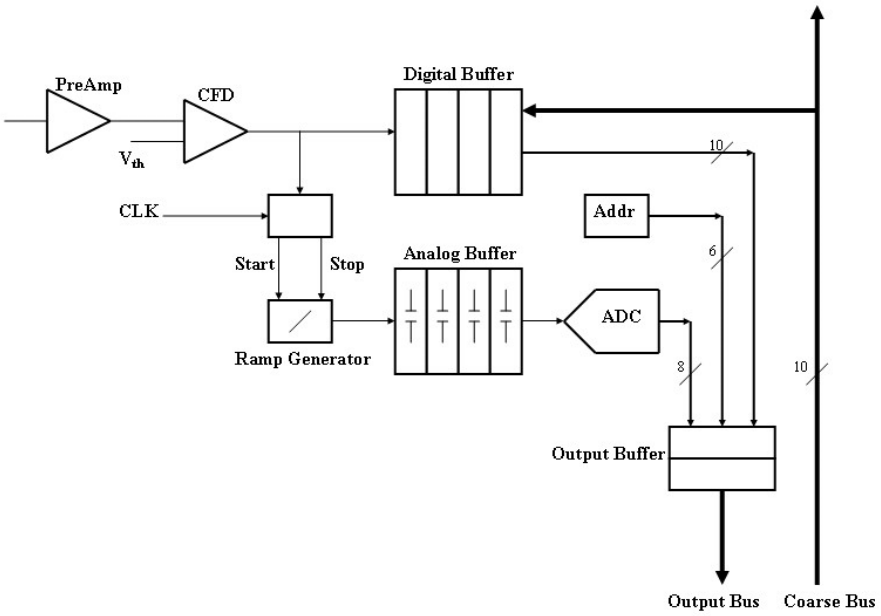

Fig. 4.24 *The pixel scheme.*

The time stamp is obtained from a Gray counter in order to avoid synchronization problems. The time information is split in two parts: a coarse time information, with the clock timing resolution, is directly obtained by storing the time stamp value at the rising edge of the CFD output. The fine time information is measured by starting a calibrated voltage ramp at the CFD rising edge and stopping it at the next clock rising edge. The measure of the voltage reached by the ramp, which is proportional to the time elapsed between the occurrence of the CFD pulse and a known clock transition, gives the timing distance between the incoming signal and the clock rising edge. The obtained voltage is therefore converted by a Wilkinson typology ADC , thus giving the fine measurement

in a digital form. The voltage ramp is obtained integrating a calibrated current on a storage capacitor.

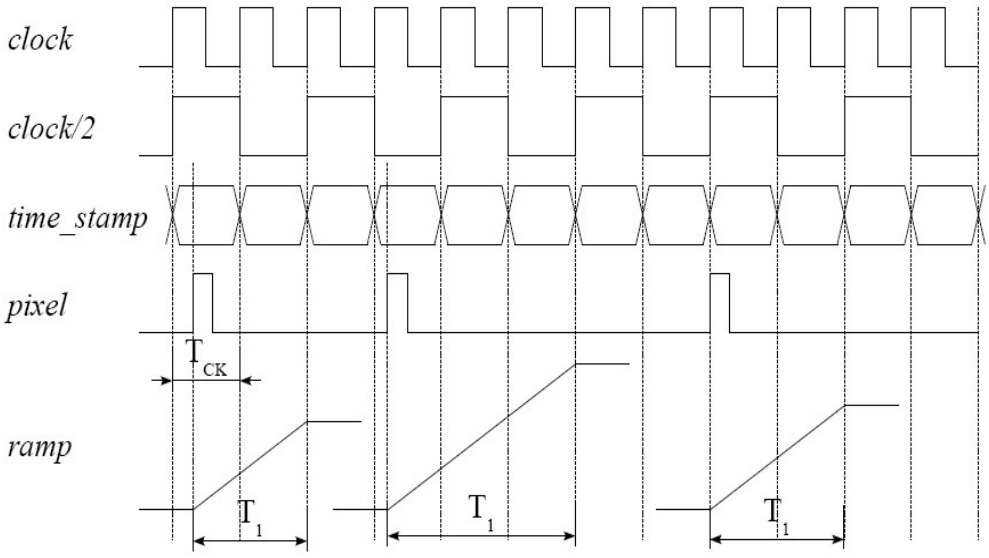

Fig. 4.25 *The analogue ramp for the TDC generation mechanism.*

The clock period is 6,25 ns, which, for a 6-bit fine time stamp, corresponds to a bin of 100 ps. However, one must take into account the possibility of timing misalignment between the coarse and the fine time logic which might occur when the CFD fires in close proximity of a clock transition. Furthermore, one must guarantee to the circuits generating the voltage ramp an adequate time for settling. For these reasons the TDC logic works at half the master clock frequency (80 MHz). Some relevant timing waveforms are shown in Fig. 4.25. The ramp is stopped on the first leading edge of the 80 MHz clock following a trailing edge. In this way a time offset is added and the risk of halting the ramp immediately after the occurrence of the CFD pulse is avoided. Given that the maximum time length of the charging ramp is 3 master clock cycles, or 18,75 ns. The A/D conversion is performed by discharging the storage capacitor with a second current generator. The ratio between the charging and discharging currents is set to 64:1, so the maximum discharge time will be 1,2 μs. With a time bin of 97,65 ps the

18,75 ns can be covered with 192 codes, hence the ramp is digitized with 7,5 bits equivalent resolution. With such an arrangement the LSB of the coarse counter and the MSB of the fine counter overlap, thus giving the possibility of a digital error correction [55]. The complete time information is therefore encoded in 18 bit: 10 bit (coarse) + 8 bit (fine) and with the clock frequency of 160 MHz the 18-bit word will cover a time range of 6,5 μs. Due to the expected pixel rate of 140 kHz, with the conversion time up to 1,2 μs, it is mandatory to implement a multi-buffering scheme. A 4-event FIFO has been adopted for both the digital coarse time information and the analogue fine time ramp final voltage. It is therefore possible to de-randomize the incoming data, thus relaxing the requirements for the pixel readout. The multi-buffer scheme has been simulated using VHDL in order to calculate the buffers depth (see next section).

4.6.3 Pixel rate simulation

In order to calculate the required depth of the buffers hosted in the pixel cell, it was performed an accurate simulations using the Hardware Description Language (VHDL). From a theoretical approach, according to the queue theory, one could estimate the buffers depth using the following formula [57]:

$$P_{LOST}(n) = 1 - \sum_{0}^{n} \frac{\rho^n e^{-\rho}}{n!}$$

Where P_{LOST} represents the probability of losing one event , n is the depth of multi-level buffers and ρ is the product between the event rate (with a Poisson distribution) and the mean time the data are stored in the buffers. In our case the ρ=0,14, derived from the maximum expected pixel rate, 140 kHz, and the conversion time, 1 μs.

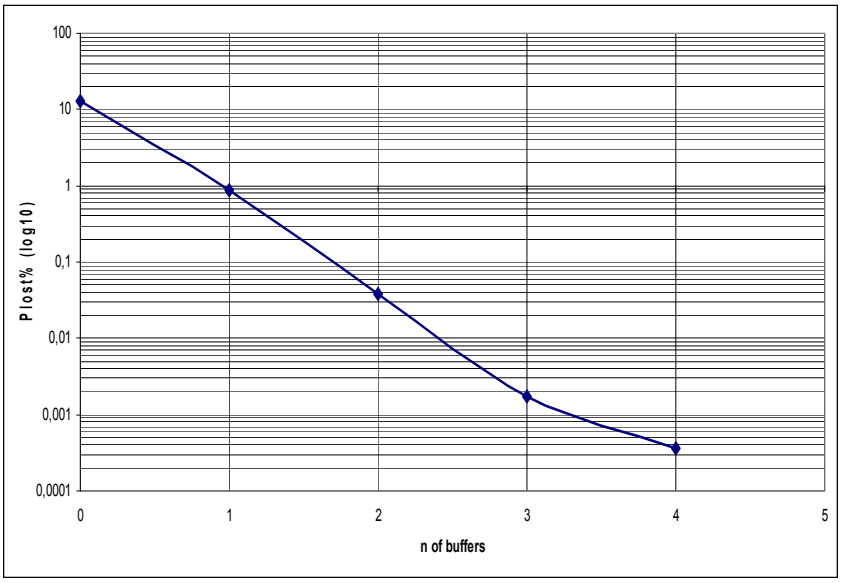

Fig. 4.26 P_{LOST} *in percent for number of buffers from 0 to 4 (log10 scale).*

Fig. 4.26 shows the probability of losing an event as a function of the number of buffers. One can observe that the inefficiency can be drastically decreased with the insertion of few buffers. To confirm these theoretical predictions several simulations were performed, using the VHDL model of the pixel showed in Fig. 4.27.

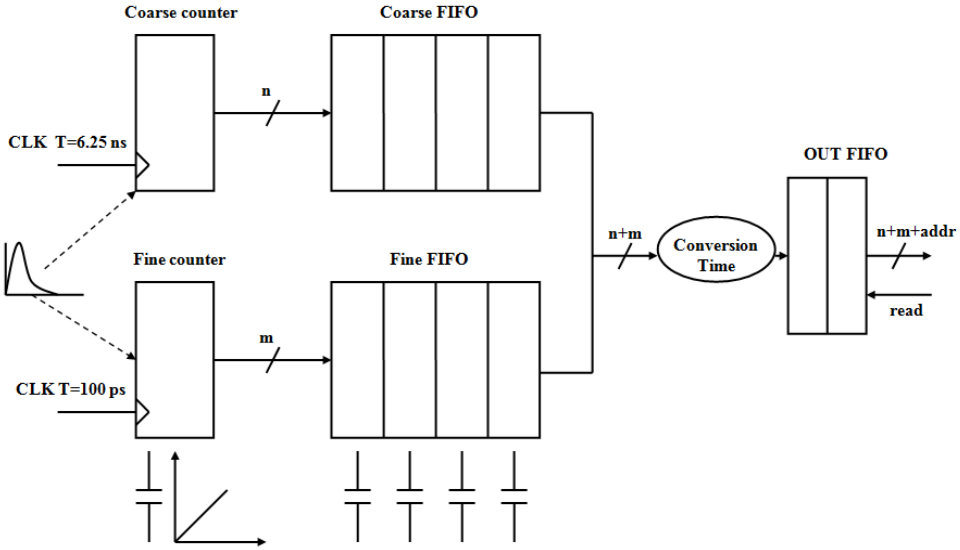

Fig. 4 .27 *The pixel model for multi-event buffer simulations.*

The coarse time information is a clock counter working at 160 MHz. The TDC here is represented as a second clock counter with the time resolution of 100 ps. At the arrival time of the hit, both of them are latched into two different FIFOs. After the conversion time the two FIFOs are readout and the data are merged to form the final time information. An output buffer stores the full word before sending the data to the End Of Column control logic (see section 4.6.6).

First one should consider that the physical events in the GTK pixel follows a Poisson time distribution. This means that the time distance between two consecutive events are exponentially distributed. The simulation program steps through the following:

- Generates the hit at the rate of 140 kHz following the exponential distribution (for the VHDL the distribution is provided by the Synopsys package)
- Write a text file with the exact simulator time
- Fine and coarse time are stored in their FIFO
- The FIFO is readout after the conversion time (1 μs, fixed)
- The output buffer is readout every 1 μs (first estimation of the End of Column controller behaviour)
- The data coming out from the output buffer are decoded by a program in C++ and the time information is compared with the one in the previous text file. Number of lost events due to the buffers occupancy or the dead time are reported in Table 4.1 for several value of hit rate and read-out time.

The probability to lose an event arises from two different conditions. The first one is the dead time of the preamplifier. Depending on the charge of the input signal this can extend up to ~20 ns. In the pixel model the above figure was set to a fixed time of 40 ns. The second condition is due to the buffer occupancy.

Hit rate	Conversion time (ns)	Readout time	Lost data 3-level buffer	Lost data 4-level buffer	Lost data preamp. dead time
140 kHz	1000	1 μs	4	0	10
140 kHz	550-1300	575 ns	5	0	14
150 kHz	550-1300	575 ns	5	0	15
160 kHz	550-1300	575 ns	5	0	18
170 kHz	550-1300	575 ns	8	0	18
180 kHz	550-1300	575 ns	10	0	19
190 kHz	550-1300	575 ns	11	0	21
200 kHz	550-1300	575 ns	13	1	25
210 kHz	550-1300	575 ns	16	1	25
220 kHz	550-1300	575 ns	19	1	22
230 kHz	550-1300	575 ns	22	1	24
240 kHz	550-1300	575 ns	28	1	26
250 kHz	550-1300	575 ns	36	1	28

Table 4.1 *Simulation results (10k events).*

The simulation in total generates 10000 events, that in the Synopsys package are occupying 8k words. To exclude systematic effects due to the randomness of the simulation, the simulation was repeated with different seeds of the exponential distribution.

To be more realistic a second set of simulations was performed adding a variable conversion time and tuning the output buffer readout time to 575 ns, which is the exact behaviour of the End of Colum logic. In this case the conversion time follows a normal distribution between 550 and 1300 ns, which are the real values of the TDC circuit (section 4.6.4.3). It was also tried to increase the pixel rate in order to evaluate the impact on the model.

The overall results of these simulations are reported in Table 4.1 and they are comparable with the theoretical predictions.

4.6.4 The analogue blocks in the pixel cell

The analog pixel section contains the preamplifier, CFD filter, discriminator, TAC and TDC circuits and their control circuits, as showed in the following diagram.

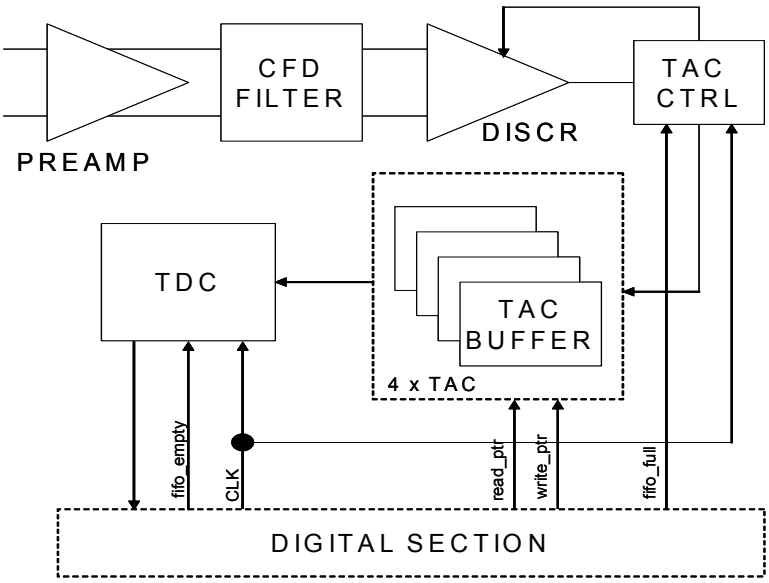

Fig. 4.28 *Block diagram of the analogue elements.*

4.6.4.1 The preamplifier

The front-end amplifier, reported in Fig. 4.29, is a transimpedance amplifier with fully differential outputs. Only the first stage is cascoded, while for the latter stage the cascode architectures were omitted since higher gain of the stage would have lead to instability. The baseline choice for the sensor material is p-in-n, however the front-end amplifier has been designed to be compliant with signal of either polarity to maintain the possibility of a different option in future upgrades of the Gigatracker.

The preamplifier has a nominal peaking time of 5 ns, a gain of 80 mV/fC and is designed to be linear up to 10 fC. The heavy radiation load to which the sensors will be exposed will increase significantly the leakage current, thus a compensation system has been provided. This system consists of a low pass filter formed by resistor R4 –R5 and capacitor C2-C3.

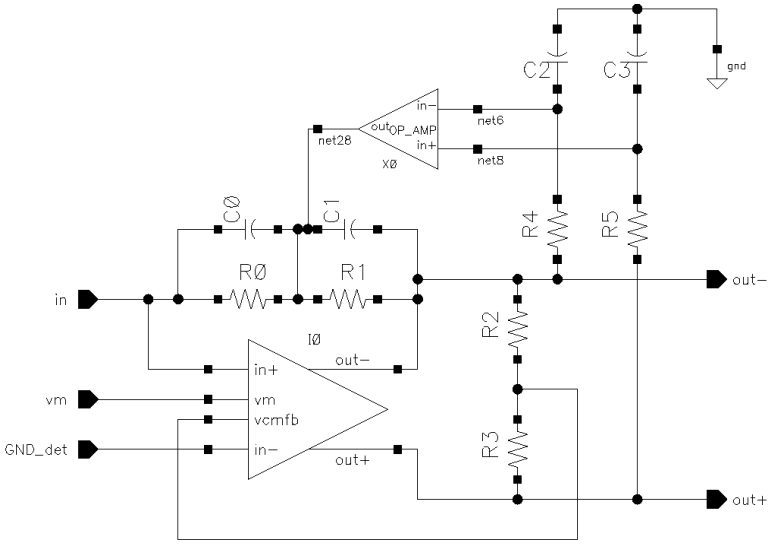

Fig. 4.29 *Block diagram of the preamplifier and leakage compensate circuit.*

If there was no common-mode mismatch, no current should flow through feedback resistors R0 and R1. With mismatch and in absence of leakage current from the detector, this current is provided by the leakage compensation op-amp, to resistor R1. This, in turn, calls for a differential offset at the output of the preamp.

4.6.4.2 The constant fraction discriminator filter

The presented CFD is formed by a passive RC filter followed by a three stage discriminator (Fig. 4.30). A constant fraction discriminator works by comparing a delayed and an inverted-attenuated copy of the input signal. In an integrated implementation the delay line can be emulated with a RC filter. Since the circuit has a fully differential topology, the signal fraction can be obtained by cross-connecting two resistors between the outputs of the filter and the outputs of the front-end amplifier [56]. From the point of view of jitter minimization the zero crossing should occur at the point of maximum slope. In our design this requires to set the fraction to one half of the signal. Statistical fluctuations of the signal generation process in the sensor may however results in a variation of the signal shape, which would

lead to an additional jitter component. To minimize this effect it is beneficial to reduce the fraction at which the zero crossing occurs. In the circuit, the attenuation fraction can be programmed by a configuration bit to be either 50% (which minimizes the noise contribution to the jitter) or 30 % (which reduces the effect of signal shape variations) [55].

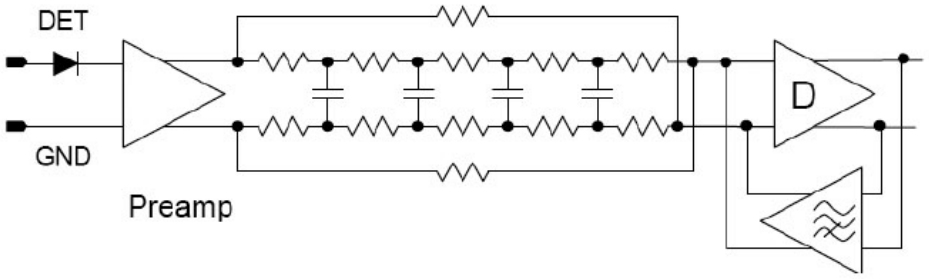

Fig. 4.30 *The schematic of the CFD: the two cross-connected resistors generate the signal fraction while the cascaded low-pass filters generate the delay.*

After the filter, the signal is amplified and then is presented to the zero-crossing detector (block D in Fig. 4.30). A typical problem is that this circuit has a nominal threshold equal to the baseline, so it fires continuously also on noise. To prevent these spurious hits from propagating to the rest of the system the output of the zero crossing detector is usually put in logical AND with the one of a leading edge discriminator. The input of this stage is connected to the non-delayed output of the front-end amplifier and a threshold well above the baseline is set in order to suppress the noise. The leading edge comparator fires before the zero-crossing, “arming” in this way the logical gate and allowing the propagation also of the walk-free signal. One problem in using this approach in our design is that in a final implementation the ASIC will have 1800 channels. Having a stage that fires continuously is then a primary concern. For these reasons it has been preferred to implement an alternative approach, based on the use of a “dynamic” hysteresis. The working of the circuit can be understood with the help of Fig. 4.30, which displays the most relevant waveforms.

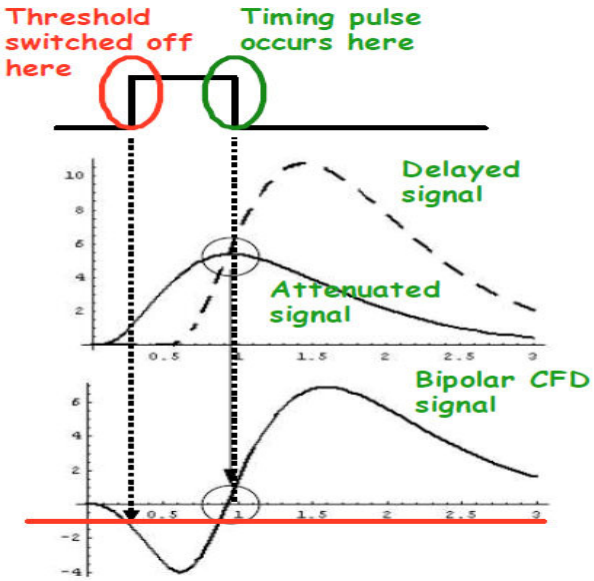

Fig. 4.31 *CFD relevant waveforms.*

The signal from the previous stage is the bipolar waveform shown in the bottom part of Fig. 4.31. The red horizontal line is the differential threshold that unbalances the circuit and avoids triggering on noise. When the threshold is crossed the leading edge transition occurs and this information is used to disable the threshold itself. The high-to low transition occurs then at the zero crossing point. After the zero-crossing a differential-to-single ended converter generated a CMOS pulse that is propagated to the rest of the circuitry.

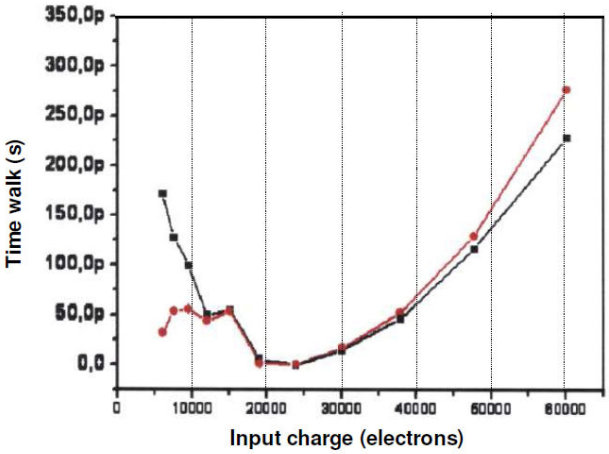

Fig. 4.32 *Measured performance on the CFD prototype.*

The CFD was previously prototyped as a separate chip. The experimental results have shown that the circuit achieves an optimal walk correction for an input signal of 24000 electrons. As it can be seen in Fig. 4.32, the time walk peak-to-peak is always smaller than 300 ps in the dynamic range of interest [56].

4.6.4.3 The TAC based TDC

To better understand the behavior of the TAC based TDC it is necessary to describe the circuit used to generate the voltage ramp, which is reported in Fig. 4.33.

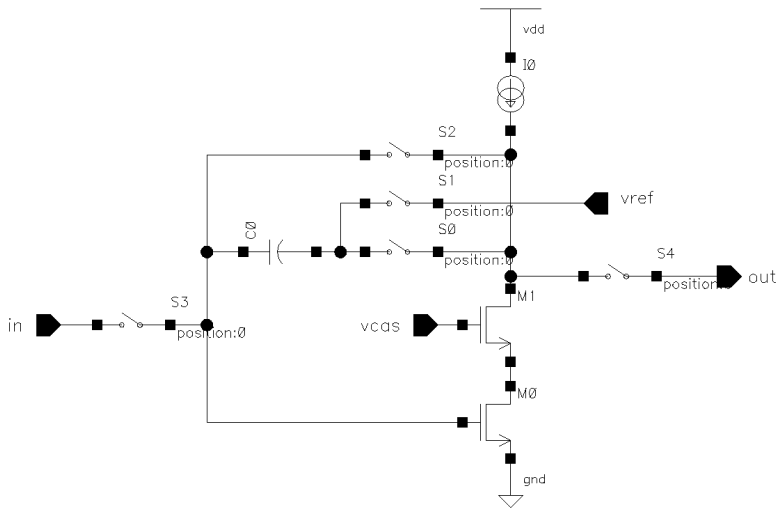

Fig. 4.33 *The Time to Amplitude Converter (TAC).*

The circuit contains a cascode common source amplifier, a linear metal-to-metal capacitor and a set of four switches. When S0 is open and S1-S2 are closed, the circuit is in the reset mode. When the vice-versa is true, the circuit is in the normal operating mode. The CFD triggers the closing of S3, which connects the input node to a constant current source. The current enters into the input node, therefore the output voltage is pulled down. Four of these circuits are located in every pixel, so four voltage ramps can be generated one after the other, thereby providing the analog multi-buffering

capability. In the schematic of the whole TDC, which is shown in Fig. 4.34 [55], the four TAC circuits are represented by the four capacitors enclosed in boxes.

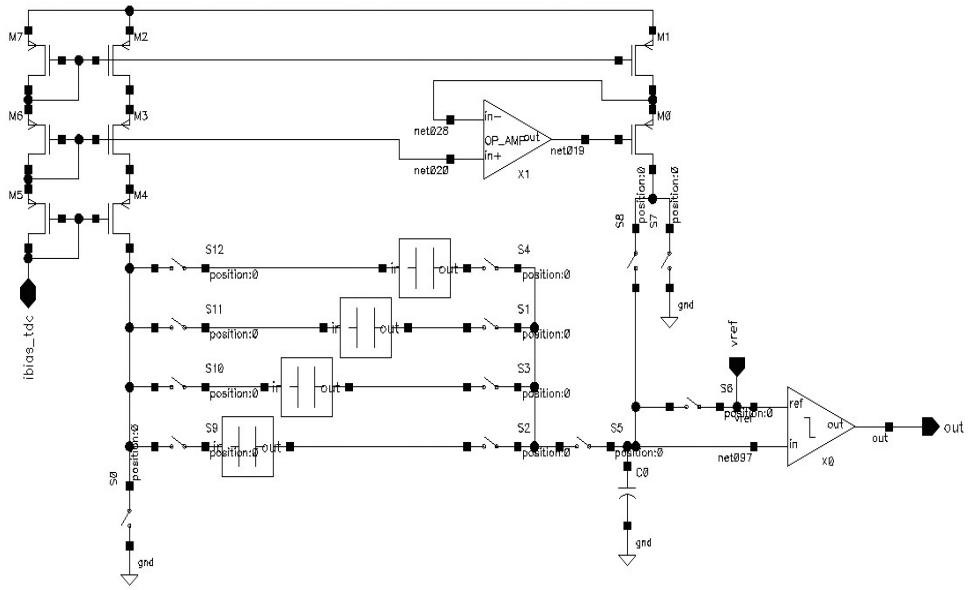

Fig. 4.34 *Simplified block diagram of the TDC circuit.*

Transistors M2-M4 form the current source creating the ramp. In the idle state this current is diverted to ground. When the CFD fires the current source is connected to one of the four TAC. When the ramp is completed the output of the TAC is sampled on capacitor C0. One has to note that since the output voltage of the TAC will be less then V_{ref}, the sampling will actually discharge C0. Therefore, C0 must be recharged to restore the baseline. This implies that one needs here a current source of the same polarity of the one that generates the voltage ramp. The ratio between the sampling capacitor and the feedback capacitor CF used in the TAC can be exploited to reduce the ratio between the current sources. For instance, in a straightforward 6 bits implementation, the current restoring the baseline on C0 should be 64 times smaller than the one used in the TAC. However, if C0 is four times CF the ratio required is reduced to sixteen, allowing for a significant saving in the total circuit area. In our case we want to have a time bin of 100 ps and cover a dynamic range of 18,75 ns. This is equivalent

to requiring a resolution of 8 bits over a range of 25 ns. If one would achieve this resolution just by scaling the currents a ratio of 256 would be required. However the time needed to restore the baseline is measured with the master clock cycle (6,25 ns) gaining a factor of four. Another factor of four is obtained by making C0 four times bigger than CF, therefore the ratio necessary between the two current sources is only sixteen [55].

4.6.5 The demonstrator chip of the P-TDC architecture

In order to evaluate the performances of the building blocks of the P-TDC architecture and the feasibility of the whole architecture, a prototype has been submitted in 2009. The chip is implemented in CMOS 130 nm technology (IBM CMOS8RF design kit with the DM metallization option) and at the moment is still under test. The prototype includes two 45 cells columns and one 15 cells column. Each cell is 300 × 300 μm^2. The end of column circuit with buffers and control logic has also been implemented .

The prototype has 118 pads which are organized in the following way :

1. 40 pads for the analogue part, organized in two 20 pads rows on the left part of the top side of the chip
2. 60 pads for the digital part, organized in two 30 pads rows on the right part of the top side of the chip
3. 9 pads for the analogue test cell, located on one column on the left side of the chip

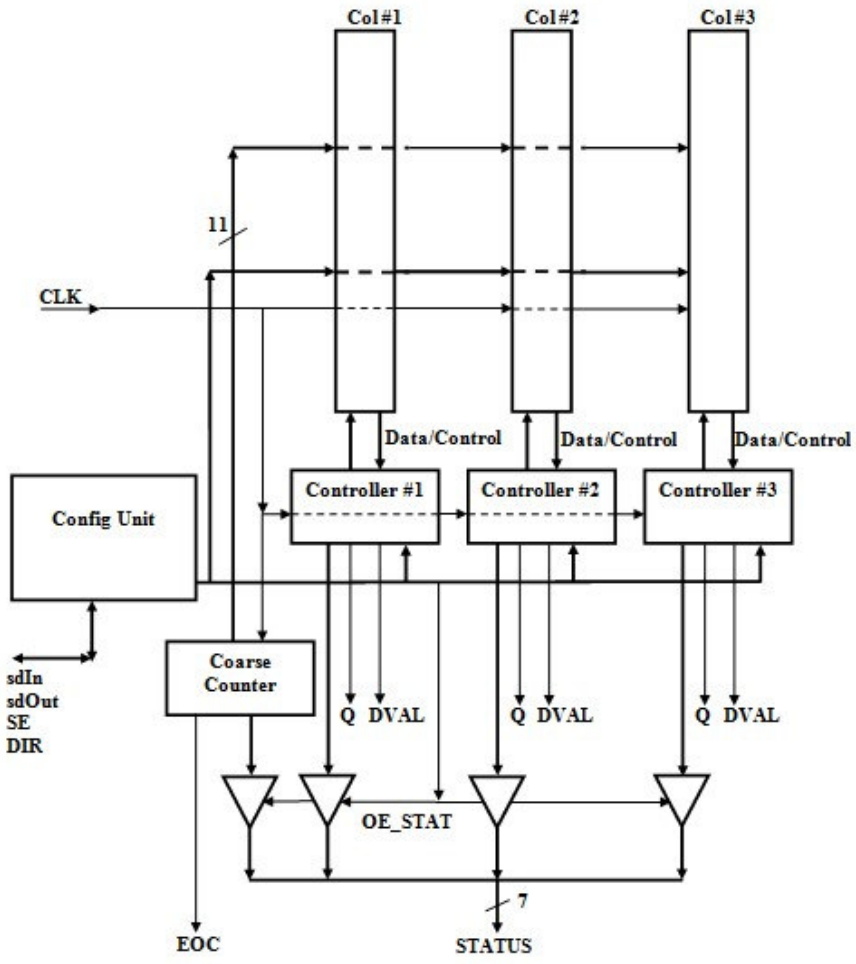

Fig. 4.35. *Block diagram of the P-TDC demonstrator chip.*

All the pads are differential (LVDS 2,5 V) except for the status bus which is single ended (CMOS 1,2V) . The chip layout is organized as showed in Fig. 4.36.

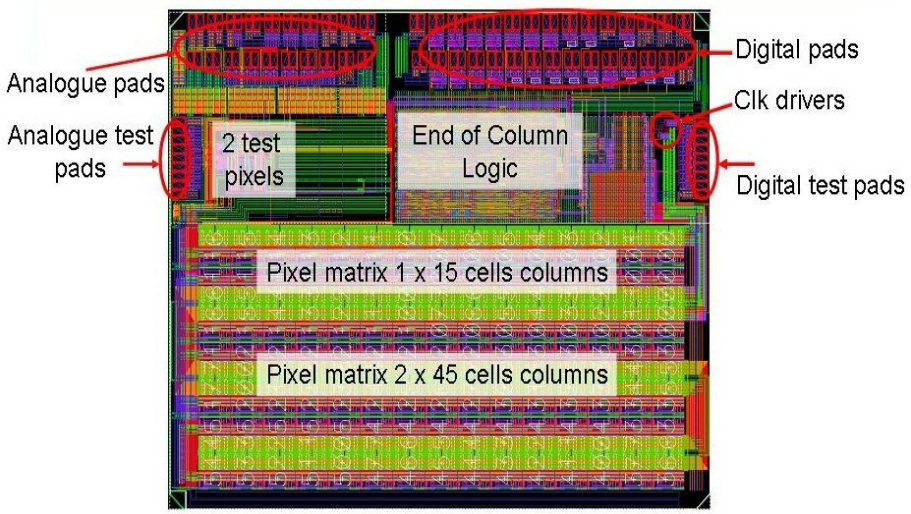

Fig. 4.36 *The P-TDC prototype's layout.*

The pixels columns are folded in order to satisfy the requests on the relative sizes of the ASIC prototypes. In addition to the three columns of pixels there are two spare cells which are equipped only with the analogue components. Their output are directly connected to the analogue test pads in order to see the behavior of the single blocks: preamplifier, CFD filter and the TAC circuit.

The clock signal has the nominal frequency of 160 MHz and it is distributed with a minimal skew to the whole chip. A single 10-bit clock counter, which can be configured both as binary or Gray, provides the coarse time information for the whole pixel matrix. The readout of the columns is performed by identical End of Column controllers (see next section) working in parallel.

The global configuration is stored in a 32-bit shift register with serial access, Chip Configuration Register (CCR). Another 8-bit register is implemented in each pixel cell for the local configuration. They are accessed through the same CCR input port by a multiplexing system. For each single pixel cell it is possible to define the discriminator threshold and the TAC discharge current, furthermore the pixel cell can be configured to work in test mode, stimulated by an external test pulse signal, or masked.

Finally a digital status bus is presented at the digital test pads. The seven outputs are configurable and through them it is possible to monitor the internal coarse counter, the state machines of the End of Column circuits, and the detected single event upset errors.

All the digital logic, in both the pixel cell and the end of column, is designed to be single event upset protected making use of Hamming encoded registers, buffers and state machines (see section 4.6.8 for details) or triple redundant flip-flops. The circuits are capable of single error correction or double error detection every clock cycle.

4.6.6 The End of Column logic of the P-TDC demonstrator chip

The block diagram of the End of Column controller is sketched in Fig. 4.37. A differential 26-bit digital bus with pre-emphasis driver connects the pixel column with the End of Column controller. The circuit is the same for the 45 or 15 pixels columns implemented in the demonstrator chip.

The coarse time information is sent to the 45 pixels. A simple state machine (Fig. 4.38) sends a read enable signal to the pixels, using a token ring mechanism. The read enable is then distributed from one pixel to the other one. Each pixel, when the read enable is on, writes out the data content and its empty FIFO flag in two clock cycles. The total time for reading the whole 45 pixels column is then 575 ns. In addition a busy signal alerts the End of Column FSM if there are available data or not in at least one of the 45 pixels.

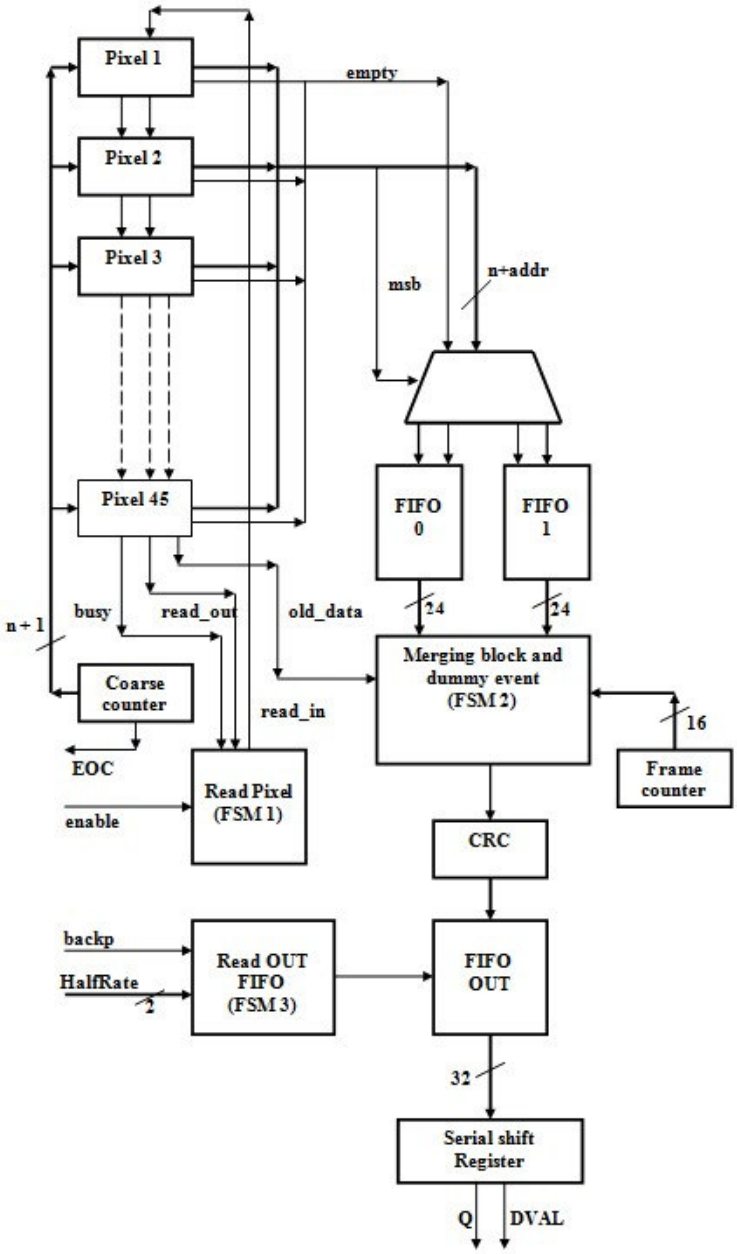

Fig. 4.37 *The End of Column block diagram.*

In order to avoid ambiguities in the time reconstruction, it is necessary to regroup each data frame inside the correct turn of the coarse counter. To do this the coarse counter sends to the pixels one more bit (11^{th} bit). This information is used to tag events of type 0 and events of type 1 (depending of the MSB bit) in two different FIFOs.

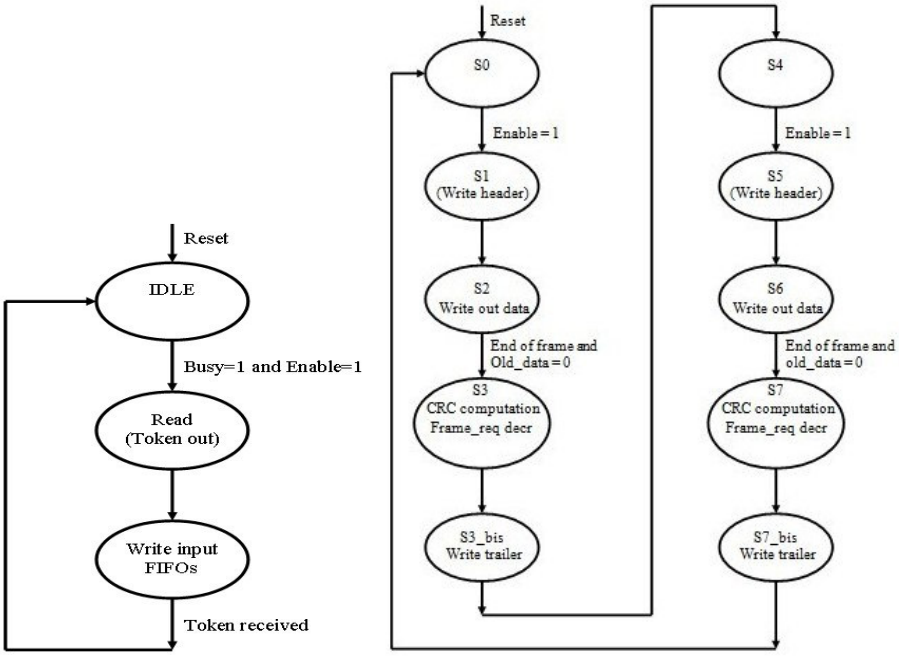

Fig. 4.38 *The input stage state machine (left) and the middle stage state machine (right).*

A second state machine (Fig. 4.38) works as merger circuit to reconstruct the right order of the data frames, adding trailer and header between consecutive frames . Inside the header the information of the frame counter is stored following the data format that is presented in section 4. To keep frames separated the circuit uses extra information provided by the pixel logic. A flag (old_data) is set in the pixel word whenever the frame changes and it contains data from the previous frame. This signal is propagated through the whole column via a fast-or.

The depth of the FIFOs has been calculated performing several simulations in VHDL. These simulations are similar to the ones performed on the single pixel and described in section 4.6.3. Since the expected average data rate for the central columns is 3,3 MHz (see Table 4.1) to infer a degree of safety, the simulations were performed with a data rate of 4,5 MHz. Events were generated according to an exponential distribution. Beingrecorded a maximum FIFO occupancy of 20, it was concluded that the FIFO depth

could be safely set to 32. The three FIFOs of the End of Column logic are built around single memory cells based on D flip-flops rewritten every clock cycle. This architecture gives a better robustness against Single Event Upset than a RAM based memory cell.

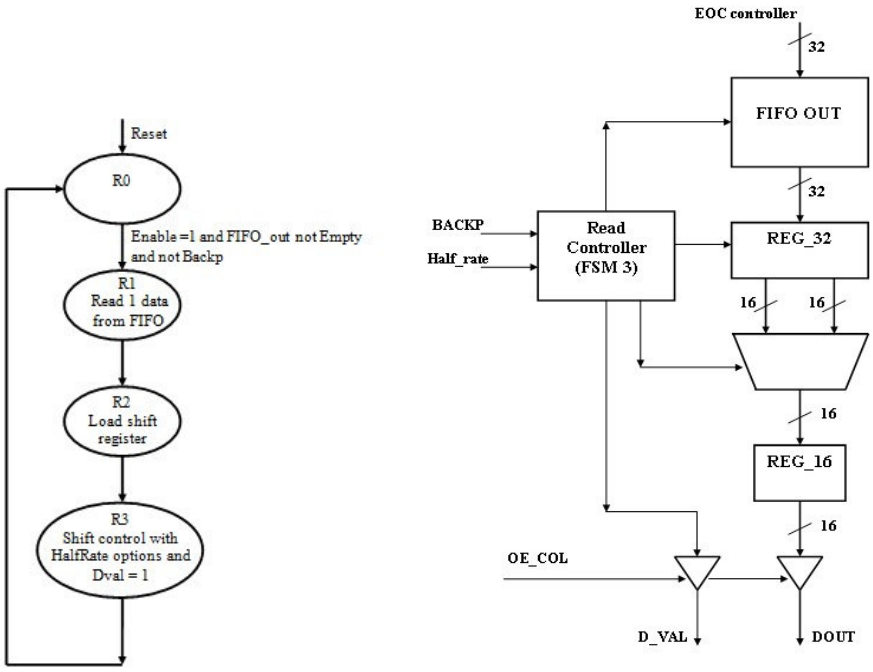

Fig. 4.39 *The output stage state machine (left) and block diagram (right).*

The output stage of the circuit provides the readout of the output FIFO as shown in Fig. 4.39. In order to reduce the number of pins, the End of Column controller has a serial data output implemented with a 32-bit shift register. In principle the reading mechanism is fully automatic. The controller sends the 32-bit word to the shift register and a flag signal (d_val), which is synchronous to serial output (Q) to indicate when the data are valid. A backpressure signal (backp) can stop the reading mechanism, but in this case the output FIFO will still be written by the End of Column controller.

In addition there are two other signals that can be used to slow down the readout (HalfRate [1:0]) . If this feature is enabled the output data stream

can be synchronized with a 80, 40 or 20 MHz clock instead of the nominal 160 MHz clock.

The layout area of the End of Column controller is 1500 µm x 300 µm, being the latter figure constrained by the pixel cell width.

The routing has been done in the layers M1-M3, MQ and MG.

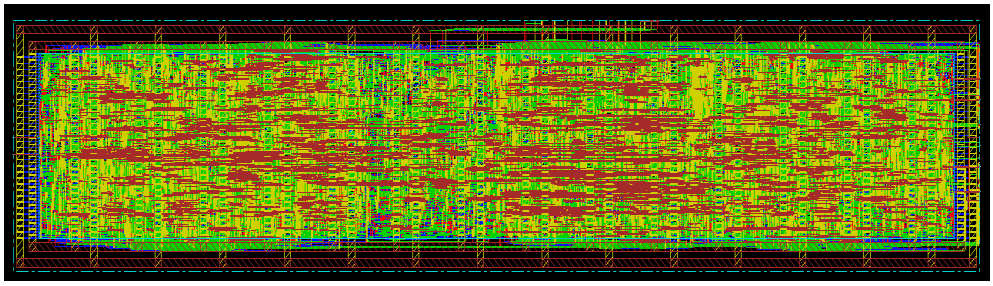

Fig. 4.40 *The End of Column layout.*

The expected power consumption of each End of Column circuit was simulated using the Value Change Dump (VCD) files generated by the post-routing simulations. These take into account the real switching activity of all the digital signals in the circuit. The power analysis performed with VDD at 1,08 V, which is a worse case condition gives the following results:

- average power(default): 1.1919e+01 mW
- average switching power(default): 3.4295e+00 mW
- average internal power(default): 8.4772e+00 mW
- average leakage power(default): 1.2427e-02 mW

4.6.7 Data format

The data format of the End of Column output is described in Fig 4.41. A data frame consists of all the data which belong to the same turn of the coarse counter and they are encapsulated between headers and trailers. Most significant bit [31:29] are used as identifier for headers and trailers.

With the clock frequency at 160 MHz and the coarse time information spread on 10 bits, the frame interval is 6,4 µs.

The total overhead per column due to header and trailer is: 2/(4,5 MHz * 6,5 µs) = 7 % . For the final implementation of the readout chip, the overhead is

considered too large. Thus headers and trailers will be added for every group of merged columns.

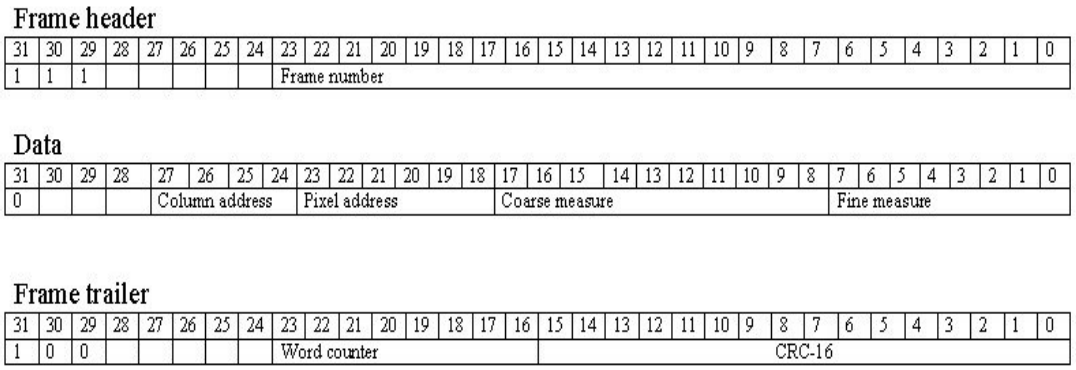

Fig 4.41 *End of Column data format.*

In order to guarantee to the DAQ the possibility of checking the data transmission, the trailer contains a Cyclic Redundancy Check (CRC) control. The CRC code implementation follows the CRC-16, which corresponds to the IBM standard as implemented in the Universal Serial Bus (USB) protocol. The polynomial form, which has been used, is: $X^{16}+X^{15}+X^{2}+1$. The CRC-16 is a rather common standard, which has also been used in the DAQ design of the CMS experiment at CERN. One should remark that in the trailer, when it is passed to the component for the CRC computation, the CRC field (bits 15 to 0) is forced to all 0. Then it is updated with the correct CRC value before to be sent. The trailer also gives the information of the length of the data frame by a 8-bit counter (trailer bit 23-16).

4.6.8 Single Event Upset protection

Due to the high particle rates the Single Event Upset (SEU) protection is an issue for the digital electronics in the GTK readout chip. In the P-TDC prototype the following solutions have been adopted:

- Pixel cell: Hamming encoded registers, state machines with auto-correction (single error correction, double error detection)
- End of Column logic: Hamming encoded registers, state machines, and counters, with auto-correction (single error correction, double error detection). Triple redundancy architecture for single flip-flops (Triple Modular Redundancy, TMR).

Concerning the three FIFOs the following considerations have been done to estimate the SEU probability.

Recent studies [60] have been performed to determine the Single Event Effects (SEE) sensitivity of the 130 nm CMOS technology. By fitting a Weibull curve, it was evaluated that the cross section of a Static Random Access Memory (SRAM) circuit was ~$1x10^{-8}$ cm^2/bit for a linear energy transfer (LET) of 10 MeV cm^2/gr and it was increasing to $2x10^{-8}$ cm^2/bit for LET larger than 30 MeV cm^2/gr.

The particle flux in the End of Column area is expected 1% of the central GTK area, corresponding to 1.3 10^6 /sec cm^2 . Taking into account the collision probability is:

$$P(x) = e^{-X/L} = 3.3\ 10^{-6}$$

where X=1 μm (silicon active region) and L = 30 cm (free mean path for nuclear interactions) It has been estimated that the expected number of nuclear interaction is given by: 3.3 10^{-6} x 1.3 10^6 = 4.29/sec cm^2.

To translate to the probability of bit flipping, one ha to consider the number of flip-flop integrated in the circuit: a FIFO (D flip-flop based) of 32 words x 32-bit has 1206 flip-flop. Therefore the expected number of SEU per second is given by:

$$N_{SEU}/sec = 4.29\ 10^{-8} \text{ x } 1.2\ 10^3 = 5.14\ 10^{-5}/sec$$

Data in the FIFO are stored for at most 12 μs , so the probability to have a SEU effect is 6 10^{-10} for single errors and 10^{-19} for double errors. For these reasons the FIFOs have an Hamming encoder at the input and a Hamming decoder with auto correction at the output of the FIFO only and not on each data register. In addition, address counters are TMR protected.

For a detailed example of Hamming code implementation see Appendix A.

4.7 Summary on the two readout architectures

From the previous sections it is clear that the two architectures proposed for the GTK readout chip are totally different, each one with advantages and disadvantages.

The End Of Column architecture has the advantage of the pixel cell is completely analogue, which means less digital noise and less power consumption in that area. On other hands there is the difficulty of propagating the analogue signal of the Time over Threshold to the end of column TDC preserving the signal as much as possible. In addition the DLL TDC and the bus system distributed to all the columns, creates a consistent density in that area of the circuit, and also the digital noise can be an issue.

The P-TDC option has the advantage of propagating only digital signals between the pixel cells and the end of column controllers. Another important pro is the possibility to perform the first derandomization on the pixel cell itself. The system clock is slower than in the EOC architecture (160 MHz instead of 320 MHz), but its propagation is critical to keep the jitter and the skew at very low levels. Another important issue is the amount of generated data. While the EOC chip performs the time walk correction with a TOT and needs to measure both the rising edge and the falling edge of the signal, the CFD filter of the P-TDC architecture requires only one edge, reducing the amount of data to transmit.

About the radiation damages the EOC architecture has the advantage of having only analogue electronics on the most exposed area of the chip. This means that in the P-TDC architecture the digital electronics on the pixel cell requires a robust SEU protection.

At this moment it is impossible to say which is the best solution for the GTK readout chip and only with the experimental results of the two prototypes it is possible to decide which one to adopt.

Chapter 5

Preliminary results on the TDC per pixel prototype

The tests of this prototype just started in the beginning of February 2010 and the presented results are preliminary while the work is still ongoing.

5.1 Test setup

Two printed circuit boards have been developed in order to accommodate the chip (sensor card) and the connection with external instruments (adapter card). The sensor card, beside the chip, hosts also the DAC for setting the thresholds of the analogue elements of the GTK readout chip. Furthermore on the sensor card are accommodated the LVDS chips for the clock and the test pulse distribution. All the signals from and to the adapter card are LVDS differential, with the exception of the serial interface for the DAC programming.

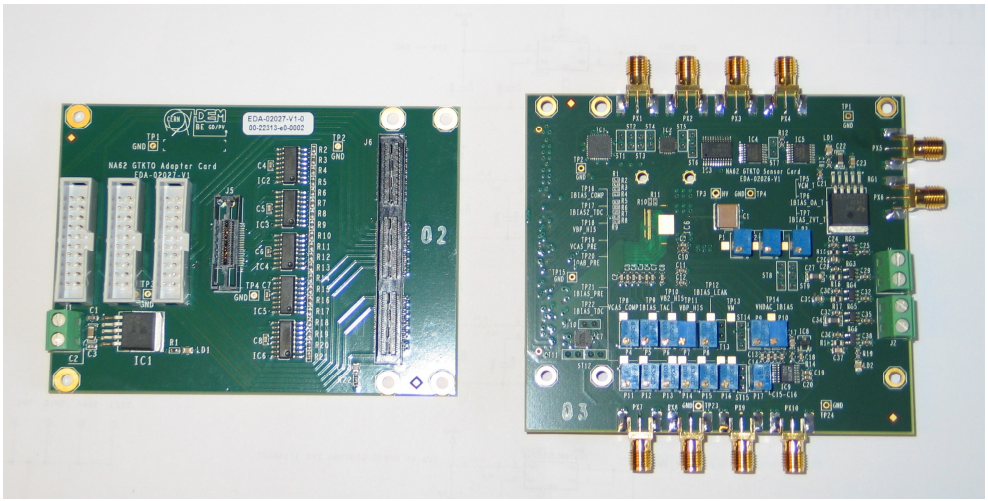

Fig. 5.1 *Adapter card (left) and sensor card (right).*

The idea is to use the sensor card in the preliminary tests connected to the adapter card (through a High Speed Mezzanine Card connector from Samtec) and from the adapter card to a pattern generator and a logic state analyzer (Agilent 16700 series). The simulations performed in VHDL language are used to create the stimulus of the pattern generator and decode the data captured by the analyzer. The clock for both instruments and the sensor card is generated by a demonstrator board of the Texas Instruments which mount the CDCE62005 chip. This is a clock synthesizer capable of generating clocks in a wide range of frequencies, single ended or differentials, with very low jitter [59].

The second phase of the tests foresees the use of an evaluation kit with the Altera StratixIII FPGA. Through the same HSMC connector the sensor card can be connected to the FPGA instead of the adapter card. Also the same sensor card with the wire bonded chip can be used for laser and beam tests with the sensor bump bonded on the top.

The wire bonding of the chip on the sensor card required a complicated PCB development. The pads pitch is 150 μm and they are organized in two rows as presented in figure 5.2.

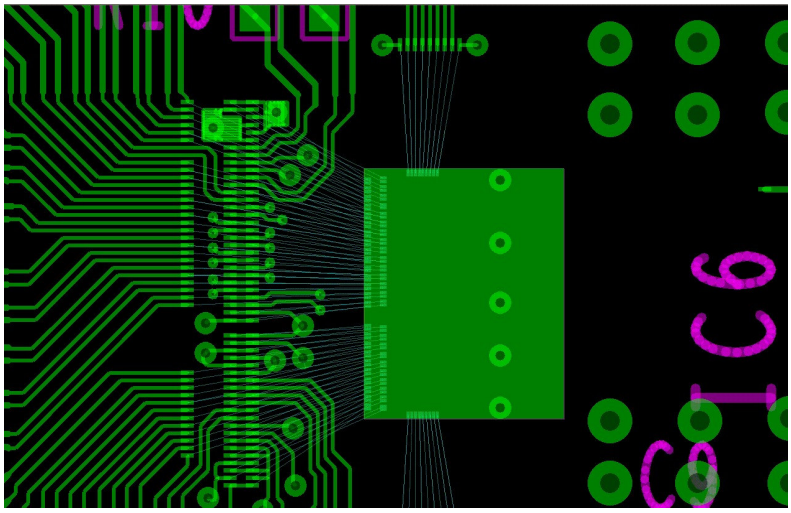

Fig 5.2 *Detail of the bonding area of the sensor card.*

5.2 Preliminary analogue results

The power consumptions have been measured with the chip configured as follows:

- one pixel in each column set in test mode;
- the test pulse running;
- the three End of Column readout active;
- the Coarse Counter in Gray mode.

The clock speed was set to the nominal value, 160 MHz. The current values are reported in the following table.

1,2V digital	1,2V digital (test pixels)	1,2V analogue	2,5 V LVDS pads
150 mA	30 mA	80 mA	60 mA

Table 5.1 *Power consumptions.*

The 1,2 V digital power supply serves all the standard cells in the ASIC, which comprise also the clock distribution and the differential data bus drivers. The power consumption scales linearly with the clock frequency as showed in the following chart. The leakage without clock is 30 mA.

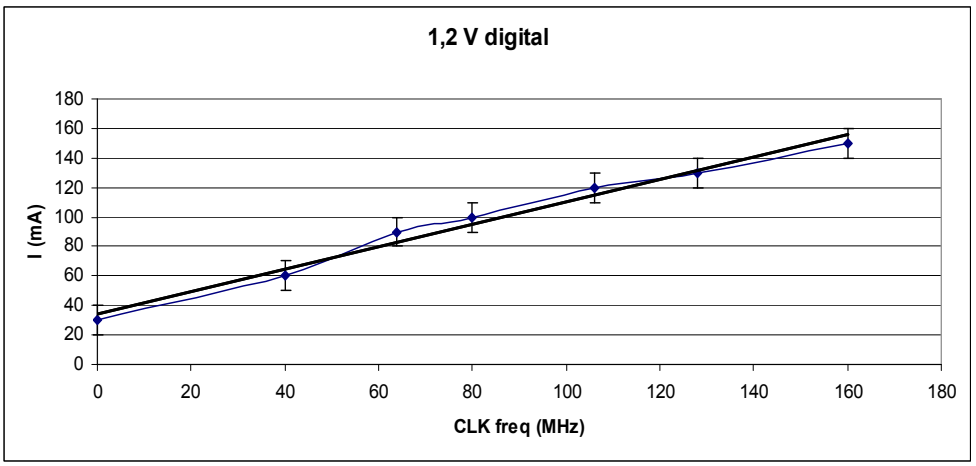

Fig 5.3 *Digital power consumption.*

The preamplifier has been characterized by checking the spare pixel designed for test purpose, with an input charge between 1 and 10 fC. The

peaking time (20%-80%) is constant with respect to the amplitude and it has been measured to be 4 ns. The plot reported in Fig. 5.4 shows the linearity of the preamplifier. To evaluate the gain one has to correct the output values for the attenuation, factor 3, of the output buffer. Moreover the measure has been performed on the single phase (positive) of the differential signal. The resulting gain is close to the design value of 60 mV/fC peak to peak.

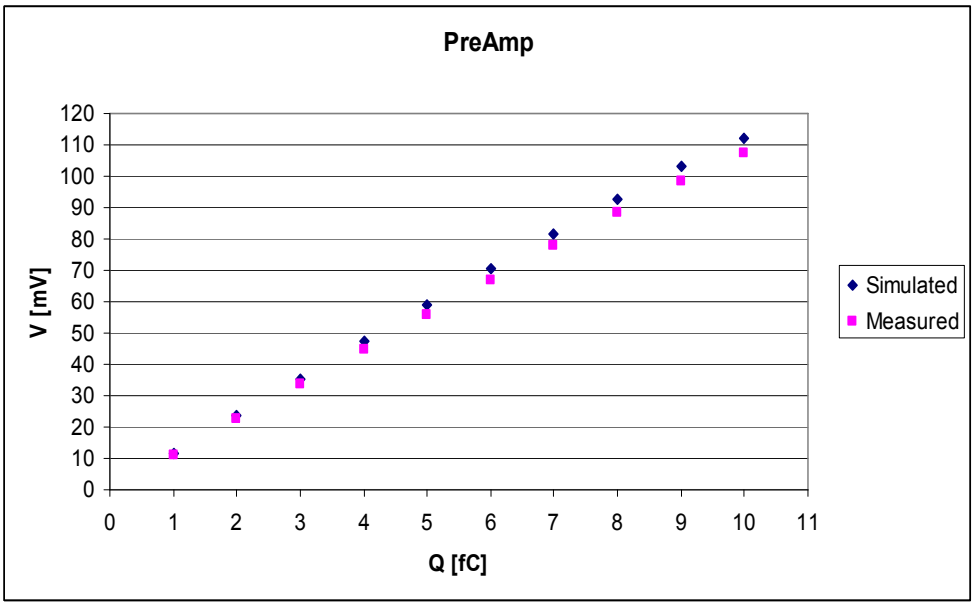

Fig. 5.4 *Preamplifier linearity curve.*

The measured noise at the preamplifier output is 5,2 mV peak to peak (p-p) without the clock signal. With the clock frequency at 160 MHz it is 8 mV p-p, while at 80 MHz is 9,8 mV p-p. The explanation of having a larger noise at lower clock frequency can be done in terms of charging and discharging effects on the input capacitance, which compensate each others at higher frequency. One should remark that this pixel cell has an input capacitor of 150 fF to emulate the sensor capacitor, while the pixels in the columns do not present the same capacitance. A typical signal at the preamplifier output is shown in Fig. 5.5, both when the clock is run at 80 and 160 MHz.

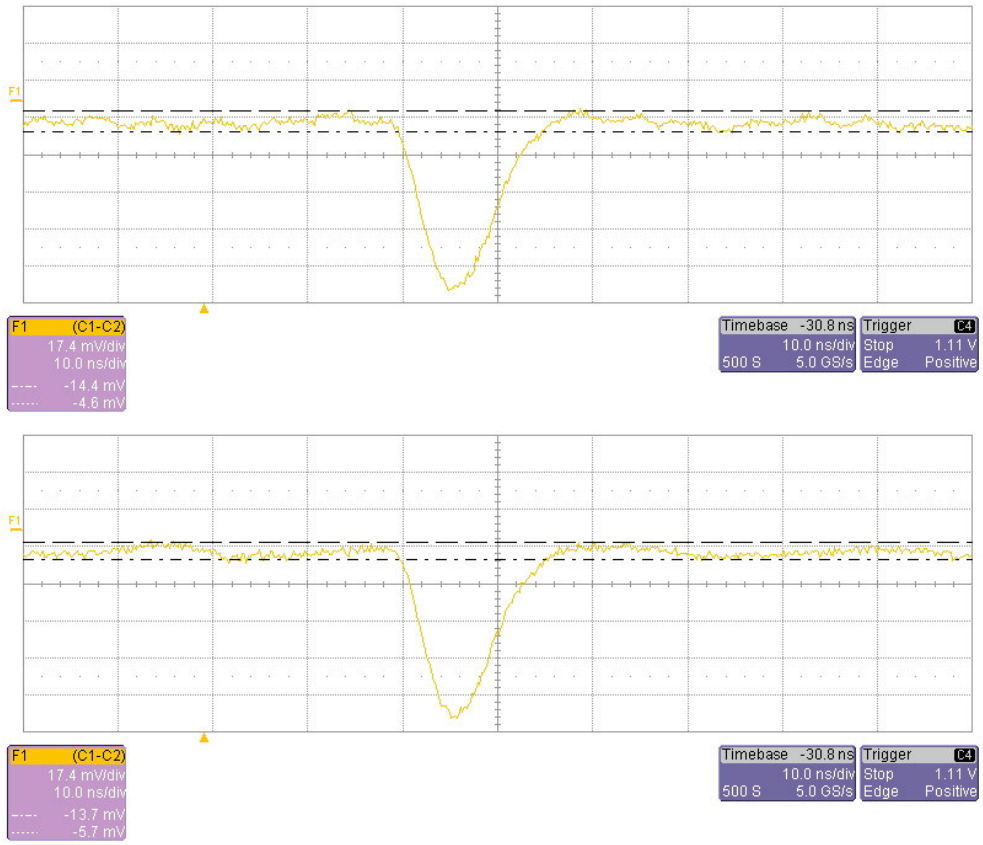

Fig. 5.5 *Output of the preamplifier with the clock frequency at 80 MHz (above) and 160 MHz (below).*

The CFD gain has been measured on the test pixel, observing the CFD output on the scope. The values for different injected charges are reported in the figure 5.6. For the test pixel, the CFD shares the same output buffer of the preamplifier with values which are attenuated by a factor 3. In any case the measured gain is lower than what is expected from the simulations. At present the discrepancy is under scrutiny, but it is interesting to note that a simulation performed with the power supply at 1 V, instead of the nominal 1,2 V, shows a CFD behaviour very close to the measured one. An internal voltage dropout on the analogue power supply can explain this difference.

Time walk and jitter have been measured at the CFD output for different values of the injected charge. To study the effect of the noise induced by the clock signal, different measurements have been performed with different

clock speeds. The results are reported in figure 5.7 (time walk) and 5.8 (jitter). While the time walk arises with the clock frequency, it seems that the CFD jitter is wider at 160 MHz. This effect has to be understood.

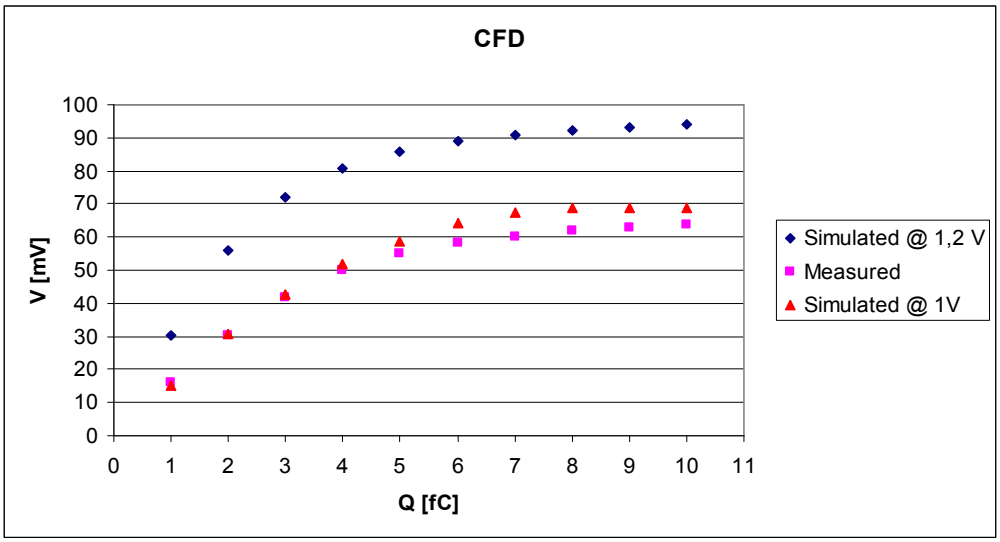

Fig. 5.6 *CFD output as a function of the injected charge: measured points (square pink) are compared to simulation results (blue diamonds for power supply at 1,2 V and red triangles for power supply at 1 V).*

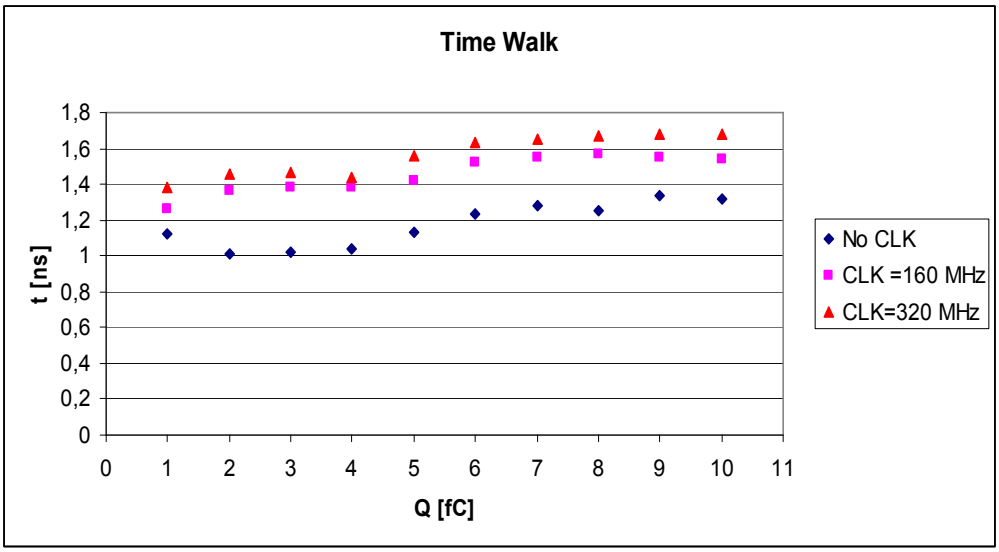

Fig. 5.7 *CFD Time walk as function of the injected charge for different clock frequencies.*

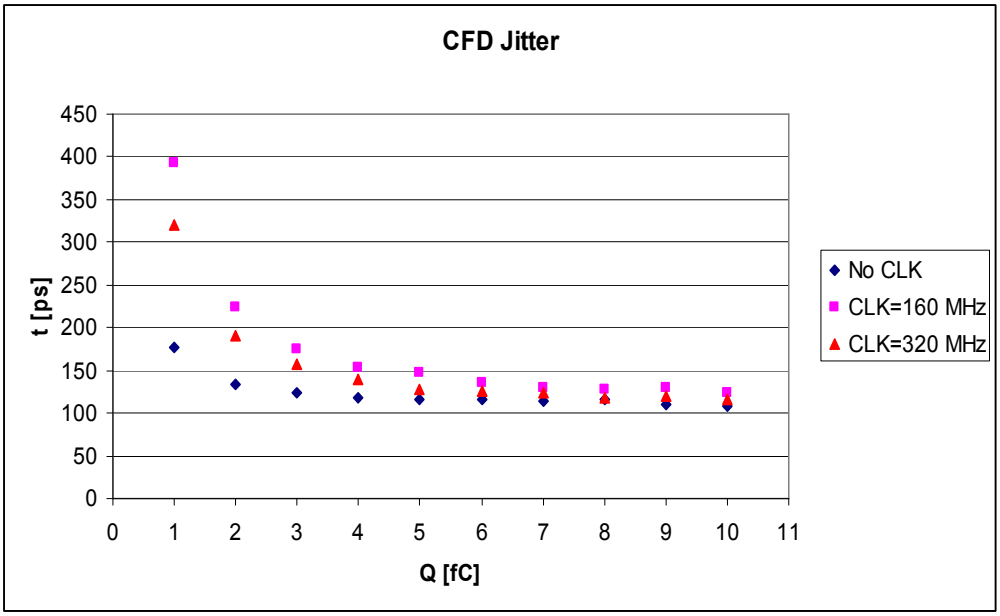

Fig. 5.8 *CFD* jitter *as function of the injected charge for different clock frequencies.*

Measuring the CFD output with the scope, it is possible to see that the induced noise is different for different clock frequencies. The worst observed cases are at 80 MHz and 160 MHz, while the best conditions are for the clock frequency set at 128 MHz or 320 MHz. The reason of this behaviour it is not clear at the moment, but further tests with different clock sources will be performed to understand it.

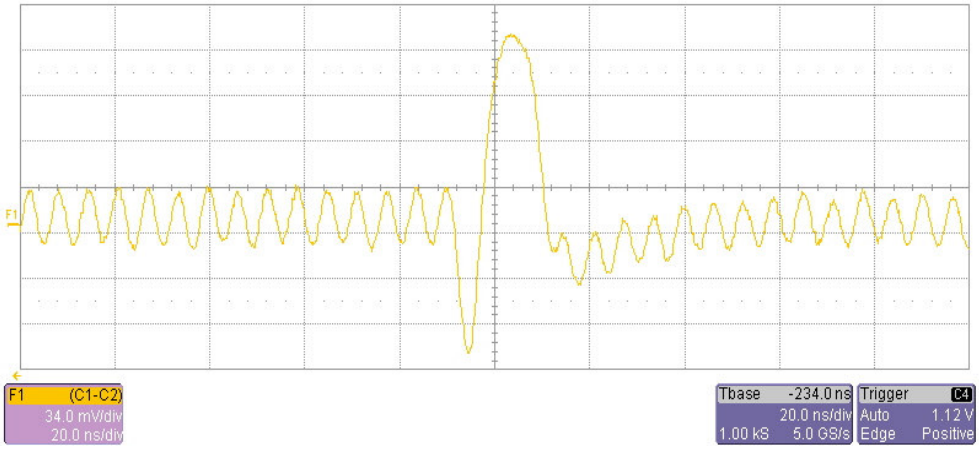

Fig. 5.9 *CFD output with clock frequency 80 MHz.*

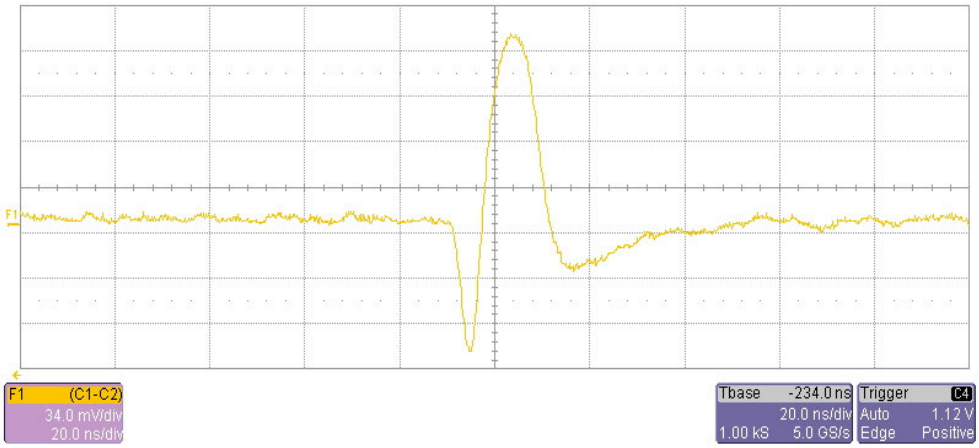

Fig. 5.10 *CFD output with clock frequency 128 MHz.*

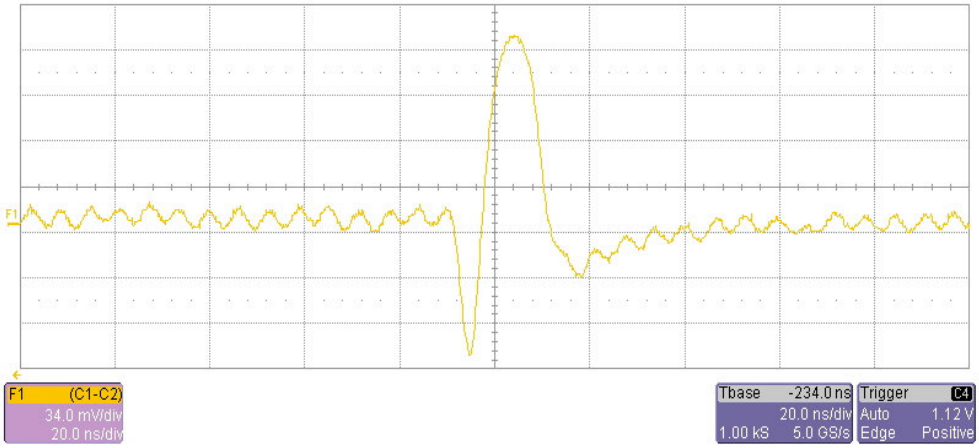

Fig. 5.11 *CFD output with clock frequency 160 MHz.*

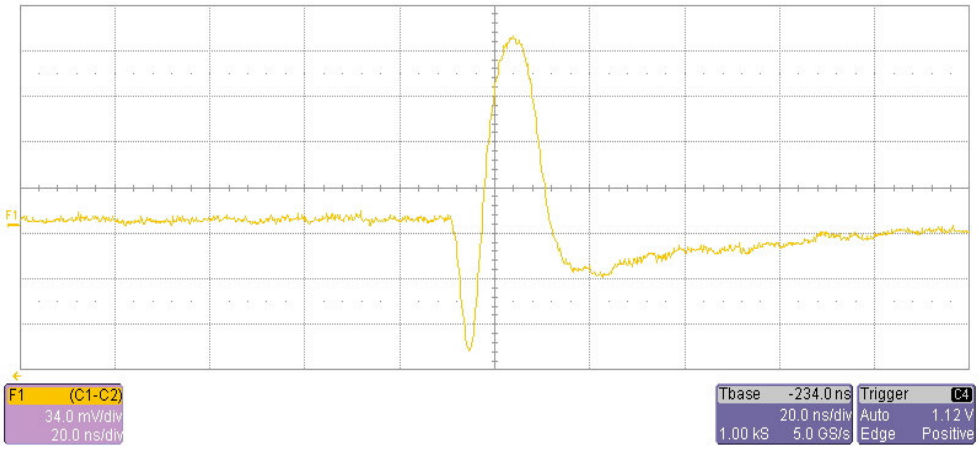

Fig. 5.12 *CFD output with clock frequency 320 MHz.*

5.3 Digital tests

The chip configuration registers are correctly uploaded and read back at 160 MHz. The End of column logic works correctly with a clock frequency of 80 MHz while at the nominal value of 160 MHz one of the signal does not behave properly. In fact, at higher speed the End of Count output, which flags the coarse counter end of count, does not reach the high value. With this failure the End of Columns state machines can not recognize the data frames and no headers or trailers are added to the data stream. The reason of this malfunctioning is due to the not adequate output driver of this signal. To partially solve this problem is possible to increase the digital power supply up to 1,5 V. In such a case this output and the End of Columns state machines work properly up to 130 MHz. Figure 5.13 shows the state analyzer window: one can see the three End of Column outputs working during the test pulse.

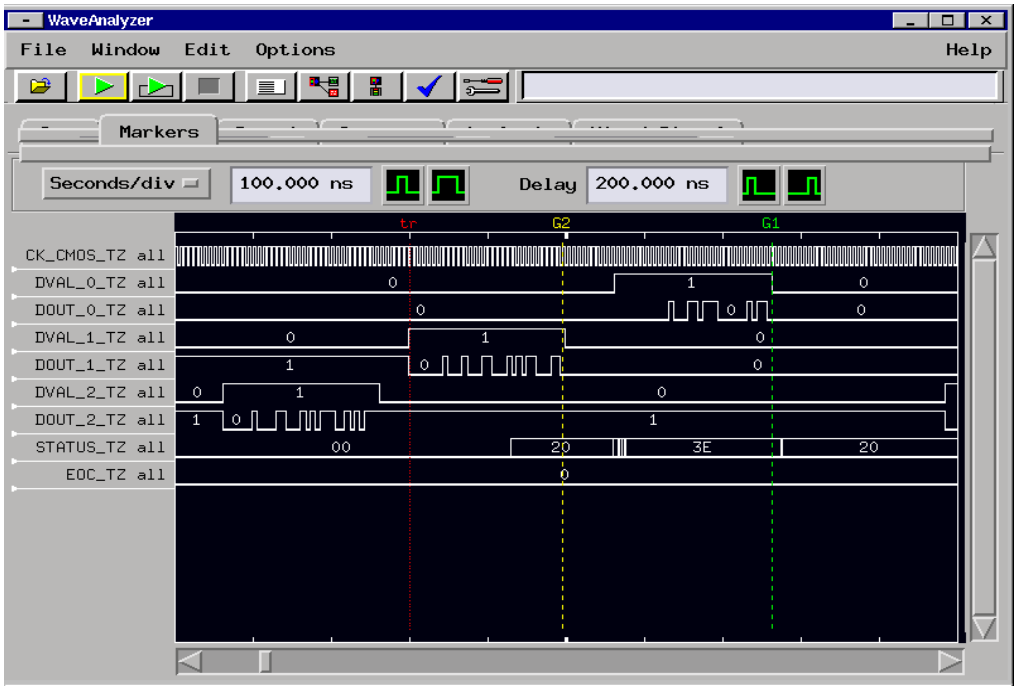

Fig. 5.13 *End of Columns data output.*

Appendix A

Hamming code implementation

The easiest way to protect against corruptions a digital word is to add a parity bit. This indicates if the number of 1 in the data is even or odd. If the bit configuration changes during the transmission, the fault can be detected. It is evident that the quality of the parity checking is poor and it is not possible the auto-correction.

The Hamming code adds more parity bits in such a way that a bit generates different error results according to the bit position, thus giving the possibility to correct the data. The number of flipped bits during the transmission is called in literature the Hamming distance [58]. The parity has a Hamming distance of two, because if two bit flips they can not be detected. The Hamming code extends this concepts increasing the distance as much as possible. The main difference is that the parity bits overlap in order to check them as they were data bit. Of course the number of added bits becomes too large if the code must be protected with double or triple error corrections.

In this application, we limited ourselves to the Hamming code with single error auto-correction and double error detection: this in general terms is said to have a distance of 3.

In this specific Hamming code, in the digital word the bit positions which are power of two (1, 2, 4 and so on) are parity bits. Each data bit in the word is checked by two or more parity bits as represented in the table A.1.

The example shows a data word of 11 bit to which has been added 4 parity bits. Using the common notation (m,n) where m is the total number of bits in the word and n is the number of data bits, the example above is (15,11). It

is evident that such a code is very convenient for long data words, while for few bits it is almost comparable to a triple redundancy architecture.

Bit position		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit contents		P1	P2	D1	P4	D2	D3	D4	P8	D5	D6	D7	D8	D9	D10	D11
Parity bit coverage	P1	X		X		X		X		X		X		X		X
	P2		X	X			X	X			X	X			X	X
	P4				X	X	X	X					X	X	X	X
	P8								X	X	X	X	X	X	X	X

Table A.1 *Hamming code for a 11-bit data word*

For instance, the Hamming code for a 2-bit data word would require three parity bits bringing the full word to (5,2). A 4-bit data word would require an additional 3 bits leading to (7,4) and a 32-bit data word (38,32). This last example shows the big advantage in terms of amount of bits, respect to the triple redundancy technique.

The detection of error transmissions (or SEU in our case) is performed in this way. If all the parity bits are correct there are no errors. Otherwise the error bit is in the position indicated by the sum of the erroneous parity bits. For instance if parity bit P1 and P2 wrong, the erroneous bit is in position 1+2, in this case it corresponds to D1. If only one parity bit is wrong, the bit itself has the error.

In the following pages is reported an example of a 8-bit register Hamming encoded. The data are encoded at the input of the register, according to the table A.1. With the same procedure the Hamming code is calculated at the output of the register, on the whole 12-bit word. If all the four parity bits at the output are low there are no errors. Otherwise the wrong bit is indicated by the output parity bits (see the process *correction_process*) and corrected by an xor operation. A case of multiple errors can be detected by the logic or of the output parity bits (signal named *code_error*), but no corrections are applied. All these operations are done every clock cycle.

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.numeric_std.all;

entity Hamm_reg8 is
  port (
    nres              : in  std_logic;
    clock             : in  std_logic;
    data_in           : in  std_logic_vector(7 downto 0);
    data_out          : out std_logic_vector(7 downto 0);
    load              : in  std_logic;
    code_error        : out std_logic);
end Hamm_reg8;

architecture rtl of Hamm_reg8 is
  signal hamming_reg  : std_logic_vector(11 downto 0);
  signal correction   : std_logic_vector(11 downto 0);
  signal b_in, b_out  : std_logic_vector(3 downto 0);

begin  -- rtl

 -- Calculate Hamming code at the input

 b_in(0) <= data_in(0) xor data_in(1) xor data_in(3) xor data_in(4) xor data_in(6);
 b_in(1) <= data_in(0) xor data_in(2) xor data_in(3) xor data_in(5) xor data_in(6);
 b_in(2) <= data_in(1) xor data_in(2) xor data_in(3) xor data_in(7);
 b_in(3) <= data_in(4) xor data_in(5) xor data_in(6) xor data_in(7);

-- Calculate Hamming code at the output

b_out(0) <= hamming_reg(0) xor hamming_reg(2) xor hamming_reg(4) xor
hamming_reg(6) xor hamming_reg(8) xor hamming_reg(10);
b_out(1) <= hamming_reg(1) xor hamming_reg(2) xor hamming_reg(5) xor
hamming_reg(6) xor hamming_reg(9) xor hamming_reg(10);
b_out(2) <= hamming_reg(3) xor hamming_reg(4) xor hamming_reg(5) xor
hamming_reg(6) xor hamming_reg(11);
b_out(3) <= hamming_reg(7) xor hamming_reg(8) xor hamming_reg(9) xor
hamming_reg(10) xor  hamming_reg(11);

 -- Generate the error flag
 code_error <= b_out(0) or b_out(1) or b_out(2) or b_out(3);

 -- Output correction

 data_out(0)<=hamming_reg(2) xor correction(2);
 data_out(3 downto 1)<=hamming_reg(6 downto 4) xor correction(6 downto 4);
 data_out(7 downto 4)<=hamming_reg(11 downto 8) xor correction(11 downto 8);


-- Hamming register process
reg_process : process (nres,clock,load)
 begin
    if (nres='0') then
      hamming_reg<=(others =>'0');
    elsif (clock'event and clock='1') then
```

```
      if (load='1') then
        hamming_reg(1 downto 0)     <= b_in(1 downto 0);
        hamming_reg(2)              <= data_in(0);
        hamming_reg(3)              <= b_in(2);
        hamming_reg(6 downto 4)     <= data_in(3 downto 1);
        hamming_reg(7)              <= b_in(3);
        hamming_reg(11 downto 8)    <= data_in(7 downto 4);
      else
        hamming_reg<=hamming_reg xor correction;
      end if;
    end if;
  end process;

correction_process : process (b_out)
begin
    case b_out is
      when "0000" =>        correction <= "000000000000";
      when "0001" =>        correction <= "000000000001";
      when "0010" =>        correction <= "000000000010";
      when "0011" =>        correction <= "000000000100";
      when "0100" =>        correction <= "000000001000";
      when "0101" =>        correction <= "000000010000";
      when "0110" =>        correction <= "000000100000";
      when "0111" =>        correction <= "000001000000";
      when "1000" =>        correction <= "000010000000";
      when "1001" =>        correction <= "000100000000";
      when "1010" =>        correction <= "001000000000";
      when "1011" =>        correction <= "010000000000";
      when "1100" =>        correction <= "100000000000";
      when others =>        correction <= "000000000000";
    end case;
end process;
end rtl;
```

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