University of Turin

Faculty of Mathematical, Physics and Natural Sciences

Physics Degree Thesis

Development of Integrated Electronics for Monolithic Detectors in Q-Well CMOS Technology

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"In questo consiste la forza dell'acqua: non potrà mai essere spezzata da un martello, o ferita da un coltello.
La più potente spada al mondo non potr mai lasciare nessuna cicatrice sulla sua superficie.
L'acqua di un fiume si adatta al cammino possibile, senza dimenticare il proprio obiettivo: il mare.
Fragile alla sorgente, a poco a poco acquista la forza degli altri fiumi che incontra.
E, a partire da un certo momento, il suo potere È totale."
P. C.

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Alla mia famiglia e a tutti voi, GRAZIE!

[1]Cascio

Abstract

This thesis is part of the ongoing studies for the upgrades of the Inner Tracking System of the Alice experiment at CERN.
ALICE is the LHC experiment devoted to the study of ultra-relativistic heavy-ion collisions. The experiment is now in the data taking phase. In 2017-2018 the LHC will be shut down for a major maintenance and it is foreseen to use this opportunity to introduce also important improvements in the ALICE experimental apparatus. One of this system considered for the upgrade is the Inner Tracking System or ITS, which is the closest detector to the interaction point. The use of a smaller beam-pipe will allow to introduce high granularity detectors closer to the interaction point, improving the vertex reconstruction and giving access to new physics channels that cannot be explored with the present set-up. The data rate capability of the system will also be increased from today's rate of 1 kHz to 50 kHz in order to improve the statistics on rare events.

Monolithic silicon detectors are considered in order to reduce the material budget. Since they do not need a conductive bond like hybrid pixel detectors, it is possible to get thinner sensors thus improving the impact parameter resolution. Several approaches exist in order to design a monolithic CMOS sensors. The Quadruple well technology provided by TowerJazz is regarded as a very promising candidate. This technology allows in fact to built complex pixels embedding both digital and analog circuits within the sensitive area. Furthermore, the feature size of 0.18 μm already allows for dense digital design.

The development of the new ITS will be a large international collaboration and it involves teams from several institutions including IN2P3, CERN and INFN. The purpose is to develop new generation of CMOS sensors suited to the ALICE requirements. Such devices will need many high performance blocks performing different functions: amplification, data compression, power regulation, data transmission. One of the key components of the CMOS sen-

sors is the data transmission link. Here, it is necessary to combine a high data throughput with a small power consumption.

In this work the design of such a link has been addressed. The link is based on the LVDS protocol, which is a widely used industrial standard. The link should work at a transmission rate of up to 1Gbit/s.
This thesis is organized as follows:

- In Chapter 1 some basic concepts about the detectors principle of operation are reported together with a brief description of some types of silicon sensors: the hybrid pixel sensors, the silicon strip and the silicon drift detectors. Furthermore, a description of the general purpose detector ALICE and of its components is given, paying special attention on the features of the actual ITS and on its limitations which motivate the upgrade.

- In Chapter 2 the state of the art in the Monolithic Active Pixel Sensors is reported. We present the standards MAPS and its principle of operation together with two alternative layout of the sensor: Deep N-well MAPS and INMAPS. Monolithic sensors based on charge collection by drift.

- Chapter 3 reports a description of the LVDS interface and of its specifications as well as the method used in order to analyze the quality of the transmitted signal, as the eye diagram.

- In Chapter 4 we describe the LVDS transceivers the we have designed. The circuit are implemented in the 0.18 μm Q-well CMOS technology. Two transmitter designs have been considered. Transmitter 1 is based on a scheme widely used in many applications at CERN. This scheme was scaled to adapt it to the technology of our interest. Some limitations were found by operating this device at power supply 1.8 V. This motivated the design of the alternative scheme Transmitter 2 that shows good performance. A receiver circuit based on a self biased amplifier was also developed.

- In Chapter 5, finally, we report the simulation results obtained with our LVDS link. Simulations were performed using both deterministic

and pseudo-random sequences to study the stability of the system and its dynamic response. The simulation were done under different conditions including the noise, mismatch effects, temperature and process variations.

Chapter 1

Particle Detection and Tracking in High Energy Physics

ALICE, acronym of *A Large Ion Collider Experiment*, is a heavy-ion experiment at the CERN Large Hadron Collider, near Geneva. The ALICE detector is designed to analyze the collisions between heavy-ions at the center-of-mass energy ~ 5.5 TeV. The purpose of the experiment is to study the physics of strong interactions, in an attempt to answer fundamental questions about the mechanism of the mass generation of handrons and to understand why single quarks and gluons have never been observed[1].
The long term projects foresees the characterization of a new state of matter, created by the disintegration of hadrons in free quarks and gluons, the *Quark-Gluon Plasma* (QPG), which is likely tho have existed just after the Big Bang. Therefore, the aim of the ALICE is to create the physic conditions for the QPG formation and to provide a comprehensive characterization of its properties like initial temperature, degrees of freedom, transport coefficients, etc.

The first part of this chapter introduces basic concepts that will be used throughout the thesis; the second part is devoted to the ALICE detector and to the Inner Tracking System (ITS) in particular.
The chapter starts with an overview of the tracking detectors employed to study the physics properties of subatomic particles. When one inserts the detector in a magnetic field, it is possible to determine the magnitude of the particles' momentum by measuring the radius of curvature of the trajectory. In addition, in order to correctly detect an event, the detector read out must be fast enough to avoid the *pile-up* of two successive events.
The second section of the chapter describes the principles on which particles detection is based, i.e. the energy loss in the sensor due to the interaction

between the impinging particle and the atoms encountered in the sensor active volume. Multiple scattering, that often reduces the capability of a detector to locate the interaction vertex, is also discussed.
In the third section a review of the most important silicon sensors used in particle physics experiments is presented.
ALICE and its sub-detectors are described in the fourth section. The last section focuses on the *Inner Tracking System* (ITS). Here, a description the current ITS (Section 1.5) is followed by a discussion of the limitations of the current set-up and of the motivations for the upgrade. (Section 1.6). Finally, the technical options for the implementation of the new ITS are examined (Section 1.7).

1.1 Basic Concepts

A detector is a device through which one detects a charged or electrically neutral particle and measures its properties. Although there are many different types of detectors (semiconductor detectors, scintillators, ionization chambers etc...), it should be noted that the principle of operation is always the same: the conversion of the energy released by the particles in the sensitive volume of the sensor into an electrical signal that is possible to handle by means of electronic circuits.

Complex systems combining different detectors are necessary to identify a particle and to measure its physical properties like energy, momentum, electrical charge and mass.
A tracking detector is used to determine the trajectories of charged particles that are deflected in a magnetic field $\vec{B}$ and to measure their momenta. In addition, it allows to reconstruct the primary vertex of interaction and to localize the secondary vertex due to the decays of the particles produced in the interaction. By means of a tracking detector it is also possible to identify a particle studying its energy loss per unit path length (*stopping power*) $\langle dE/dx \rangle$ and to select specific events.

1.1.1 Impact parameter resolution

For optimal performance, a tracking detector should be as close as possible to the interaction point. In fact, many particles of interest live for a very short time τ before disintegrating into the daughter particles. For example, the Pb-Pb collisions at LHC produce D^0 mesons that have lifetime $\tau \approx 10^{-12}s$, during which they cover a distance of $c\tau \approx 300\mu m$. Then, they

decay generating K^- and π^+. In this case, given that the D^0 meson is a neutral particle, the only way to reveal it by using a tracking detector is to trace the trajectories of secondary particles and to localize the decay point. This is a simple example of a general method used for all particles that have short lifetimes. Here, the relevant quantity is the minimum distance between the primary vertex where the collisions take place and the secondary vertex, where the particle has decayed, i.e. the *impact parameter* b. This must be determined with the best possible resolution, e.g. $\lesssim 0.03\ mm$ for particles which have lifetimes of $\sim$ ps [2].

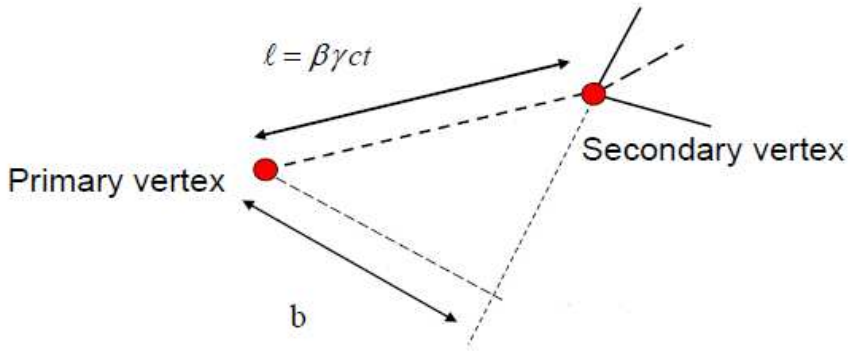


Figure 1.1: Interaction Point: primary vertex and secondary displaced vertex, [3]

The impact parameter b depends on the energy of the particle, its lifetime τ and the angle between its direction of flight and the particles produced in the decay:

$$b = \gamma\beta c\tau \sin\theta \tag{1.1}$$

For high momentum particles $\sin\theta \approx 1/(\gamma\beta)$ and therefore $b \approx c\tau$ is equivalent to the distance traveled by the particles before they decay spontaneously. In this case the resolution σ_b doesn't depend on the magnitude of the particles momentum. On the contrary, σ_b only depends on detector's properties, like resolution and geometry, and the closer the detector is to the interaction

point, the better the spatial resolution will be.
To give a quantitative idea, let's consider a cylindric tracker disposed around the interaction point that is formed only by two layers 1 and 2. The two layers are separated from the interaction point by r_1 and r_2, with $r_1 < r_2$ and their resolutions are respectively σ_1 and σ_2. This is a crude simplification of a realistic tracker, which is usually composed of many layers. We suppose here to neglect also the magnetic field $\vec{B}$.

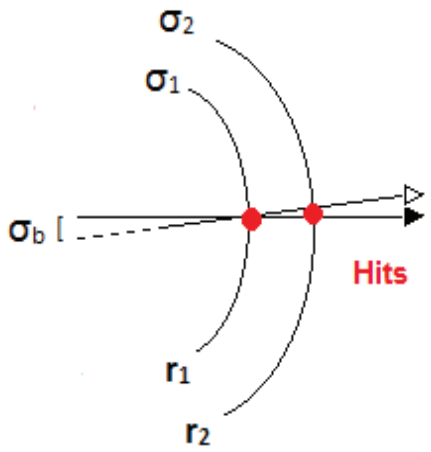


Figure 1.2: Impact parameter resolution

Now, let's approximate the trajectory with a straight line like $t(r) = b + Ar$, where the impact parameter b and the constant A represent respectively the offset and the slope of the track. We apply a weighted least square on the track point because each layers has its own resolution σ_i. Therefore, the impact parameter resolution is obtained through the offset's error:

$$\sigma_b^2 = \frac{\sum_i w_i r_i^2}{\Delta} = \left(\frac{r_1^2}{\sigma_1^2} + \frac{r_2^2}{\sigma_2^2}\right)\frac{1}{\Delta} \tag{1.2}$$

where $w = 1/\sigma_i^2$ represents the weight of each layer and Δ is defined as:

$$\Delta = \sum_i w_i \sum_i w_i r_i^2 - \Big(\sum_i w_i r_i\Big)^2 =$$
$$\frac{1}{\sigma_1^2}\Big(\frac{r_1^2}{\sigma_1^2} + \frac{r_2^2}{\sigma_2^2}\Big) + \frac{1}{\sigma_2^2}\Big(\frac{r_1^2}{\sigma_1^2} + \frac{r_2^2}{\sigma_2^2}\Big) - \Big(\frac{r_1}{\sigma_1^2} + \frac{r_2}{\sigma_2^2}\Big)^2 =$$
$$\Big(\frac{1}{\sigma_1^2} + \frac{1}{\sigma_2^2}\Big)\Big(\frac{r_1^2\sigma_2^2 + r_2^2\sigma_1^2}{\sigma_1^2\sigma_2^2}\Big) - \Big(\frac{r_1\sigma_2^2 + r_2\sigma_1^2}{\sigma_1^2\sigma_2^2}\Big)^2 = \tag{1.3}$$
$$\frac{(\sigma_1^2 + \sigma_2^2)(r_1^2\sigma_2^2 + r_2^2\sigma_1^2) - (r_1^2\sigma_2^4 + r_2^2\sigma_1^4 + 2r_1r_2\sigma_1^2\sigma_2^2)}{(\sigma_1^2\sigma_2^2)^2} =$$
$$\frac{r_1^2\sigma_1^2\sigma_2^2 + r_2^2\sigma_1^2\sigma_2^2 - 2r_1r_2\sigma_1^2\sigma_2^2}{(\sigma_1^2\sigma_2^2)^2} = \frac{(r_2 - r_1)^2\sigma_1^2\sigma_2^2}{(\sigma_1^2\sigma_2^2)^2} =$$
$$\frac{(r_2 - r_1)^2}{(\sigma_1^2\sigma_2^2)}.$$

From (1.2) and (1.3) and with the previously mentioned approximation, one gets:

$$\sigma_b^2 \approx \Big(\frac{r_1^2\sigma_2^2 + r_2^2\sigma_1^2}{\sigma_1^2\sigma_2^2}\Big)\Big(\frac{1}{\Delta}\Big) = \Big(\frac{r_1^2\sigma_2^2 + r_2^2\sigma_1^2}{\sigma_1^2\sigma_2^2}\Big)\frac{\sigma_1^2\sigma_2^2}{(r_2 - r_1)^2} = \tag{1.4}$$
$$\Big(\frac{\sigma_1 r_2}{r_2 - r_1}\Big)^2 + \Big(\frac{\sigma_2 r_1}{r_2 - r_1}\Big)^2 = \frac{1}{(r_2 - r_1)^2}[(\sigma_1 r_2)^2 + (\sigma_2 r_1)^2]$$

This shows that the precision on the inner layer provides the main contribution because σ_1 is highlighted by the greater radius.
If one supposes $\sigma_1 = \sigma_2 = \sigma$, 1.4 is rewritten as:

$$\Big(\frac{\sigma_b}{\sigma}\Big)^2 \approx \Big(\frac{1}{1 - r_1/r_2}\Big)^2 + \Big(\frac{1}{r_2/r_1 - 1}\Big)^2 \tag{1.5}$$

from which it is clear that the impact parameter resolution can be improved by properly setting the ratio between the distances of the layers from the interaction point [3].

1.1.2 Deflection in magnetic field

It is well known that when a charged particle is moving in a magnetic field $\vec{B}$ its trajectory is deflected due to the Lorentz force. The magnitude and

the direction of the particle deflections are functions of the rest mass m_0 and the charge q of the particle: two particles having opposite charge moving in the same direction at velocity $\vec{v}$ will have opposite deflections; two particles having the same charge but different masses, will have different curvature radii R.
In the relativistic case one has:

$$\vec{F} = q(\vec{v} \times \vec{B}) \qquad R = \frac{p}{qB} = \frac{\gamma m_0 v}{qB} \tag{1.6}$$

By knowing the magnitude of the magnetic field and the curvature radius,

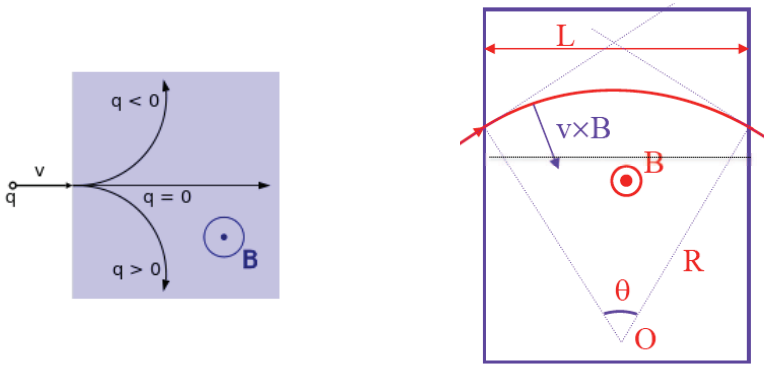


Figure 1.3: (Left) Charge dependence of deflection in magnetic field; (Right) Radius of curvature

that is the deflection angle θ, it is possible to go back to the momentum of the charged particle $p = \gamma m_0 v$ or, if the detector is put into a solenoidal magnetic field, one measures the transverse momentum p_T on the deflection plane $r\phi$ of the particle.

1.1.3 Occupancy, dead time and pile-up

A notion that will be used later is the *occupancy* of the detector. As it may be inferred, the occupancy has to do with the number of busy channels in a detector, that is those channels that are active since they have been hit by a particle.
The occupancy value is expressed as a percentage and it is important because it determines the hit rate of a channel and its ability to reconstruct correctly two different events.
Let's assume that we have a collision rate $50kHz$ and that in each collision

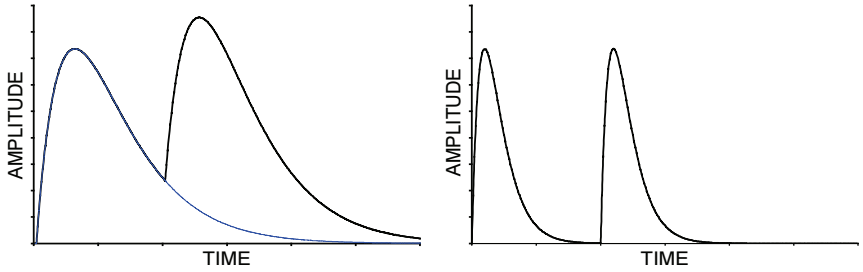


Figure 1.4: Illustration of the concept of pile-up, which occurs when the time between two events is comparable with the readout time. [3].

100 different particles per cm^2 are produced. If we have a detector with 10^4 pixels per cm^2 the occupancy is 2%, that is 200 pixels only are experiencing simultaneously a signal. The rate per pixel will then be:

$$r_p = 50kHz \times (2\%\ 10000) = 1kHz \tag{1.7}$$

The time Δt required by the detector to process an event is defined as *dead time* and, in general, mainly depends on the dead time of the front-end. The latter should not be too long so that the ability of the detector to correctly detect the next event is quickly restored . In fact, when the detector is hit, it may remain sensitive or not to subsequent events: in the case in which the detector is no longer sensitive, each signal that arrives during Δt is missed; instead, if the detector is still sensitive the pile-up of the events occurs. In the latter case, a distortion of the signal with loss of information affect both on the first hit and the following ones. We have also a dilation of the dead time [4]. It is therefore important to estimate the pile-up probability for a given detector.
If one assumes that the time instants in which two different hits occur are statistically uncorrelated, the Poisson distribution can be used to calculate the probability to have a number of events n in the time Δt:

$$P(n) = \frac{(r_p \Delta t)^n e^{-r_p \Delta t}}{n!} \tag{1.8}$$

Suppose now to consider the case in which the dead time is equal to the average event rate, i.e:

$$\Delta t = \frac{1}{r_p} \tag{1.9}$$

which implies:

$$\Delta t \frac{1}{r_p} = 1 \tag{1.10}$$

With a rate of events of $1/\Delta t$ the probability that no signal arrives while the system is in dead time is obtained with $n = 0$. Then (1.8) becomes:

$$P(0) = e^{-r_p \Delta t} \approx \frac{1}{e} \qquad \text{setting } r_p \Delta t = 1 \tag{1.11}$$

that is the probability that two event are not superimposed is $\approx 30\%$ and the pile-up probability is $1 - P(0) \approx 70\%$. Therefore the smaller is $r_p \Delta t$, that is for $\Delta t << 1/r_p$, the more the pile-up will be negligible [3].

1.2 Energy Loss of Heavy Charged Particles

When a particle goes through a detector it interacts with the atoms of the active material of the sensor loosing energy. The energy loss has a strong dependence ont the total energy, the mass and charge of the particle. For heavy charged particles two processes occur: the inelastic Coulomb scattering with the atomic electrons and the elastic scattering with the nuclei. However, only the former is fundamental in the interaction with a material because it is the mechanism by which the heavy charged particles release energy in the medium.

Since for each interaction with an electron the amount of energy lost by a charged particle is very small, about 1/500 of the particle energy per nucleon, and since the particle interacts with many electrons before stopping, a energy loss will result that can be represented with a continuous function. Due to the amount of energy transferred in the interaction, the atomic electrons can jump to excited states or they can be expelled from the atom, which becomes ionized. In a detector, an electric field is in general appplied to sweep the electrons far from the ions and prevent recombination[6]. Finally, the number of the produced ion pairs is determined by calculating the ratio between the energy released by the particle and the average ionization energy E_i. In the case of silicon, which is of particular interest for this thesis, $E_i = 3.6eV$.

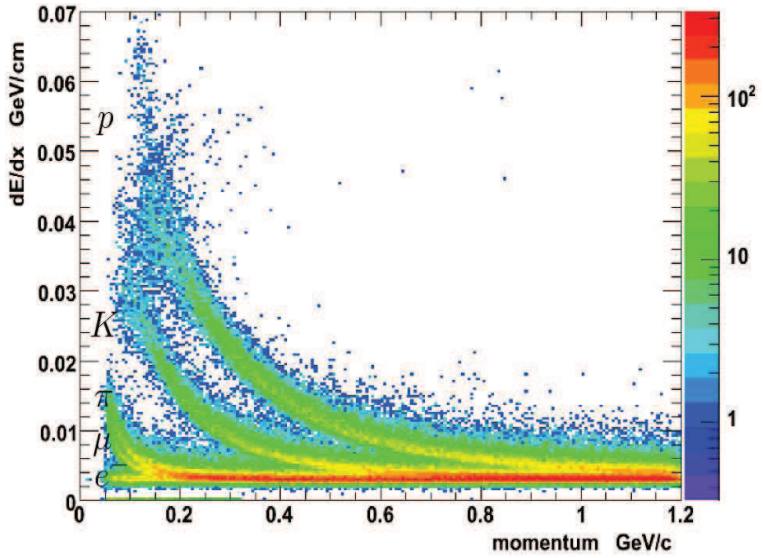


Figure 1.5: Energy Loss vs momentum for Hadrons and Leptons [5]

1.2.1 The Bethe-Bloch formula

The energy loss of a particle in the interaction with a material is characterized by the *linear stopping power* S that is the average energy loss per unit path length:

$$S = -\frac{dE}{dx} \tag{1.12}$$

If one takes into account the quantum-mechanical nature of the scattering between the particles that pass through the medium and the atomic electrons, one obtains the Bethe-Bloch formula for the energy loss:

$$-\langle\frac{dE}{dx}\rangle = Kz^2\frac{Z}{A\beta^2}\Big[\frac{1}{2}ln\Big(\frac{2m_ec^2\beta^2\gamma^2T_{max}}{I^2}\Big) - \beta^2\Big] \tag{1.13}$$

with:

$\langle \frac{dE}{dx} \rangle$	energy loss expressed in $\frac{eV}{g/cm^2}$;
K	$4\pi N_{av} r_e^2 m_e c^2 = 0.307075 MeV cm^2$ e r_e classical electron radius;
z	charge of incident particle in units of the electron charge;
Z	atomic number of absorption medium (14 for silicon);
A	atomic mass of absorption medium (28 for silicon);
$m_e c^2$	$0.511 MeV$ rest energy of the electron;
β	velocity of the particle in units of the speed of light;
γ	Lorentz factor defined as $(1-\beta^2)^{-\frac{1}{2}}$;
T_{max}	maximum kinetic energy transferred to the particle;
I	mean excitation energy (137 eV for silicon).

It must be noted that $\langle dE/dx \rangle$ depends on the characteristic of the absorber and especially on the properties of the incident particle like its charge and its mass M. The mass is contained in the expression of T_{max} and necessarily determines the behaviour of the function (1.12). Then, by measuring how particles of different masses lose energy one can identify them. figure 1.5 shows how hadrons and different leptons release energy as function of their momenta.
A particle whose energy is in the minimum of the Bethe-Bloch curve is defined as a *Minimum Ionizing Particle* or MIP.
figure 1.6 shows that after the minimum $\langle dE/dx \rangle$ slowly grows and has a plateau for high values of energy; conversely, in the low energy range ($\beta\gamma < 1$) the energy loss is like $1/\beta^2$.
In practice, the Bethe-Bloch formula should be modified consider the effects that occur both at high and low energies, so that:

$$-\langle \frac{dE}{dx} \rangle = K z^2 \frac{Z}{A\beta^2} \Big[\frac{1}{2} ln \Big(\frac{2 m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} \Big) - \beta^2 - \frac{\delta}{2} - \frac{C(I, \beta\gamma)}{Z} \Big] \quad (1.14)$$

Here two corrections are included: the density effect correction δ and the shell correction C. The former manifests to high energies: it is due to relativistic effects that modify the electric field of the incident particle and result in a slowdown of the logarithmic slope of the function. The second one occurs at low energies, when the velocity of the traversing particle is almost similar to the speed of the electrons in the atomic shells. At such energies the assumption of stationarity of the electron with respect to the incident particle

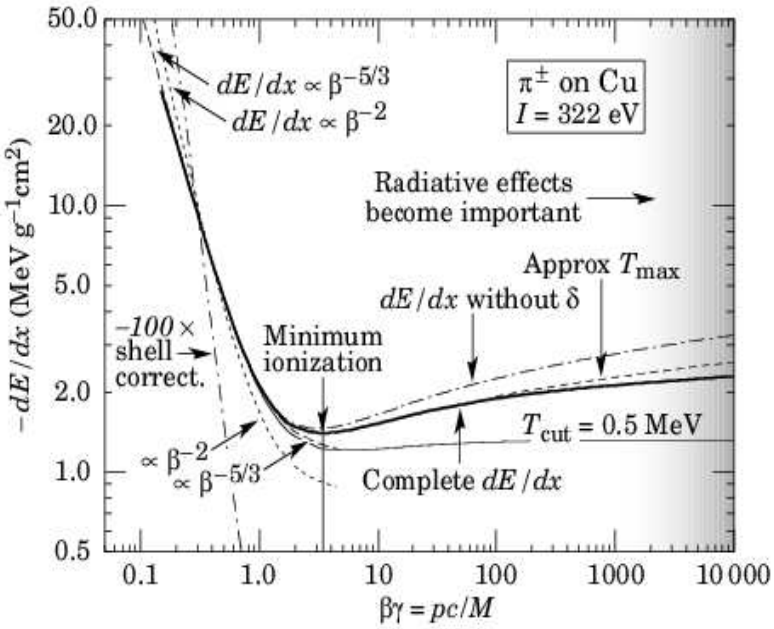


Figure 1.6: Energy Loss in medium

breaks down [4].

The corrected form of the Bethe Bloch formula (1.14) shows the mean value of the Landau distribution that describes the energy loss of the particle per unit path length. If a particle is not stopped in the sensor, the response varies around the peak of the distribution and there is a significant probability of high signals. This leads to the displacement of the mean value of the distribution toward energies higher than the one corresponding to the most probable value. The fluctuations of Landau distribution are due to the production of δ-electrons, i.e. those electrons released by the atoms that have so much energy to produce further ionizations. The main consequence is a worse spatial resolution of the charge cloud because the δ-electrons have a direction perpendicular to that of the traversing charged particle. The thinner is the sensor the more evident is the effect [2].
The number of ionizations that a particle produces changes with its kinetic energy. In the case in which the particle is completely stopped, the number of the produced electron-ion pairs increases at the end of the trajectory (fig 1.7) because the energy loss per unit path length is greater at the end of the

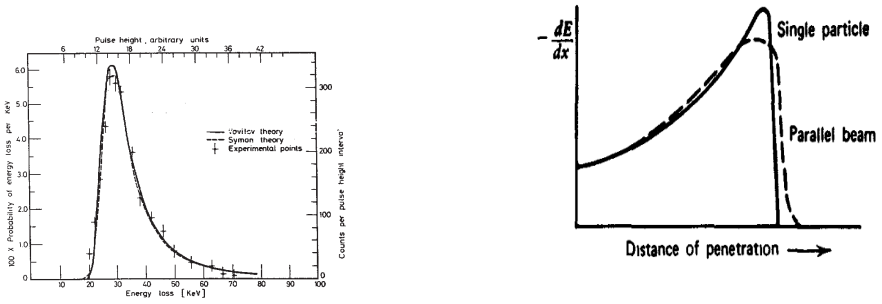


Figure 1.7: (Left) Landau Distribution: probability of energy loss; (Right) Bragg's curve: number of ionizations for single particle and parallel beam. [4]

path rather than at the beginning.

1.2.2 Multiple Scattering

A traversing particle is scattered by the atomic electron but also by the atomic nuclei. In the realistic hypothesis that the latter are heavier than the incident particles, the energy loss during the Coulomb scattering is negligible (elastic scattering) and the particles are just deflected. While a particle crosses the detector, multiple collisions occur and the particle trajectory can be significantly perturbed (multiple scattering). Multiple scattering worsens the space resolution on the particle track, thereby reducing also the impact parameter resolution σ_b.
The distribution of the scattering angles is mostly Gaussian with a rms given

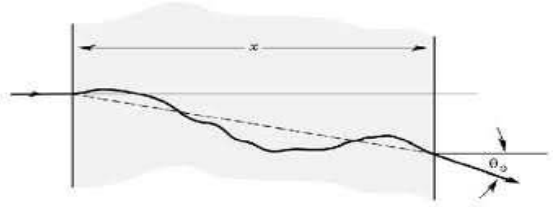


Figure 1.8: Multiple scattering

by:

$$\vartheta_{plane}^{rms} = \frac{13.6MeV}{\beta pc} z \sqrt{\frac{x}{X_0}} \Big[1 + 0.038 ln\Big(\frac{x}{X_0}\Big)\Big] \tag{1.15}$$

where ϑ is expressed in rad, β is a velocity of the particle in unit of speed of light, p is the momentum of the particles expressed in MeV/c and z is a charge of the particle. X_0 is defined as *radiation length* and it is a specific property of each material. For example, the radiation length of silicon, the most common material used for sensors, is 9.36 cm. X_0 indicates how long one electron can travel in a material before its energy is reduced to 1/e of the the initial value E_0 because of Bremsstrahlung:

$$E = E_0^{-\frac{x}{X_0}} \tag{1.16}$$

I must be point out that the appearance of X_0 in the multiple scattering formula is fortuitous.

1.3 Silicon Sensors

Three key requirements of particle detectors are:

- Speed, in order to allow to study as many events as possible.
- Spatial resolution, to allow precise tracking and momentum measurement
- Radiation hardness, since in many experiments the sensors are exposed to significant amounts of both ionizing and not inionizing radiation.

Semiconductor detectors are widely used as they satisfy all the above requirements. In particular, silicon detectors provides the best spatial resolution and also a good energy resolution. In addition, it is possible to design very thin silicon detectors to minimize multiple scattering. Due to their radiation hardness, the can be located close to the interaction point with the main consequences of improving the impact parameter resolution and the separation of multiple tracks.

Silicon is a semiconductor material with an energy gap of 1.12 eV. The average energy required to generate an electron-ion pair is only 3.6 eV. It has an atomic number $Z = 14$ and a high atomic density, about 2330 kg/m^3.

These are fundamental properties to measure $\langle dE/dx \rangle$ and for track reconstruction (see eq. 1.13). In addition, the high mobility[1] of the charge carriers in the semiconductor, even if at room temperature, is such that the charge collection time is very fast.
Four technologies of silicon sensors are examined in the following: the Hybrid Pixel and Monolithic Active Pixel Detectors, the Silicon Drift Detector, the Silicon Strip Detector. These devices have a different electrode segmentation but are all formed by a p-n junction that is reversely biased to deplete as much as possible the sensitive volume (depletion zone) of the sensor.
In doing so, the charge signal produced by a traversing particle is maximized. The average number of electron-hole pairs generated by a particle in the active volume can be calculated by dividing the energy lose E by the average energy necessary to produce the charge carriers E_i:

$$Q_s = \frac{E}{E_i}; \tag{1.17}$$

for example, a MIP traversing a silicon detector gives on average about 80 electron-hole pairs per μm path length [3].

Because of the reversed bias, in the depletion zone an electric field $\vec{E}$ is established that accelerates the carriers of opposite sign in opposite directions. The drift velocity of carriers depends on the magnitude and the direction of $\vec{E}$: $\vec{v}(z) = \mu\vec{E}(z)$ where μ is the mobility of the carriers in a medium and z is a depth of the sensor.
The field lines remain parallel to the electrodes into the volume of the sensor but they bend on the surfaces. Then, the geometry of the electrodes and their pitch segmentation affect the resolution of the particles position.
In this context, the read out mode (analog or binary read out), the algorithm of the track reconstruction, the magnitude of the shared charge between two elements of the detector, are also very important [2].
In the case of binary read out, the response function is box-like and the resolution of a single detector is equal to the pitch of the segmentation [3]. It should be noted that the particles hit a detector randomly. Then, the average difference between the true impact position and the measured one with a uniform distribution of the particle is given by [2]:

$$\sigma_p^2 = \int_{-\frac{p}{2}}^{\frac{p}{2}} \frac{x^2}{p} dx = \frac{p^2}{12}. \tag{1.18}$$

[1]Mobility of charge carriers is determined by the material considered, the temperature, the charge of the carrier and its effective mass. In the case of silicon, elctron and hole mobilities are respectively $\mu_n = 1350 cm^2/(Vs)$ e $\mu_p = 450 cm^2/(Vs)$.

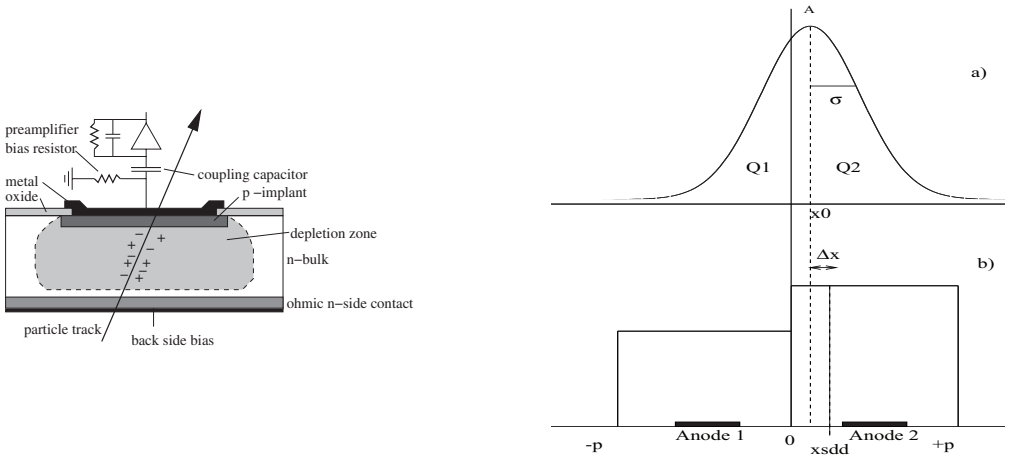


Figure 1.9: (Left) Cross section of general silicon sensor [2]; (Right) Position Resolution: a) Gaussian distribution; b) Centroid method [3].

This expression corresponds to the spatial resolution $\sigma_p \approx 0.28p$, i.e. setting $p = 100\mu m$ σ_p is about $28\mu m$.
In addition to the drift, the thermal diffusion of the particles must be considered because it spreads the charge cloud in any direction. The thermal diffusion, too, is random with a rms width given by:

$$\sigma_y = \sqrt{2Dt} \tag{1.19}$$

where D[2] is the diffusion constant of the carriers in silicon and t is the collection time.

If the charge cloud spreads out, two or more neighboring elements of the sensor share the signal charge and form a group which is called *cluster*.
While at a first glance this charge sharing degrades the performance of the sensor to exactly localize the impact point, on the other hand it improves the resolution of the position since the shared fractional charge is determined by superimposed Gaussian distribution[3]. The integral of the superimposition tend quickly to zero for deviations beyond several standard deviations: the technique to calculate the exact position of the particles is the *centroid method*.
The simplest case is with only two collection anodes that have a pitch p and measure respectively the fractional charges Q_1 e Q_2: then, the impact point

[2]The diffusion constant is related to the mobility of the carriers by the Einstein relation $D = \frac{kT}{q}$.

is given by:

$$x_{cm} = \frac{-(p/2)Q_1 + (p/2)Q_2}{Q_1 + Q_2}. \tag{1.20}$$

If the width of the charge sharing is ($s < p$) and a cluster is formed by two elements only the expected σ_p is $s/\sqrt{12}$, i.e. we have an improvement of the spatial resolution. In fact, for a cluster formed by one element only the expected σ_p is $(p-s)/\sqrt{12}$. The best average spatial resolution is obtained when the number of the cluster formed by one element only is equal to those formed by two elements, i.e. if $s = p/2$.
An analog read out delivers a voltage proportional to the collected charge. To obtain a better spatial resolution, the rule of thumb requires that the electrodes pitch must be divided by the signal-to-noise ratio of the analog pulse. However, the spatial resolution is always limited to the value $(p-s)/\sqrt{12}$ when a single anode is active.
In the following sections, the four technologies for the silicon sensors mentioned above are discussed.

1.3.1 Hybrid Pixel Detectors and MAPS

For the hybrid technology the sensor and the front-end electronics are fabricated in two distinct silicon wafers that have their own thickness [3] as it is shown in figure 1.15. The electrodes are segmented in two dimensions on the sensor surface to create a pixels matrix; each electrode is bump bonded with the corresponding read out cell. The connectivity between the two wafers is vertical and there is a correspondence between the matrix of the pixels and those of the read out cells, i.e. between the pixel area and those of the read out cell. At present, in the hybrid architecture the minimum dimensions of the pixels are $50\mu m \times 50\mu m$ and are limited by the presence of the conductive bumps.
The pixel detectors today in use in the ALICE ITS have a cell size of $50\mu m \times 425\mu m$. The ALICE sensors are of the *p-in-n* type and the layer underneath the bulk is n^+ type.
Two techniques are widely used to degrade the bias voltage towards the sensor edge and have a more stable electrical current in the device: multiple guardrings and edge implantation. Nowadays edges sensors are studied since the guardrings are dead zone that have an extension which ranges from a few μm to a few mm[8].

[3] A detector has a total thickness about 350 μm: 200 μm for the pixel and 150 μm for the front-end.

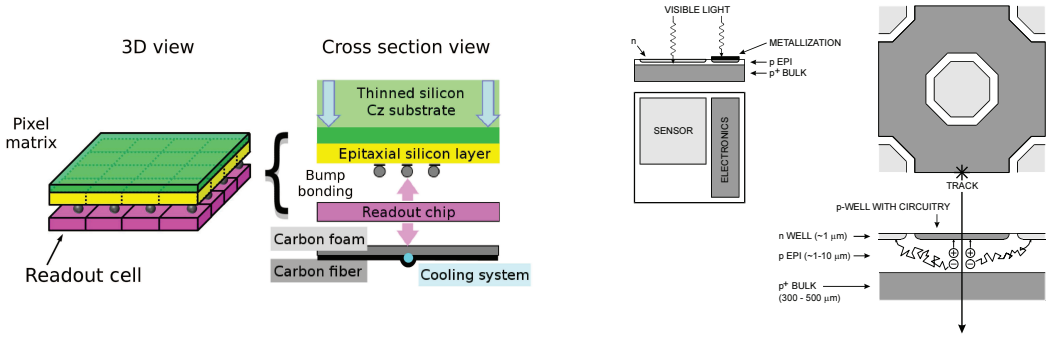


Figure 1.10: (L) Hybrid Pixel Sensors, [5]; (R) Standard MAPS , [3]

The monolithic technology is treated in detail the next section whereas here we have only a brief description.
Monolithic detectors are peculiar because they embed into the same CMOS ASIC both the sensor and the front-end electronics.
For this technology, we have different flavours of devices. For a standard monolithic active pixel sensor (standard MAPS) the sensitive volume is an p-type epitaxial layer (referred to as the "epi-layer") grown on the p^+ silicon substrate. The thickness of the epi-layer ranges between 10-18 μm, then the depletion zone is not as wide as that of hybrids.
When the impinging particle traverse the sensor, the charge generated by ionization is collected by the n-well deposited into the bulk. Since the sensor and the front-end electronics are in the same wafer the bump bonding is not needed and the size of the pixel can be reduced well belowe 20 $\mu m \times 20 \mu m$. Several architectures for the monolithic sensors exist and they will be describe later: standard MAPS, quadruple well, deep n-well, CMOS sensors on high resistivity wafers.

1.3.2 Silicon Strip Detectors

Silicon Strip Detectors (SSD) are divided into single sided and double sided. In a single sided detector, the electrodes are segmented only on one face of the wafer and the position information is unidimensional. Instead, double sided micro strips sensors give a two-dimensional information since both wafer surfaces are patterned. In this manner both the x and y coordinates can be determined. By using the SSDs it is possible to limit the number of channels with respect to that of the pixels maintaining the spatial resolution. In general, strip sensors allow also for a smaller material budget. However, the ghost hit effect is the main drawback of double sided strip sensors. This

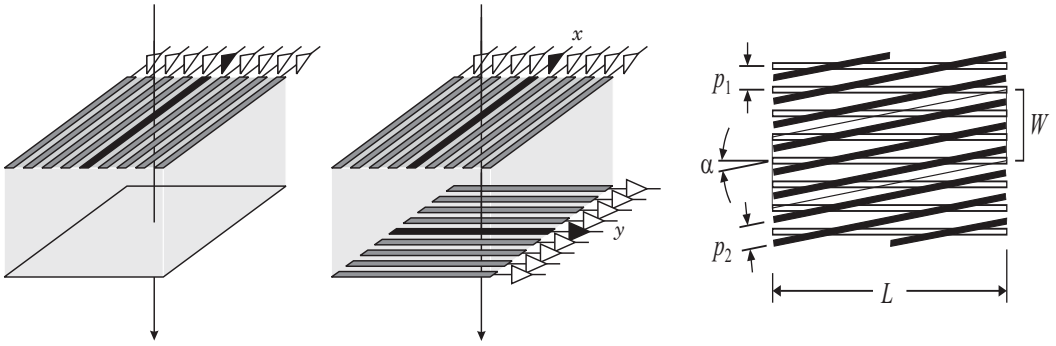


Figure 1.11: (Left) Double-sided micro-Strip Detector: orthogonal strips; (Right)Double-sided micro-Strip Detector: stereo- angle α . [3]

phenomenon occurs when two particles hit simultaneously the detector[5]. Indeed, with the layout depicted above, it is very difficult to identify the different positions of the two particles because each horizontal strip crosses more than one vertical strips. Doing so, the number of points that have to be inspected grows because each strip forms a combination with all of the strip traversing it on the othe side. A compromise solution is to form between the strips on the two opposite side a small angle α named *stereo angle*. The number of ghost hits is minimized because the combinations between the strips are reduced.
To give a qualitative idea of the probability of the ghost hits for each of the two layouts shown in figure 1.11, let's suppose that the length of the sensing elements of each surface is respectively L_1 and L_2 and consider the pitches p_1 and p_2. By setting $\alpha = 90°$, the strips subtend the area $A = L_1 \times L_2$ and the probability of ghost hit is maximized. Instead, let's suppose now $L_1 = L_2 = L$. In case of small *alpha* the probability of "ghosting" is reduced with the magnitude of the stereo angle as the area subtended by the strips is $A \approx L^2(p_2/p_1)\tan\alpha + Lp_2$ [3].
Finally, it must be noted that, unlike pixels, the power of the SSD and the space occupied by its front-end electronics are not limited by the layout of the sensor.

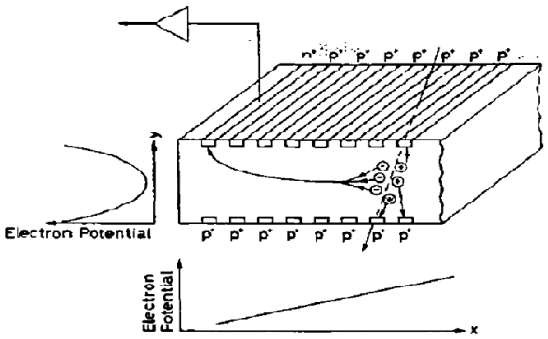


Figure 1.12: Layout of the Silicon Drift Detectors, [4]

1.3.3 Silicon Drift Detector

The layout of a Silicon Drift Detector (SDD) is made depositing p^+ contacts on both surfaces of a n-type silicon wafer. By doing so, two depleted zones are created that are symmetrical with respect to the central zone of the wafer. The formed $p^+ - n$ junctions are then reverse biased to completely deplete the sensitive volume. This is necessary to allow the collection of the electron-hole pairs generated when a particle traverses the sensor. The carriers so generated experience a parabolic potential. The holes are collected by the nearest p^+ strips. The electrons, on the other hand, are pushed to the middle of the n-bulk and then drift to one extreme of the device. Here they are swept towards the surface where they are collected by an array of n^+ contacts. Each collection electrode is connected to its own front-end electronics.
The information about the x coordinate of the impact point of the particle is obtained identifying the electrode that has given the signal. The y coordinate is deduced measuring the time t employed to the charge cloud to arrive in the collection zone and multiplying t by the drift velocity of the electrons.
By using SDD the advantage is to minimize the number of the channels necessary for the read out of a surface. In a typical SDD the pitch between the collection anodes is between 200 and 300 microns. An analog readout is then employed to measure the amplitude of the signals on the anode and the x coordinate is reconstructed by calculating the centroid of the charge distribution.

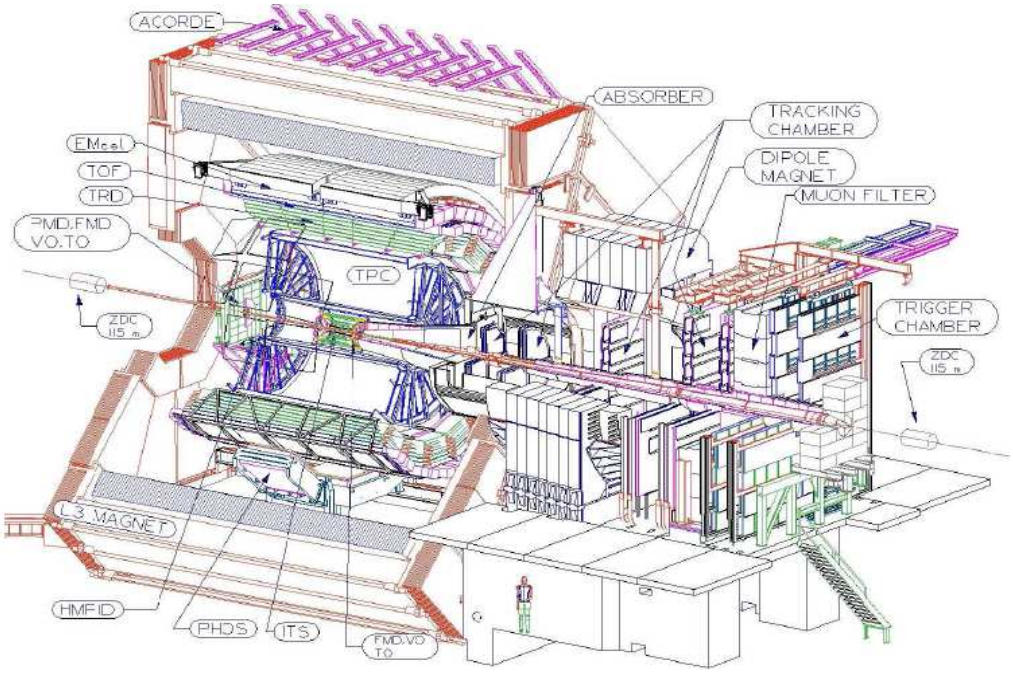


Figure 1.13: ALICE Detector [7]

1.4 An example: the ALICE experiment at CERN

The purpose of the ALICE experiment is to characterize the quark-gluon plasma, that should formed in the collision of ultra-relativistic heavy ions. To achieve this goal, several detectors are used. Starting from the closest layers to the beam pipe and going towards the external part, we have:

- tracking detectors:
  - *Inner Tracking System* (ITS): it is the nearest detector to the interaction point and it is necessary to localize the primary vertex of interaction and to reconstruct the secondary vertex of hyperons and mesons D and B decay.
    The ITS is also employed to identify particles with momentum below 200 MeV/c. The *Inner Tracking System* is described in the following section.
  - *Time-Projection Chamber* (TPC): it is the main tracking detector

of the central barrel and it is employed to measure the charged-particle momentum with a good two track separation. It is also used for particle identification.

- *Particle IDentification* (PID):
  - *Transition Radiation Detector* (TRD): this device identifies electrons with momentum above 1 GeV/c whilst, below this value, particle identification is obtained through the TPC. TRD, ITS and TPC identify the particles but in different ranges of momentum. Therefore it is possible to combine their measurements to study the production of light and heavy vector-meson resonances and the dilepton continuum both in p-p and in Pb-Pb collisions.
  - *Time-of-Flight Detector* (TOF): it is a detector used to recognize pions, kaons and protons for particles momenta ranging from 1 GeV/c to 4 GeV/c. This range of momentum overlaps with those covered by the ITS and the TPC. In fact, the TOF is employed together with these detectors to measure the energy loss of the partcles and to track and reconstruct the vertex of interaction. Doing so, the TOF provides the identification event by event of big samples of pions, kaons and protons.
  - *High-Momentum Particle Identification Detector* (HMPID): this device is based on the ring imaging Cherenkov. Unlike the previous detectors, HMPID is devoted to the recognition of hadrons with a high transverse momentum improving the overall identification capabilities of ALICE.
- electromagnetic calorimeter:
  - PHOS: it is located at 4.6 cm from the vertex of interaction and made of dense scintillating crystals. This calorimeter detects both neutral mesons and photons produced by several mechanisms as thermal production or *hard* QCD processes;
  - EMCal: with Pb-scintillators, this calorimeter has the aim of measuring the *jet* production and the fragmentation function together with the others detectors of ALICE.
- Muon spectrometer: it is a device designed to detect the whole spectrum of heavy-quark resonances with a mass resolution sufficient to separate all states in the channel of decay $\mu^+\mu^-$.

- systems of small detectors dedicated to analyze the characteristics of some global events as the time of interaction (T0, V0, etc...) or for the triggering (FMD and PMD are multiplicity and photon detectors respectively, the ZDC calorimeter, etc..).

In ALICE the sub-detectors covers an angular range from 45°to 135°. Since to perform the measurements the magnetic fields are necessary, as in the case of the determination of the particle momentum, the smallest detectors are located into the dipolar magnetic field unlike the other ALICE detectors that are surrounded by a big solenoid producing a uniform weak magnetic field about 0.5 T [7].

1.5 Inner Tracking System (ITS)

The Inner Tracking System is the nearest detector to the vertex of interaction and consists of six silicon cylindrical layers. They are coaxial and have radii from 3.9 cm to 43 cm. The front-end electronics is located on a very light weight carbon fiber frame. The inner radius measures 3.9 cm since this is the minimum length because ITS surrounds the beam pipe, i.e a 800 μm thick beryllium tube with an outer diameter of 6 cm [7]. Instead, the outer radius of ITS is determined by the requirements to match the tracks of the ITS with those of the TPC.

Given the required accuracy to localize the vertices of interactions ($\approx 10\mu m$), the layers of the current ITS consist of semiconductor detectors, in particular, silicon wafers properly segmented: *Silicon Pixel Detector* (SPD) on the first two layers, *Silicon Drift Detectors* (SDD) on the intermediate layers and *double-sided Silicon micro-Strip Detectors* (SSD) on the last two. The characteristics of detectors that covers ITS layers are shown in figure 1.18.

The SPDs are used for the inner layers of ITS because in this part of the central barrel there is a high density of particles (up to 100 particles per cm^2) and highly segmented detectors are needed to achieve a good distance of closest approach (or dca) resolution. The radius of the first layer is 3.9 cm while the one of the second one is 7.6 cm. With the Silicon Pixel Detectors it is possible to determine the primary vertex position and the impact parameter of the secondary tracks due to the decay of strange, charm and beauty particles also.

The SPDs have been optimized to reduce both the material budget and the mean thickness traversed by a particle perpendicular to the detector surface. They consist of $50\mu m \times 425\mu m$ silicon hybrid pixels that have a binary read

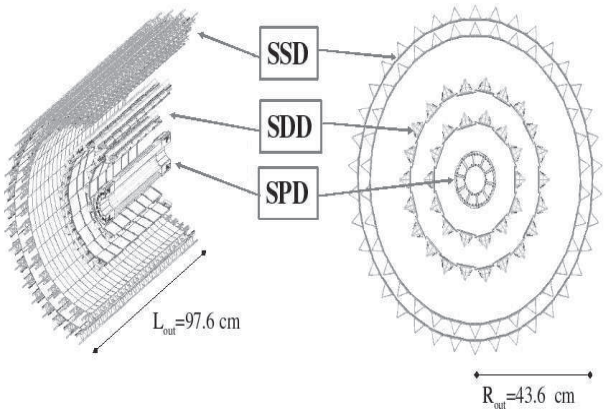


Figure 1.14: Current Detectors of Inner Tracking System, [7]

out[7].

The Silicon Drift Detectors equip the intermediate layers of the ITS that have a radius of 15.0 cm and 23.9 cm respectively. The sensors are 300 μm thick. The density of the tracks for the SDD is less than for SPDs (about 7 particles per cm^2). These detectors allow to identify the particles by measuring the energy loss dE/dx. For each track, the dE/dx is calculated using a truncated mean: if four points are measured, the three lowest points are averaged. If only three points are measured a weighted sum of the lowest and the second lowest point is executed. In addition, the SDDs allow to detect the impact parameter position.

The two outer layers of ITS are equipped with SSDs that face a small track density, about one particle per cm^2 [8]. The read out of the SSDs is analog. The measurements of the position tracks detected are revealed by means of SSDs . These measurements are to be compared both with those obtained by the TPC and the data about dE/dx necessary to identify low momentum particles.

The ITS was designed for a maximum density of 8000 tracks per unit of rapidity. In this case up to 15000 tracks will have to be detected simultaneously. Furthermore, to get an occupancy of a few per cent each layer of the ITS requires several million of active cells. The spatial resolution is about a

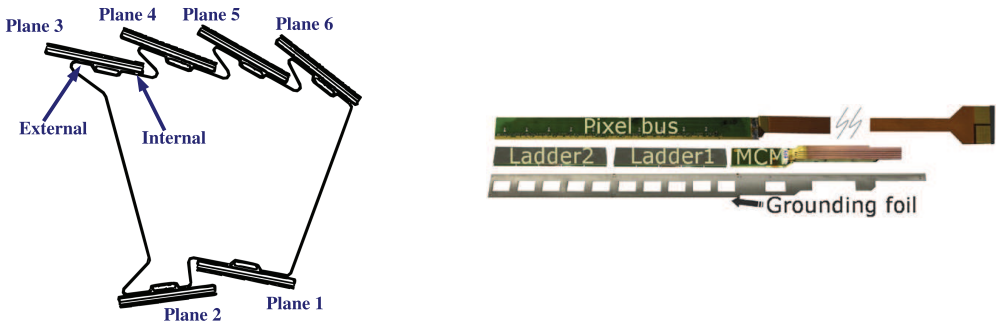


Figure 1.15: (L) Structure of the two inner ITS layers, [7]; (R) Component of the SPDs, [10].

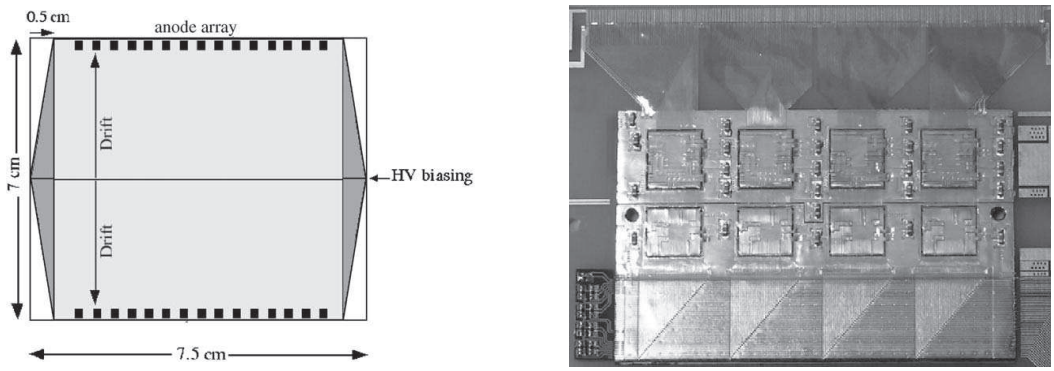


Figure 1.16: (L) Silicon Drift Detector in current ITS, [11]; (R) First prototype of the SPDs, [11].

few tens of μm but goes down up to 12 μm for the two layers near to the primary vertex improving the impact parameter resolution. The latter have to be better than 100 μm in the $r\phi$ for charmed particles [9].
The properties of the current ITS are resumed in figure 1.19.

1.6 Limitations of current ITS and Motivations for the Upgrade

To fully accomplish the physics goals of ALICE an upgrade of the central detectors is needed.

The limitations of the current ITS concern several aspects. Besides the difficulties to access the apparatus for maintenance and repair, the drawbacks that limit the performance of the system are:

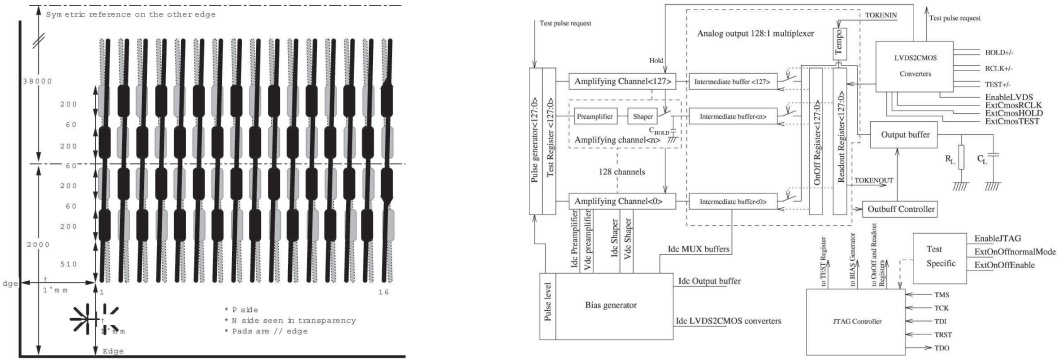


Figure 1.17: (L) Double sided micro Strip Detector in current ITS, [12]; (R) Block diagram of the front-end chip, [12].

- The limited rate that allows to use only a small fraction of the effectively produced Pb-Pb or p-p collisions in LHC. It is planned that the upgraded ITS will work with a readout rate of 50 kHz, to be compared with the 1 kHz of the present detector.This is of primary importance, expecially in case of rare probes.

- An insufficient precision in the determination of the distance of closest approach for transverse momenta below 2 GeV/c for charmed mesons.

- An unsatisfactory resolution for the tracks reconstruction for all baryons formed by more than one heavy quark (beauty e charm).

The new physics program is defined by studying the following benchmark channels [9]:

- charm meson production via $D^0 \to K^-\pi^+$;

- charm baryon production via $\Lambda_c \to pK^-\pi^+$;

- beauty production via

  - $B \to D^0(\to K^-\pi^+)$;
  - $B \to J/\psi(\to e^+e^-)$;
  - $B \to e^+$;

In the new ITS, the increase of the collision will increase also the amount of radiation received by the detectors with the need to have a higher radiation hardness. Furthermore, a reduction of the material budget of the detectors is

Parameter		Silicon Pixel	Silicon Drift	Silicon Strip
Spatial precision rφ	(μm)	12	35	20
Spatial precision z	(μm)	100	25	830
Two track resolution rφ	(μm)	100	200	300
Two track resolution z	(μm)	850	600	2400
Cell size	(μm^2)	50×425	202×294	95×40000
Active area per module	(mm^2)	12.8×69.6	72.5×75.3	73×40
Readout channels per module		40 960	2×256	2×768
Total number of modules		240	260	1698
Total number of readout channels	(k)	9 835	133	2608
Total number of cells	(M)	9.84	23	2.6
Max. occupancy for central Pb-Pb (inner layer)	(%)	2.1	2.5	4
Max. occupancy for central Pb-Pb (outer layer)	(%)	0.6	1.0	3.3
Power dissipation in barrel	(W)	1350	1060	850
Power dissipation end-cap	(W)	30	1750	1150

Figure 1.18: Characteristics of the varius detector types, [7]

essential to limit the multiple scattering and improve the resolution. [4] The current impact parameter resolution does not allow to detect particles that have a decay length below $100\mu m$. By means of the new detector it should be possible to achieve exclusive measurement of the beauty production and obtain data with sufficient accuracy also for low momenta.

1.7 Options for Upgrade

At the time of this writing, two options are considered for the ITS upgrade. The first option foresees to use pixellated detector in the first three layers and double sided silicon microstrips in the four outermost layers. In this case, the pixel sensors could be either of the hybrid type or monolithics. In

[4] The thick of the current silicon detetectors is $\approx 350\mu m$

Layer / Type	r [cm]	$\pm z$ [cm]	Number of modules	Active area per module $r\phi \times z$ [mm^2]	Intrinsic resolution [μm] $r\phi$	z	Material budget X/X_0 [%]
Beam pipe	2.94	-	-	-	-		0.22
1 / pixel	3.9	14.1	80	12.8 × 70.7	12	100	1.14
2 / pixel	7.6	14.1	160	12.8 × 70.7	12	100	1.14
Th. shield	11.5	-	-	-	-		0.65
3 / drift	15.0	22.2	84	70.2 × 75.3	35	25	1.13
4 / drift	23.9	29.7	176	70.2 × 75.3	35	25	1.26
Th. shield	31.0	-	-	-	-		0.65
5 / strip	38.0	43.1	748	73 × 40	20	830	0.83
6 / strip	43.0	48.9	950	73 × 40	20	830	0.83

Figure 1.19: Characteristics of current ITS detectors, [7]

the second option, the ITS will consist only of pixel detectors. The cost of hybrid pixel sensors prevent them from beign used to cover large surfaces. Therefore, the second scenario implies the use of monolithic CMOS sensors for the whole apparatus. CMOS sensors offer the obvious advantages of allowing for smaller pixels and reduced cost. However, their capability of whistanding the radiation doses required in the inner part of ALICE is not yet fully demonstrated. For this reason, a dedicated R&D is in progress within the ALICE collaboration. The results obtained on first prototypes are however very encouraging and this weight the balance more in favor of the monolithic option. At larger radii, the use of monolithics poses challenges for what concern the integration and the power dissipation. In fact, the size of monolithic sensors is limited by the reticle size used in the production of CMOS chips, which can be in the order of 2 cm×3 cm. The use of such small sensors to cover large area may result in additional inneficiency. A particular

procedure, called stiching, allows to produce CMOS sensors which are larger then the reticle size. In this way, sensors with a surface comparable with the one of a standard microstrip detectors could be fabricated. However, the yield of such large structures must be assessed. Another concern in using of CMOS sensors at larger radii is their power consumption, which is still higher than the one found in a typical strip sensors. Finally, it must be mentioned that the use of four layers of strips will allow to maintain in the future tracker a particle identification capability comparable with the one of the present ITS. Simulations have also suggested that a sufficient, although not optimal, PID performance could be provided by equipping seven layers of monolithic sensors with analog readout. The final layout will be chosen by the end of 2013. Several technologies are considered to design of the front-end electronics. In particular, 0.13 μm CMOS technology could replace the 0.25 μm CMOS technology currently used for the LHC detectors. The 0.13 μm CMOS is to be preferred because of its radiation tolerance: indeed, the reduced dimensions of this technology causes the smaller capacitance of the digital gates and the lower power supply voltage reduces the digital power consumption. Finally, the 0.13 μm CMOS technology is very versatile then permits to avoid interferences between digital and analog blocks [8].

The last technology considered for the upgrade of ALICE, that will be likely used, is offered by TOWER/JAZZ: this is a 0.18 μm quadruple well CMOS standard process widely used for image sensors. This technology has been identified as the most promising candidate for dedicated R&D in ALICE since it has some interesting features:

1. A high resistivity epitaxial layer up to 18 μm thick and a gate oxide thickness below 4nm which make the sensor more robust to the dose radiation;

2. The resistivity of the epitaxial layer ranges from 1 kΩcm to 5 kΩcm, thus the 18 μm thick epitaxial layer can be depleted by applying a revers bias between 1-2 V, in order to increase both the signal-to-noise ratio and the radiation hardness;

3. The possibility to fabricate in same pixel area both PMOS and NMOS to make more complex in-pixel signal processing [8].

In any case, the signals which are registered in the sensor chip will be sent out by using a LVDS transmission in order to minimize the ground loop effect and the switching noise. By means of the LVDS transmission the current direction can be varied in order to transmit two different logic level.

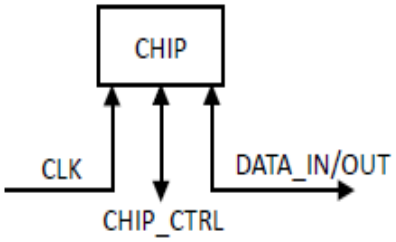


Figure 1.20: I/O of a single chip, [**?**]

In figure 1.20 a schematic view of the data transmission in showed. The CLK is a master clock which controls the on chip synchronous logic levels and it is unidirectional (input of the chip); the CHIP_CTRL and the DAT_IN/OUT are bidirectional: the first one controls the write/red chip configuration an provides trigger information and global asynchronous reset whereas the second one sends out the stored signals.

Chapter 2

Monolithic Active Pixel Sensors

Monolithic Active Pixels (MAPS) are of central interest for the ITS upgrade. Actually, MAPS can be thinned down to 50 μm or less. Furthermore, the may allow a significant cost reduction due to the use of standard CMOS technologies for their production and because no hybridization processes is needed. In fact, unlike hybrid pixels, in the monolithics both the sensor and read out electronics are in the same wafer. With MAPS, very small pixels can be achieved (pixel smaller than 2 μm $\times$ 2 μm are already in production) even though the size of a pixel used in high energy physics is in general bigger than 10 μm $\times$ 10 μm . In fact, a pixel as large as 100 μm is often already adequate.

A silicon wafer used for standard CMOS technologies for the electronics (*electronic grade*) needs to have low resistivity and is grown by the Czochralski method. Unfortunately, this technique leave in the silicon bulk both crystalline defects and atoms of impurities, like oxygen. In addition, also the formation of structural defects may occur. Instead, a *detector grade* silicon must have a high resistivity that allows to deplete easily the sensitive volume. A low density of defects is also necessary to reduce both the generation and the recombination of the carriers by the mechanism of trapping that modify the leakage current flowing in the device. Because of monolithic integration it has been necessary to match both the requirement of high resistivity for the sensor and low resistivity for the electronics. This is made by growing a silicon epitaxial layer on the Czochralski substrate, with the advantage to have a very ordered epitaxial layer with a poor probability to incorporate impurities, i.e. an epy-layer with a low density defects. The overall thickness occupied by sensor and electronics can be reduced to less than 50 μm.

The operating principle of a MAPS is based on the creation of p-n junction that works for the collection of the charge produced by a ionizing particle

traversing a detector. The carriers so generated into the device move because of thermal diffusion, so the time necessary to collect the charge is comparatively long, $\approx 100\ ns$. Due to the long collection time, the probability of charge recombination is increased. This may become a probelm when the devices are exposed to non-ionizing radiation that damages the silicon bulk. An alternative solution to the active pixel sensors (APS), still using the monolithic integration of both sensor and read out electronics, requires the application of reverse bias to the collection diode: in this manner the depletion of the sensible volume is driven and the transport of the charge is mainly due to the drift, so the charge collection is very fast.

This chapter starts with a review of the working principle of a p-n junction, i.e the sensor key structure.
In the section 2.2 the principle of operation of standard MAPS is shown: these sensors, even if they have many interesting features for a tracking detector, exhibit some limitations about the components that it is possible to use for the read out. Two modified designs allow to overcome limits imposed by the layout of standard MAPS and they are discussed in sections 2.3 (DNW MAPS) and 2.4 (INMAPS).
In the sensors mentioned up to now, charge is collected by diffusion; instead, in both LePix (section 2.5) and pixel detectors in high voltage CMOS technology (section 2.6) an electrical field is applied to speed up the collection process.
In conclusion general aspects about the singal readout in monolithic sensors are discussed. In section 2.7 the amplifiers used for a MAPS are analyzed while in section 2.8 the Correlated Double Sampling technique is described since it is employed to remove both offset and low frequency noise that affect the signal charge measured by each pixel.

2.1 P-n junction

Silicon is a semiconductor widely employed in electronics since its resistivity can be modified by means of the doping with donors (n-type) or acceptors (p-type).
The resistivity of silicon doped with a n_p density of acceptors and n_n of donors is given by:

$$\rho = \frac{1}{q(\mu_n n_n + \mu_p n_p)} \tag{2.1}$$

ρ can be varied adjusting the density of the dopants. For example, setting $n_p >> n_n$ the majority charge carriers in the material are the holes so the

silicon resistivity is $\rho \approx 1/(q\mu_p n_p)$.
The doping levels are typically $10^{14} - 10^{19}$ atoms/cm^3.

When two regions of a semiconductor are doped with complementary impurities, such as p-type and n-type regions, a p-n junction is formed. Because of the gradient of concentrations of holes as well as electrons between the two regions in the material, the thermal diffusion will drive the majority charge carriers across the junction, leaving in the p-type region an excess of negative ions and in the n-type an excess of positive ions. Therefore, a region of non-mobile space charge is formed. The potential barrier V_{bi} is generated between the two space charge densities. This potential prevents electrons and holes from diffusing further. In other words, between the space charge densities the electrical field $\vec{\mathcal{E}}$ is established and it accelerates particles of opposite charges in opposite direction.
No mobile charge carrier is in the central zone of the junction that, for this reason, is named depletion zone: its spatial extent W depends on the doping levels with donors N_D for the n region or acceptors N_A for the p region:

$$W = \sqrt{\frac{2\epsilon_s V_{bi}}{q}\Big(\frac{1}{N_A} + \frac{1}{N_D}\Big)} \tag{2.2}$$

where ϵ_s is the silicon dielectric constant and q is the electrical charge.
Since the density of the dopants are not symmetrical, W is wider in the part in which the doping level is lower. For example, if we consider $N_D >> N_A$, where the junction is asymmetrical with a very strong doping level of the n region ($p - n^+$), the depletion zone is more extended in the p region than in the n region.

When a ionizing particle hits the diode and traverses the depletion zone, it loses energy according to the formula (1.13). The energy lost causes the generation of the free charge carriers that are efficiently separated by the electrical field of the junction.
Having a large depletion zone implies to increase the size of the sensitive volume of the diode and, consequently, the magnitude of the registered signal. The depletion zone can be widened by reverse biasing the junction, i.e. connecting the p region to a lower voltage then the n region:

$$W = \sqrt{\frac{2\epsilon_s (V_{bi} + V)}{q}\Big(\frac{1}{N_A} + \frac{1}{N_D}\Big)} \tag{2.3}$$

This fact rises the height of the potential barriers for majority charge carriers in each part of the diode, so stopping their diffusion. However, the

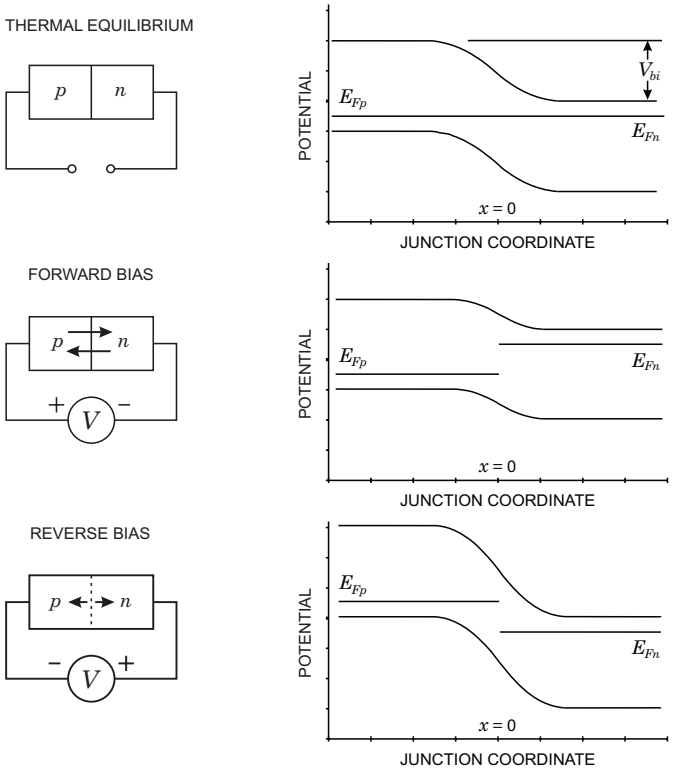


Figure 2.1: p-n junction: the the height of the potential barriers changes depending on the bias, [3].

reverse bias that can be applied to the junction is limited because too high values can lead to junction breakdown.
The negative potential difference at the junction limits the thermal diffusion of the carriers, but the minority charge carriers[1] can move across the junction. Thermally generated carriers in the depletion region are swept by the electric field, generating a leakage current. The leakage current depends on the intrinsic carrier concentration n_i of the silicon ($n_i = 1.45 \cdot 10^{10} cm^{-3}$), the diffusion constant $D_{p,n}$ of both holes and electrons, the diffusion length $L_{p,n}$ of the charge carriers [2] and on the diode section A:

$$I_s = -q\Big[\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D}\Big] n_i^2 A \tag{2.4}$$

Since the concentration of minority carriers is lower than that of the majority carriers, the current I_s is very low, about nA in silicon.
In the junction diode the electrical current flows in one direction only: this is a feature of this device. In fact, when the diode is forward biased the magnitude of the potential barrier between the junction is lowered, in favor of the minority carriers current. The ideal I-V characteristics of the diode is then:

$$I = I_s(e^{\frac{qV}{k_B T}} - 1) \tag{2.5}$$

where V is the tension applied (forward or reverse bias); this characteristics is shown in figure 2.2.

Because of the opposite ions in the two regions of the p-n junction, a diode resembles a capacitor which has a capacitance given by $C_j = (\epsilon_s A)/W$. The capacitance hence depends on the section of the diode as well as on the length of the depletion zone, i.e. $C_j = (\epsilon_s A)/W$ depends on the doping levels of the n and p regions [2]. The value of C_j is important for the charge conversion efficiency (from current signal to voltage signal) as well as for its influence on the thermal noise of the front-end electronics. However, C_j does not affect the shot noise i_n that is given by $i_n = \sqrt{2qI_g\Delta f}$, where I_g is the electrical current generated by a particles that traverses the device and Δf is the bandwidth.

[1] Minority carriers are electrons in a p-region or holes in n-region

[2] The diffusion length is the mean specific distance that a free charge covers in the material because of the thermal diffusion, before recombining it with a carriers of opposite charge. $L_{p,n}$ is given by: $L_{p,n} = \sqrt{D_{p,n}\tau_{p,n}}$, where $\tau \approx \mu s$ is the time needed for a decrease of 1/e of the minority carriers.

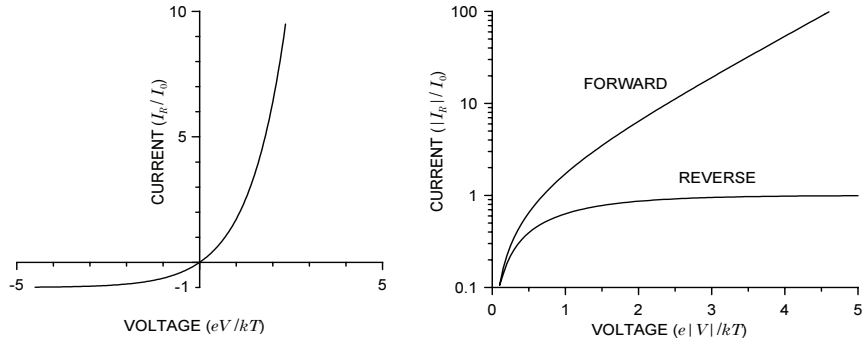


Figure 2.2: I-V characteristics[3]

2.2 Standard MAPS

A standard MAPS is made of a silicon substrate at low resistivity heavily doped with p-impurities. On the substrate, a p-doped epitaxial layer (p epi-layer) is grown. The p epi-layer can be up to 20 μm thick. Moving towards the surface there is a n-well[3], forming with the p epi-layer the collection charge diode. Under the n-well, a thin depletion region is formed in which the electrons generated in the sensitive volume, that is in the epi-layer, are collected.
The doping level p^- of the epi-layer is much smaller from that of the p^{++} substrate as well as of that of p^+ p-wells: this is the reason why a depletion region is formed. The charge generated in the undepleted epi-layer move because of thermal diffusion. When they reach the depletion region associated to a nwell-p-epi junction they are collected by the electric field present in the depletion zone.
Actually, the charge carriers are also generated in the substrate but here the probability of charge recombination is very high. In fact, the carriers move in the bulk driven by the thermal diffusion, so they are fairly slow. In addition, the substrate is very thick and has a very high doping level. All this implies that the generated particles recombine each others before bing collected so they do not contribute to the signal current in the detector.

[3]The doping level of the n-well is typically about 10^{18}atomi/cm^3.

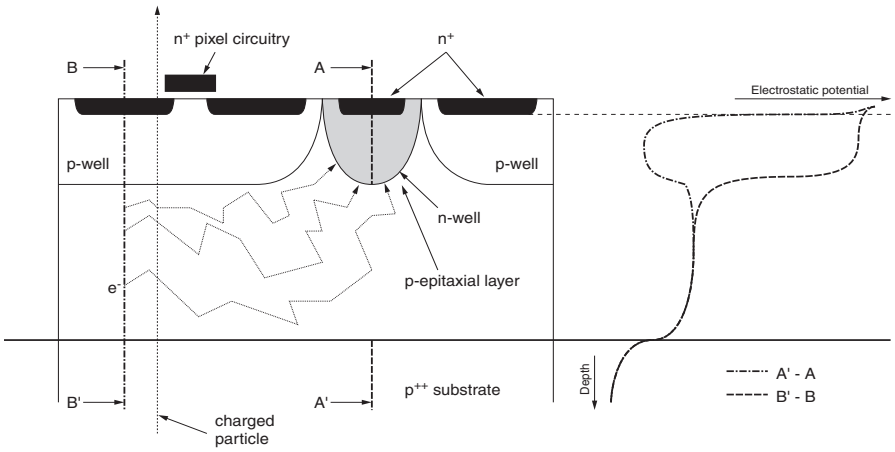


Figure 2.3: Standard MAPS operating principle: (L) Charge Diffusion in the p epi-layer; (R) Potential distribution in the device. [2]

Since the sensitive volume is very thin, the charge signal collected is weaker ($\approx 1000e^-$) compared to that produced in the hybrid pixels, so the noise in the read out electronics circuitry must be minimized [13].

The simpler and most compact structure of a MAPS pixel is shown in figure 2.4: the collection diode is modeled by a current source with a capacitance C_{PD} in parallel, while the read out circuit is formed by three NMOS transistors (3T architecture).

M_1 is the reset transistor necessary to restore the dc bias point of the diode after each readout and to charge the diode capacitance at the power supply V_{dd}; M_2 is a source follower; M_3 is a pass transistor connected to the read out electronics, through which the output is accessed [14].
The circuit shown in figure 2.4 converts the current generated in the diode into the voltage output v_{out} of the pixel. v_{out} depends on the capacitance C_{PD} as well as on the gain[4] A_{SF} is the gain of the source follower which it is

[4]With a small signal model the gain of the source follower is $\frac{v_{out}}{v_{in}} = \frac{g_m}{g_m+g_{mb}} \approx \frac{1}{1+1/3} < 1$. Here: g_m is the transconductance of the transistor that generally depends on the size of the device; g_{mb} is the bulk transconductance that represents the effect of on the current of the voltage variation between source and bulk when the source is not grounded.

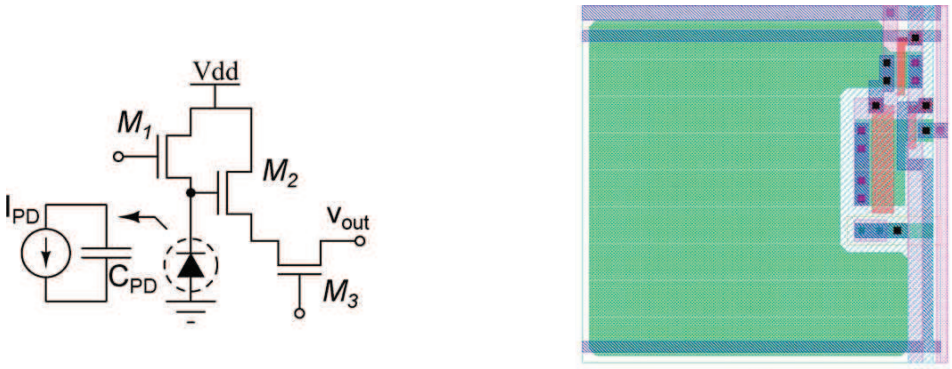


Figure 2.4: (L) The 3T Pixel Circuit with NMOS transistors ; (R) Layout of the 3T pixel circuit . [14]

below one:

$$v_{out} = A_{SF}\frac{1}{C_{PD}}\int I_{PD}dt \tag{2.6}$$

The formula 2.6 shows that to obtain an high voltage output the value of the capacitance C_{PD} must be minimized, which implies a small collection electrode. The further advantage in using the 3T architecture is the reduction of power consumption since the amplifier circuit can be turned on only when the pixel is read.

A more complex circuit used for the pixels is the CTIA, i.e. *Capacitive Transimpedance Amplifier*, shown in figure 2.5. Here A is a single stage cascode amplifier designed with both NMOS and PMOS transistors and it is AC coupled to the sensing diode.
Transistor M_1 is a reset switch: it will be on to discharge the capacitor C_{fb} and off at the beginning the integration time. In the CTIA architecture v_{out} depends on the feedback capacitance [5]: this is an advantage over 3T architecture in which v_{out} is determined by the diode capacitance that it is difficult to control since it depends of several quantities, e.g. the width of the depletion region.
With $C_{fb} << C_{PD}$ and for high gain of the amplifier (in this context the cascode configuration is fundamental), the circuit effectively pins the diode output and drives the current I_{PD} to charge the feedback capacitance. Then,

[5]The equation of the circuit is given by: $I_{PD(s)} + \frac{v_{out(s)}}{A}sC_{PD} + \left(\frac{v_{out(s)}}{A} - v_{out(s)}\right)sC_{fb} = 0$

the output of the amplifier is:

$$v_{out} = \frac{1}{C_{fb}} \int I_{PD} dt \tag{2.7}$$

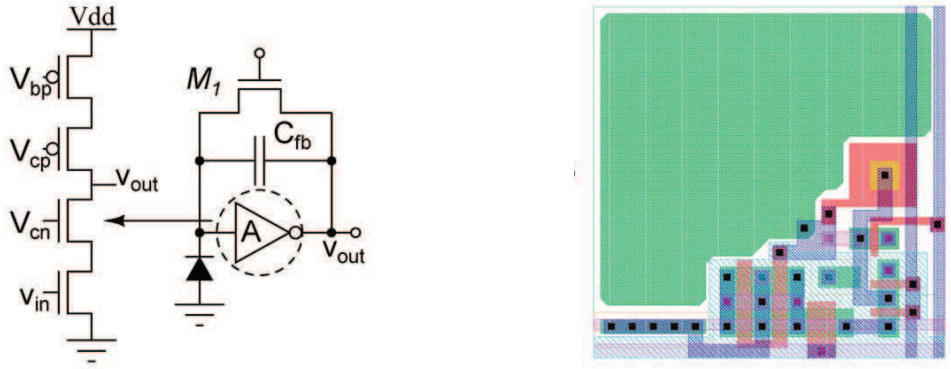


Figure 2.5: (L) The CTIA Pixel Circuit: A is a single stage cascode amplifier with NMOS and PMOS transistors; (R) Layout of the CTIA Pixel Circuit [14]

In the schemes shown in the figures 2.4 and 2.5 NMOS and PMOS are employed, even though the layout of standard monolithic active sensors allows us to use n-type transistors only. In fact, the building of the p-type transistors requires two further n-wells on the p-type epitaxial layer. However, these n-wells are in competition for the charge collection with the standard n-well, worsening the collection efficiency.
To compensate the above problem, MAPS with NMOS only can be used, otherwise the read out circuits that need PMOS transistors can be moved on the periphery of the matrix [13].
The need to use p-type transistors is linked to the need to make more complex circuits for the in-pixel signal processing than those designed with NMOS only. For this reason, several alternative layouts of MAPS have been developed. These allow that both n- and p-type transistors can be used without efficiency reduction.

2.3 Deep n-well MAPS

The SLIM5 collaboration submitted an alternative design of a monolithic active pixel sensor. This new device allow to build PMOS and NMOS on the same layer, limiting the drawback of the competing n-wells (CNW).

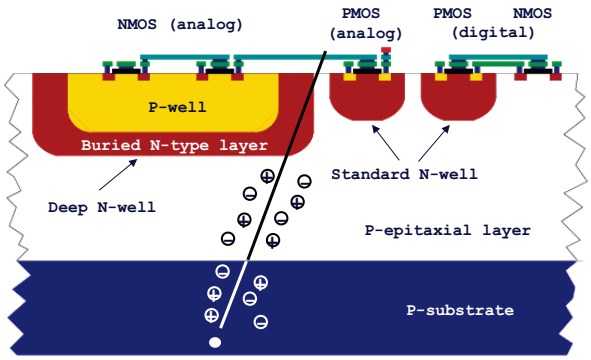


Figure 2.6: Layout of the DNW MAPS, [15]

This technology is the *deep n-well* MAPS (DNW MAPS) based on the *triple well* option offered by many deep submicron CMOS processes. It should be noted that both the analog and the digital part of the front-end are in the same pixel.

The design of a DNW MAPS is shown in figure 2.6: in the p-type epitaxial layer a very large deep n-well is embedded and on it another p-well is grown. In this p-well the n^+ implants are formed. These will provide the source and drain of of the n-type transistors .
On the DNW MAPS the collecting diode is formed between the epitaxial layer and the DNW. The front-end electronics is overlapped with the area of the sensitive element, so to allow a more complex in pixel read out electronics [16].
The chain of the analog read out is formed by the charge sensitive amplifier (CSA) directly connected to the deep n-well, the RC-CR shaper, the discriminator and finally a latch. The asynchronous discriminated signal is stored by a latch and after processed by the digital read out located in the periphery of the pixel.

Since the CSA is directly placed in the pixel, the voltage gain does not depend on the collecting diode capacitance but on the feedback capacitance. Than, employing a DNW allows one to have collecting electrodes very large and, accordingly, the pixel area can large up to 900 μm^2 with a 50 μm pitch: This permits to implant the CNWs far from the DNW so that the charge-collection efficiency of the sensor is not affected (the fill factor is about 90%). Finally, in the CNW the PMOS transistors, that are necessary for both ana-

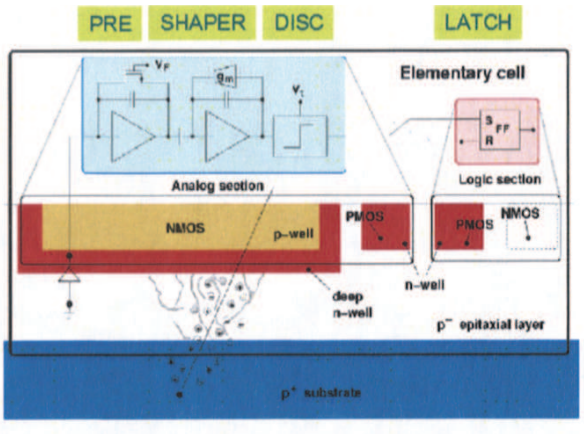


Figure 2.7: Layout of the DNW MAPS, [15]

log and digital read out, are placed [15]. However, it should be noted that although the above trick using DNWs, competing n-wells are not shielded from collecting the generated charge carriers.

Several prototypes of DNW monolithic active pixel sensors (APSEL, Active Pixel Sensor Electonics) have been realized with the STMicroelctronics in 130 nm triple well technology using sparsified read out techniques. However, they have undergone some changes about front-end electronics and sensor both to improve the signal-to-noise ration and to reduce power consumption. The charge collection efficiency of a DNW depends on both its shape as well as its fill factor[6]. The fill factor can be optimized varying the size of the collecting electrode and of the competing n-wells.

In this context, Apsel $3T_1$ chip (member of the Apsel series) have been tested. It is composed by two 3×3 pixel matrices which differ in the shape of deep n-wells only: in type M_1 matrix the DNW is rectangular and connected to additional satellite n-well. In the M_2 matrix, instead, the central DNW is "T" shaped. The two matrices covered a $150\mu m \times 150\mu m$ area and the distance between them is about 200 μm; each among the nine pixel that compose the matrices have its own read out circuit.
Apsel $3T_1$ chip was tested in 2008 with photons from ^{55}Fe and electrons from ^{90}Sr [15]. Another test was executed in 2009 at the SPS H6 beam line at CERN with a 120 GeV/c pion to measure both the charge collection and tracking efficiency; the gain of the analog read out circuit was tested before the beam test using K_α and K_β lines from ^{55}Fe since these lines generate a well-know charge quantity. In addition, the radiation hardness of the chip

[6]The fill factor is given dividing the area of the deep n-well by the pixel area [16].

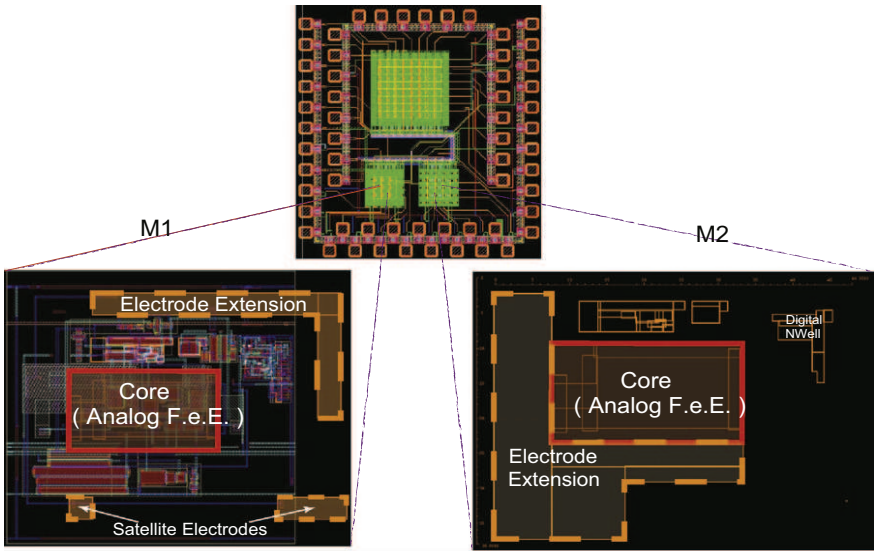


Figure 2.8: Apsel $3T_1$ chip: elementary cell of M_1 and M_2 matrices, [**?**].

was tested using a 10 MRad dose from^{60}Co.
In the experiment with pions the total charge collected by matrices M_1 e M_2 was obtained considering all nine pixels of the 3×3 cluster and exhibits a Landau distribution [16].
The data obtained by the beam test showed that the *most probable value* (MPV) of the Landau distribution, noise and signal-to-noise ratio are higher for the type M_1 matrix than type M_2 matrix, both before and after the ^{60}Co dose.

2.4 Isolated n-well MAPS (INMAPS) or Quadruple Well technology

The quadruple well technology was introduced for CMOS image sensors which are used, for instance, in full frame digital cameras. This technology turns out to be interesting for particle physics since it allows to maintain charge collection efficiency of the standard MAPS and, simultaneously, to position NMOS and PMOS within the same pixel.

INMAPS pixels are based on standard MAPS: on a very low resistivity p-type substrate (about a few tens of $m\Omega \cdot cm$), a few tens of μm thick, a 20 μm thickness epitaxial layer, whose resistivity is about 10 $\Omega \cdot cm$ up to a few $k\Omega \cdot cm$, is grown. The p-wells and the n-wells are placed on the wafer

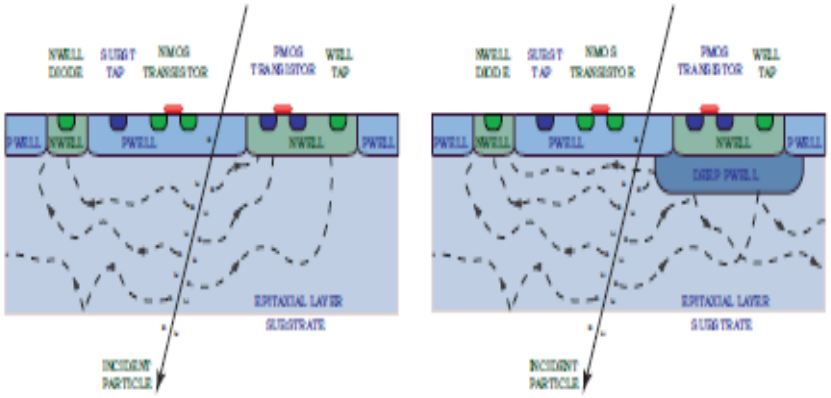


Figure 2.9: Comparison between standard MAPS and INMAPS

surface: the p-wells are occupied by NMOS transistors whereas the n-wells form the charge collecting diode with the epi-layer.
Regarding the isolated n-well MAPS, there is a gradient of the p-type doping level due to which two potential barriers are generated: the first one is located between the epi-layer and the substrate whereas the second one is situated between the p-wells and the epi-layer. The charge carriers generated by ionizing particles move due to the thermal diffusion. The potential barriers repel the charge carriers (electrons), keeping them within the epitaxial layer.
In the INMAPS a further n-well, inside which the PMOS transistors are placed, is implanted. This nwell is shielded from the substrate by a deep pwell, so it does not compete with the main nwell for the charge collection. In fact, the deep p-well, by stopping the charge carriers, shields and isolates the collecting electrode.

INMAPS pixels were developed in 0.18 μm standard CMOS technology that features six metal layers and passive precision components for analog design.
The quadruple well process allow to build sensors with a complex in-pixel processing, while maitaining a high charge collection efficiency.

In order to demonstrate the feasibility of the INMAPS approach, the test sensor TPAC1.0 was designed for an electromagnetic calorimeter present in the ILC, which requires that each pixel recognizes the passage of a MIP.
TPAC1.0 incorporates sub-arrays containing four different pixel designs, amongst which the most important are *preShape* and *preSample* architectures.
To give an example, figure 2.11 shows the layout of a 3×3 array for *pre-*

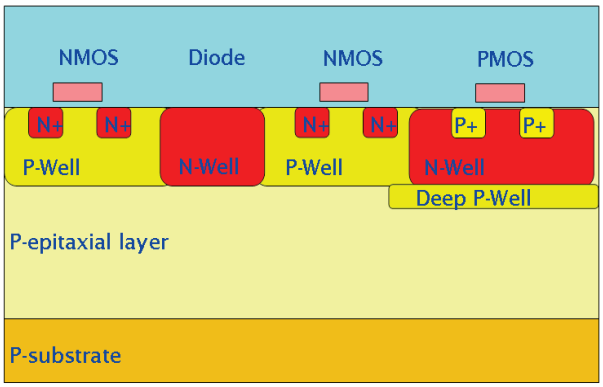


Figure 2.10: Cross section of a quadruple well techology INMAPS, [17]

Shape architecture of TPAC1.0 sensor. Each pixel is a $50\mu m \times 50\mu m$ square: n-wells are purple whilst p-wells are gray. The charge collecting diodes are represented by four small lateral squares on each pixel. They are kept very small in order to minimize the parasitic capacitance and obtain a high signal-to-noise ratio. In addition, the four diodes are connected together by metal lines. Finally, the transistors and the other read out elements occupy the n-wells placed in the deep p-wells.

2.5 LePix

Although the operation principle of LePix is very similar to that of a standard MAPS since in both of them a p-n junction is generated to collect the charge, their sensors layout are, in some respects, rather different .
Likewise the standard MAPS, in LePix both the sensor and the read out electronics are integrated on the same silicon wafer. The substrate is p-type whereas the collecting electrode is an n-well. However, the input transistor is not hosted in the p-wells but placed in the n-well.
As for the hybrid pixels, if we apply a reverse bias to the device, the depletion region of the collecting diode is enlarged and an electrical field $\vec{\mathcal{E}}$ is determined. $\vec{\mathcal{E}}$ will drive the motion of the charge carriers so that drift preponderates over the random walk caused by thermal diffusion.

The voltage signal generated in LePix is directly proportional to the charge collected by the diode and in inversely proportional to its parasitic

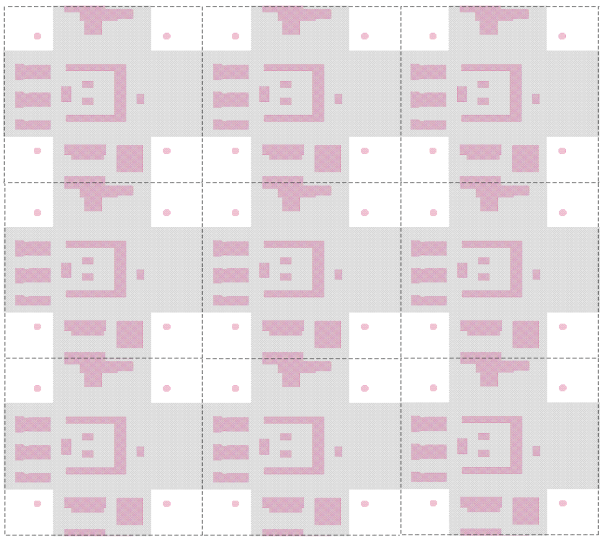


Figure 2.11: Layout of a 3×3 array of the preShape architecture, [17]

capacitance. In order to maximize the conversion gain at a certain fixed signal-to-noise ratio the parasitic capacitance must be minimized. For this purpose it is necessary to use very small pixels combined with a high resistivity substrate ($> 100\ \Omega \cdot cm$). For a 30 μm depletion layer and 10 fF sensor capacitance, the voltage signal due to the passage of a MIP is about 38 mV. In LePix all the NMOS transistors must be placed in a triple well in order to isolate them from the substrate which is kept at high voltage. For this reason it is preferable to use a PMOS device as input transistor in order to maintain a low occupancy. Analog and digital circuits, which are built with the same CMOS standard process, are positioned at the periphery of the chip.

The main goal when LePix devices are employed is to create a uniform depletion region below a small collecting electrode, in order to have an homogeneous sensor response. For this reason guard rings in the area around the pixel are used to bound the high voltage region.
The simulation of the sensor showed that, when we apply a 100 V reverse bias, a uniform depletion layer of some tens of μm can be obtained, avoiding the device breakdown [18].

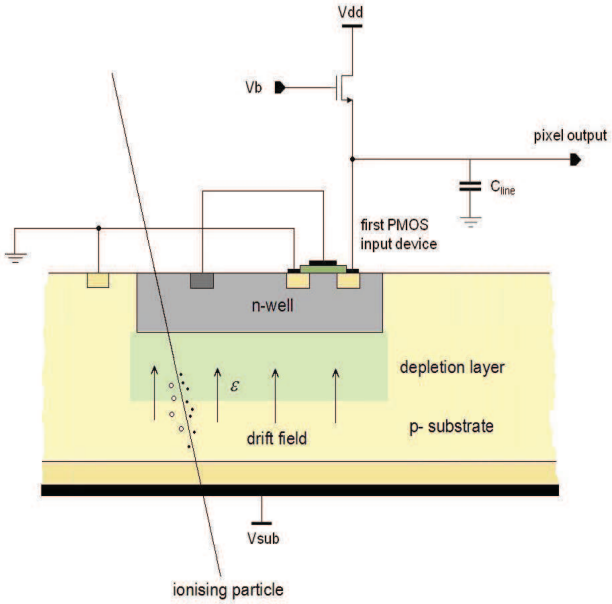


Figure 2.12: Cross section of LePix sensor, [18]

A strong point of the LePix project lies in its parallel pixel read-out which makes the matrices scanning process faster than the serial read out of the standard MAPS. However, since each pixel has its own read-out circuit, the interconnection density is high and requires an *ultra-fine* pitch litography: this is the reason why the 90 nm standard CMOS technology is used in the design of the LePix.

2.6 Pixel detectors in high-voltage CMOS technology

As a further alternative to the monolithic active pixel sensors, Perić *et al.* [19] proposed a new series of detectors in High-Voltage CMOS technology featuring a layout of the devices similar to that of DNW MAPS due to the deep n-well option. The pixel so designed is called "smart diode" (SD): the deep n-well and the substrate inside on which is located form the collecting diode, and only the deep n-well hosts the overall CMOS electronics of each pixel.
As shown on the left of the figure 2.13, PMOS transistors are directly placed inside the DNW whilst NMOS transistors are in the p-well which is enclosed in the DWN. This is different from the deep n-well approach discussed above, since the PMOS transistors are placed directly in the sensing diode .

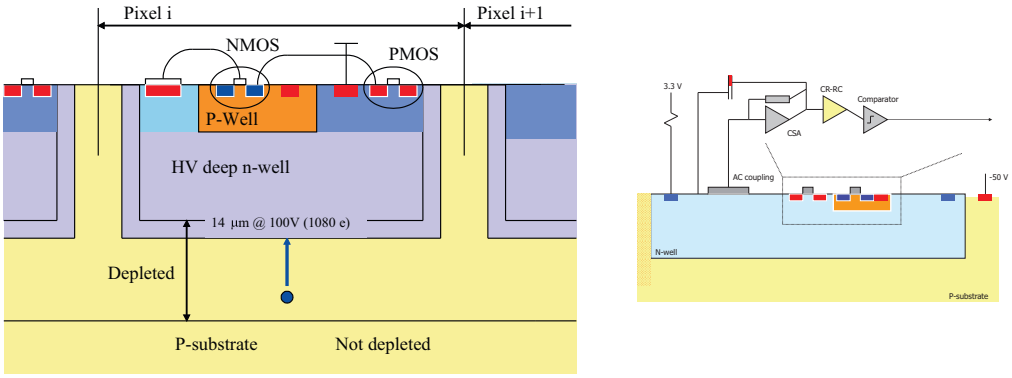


Figure 2.13: Layout of "smart diode" [19]

Another element of novelty lies in the use of H-V CMOS technology since the SD is designed so that the collecting electrode can be reverse biased with respect to the substrate which gives two advantages:

1. the possibility to enlarge the depletion region in order to record a high signal;

2. the collection charge by drift.

A reverse bias about $\approx 100\ V$ is sufficient to create a depletion region of $14\ \mu m$.
Due to the drift, the charge carriers move very fast in the device thus the time interval used to collect the charge is ≈ 40 ps, which is very small compared to the time interval obtained with the MAPS that is ≈ 100 ns.
In order to bias the deep n-well a reset switch or a bias resistor are generally used. Their purpose is to restore the voltage of the n-well which is slightly lowered once the charge signal is collected. In addition, the n-well hosts a CSA (Charge Sensitive Amplifier) that amplifies the recorded current signal and converts it into a voltage. These operations are executed before the voltage level of the n-well is restored.

Likewise DNW MAPS, the high voltage CMOS technology used for the detectors allows us to employ both NMOS and PMOS transistors so that the in-pixel signal processing can be very fast. PMOS transistors are fundamental in this case also for the radiation tolerance. In fact, SDs permit to employ radiation tolerant p-type transistors which limit the radiation damages amongst which are: the increase of the leakage current; the inversion of the doping type in the depleted region; the formation of crystal defects that

are similar to “traps” for the charge carries generated by the ionization of the material.
This technology allows to diminish the production costs thanks to the monolithic integration of the electronics and the sensor developed with the same CMOS process. HV CMOS technologies are in fact widely used in commercial applications, such as automotive electronics, LCD monitors, mobile phones, etc.

The main drawbacks of this approach are:

- the capacitive coupling between the drain-source regions of the pmos transistors and the nwell which can trigger positive feedback. The use of CMOS circuit topologies hence required very careful design.
- The size of collecting electrode which imposes values of the capacitance in the range from 10 fF to 200 fF, depending on the size of the pixel and the architecture of the read out circuit. This requires higher power consumption in the front-end to maintain good signal-to-noise ratio.
- The signals generated in the partially depleted sensor are lower than those collected in a totally depleted device.

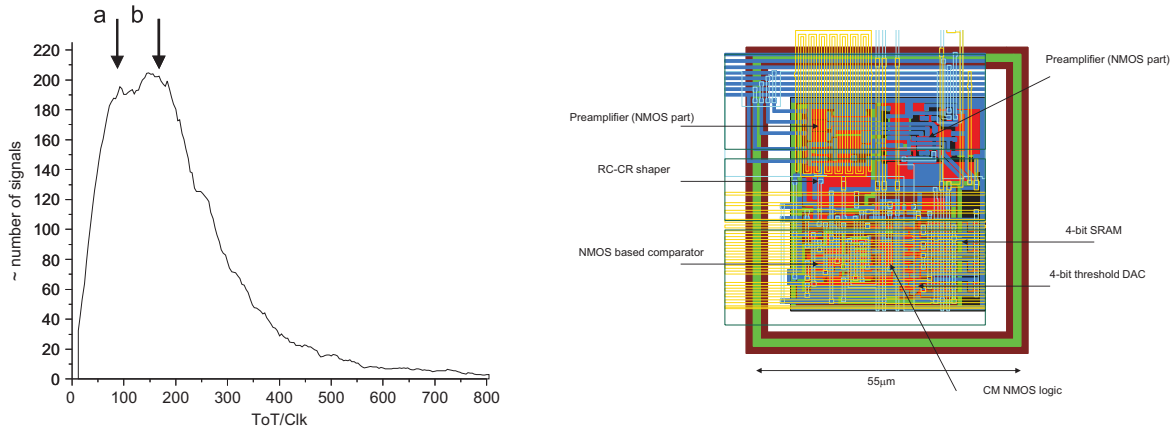


Figure 2.14: (L) β^- spectrum with a single pixel; (R) Pixel chip [19]

The first test detector using SDA (”smart” diode array) was designed in 0.35 μm CMOS technology and has a $55\mu m \times 55\mu m$ area pixel, in-pixel hit detection and binary read out [19] (figure 2.14). Recently, another test detector was developed in 0.18 μm CMOS technology.
Several measurements are performed with β^- spectrum from ^{90}Sr source in order to estimate the collected charge : the collected data are shown in the

graphic on the left of figure 2.14. Here it is possible to observe two maxima (a) e (b): the produced signal charge corresponding to the highest maximum (b) is about 1800 e^-. Up to now three models of the chip have been designed:

1. The PM1 is the simpler amongst them and has both a binary read-out and an in-pixel signal processing.

2. The PM2 has small pixels and its read out architecture is the rolling shutter.

3. the CCPDs (capacitive coupled pixel detectors) are similar to hybrid pixels but they haven't got the conductive bump and are based on the signal transmission chip-to-chip.

All these devices showed a high signal-to-noise-ratio but the chip which has the best performance in terms of signal-to-noise ratio (≈ 70), read out speed and charge collection efficiency, is the PM2 which was developed using the rolling-shutter architecture [19].

2.7 Amplifiers for MAPS

Since the signal to noise ration of a MAPS depends on the capacitance of the collection diode, it is necessary to optimize its geometry.
Actually, in order to enhance signal-to-noise ratio, in-pixel amplifiers can be designed to obtain the best performance in terms of signal processing, power consumption, gain and noise.
To maximize the signal-to-noise we can modify the gain A_v of the amplifier.

In the simple case of the standard common source amplifier (CS) shown in figure 2.16, we obtain by means of the small signal model the voltage gain which depends on the transconductance g_m of M_1 as well as of the diode connected load M_2. Since the source terminal of M_2 is not grounded, its bulk transconductance g_{mb2} must be considered.
The voltage gain of the common source amplifier is given by :

$$A_{vs} = \frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{mb2} + \frac{1}{r_{01}} + \frac{1}{r_{02}}} \tag{2.8}$$

where r_{01} and r_{02} are the resistors connected between drain and source terminals representing the effect of channel modulation.

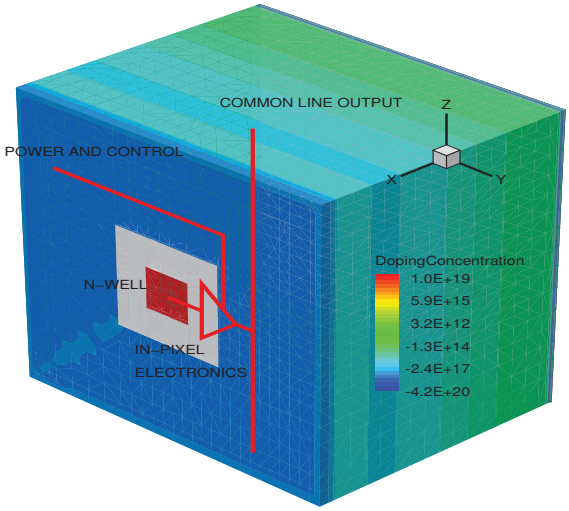


Figure 2.15: Basic MAPS pixel cell, [20]

Generally, A_{vs} is not sufficient to limit the effect of noise after the amplification. Hence, in order to obtain a very high gain we use the improved common source (ICS) (ICS is shown on the right of figure 2.16) in which the transistor M_3 is necessary to bias the load M_2. Therefore, the voltage gain of ICS amplifier is given by:

$$A_{vi} = \frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{mb2} + \frac{1}{r_{01}} + \frac{1}{r_{02}}} \tag{2.9}$$

In this case, the effect of the load transistor transconductance is eliminated for frequencies higher than $g_{m3}/{C_{gs3}}^7$, the AC gain increases of about a factor two whereas DC gain and DC operation points are maintained: in this manner, we can apply a negative feedback to stabilize the operation point of the amplifier, [20].

In order to give a negative feedback to in-pixel improved common source amplifier, we can use a feedback circuit consisting of a transistor M_4, a diode D_2 and a capacitor C_1; the transistor M_5 and capacitor C_2 are added in improved cascode (CAS) amplifier, as shown in figure 2.17. However, in both

[7] C_{gs_3} is the capacitance between gate and source of transistor transistor M_3.

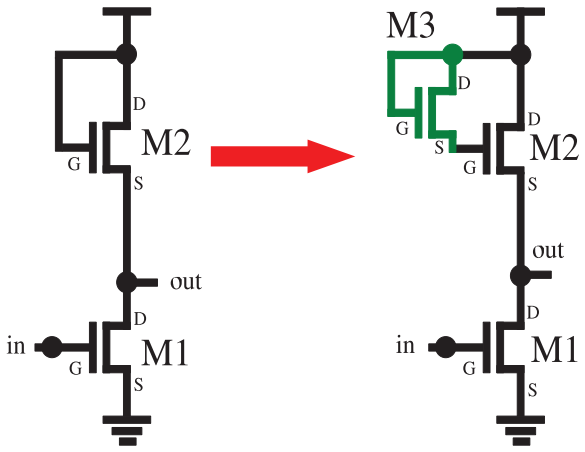


Figure 2.16: Schematics of the amplifiers: (L) Standard Common Source; (R) Improved Common Source. [20]

cases the feedback is a low pass filter with very high time constant C_1/g_{m4} and it provides the bias of the collection diode D_1 via diode D_2. The signal current is converted to a voltage by means of the input parasitic capacitance; the small-signal resistance of the collecting diode is large due to its very small leakage current.

Since time constants of low pass filter and diodes capacitances are very large, unwanted memorization effects of the signal may occur. For this reason each pixel is equipped with a Correlated Double Sampling (CDS) circuit .
In terms of simplicity of the schematic as well as of higher gain, a better alternative approach is to employ negative time variant feedback, in which the DC operational point is fixed by a short pulse to the gate of transistor M_3, as shown in figure 2.18.
The drawback of this layout lies in the cross-talk between the collecting diode D_1 and the switch M_3; however, this effect can be reduced by increasing the size of the diode capacitance or by lowering down the controlling voltage pulse [20].

As mentioned above, each pixel is equipped with a CDS circuit, which is necessary to remove noise effects or unwanted DC offset; the correlated double sampling will be discussed in the next section.

The charge collection efficiency of in-pixel amplifiers above introduced was analyzed by the paper authors using ISE TCAD. The test chip was fabricated in 0.35 μm CMOS technology and it was designed with a 25 μm

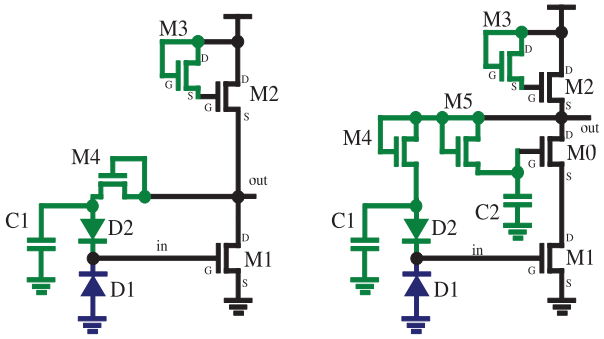


Figure 2.17: Schematics of the amplifiers with negative feedback: (L) Improved Common Source; (R) Improved Cascode. [20]

pitch and a 20 μm thick epitaxial layer. The substrate and the n-well form the collecting diode.
Two different collecting electrode shapes were considered: square shape and L-shape. The geometries of collecting diodes are shown in figure 2.19.
Both shapes of D_1 n-well were designed for the amplifiers with time invariant feedback. For time variant feedback only L-shaped diodes were instead used.

Two different doping levels of the epi-layer were simulated: uniform and gradual doping. Whit gradual doping, the p-doping decreases in the n-well direction as power 10 of the distance; the thickness of epitaxial layer was varied as well.
The experimental results show that charge collection efficiency of a gradually doped device is two times higher than the one of uniform doped device, when we consider the same substrate thickness for both devices. The electron concentration slowly decreases for uniform doping as we can see in figure (figure 2.20).
Furthermore, the chip was also tested with X-Ray produced by ^{55}Fe of 5.9 keV energy. The pixel read-out time is 160 ns, whereas the integration time is 160 μs.
The signal-to-noise-ratio is defined as the most probable value of the signal in the seed pixel divided by its noise. Experimentally, we can observe the highest values of signal-to-noise ratio in improved common source amplifiers (S/N = 19.4) as well as in improved cascode (S/N = 23.3) that has time invariant feedback and a squared n-well. Regarding the devices having L-shaped n-well, instead, the signal-to-noise ratio is lowered down due to the increase of

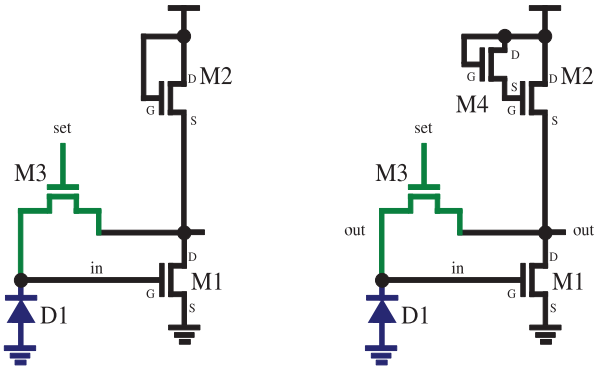


Figure 2.18: Schematics of negative time variant feedback: (L) Standard Common Source; (R) Improved Common Source. [20]

the capacitance. Vice versa, charge collection efficiency of improved common source (16.1%) and improved cascode(13.7%) amplifiers with both squared well and time invariant feedback is very small compared to that of both common source standard (37.5%) and improved (26.7%) amplifiers featuring time variant feedback and L-shaped well[8] [20].

2.8 Correlated Double Sampling

The distinctive feature of monolithic pixels is to allow the integration of both, the sensor and the read out circuit, on the same silicon wafer, in order to permit in-pixel signal processing.
So far, all the analyzed sensors convert the collected charge in a voltage signal and, for this reason, they are represented by a current source I_{PD} with a capacitance in parallel: the energy deposited by the particles traversing the sensor generates hole-electron pairs that are registered as a current signal.
Since the sensitive volume of MAPS is relatively small, the revealed signal is not too high, about some millivolts. Furthermore, it should be observed that this charge signal is affected by several types of noise: the shot noise i_{nd} introduced by the leakage current of the sensor; the reset noise due to the reset transistors which restores detector characteristics after each events.

A MOSFET used as switch is off (switch off) or in triode region (switch on) , so changing its resistance value. However, the resistance R_p of re-

[8]Charge collection efficiency of seed pixel

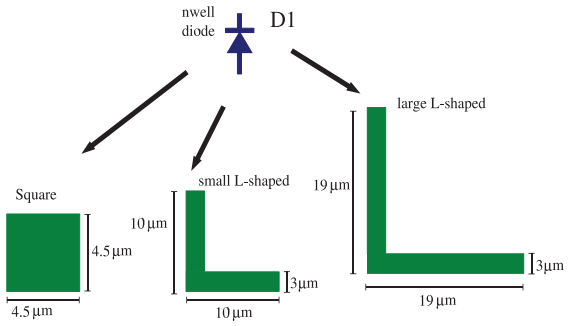


Figure 2.19: Geometries of the collecting diode, [20]

set transistor is connected in parallel with detector capacitance C_D (for CTIA circuit R_p is connected in parallel with feedback capacitance): thus, it generates a noise voltage $v_n^2 = k_B T/C_D$ corresponding to noise charge $Q_n^2 = v_n^2 C_D^2 = k_B T C_D$. To remove or alleviate reset noise effects, especially when time-variant feedback amplifiers are used, we apply CDS technique: each pixel is equipped with a sampler circuit positioned after the preamplifier, at the input of the pulse shaper.
The CDS circuit (fig. 2.21) consists of two switches, S_1 and S_2, that are switched off for noise sampling or switched on when the overall collected signal has to be sampled; the capacitances on the inverting and non-inverting shaper inputs, instead, are employed to store the sampled signals.
On the right of the figure 2.21 we can follow time evolution of the CDS process. All signals are affected by the noise, represented as an oscillating baseline. The switch S_1 is rapidly closed and then open, so that the voltage on the node V_1 rises up to the noise voltage v_n; afterwards, S_2 is quickly switched so that the node V_2 is at the voltage level $v_s + v_n$. It should be noted that the voltages at the nodes V_1 and V_2 must be constant during the sampling time T.
V_1 and V_2 are respectively to the inverting and non-inverting input of the shaper; thence, the shaper will give in output the difference $V_o = v_s$ between the two inputs, removing in that way the noise baseline [3].

Although the CDS gets rid of most noise affecting the signals, it introduces another noise component in the overall system.
For the sake of simplicity, in order to analyze the noise in the circuit that we are focusing on, we can refer to the time domain by introducing the *weighting*

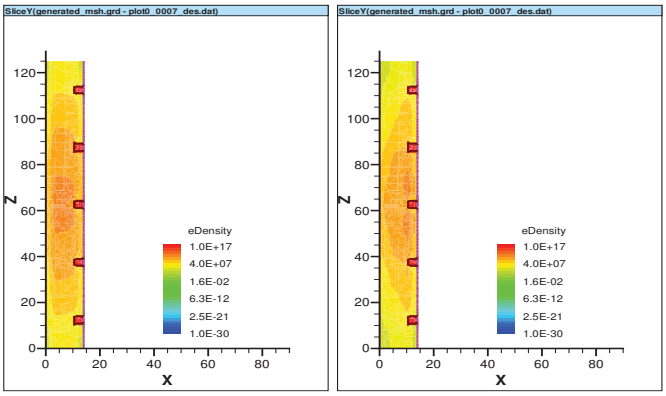


Figure 2.20: Electron concentration for uniform (L) and graded (R) p-epilayers, [20].

function W(t) of a shaper. W(t) describes the individual noise contributions at time t. The noise characteristics of the shaper is given by the time integral of $[W(t)]^2$, named as *noise index*; it is defined by:

$$N_n = \int_{-\infty}^{\infty} [W(t)]^2 dt \tag{2.10}$$

In the case examined here, W(t) is the convolution of the signal sampled by means of CDS with RC prefilter response, in the time interval T. The signal produced in a pixel is first sent through a RC prefilter before being processed by the CDS circuit. The response of the RC low-pass filter is a voltage signal proportional to $(1-e^{-t/\tau})$, where $\tau = RC$ is the characteristic time constant of the filter. We assume that the time interval T is large compared to the time in which the amplitude of a signal is sampled,so the sample pulse in the sensor can be represented as a δ function. The previous function is integrated by the preamplifier and converted in the step function in input of the low-pass filter. Therefore W(t) is:

$$\begin{aligned} t < 0 \qquad & \mathrm{W(t)} = 0; \\ 0 \leq t \leq T \quad & W(t) = (1 - e^{-t/\tau}); \\ t \geq T \qquad & W(t) = (1 - e^{-t/\tau}) - (1 - e^{-(t-T)/\tau}) = e^{-t/T}(e^{T/\tau} - 1); \end{aligned}$$

The equivalent noise charge (ENC) Q_n^2 is given by the sum:

$$Q_n^2 = Q_{ni}^2 + Q_{nv}^2 \tag{2.11}$$

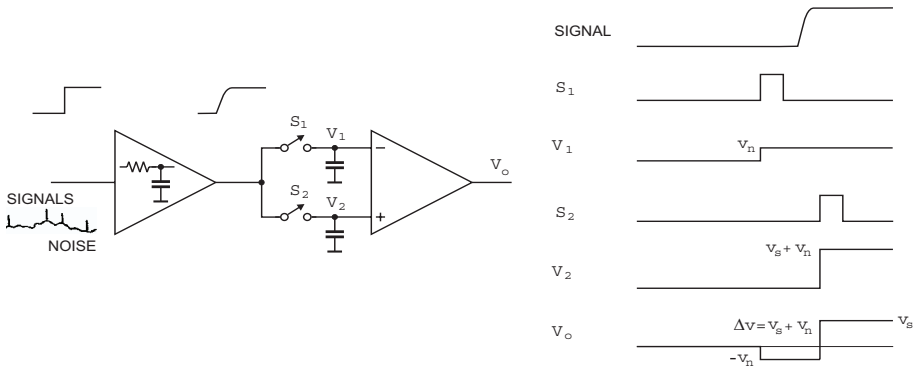


Figure 2.21: Principle of Correlated Double Sampling - time evolution[3]

Q_{ni} is the noise current contribution whereas Q_{nv} is the voltage noise contribution: since we know the weighting function of the system, we can express both contributions. W note that Q_{ni} and Q_{nv} are considered uncorrelated noise sources.
The noise current source (shot noise) gives us the contribution:

$$Q_{ni}^2 = \frac{1}{2} i_n^2 N_{ni} = \frac{1}{2} i_n^2 \int_{-\infty}^{\infty} [W(t)]dt = \frac{1}{2} i_n^2 \Big[\int_0^T (1 - e^{-t/\tau})^2 dt + \int_T^{\infty} e^{-}2t/\tau (e^{T/\tau} - 1)^2 dt \Big] \quad (2.12)$$

and by the integration we obtain

$$Q_{ni}^2 = \frac{1}{2} i_n^2 (T - \tau(1 - e^{-T/\tau})) \quad (2.13)$$

The noise voltage, instead, is given by:

$$Q_{nv}^2 = \frac{1}{2} C^2 e_n^2 N_n v = \frac{1}{2} C^2 e_n^2 \int_{-\infty}^{\infty} [W'(t)]^2 dt \quad (2.14)$$

Regarding Q_{nv}^2 we can consider the first derivative of W(t) since the noise thermal voltage has a white frequency spectrum, i.e. its spectrum does not

depend on the frequency, so in the time domain is represented by the δ function. Since the δ is infinitesimally short, it can be treated as two infinitesimally spaced step pulses of opposite signs, so that the voltage noise is the derivative of the step function [3].
By the above expression of W(t), we obtain:

$$\begin{aligned} &t < 0 && W'(t) = 0; \\ &0 \leq t \leq T && W'(t) = \tfrac{1}{\tau} e^{-t/\tau}; \\ &t \geq T && W'(t) = \tfrac{1}{\tau} e^{-t/\tau}(1 - e^{T/\tau}); \end{aligned}$$

Then, the equivalent noise charge generated by the voltage noise is given by:

$$Q_{nv}^2 = \frac{1}{2} C^2 e_n \Big[\int_0^T (\frac{1}{\tau} e^{-t/\tau})^2 dt + \int_T^\infty \Big(\frac{1}{\tau} e^{-t/\tau}(1 - e^{T/\tau}) \Big)^2 \Big] \quad (2.15)$$

and, by the integration

$$Q_{nv}^2 = \frac{1}{2} C^2 e_n \frac{1}{\tau} (1 - e^{-T/\tau}). \quad (2.16)$$

In order to determine the equivalent noise charge, the noise have to normalized by the signal. The amplitude of the low-pass filter output is $(1 - e^{-t/\tau})$ but, following the sampling time of CDS, it becomes $(1 - e^{-T/\tau})$. Accordingly, Q_{ni}^2 and Q_{nv}^2 are given by:

$$Q_{ni}^2 = \frac{1}{2} i_n^2 \frac{1}{(1 - e^{-T/\tau})} \Big(\frac{T/\tau}{(1 - e^{-T/\tau})} - 1 \Big) \quad (2.17)$$

$$Q_{nv}^2 = \frac{1}{2\tau} C^2 e_n^2 \frac{1}{(1 - e^{-T/\tau})}. \quad (2.18)$$

By setting T = 0 the two noise contributions vanish; instead, for $T/\tau \gg 1$ we note that:

- $Q_{ni}^2 \approx \frac{1}{2} i_n^2 T$, i.e. this noise contribution raises due to the increasing value of the sampling time. If we consider only the shot noise, the noise current spectral density is $i_n^2 = 2eI$, where e is the electron charge and I represents the current noise in the sensor; the equivalent noise charge, expressed in electron units (ENC), is given by $Q_{ni} = eIT/e^2 = IT/e$. Since the ratio between the current I and the charge e is proportional to the numbers of collected electrons in the time interval, then $Q_{ni} \propto \sqrt{N}$;

- $Q_{nv}^2 = \frac{1}{2\tau} C^2 e_n^2$, i.e. it is two times the RC filter noise. If the sampling time varies, Q_{nv}^2 does not change.

Finally, the total equivalent noise charge is:

$$Q_n^2 = Q_{ni}^2 + Q_{nv}^2 = \frac{1}{2} \frac{1}{(1 - e^{-T/\tau})} \left(i_n^2 \tau \left(\frac{T/\tau}{1 - e^{-T/\tau}} - 1 \right) + \frac{C^2 e_n^2}{\tau} \right) \quad (2.19)$$

The noise charge depends on the RC filter time constant τ as well as on the normalized sampling time T e τ. Minimum noise varies for any given values of T/τ; it is obtained when the current and voltage noise are equal. By doing so, the optimum RC filter time constant τ_{opt} is determined.
The two graphics below show the behaviour of the equivalent noise charge vs the sampling time when the optimum filter constant time varies. In this case, the total input capacitance is 30 pF, the detector current is 10 nA and the amplifier has an equivalent input noise ofi 2.5 nV/$\sqrt{Hz}$ [3]:

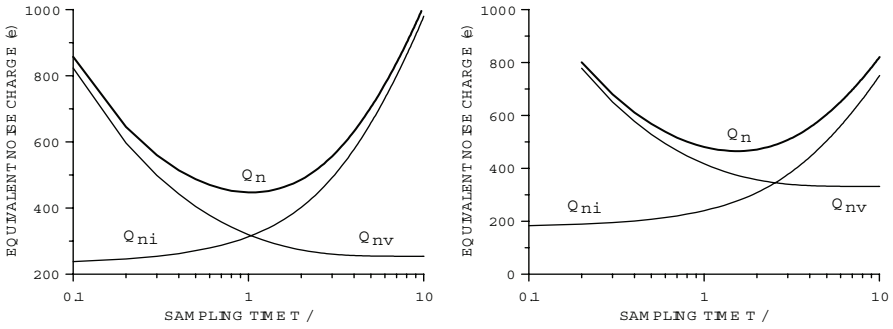


Figure 2.22: $Q_n(T)$ for two different values of τ_{opt}: (L) $\tau_{opt} = 1.7\mu s$; (R) $\tau_{opt} = 1.0\mu s$ [3].

2.9 Data Transmission

After amplification, we need to format the stored data and transmit them out of the chip. As we have noted in Chapter 1, when a ionizing particle hits

the sensor, it activates some pixels forming a cluster because of the diffusion of the generated charge cloud. However, if the signal value registered by the cluster is below a certain threshold or if only a single pixel fires, then this information may be discarded since it is not relevant to analyze the collision events (zero suppression technique). The data should be transmitted in digital form using a differential transmission protocol. This minimizes the sensitivity to external interferences and allows to keep the ground loop under control. This point can be understood with the help of figure 2.23 which compares a single ended and differential transmission schemes. The single

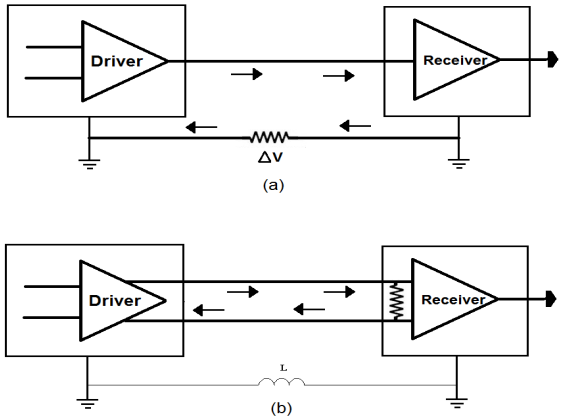


Figure 2.23: Comparison between single ended (a) and differential (b) data transmission

ended circuits requires a common ground return from the receiver back to the transmitter. Due to the impedance of the connections a voltage drop ΔV between the driver and the receiver grounds is developed and it is superimposed to the signal as an additional component.
Furthermore, this requires a strong connection between the receiver ground (usually located on a noisy digital chip) and the transmitter ground located on a sensitive mixed-mode ASIC. Therefore, the ground of the sensor chip can be contaminated by the switching noise of the digital ground. The current between transmitter and receiver flows in large loops whose area is not controlled, increasing the susceptibility to electromagnetic interference. By using a differential transmission scheme ground loop effect is minimized since the current is forced to follow a well defined path. The receiver senses only the difference between its inputs and rejects the common mode components. As a consequence the link between the analog and the digital ground of the system can be weaker. This is represented in figure 2.23 with an inductance connected between the two grounds. In this way the grounds are kept at the

same DC voltage, while the propagation of high frequency disturbances from the digital to the analog ground is reduced.
Indeed, the drivers which are used in current steering mode ensure that in both transmission lines the instantaneous current levels are equal but of opposite sign. The most common standard for differential digital data transmission is the Low Voltage Differential Signaling (or LVDS) that will be the topic of the rest of this thesis.

Chapter 3

The LVDS Transmission System

The quadruple well process in 0.18 μm CMOS has been chosen as baseline for the R&D of the ALICE upgrade. A cooperative effort between several institutions, among which there are CERN, IN2P3 and INFN, is underway to assess the performance of the technology with respect to the ALICE needs. In this context several test structures have been already produced and others are under design. Among the test structures already fabricated there are simple transistors to investigate the radiation hardness of the technology and matrices of pixels with simple rolling shutter readout.

In a detector readout systems there are functional blocks which are commonly used. Such blocks include Phase Lock Loop (PLL), Analog to Digital Converters (ADC), Digital to Analog Converters (DAC), digital output drivers and receivers. These blocks are often provided by the foundries as commercial IPs. Unfortunately, sometimes commercial IPs do not meet the requirements of a particle detectors because of the radiation hardness is not adequate and the power consumption is too high. For example, many I/O structures or voltage regulators employ transistors that can sustain a 3.3V voltage supply. However, these transistors have a thicker gate oxide and they are more prone to suffer from radiation damage. In addition, commercial IPs have high cost and in general a fee must be payed every time a given block is used in a design. This can increase significantly the R&D cost of a new chip. In fact, several submission can be necessary before the optimal performance of the ASIC are finally reached and each time a submission is made it might be necessary to pay for the used IPs . The above considerations motivate the development of custom components, even though they are in principle already available from the silicon foundry.

In this work, we focus the attention on the development of a LVDS (Low Voltage Differential Signaling) transmission system. This choice was motivated by the fact that a high speed differential link is of primary importance for any mixed mode circuit, such as complex front-end for radiation sensors usually are.

The first part of Chapter 3 describes the LVDS differential transmission concept.
A LVDS system consists of differential driver and receiver and allow to transmit digital signal at very high data rate, from 500 Mbit/s up to 2 Gbit/s, whilst the power consumption is very low.
A common metric to evaluate the quality of a transmission signal is the eye diagram, i.e. a signal pattern which is obtained by superimposing on the same time interval the sent bits. In the second part of this chapter, we describe the concept of eye diagram and the informations which can be extracted out of it. In particular, the effect of the *time jitter* is very interesting, i.e. the deviation of ideal position in time of a noisy signal. Since we must distinguish always two different transmitted bits, we need to reduce the timing jitter as well as the amplitude noise because together can determine an error on the detected logic level.

3.1 LVDS Specifications

The standard ANSI/TIA/EIA-644 specifies the electrical characteristics of the LVDS system.
The LVDS interface is the most popular differential system in transmission of digital signal at high speed and it is widely employed in commercial applications. A LVDS system consists of a fully differential driver and a receiver with differential inputs.
Differential transmission has several advantage compared to single ended scheme since a differential receiver is less susceptible to the common mode noise as well as to the problem caused by ground loops and cross talk. Indeed, when we design the driver and the receiver we connect them at the same ground; however, sometimes a difference in the ground reference can occur which causes variations of common mode voltage. Since the receiver performs the difference between its inputs, all common mode components are removed to advantage of signal-to-noise-ratio.
The driver and the receiver are connected by means of a transmission lines which have a characteristic impedance $Z_0 = \sqrt{L/C}$, where L and C respectively represent inductance and capacitance per unit length of the lines; typically, $Z_0 \approx 50\Omega$.

The impedance mismatches causes the reflection of the signal transmitted by the driver. So, in order to avoid this effect, we place a termination resistance $R_{Term} \approx 100\Omega$ at the input of the receiver. Furthermore, since the receiver has a high input impedance, the signal current at the driver output flows trough the termination resistors defining an output voltage swing.

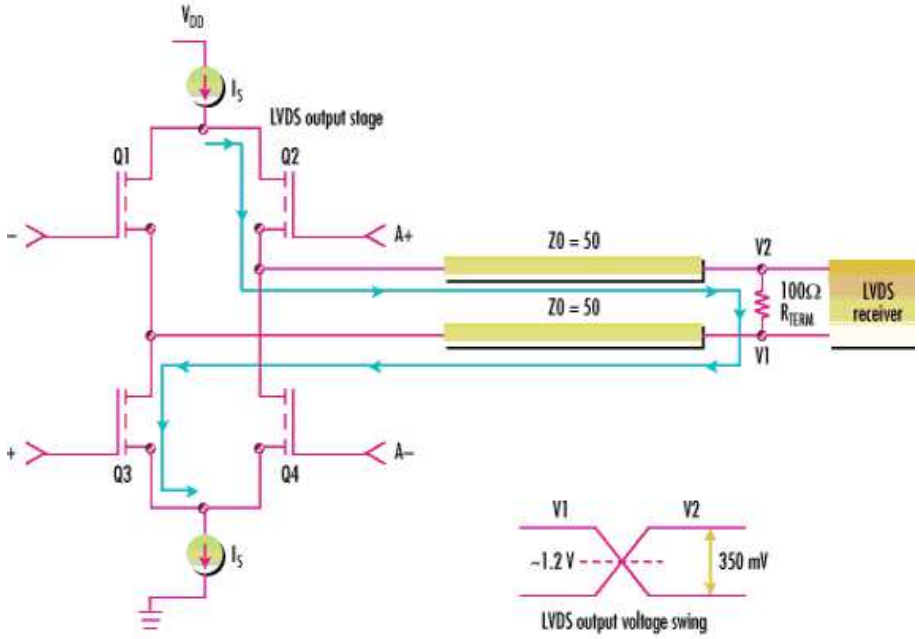


Figure 3.1: LVDS transmission system

The LVDS standard determines the features of the digital signal at the driver output[21]:

- Differential Signal;
- Voltage Swing;
- Max Transmission Rate;
- Minimum Power Dissipation.

The output voltage swing is the variation of the voltage between the driver output terminals; it is considered "low" when it is below 500 mV; typical values of the transmission rate are from 500 Mbit/s up to 2 Gbit/s [21].

In figure 3.1 a standard LVDS system is shown, where the characteristic value of the supply voltage is $V_{DD} = 2.5V$ and the current I_S, flowing in the driver, ranges from 2mA to 4 mA. The voltage swing V_{VS} is given by:

$$V_{VS} = I_S R_{Term}. \tag{3.1}$$

Therefore, the voltage drop across the termination resistor terminals ranges from 200 to 400 mV.

The driver is fully differential, it has an output common mode voltage V_{cm} which is about half of the voltage supply V_{DD}. The LVDS standard, the optimum value of the driver common mode voltage is centered $\approx 1.2V$.
The receiver is differential too, therefore its input common mode voltage range has to be matched with the output common mode voltage range of the driver.

3.1.1 LVDS Driver

A LVDS driver can be designed as four switches and two current sources which are switched on and off in order to allow the current to flow in one direction or the other.

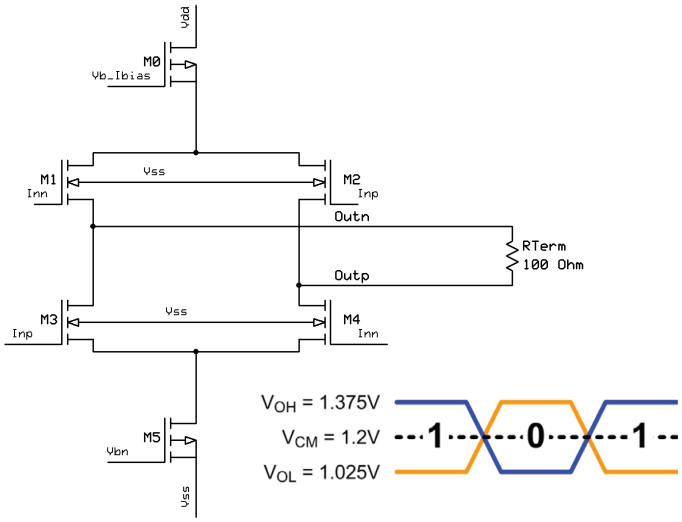


Figure 3.2: LVDS Driver - M1, M2, M3 and M4 are transistors utilized as switches; V_{OH} and V_{OL} are logic levels with a 3.5 mA constant current.

As we can observe in figure 3.2, the switches are implemented by four MOS transistors controlled by the input voltage. The switches are closed if

the MOS transistors work in triode region, i.e. if they exhibit a low resistance between drain and source and therefore the current can flow in the circuit. Vice versa, switches are open if MOS transistors are in the cut-off region, that is if the resistance between drain and source terminals is ideally infinite, thereby blocking the current flow.
The input signals at the gates of M1 and M2 are phase shifted by 180° so when M1 is switch on then M2 is switch off. Moreover, M1 is associated with M4 as well as M2 is paired up with M3: these switch pairs are simultaneously open and closed in order to reroute the current in the two directions. In this sense a LVDS driver works by steering a DC current source (current-mode control).
Let's suppose that M1-M4 are closed and M2-M3 are open: I_S flows in one of the two transmission line it continues trough the termination resistor and returns by traversing the second transmission line; then, it enters in the driver passing trough M4. The situation is specular if the closed switches are M2 e M3.
At the driver outputs we measure the voltage drop across the ends of R_{Term} as a function of the time, obtaining two logic levels named "High" (logic 1) and "Low" (logic 0). They respectively correspond to V_{OH} and V_{OL} in figure 3.2. These voltage levels depend on the common mode voltage and on the current I_S which determines the output voltage swing; hence we obtain:

- $V_{OH} = V_{cm} + \frac{1}{2}V_{VS}$ corresponding to the high logic level ;
- $V_{OL} = V_{cm} - \frac{1}{2}V_{VS}$ corresponding to low .

3.1.2 LVDS Receiver

The LVDS receiver has two differential inputs and a single ended output. It acts as a comparator since it is sensitive to the voltage difference across its inputs and returns a logic 1 or a logic 0 depending on the sign of this difference. We note that most receiver designs are based on hysteresis circuit in order to avoid the possibility of oscillation at the output. Sometimes, indeed, the output receiver oscillations arise when the driver outputs are not well defined, like during signal transition [21].

3.2 Performance Qualification

Since each signal suffers from noise, we perform qualitative and quantitative analysis of a transmitted digital signal. In order to do this, the *eye diagram* is a standard tool since it allow us to evaluate and, eventually, to solve the

problems connected with information transmission.
An ideal eye diagram should be nearly square; however, several effects, as the timing jitter, the amplitude noise the attenuation and the dispersion of the signal modify its characteristic form (Fig. 3.3).

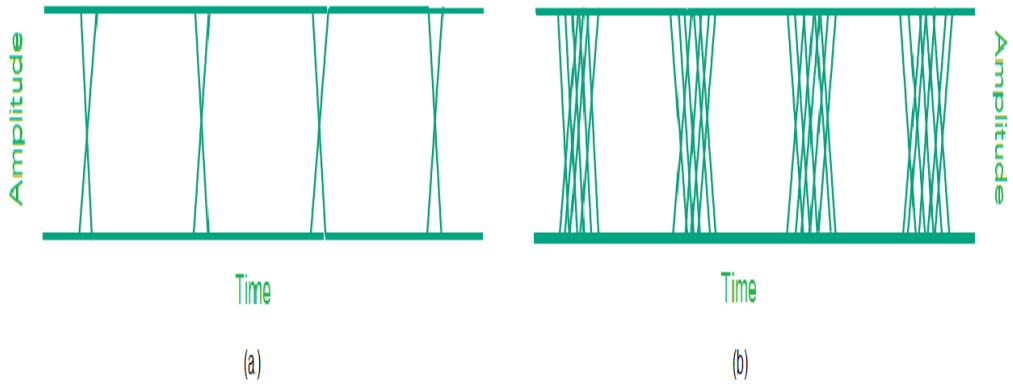


Figure 3.3: Eye Diagram Example: (a) Ideal eye diagram; (b) Jitter.

3.2.1 Eye Diagram

The eye diagram is obtained when a signal is repetitively sampled in time and the samples are overlapped in the same time interval[1], as shown in figure 3.4. In order to crate the eye diagram, all possible sequence of binary symbols are generated so that we can display the overall transmission in a compact representation.
By overlapping the samples we obtain the envelops having the typical eye-shape, as shown in figure 3.3, which allow us to inspect the overall transmitted pattern.
Depending on the features of the designed circuit and on the quality of the transmission line, the eye can be more or less open. The eye aperture is the most important parameter that we can use in order to analyze the quality of the signal transmission since it corresponds to the maximum distance between the logic levels 0 and 1. Indeed, a system employ a determined time interval in order to transmit a logic level. Since we need always to distinguish

[1]This time interval is the pulse period of the transmitted signal

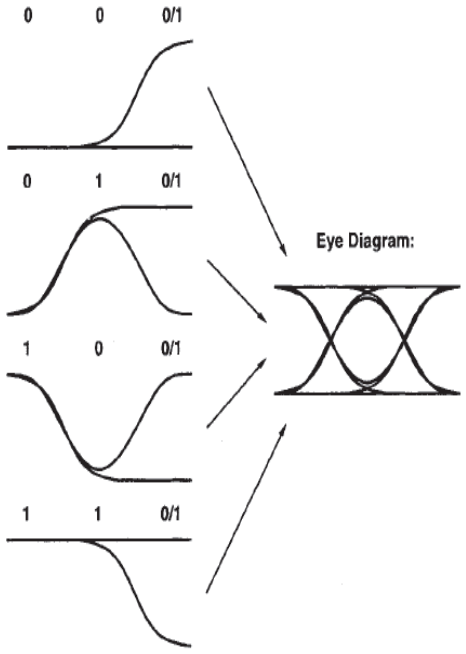


Figure 3.4: Generation of an eye diagram [22]

between a "High" or a "Low" (respectively logic "1" or "0"), the wider is the eye opening, the easier the distinction is and it is less influenced by the noise.

In figure 3.5 we show a description of the eye diagram:"0" and "1" are the value of the two logic levels; the rise time is the time interval required by the signal to make a transition from 10% to 90% of its final value; the fall time is the time interval from 90% to 10% of the final signal value. The eye width and the eye height, indeed, give us a measure of the eye aperture. At the intersection between the rising and the falling edges of the signal we can measure the deterministic timing jitter.

3.2.2 Timing Jitter

The *Jitter* is defined as the short term variation of significant instants of a digital signal from their ideal positions in time [23]. Hence, timing jitter is the instant error of the signal transition from a logic level to another.
The total jitter of a system consists of two components:

$$T_j = D_{jPP} + n \times R_{rmsj} \tag{3.2}$$

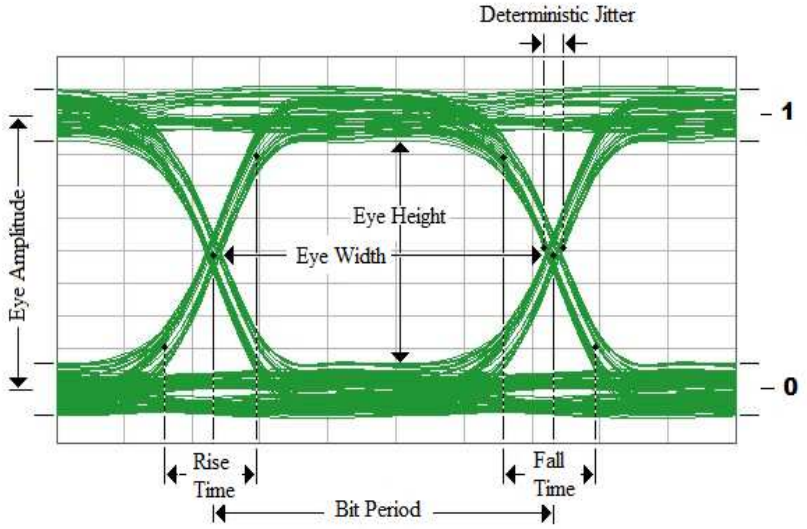


Figure 3.5: Description of the eye diagram

- D_{jPP}: the peak-to-peak deterministic jitter is due to specific problems of the examined system, as the electromagnetic interference, the inter-symbol interference (ISI), crosstalk, etc. Sometimes it can be reduced by taking precautions when we design a circuit.

- R_{rmsj}: the random jitter varies randomly and it is impossible to eliminate. It is the most important component of the total jitter and it is generated by several causes: thermal noise, shot noise, etc... Generally, we assume that R_j follows a Gaussian distribution characterized by the width σ and the mean value μ. This Gaussian distribution describes the probability that the eye edges cross the sampling point which is situated in the center of the eye. σ represent the contribution of the random jitter to the total rms jitter, i.e. $R_{j_{rms}} = \sigma$.
  In absence of deterministic jitter, R_j determines the time position of the eye edges[24]. It can be reduced by decreasing the transition time.

- n is a factor determined by the bit error rate (or BER) required of the link.

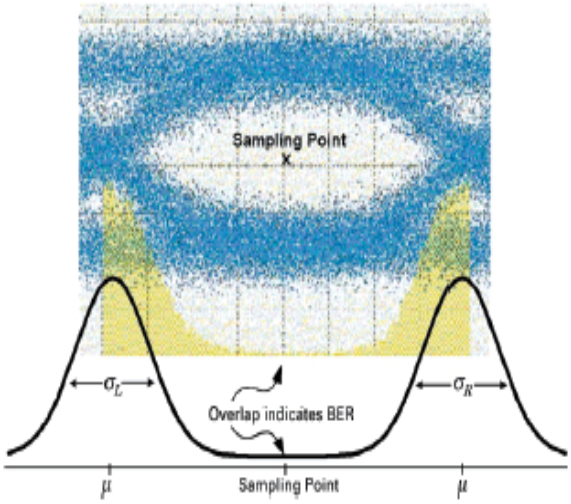


Figure 3.6: Effect of the random jitter. The mean value μ of both Gaussian distributions is the same whilst σ_L can be different compared to σ_R .

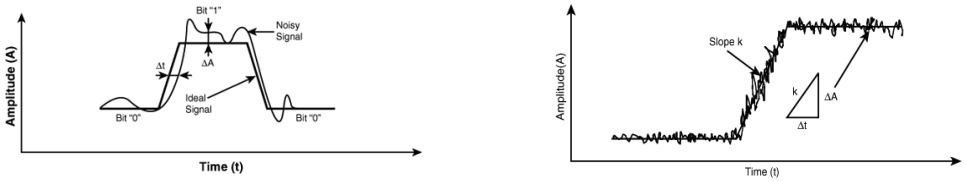


Figure 3.7: (L): Ideal and noisy digital signal; (R): Determination of timing jitter. [23]

The noise and the jitter affect the bit transmission because they move along the t-axis the eye edges whilst the amplitude varies only along the voltage axes.
More generally, let's indicate with A the amplitude of a generic physical quantity and suppose that it is a function of the time. Assuming that A_0 is the waveform amplitude and is the noise amplitude, we can describe the total waveform as: $A(t) = A_0 + \Delta A(t)$. The noise amplitude sometimes moves up the actual signal whilst sometimes moves it down: in this manner, $\Delta A(t)$ affects the crossing of the ideal signal by the actual signal (Fig.3.7) determining an error in crossing time. The timing jitter corresponding to ΔA

can be calculated by using the linear small-signal perturbation theory[23]:

$$\Delta t = \frac{\Delta A}{\frac{dA_0}{dt}} \tag{3.3}$$

In the equation 3.3, $\frac{dA_0}{dt}$ is the slope or the slew rate of the waveform: hence, we can infer that in order to minimize the timing jitter effects we need to optimize a system in order to have very fast rise time as well as fall time: indeed, the higher the slope the less is the timing jitter [23].

Chapter 4

Design of a Custom LVDS Interface in 0.18 μm CMOS

The LVDS standard has been chosen for the ITS upgrade because it is the most widely employed transmission technique for deep submicron technologies.
Usually, the LVDS transceiver is used when the supply voltage ranges between 2.5V and 3.3V. However, to reduce the material budget as well as minimize the power consumption of the ITS detectors, we have implemented two driver schemes in 0.18 μm CMOS technology fed with 1.8 V supply voltage. This value of the supply voltage will be used to power the front-end chip in order to minimize the power consumption.

This chapter gives a description of the two drivers and the receiver designed. The first driver (Transmitter 1) is based on the one already implemented in several applications at CERN; the second (Transmitter 2) is a slew controlled LVDS output driver circuit based on [25]. Both drivers are designed in the 0.18 μm Q-well CMOS technology provided by the foundry TowerJazz, in order to satisfy the requirements of ITS upgrade.
Also the receiver circuit is well know and already employed in several CERN applications. It allows us to obtain a high gain and a suitable voltage swing even if the power supply voltage is reduced. Also this circuit was designed in 0.18 μm Qwell CMOS technology.

4.1 Transmitter 1

In figure 4.1 we show the schematic of the Transmitter 1. It consists of the replica bias circuit plus the actual driver. As mentioned above, this circuit

has been modified in order to use the 0.18 μm CMOS technology and 1.8 V supply voltage. The adaptation process is based on the variation of both the gate length L and the gate width W of a MOSFET, hence it is a geometrical process.
The supply voltages of the system are $V_{DD} = 1.8V$ and $V_{SS} = 0V$; the current I_6, flowing in the driver, ranges from 2 mA to 4 mA in order to obtain a driver voltage swing V_{VS} between 200 mV and 400 mV.

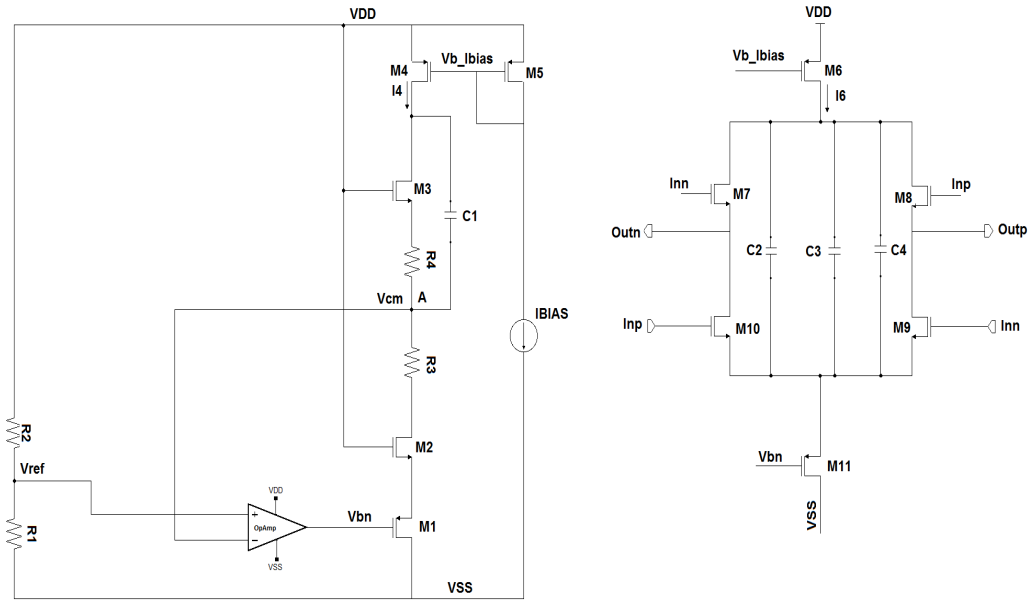


Figure 4.1: Transmitter 1 schematic. (L) The replica bias circuit defines the common mode voltage. (R) The driver consists of four NMOS transistors used as switches. The supply voltages of the overall circuit are V_{DD}=1.8 V and V_{SS}=0 V.

The replica bias circuit is formed by:

- An operational amplifier (OpAmp).
- A resistor divider consisting of $R1$ and R_2 ($R_1 = R_2 = 50k\Omega$).
- The transistors M1, M2, M3, M4 that form the "replica branch" together with the two resistor R_3 and R_4
- Two resistors $R_3 = R_4 = 600\Omega$.
- The current source I_{bias} that controls the voltage level Vb_Ibias of the active current mirror M4-M5.

Then OpAmp (fig.4.2) is used as a comparator between its inputs, i. e. between the voltage in the node A and V_{ref}. The replica bias circuit generates a local feedback that senses voltage on the node A and provides the proper bias voltages to the transistors of replica branch, whereas V_{ref} is fixed by the resister divider at the value of 900 mV. In addition, this local feedback does not affect the driver's transistors nor it suffers from the effects of the driver's faults.

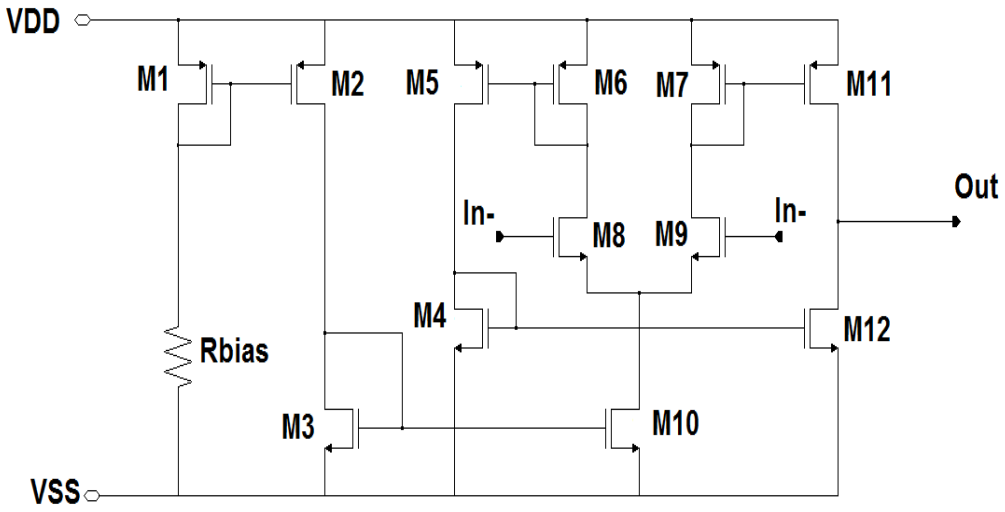


Figure 4.2: OpAmp schematic. The supply voltages of the overall circuit are V_{DD}=1.8 V and V_{SS}=0 V.

In the replica branch, $R_3 = R_4$, transistors M1-M4 and M2-M3 have the same size and this part of the circuit is symmetrical respect to the node A. We note that transistors in this part of the replica bias circuit work in the same way as in the driver. In fact, M2 and M3 are the replica of each switch pairs as well as the two resistors R3 and R4 are the replica of the termination resistors placed at the receiver input; finally, M4 and M1 correspond respectively to M6 and M11.

Transistors M4 and M6 form with M5 a current mirror and are used to drive the current within the whole circuit, so that they have to work in saturation region. However, it must be noted that the current I_4 in the replica bias circuit is lower than the current I_6 flowing in the driver. In particular, the relation between the two currents is based on the ratio between the

Table 4.1: Gate Length and gate width of the transistors in Transmitter 1

Component	L (μm)	W(μm)	Component	L (μm)	W(μm)
M1	0.3	82.14	M7	0.18	667
M2	0.18	57.8	M8	0.18	667
M3	0.18	57.8	M9	0.18	667
M4	0.3	82.14	M10	0.18	667
M5	0.3	27.38	M11	0.3	986
M6	0.3	986			

resistor R3 (or R4) and one of the termination resistors $R_T = 50\Omega$:

$$\frac{R3}{R_T} = \frac{600\Omega}{50\Omega} = 12 \tag{4.1}$$

Therefore, the current source I_{bias} will give a current which is twelve times smaller than the one in the driver, because it controls the current in the replica bias circuit.
The currents I_4 and I_6 are related by the ratio between the dimensions (gate length L and gate width W) of M4 and M6. Neglecting the mismatches between the two transistors, we obtain:

$$\frac{I_4}{I_6} = \frac{W_4}{W_6}\frac{L_6}{L_4} = 12 \tag{4.2}$$

The same is true for M1 and M11 which respectively give the proper bias currents in the replica bias circuit and in the driver:

$$\frac{I_1}{I_{11}} = \frac{W_1}{W_{11}}\frac{L_{11}}{L_1} = 12 \tag{4.3}$$

The transistors used as current source are p-type, while the transistors used as switches are n-type. As usual, the gate lengths of the switches have been kept to the minimum; on the other hand, the gate width of the current mirrors have been determined according to the ratio 4.2.

In the original design of Transmitter 1, zero threshold NMOS transistors (zero V_t transistors) were used in order to minimize the propagation delay of the signal. In our case, this was not possible because in the TowerJazz technology the low V_t are not available. This implies that large parasitic capacitances are introduced in the circuit because of the large gate width,

about 700 μm required to compensate for the higher threshold. Furthermore, due to the size of NMOS transistors, the common mode voltage V_{cm} have been fixed at 900 mV, lower than the standard value of 1.2 V (Chapter 3). Indeed, with 1.8 V voltage and a V_{cm}=1.2 V not all transistors would have a suitable biasing point.

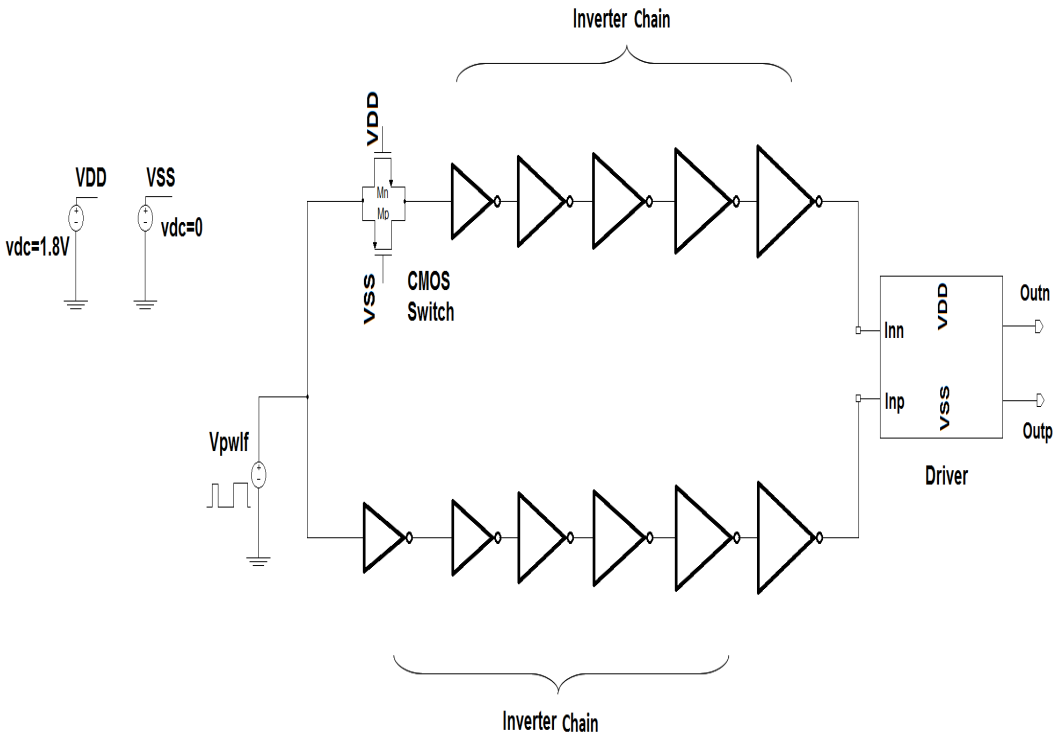


Figure 4.3: Block Diagram of the driver and the inverters chains.

The driver inputs Inp and Inn receive two signals of opposite phase; to do this, two inverter chains were implemented (fig. 4.3) in order to perform the single ended to differential conversion.
The long chain of the inverters is due to the large load capacitances introduced by the NMOS ($C_p \approx C_{ox}WL$): the signal delay, encountered in driving this loads directly from a minimum-size inverter, would be in fact unacceptable.

In order to reduce the time delay of the signal, the size of MOS transistors were determined in the following way.
Let's consider the simple case with only two inverters, shown in figure 4.4,

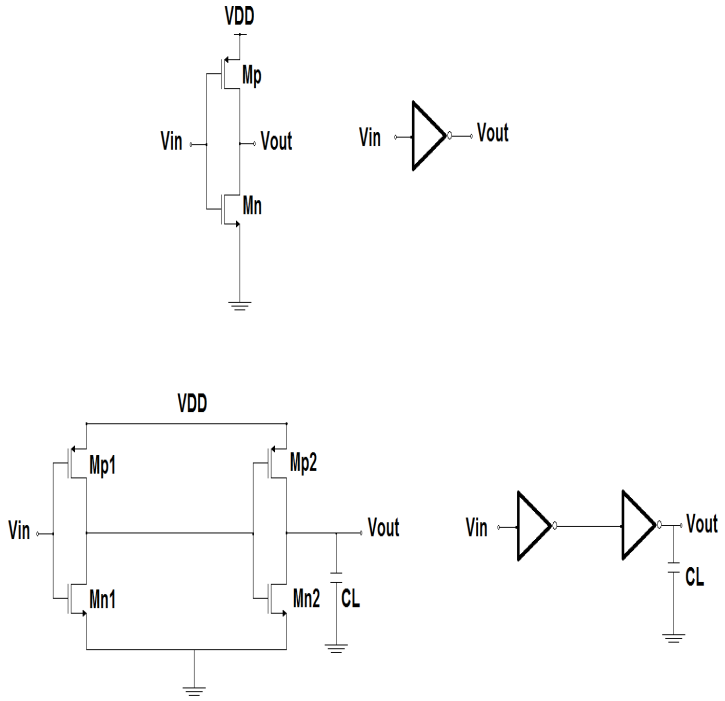


Figure 4.4: Example of inverter cascade

each sized by 2:1 sizing rule[1]. If the capacitive load is C_L and the input capacitance of the reference inverter (formed by $M_{n1} - M_{p1}$) is C_G, the value of C_G is given by the ratio:

$$C_L = \alpha^n C_G \tag{4.4}$$

where $\alpha \approx 3$ and n is the number of the inverters in the cascade [26].
Since the gate length of the NMOS in all inverters was kept to a minimum value of $L_{Mn} = 0.18\mu m$, the gate width of these transistors was calculated by the rule (4.4).
Since the two inverter chains in figure 4.3 do not have the same number of elements, an always-on CMOS switch was introduced to obtain the same propagation delay of the signals at the inputs of the driver. The length and the width of the transistors, forming the CMOS switch, are the same of those devices corresponding to the first inverter of the second cascade. In order to ensure that the rise and fall times of the input signals in Inp and Inn are equal, it should be emphasized that the sizing of the inverters as well as the

[1] $W_{Mp} = 2W_{Mn}$ meanwhile $L_{Mp} = L_{Mn}$

CMOS switch is fundamental. The same is true for the fall time.
After detailed simulations, it turned out that Transmitter 1 is not adequate for the following reasons:

1. the long inverter cascades at the driver inputs have too high power consumption;

2. the driver outputs suffers from both the voltage spikes and the signal reflections, thus limiting the quality of the signal transmission;

3. the output common mode of the Transmitter 1 is lower than the standard value of the input receiver. Consequently, we need some additional blocks in order to adapt this driver to the standard receiver input.

4.2 Transmitter 2

We designed an alternative driver circuit because of the limitations encountered with the previous system.
Transmitter 2 is based on the schematic proposed in [25] which is a slew rate controlled LVDS output driver circuit already designed in 0.18 μm CMOS technology.

The supply voltages are $V_{DD} = 1.8V$ and $V_{SS} = 0$; regarding the common mode output voltage, it is fixed to the value of $V_{cm} = 1.1V$.
As shown in figure 4.5, Transmitter 2 is very compact compared to Transmitter 1, as shown in figure 4.5. Furthermore, two additional differences must be noted:

1. The common mode output voltage is controlled by a common mode feedback loop.

2. A further non-linear differential pair of MOS current switches, named G_{m2}, is introduced. This is substantially a cross coupled transconductor[2].

In Transmitter 2, the common mode feedback circuit (CMFB) takes the place of the replica bias circuit. In fact, when fully differential system are designed, it is customary to add a CMFB in order to determine the common mode output voltage level. The common mode feedback circuit generates a feedback loop which fixes the common mode voltage by adjusting the bias

[2]A transconductor transforms an input voltage into a current output with the additional condition that the output current must be linearly related to the input voltage: $I_{out} = G_m V_{in}$.

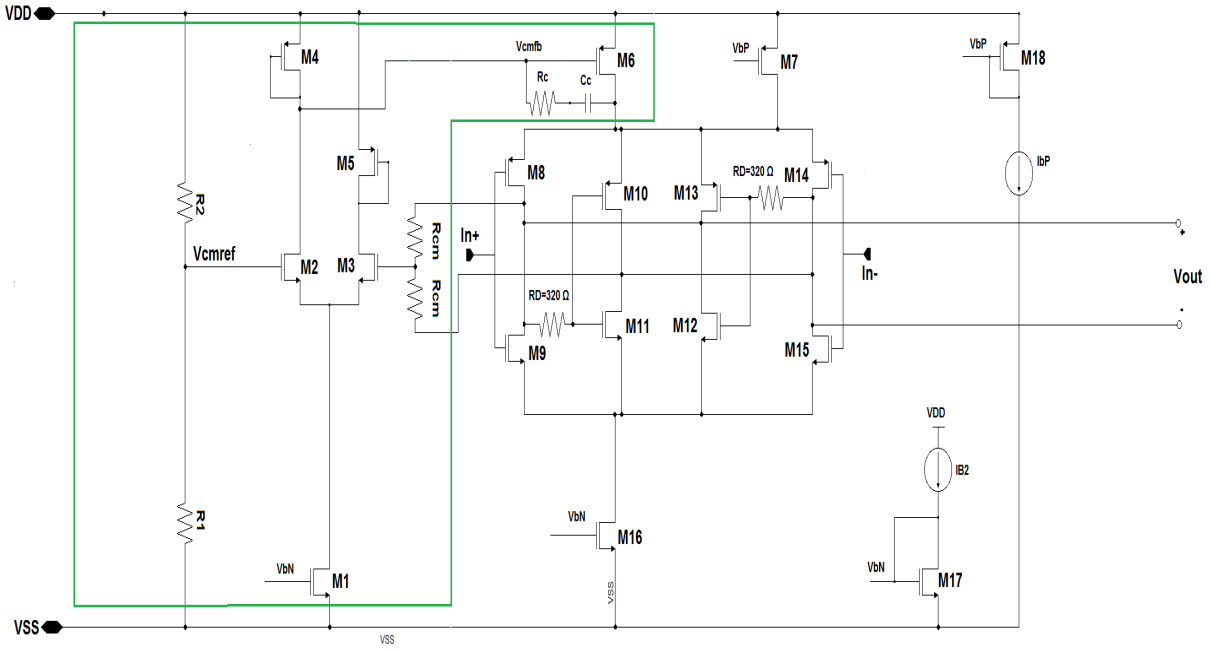


Figure 4.5: Transmitter 2 schematic. The CMFB circuit is circled whereas G_{m2} consists of the transistors M11, M12, M13 and M14.

currents in the overall system. Also in this driver the voltage reference V_{cmref} is fixed to the value of 1.1V by a resistive divider.
With regard to the stability of the system, the $R_c - C_c$ series compensates the CM feedback loop frequency response. Moreover, the current in the driver is provided by both the transistors M6 and the transistor M7, in order to reduce the common mode feedback loop gain[25]. The two current sources I_{bN} and I_{bP} independently bias the upper and the lower current mirrors.

By using Transmitter 1 we observed voltage spikes as well as ringing which are due to several non-idealities in the circuit, such as the impedance mismatches and the imperfect terminations. In particular, the signal reflections are generated by the impedance mismatch and they result an overshoot or an undershoot at the output of the driver. A G_{m2} scheme is added in Transmitter 2 in order to control the variation of the output voltage swing in fast transitions of the system. Even if the output current remains unchanged, a part of the total driver current flows in G_{m2} and it is delivered to the load by some delay which is provided by R_D and C_D, $\tau = R_D C_D$. In this case, G_{m2} works like a simple current source, i.e. two of its transistors are working in saturation region whilst the other two are turned off.

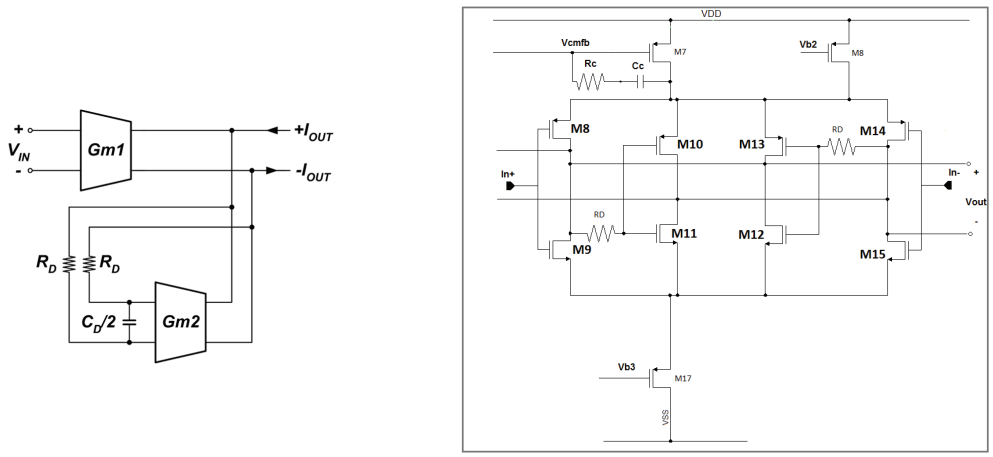


Figure 4.6: (L) The output driver circuit is represented by using the two transconductors G_{m1} and G_{m2} [25]; (R) Focus of the driver.

During the transition, before G_{m2} completely switches, the transfer function of the circuit is:

$$\frac{V_{OUT(s)}}{V_{IN(s)}} = \frac{G_{m1}(1 + R_D C_D s)}{b_0 + b_1 s + b_2 s^2 + b_3 s^4} \tag{4.5}$$

in which the coefficients b_n, n=0...3, depend on the termination resistor R_{Term}, on the resistor R_D, on the capacitance C_D and on the model of the transmission line which is used. In the formula (4.5) G_{m1} is the transconductance value of G_{m1}. In order to ensure the stability of the driver it is necessary that $G_{m2} < \frac{1}{R_{Term}}$.

The total transconductance G_m of the circuit can be lowered in order to control the output voltage slew. It is given by the expression:

$$G_m(s) = \frac{I_{out}(s)}{V_{in}(s)} = (G_{m1} + G_{m2}) \cdot \frac{1 + sR_D C_D \frac{G_{m1}}{(G_{m1}+G_{m2})}}{1 + sR_D C_D} \tag{4.6}$$

in which the zero of the transfer function is larger than its pole.
Furthermore, in this configuration of the circuit the total input capacitance of the output stage can be reduced by means of the proper sizing of the transistors. As shown in [25], the input capacitance of the output stage diminishes if the size of the cross coupled switches is larger than the size of the main switches. In particular, by defining the ratio:

$$r_f = \frac{G_{m1}}{G_{m1} + G_{m2}} = \frac{W_{M8}}{W_{M8} + W_{M10}} = \frac{W_{M9}}{W_{M9} + W_{M11}} \tag{4.7}$$

the minimum input capacitance of the output stage is obtained when $r_f = 0.375$ [25]. However, in sizing G_{m2} transistors we also have to consider the suitable value of the capacitance C_D, since it is implemented by means of these transistors and its value influences the delay time τ_D. Thus, in order to minimize the time degradation at the input of G_{m2}, we needed a proper choice of the transistor sizes.

Finally, we emphasize the differences between the Transmitter 2 and the Transmitter 1:

- the original design of Transmitter 1 uses a 0.13 μm CMOS technology with a 2.5 V supply voltage and 1.2 V common mode voltage. Thus we had to scale this circuit to adapt it in 0.18 μm CMOS technology and reduce its power supply. Transmitter 2, instead, has already been designed in the same technology node of our interest, with 1.9 V supply voltage and 1.2 V common mode voltage, thus we modified slightly the original scheme.

- In Transmitter 1 the switches are implemented using NMOS transistors in order to speed up their ON/OFF switching. In Transmitter 2 both NMOS and PMOS transistor are used as switches.

- In Transmitter 1 the common mode voltage is fixed by means of the replica bias circuit. Otherwise, a common mode feedback circuit is used in Transmitter 2.

4.3 Receiver

In order to complete the LVDS interface, we designed a receiver in 0.18 μm CMOS technology based on the circuit already employed in similar applications at CERN. Also in this case a scaling process was necessary. Figure 4.7 shows the receiver schematic. This first stage of the receiver is a CMOS complementary self-biased differential amplifier with rail-to-rail common mode input range which works with the same driver supply voltages, $V_{DD} = 1.8V$ and $V_{SS} = 0V$.
The circuit thus designed allows to circumvent the problems due to the low supply voltage. Indeed, when we lower the power supply voltage the input common mode voltage should not be very close to the supply voltages in order to guarantee both the appropriate gain and a sufficient voltage swing of the amplifier. Indeed, with the present configuration the input common mode ranges from V_{DD} to V_{SS} .

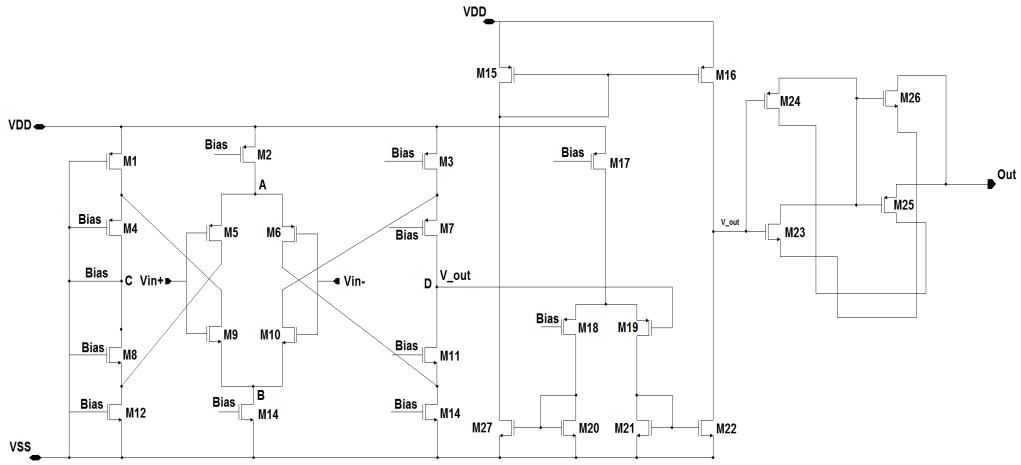


Figure 4.7: Receiver schematic. The first gain stage is a complementary self-biased differential amplifier with rail-to-rail common mode input voltage range.

The self-biasing scheme, it has two advantages. The bias scheme makes the bias point less sensitive to the temperature or process variations, supply voltage variations and common mode input voltage because of an internal negative feedback provided within the system. Moreover, the self-biasing provides a strong common mode rejection ratio which allows to enlarge the input common mode voltage range [27].
If we short the two input lines and connect them to the voltage V_{cm}, the self biasing scheme ensures that the output voltage V_{out} measured in the node D is always equal to the bias voltage (V_{bias}) at the node C even if V_{cm} can vary from V_{DD} to V_{SS} (rail-to-rail variation). Indeed, if V_{cm} varies, the negative feedback attenuates the changes in V_{bias} and, correspondingly, in $V_{out} = V_{bias}$. The common mode gain of this stage is defined as

$$A_c = \frac{1}{2}\frac{v_{out}}{v_{in+} + v_{in-}} \tag{4.8}$$

where v_{out}, v_{in+} and v_{in-} are respectively the small signal variations of the output and the two inputs. By using a small signal model we obtain a good approximation of the common mode gain:

$$A_c \approx \frac{g_{d2} + g_{d13}}{g_{m2} + g_{m13} + 2g_{m4} + 2g_{m12}} \tag{4.9}$$

where the terms g_d indicate the drain conductance[3] and g_m are the transconductances of the transistors. We can note in this formula that A_c is minimized

[3] $g_d = \frac{1}{r_{ds}}$ represents the channel length modulation.

thanks to the g_m contributions[27].

This receiver has differential inputs and single ended output. It amplifies the difference between the two inputs V_{in+} and V_{in-} which are measured to the ends of termination resistors.
It should be noted that the system has two symmetrical branches with the nodes A and B, even if on the right of these nodes we take the output signal whilst on the left the bias voltage is measured.
A negative feedback is generated which provides the bias voltage from the point C to the gates of M2- M13 and to the gates of the transistors in the two symmetrical branches. This scheme makes the amplifier less sensible to the variations with temperature, process, etc., which cause a change in the bias. Indeed, if the bias voltage rises, the voltage at the gates of transistors M1 (PMOS) and M8 (NMOS) rises but whith the effect of lowering the bias voltage. A similar situation occurs when the bias voltage decreases.

The amplification of the inputs is due to a folded cascode pairs on the left part of the circuit as well as on the right part. Indeed, each transistor pair M5-M8 as well as M9-M4 on the left branch (M6-M11 and M10-M7 on the right branch) consists of NMOS and PMOS transistors so that the current folds around in direction when flow in the two device. This design allows us to obtain a high gain even though we are using a single stage amplifier.
With an input common mode of 1.1 V both of the two input pairs are in active region; thus a small signal model give us a differential gain which is approximately

$$A_d = \frac{g_{m5} + g_{m9}}{g_{d4} + g_{d8}} \tag{4.10}$$

Finally, we observe that this scheme consists mainly of complementary pairs, so that each transistor above the nodes C and D has proper counter part of opposite type below the two nodes.
The second stage of this receiver is very similar to the OpAmp employed in Transmitter 1. Also in this case it is used as a comparator, thus it does not need a high gain but its architecture reduces the propagation delay time[26].

Chapter 5

Link Optimization

In this chapter we present the results of the simulations performed with the transceivers described in Chapter 4.
We design the drivers and the receiver in 0.18 μm Qwell CMOS technology, in order to satisfy the requirements of the ITS upgrade, including the reduction of the power consumption, the minimization of the material budget, the high transmission rate (up to 1 Gbps). Furthermore, we verified that the interfaces fulfill the standard of the LVDS transmission (see Chapter 3).
In Chapter 4 it was shown that Transmitter 1 does not permit to obtain a good quality of the transmitted signal. The unadequate driver performance with a bit rates of 320 Mbit/s provided the motivation to design the alternative device named Transmitter 2.

A deeper analysis about the behviour of the Transmitter 2 shows that it is possible to obtain a good quality of the transmission at the bit rates up to 1 Gbps.
We perform Monte Carlo simulations, which includes process variations and mismatch effects of all elements, and the corner simulations for different temperature values in order to study the performance of the system in a comprehensive way.
Finally, the simulation results of the complete interface consisting of Transmitter 2 and the receiver are reported.
Here the advantages of the differential transmission can be recognized, since it allows to minimize the disturbances in the driver outputs in order to improve the characteristics of the received signal.

5.1 Transmission line

The connections between the driver outputs and the receiver inputs are modeled by a real transmission line with a multi-conductor transmission line (mtline) followed by some capacitances and inductances which represent the parasitic effects of the package.
Regarding the parasitic components, they are caused by the chip structure and the packagings. In our model we set $L_{n1} = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$.

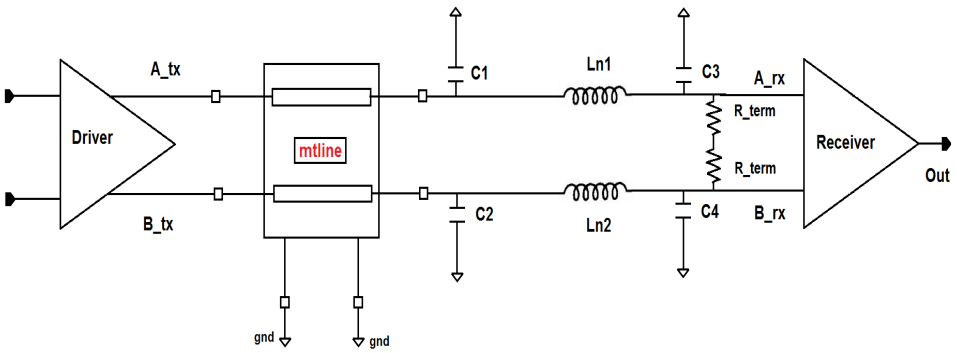


Figure 5.1: Transmission line model; the scheme is not in scale.

The mtline has a characteristic impedance $Z_0 = 50\Omega$ (see Chapter 3). Its properties are summarized in Tab. 5.1 where the signal line conductivity corresponds to the copper metal line.

The physical length L of the mtline causes a delay in the propagation of the signal, which get worse by increasing L. As shown in figure 5.2, if B_{tx} is the input signal of the mtline, thus the signal B_{rx} at its output suffers of a propagation delay t_{pd} which is determined by subtracting the time intervals that B_{tx} and B_{rx} require to reach the 50% of their final values.
Simulations were performed by setting L equal to 0.5 m, 1 m and 2 m; the obtained t_{pd} are reported in Tab. 5.2.

During these simulation with different physical length values, we also

Table 5.1: Mtline Properties

Numb. of lines	2
Physical length (L)	50 cm
Multiplicity factor	1
Rel. dielectric constant of layers (er)	4.45
Dielectric layer thickness	150 μm
Signal line width	280 μm
Signal line thickness	9 μm
Signal line height (h)	9 μm
Signal line spacing	280 μm
Ground plane Thickness	9 μm
Signal line conductivity	33.3 MS

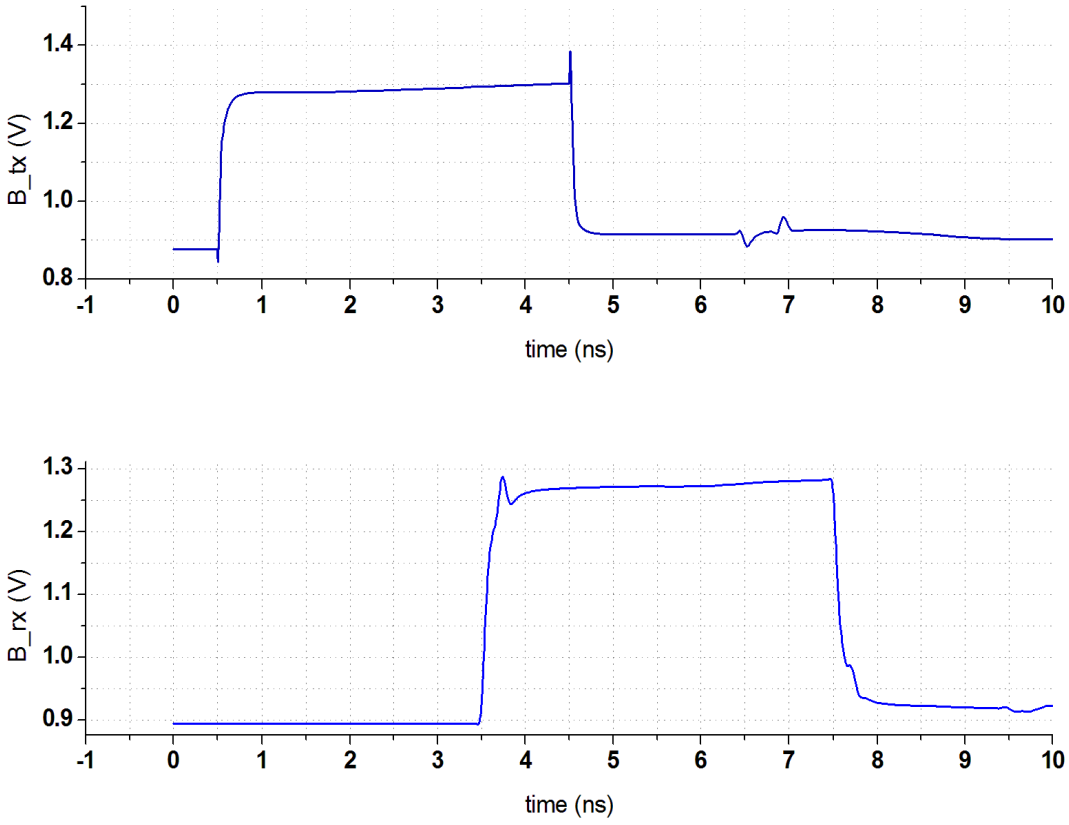
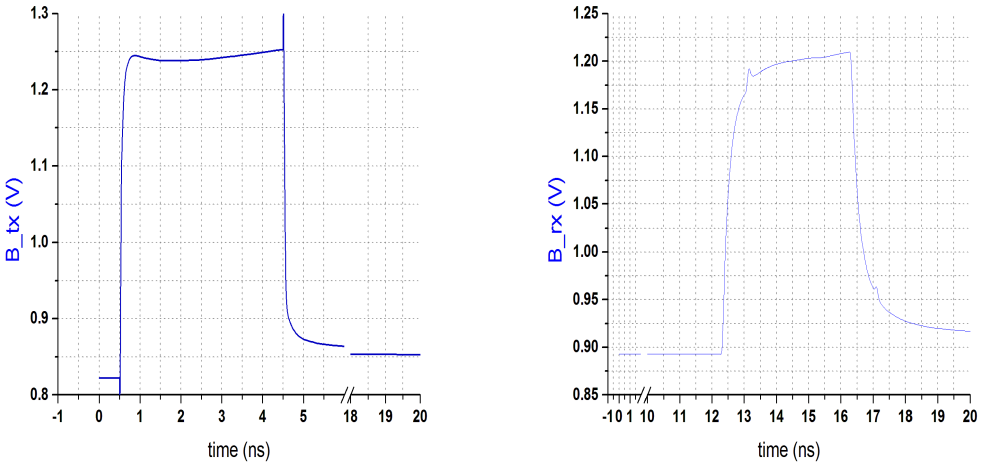


Figure 5.2: Propagation delay with a 50 cm mtline.

Table 5.2: Propagation delay

Phys. Length L (m)	t_{pd} (ns)
0.5	3.01
1	5.97
2	11.93



(a) Mtline input.

(b) Mtline output.

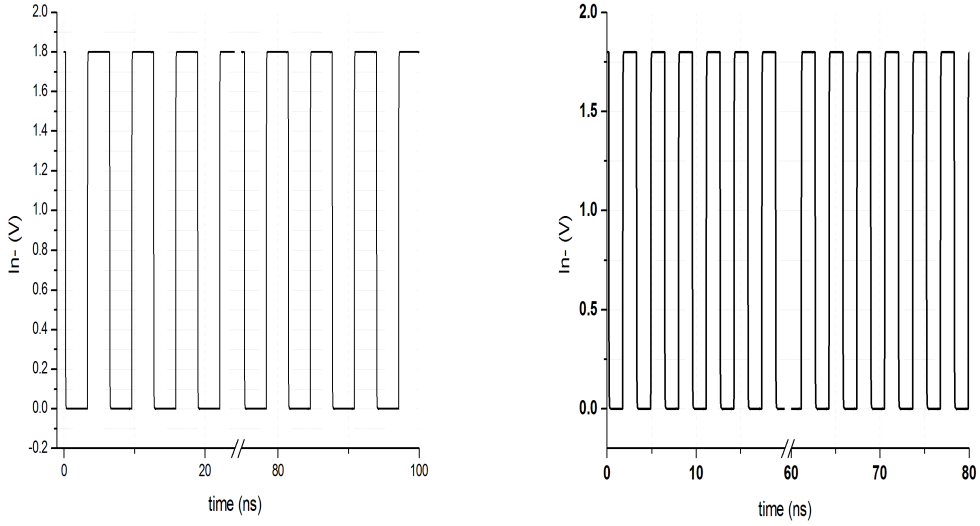
Figure 5.3: Simulated impulse response with a 2 m mtline; the simulation was performed by using Transmitter 2

noted a small attenuation effect of the signal which traverses the mtline, due to at the physical properties of the modeled cable.
A comparison between B_{tx} and B_{rx} with a 2 m mtline is shown in figure 5.3.

5.2 Simulation Test Bench

In order to test the performances of our LVDS interfaces we perform the simulations by using the square waves and the Pseudo Random Binary Sequence or PRBS.
The square waves were sent by using a built-in voltage source already present in the Cadence library. They are deterministic waveforms employed in order to control if the ringing effect or the overshoot in driver outputs were present. By means of the simulated square waves we verified that the rising edge cross the falling edge at the common mode output of 1.1 V as we fixed in design

stage and if some asymmetries affects our systems.
Since the bit rate of our interest ranges between 320 Mbit/s to 1 Gbit/s, we use square waves which have the same frequencies.



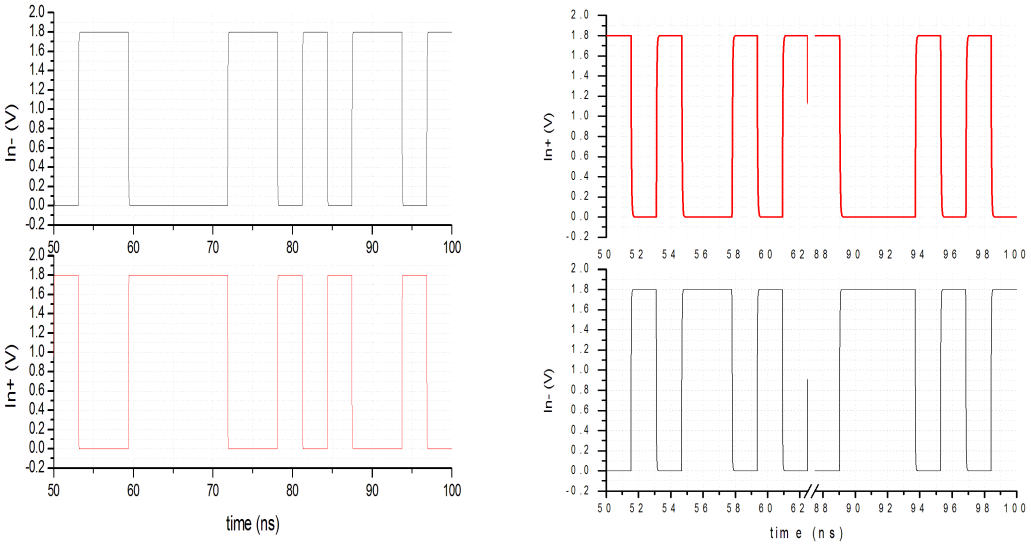
(a) 320 Mbit/s Input square wave

(b) 620 Mbit/s input square wave

Figure 5.4: Input square waves.

The PRBS is a waveform defined for points which is used in order to test the dynamic response and the stability characteristics of the circuits in different conditions. Thus, the transmitted signals were analyzed by means of the eye diagrams.
The PRBS is pseudo random since after N bit it starts to repeat itself. These waveform are already present in Cadence library but the users have the possibility to generate them by using a Verilog file.
In our case, we used both the custom PRBSs at 320 Mbit/s and 640 Mbit/s and the1 Gbit/s PRBS already present in Cadence. The waveforms are showed in figure 5.5.

By using SPECTRE in Cadence environment we can perform transient simulations, i.e. we analyze the time evolution of the signal transmission. Indeed, all the simulation reported below were executed by setting a transient time of 300 ns for the square waves and of 1 μs for the PRBS.
This method is useful to estimate the deterministic jitter affecting both the drivers and the receiver.



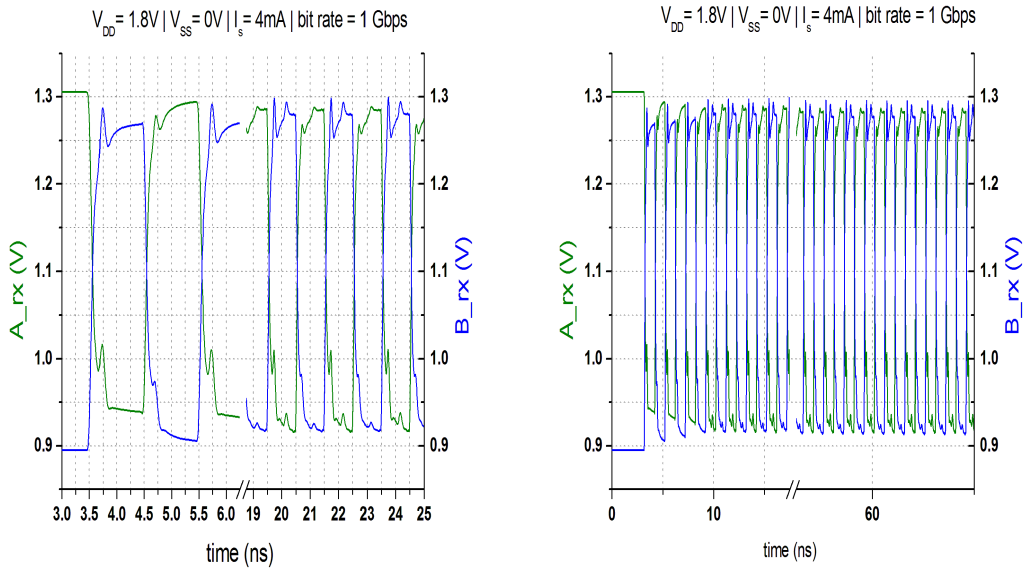
(a) 320 Mbit/s Input PRBS

(b) 620 Mbit/s Input PRBS

Figure 5.5: Input PRBS.

However, SPECTRE permits also to simulate the noise in the time domain. By selecting the Transient Noise Analysis, the noise sources are added providing random noise signals in the simulations during the time domain evolution.
The users can be set the bandwidth of the noise in order to define the maximum and the minimum frequency noise components (respectively noisefmax and noisefmin). Furthermore, we can specify the noise seed (noiseseed) which is the seed for the random number generator and the minimum time interval between noise source updates (noisetimin).
If the noise is added in the simulations, we can calculate the contribution of the random jitter which is due to the noise amplitude.
For this reason, all the simulations which are reported in this work, including corner analysis, were performed by using the transient noise analysis, by setting:

- noisefmax = 10 GHz;
- moisefmin = 1 mHz;
- noiseseed = 1;
- noisetmin = 100p.



(a) 1 Gbit/s simulated square wave

(b) 1 Gbit/s simulated square wave including transient noise

Figure 5.6: Comparison between the 1 Gbit/s simulated square waves.

5.3 Results of Transmitter 1

In order to give an idea of the transmission quality of this driver we report only the simulations of Transmitter 1 with a 320 Mbit/s PRBS.
figure 5.7 shows the Transmitter 1 outputs: the effect of the ringing on the rising edge of the signal together with the rapid discharge in the falling edge, negatively influences the signal transmission.
The ringing is due to the impedance mismatch between the transmission line and the load, as observed by setting $L_{n1} = L_{n2} = 0$. As a consequence, the threshold of the transition from the low logic level to the high logic level and vice versa is not equal to the output common mode value V_{cm} of 900 mV and it varies during the whole transmission.
This is well depicted by the eye diagram in figure 5.8: the high and the low logic levels are not well defined and the eye is not wide open because of the total jitter affecting the signals.

Since this driver performances with a 320 Mbit/s bit rate does not satisfy the standard LVDS requirements, further analysis at more high bit rate were not performed.

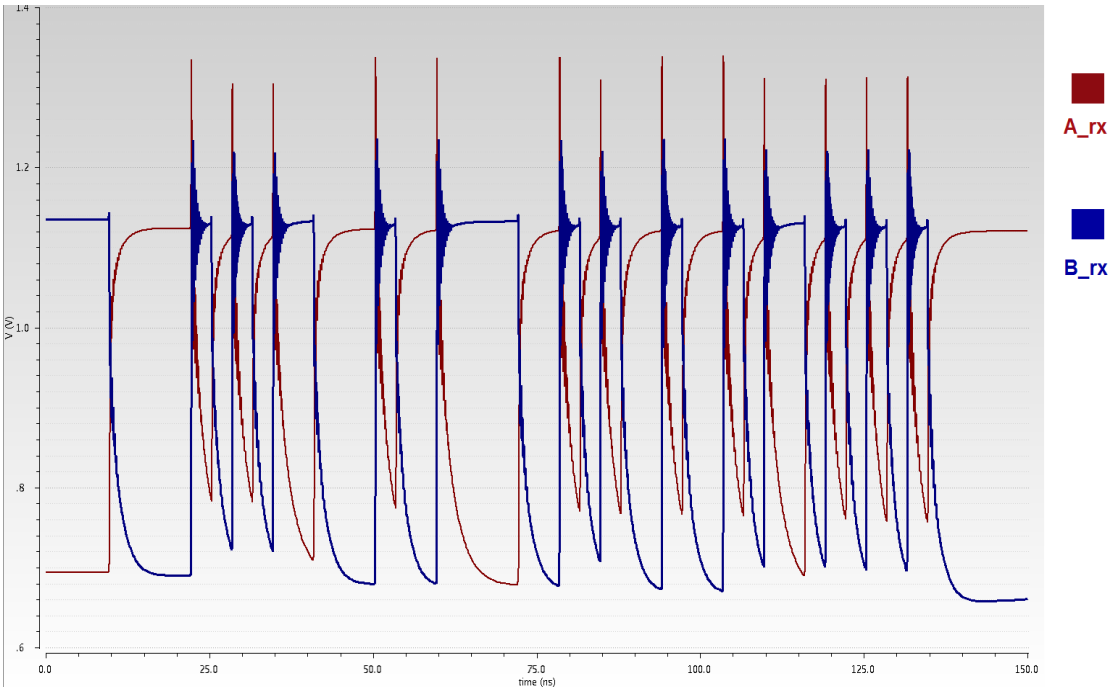


Figure 5.7: Transmitter 1 outputs: simulated 320 Mbit/s PRBS response. The current flowing in the driver is $I_S = 4mA$

5.4 Results for Transmitter 2 and receiver

It should be noted that the ringing and the picking which suffered the output of Transmitter 1 are strongly reduced in Transmitter 2, as shown in the simulated 320 Mbit/s square wave in figures 5.9 (a) and 5.9(b). After some time ($\approx 3ns$), the driver well replicates the input square wave for all I_S values: in this way the voltage swing V_{VS} at the ends of the termination resistors is about 400 mV when $I_S = 4mA$ whereas V_{VS} is about 250 mV if $I_S = 2.5mA$. Although the behaviours of the two driver outputs A_{rx} e B_{rx} are slightly different, the crosspoint between the rising edge and the falling edge of the signal lies around the common mode value of 1.1 V, as it was defined during the circuit design.
By varying the frequency of the square wave at the input of Transmitter 2, a small variation in the rise time and in the fall time of the simulated square wave is recorded. However, the output V_{cm} is unchanged at the value of 1.1V.

At a simulated square wave frequency of 1 Gbit/s overshoot of the signal is present. However, it does not significantly influence the receiver output (Fig 5.11). Indeed, thanks to its design characteristics, the receiver elaborates the

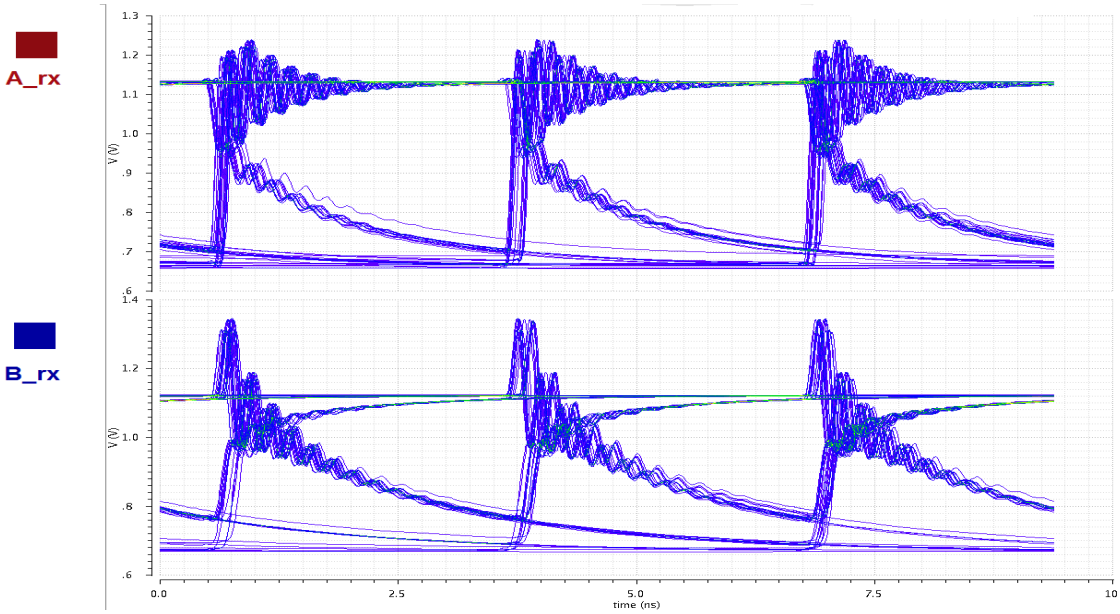


Figure 5.8: Eye diagram of Transmitter 1 outputs.

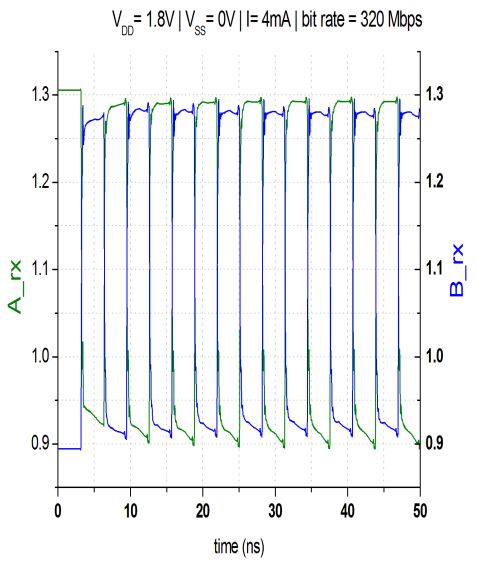
difference between its inputs, A_{rx} and B_{rx}, minimizing the ringing effect and giving at the output the same input square wave.

In order to determine the random jitter affecting our driver, we send in input a 1 Gbit/s square wave including the noise component in the simulation.
By analyzing how the cross point of the driver output signals is moved respect its optimal value, we determine a random jitter component of $R_{rmsj} = 3.4ps$.

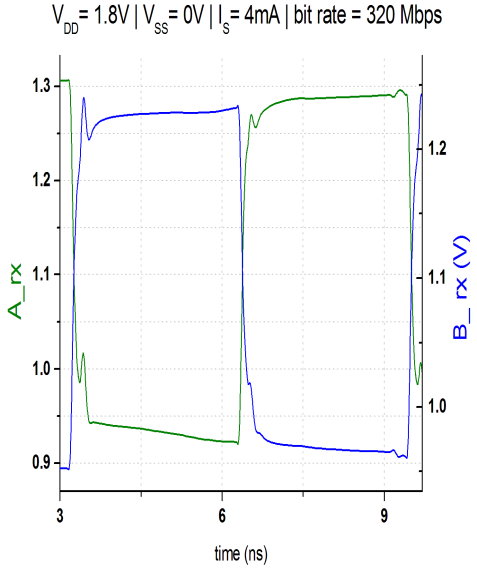
5.4.1 Corner Analysis

The transceiver was also simulated in some corners in order to take into account process variation, mismatch effects and temperature variations.
The corner analysis is a worst-case approach in which we take into account multiple corner process, power supply and temperature variations.
As we can see in figure 5.12, the behaviour of Transmitter 2 at room temperature does not change when temperature variations occur. The small changes in the values of the logic levels are especially due to the reduction of the mosfet threshold by increasing the temperature.

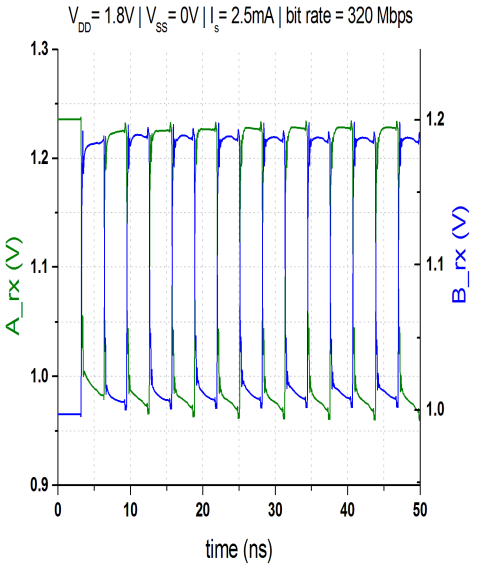
Monte Carlo simulations are employed in order to verify the stability of the system with statistical variations. They include process variations and



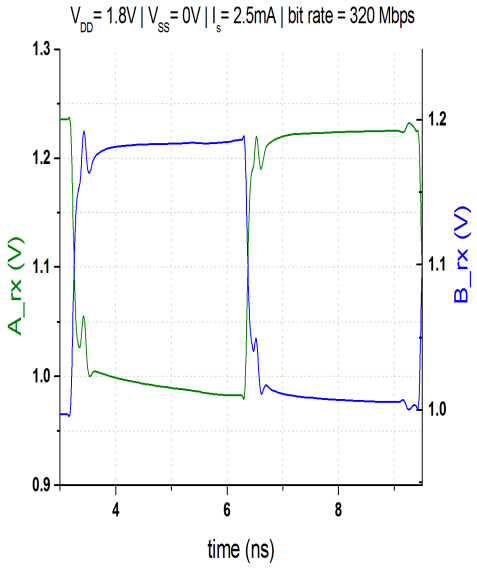
(a) Simulated 320 Mbit/s square wave



(b) Zoom on the step of B_rx output

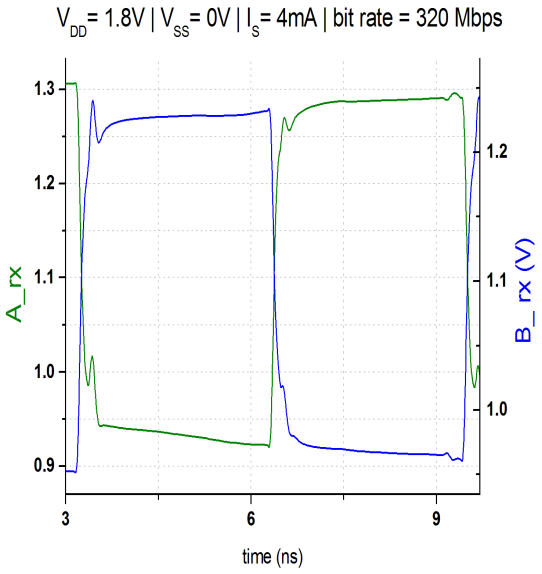


(c) Simulated 320 Mbit/s square wave

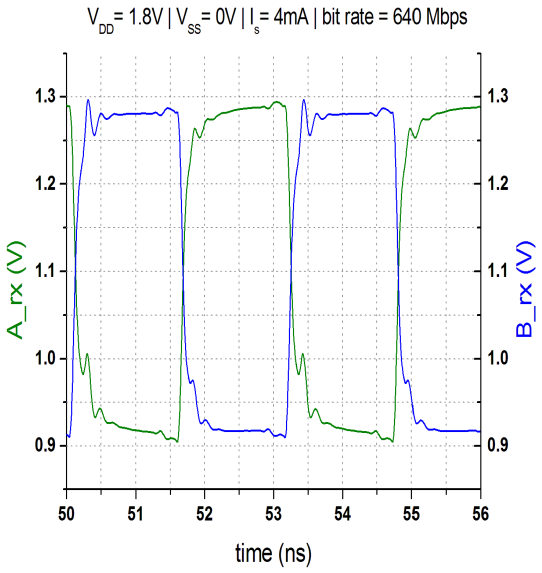


(d) Zoom on the step of B_rx output

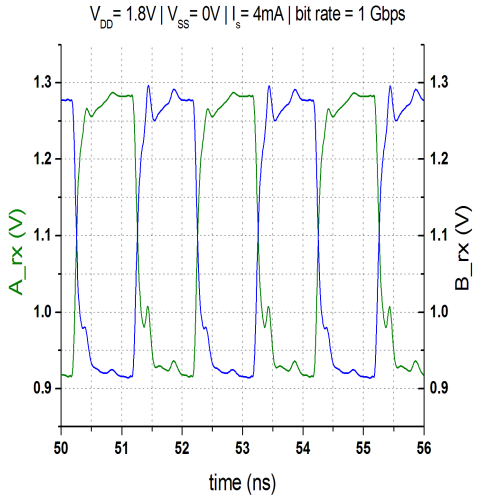
Figure 5.9: In this simulation the transmission rate is 320 Mbit/s, the lenght of the mtline is assumed L = 50cm and the parasitic effects are $Ln1 = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$.



(a) Simulated 320 Mbit/s square wave

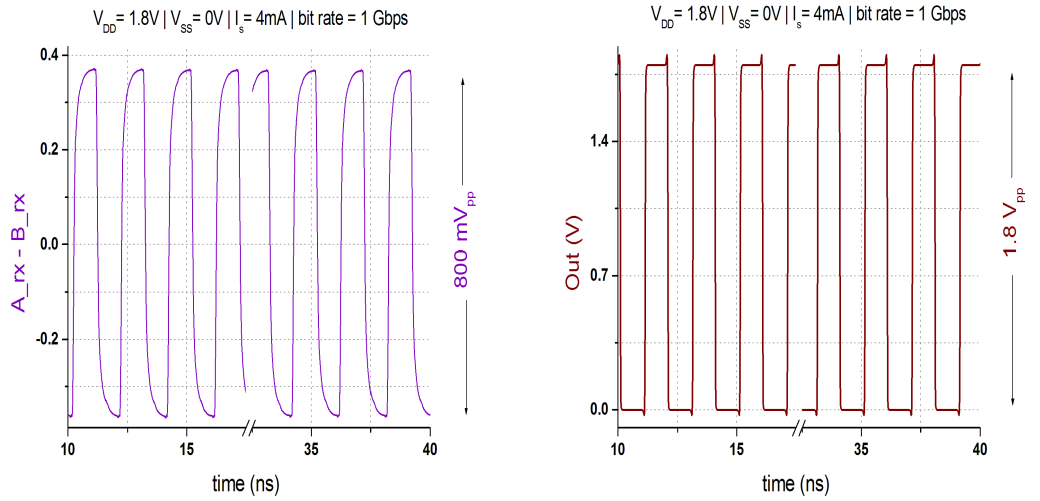


(b) Simulated 640 Mbit/s square wave



(c) Simulated 1Gbp/s square wave

Figure 5.10: In these simulation the lenght of the mtline is set to L = 50cm the parasitic effects are $L_{n1} = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$. The current delivered to the load is I_S is 4 mA.



(a) Differential receiver input at 1Gbit/s transmission rate

(b) Receiver output at a 1Gbit/s transmission rate

Figure 5.11: In these simulation the transmission rate is 320 Mbit/s, the lenght of the mtline is set to L = 50cm and the parasitic effects are $L_{n1} = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$.

mismatch effects and take into account the possibility that, during the fabrication of the ICs, the electrical parameters of the adopted technology can change randomly. For example, the threshold voltage and the k parameter of the NMOS and the PMOS strongly change with the corner process: for the "typical" mosfet model the V_{th} is about 600 mV whilst the same parameter for the "fast" model V_{th} is only 400 mV.
The simulation results are shown in figure 5.14, where (a) refers to the driver outputs A_{rx} and B_{rx} whereas (b) is the transceiver output. Although the behaviour of the driver outputs is similar to what achieved with typical conditions ($T = 27$, "typical" MOS), the process variation and mismatch effects are more evident in the transceiver output.

We also consider the possibility of reduction of the supply voltage V_{DD} from the value of 1.8 V to the value of 1.7 V.
According to what we expected, the output common mode level is lowered to the value $V_{cm} = 1.0V$ and the waveform shape does not change.

Furthermore, thanks to the rail-to-rail receiver, the transceiver output faithfully reproduce the input square wave (Fig. 5.16).

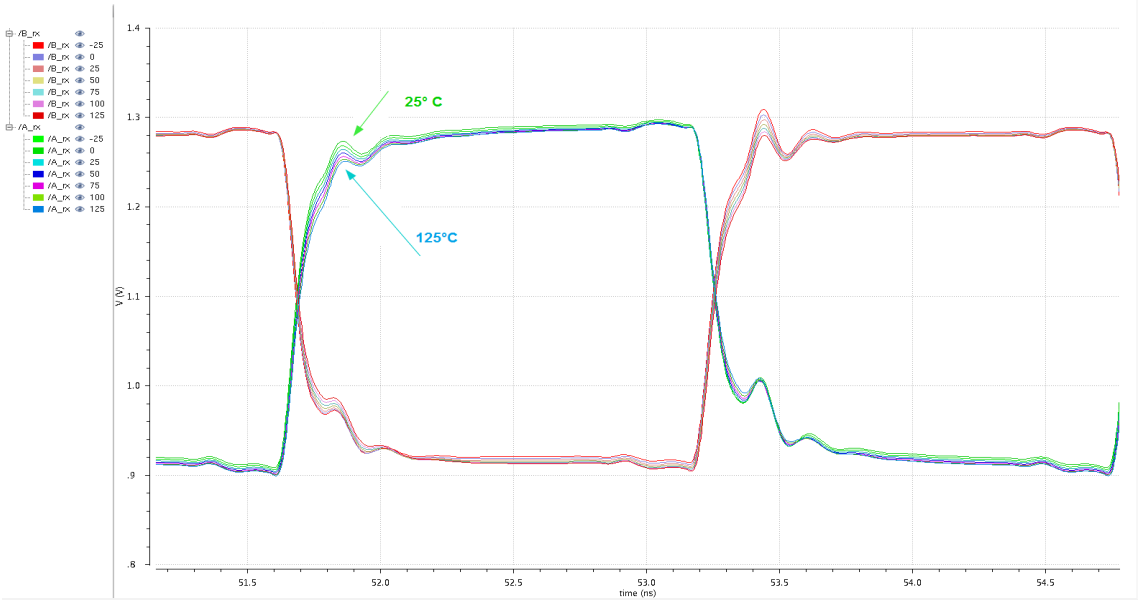


Figure 5.12: Corner simulation results for different temperature. In this simulation the input is a 640 Mbit/s square wave, the lenght of the mtline is set to L = 50cm and the parasitic components are $Ln1 = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$. The temperature ranges from -25 to 125.

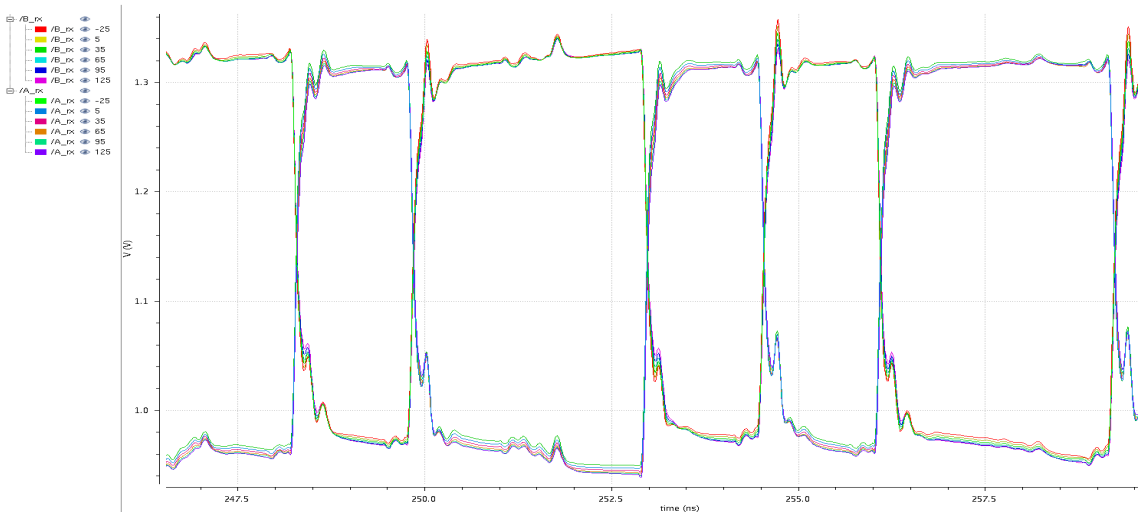
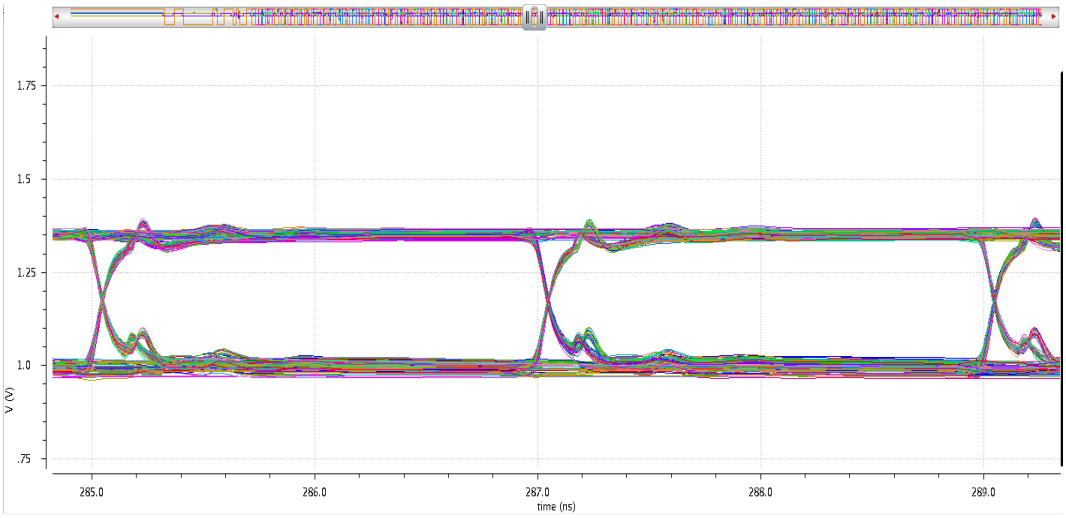
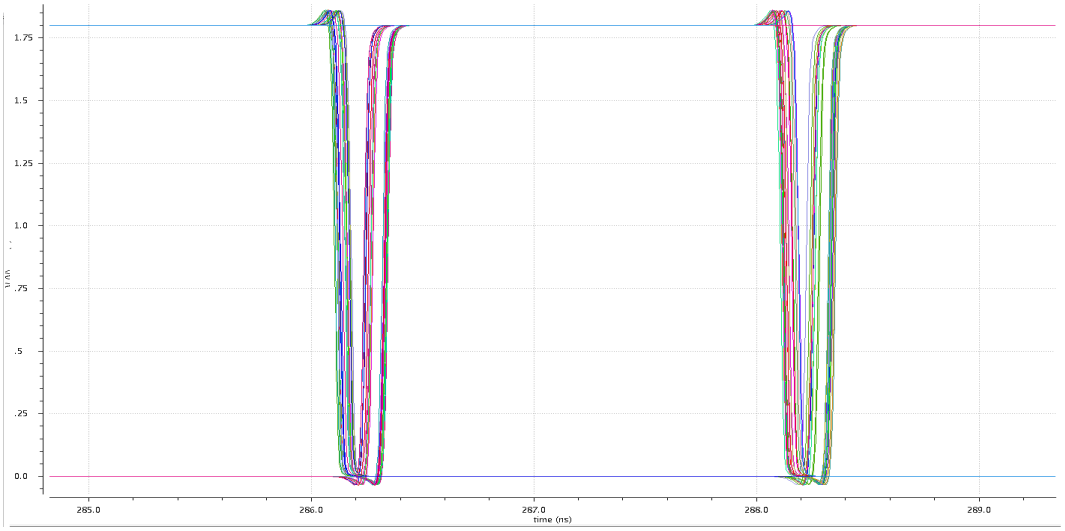


Figure 5.13: Corner simulation results for different temperature. In this simulation the input is a 640 Mbit/s PRBS, the lenght of the mtline is set to L = 50cm and the parasitic components are $L_{n1} = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$. The temperature ranges from -25 to 125.



(a) Driver outputs A_{rx} e B_{rx}

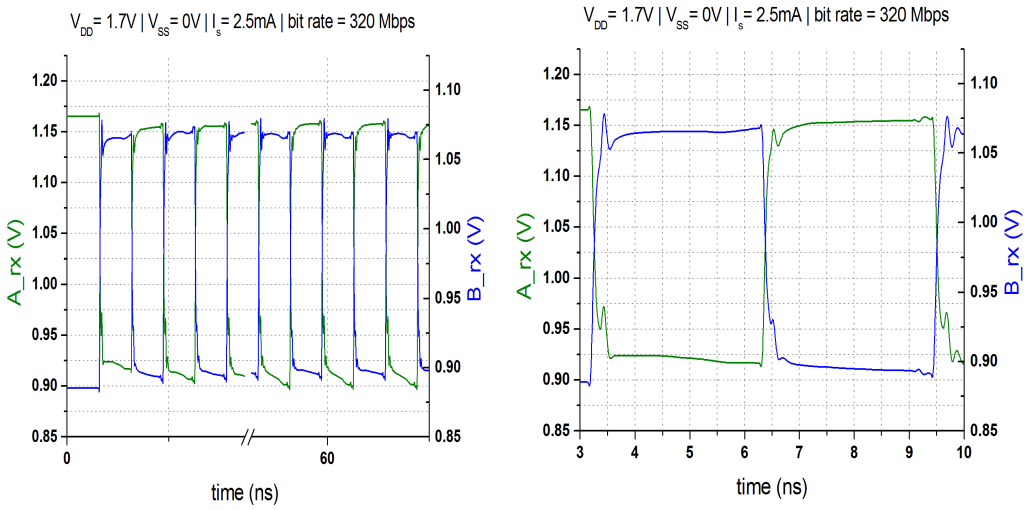


(b) Receiver output

Figure 5.14: Monte Carlo simulation including both process variation and mismatch effects. In these simulation the transmission rate is 320 Mbit/s, the lenght of the mtline is set to L = 50cm and the parasitic components are $L_{n1} = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$.

5.5 Transmitter 2 Eye Diagrams

In order to analyze the quality of the signal transmitted by the driver and the receiver we use PRBS at several data rate which simulate the condition



(a) Driver outputs.

(b) Zoom of the simulated 320 Mbit/s

Figure 5.15: Simulated 320 Mbit/s square wave when the voltage supply is lowered to the value $V_{DD} = 1.7V$. In these simulation the lenght of the mtline is set to L = 50cm and the parasitic components are $Ln1 = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$.

at which the system have to work in a detector system.
By selecting the sampling interval and the expected period of the outputs, SPECTRE provides the eye diagrams of the output waveforms, connecting them with a vertical histograms by means of which we can determine the mean of the high and the low logic level. Some additional information, as the eye amplitude, the eye width etc. can also be obtained.

5.5.1 320 Mbit/s input data stream

The eye diagrams of the driver outputs $A_{rx}$and B_{rx} for a 320 Mbit/s PRBS are shown in figure 5.17 together with the eye diagram of the difference $(A_{rx} - B_{rx})$.
In these pattern we can observe an oscillating effect due to an overshoot on A_{rx} and on B_{rx} already underlined in the square wave simulations.
Analyzing the A_{rx} or B_{rx} eye diagram, the logic level 1 and the logic level 0 are determined together with their standard deviations. Indeed, two vertical histograms are obtained by subdividing the level 0 y-range (from 0% to 50% of the amplitude) and the level 1 y-range (from 50% to 100% of the amplitude) into one hundred bins. Furthermore, also the level 0 x-range and the

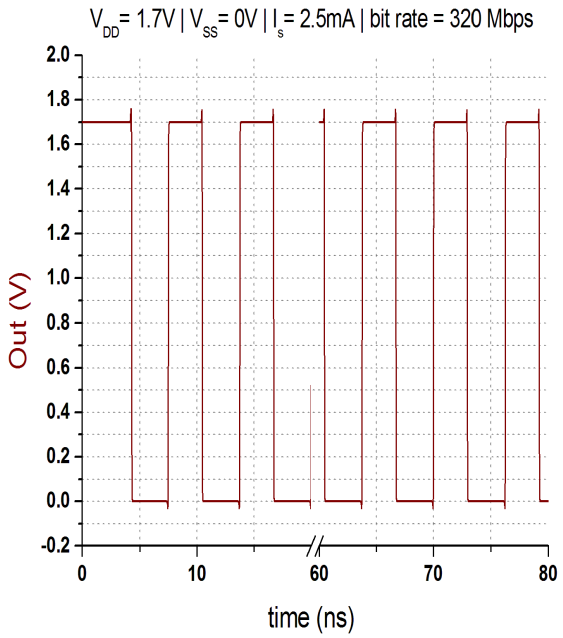


Figure 5.16: Transceiver output - Simulated 320 Mbit/s square wave when the voltage supply is lowered to the value $V_{DD} = 1.7V$. In these simulation the lenght of the mtline is assumed L = 50cm and the parasitic effects are $Ln1 = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$.

level 1 x-range have to be selected in order to determine the mean logic level values, the eye amplitude, the eye width and the eye height.
Finally, by isolating A_{rx} the list of the eye characteristics give:

- Logic level 1 lies in $(1.23 \pm 0.08)V$;
- Logic level 0 lies in $(0.97 \pm 0.08)V$;
- Eye Amplitude is 245 mV ;
- Eye Height is 235 mV;
- Eye Width is 3.105 ns

By the values reported above it should be realized that the overshoot of the signal tends to close the eye, resulting in a restriction of the eye amplitude at a value of about 300 mV instead of the nominal value of 400 mV. Furthermore, a reduction of the eye width at a value of 3.105 ns instead the bit period of 3.125 ns is also present.

The amount of the total peak-to-peak jitter is acceptable : the measured output total jitter is $T_j^{pp} = 12ps$.

However, the output difference eye diagram is quite open, although an

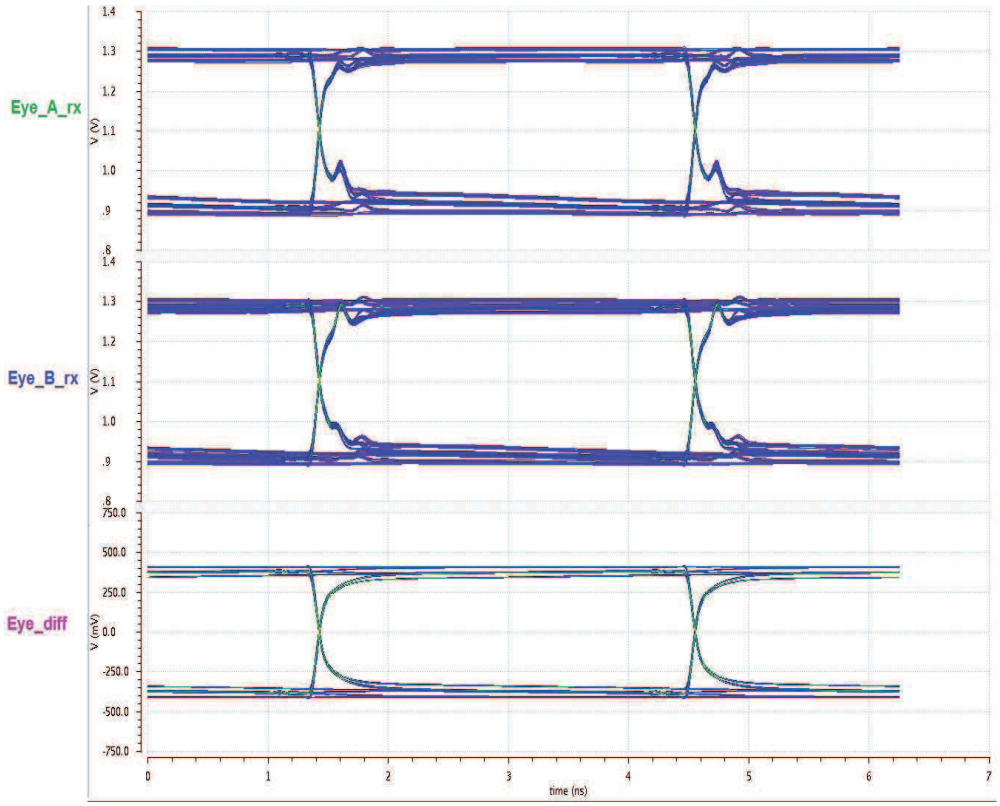
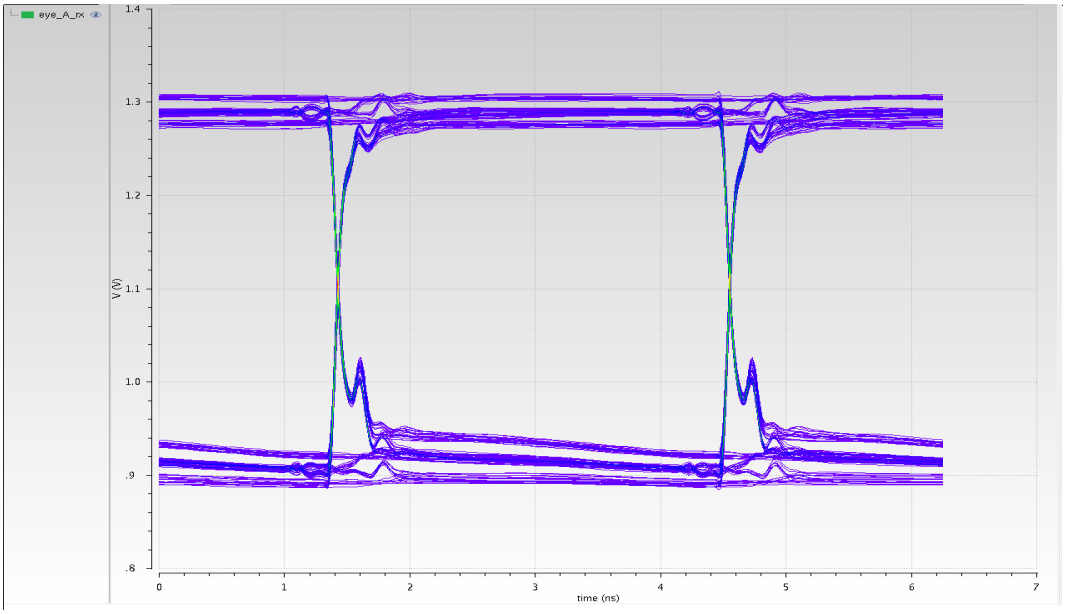


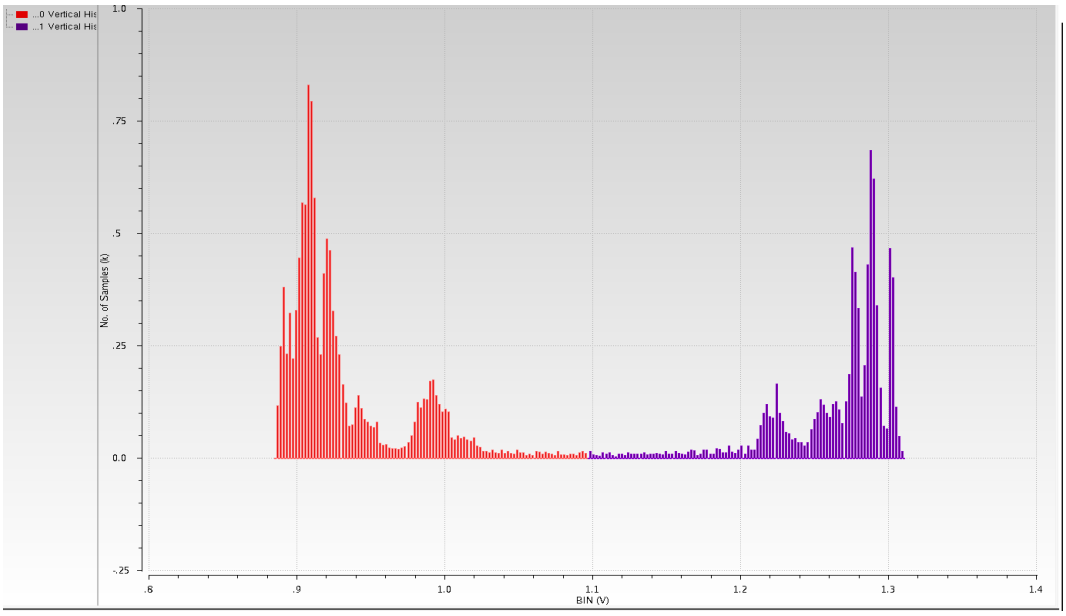
Figure 5.17: Eye Diagrams of the simulated 320 Mbit/s PRBS. In this simulation the transmission rate is 320 Mbit/s, $I_s = 4$mA, the lenght of the mtline is set to L = 50cm and the parasitic components are $L_{n1} = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$. Transient time 1 μs

attenuation of the eye amplitude is persistent; the total peak-to-peak jitter is about 13 ps. The eye characteristics are listed below:

- Logic level 1 lies in $(0.33 \pm 0.08)V$;
- Logic level 0 lies in $(-0.32 \pm 0.08)V$;
- Eye Amplitude is 642 mV instead the nominal value of 800 mV;
- Eye Height is 139.1 mV;



(a) A_{rx} eye diagram.



(b) Vertical Histograms - The number of Bins is 100

Figure 5.18: Eye Diagram of the simulated 320 Mbit/s PRBS. I_s = 4mA, the lenght of the mtline is set to L = 50cm and the parasitic components are $Ln1 = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$. Simulation time 1 μs

- Eye Width is 3.106 ns
- Rise Time is 258 ps
- Fall Time is 246 ps

It should be noted that the rise time is evaluated between the 10% and the 90% of the signal final value whereas the fall time is measured between the 90% and the 10% of the signal final value for the simulation at each data rate.

The eye diagram of the output transceiver is shown in figure 5.20. It should be noted that the rising edge does not cross the falling edge at the value of 900 mV. Furthermore, a large amount of jitter affects the signals and it is due to the time delay during the overall transmission and to deterministic jitter. Indeed, by substituting the our receiver with an "ideal" receiver we note that the previous effects are reduced. In consequence of this, the eye width is reduced whilst the eye amplitude and the eye height are equal to the nominal value of 1.8 V.

5.5.2 640 Mbit/s input data stream

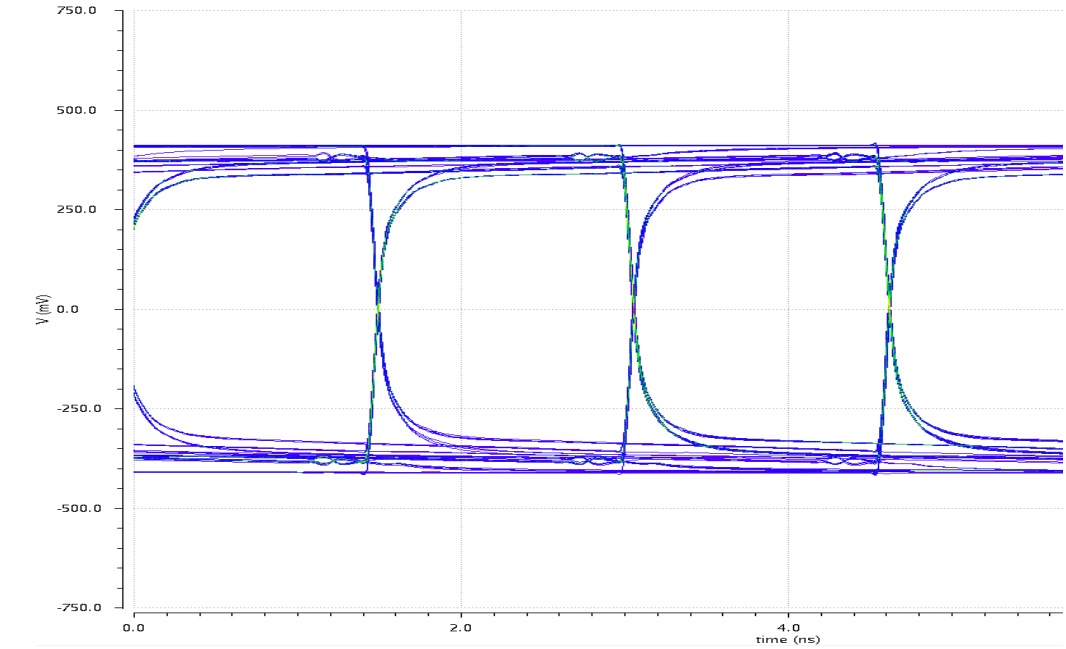
Also the driver output eye diagrams obtained with a 640 Mbit/s PRBS suffer of an overshoot of the signals which restricts the eye width and reduce the eye height.

The eye diagram characteristics obtained with this bit rate are not so different than the previous, which means that the driver behaviour appears similar in the two cases:

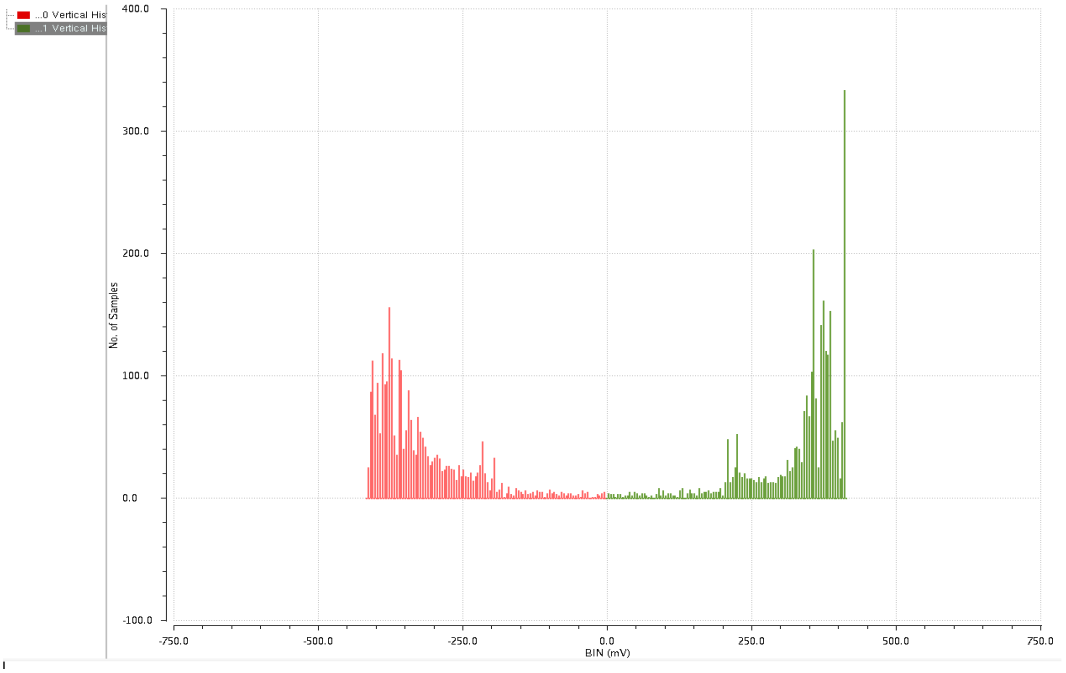
- Logic level 1 lies in $(1.23 \pm 0.08)V$;
- Logic level 0 lies in $(0.98 \pm 0.08)V$;
- Eye Amplitude is 245 mV ;
- Eye Height is 237 mV;
- Eye Width is 1.53 ns

The amount of the total peak-to-peak jitter in this case is $T_j^{pp} = 13ps$.
Regarding the difference of the Transmitter 2 outputs, the signal attenuation level is a little bit more evident:

- Logic level 1 lies in $(0.250 \pm 0.16)V$;

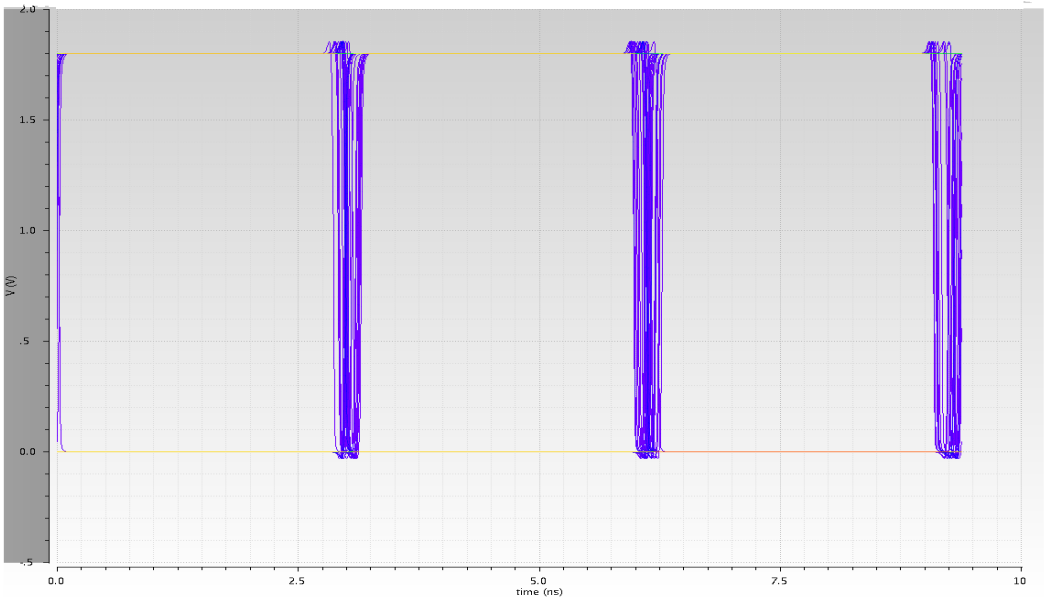


(a) Driver output difference eye diagram

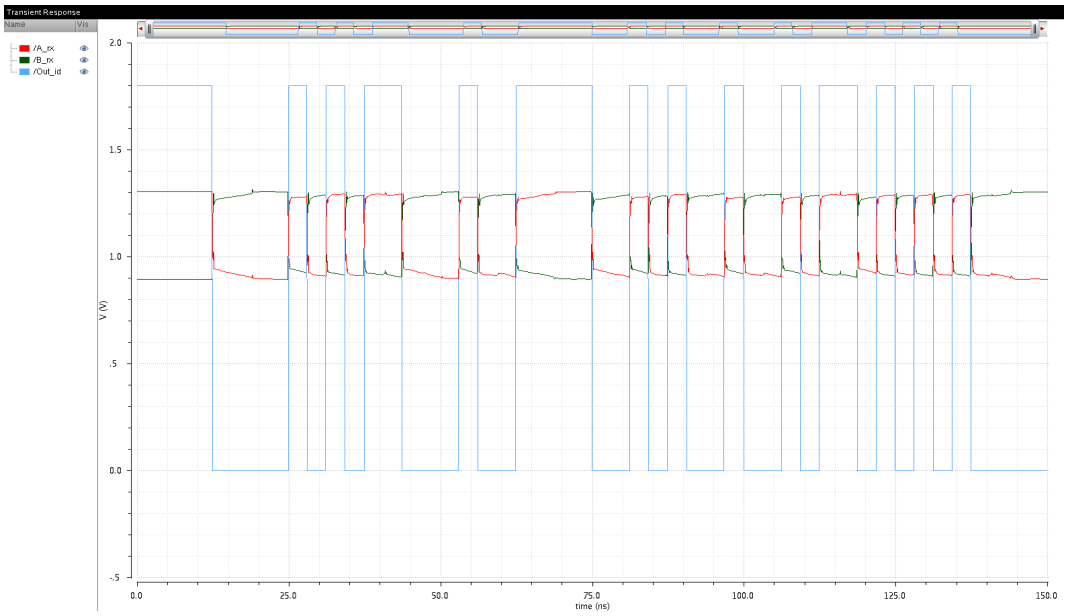


(b) Vertical Histograms - The number of Bins is 100

Figure 5.19: In this simulation the transmission rate is 320 Mbit/s, I_s = 4mA, the lenght of the mtline is assumed L = 50cm and the parasitic effects are $Ln1 = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$. Transient time 1 μs



(a) Transceiver Eye Diagram of the simulated 320 Mbit/s PRBS with our receiver



(b) Driver and transceiver output with an ideal receiver

Figure 5.20: In this simulation the transmission rate is 320 Mbit/s, I_s = 4mA, the lenght of the mtline is assumed L = 50cm and the parasitic effects are $Ln1 = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$. Transient time 1 μs

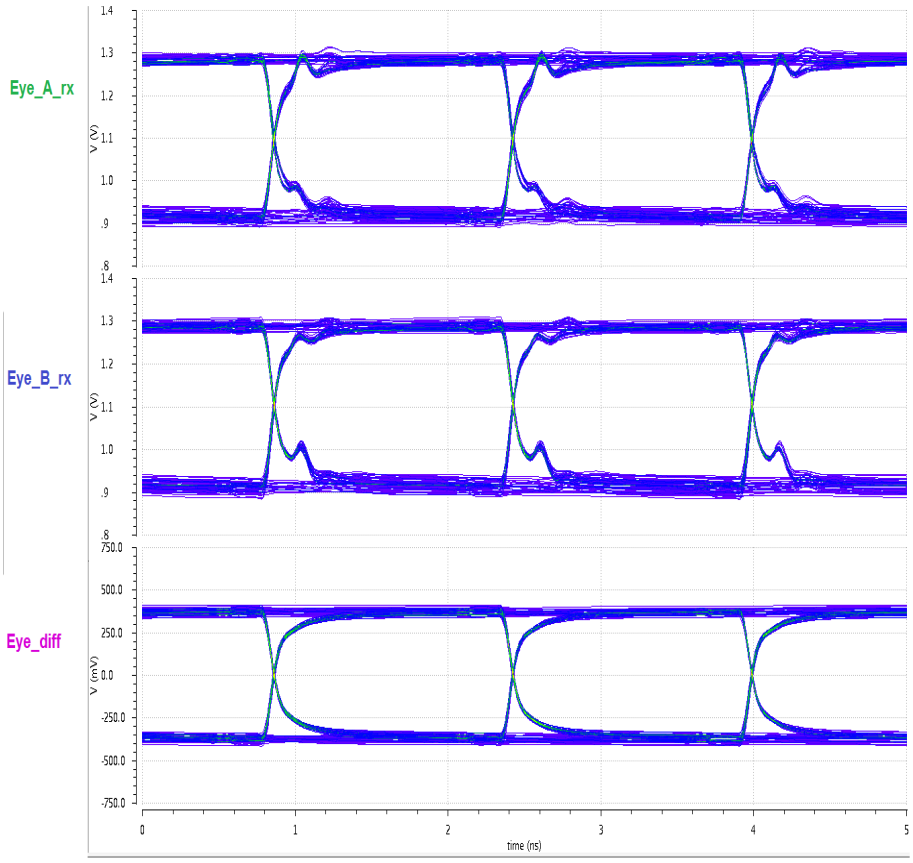
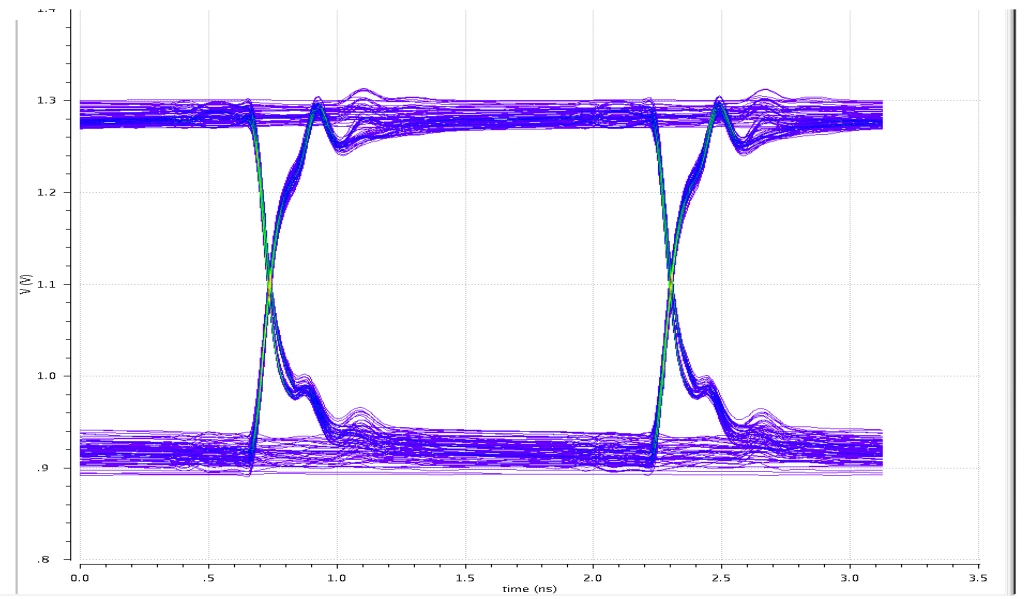


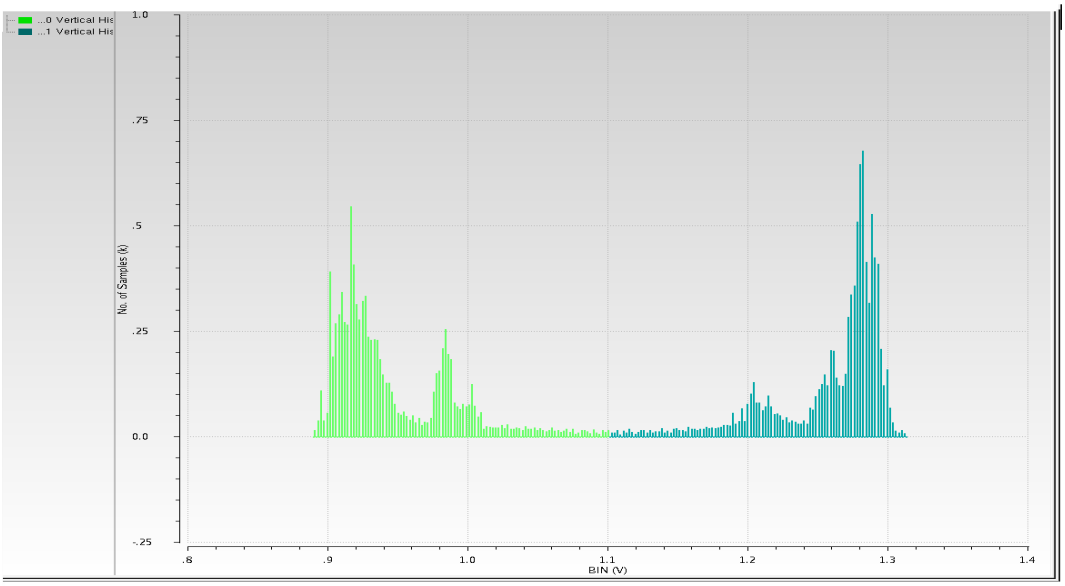
Figure 5.21: Eye Diagram of the simulated 640 Mbit/s PRBS. I_s = 4mA, the lenght of the mtline is set to L = 50cm and the parasitic components are $Ln1 = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$. Simulation time 1 μs.

- Logic level 0 lies in $(-0.253 \pm 0.16)V$;
- Eye Amplitude is 503 mV ;
- Eye Height is 478 mV;
- Eye Width is 1.53 ns
- Rise Time is 276 ps
- Fall Time is 271 ps

However, the large receiver input common mode allows to obtain an output of the transceiver which have the desired eye amplitude, also if the total jitter amount is relatively high, like in the previous case.

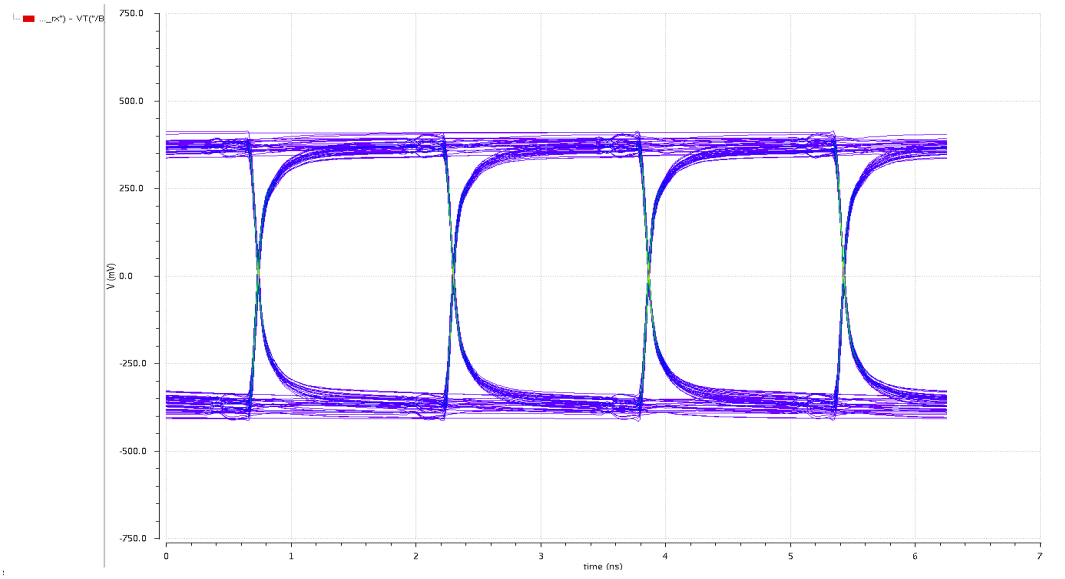


(a) Eye Diagram of the simulated 640 Mbit/s PRBS

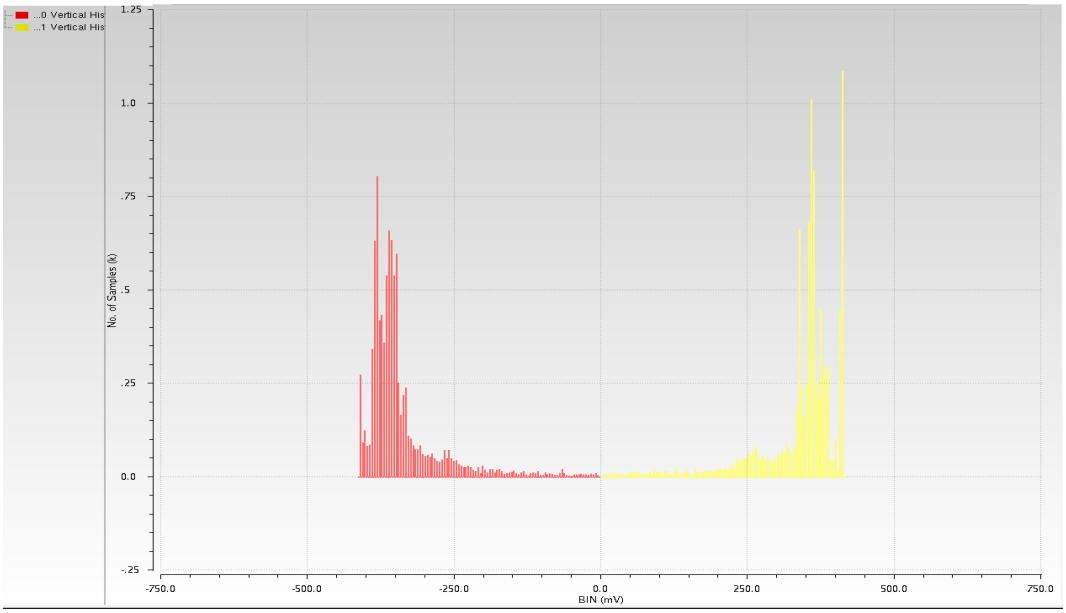


(b) Vertical Histograms - The number of Bins is 100

Figure 5.22: In this simulation the transmission rate is 640 Mbit/s, I_s = 4mA, the lenght of the mtline is set to L = 50cm and the parasitic components are $Ln1 = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$. Simulation time 1 μs



(a) Eye Diagram of the difference between the driver outputs



(b) Vertical Histograms - The number of Bins is 100

Figure 5.23: In this simulation the transmission rate is 640 Mbit/s, I_s = 4mA, the lenght of the mtline is set to L = 50cm and the parasitic components are $Ln1 = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$. Simulation time 1 μs

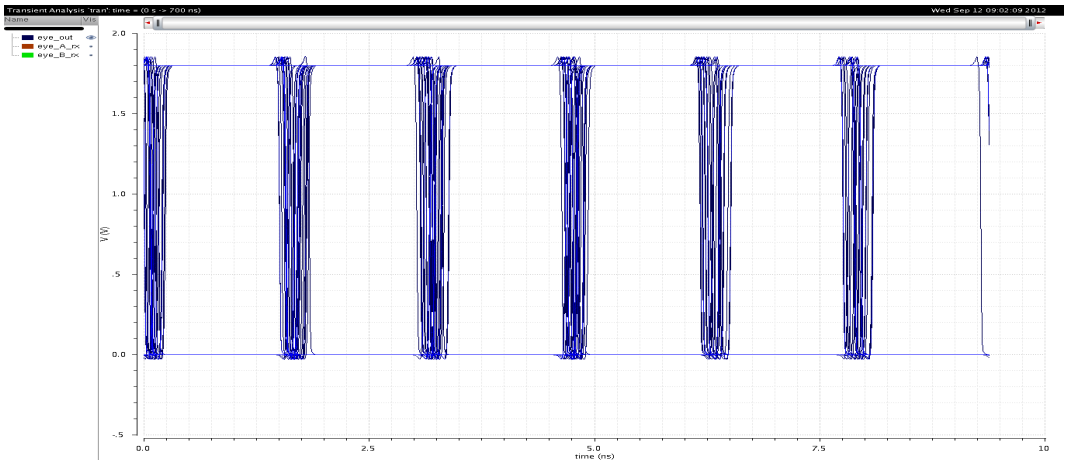


Figure 5.24: In this simulation the transmission rate is 640 Mbit/s, $I_s = 4$mA, the lenght of the mtline is assumed L = 50cm and the parasitic effects are $Ln1 = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$. Transient time 600 ns.

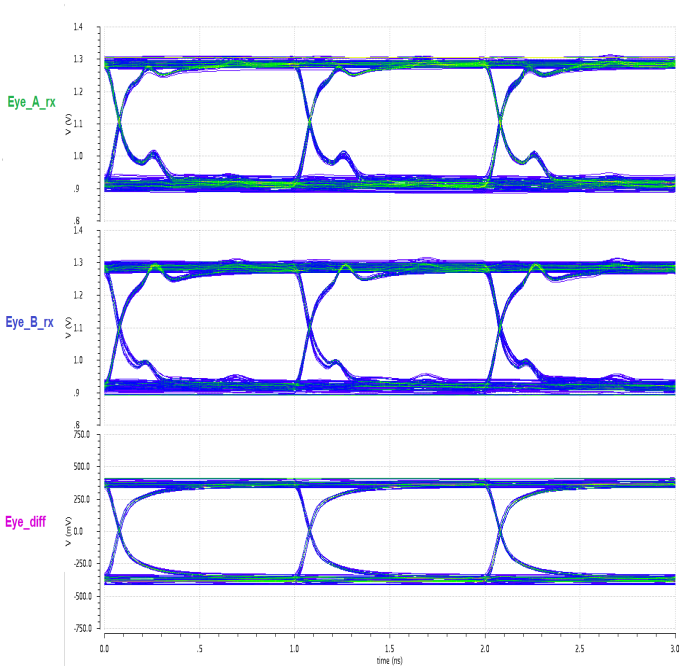


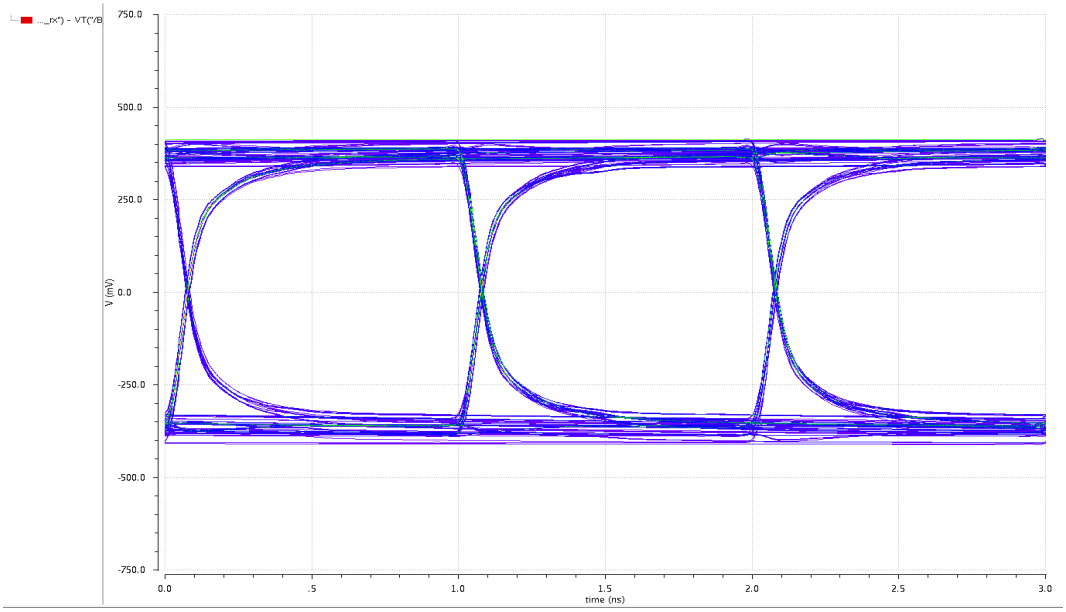
Figure 5.25

5.5.3 1 Gbps input data stream

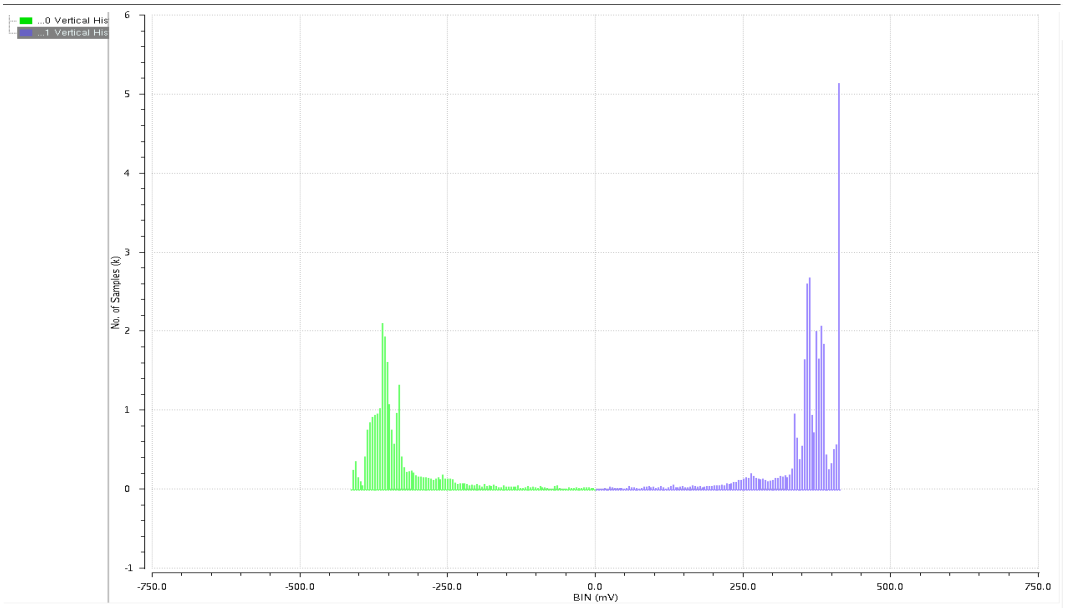
Finally, we simulated a 1 Gbps PRBS since this will be the transmission rate required in the new ITS. Here the ringing of the output signals is more evident, even if the eye diagrams are not so closed.
By isolating the difference between the Transmitter 2 outputs, the total peak-to-peak jitter is about 21 ps whereas the eye has the following characteristics:

- Logic level 1 lies in $(0.30 \pm 0.14)V$;
- Logic level 0 lies in $(-0.25 \pm 0.14)V$;
- Eye Amplitude is 604 mV ;
- Eye Height is 197 mV;
- Eye Width is 1 ns;
- Rise Time is 247 ps;
- Fall Time is 267 ps;

Also if the eye amplitude differs from the nominal value of 800 mV, it is compatible with the eye amplitude estimated in the two previous cases. Furthermore, we can underline that the transition threshold between the two logic levels remains always 0 V, although the rise time and the fall time of the eye diagram vary slightly . Regarding the output transceiver eye diagram, the same behaviour of the two previous cases can be observed, even if the total jitter here is larger (Fig 5.27).



(a) Eye Diagram of the difference between the driver outputs



(b) Vertical Histograms - The number of Bins is 100

Figure 5.26: In this simulation the transmission rate is 1 Gbit/s, I_s = 4mA, the lenght of the mtline is set to L = 50cm and the parasitic components are $L_{n1} = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$. Simulation time 1 μs

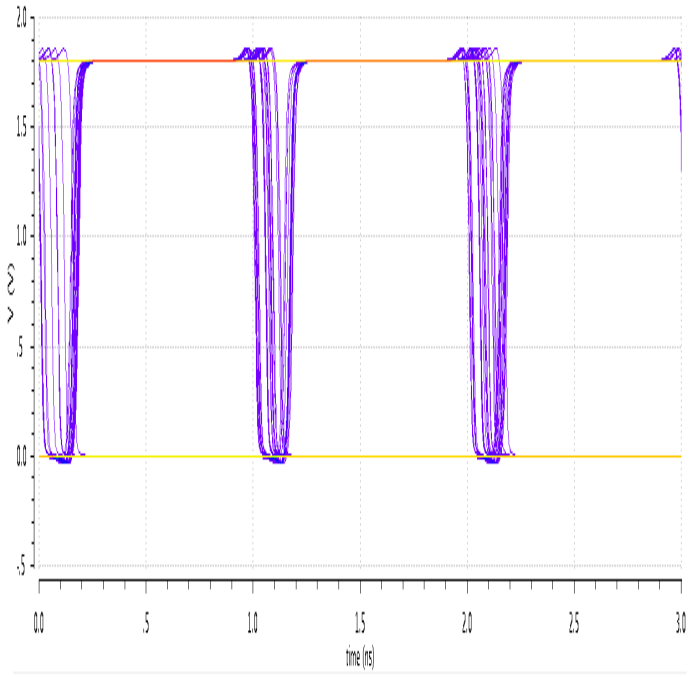


Figure 5.27: In this simulation the transmission rate is 1 Gbit/s, I_s = 4mA, the lenght of the mtline is set to L = 50cm and the parasitic components are $L_{n1} = L_{n2} = 1.5nH$, $C_1 = C_2 = 250fF$, $C_3 = C_4 = 600fF$. Simulation time 1 μs

Conclusions

In this thesis, a LVDS data transmission system was designed and simulated in a 0.18 μm CMOS technology. The peculiarity of the process employed is that it is optimized for the fabrication of complex CMOS sensors. Provided by TowerJazz, this technology has been chosen as baseline in the R&D for the upgrades of the silicon tracker of the ALICE experiment at CERN.

Two different designs were considered for the LVDS driver. The first scheme (called Transmitter 1) employs the same topology which has been used at CERN to implement LVDS drivers in 0.25 μm and 0.13 μm. The circuit uses only NMOS transistors as switches to maximize the switching speed, taking advantage of the availability of zero-threshold devices in the two processes in which it was implemented. The common mode output level is defined with a replica bias circuit. In the original implementations, the device was powered at 2.5 V. Several issues were identified when porting this circuit in the 0.18 μm process of interest.

The aim of our design was in fact to have a circuit that can be powered by a power supply of 1.8 V. This will be in fact the standard power supply of the target technology. To simplify the power distribution network it is important that also the I/O can be powered at the same voltage that will be used by the rest of the chip. Furthermore, this allows to use only thin oxide transistors, which are less sensitive to radiation damage. On the other hand it is desirable to maintain the output common mode voltage close to 1.2 V, which allows also interface easily the custom-designed driver with commercial receivers.

The reduction of the power supply voltage from 2.5 V to 1.8 V made the design of Transmitter 1 not suitable for high speed operation. A transmission speed of 320 Mbit/s could hardly be achieved, while operation at higher speeds was not satisfactory.

A different design, called Transmitter 2, was then considered. This circuit is based on the design presented in [25]. Transmitter 2 draws a current which ranges from 2.5 mA to 4 mA, thus the voltage swing produced at the end of the termination resistors lies in the range (250-400) mV when the supply

voltage is 1.8 V.
The driver makes use of CMOS inverter for current steering. A transconductor is also added to limit the ringing and the overshoot at the output.
The common mode level is defined by a common mode feed-back circuit made of a simple differential amplifier and a resistive network.

A receiver that converts the LVDS signal back to CMOS levels was also designed. The circuit employs a topology widely used in LVDS receivers. It consist of a self biased differential pair with a rail-to-rail common mode input range.

The full chain was simulated and studied with the eye diagram method, which is the standard approach to qualify a data transmission system. Simulations were done with different input patterns, both deterministic (square waves) and pseudo-random. A model of the transmission line connecting the transmitter and the receiver was also introduced to have simulations as realistic as possible. The performance of the chain were then studied under different conditions. In particular, the effects of process and temperature variations were examined in detail.

The proposed driver circuit called Transmitter 2 is adequate to transmit data up to a rate of 1 Gbit/s whilst further improvements are desirable to minimize the deterministic jitter in the receiver which is the largest component of the total jitter. However it must be pointed out that on the sensor chip the receiver will only process the low frequency data (below 40 MHz), so the present design is already adequate. The transmission line model employed is however a first approximation, since a model of the cable that will be used in the final system is not yet available.

This work has created a framework in which the design of the proposed transmission system can be quickly finalized. The next steps should be the verification of the circuit performance with the final transmission line model and the design of the mask layout for circuit production.

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