Università degli Studi di Torino

Facoltà di Scienze M.F.N.

Corso di Laurea in Fisica
delle Tecnologie avanzate

Tesi Magistrale

A Charge and Time Encoder for the Microstrip Sensors of the $\overline{\text{PANDA}}$ Experiment at FAIR

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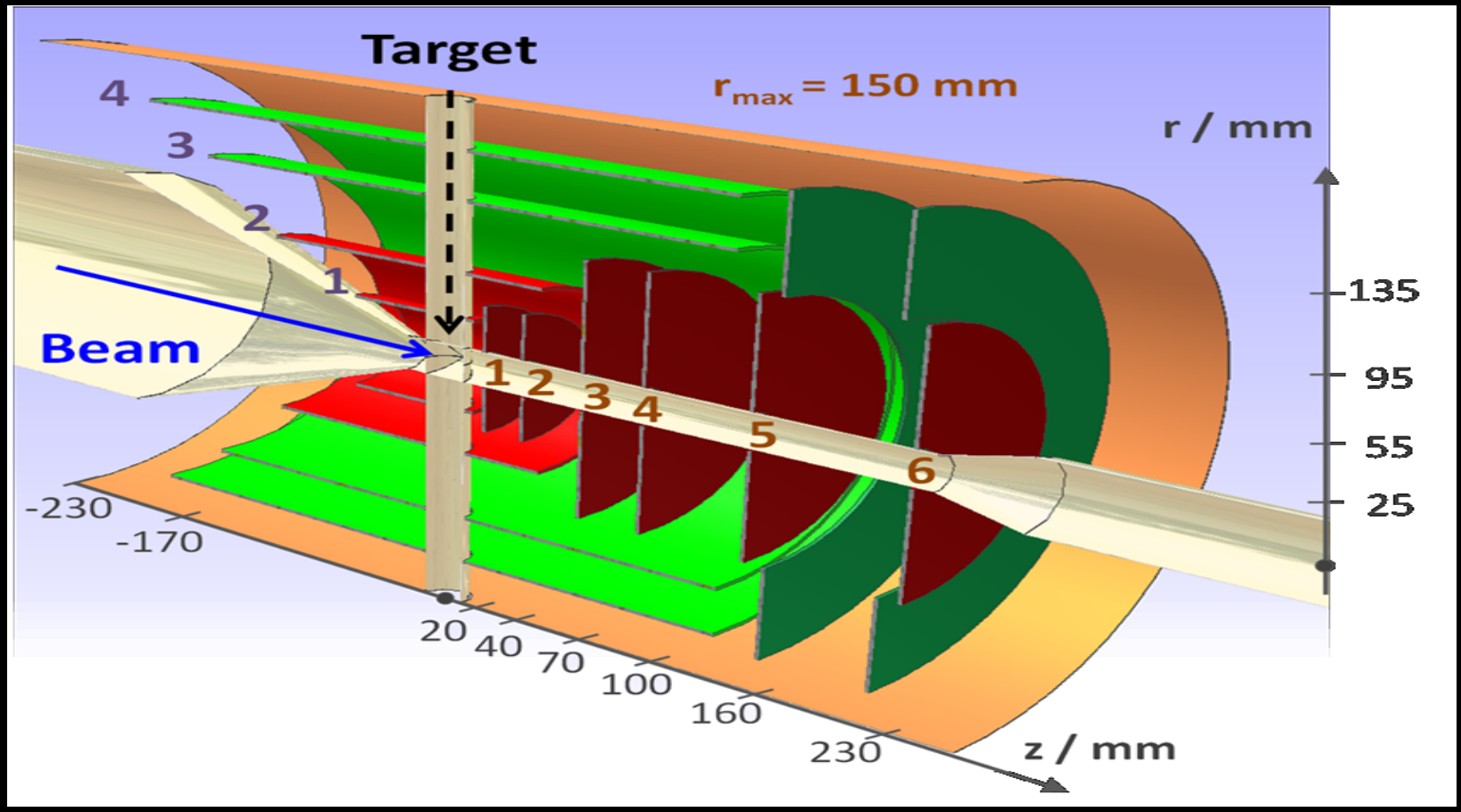
Contents

1. Microvertex Detector
2. Architectures for Strips
3. Time to Digital Converter
4. Simulations
5. Outlooks

MVD

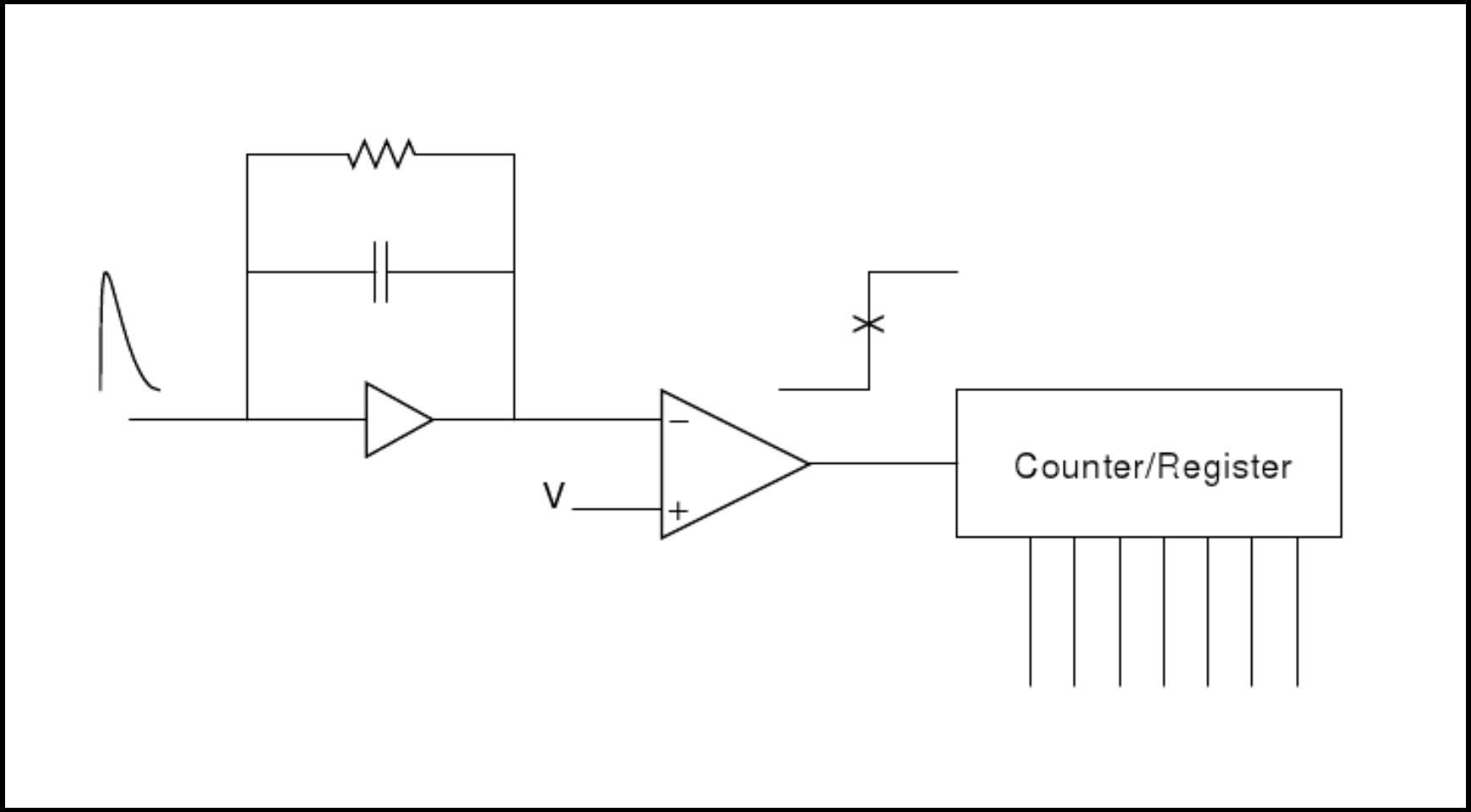


Red zone covered by pixels and green one by strips

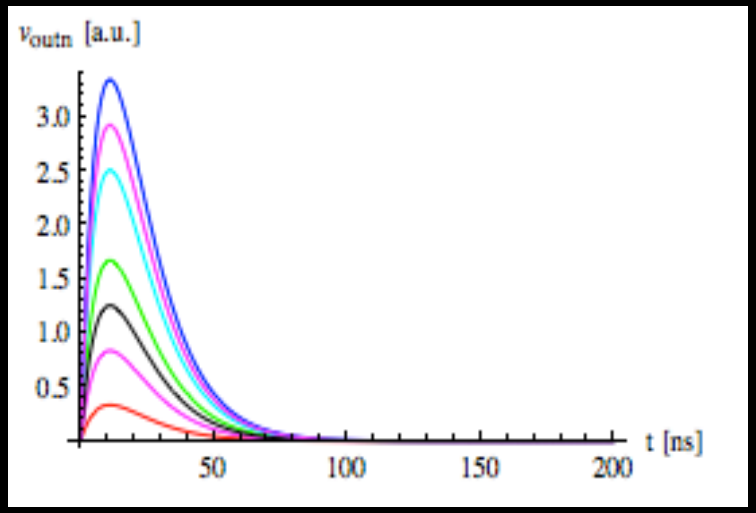
Requirements

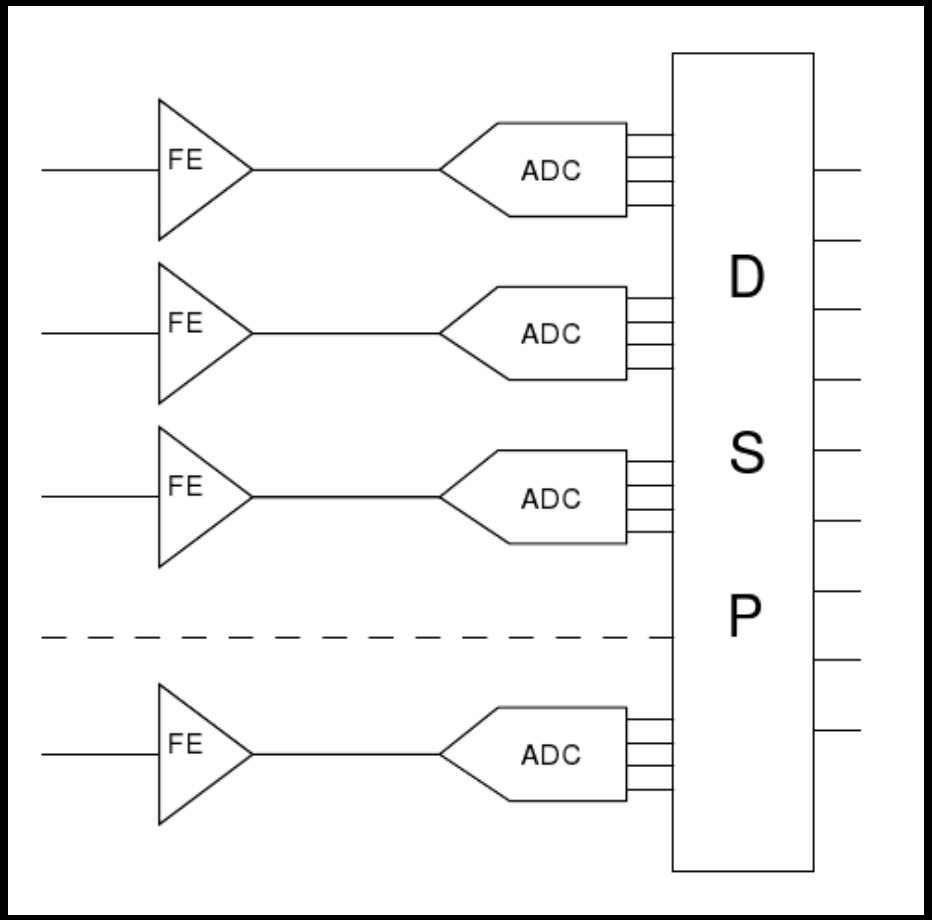
- Rate/channel ~ 30 kHz
- ~ 4 mW per channel
- 200000 channel
- **Triggerless**
- **Preserve the charge information**
- **Only digital outputs with 9 bits**

Electronics for strips: binary

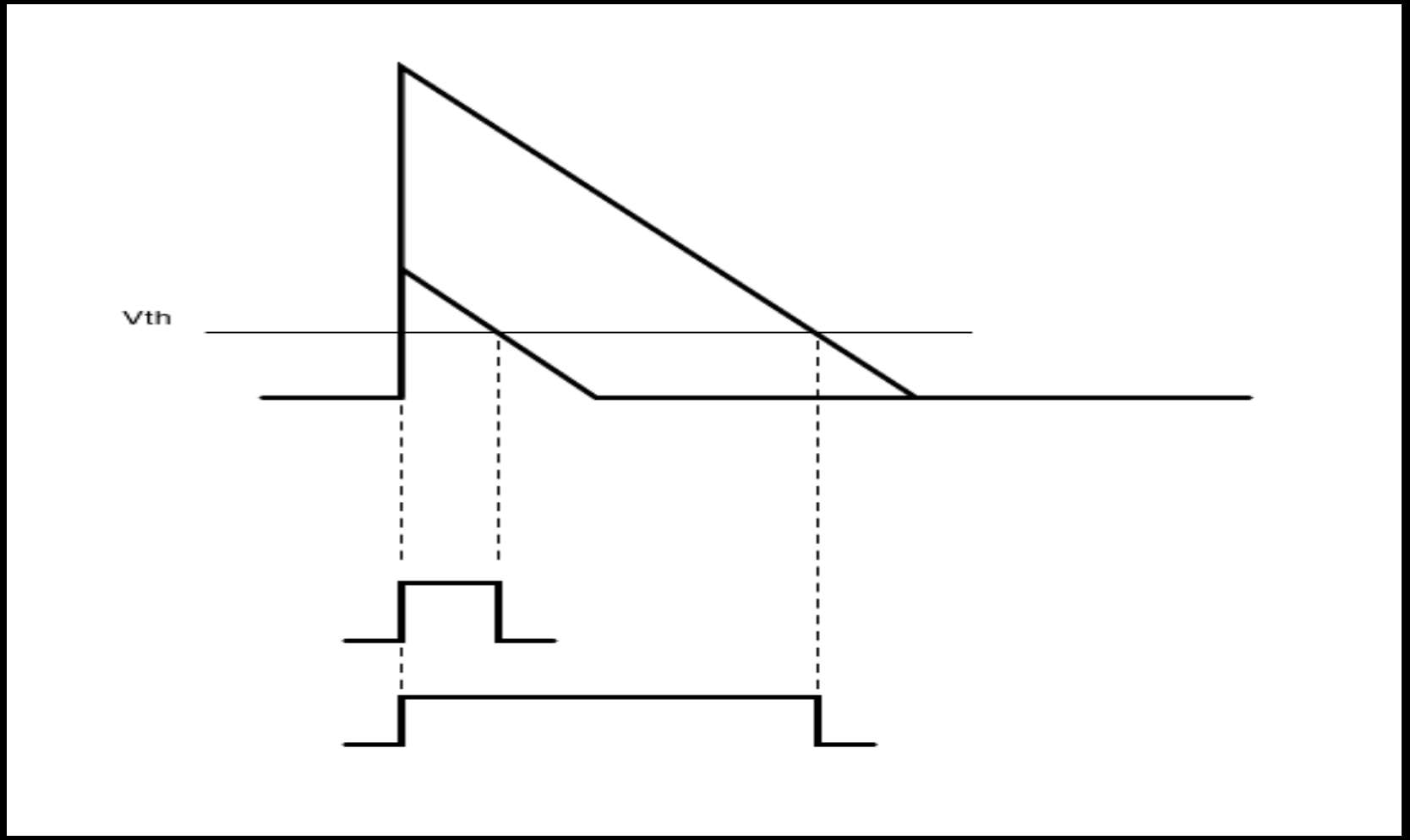


ADC

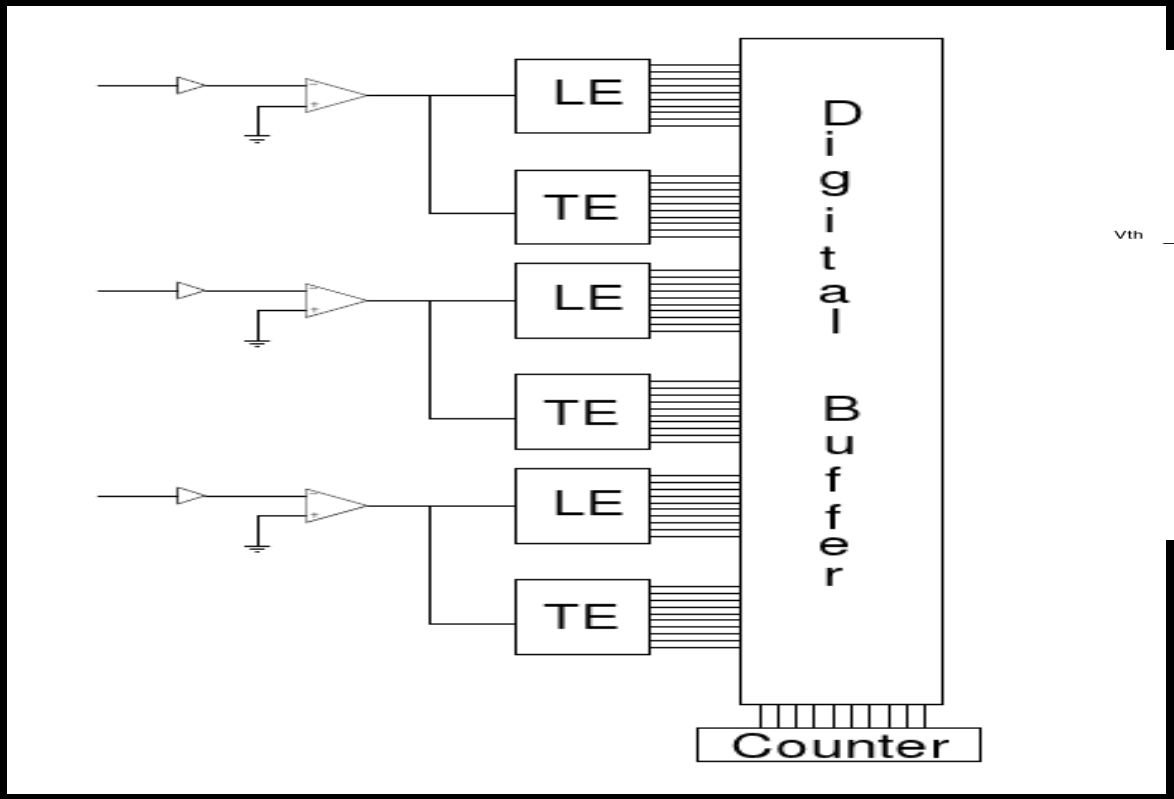

v_{outn} [a.u.]
3.0
2.5
2.0
1.5
1.0
0.5
50
100
150
200
t [ns]

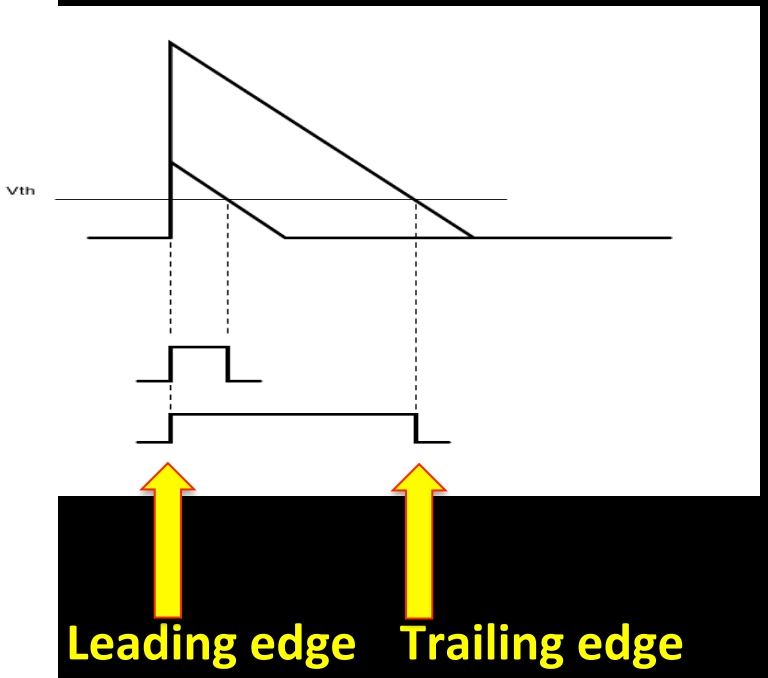

FE
ADC
FE
ADC
FE
ADC
FE
ADC
D
S
P

Time Over Threshold technique



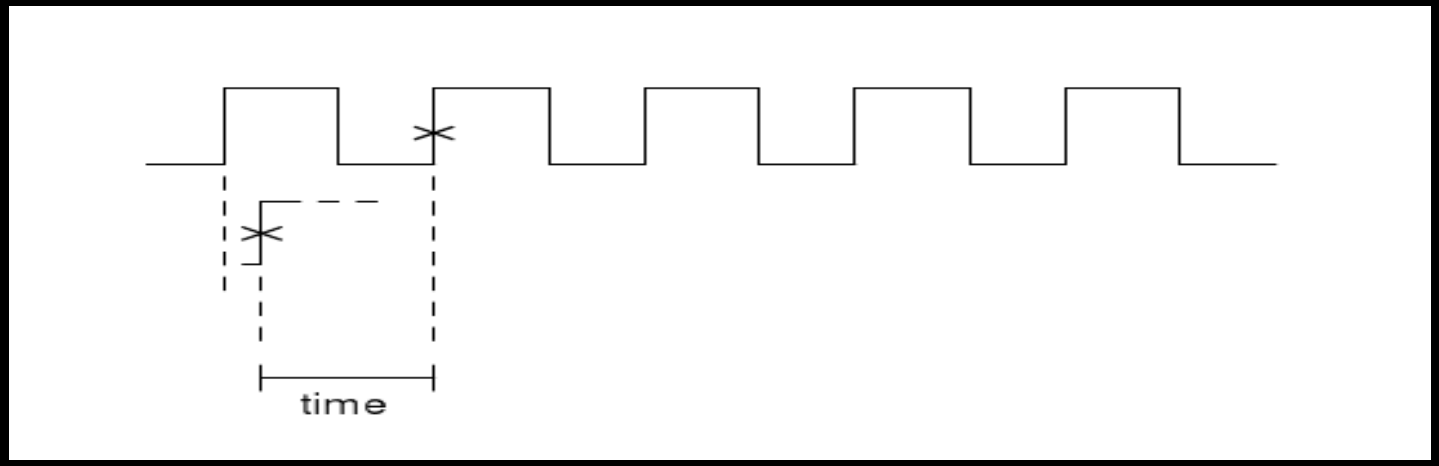
Chip architecture





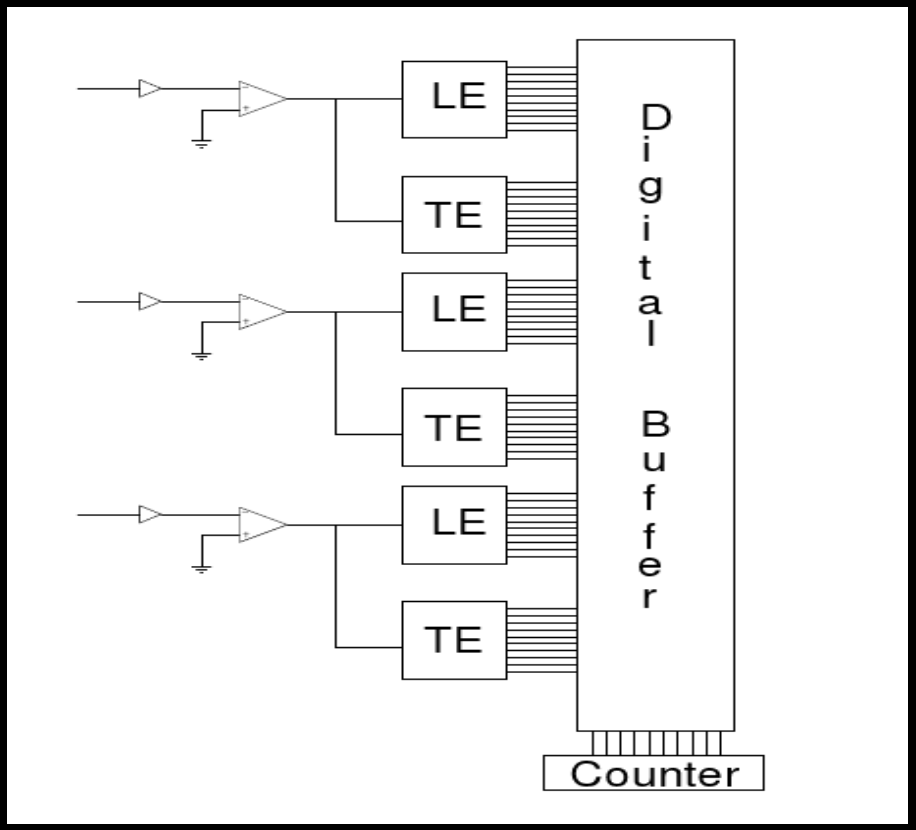
Clock resolution

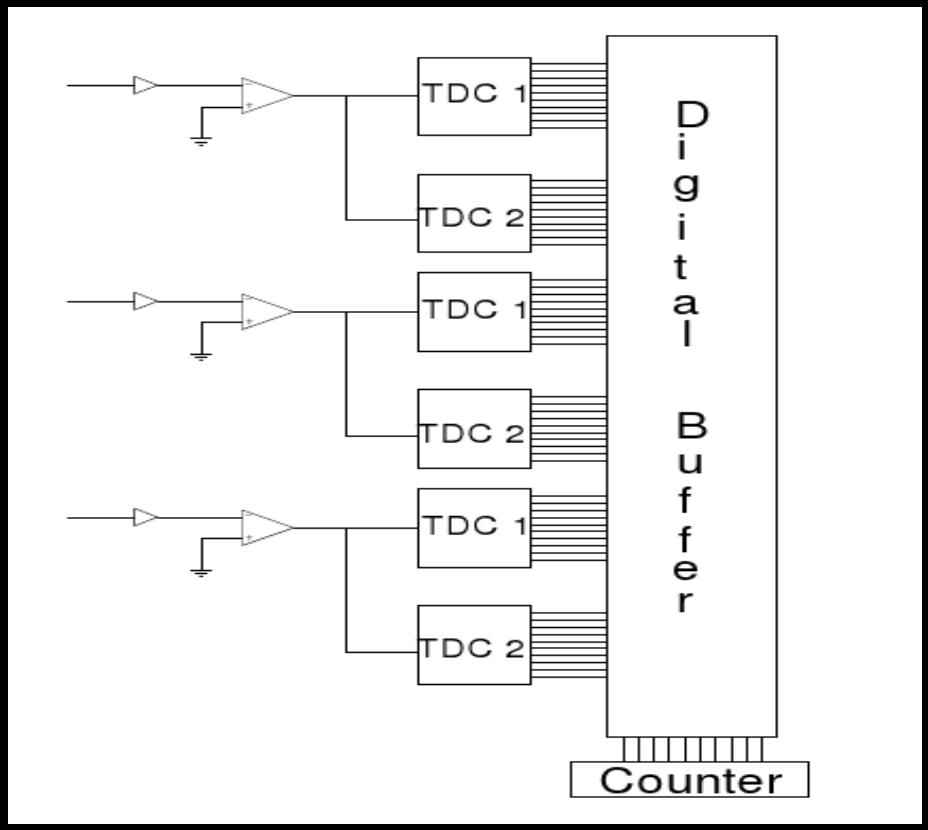
$2^9 = 512$ → 6.25ns • 512 = 3.2us



Since the rate per strip is about 30 kHz the biggest signal is exhausted in 3.2us, so we have a pile-up problem.
We want a system that has 1LSB = 400ps

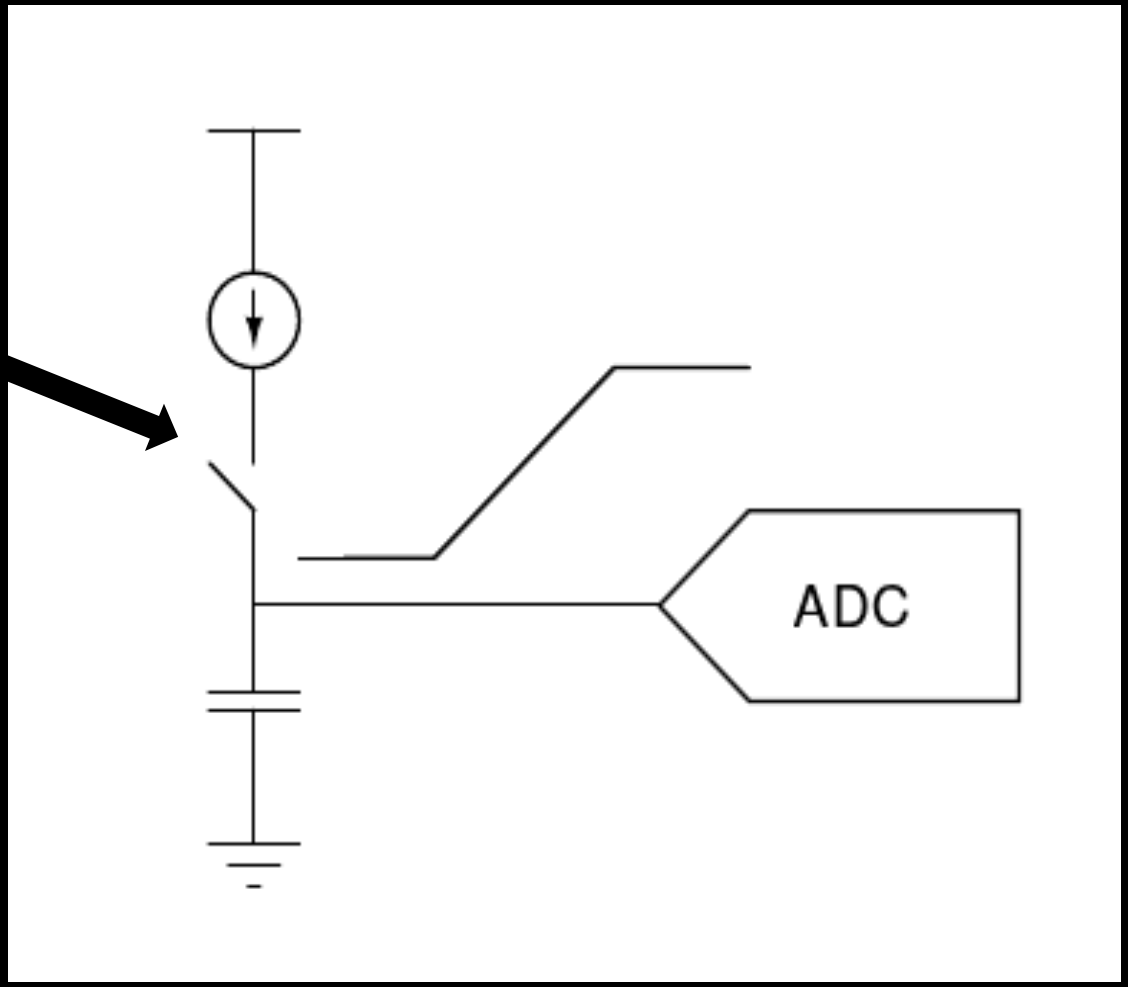
Goals





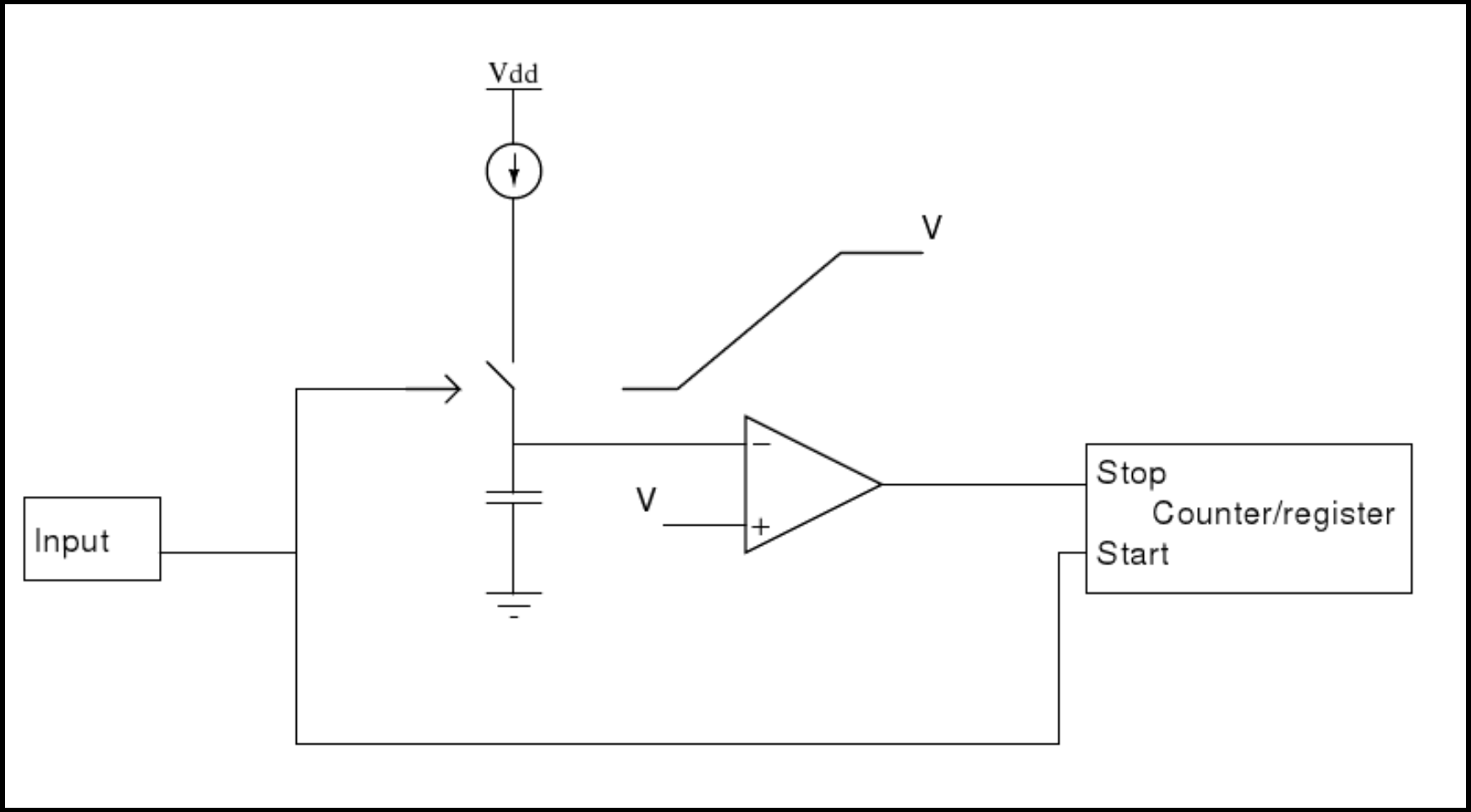
- Redesign and optimization the TDC
- Investigation about new technology

Time to Digital Converter

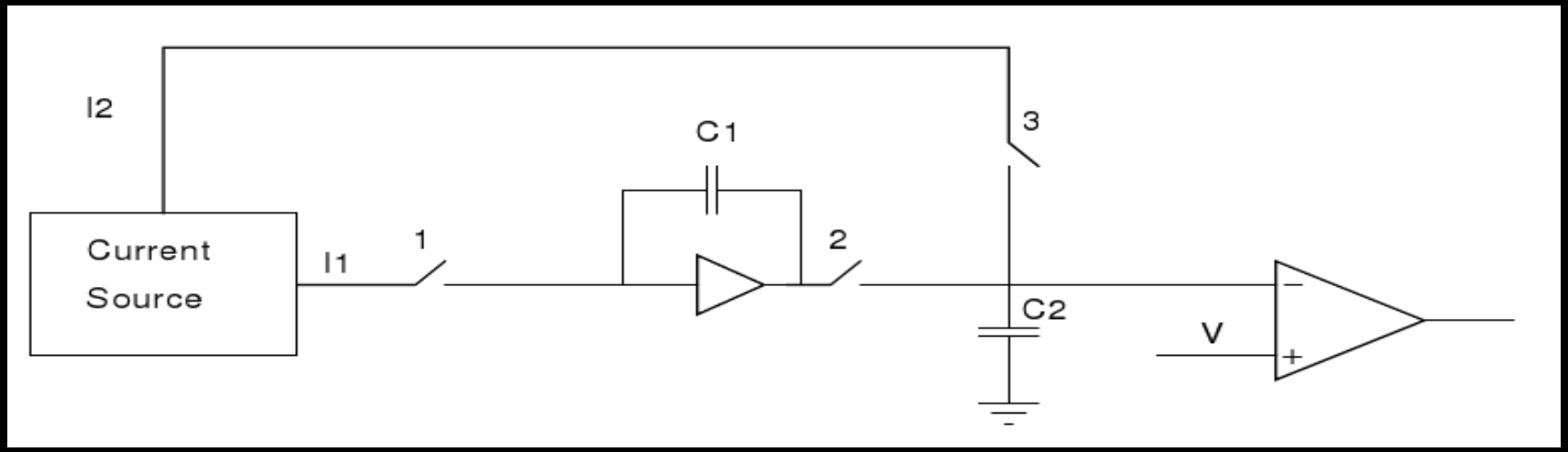


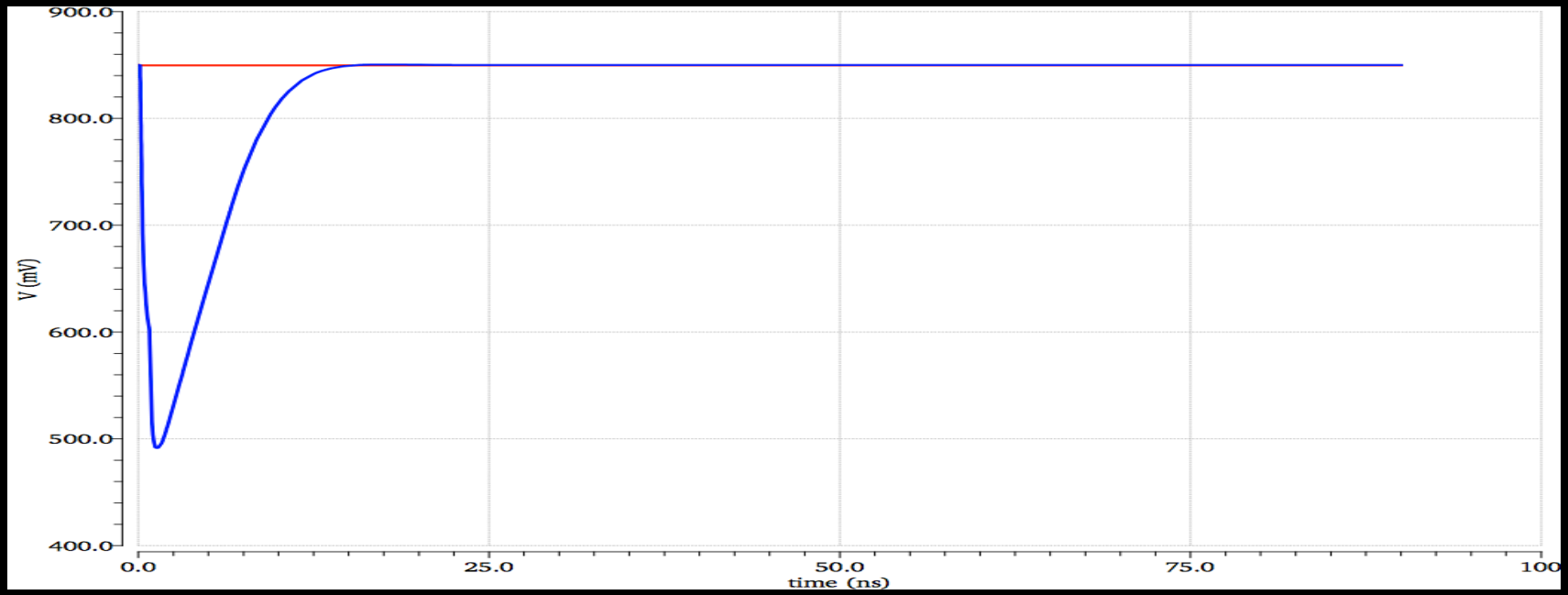
- Accurate
- Low power
- Compact
- Slow

Wilkinson ADC

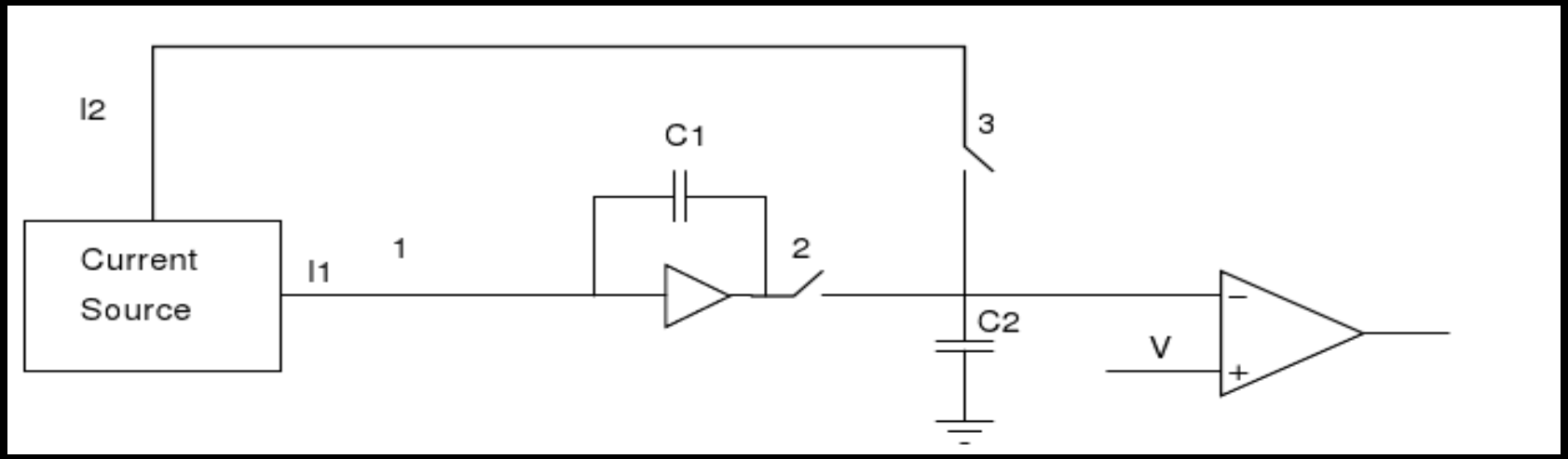


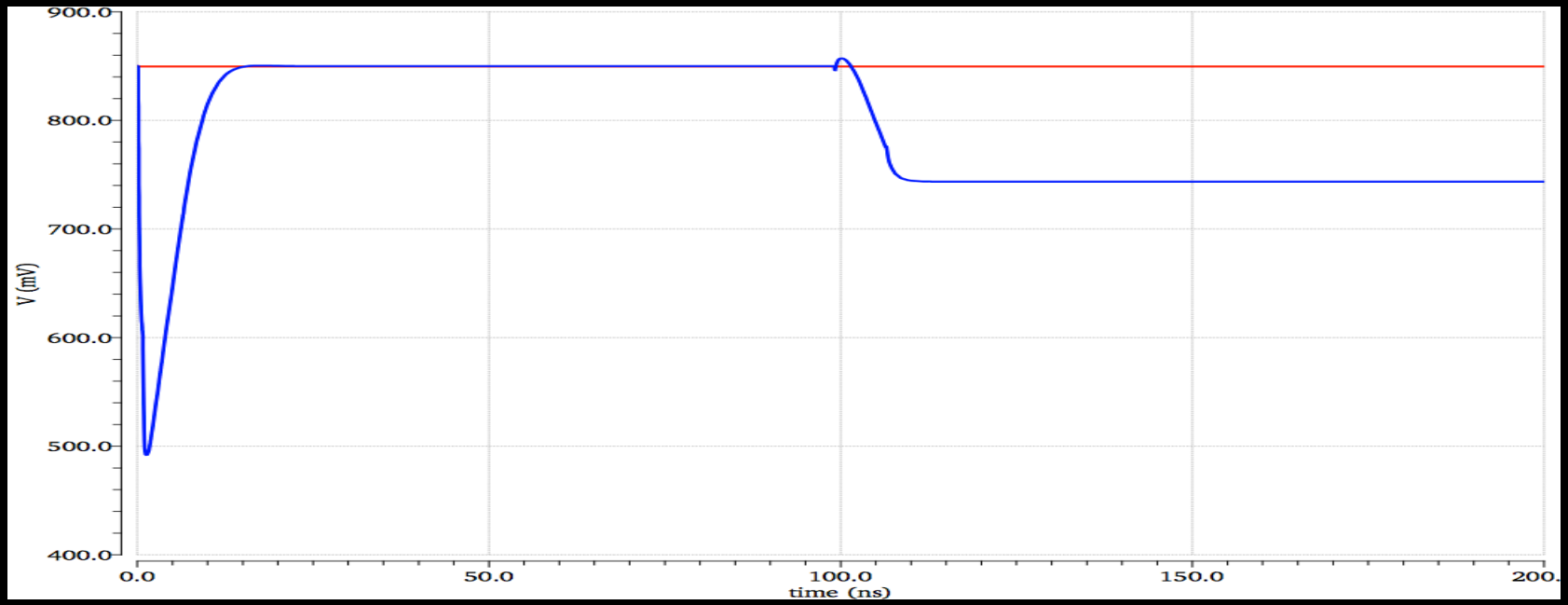
TDC implementation



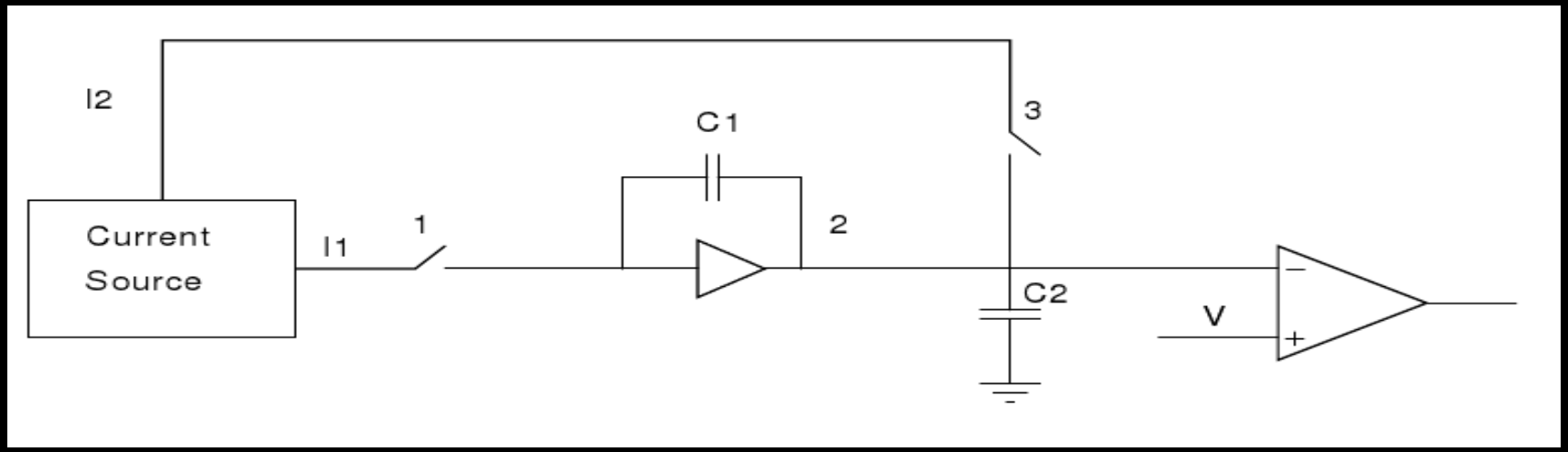


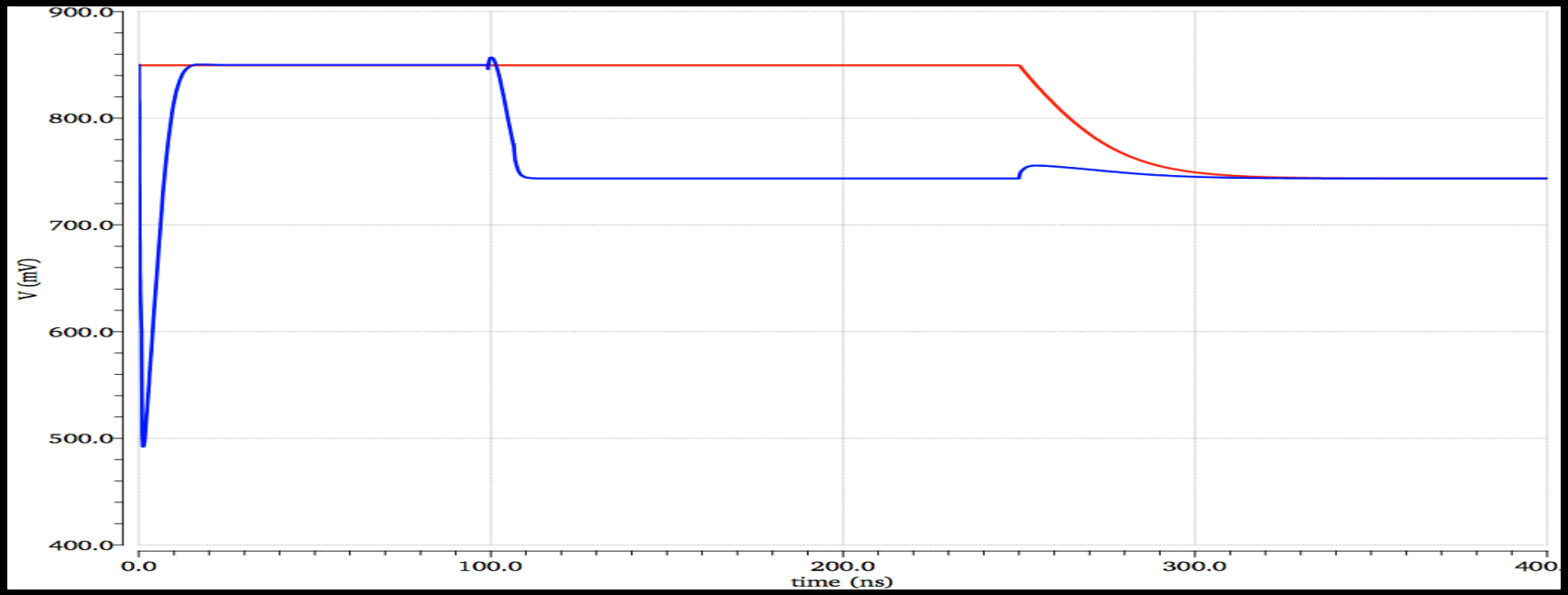
TDC implementation



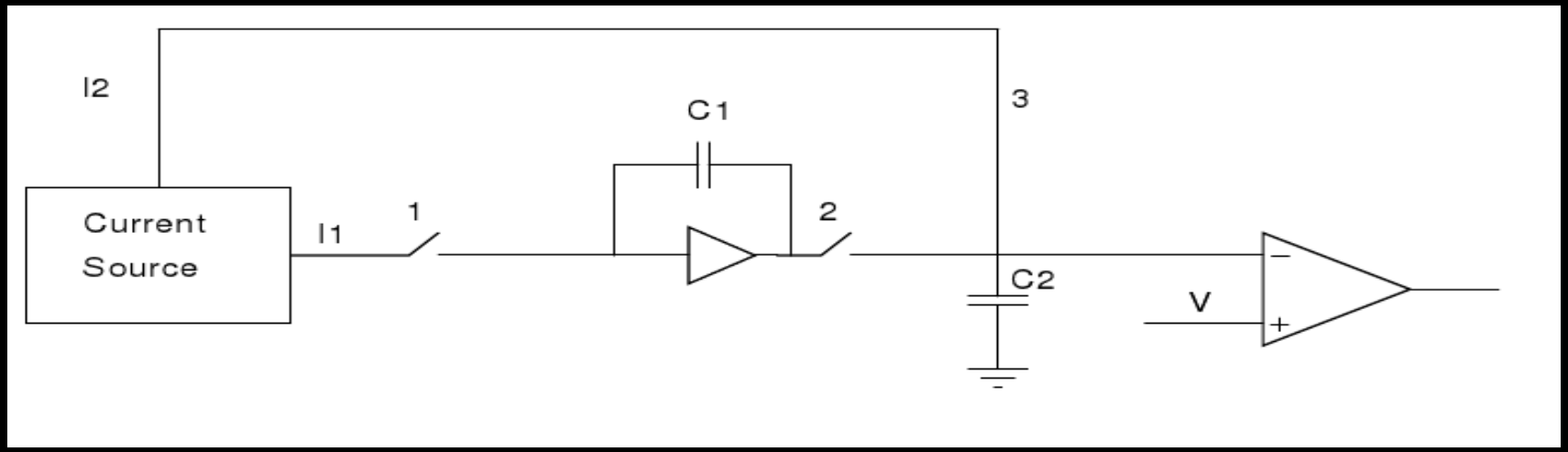


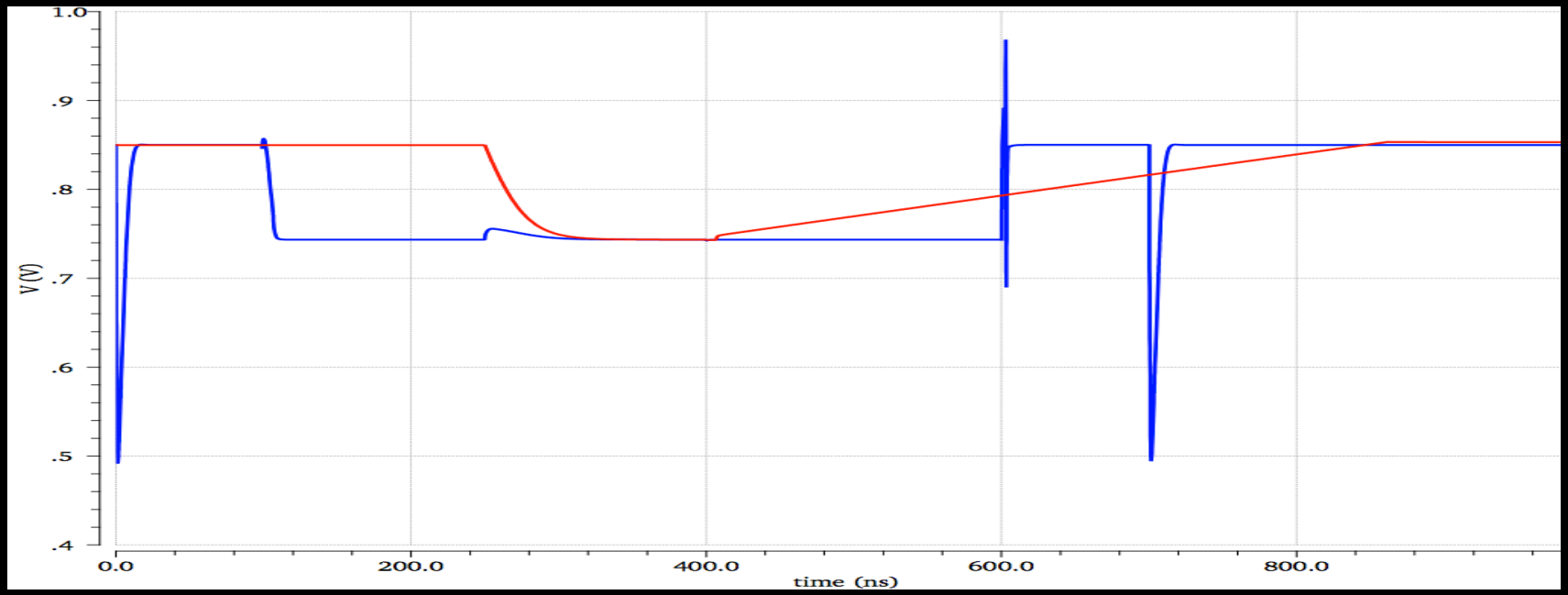
TDC implementation



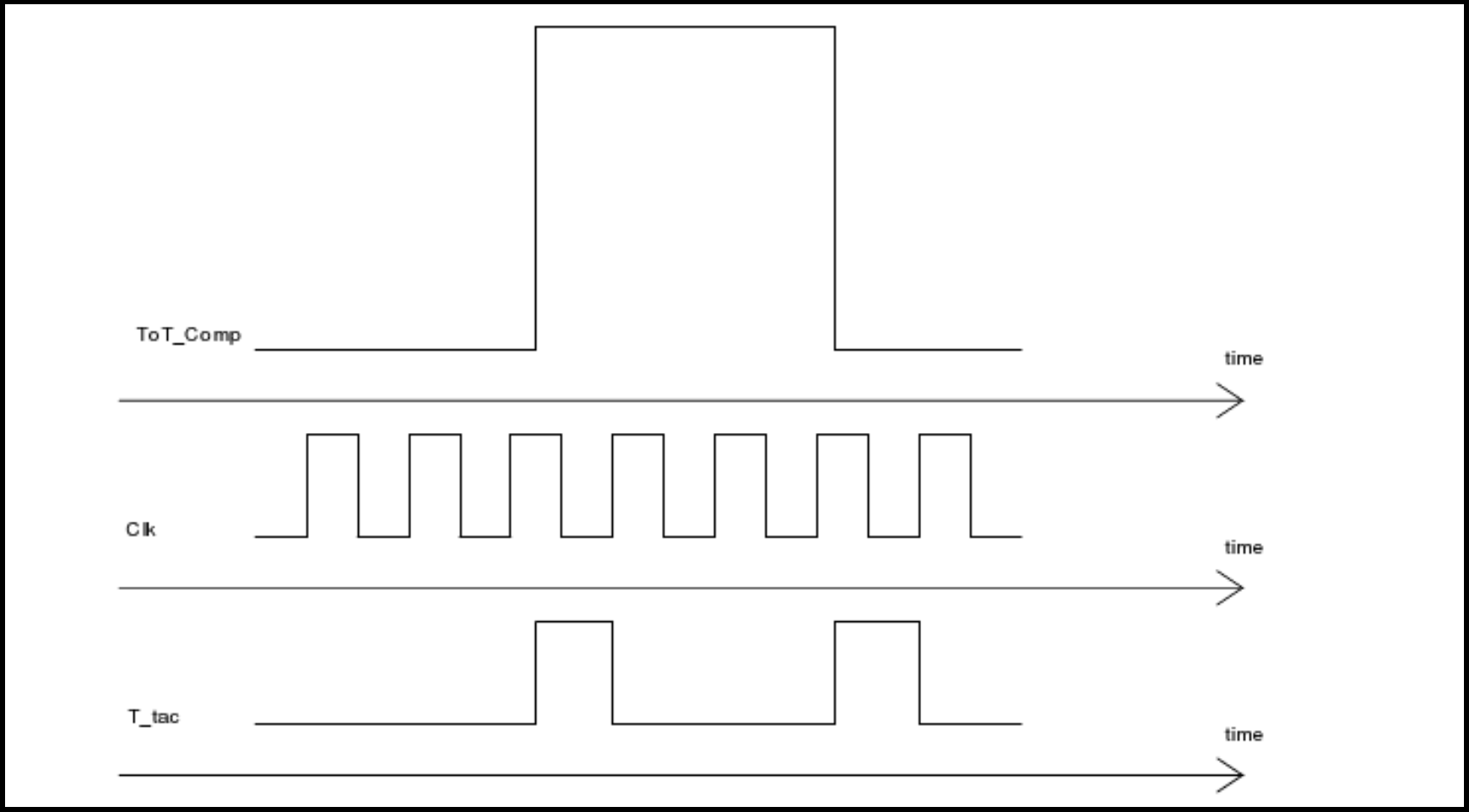


TDC implementation



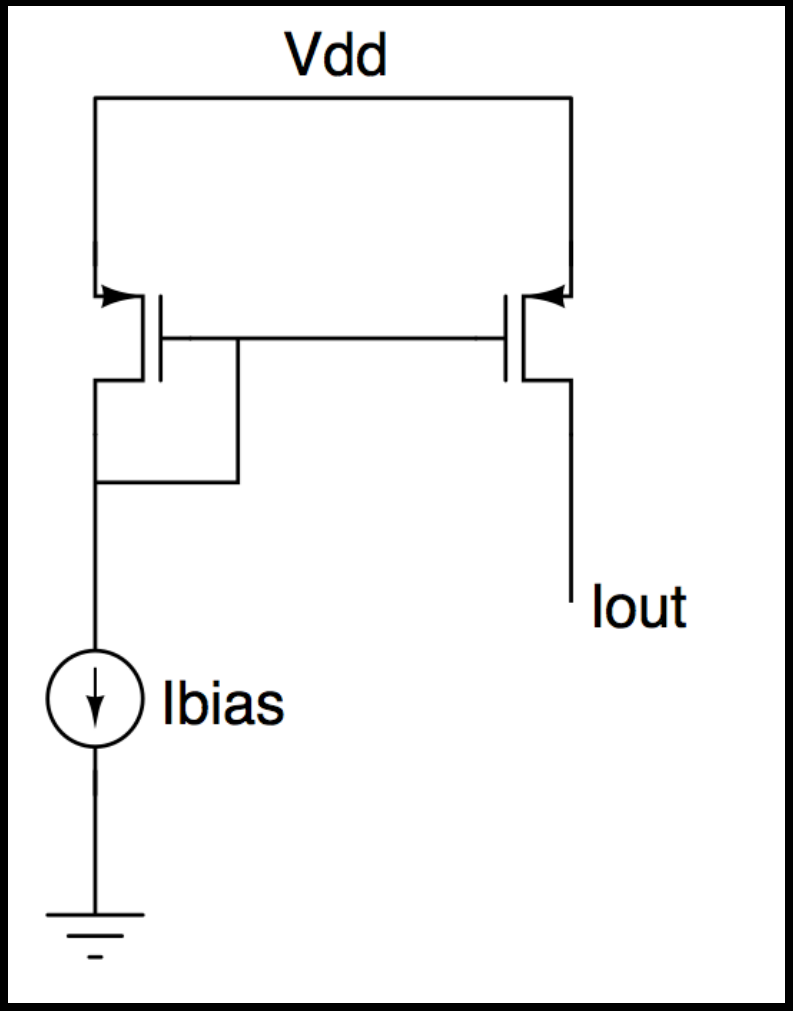


Timing



With this system we obtain that 1LSB = 49ps, since we have 6.25ns/128

Current Mirror



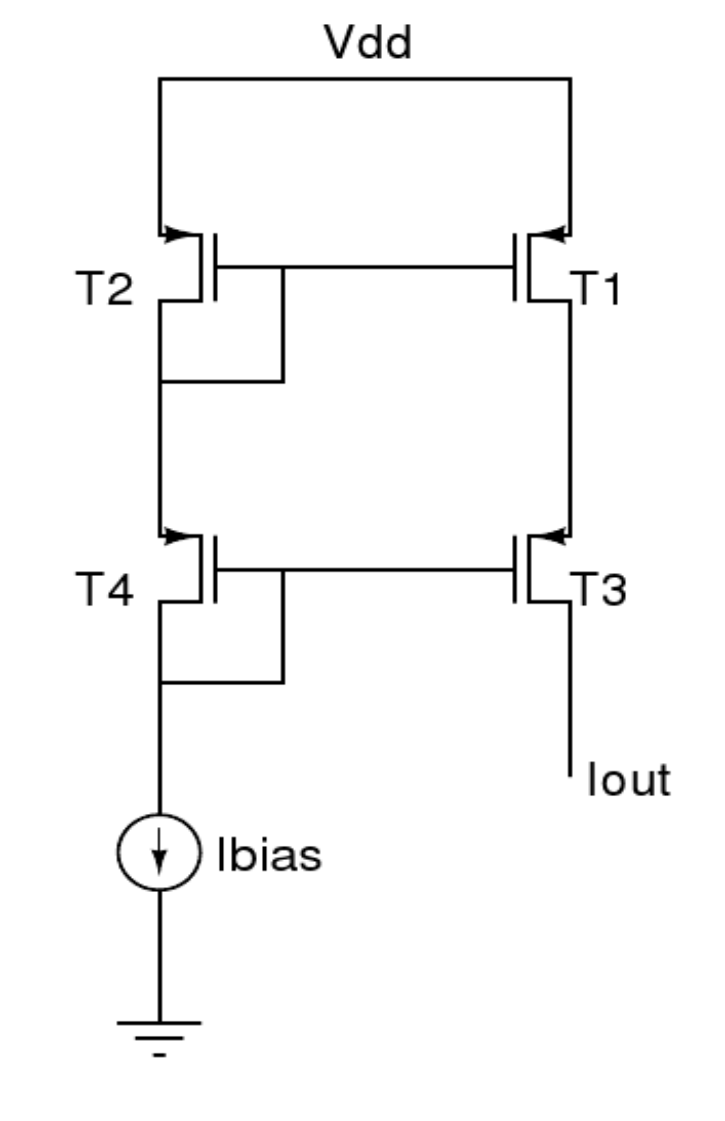
$$2^9 = 512 \rightarrow 1LSB = \frac{1}{512} \approx 2‰$$

For a nominal current of 500nA the 2‰ is 1nA

$$r_{out(th)} = \frac{\Delta v}{\Delta i} \approx 400M\Omega$$

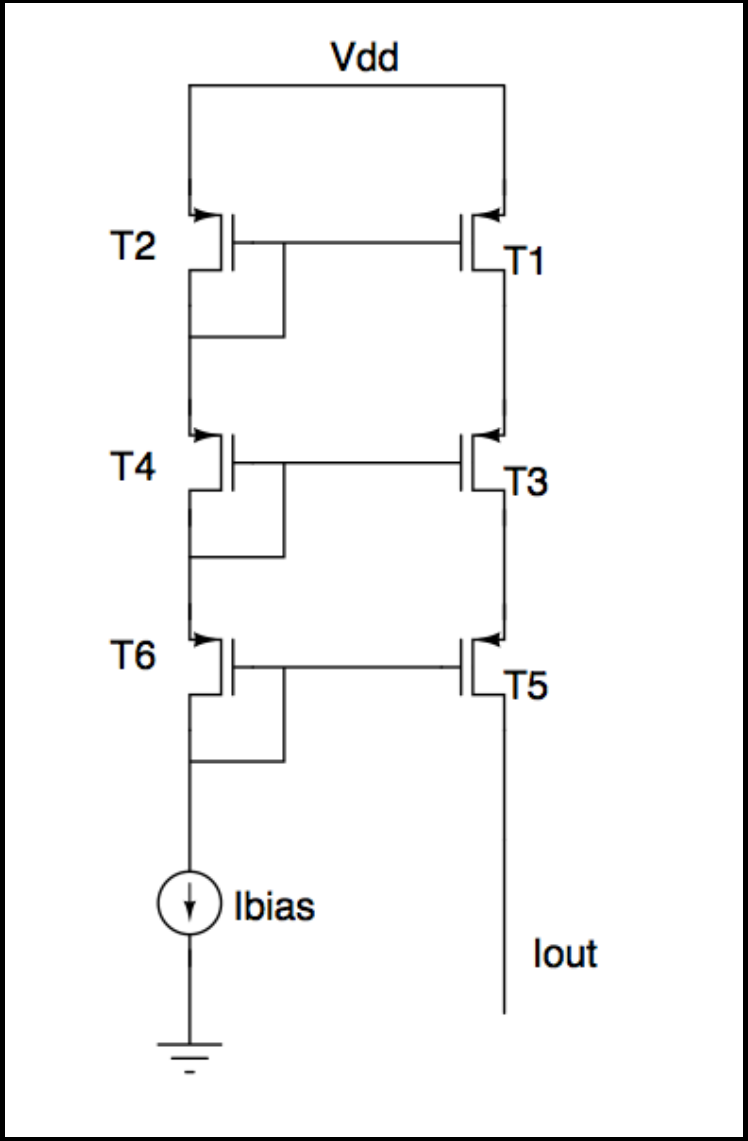
$$r_{out} \cong \frac{1}{g_{ds}} \cong 20k\Omega$$

Cascode current mirror



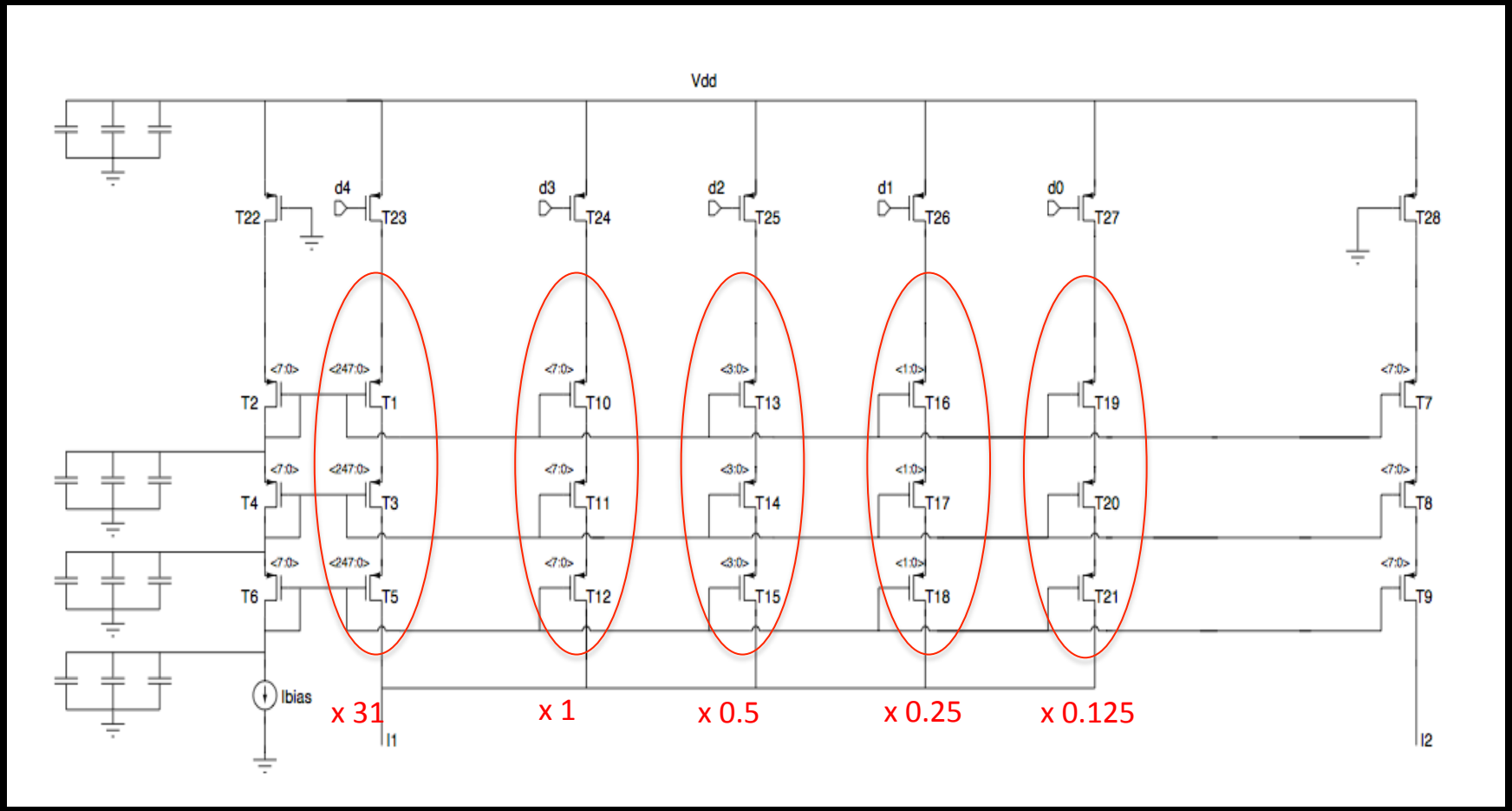
$$r_{out1} \approx g_{m3} r_{03} r_{01} \approx 20 M\Omega$$

Double cascode current mirror

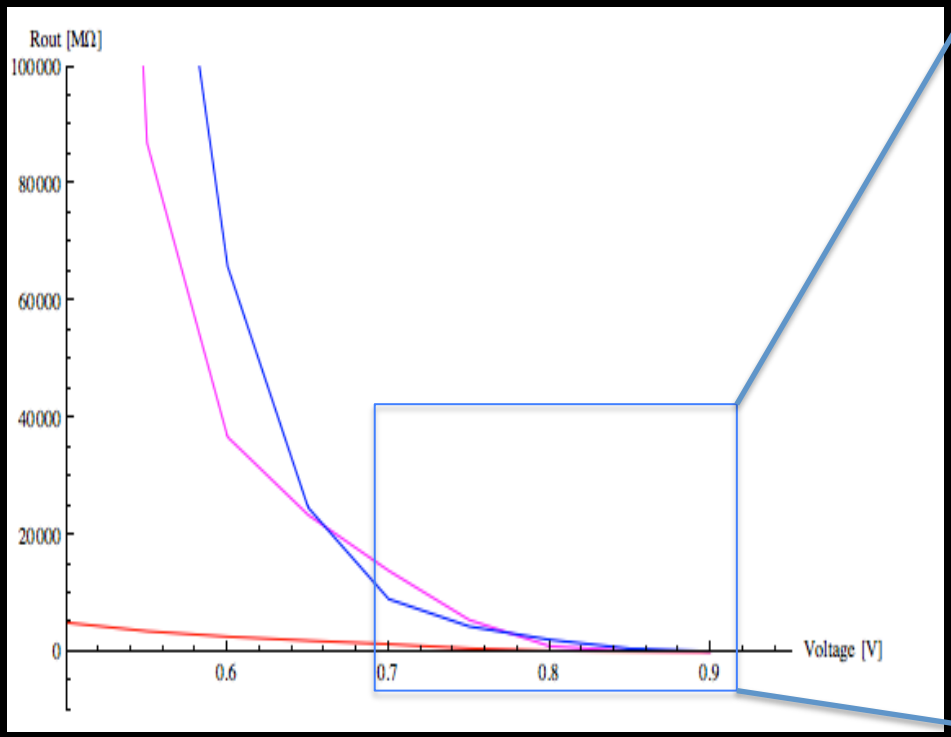


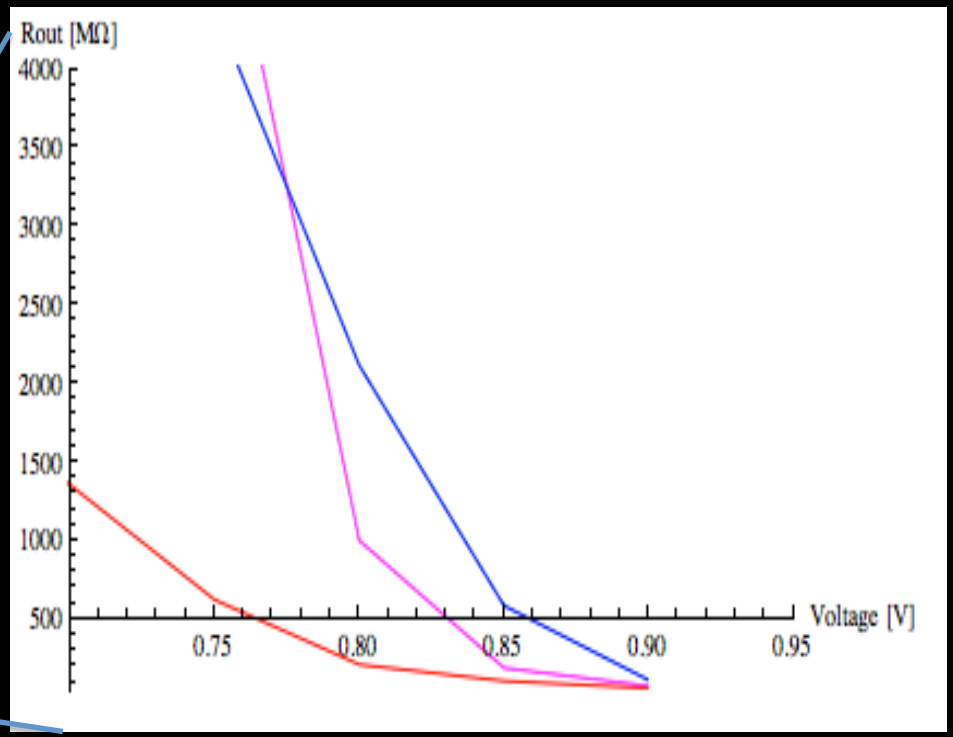
$$r_{out} \approx g_{m5} r_{05} r_{out1} = g_{m5} r_{05} g_{m3} r_{03} r_{01} \approx 550 M\Omega$$

Transistor level implementation

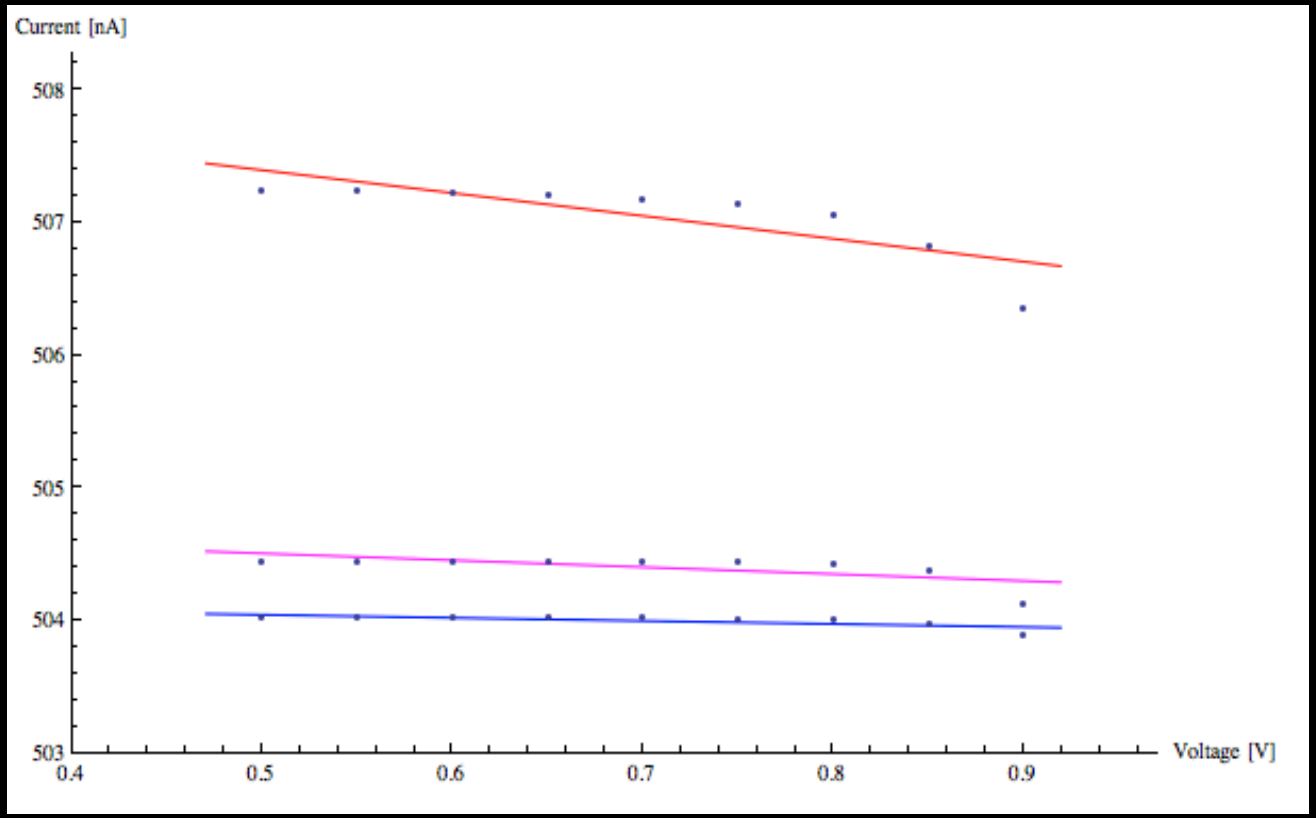


Costant Current Source: I_2



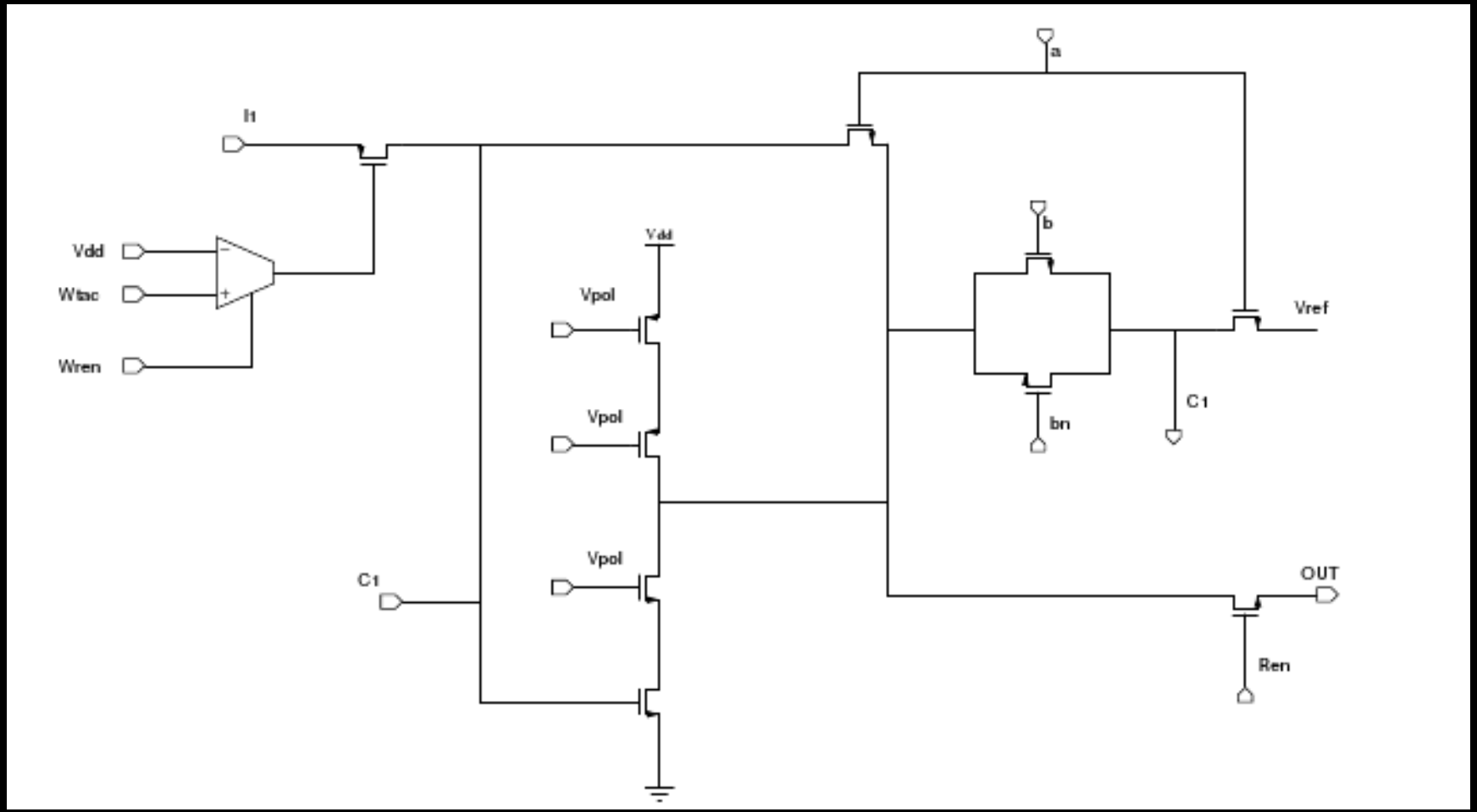


Costant Current Source: I_2 (2)

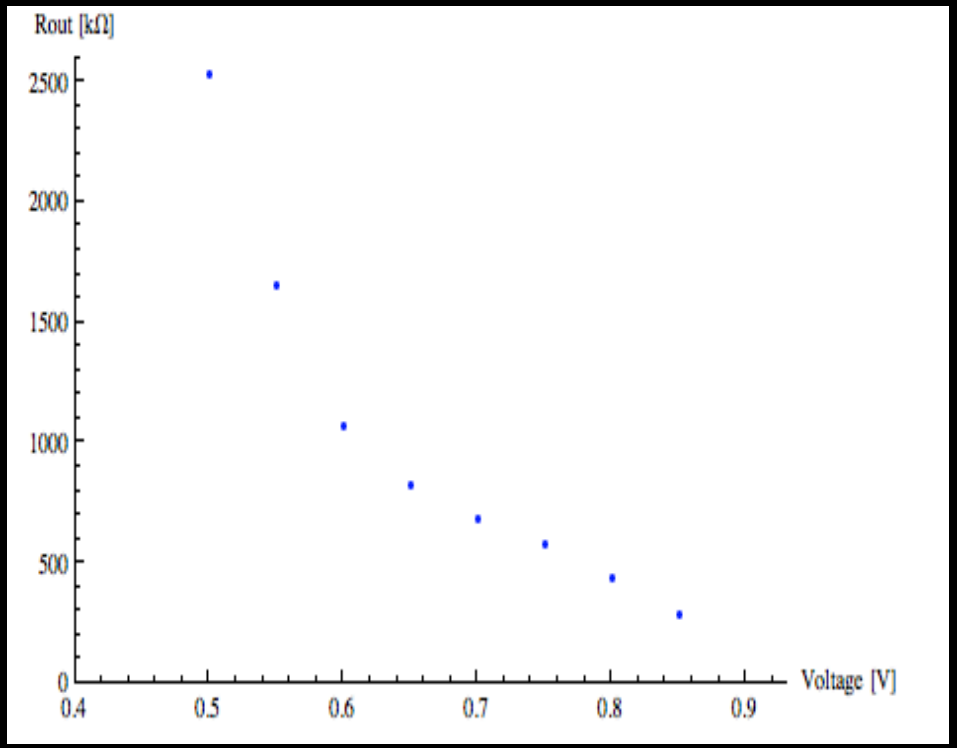


Nominal	0.408‰
FF	0.176‰
SS	1.360‰

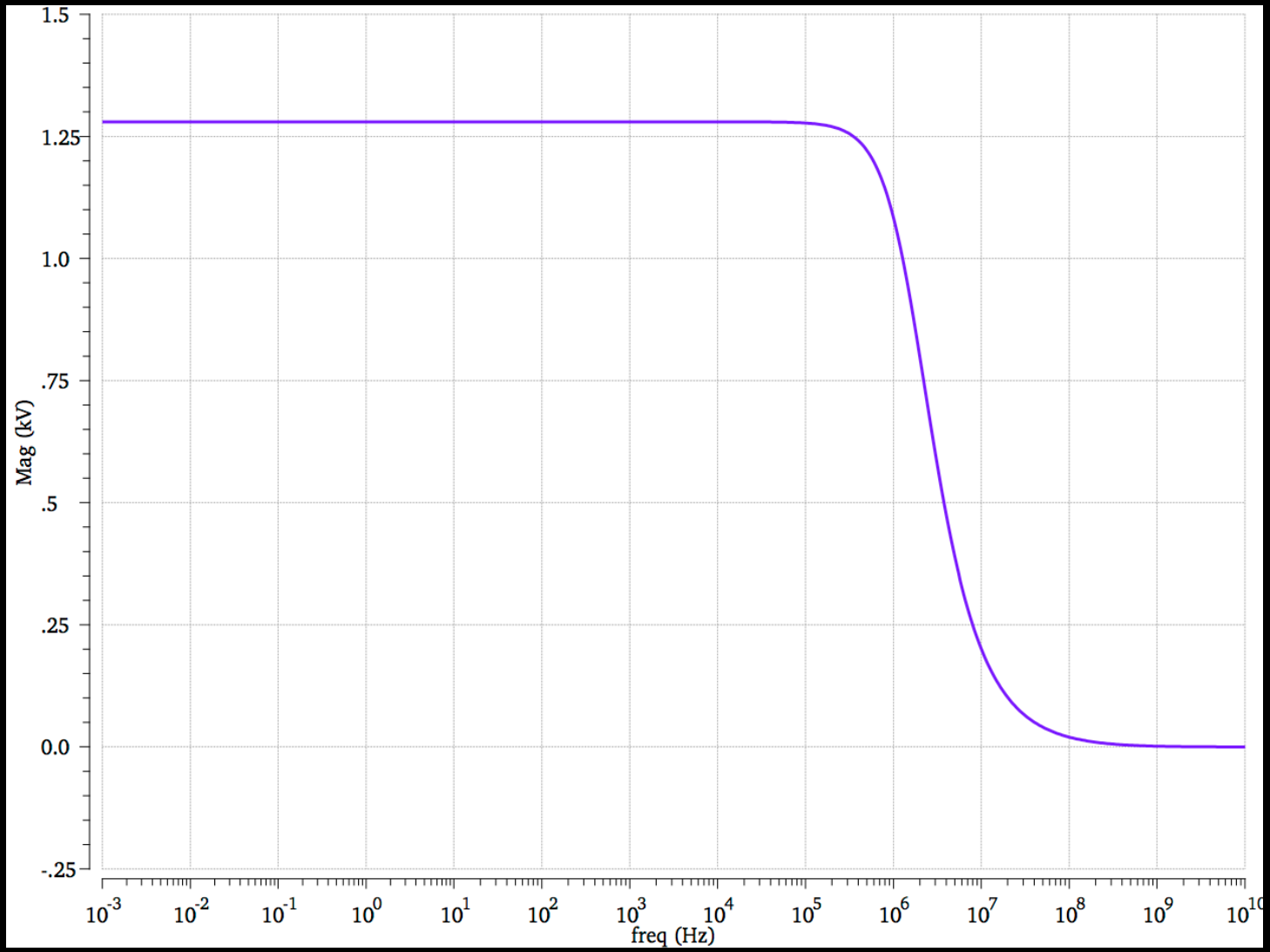
Time to Amplitude Converter



TAC characteristic

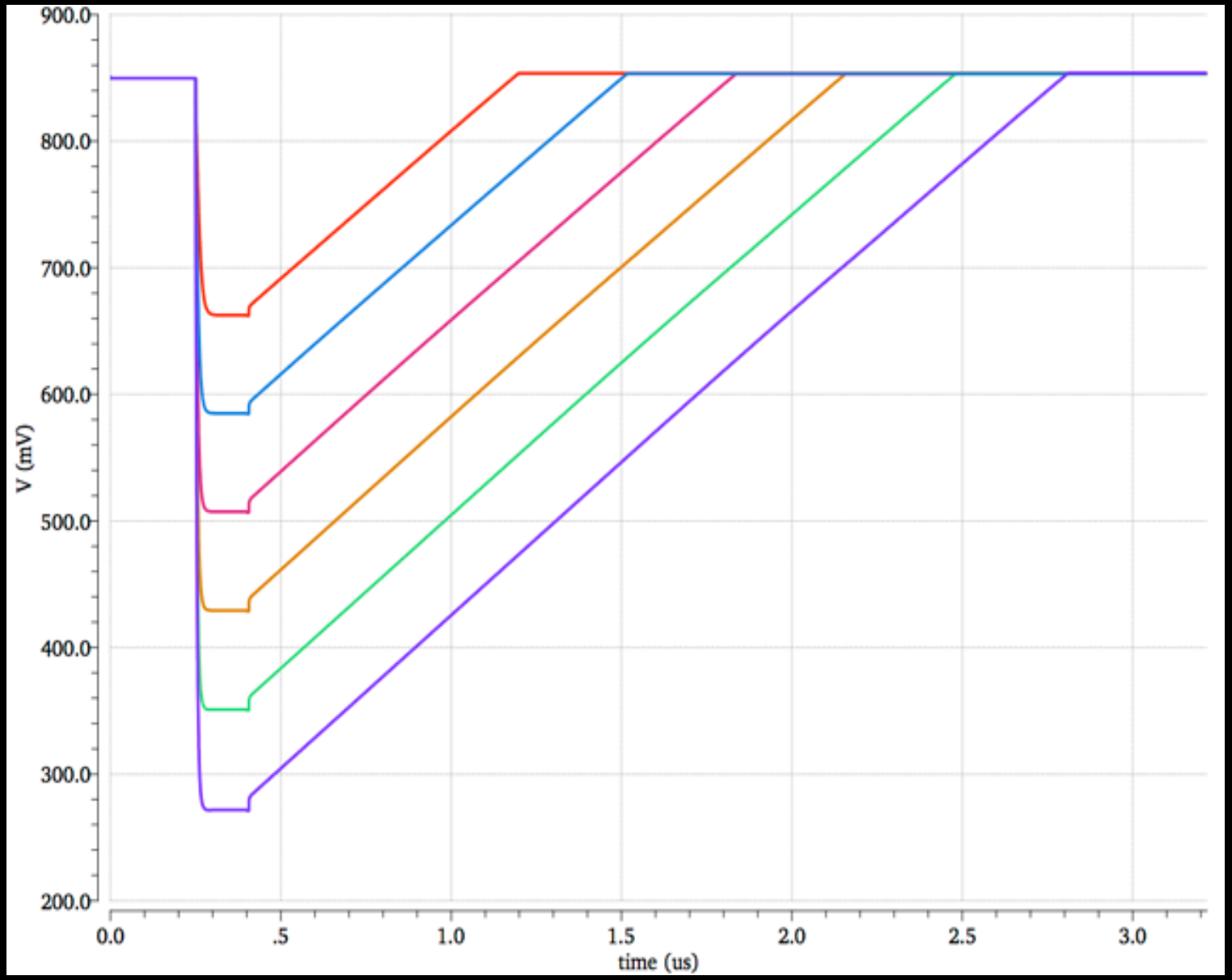


TAC characteristic

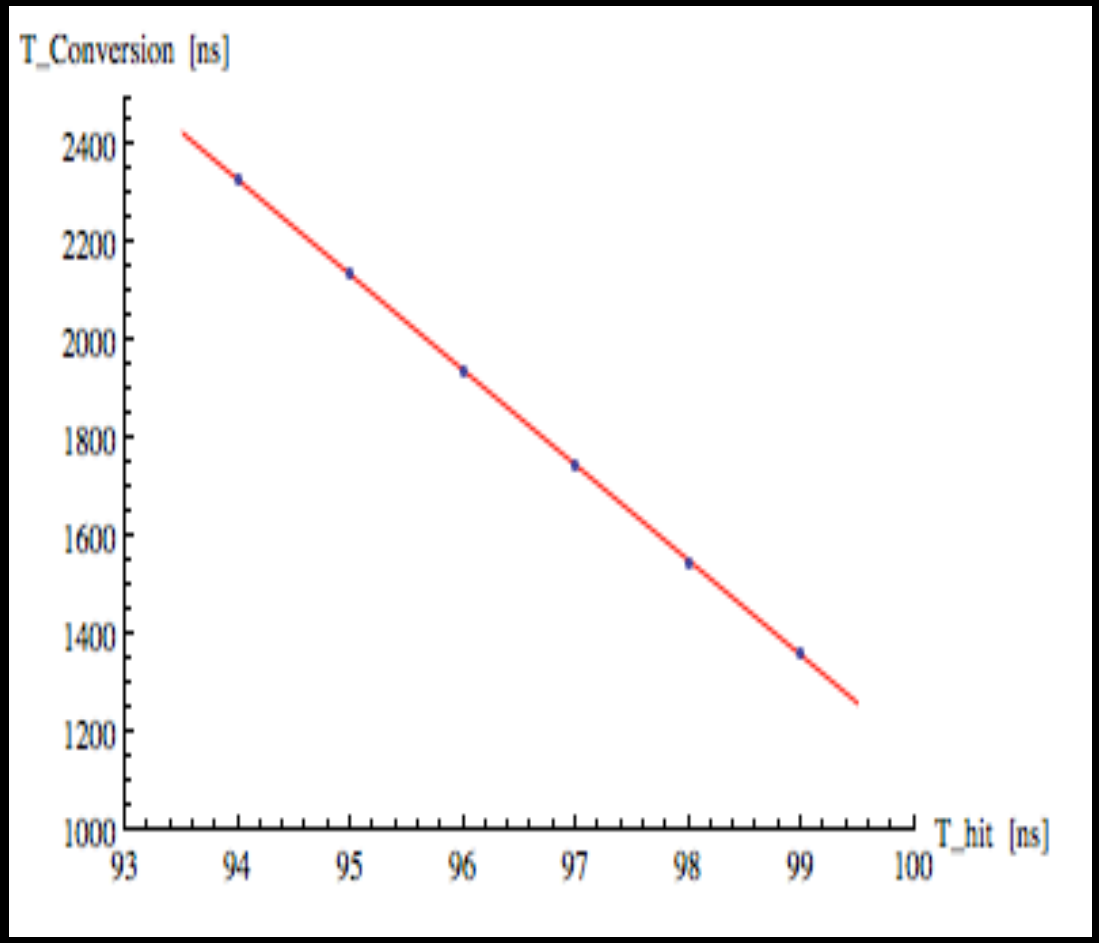


	Gain
Nominal	1250
FF	861
SS	860

TDC linearity

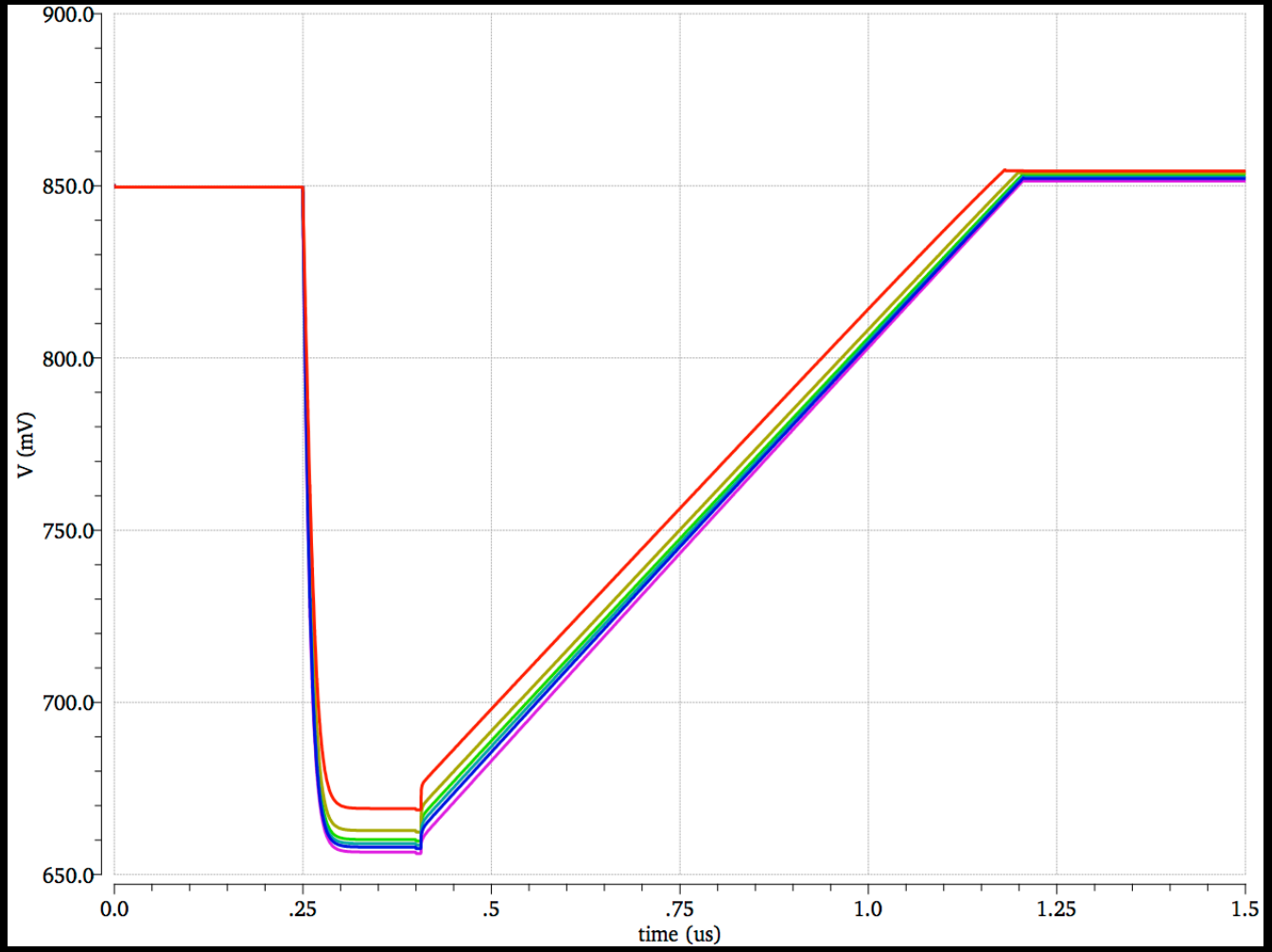


TDC linearity (2)



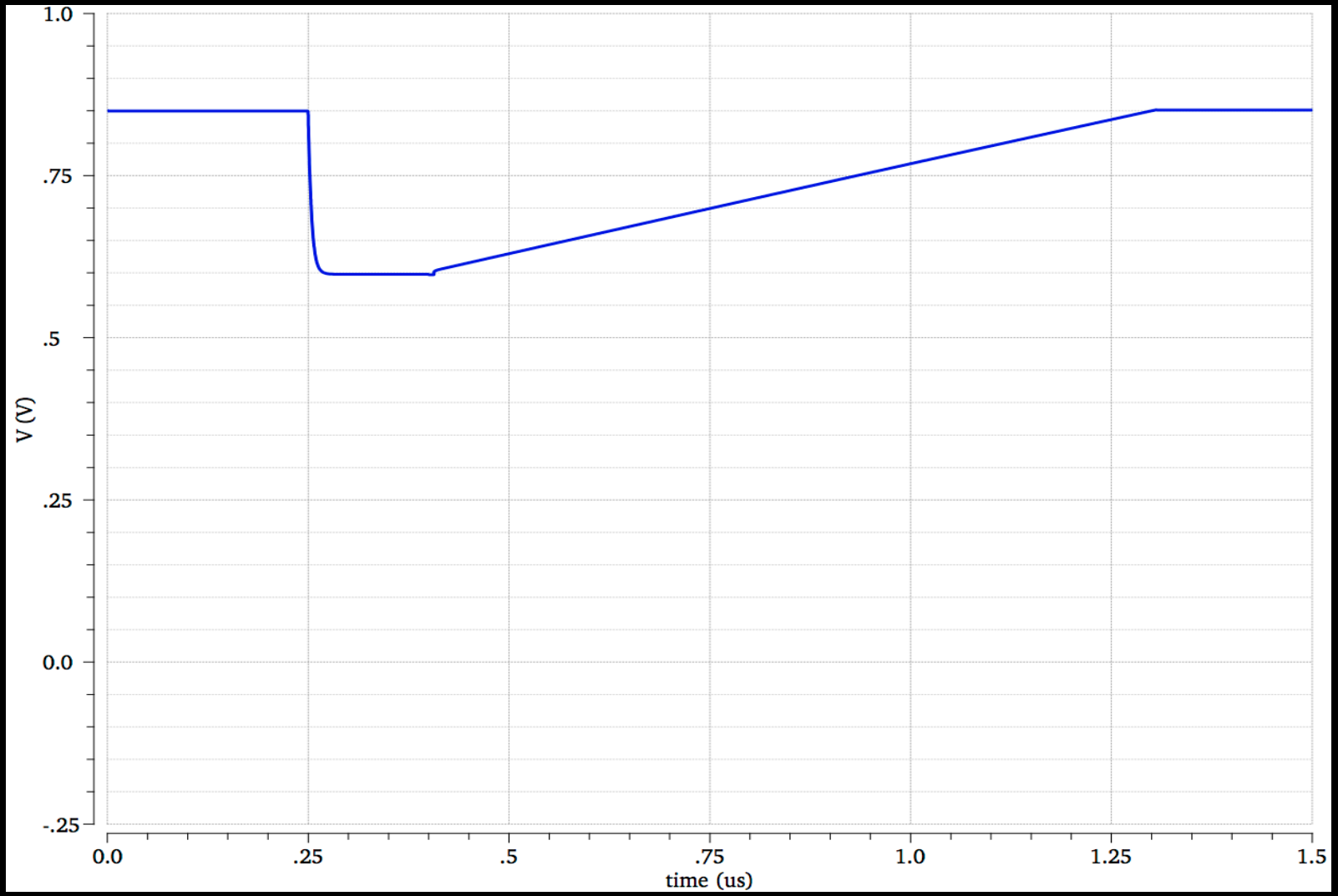
Linearity = 0.13%

Temperature

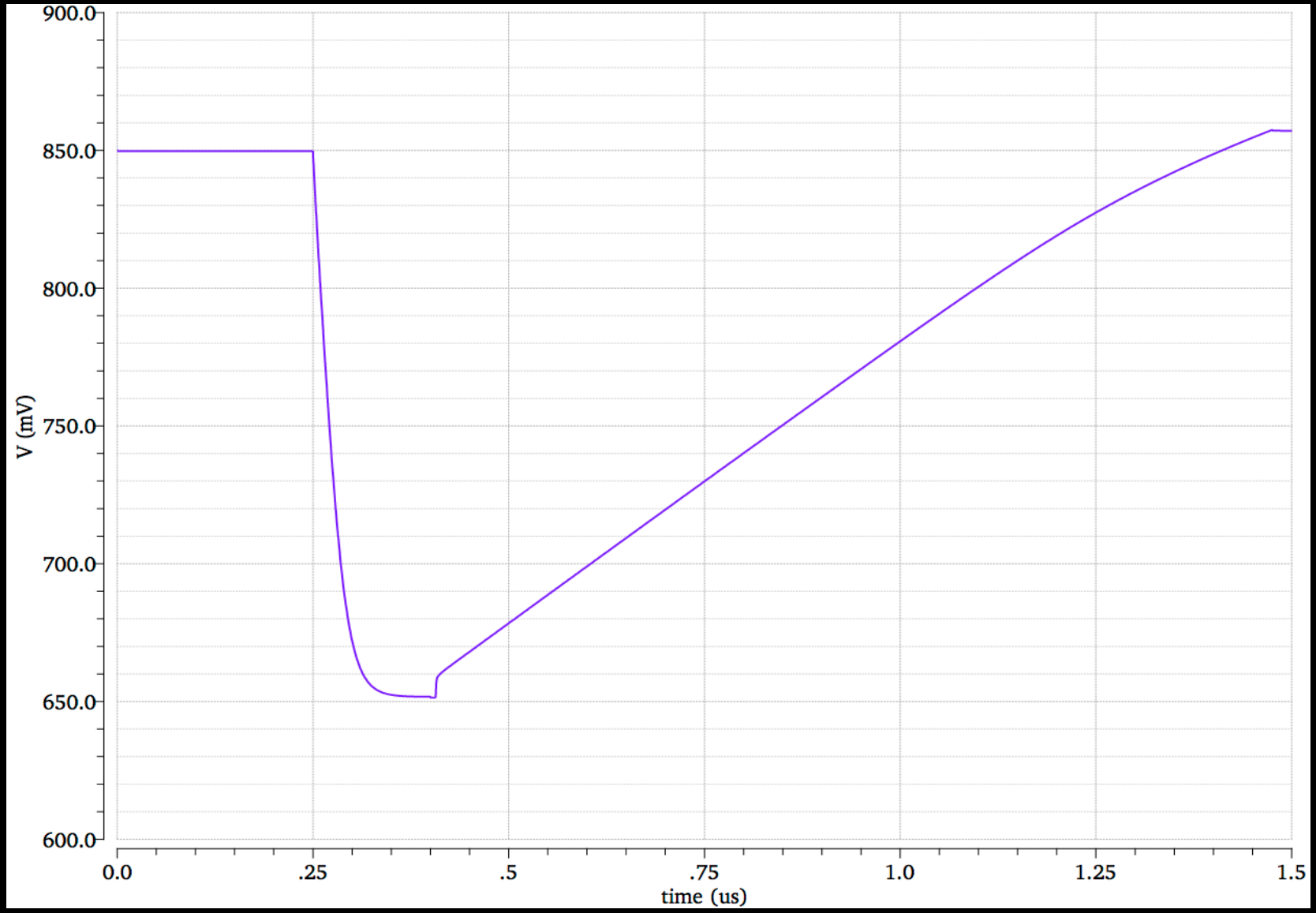


T (°C)	Bits
0	0010111101
25	0011000000
50	0011000001
75	0011000001
100	0011000001
125	0011000001

Corners Process FF



Corners Process SS

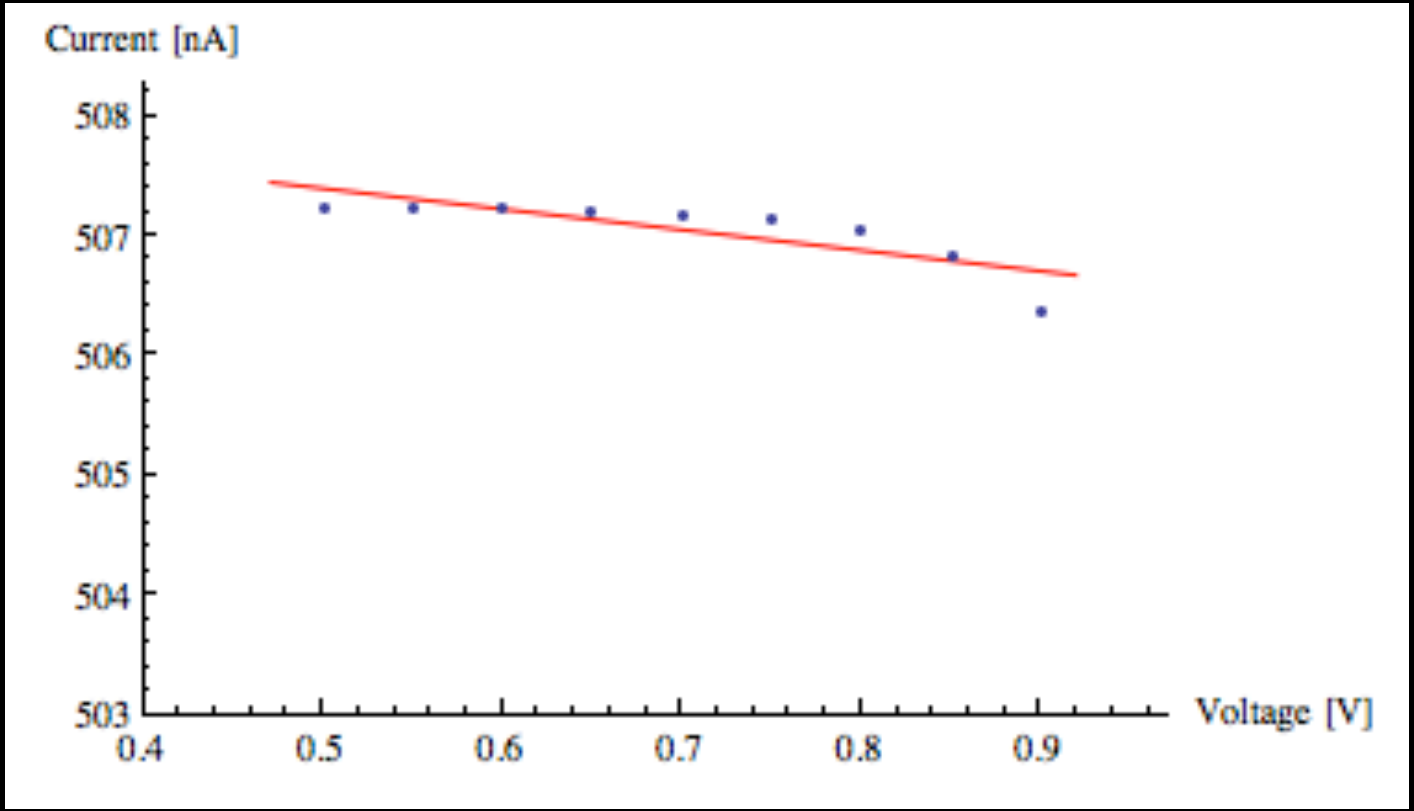


Outlooks

- Improve TDC flexibility
- Further study of the TDC
- Study the complete circuit ToT-TDC

Thank you for your attention

Current error

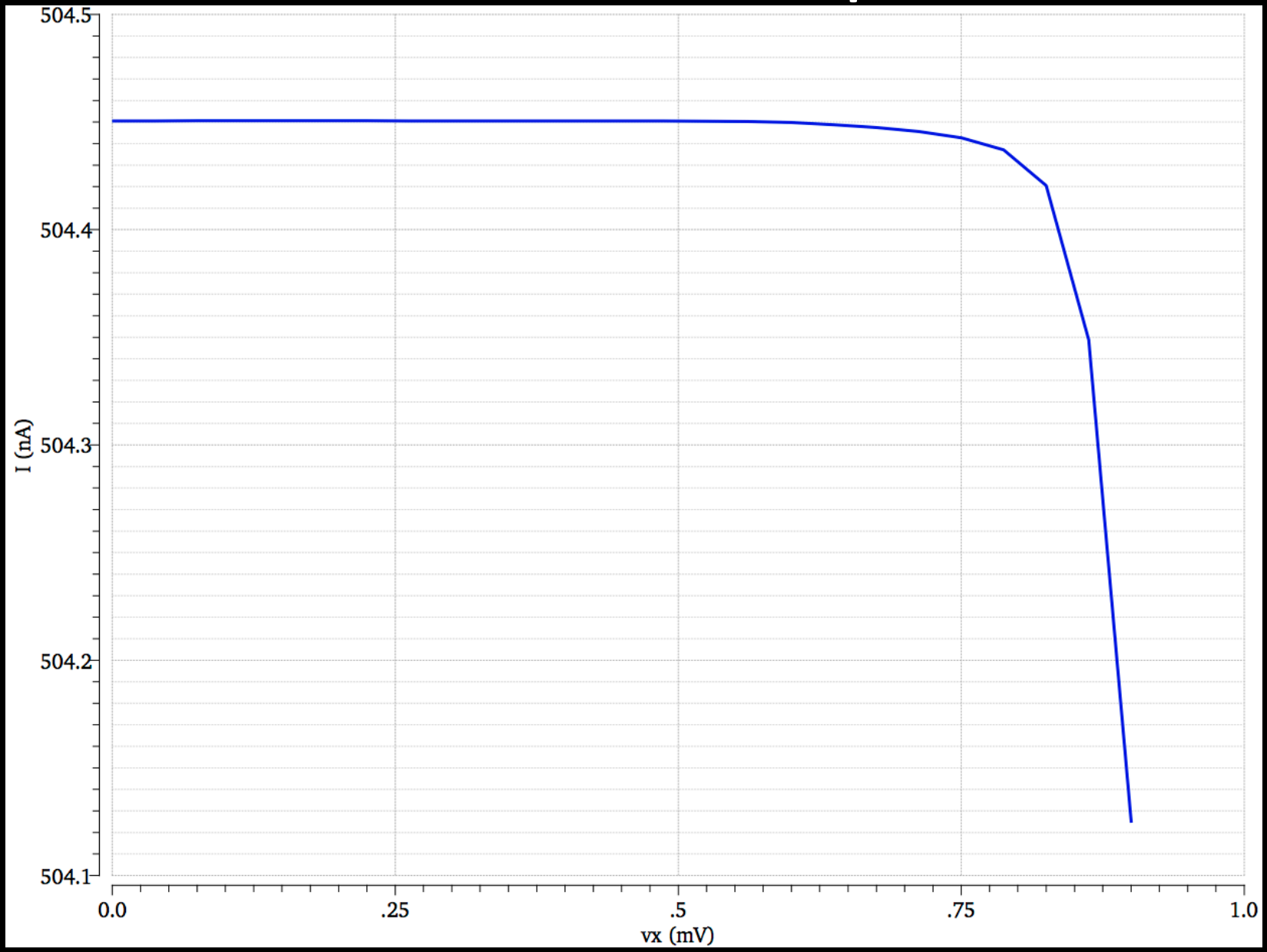


$$y = a + bx = 508.257 + 1.724x$$

$$\frac{\Delta y}{\langle y \rangle} = \frac{b}{\langle y \rangle} = 0.00340$$

$$0.00340 * 0.4V = 0.00136 = 1.36‰$$

Current sweep



TAC number

Event rate max ~ 50kHz

Deat time ~ 3.2us

$$P(n) = \frac{(r\Delta t)^n e^{-r\Delta t}}{n!}$$

P(0)=86.07%

1-P(0)=13.93%

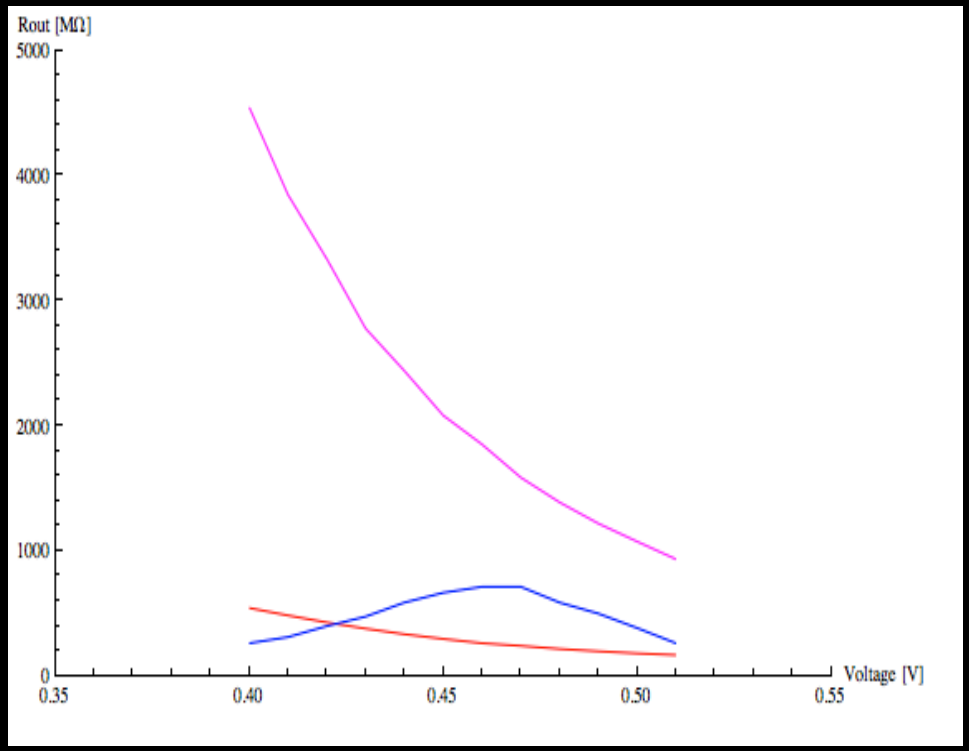
P(1)=12.91%

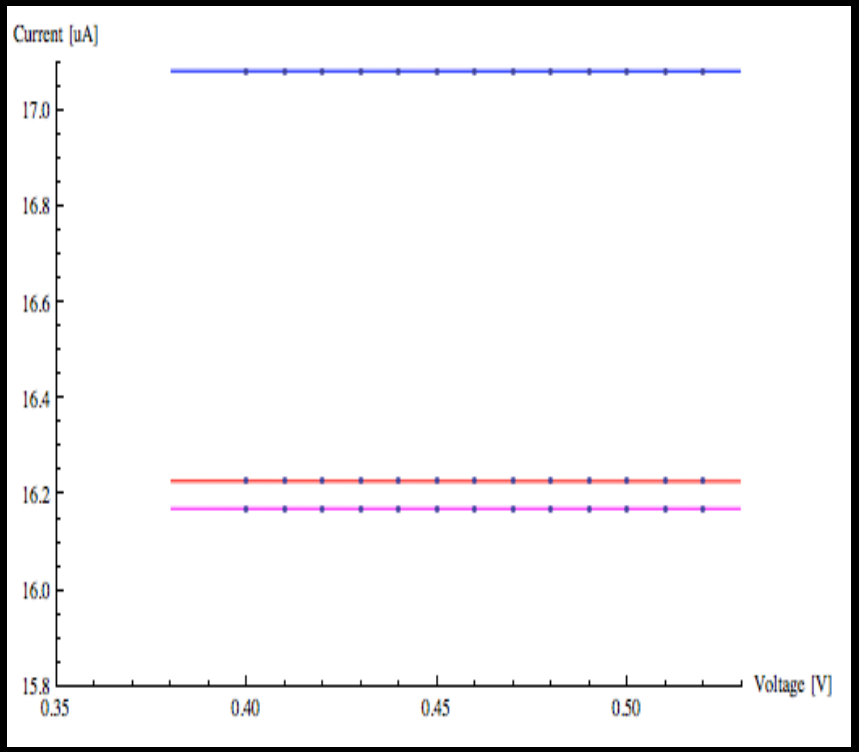
1-P(0)-P(1)=1.02%

P(2)=9.68‰

1-P(0)-P(1)-P(2)=0.51‰

Costant Current Source: I_1

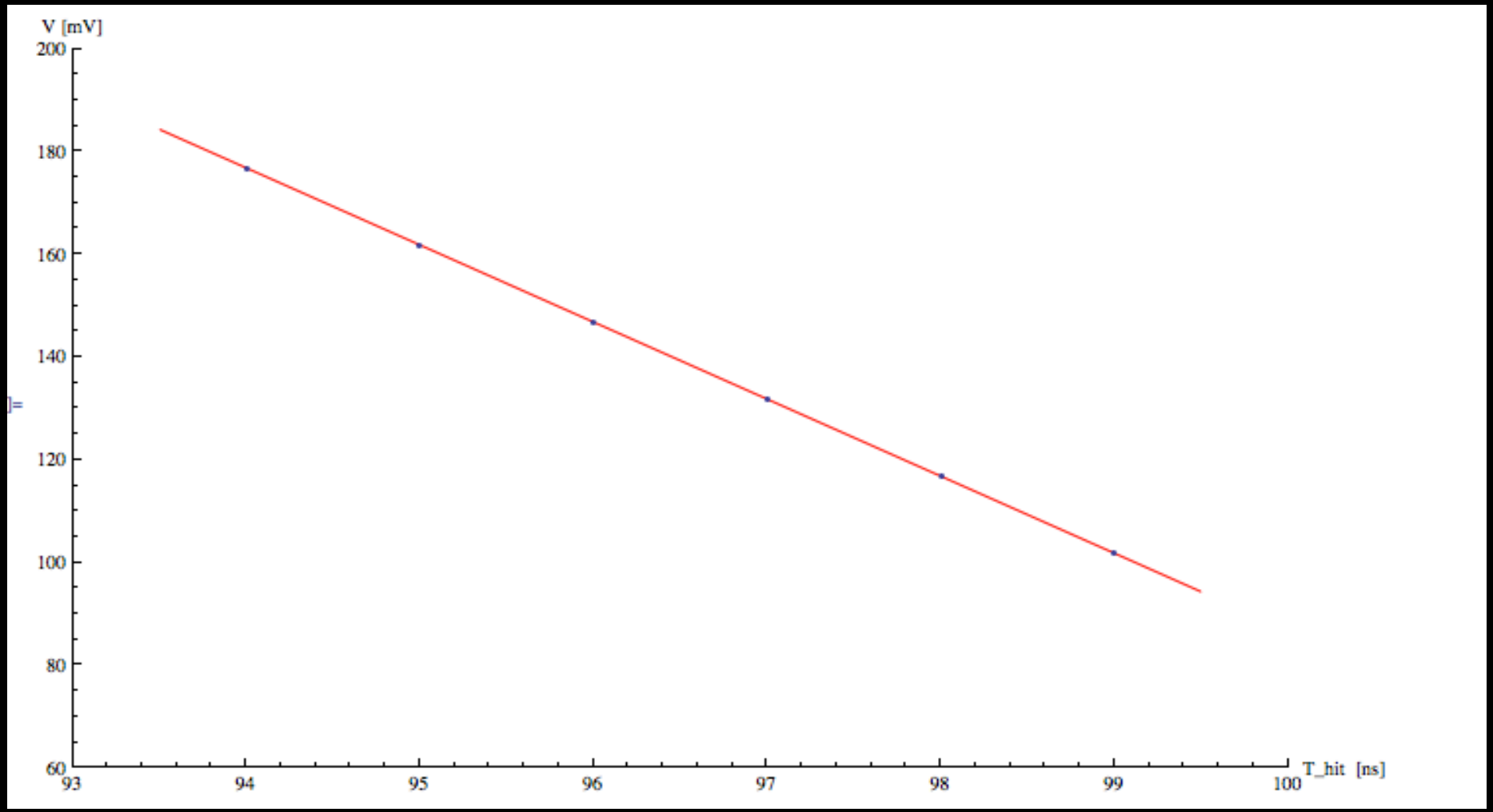




With 9 bits the percentage error is 1/512 =2‰

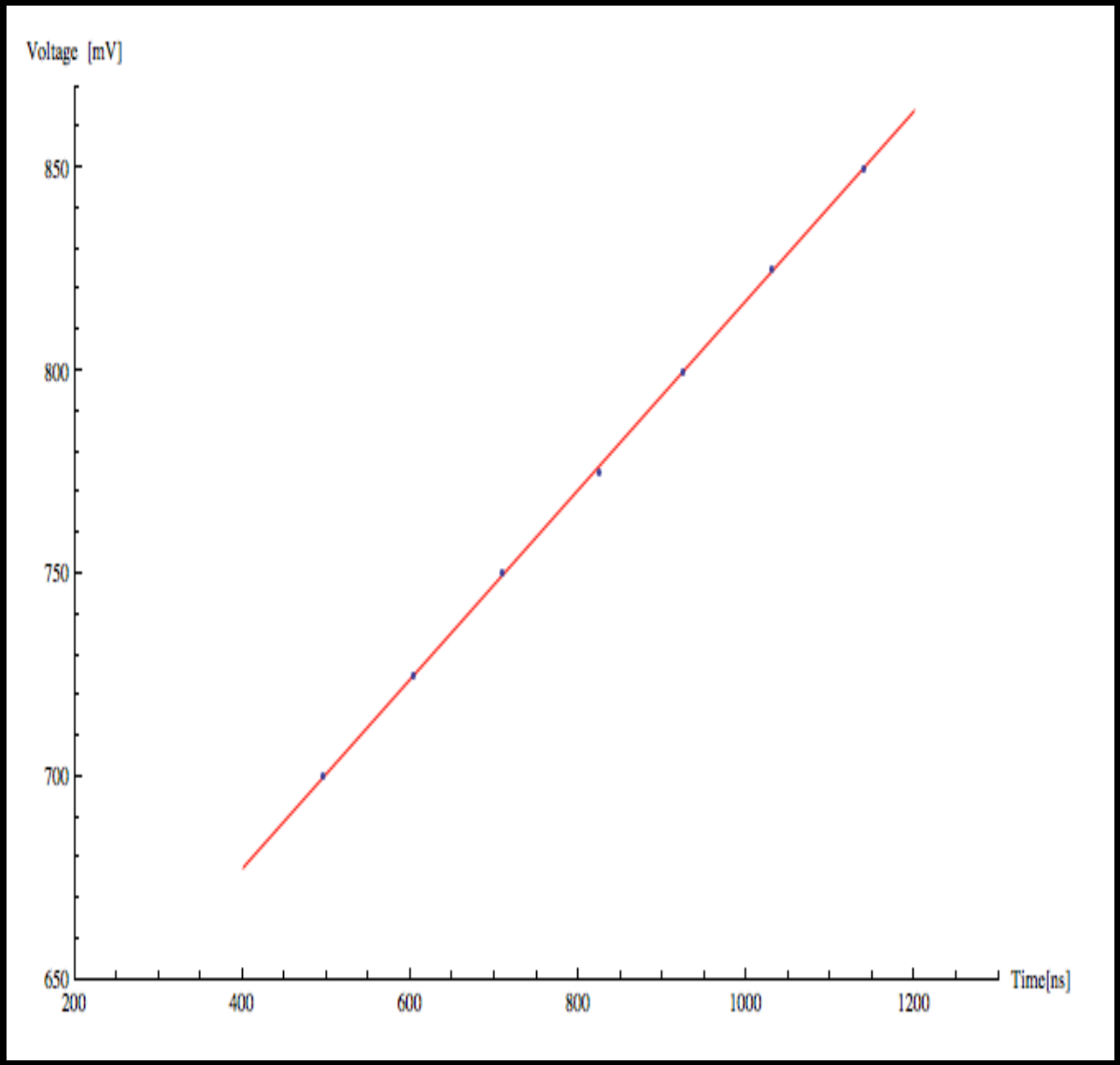
Nominal	0.004‰
FF	0.001‰
SS	0.003‰

TDC linearity(2)



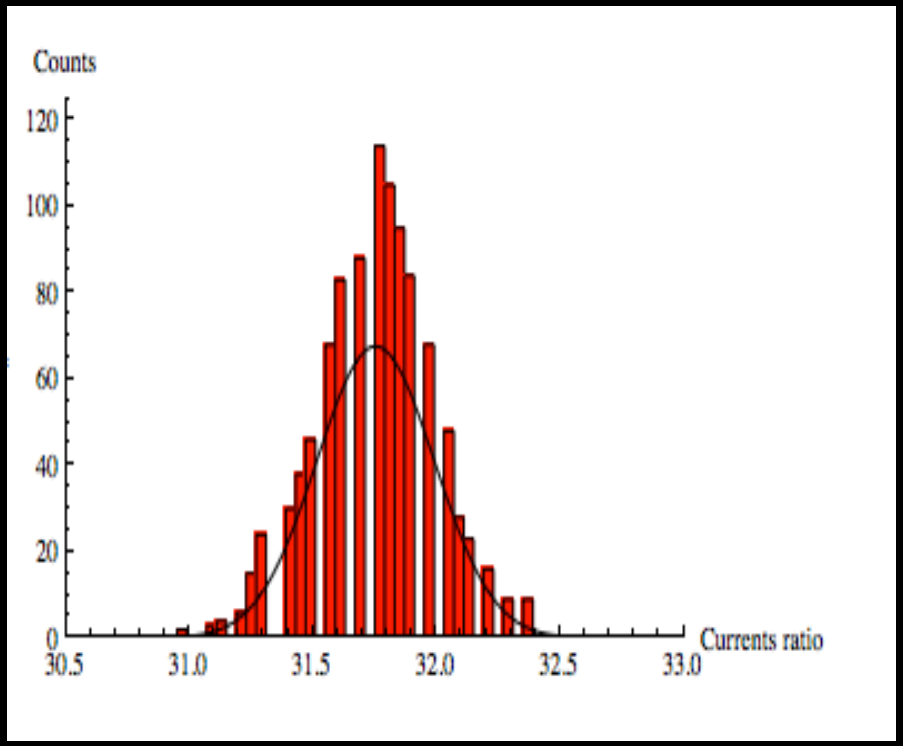
Linearity : 0.02%

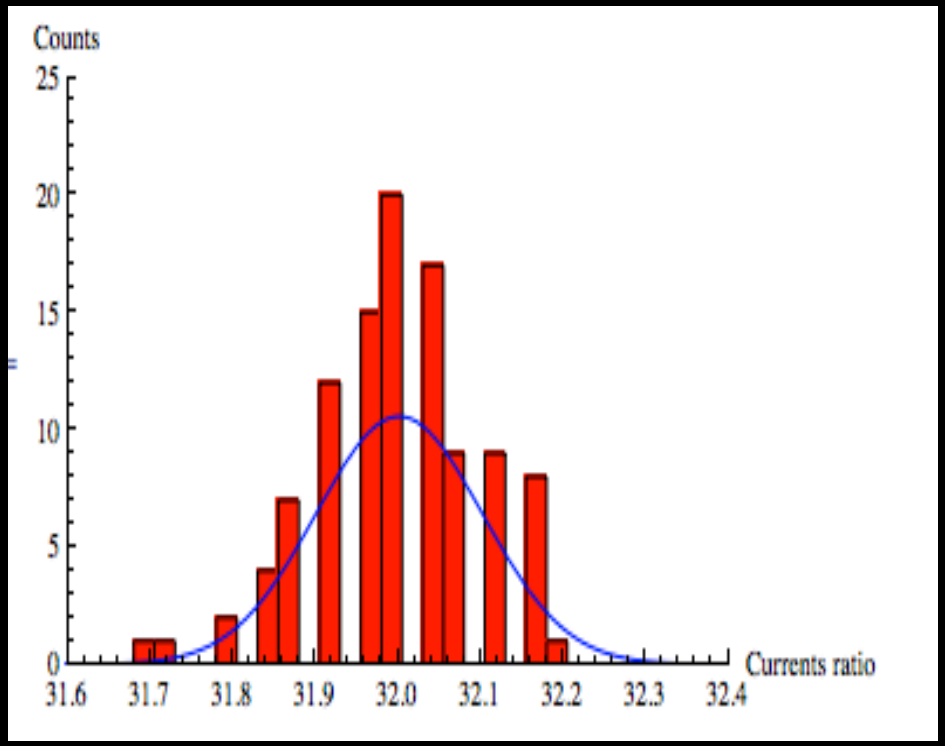
TDC linearity (3)



T_hit (ns)	Goodness(%)
99	0.021
98	0.025
97	0.030
96	0.005
95	0.008
94	0.011

A technology vs B technology





Mean = 31.75

Standard deviation = 0.24

Mean = 32.00

Standard deviation = 0.10