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LePix: Monolithic Sensor for Particle Tracking in a 90 nm CMOS technology

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Introduction

High energy particle physics experiments investigate the elementary constituents of the matter and how they interact with each other. In particular, they are interested in strong interactions (range $\approx 10^{-18}\ m$). The energy required to probe that range is in the TeV range, which is the energy scale typically used in hadrons collider experiments. In these experiments, massive particles are accelerated to reach a speed close to the light speed and they collide with themselves creating quark-antiquark pairs which recombine forming new hadrons. Most hadrons decay in new particles which can be stable or unstable. The latter will decay until a stable configuration is reached. By measuring the characteristics (momentum and energy) of the particles produced after collisions, it is possible to obtain informations about the particles created immediatly after the collisions. To do that, detector systems are built. The first layers of a detector system have several constraints in terms of space resolution, time resolution and granularity to have the possibility to detect and distinguish as many tracks as possible in the rate imposed by the machine. Moreover, a low mass, low power and low noise system is usually required in the inner layers of a detector system. Nowadays, the hybrid pixel sensors are the best solution for inner tracking systems that have to operate with very high particle fluxes. They consist of a detector and a readout chip assembled by bump bonding. The detector is based on a semiconductor p-n junction fully depleted while the read-out chip is based on a electronics system made in a planar CMOS technology. Both the sensor and the electronics are a well-known and mature technology to be used in the main detectors to detect high energy particles. They have excellent performance in terms of space resolution (a few μm), time resolution (a feew tens of ns), power consumption (typycally 50 μW per channel) and radiation hardness (about $10^{15}\ n(1MeV)/cm^2$ in terms of non-ionizing

radiation and about 10 $Mrad$ in terms of ionizing radiation). The main drawback of the hybrid pixel sensors approach is represented by the high mass production costs due to the bump bonding process.
In the last twenty years, an intense $R\&D$ effort has been invested in monolithic detectors. Monolithic devices integrate on the same substrate the sensor and the front-end electronics: in a p-type substrate a n-well, containing the front-end electronics, is used as collection electrode. The integration between the sensor and its front-end electronics is automatically realised at the factory, avoiding expensive interconnection technologies such as the fine pitch bump bonding required by high resolution hybrid pixel detectors. The devices can be thinned down to 50 μm or less, making the contribution of the sensor to the overall material budget very small. Last, but not least, one can take profit of the scale economy offered by state of the art CMOS technologies, which allow to pattern 8 or 12 inch wafers with costs of a few thousand dollars per sample. The main drawbacks of the monolithic approach are represented by the charge collection mechanism and the limited possible options in terms of read-out electronics. Since no-external electric field is applied, the main collection mechanism is based on charge diffusion, which usually means a few hundreds of ns in terms of collection time. Moreover, the limited options in terms of front-end electronics usable in the collection electrodes force the read-out time to be several tens of microseconds. The charge collection time and the read-out time are not suitable for fast applications, where a time resolution in the order of tens of nanoseconds or less is demanded. Furthermore, the charge collection occuring mainly by diffusion weaks the sensors resistance against bulk damage induced by non-ionizing radiation. It is clear that a sensor produced in a standard CMOS technology collecting the charge by drift represents an interesting perspective in terms of time resolution and radiation hardness. These were the main motivations driving the development of the LePix sensors.
This thesis work is organized as follows:

- Chapter 1 shows a brief introduction on High Energy Particle Experiments and discusses the Hybrid Pixel Sensors approach;
- Chapter 2 describes the monolithic sensor approach describing the state of art of the $R\&D$ activity, focusing on the performance of some prototypes produced;

- Chapter 3 shows the LePix approach, focusing on the technology choice, the sensor principle, the device design and the pratical device implementation;
- Chapter 4 describes the diode-prototype produced to evaluate the performance of the CMOS technology chosen in the LePix project whit a back-bias applied;
- Chapter 5 describes the breakdown-prototype produced to deeply evaluate the geometry on which the LePix detector is based on;
- Chapter 6 shows the matrix-prototype used to detect particles, containing both the electrodes and the front-end electronics ;
- Chapter 7 describes the performance of the matrix-prototype in terms of collection capacitance, leakage current and noise;
- Chapter 8 shows the performance of the matrix-prototype in terms of charge collection efficiency;
- Chapter 9 shows the diode-prototype and the matrix-prototype performance in terms of radiation hardness;
- Chapter 10 describes an alternative read-out approach based on a binary output for the matrix-prototype;
- Chapter 11 shows the performance of the matrix-prototype with the read-out electronics based on a binary output.

Chapter 1

Hybrid Pixel Sensors

In this chapter, a description of hybrid pixel sensors will be given. The chapter starts with a brief introduction on High Energy Particle (HEP) experiments (that is not the main subject of this thesis) focused on the constrains for the inner tracker silicon detector. Then the hybrid pixels approach will be discussed. In particular, the sensor characteristics, taking into account the main parameters to optimize in the device, and a classical approach for the front-end electronics will be reviewed. The aim of this chapter is to introduce some concepts that will be continuously used in the thesis.

1.1 HEP Experiments

The goal of high energy particle physics experiments is to investigate the elementary constituents of matter and how they interact with each other. To do so, high energy particle accelerators have been built. High energy is necessary both to have a wavelength as short as possible and to produce massive particles. These particles interact by electroweak and strong interactions. High energy particle physics experiments are mainly interested in strong interactions (range $\approx 10^{-18}\ m$). By following the *de Broglie* law, the energy necessary to probe particles in that range is given by:

$$E = \frac{hc}{\lambda} \approx 1.2\ TeV \tag{1.1}$$

The TeV is the typical energy scale used in high energy hadrons collider experiment (LHC, TEVATRON). In these experiments, massive particles

are accelerated to reach a speed close to the light speed. After their collision, quark-antiquark pairs are produced, which recombine forming new hadrons, in a few fermi range from the interaction point. In same cases, they can also recombine forming a spray of hadrons, called jets. Most hadrons decay a few hundred of micrometers far from their production point (called primary vertex). By measuring the characteristics (momentum and energy) of the particles produced at that distance (called secondary vertex), it is possible to obtain information about the primary vertex and, consequently, about the quarks' parameter. The goal of a detector system is to detect and track the particles produced after the collisions. For example, the sigma barion Σ^+ lifetime is $\tau = (8.018 \pm 0.025) \cdot 10^{-11}$ s: the distance covered by this barion is $d \approx 24$ mm. It decays (see Fig. 1.1) in a proton (stable) and a pion (π^0). The pion decays immediately in two photons. The first layer of detector, usually placed a few centimeters far from the interaction point, will detect only the protons: only by offline analysis it will be possible to go back to the primary vertex. The accuracy commonly required to the first layers is $\approx 10\%$ $c\tau$: it means less than 30 μm for a particle having a lifetime in the order of a picosecond. In addition, many other particles could pass close to the decay point. To distinguish multiple tracks, not only high space and time resolution are required, but also a high granularity, that means an appropriate number of independent sensing elements. In

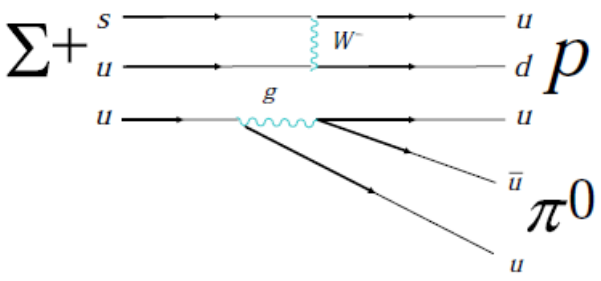

Figure 1.1: The Σ^+ barion decay process.

fact, the first layers of a detector system have to deal with a huge number of primary and secondary vertexes. An interesting example is given by the LHC ([1]) working in an ideal regime. In this machine, two proton beams are accelerated (one rotating clockwise, the other one counterclockwise) at

7 GeV; each beam contains many bunches of 10^{11} particles. They cross each other every 25 ns but only a few particles per crossing collide (about 20). For a detector layer placed 5 cm far from the collision point, it means a rate of $\approx 50\ \frac{MHz}{cm^2}$. Of course, not all the hits represent an interesting event and multistep selection criteria will reduce considerably the amount of data but the sensors and their electronics front-end have to deal with that order of magnitude in rate. Finally, the detector has to be robust enough to tolerate the high irradiation flux coming from the impinging particles: the detector performance tends to decrease because of the radiation damage.
In short, the main characteristics of an inner detector system are:

- high time and space resolution, to be able to deal with the high particles rate;
- high accuracy, to be able to distinguish close tracks;
- high radiation hardness, to be able to have good performance in a high flux of particles environment.

Furthermore, the detectors must have low mass (to reduce the multiscattering effect) and, together with their electronics, low noise and low power consumption. Obviously, it is not possible to satisfy all these requirements simultaneously. For example a thin semiconductor detector offers excellent performance in terms of radiation tolerance and multiple scattering, but only yields a relatively small signal, making the design of the front-end circuit more challenging and typically requiring more power consumption and, consequently, more mass in cabling to cool down the system. Even if it is not possible to optimize all the requirements at the same time, it is possible to obtain interesting performance through reasonable compromises. Nowadays, the hybrid pixel sensors are the best solution for inner tracking systems that have to operate with very high particle fluxes. In the following sections, both the detector and the frontend electronics will be described.

1.2 Hybrid Pixel Detectors

Hybrid pixel detectors consist of a detector and a readout chip assembled by bump bonding (see Fig. 1.2). They can cover several square cm in one unit. The front-end chip is made in a planar CMOS technology. Both the

sensor and the electronics are a well-known and mature technology to be used in the main detectors to detect high energy particles.

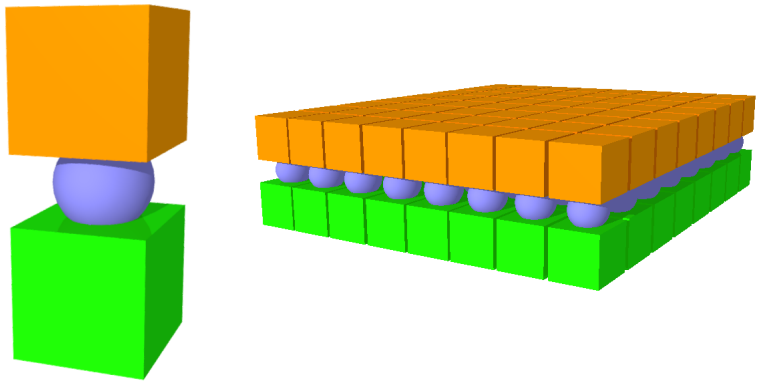

Figure 1.2: Schematic view of a hybrid pixel (left) with the sensor in the bottom part (green) and the front-end electronics connected through a bump bonding and a matrix of sensors (right).

1.2.1 Sensor

The sensor is a two dimensional matrix of *pin* diodes. The detection principle of a semiconductor is the same of a gas ionization chamber: the energy released by an impinging particle produces electron-hole pairs and, by applying an electric field, it is possible to collect the charges produced and measure the energy lost by the impinging particle. However, in the diode case, a semiconductor junction is used to separate electrons and holes for charge collection. The main advantage compared to the gas chamber is the energy resolution given by:

$$N = \frac{E}{E_i}$$

where N is the number of charged pairs due to the energy lost by the particles and E_i is the energy required to have an electron-hole pair (a few eV for a semiconductor, 20 eV for a gas chamber). The p-n junction is the basic building block of silicon sensor. In fact, only one doped semiconductor is not sufficient to detect particles: the energy lost by a minimum ionizing particle (MIP) in silicon generates about 80 electron-hole pairs per micrometer. Assuming a detector with the typical size of a pixel detector (thickness $d \approx 300\ \mu m$ and area $A = 10^4\ \mu m^2$), the number of electron-hole pairs is

given by:

$$N_{e-h} = 80 \cdot 300 = 2.4 \cdot 10^4$$

The number of electron-hole pairs excited by thermal effect at $T = 300\ K$ for an intrinsic semiconductor having the same volume is given by:

$$N_{e-h} = n_i \cdot d \cdot A \approx 4.4 \cdot 10^4$$

with n_i intrinsic charge carrier density at $T = 300\ K$ ($n_i = 1.45 \cdot 10^{10}\ cm^{-3}$). The number of thermal created electron-hole pairs has the same order of magnitude of the pairs due to a MIP. In a p-n junction, the space charge region (that is the depleted region) is almost completely depleted of mobile charge carriers and consequently the number of electron-hole pairs generated via thermal effect is negligible compared to the number due to a MIP. The main parameters to be study in a semiconductor sensor are the depletion region, the charge collection time and the leakage current.

1.2.1.1 Depletion region

Most modern p-n junctions are fabricated using a planar technology: in a low doped substrate bulk, a high doped well having the opposite doping is introduced. Usually the thickness of the bulk is a few hundred of micrometers. By applying a reverse bias to the junction, it is possible to increase the depletion region depth up to the thickness of the detector. Having a fully depleted sensor is important both to maximize the efficiency of the detector, which is useful to detect particles penetrating the device with a shallow angle (Fig. 1.3), and to maximize the output signal due to the impinging particle. In fact, if the detector is fully depleted, all the electron-hole pairs created by the impinging particle will be collected (provided there are not trapping effects present). The depletion region width for a planar and abrupt junction is given by:

$$d = \sqrt{\frac{2 \cdot \epsilon}{q \cdot N_{eff}} \cdot (V_{appl} + V_{bi})} \tag{1.2}$$

with ϵ silicon permittivity, q electron charge, N_{eff} effective doping level (also accounting for radiation damage effects, if present), V_{appl} potential applied at the junction and V_{bi} built-in potential. Full depletion voltage can be

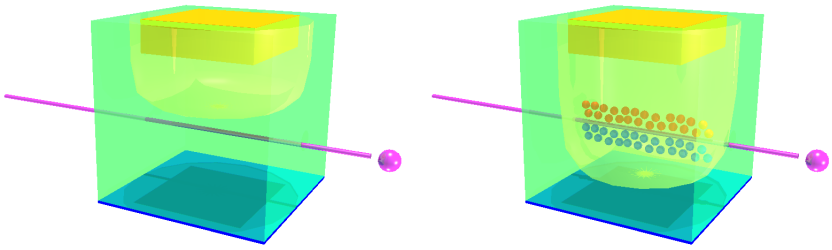

Figure 1.3: Efficiency of the pn junction not depleted (left) and depleted (right): maximizing the depletion region allows to collect charge over the full volume of the detector.

determined by capacitance measurements. A reversed biased detector acts as a capacitor having the value:

$$C = \epsilon \cdot \frac{A}{d} \tag{1.3}$$

where A is the detector area and d is the depletion region depth. As soon as the detector is fully depleted, the capacitance reaches its minimum constant value (Fig. 1.4). However, the capacitance to the back-plane is only one

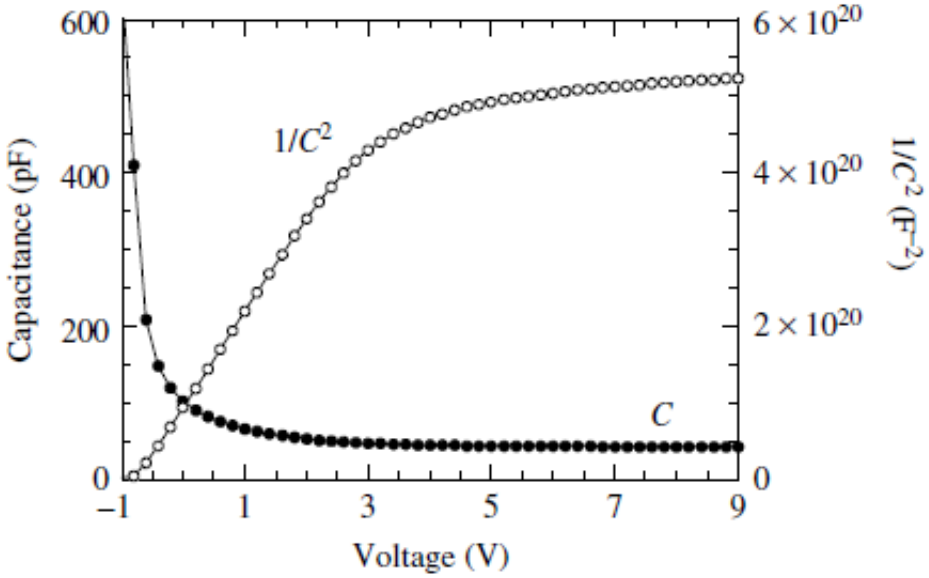

Figure 1.4: $C - V$ curve and $1/C^2 - V$ curve of a Si n^+p diode ([7]).

of the capacitive contributions at the input of the front-end electronics; in fact, the other contributions are due to:

- the sum of the capacitances to the neighboring pixels;
- the front-end electronics input capacitance;
- the capacitance due to the bump and parasitic capacitance of the bump bonding pad.

The largest contribution to the total capacitance in hybrid pixel sensors is normally given by the interpixel capacitance which is due to the parasitic capacitances between one pixel and its neighboring pixels. This interpixel capacitance is proportional to the perimeter of the pixel and to the gap size between the pixel implants. For pixels typically used in high energy particle experiments, the contribute due to the interpixel capacitance is a few tens of fF; in particular, it has been estimated to be about 60 fF for a 125×125 μm^2 pixel having a 20 μm gap (close to the choice of the CMS experiment) and, for a pixel having sizes of 50×400 μm^2 (choice of ATLAS experiment), between 30 and 100 fF ([8]). The main effect of the interpixel capacitance is the parasitic signals induced by a charge deposited on a single pixel on the neighboring pixels: this effect is usually called *cross-talk* and can be minimized by a correct electronics front-end design. A realistic value of the total capacitance of a detector is a few hundreds of fF. A MIP in a 300 μm thickness fully depleted device generates 24000 electron-hole pairs (80 $pairs/\mu m$), that is a charge $Q = 3.84$ fC. By considering a typical capacitance value seen at the input of the front-end electronics of 200 fF, it is possible to estimate the signal at the output of the sensor: $V_{sign} = \frac{3.84\ fC}{200\ fF} = 19\ mV$ that is the order of magnitude of the signal that has to be processed by the front-end chip.

1.2.1.2 Charge Collection Time

The charge generated in a semiconductor detector does not appear at the input of the amplifier instantaneously after the impact of an ionizing particle: it takes some time for the generated charge to reach the collection electrode. There are two possible charge collection mechanisms in the p-n junction: diffusion and drift. The former happens when no external voltage

bias is applied to the junction and, consequently, there is not an electric field moving the charges generated outside the depleted region but their movement is due to a carrier concentration gradient; the latter is dominant when an external bias is applied in the same direction as the built-in voltage (there is also a diffusion component but it is negligible compared to the drift component). The charge movement is due to the electric field applied at the junction. The time spent by the device to collect a charge generated in the substrate depends on the ΔV applied to the p-n junction. In fact, the speed of a charge in a semiconductor is given by:

$$v = \mu E$$

where μ is the mobility of the charge in the medium and E is the electric field applied. If we suppose to apply a reverse bias $\Delta V = 100\ V$ to have a fully depleted 300 μm junction, we can estimate the charge collection time. In fact, for a device collecting electrons, this is given by:

$$t = \frac{d}{v} = \frac{d}{\mu \cdot \frac{dV}{dx}} = \frac{300\ \mu m}{0.14\ \frac{m^2}{V \cdot s} \cdot \frac{100\ V}{300\ \mu m}} \approx 6\ ns$$

The formula to calculate the collection time assumes a constant field across the detector. Even if this is an approximation which is only true in case the detector has significant over depletion voltage, it is useful to have an idea about the order of magnitude of the collection time. For a device collecting holes, the mobility is lower and, consequently, the collection time is approximately three times higher.

1.2.1.3 Leakage Current

The leakage current (or dark current) is the current flowing in the sensor in absence of external effects like particles or light if a reverse bias is applied ([8]). It can be due to free carriers which diffuse from the undepleted volume into the space charge region or, more important, charges generated by thermal excitation in the depletion region. A typical current to voltage curve for a reversed biased sensor is shown in Fig. 1.5 ([8]). For voltages lower than the full depletion voltage, the current is proportional to the square root of voltage; when the full depletion is reached, it remains constant up to the electrical breakdown. In first approximation, its behavior can be obtained

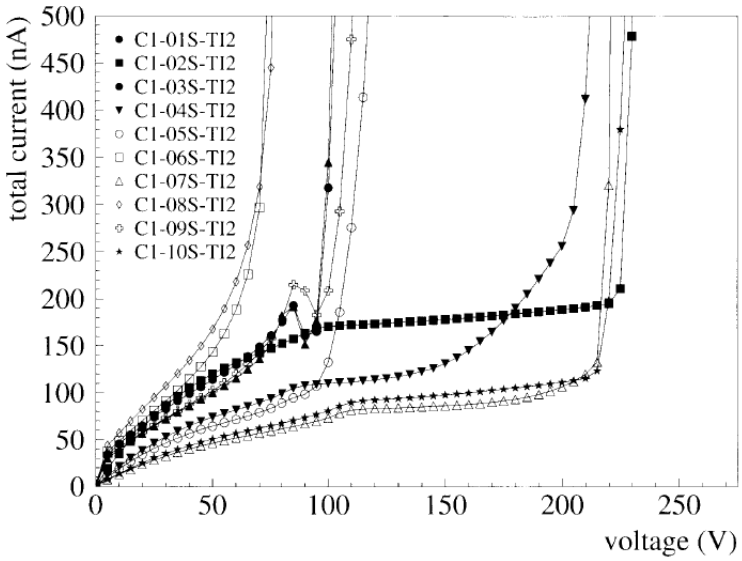

Figure 1.5: I-V curves for different pixel sensors of about 8.8 cm^2.

from the following equation:

$$J_{vol} \approx -e \cdot \frac{n_i}{\tau_g} \cdot d \tag{1.4}$$

where J_{vol} is the current density, τ_g is the carrier generation lifetime, d is the depletion region depth and n_i is the intrinsic carrier concentration. The current depends on the temperature and this dependency is hidden in the term n_i; the dependency can be obtained from the following equation:

$$J_{vol} \propto T^2 e^{-\frac{Eg(T)}{2kT}}$$

Usually a rough estimation is to assume that the current doubles every $8K$. One of the most crucial regions for the sensor stability in terms of leakage current and breakdown voltage is represented by the edge termination. The sensor behavior at the edge is determinated by the potential surface in that region. An a priori prediction of the surface voltage in the edge region is complex due to the several parameters influencing it (local variations of surface conductivity, surface humidity, dust contamination and so on). The two worst-case scenarios for the edge are represented in the top part of Fig. 1.6. In the first case, the depletion region reaches the sensor edge which is full of generation-recombination centers because of its imperfect lattice

structure due to the mechanical damage caused by the dicing procedure: the free charges are driven by the electric field causing an unwanted current flowing in the device. Usually this is avoided by design allowing enough space for the extension of the depletion layer.
In the second extreme case the surface potential drop to the bulk voltage through the device scribe-line causing an electrons accumulation layer. Due to the conductive nature of the electrons layer, the potential in that region will be close to the back-bias voltage, causing a local breakdown due to the high voltage drop in a small region. Floating rings are typically used to increase the breakdown voltage of the detector since they allow to drop the voltage over several junctions.

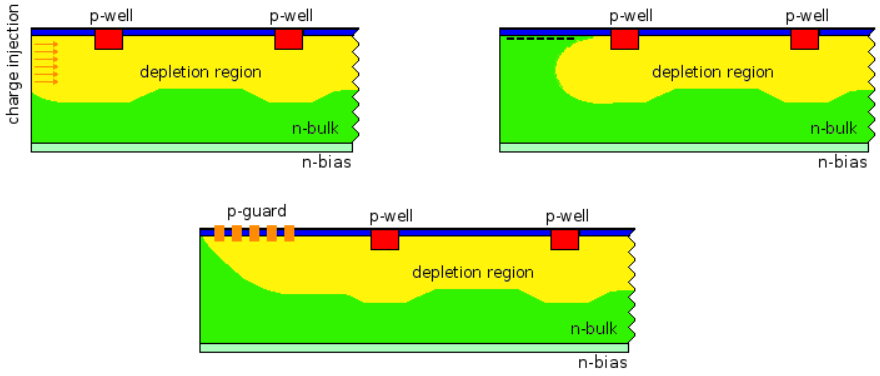

Figure 1.6: Worst scenario in terms of edge leakage current (top-left), breakdown voltage (top-right) and solution used to have a smooth voltage drop towards the cutting edge (bottom).

1.2.2 Front-end Electronics

The front-end electronics has to convert an analog signal coming from the output of the sensor into a signal manageable by the digital interface: usually, the raw detector signal has to be processed to perform amplitude or time measurements. Several constraints are imposed to the front-end electronics chips; for example, the size of the chip is limited by the size of the pixel matrix, the power consumption has to be limited to avoid a too aggressive cooling system, the circuit noise has to be as small as possible to have a high detection efficiency, the circuit has to work at a sufficient speed to deal with

all signals coming from the detector avoiding to overlap them and avoiding to miss some signals, a high radiation-hardness has to be guaranteed. Nowadays, these features can be satisfied using modern CMOS technology which allows to design fully custom made Integrated Circuit (IC): their complexity depends on the measure they have to perform. Even if a huge number of different ICs having different purposes have been designed and produced, it is possible to spot several common building blocks. In particular, the chips can be divided in an active area and a periphery. The active area is made of a repetitive Pixel Unit Cell (PUC) having approximately the same area of the corresponding pixel; in the PUC, the signal coming from the sensor is amplified and a noise filtering is usually done. A typical scheme employs a Charge Sensitive Amplifier (CSA) and a shaper filter (see Fig. 1.7). The

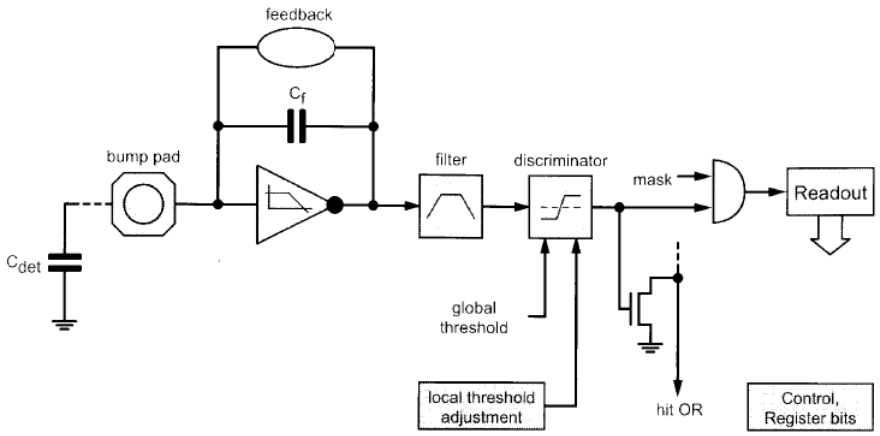

Figure 1.7: Schematic view of a possible readout for pixel particle detectors.

CSA, which amplifies the signal, is one of the most crucial stages of the front-end electronics. In fact, it has to be designed having a high gain with a sufficient bandwidth, with a low power consumption (typically 50 μW in high energy physics) and low noise, with a good immunity to the fluctuation in the supply voltage and a good uniformity between different channels. The shaper filter is also an important stage because it allows to fix the desired rise and decay times, through RC high-pass and low-pass filters, and, more importantly, it allows to improve the signal to noise ratio. If an information about the energy of the impinging particle is required, the signal at the output is usually digitalized by an ADC which converts the signal in discrete

steps corresponding to the digital bits. Since the power consumption of an ADC is usually high, it is placed in the periphery of the chip and it does not process all signals but it works only when it is activated by a trigger system. When no information about the energy lost by the particles is required, the stage at the output of the shaper is made by a discriminator which compares the input signal to a threshold value, usually set as low as possible to maximize the detection efficiency without suffering from noise: the logic output value is then sent to the chip periphery. The resolution of a segmented detector is strongly dependent on the readout. In fact, for a binary readout, the maximum reachable spatial resolution is $p/\sqrt{12}$, where p is the pixel pitch. It means a spatial resolution of a few ten microns for a pixel pitch $p \approx 100\ \mu m$. With an analog readout, a higher resolution (up to a few microns) is possible by using a *charge center of gravity* reconstruction based on the amplitude of the signal coming from a group of pixels.

1.2.3 Noise Analysis

The noise optimization represents a crucial point in the IC design. In fact, the detector charge collection efficiency is tightly correlated to the noise level: the magnitude of the noise must be sufficiently low that, at the minimum signal level, it is still possible to have the required efficiency. Since the first amplifying stage gives the dominant contribution to the noise figure, it is possible to optimize the noise performance by minimizing the noise of the input stage. In fact, the noise in terms of equivalent noise charge can be written as follows ([9]):

$$Q_n^2 = i_n^2 F_i T_s + e_n^2 F_\nu \frac{C^2}{T_s} + F_{\nu f} A_f C^2 \tag{1.5}$$

where i_n is the input noise current spectral density, e_n is the input noise voltage spectral density, C is the sum of all capacitances shunting the input, A_f is the $1/f$ noise coefficient, T_s is the shaping time and F_i, F_ν and $F_{\nu f}$ are shape factors. Fig. 1.8 illustrates that voltage noise becomes dominant for smaller shaping times and current noise for larger shaping times; moreover it can be demonstrated that the minimum noise can be obtained with a

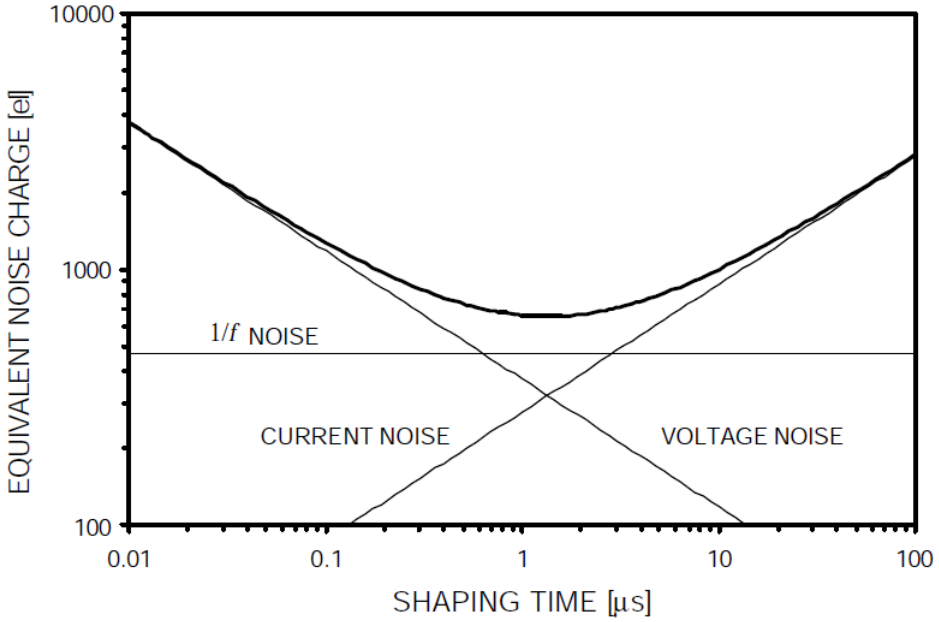

Figure 1.8: Equivalent noise charge versus shaping time ([9]).

shaping time of:

$$T_s = \frac{e_n}{i_n} C \sqrt{\frac{F_\nu}{F_i}}$$

The influence of the input capacitances and of the input transistor can be better understood by studying the signal to noise ratio at the input node:

$$\left(\frac{S}{N}\right)^2 = \frac{(\frac{Q}{C})^2}{e_n^2} = \frac{Q^2}{(C_d + C_{in})^2} \cdot \frac{g_m}{4\gamma kT}$$

where C_d is the capacitance due to the detector (pixel capacitance and inter-pixel capacitances), C_{in} is the MOS input capacitance, g_m is the transconductance and γ is a constant factor. In this case, both the current noise of the transistor and the detector noise are considered to be negligible. It is possible to maximize the signal to noise ratio by optimizing the device geometry. In fact, for $C_d \gg C_{in}$, the signal to noise ratio can be written as:

$$\left(\frac{S}{N}\right) \propto \frac{\sqrt{g_m}}{C_d}$$

For a transistor working in strong inversion, the transconductance increases as the device width is increased and, consequently, also the signal to noise ratio increases; however, the increase will stop as soon as the transistor capacitance will be the dominant contribution. For $C_d \ll C_{in}$ the signal to noise ratio can be written as:

$$\left(\frac{S}{N}\right) \propto \frac{\sqrt{g_m}}{C_{in}}$$

For a transistor working in strong inversion, both the transconductance and the input capacitance are directly proportional to the device width. Consequently, the signal to noise ratio is in inverse proportion to the square root of the transistor width:

$$\left(\frac{S}{N}\right) \propto \frac{1}{\sqrt{W}}$$

and it can be optimized by reducing the transistor width.
As already mentioned, the voltage noise spectral density is given by:

$$e_n^2 = 4\gamma \frac{kT}{g_m}$$

It is strongly dependent on the working condition of the input transistor. For a transistor working in saturation, the transconductance is given by:

$$g_m = \sqrt{2 I_d \mu \frac{\epsilon_{ox}}{d_{ox}} \frac{W}{L}}$$

In principle, by fixing the drain current and the MOS sizes, it is possible to see the intrinsic advantage of MOS scaling in terms of noise reduction ($e_n^2 \propto \sqrt{d_{ox}}$); however, by scaling the technology maintaining the same biases and sizes, it may be possible that the input transistor changes from strong to weak inversion, in which case the transconductance is no more given by the previous relationship. For a MOS transistor working in weak inversion, the transconductance is given by:

$$g_m \propto I_d \frac{q}{kT}$$

Consequently the relations between the noise voltage spectral density for a transistor working in strong inversion

$$e_{ns}^2 \propto \frac{1}{\sqrt{I_d}}$$

and in weak inversion

$$e_{nw}^2 \propto \frac{1}{I_d}$$

show the input noise scaling with the inverse of the square root of the current in the former case and with the inverse of the current in the latter case. In Fig. 1.9 it is possible to compare the transconductance in both cases: weak inversion for small drain current (linear relationship) and strong inversion for high drain current (square root relationship). The strong inversion regime is

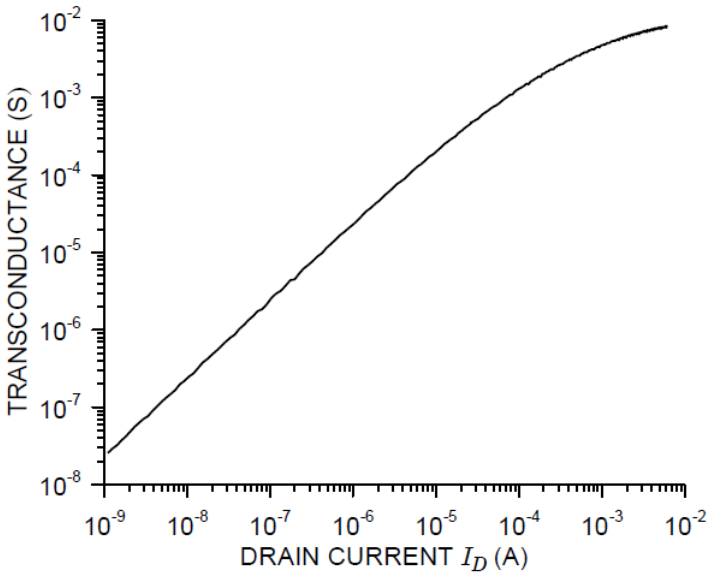

Figure 1.9: Transconductance vs Drain Current in a MOS transistor ([9])

commonly used when minimum noise is required because it allows to reach the highest transconductance value. Moreover, it allows to have the highest gain bandwidth product, given by:

$$f = \frac{g_m}{2\pi C_0}$$

However, using the transistor in strong inversion often yields prohibitive power consumption for low power applications like HEP, where usually weak inversion is preferred as it offers the maximum g_m/I ratio. Assuming the transistor to be in weak inversion, the square of the noise charge is proportional to the square of the input capacitance divided by the drain current:

$$Q_n^2 \propto \frac{C_{in}^2}{I_d}$$

For a constant noise charge Q_n, the power is therefore proportional to the current and, consequently, to the square of the input capacitance:

$$P \propto I_d \propto C_{in}^2$$

For hybrid pixel detectors the parasitic capacitance is often proportional to the perimeter and therefore segmenting further will be advantageous. In fact, supposing to be dominated by the perimeter parasitic capacitances, the input capacitance is proportional to the sensor perimeter:

$$C_{in} \propto 2l + 2p$$

where l is the cell length and p is the pitch. Consequently, the noise will be given by:

$$Q_n^2 \propto (2l + 2p)^2$$

In the strip case, the perimeter is dominated by the length:

$$Q_{ns}^2 \propto 4l^2$$

In the pixel case, the area covered by n strips is covered by $n \times n$ pixels having a pitch p and a length $l^1 = l/n$, where l is the length of the strips considered in the previous case. Consequently it is possible to write:

$$Q_{np}^2 \propto \left(2\frac{l}{n} + 2p\right)^2$$

In case of a square shaped pixel ($p = l/n$), the noise will be written as follow:

$$Q_{np}^2 \propto 16\frac{l^2}{n^2}$$

It is possible to study the noise improvement given by the pixel shaped detector compared to the strip shaped detector:

$$Q_{np}^2 \propto \frac{16\frac{l^2}{n^2}}{4l^2} Q_{ns}^2 = \frac{4}{n^2} Q_{ns}^2$$

The power consumption for a strip will be given by:

$$P_s \propto 4l^2$$

and for a pixel having a length l/n it will be:

$$P_p \propto 16\frac{l^2}{n^2}$$

By comparing the two power consumptions, it can be written:

$$P_p = \frac{4}{n^2} P_s$$

Since the power consumption for one pixel can be written as the power consumption of all pixels divided the number of pixels ($P_p = P_{p-tot}/(n \times n)$) and also the power consumption of one strip can be written following the same idea ($P_s = P_{s-tot}/n$), it can be written:

$$P_{p-tot} = \frac{4}{n} P_{s-tot}$$

The above illustrates the advantage of segmentation for analog power consumption. Of course beyond a certain segmentation, the reduction of the input capacitance will saturate and will no longer yield a further power reduction for the same noise level. Another important advantage of a pixel detector is its capability to deal with high trace density without generating ghost hits or ambiguity as in strip detectors for multiple hits. The main drawback of a hybrid pixel detector is its cost usually dominated by the bump bonding cost, which is normally larger than the cost for silicon sensors and the readout chips. For this reason only the central part of the detectors are typically implemented as hybrid pixel detectors, while the outer part are strip detectors to contain the cost. Hybrid pixel detectors now yield almost noise-free and unambiguous tracking information in the inner detectors of the LHC. Monolithic pixel detectors were not sufficiently mature at

the time of the construction of the present LHC detectors, but they do not suffer from the same cost penalty and even offer the perspective of improved performance. They are the topic of the next chapter.

Chapter 2

Monolithic Sensors

In this chapter, monolithic sensors will be discussed with their benefits (low capacitance, low material budget, low power consumption, low noise, low cost) and drawbacks (in particular the radiation hardness). The main approaches for monolithic integration will be presented with their device and circuitry solutions and their performance.

2.1 Monolithic Active Pixel Sensors

Monolithic devices integrate on the same substrate the sensor and the front-end electronics. Several developments have yielded functional pixel detectors. One of the most used approach is based on the so called Monolithic Active Pixel Sensors (MAPS), which traditionally collect charge by diffusion and hence offer reduced radiation tolerance, and which often have readout of the rolling shutter type usually not compatible with HEP requirements. The very significant advantage of MAPS is their compatibility with standard CMOS processing which allows a low price production. Some other developments also yielded functional devices and radiation tolerance, but required exotic process steps like double sided processing not compatible with standard CMOS manufacturing. For example, in the early $'90$ a successful prototype of monolithic detector in a non-standard CMOS process on high resistivity and fully depleted p-bulk was produced ([14]). It was based on a monolithic pixel array of 10×30 pixels measuring each $125 \times 34\ \mu m^2$. A schematic view of the device is shown in Fig. 2.1. It is based on a p-n junction made by a n-diffusion and a low doped p-substrate. The pixel is made

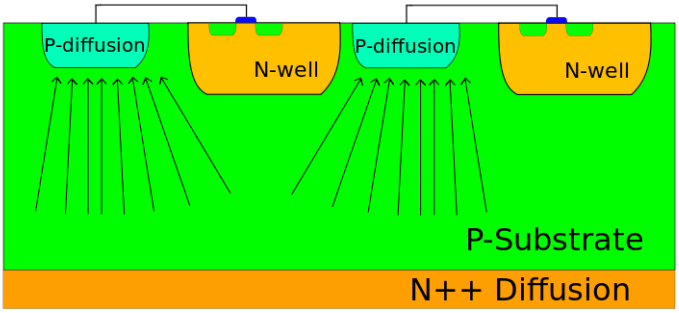

Figure 2.1: Schematic view of one of the first monolithic detectors built.

of a n-well containing the PMOS circuitry and a highly doped p-diffusion used as collection electrode. Both the n-well and the p-diffusion are placed in the p-substrate. The different doping level between the p-substrate and the p-diffusion allows the electron-hole pairs due to the impinging particle to flow towards the p-diffusion; the signal is sent to the adjacent n-well containing a first circuitry stage which produces a signal which is sent to the periphery where both types of transistors are used in p-wells and n-wells for the read-out electronics. This detector reached an effective capacitance of $\approx 25\ fF$ and it was used in a muon beam test obtaining excellent results: a 100% efficiency, a spatial resolution of 2.2 μm and a signal to noise ratio of 55; however no further development followed due to the complicated double side processes required for the backside diffusion.

As already mentioned, MAPS offer the opportunity to integrate analog and digital electronics together with the sensor in the same substrate. A schematic view of the typical pixel cell of a MAPS made in a CMOS technology is shown in Fig. 2.2. Most commercial CMOS technologies use only low resistivity silicon which is not suited for charge collection. However, some of them offer the possibility to grow a lightly doped epitaxial layer, having a thickness from a few μm to 20 μm, useful as active layer. In the epitaxial layer, a n-well used as collection electrode is built; another p-well highly doped is used to place the NMOS transistors used as amplifier. The signal at the output of the input NMOS transistor is usually sent to the periphery where double and triple well structures allow to use an appropriate readout electronics.

In MAPS there is usually no significant reverse substrate bias and therefore

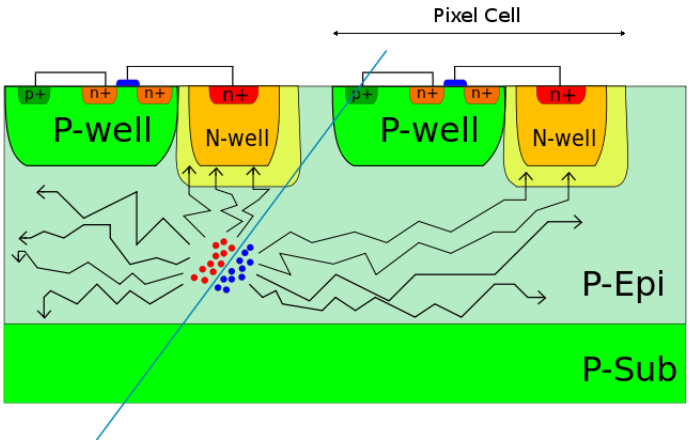

Figure 2.2: Schematic view of a MAPS (the yellow region represents the depleted volume).

most of the epitaxial layer remains undepleted, yielding charge collection dominated by diffusion in the absence of a significant electric field. As a result, the generated charges tend to spread over several pixels (see Fig. 2.3). It is possible to estimate the width of the charge carrier distribution. In fact, it is defined as:

$$\sigma = \sqrt{2Dt}$$

where D is the diffusion coefficient defined as:

$$D = \frac{kT}{q} \cdot \mu$$

and t is the collection time. For electrons spending 100 ns to reach the electrode (which is the typical collection time in a MAPS) at $T = 300\ K$, the width of the distribution is $\approx 20\ \mu m$: the diffusing charge is generally shared between neighboring pixels. Even with a charge carrier distribution width much higher than hybrid pixels, several prototypes of MAPS detectors have been reached an excellent spatial resolution ($\approx 1.5\ \mu m$ for the so called MIMOSA detectors, as explained in [15]). For MAPS devices the substrate represents a material which does not yield useful signal and, for HEP, it is therefore desiderable to use wafer thinning techniques to reduce this excess material and minimize scattering of particles in the detector.
The low leakage current is surely a key point in monolithic devices as it

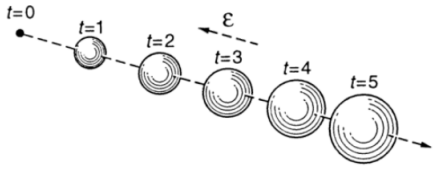

Figure 2.3: Schematic view of the widening effect due to diffusion: the charge cloud sizes increase with time ([8]).

contributes to the noise. Because in MAPS depletion is not complete, leakage current is typically collected only from a small fraction of the sensitive volume and, consequently, also the noise related to the leakage current is less than for fully depleted sensors.

A very important advantage of monolithic detectors is the possibility to reach a very low input capacitance, down to a few fF, because there is no need for bump bonding and the collection electrode is very small; moreover, since most of the capacitance is not to the neighboring pixel but to a fixed potential, the cross-talk between pixels is also reduced. This low capacitance value allows to reach very good signal to noise ratios for a low analog power consumption: even if the collected charge is less than for hybrid pixel detectors due to the smaller charge collection volume, the reduction in capacitance by a few orders of magnitude sometimes still yields better charge over input capacitance ratios and hence better signal to noise-power performance.

Another advantage of MAPS is the low cost compared with hybrid pixel detectors (potentially $\approx 25\ €/cm^2$).

With their high granularity, high signal to noise ratio, low power consumption and low cost, MAPS seem to be an interesting alternative to hybrid pixel sensors in vertex detectors of high energy experiments but their low radiation hardness, in particular for non ionizing radiation, does not allow to use them in a harsh radiation environment. In fact, the duration of the collection process increases the trapping probability making them more sensitive to the bulk radiation damage. Furthermore, the charges trapped in the undepleted volume are not subjected to any electric field: once a charge is trapped there is not the possibility to move it away from the trap. Consequently, it is possible to have groups of trapped charges causing undesired electric fields in the undepleted region. The radiation damage caused by

ionizing particles is much less influent than bulk damage. In fact, MAPS detectors take advantage of the intrinsic radiation hardness of sub-micron technology which is increasing with scaling. Nowadays, MAPS detectors can work in a reasonable performance regime up to a 10^{13} $n_{eq}/(cm^2 \cdot year)$ non ionizing fluence and a few $Mrad$ ionizing dose: this represents the main restriction to their use in the innermost layer of a vertex tracker in a hadron machine, in which the non ionizing fluence can reach values higher than 10^{14} $n_{eq}/(cm^2 \cdot year)$, while it is not an issue for lepton machines, in which the non ionizing fluence reach values around 10^{12} $n_{eq}/(cm^2 \cdot year)$ (Table 2.1).

A second limitation of traditional MAPS is the impossibility to use full

Machine	Luminosity $[cm^{-2} \cdot s^{-1}]$	Non Ionizing Fluence $[n_{eq} \cdot cm^{-2} \cdot yr^{-1}]$	Ionizing Dose $[kRad \cdot yr^{-1}]$
LHC	10^{34}	1.4×10^{14}	11300
Super LHC	10^{35}	1.4×10^{15}	71400
ILC	10^{34}	1.0×10^{11}	50
CLIC	$10^{34} - 10^{35}$	1.0×10^{11}	70
Super Belle	10^{35}	6.0×10^{11}	500
RHIC	8×10^{27}	3.0×10^{12}	80

Table 2.1: Main accelerator machines built or to be built in the future with their nominal luminosity, non ionizing fluence and ionizing dose.

CMOS in the pixel: an additional N-well necessary for the PMOS transistors would compete with the N-well collection electrode to collect the signal charge, and can result in charge loss and even loss of detection efficiency (Fig. 2.4). This NMOS only limitation in the pixel is actually quite a significant constraint for the design of the readout circuitry. Finally, the CMOS technology is optimized for general purpose electronics and not for detector devices: consequently, there is a low flexibility in the processes. Despite the availability of specific CMOS imagers technologies, these are often oriented towards the detection of visible light only and hence do not generally offer very thick epitaxial layers which would yield a more advantageous signal for HEP.

Nevertheless, despite some of these drawbacks, very promising results have been obtained by the MIMOSA (Minimum Ionizing MOnolithic Active pixel Sensor) collaboration. The first prototype has been produced in the late ′90 in a 0.6 μm AMS CMOS technology ([16]). The chip has been divided in

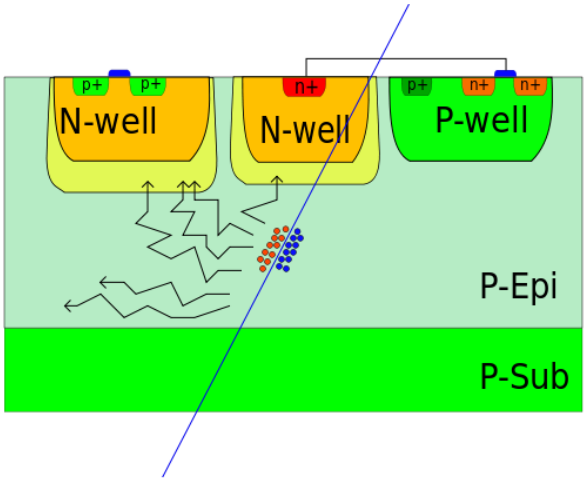

Figure 2.4: Schematic view of the competitive effect between the electrode and the N-well used for the circuitry.

four matrices having small design differences. Each matrix consists of 64×64 pixels having a pitch of 20 μm: each pixel is made of four diodes connected in parallel; in this way it is possible to reduce the charge dispersion and the collection time at the expense of a larger capacitance, hence a lower charge to voltage conversion gain and a higher noise. The signal at the output of the pixel is read by a three transistors structure ($3T$) implemented in the pixel itself. A schematic view of the readout system is shown in Fig. 2.5. The three transistors structure is based on a reset transistor, which resets the diode voltage, a source follower transistor and a row selector transistor, which allows to read the signal of the pixel: in this way the low power consumption is guaranteed by the activation of the pixel circuitry only during the read-out phase avoiding to have power dissipation due to digital clock signals driving large capacitances. Usually the sensor works in a so called *rolling shutter* mode: all pixels in one raw are read in parallel by using the row-selector transistor. During the test of the chip, the possibility to reach a capacitance in a few fF range and a charge collection time of ≈ 150 ns were demonstrated. The measured noise was estimated to be a few e^- ENC and, after a beam test, the efficiency reached by the sensor was close to 100% with a spatial resolution of a few μm. The sensitivity to neutron irradiation has been investigated obtaining a charge-to-voltage conversion almost constant up to the highest fluence (10^{13} n/cm^2). An increase of the leakage current

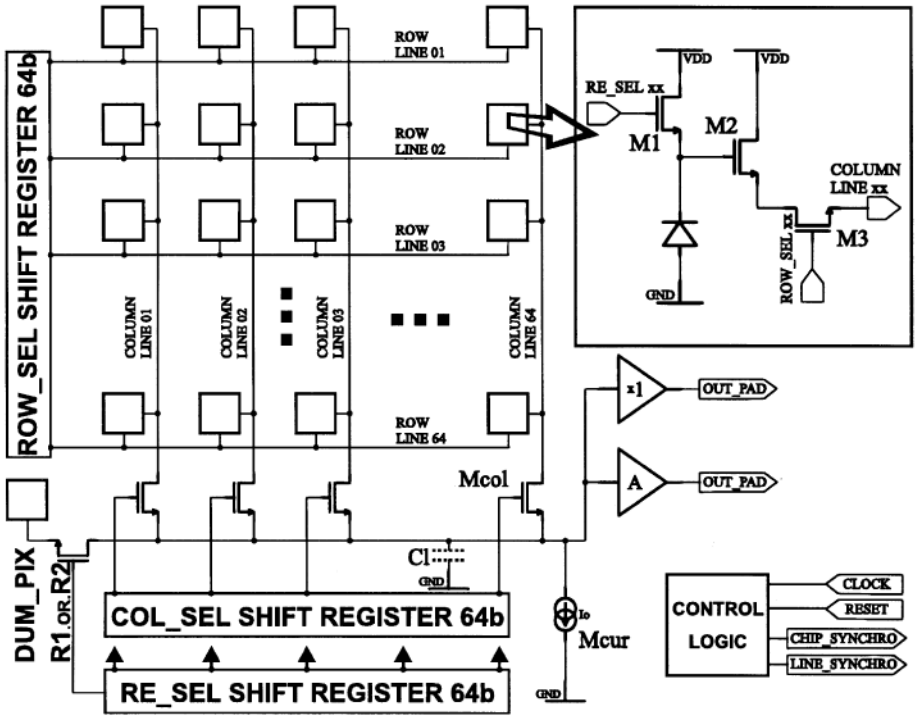

Figure 2.5: Schematic view of the readout chain of the MIMOSA 1 chip.

of an order of magnitude (from a few fA per diode to a few tens of fA per diode) has been observed without a significant noise penalty. However, charge losses have been observed for fluence exceeding $\approx 10^{12}$ n/cm^2 ([16]). Even more interesting is one of the last prototypes produced, $MIMOSA-28$, the second large scale sensor of the MIMOSA series ([18]). It has been produced in a 0.35 μm AMS CMOS technology, with an epitaxial layer of 20 μm and a pixel pitch of 20 μm. A matrix of ≈ 0.9 million pixels divided in 960 columns of 928 pixels, for an active area of 19.9×19.2 mm^2 has been designed. In each column, the pixels are read sequentially with a typical read-out time of ≈ 200 ns by a rolling shutter based read-out; the columns are read in parallel. The readout circuit is based on a common source stage and a source follower stage (Fig. 2.6). The power consumption of the sensor has been measured to be ≈ 150 mW/cm^2. The noise has been estimated to be $\approx 15e^-$ ENC per pixel. After a beam test, the efficiency of the system has been calculated to be $\approx 100\%$ with a resolution of ≈ 3 μm. These same performance have been obtained also for irradiated sensors up to a 150 $kRad$

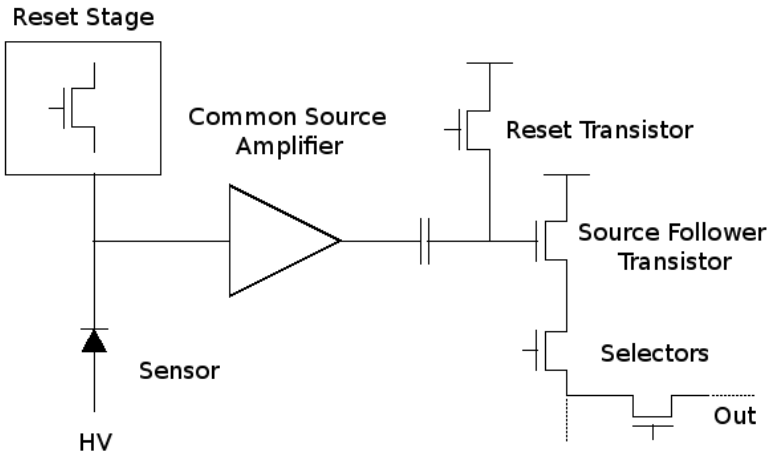

Figure 2.6: Schematic view of the readout chain of the MIMOSA-28 chip.

ionizing dose and a $3 \cdot 10^{12}$ n/cm^2 non ionizing fluence.

2.2 Deep N-well MAPS

Deep n-well (DNW) MAPS ([19]) devices represent an interesting evolution of classical MAPS in terms of read-out speed. They have the possibility to implement at pixel level the standard front-end electronics used for hybrid pixel sensors (see 1.2.2) by taking the advantage of modern submicron triple well CMOS commercial technology, where a n-well with a deep junction is available to have a better insulation of the NMOS transistors from the substrate and the neighboring digital devices. A schematic view of the sensor is shown in Fig. 2.7. The deep n-well is the collecting electrode; the triple well process allows to have a p-well placed in the n-well to have the possibility to use also NMOS transistors. A more complex circuitry than standard MAPS can be used to process the signal: a charge amplifier, a shaper and a discriminator. By using a charge preamplifier, the charge sensitivity is almost independent on the capacitance of the electrode allowing to have a large area sensor. There is also the possibility to have standard n-wells which contain PMOS devices for the analog and the digital part; their area has to be minimized to avoid to capture part of the signal from the deep n-well: the degradation of the charge collection efficiency depends on the ratio between

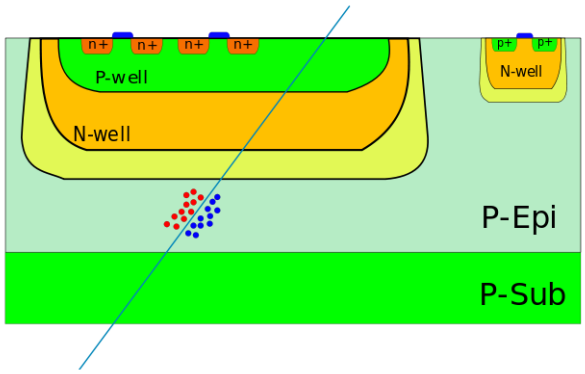

Figure 2.7: Schematic view of a DNW MAPS (the yellow region represents the depleted volume).

the deep n-well sensor and the n-well used to place the PMOS transistors. However, even by minimizing the area of the small n-wells, it is not possible to eliminate completely the charge loss.
By following the deep n-well approach, interesting results have been obtained with the APSEL prototypes series mostly produced in a 130 nm technology. In Fig. 2.8 it is possible to see a schematic view of the typical front-end of the APSEL series ([25]). The preamplifier is based on a cascode stage

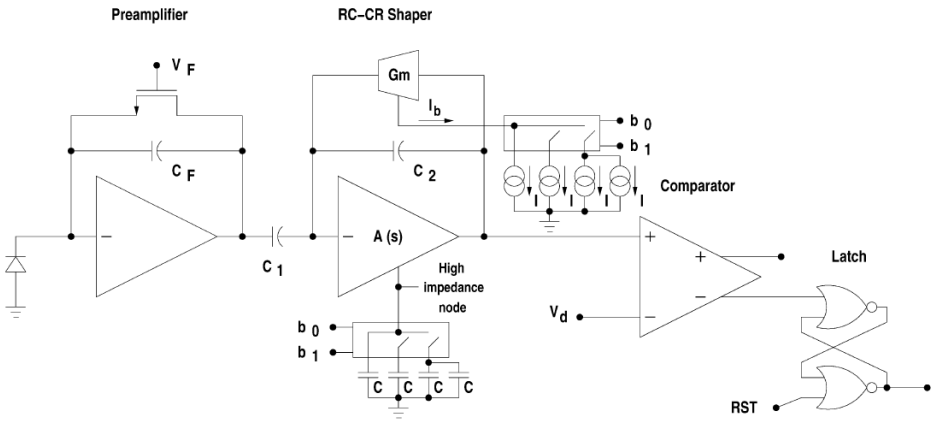

Figure 2.8: Schematic view of the typical front-end electronics of the APSEL chip series.

with a capacitive feedback: the capacitance of a few fF, implemented using a MOS capacitor, allows to achieve a large charge sensitivity. The charge sensitive amplifier is AC coupled with a RC-CR shaper; it is based on a high

gain amplifier with a capacitive and transconductive feedback. The input capacitance, the feedback capacitance and the transconductive feedback allow to program the peaking time (see [25]) to deal with the charge collection time of the monolithic detector. The transconductive feedback (Fig. 2.9)

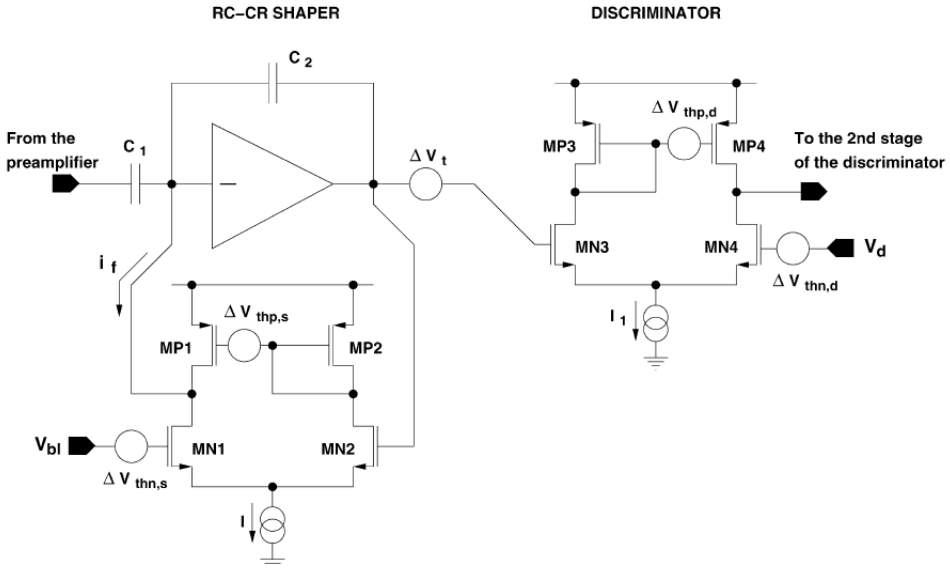

Figure 2.9: Schematic view of the RC-CR shaper and the discriminator of the APSEL chip series.

is based on a differential pair providing current at the input when a signal arrives at the input of the shaper amplifier. The signal at the shaper output is compared to an external voltage by a comparator and the binary information is then stored in a NOR latch.
A chip of that series obtaining interesting results is the APSEL4D chip. It is based on a 4096 pixels matrix, 32 rows by 128 columns, with a pitch of 50 μm for an estimated capacitance of 300 fF, an average gain of 890 mV/fC, a power consumption of $\approx$ 35 μW per pixel and a noise of $\approx 75e^{-}$; the efficiency has been measured to be higher than 90% and the resolution slightly lower than 15 μm.

2.3 INMAPS

Another interesting solution to the competitive effect between n-wells is represented by the INMAPS devices ([26]); their approach allows to use

both type of transistors in a monolithic device by using a p-implant forming a deep p-well which screens the n-well used to place the PMOS transistors (Fig. 2.10): the deep p-well prevents the charge collection of the N-well containing the PMOS transistors and the associated signal loss. It therefore allows the use of full CMOS circuitry in the pixel without penalty. By

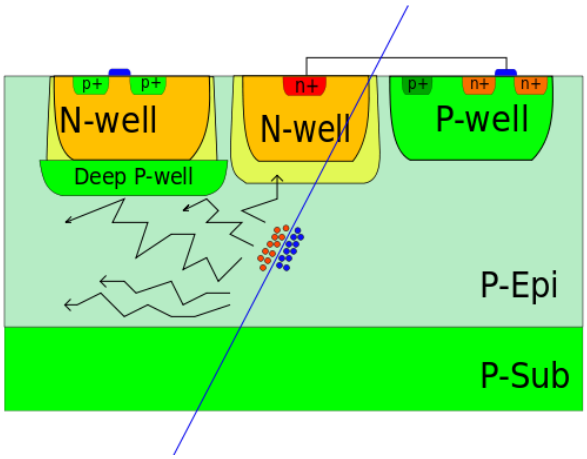

Figure 2.10: Schematic view of a INMAPS (the yellow region represents the depleted volume).

using both type of transistors, it is possible to develop a more complex read-out electronics, compared to standard MAPS read-out electronics. In Fig. 2.11 and Fig. 2.12, two possible read-out electronics used in [26] are shown. In the former, a double sampling approach, similar to a conventional MAPS device, is used: a so called *pre-sample stage* buffers the voltage drop on the diode node and a charge amplifier is used to generate a voltage step proportional to the input. A reference signal previously stored in a sampling capacitor is used to obtain a pseudo-differential signal which is then sent to the remaining part of the read-out electronics. In the second circuit, a pre-amplifier is used to amplify the collected charge. Moreover, a CR-RC shaper is used to generate a signal with peak and decay time proportional to the input. The input of the shaper stage is also used as reference to obtain a pseudo-differential signal.

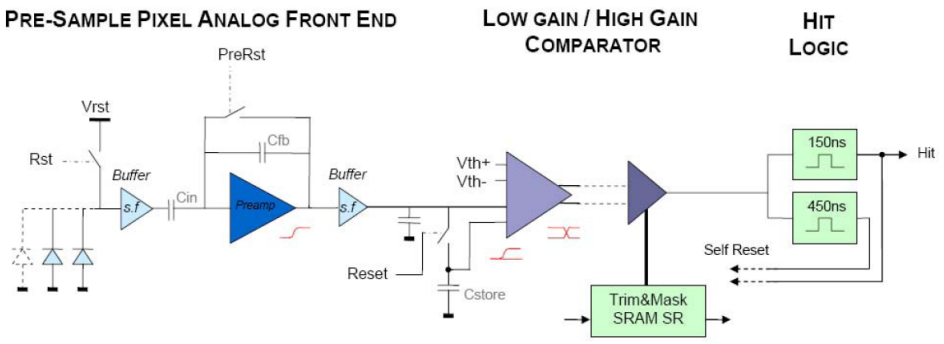

Figure 2.11: INMAPS read-out electronics based on a pre-sample pixel analog front-end.

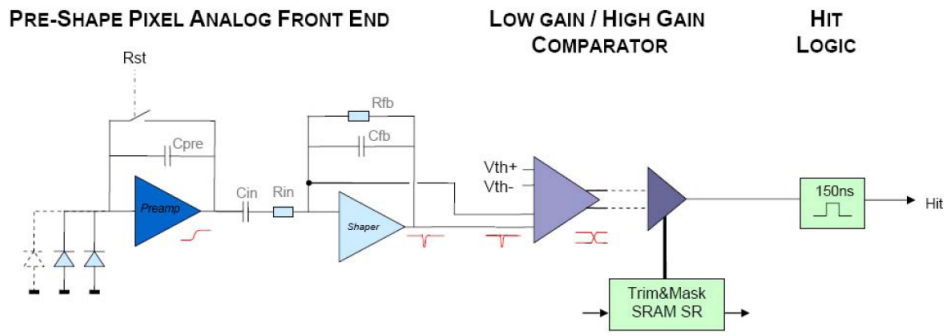

Figure 2.12: INMAPS read-out electronics based on a pre-shape pixel analog front-end.

2.4 High Voltage MAPS

An innovative approach to monolithic detectors is represented by the so called High-Voltage (HV) MAPS: they take the advantage of high voltage CMOS technology to develop a detector. In this context, the term *high voltage* means a voltage significantly higher than the standard low voltage applied to CMOS devices. By using this technology it is possible to apply a voltage bias to the substrate higher that 50 V offering two advantages compared to a standard MAPS: increased depletion thickness (and hence more signal), and charge collection by drift yielding faster signals and better radiation tolerance (as the charge has much less time to be trapped before being collected).

Interesting results in this field has been obtained by [28]. In that project,

a 0.35 μm CMOS technology has been used to produce a small matrix of 50×50 μm^2 pixels. A schematic view of the detector is shown in Fig. 2.13:

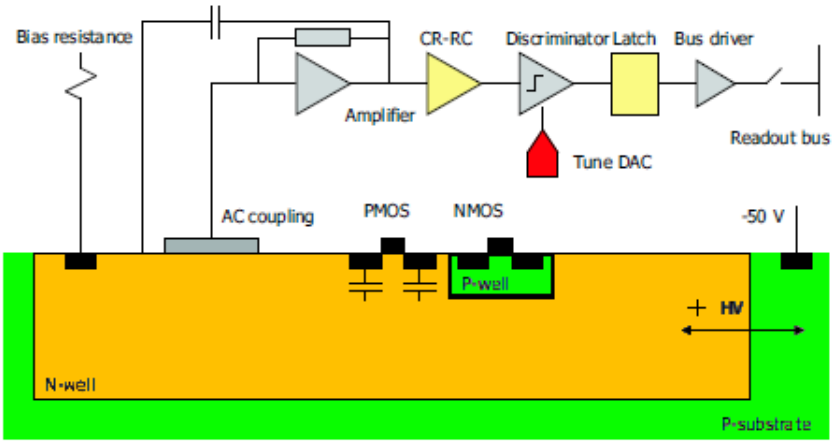

Figure 2.13: Schematic view of a HV MAPS detector ([28]).

a deep n-well is placed in a p-substrate and it is used as main collecting electrode; the substrate is negatively biased down to $50V - 60$ V. Inside the n-well electrode, both PMOS transistors and a p-well containing NMOS transistors are placed, allowing to take the advantage of the complementary MOS structures of the CMOS technology. The n-well is biased by V_{dd} through a high value resistor ($R \approx G\Omega$) to avoid to have the charge flowing to the positive power supply before the amplifier can react. The sensor is AC coupled to the front-end electronics based on a charge sensitive amplifier with a constant current feedback used to discharge the capacitive feedback, a shaper based on a $CR - RC$ filter, a threshold discriminator and a latch. The charge sensitive amplifier is based on a folded cascode stage (Fig. 2.14). The p-diffusions (a,b,c and d in Fig. 2.14) are capacitively coupled with the n-well and can be source of cross-talk; however, the diffusions a,b and c are connected to voltage values almost constant and represent only a parasitic contribute to the detector capacitance; the diffusion d connects the output with the n-well and represents a capacitive feedback regulating the charge amplifier gain ($V_{out} = Q_{in}/C_{fb}$). Since the p-diffusion of the $M1$ transistor can be made narrow, the feedback capacitance is relatively low ($C_{fb} \approx 1\ fF$) and it guarantees a high gain. The dominant parasitic capacitance is due to the P-well containing the NMOS transistors. The ΔV between the p-well

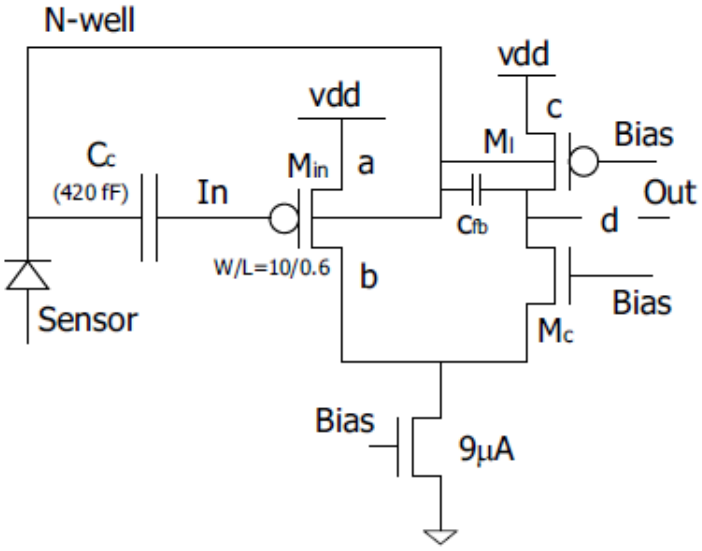

Figure 2.14: Charge sensitive amplifier of the HV MAPS ([28]).

and the n-well is only a few volts and, consequently, the depletion region is small and the capacitance is high (see formula 1.2 and 1.3). The detector capacitance has been estimated to be $\approx 38\ fF$ and the parasitic capacitance is $\approx 180\ fF$. In terms of performance, the detector has been able to be depleted up to $\approx 9\ \mu m$ for a reverse bias of $\approx 60\ V$, with a detector noise $85e^-$ and a threshold dispersion of $75e^-$ for a minimum detectable signal of $6\sigma_{noise} = 960e^-$ and a 100% fill factor.
Interesting results have been obtained also from another prototype of the HV MAPS collaboration ([29]). The new prototype implemented in a 0.35 μm CMOS technology is based on a matrix of 128×128 pixels of $21 \times 21\ \mu m^2$. In this prototype the P-well has been eliminated by implementing the front-end electronics only in PMOS (see Fig. 2.15). This significantly reduced the parasitic capacitance compared to the previous prototype. Moreover, using only PMOS transistors offers also the advantage of lower radiation induced transistor leakage. The front-end electronics is shown in Fig. 2.16: the sensor is AC coupled with the source follower through the capacitance C_c; a reset transistor (Rst_1) is used to bias the n-well before the acquisition time: in this way it is possible both to have the bulk of the PMOS at the highest voltage and the n-well floating during the acquisition. A second reset transistor (Rst_2) is used to bias the gate of the source follower. The voltage

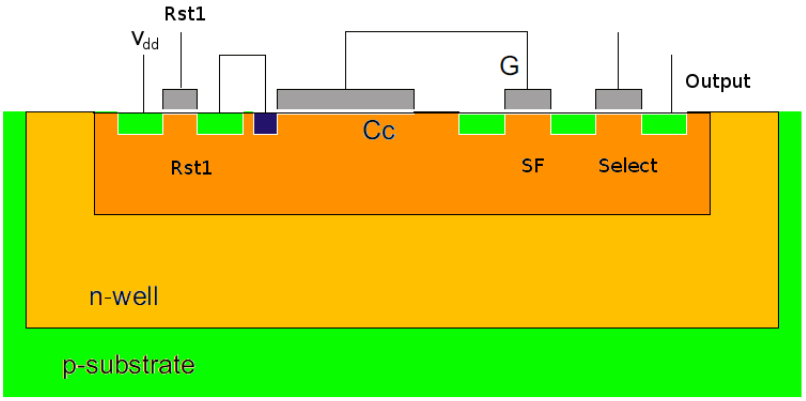

Figure 2.15: New prototype of HV MAPS.

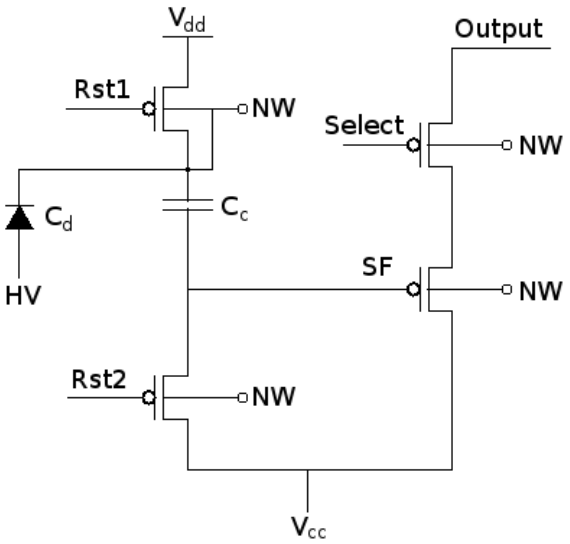

Figure 2.16: Front-end electronics of the new HV MAPS prototype based only on PMOS transistors.

signal at the source follower input is $V = Q_{in}/C_d$; the signal is then stored at the output where it will be treated by a voltage amplifier and digitalized by an ADC. The output readout is based on the rolling-shutter method. The main results obtained by testing this prototype are a spatial resolution of $\approx 7\ \mu m$, a detection efficiency higher 85%, a noise of $90e^-$ and a power consumption of the pixel matrix of $8\ mW$.

2.5 Silicon on Insulator

Silicon on Insulator (SOI) technology represents an interesting alternative to CMOS technology which is reaching its performance limits with ultra deep submicron nodes, such as 45 nm and 32 nm, in terms of power consumption and speed. The possibility to use high-resistivity bulk material maintaining CMOS processing of electronics circuits makes them interesting also for particles detector applications. A schematic view of a SOI detector is shown in Fig. 2.17 ([32]). An oxide layer (of a 10 nm to 5 μm thickness) is grown on a

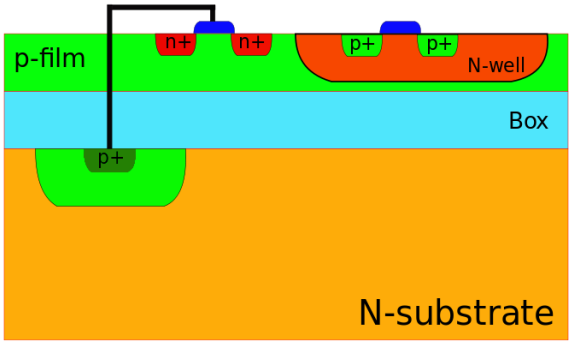

Figure 2.17: Schematic view of a SOI detector (the clear green part represents the depletion region due to the pn junction).

n-type substrate. The circuitry is built on a silicon film layer, usually floating, resting on the silicon dioxide layer. A p-well in the n-substrate is used as collecting electrode; the sensor is DC coupled with the front-end electronics by a connection (typically tungsten) passing through the oxide and the silicon film. The buried oxide (Box) acts as excellent isolation between the sensor and the circuitry allowing to place an n-well in the front-end electronics and, consequently, to use both types of transistors (NMOS and PMOS) having more flexibility in the electronics design. Furthermore, it acts as dielectric barrier reducing considerably the substrate noise (in particular the digital noise affecting the analog circuit), the junction capacitance (in fact, the junctions and the bulk are now separated by the oxide), the cross-talk between neighbor circuits via substrate (which is now totally isolated) and the latch-up problem. The decreasing of the parasitic capacitances and the parasitic current allows to have better performance in terms of speed and power consumption. However, the main drawback is represented by the low

radiation hardness due to the Box which is highly sensitive to ionizing radiation damage. Consequently, they can find more applications as soft radiation detector (such as X-ray and near visible), for which radiation damage is not an issue.
By applying a reverse bias it is also possible to obtain a fully depleted substrate. The main problem due to the back bias is the so called *back gate effect*: the transistors placed in the silicon film are close to the sensor where the high voltage bias applied influences the transistor threshold; in fact, the Box acts as a secondary parasitic gate causing the previous mentioned issue (see Fig. 2.18). It can be solved by placing a low-doped p-implant surround-

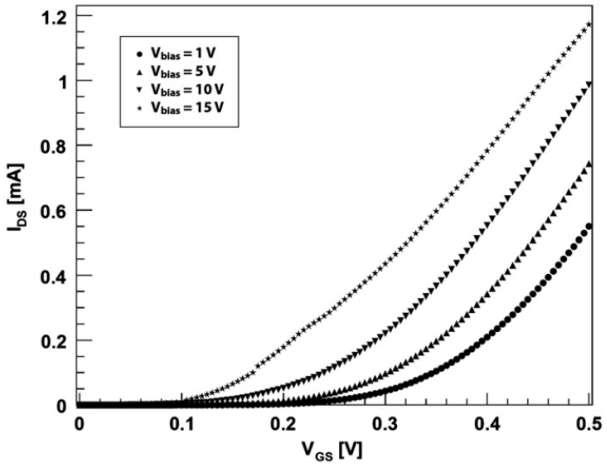

Figure 2.18: Shift of the threshold voltage for different substrate biases for a NMOS transistor (from [33]).

ing the p+ electrode which shields the transistors in the SOI.
The SOI Pixel Collaboration is obtaining interesting results in SOI application, in particular with the $SOImager-2$ sensor ([35]), designed in a 0.2 μm SOI technology. The sensitive area is made by a 256×256 pixels matrix having a pitch of 13.75 μm. The front-end is based on a 3T configuration and the pixels are read-out by four parallel arrays of 64 columns each by the rolling shutter method. Measurements results show an efficiency close to 100%, a signal to noise ratio up to 50 and a point resolution down to 1.07 μm.

Chapter 3

LePix

The LePix project explores monolithic pixel sensors fabricated in a 90 nm CMOS technology on a high resistivity substrate. The sensor has the advantage of a monolithic device and offers also the possibility to collect charge by drift applying a reverse bias to the substrate; consequently there is the possibility to reach interesting performance in terms of signal to noise ratio and radiation tolerance. In this chapter the technology and foundry choices, the sensor principle and some practical device implementations will be shown; in particular, the main solutions used to deal with the technology limitations will be discussed. Only the detecting device will be treated: the circuitry implementation to process the signal will be described in the following chapters.

3.1 Technology Choice

The goal of the LePix project is to produce a monolithic detector exploiting charge collection based on drift. The initial $R\&D$ involved several institutes: $INFN$, $IPHC$, $C4i-MIND$ and $CERN$ with some small financial contributions from some other institutes. The approach is similar to the HV MAPS: by applying a reverse bias to the junction it is possible to obtain a thick depletion layer in the substrate and charge collection by drift. The process is a standard CMOS technology implemented on a substrate of moderately high resistivity ($\approx 1k\Omega cm$). There is some risk related to the isolation of the CMOS from the high voltage but the resistivity higher than available in HV CMOS offers higher depletion thickness and hence more

signal.
The technology and the foundry choices are strictly related to the target performance of the detector. To reach the goal of a fully depleted substrate, the high resistivity processes are preferred (see Fig. 3.1). Nowadays, several foundries offer CMOS technology on substrate of moderate resistivity ($50 - 100\ \Omega cm$) down to the 0.18 μm processes; some foundries offer also substrates on high resistivity on CMOS technologies beyond 0.18 μm. A

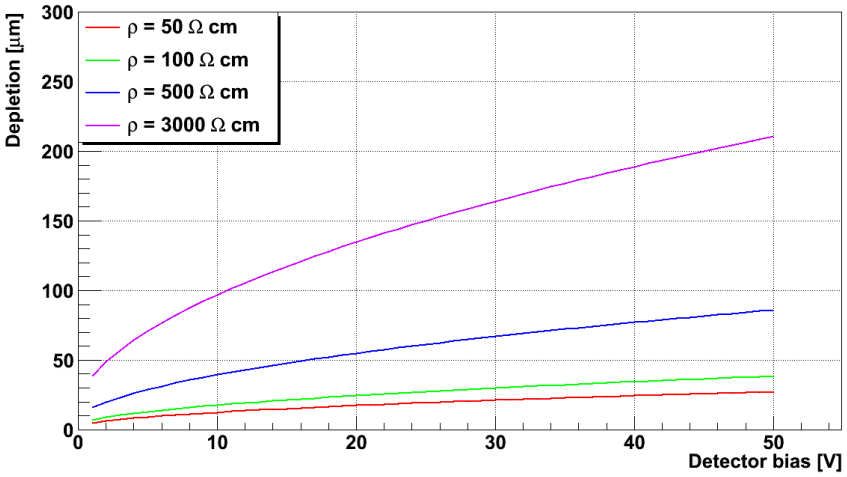

Figure 3.1: Depletion region depth vs substrate voltage at different resistivity values (from moderate to high resistivity) for an ideal planar abrupt junction.

high resistivity process on a very deep submicron technology results particularly useful in terms of signal to noise ratio. In fact, as already mentioned, the high resistivity is helpful to fully deplete the substrate and, moreover, a technology node smaller than 0.18 μm gives access to the lowest possible input capacitance and, consequently, a higher charge to voltage conversion and a better signal to noise ratio (see chapter 1).
Some foundries offer also a 90 nm CMOS technology with low-k dielectrics in the metal stack, offering high metal density with only moderate parasitic capacitance. This is an important advantage for monolithic detectors as the required metal routing can be quite dense. Therefore, such 90 nm technology was chosen to implement the device. However, the technology has also a drawback: the cost of a very deep submicron technology is an order of magnitude higher than a submicron technology (the mask cost increases

significantly for smaller line widths); a realistic estimation of the project development is based on a couple of iterations to establish the validity of the approach plus another couple of iterations to make a large scale prototype. On one hand, a detector based on the LePix approach could represent an interesting solution for its cheap production in large scale which allows to use it as the main detector of a tracker; on the other hand, the $R\&D$ phase is considerably more expensive than a typical $R\&D$ made on standard MAPS. Moreover, the project offers more challenges than standard MAPS: the rules imposed by the foundry and to be respected for manufacturability (e.g. the layer density rules) and the physical implementation of the device in a standard CMOS technology (in particular because of the necessity to deal with a technology which has not been thought to work with a strongly reversed substrate).

3.2 Sensor Principle

The detector chip is made of a matrix divided in two parts: an active area with the sensitive elements, placed in the center of the chip, and a periphery with the read-out electronics (see Fig. 3.2). The sensitive part is made of a two dimensional array of n-wells diffused into a p-substrate of high resistivity (500 Ωcm). Each of the n-wells forms the collection electrode of the pixel; each electrode contains a local read-out circuit. The local read-out of the pixel is connected to the periphery where the remaining part of the read-out circuit is placed in a triple well structure, to be isolated from the substrate voltage bias. Charge collection electrode and read-out circuitry are biased near ground (a power supply of $\approx 1\ V$, typical of the very deep submicron technology). The p-substrate is negatively biased to several tens of Volt by a top side contact placed outside the guard ring surrounding the read-out circuit and the detector matrix. By applying a sufficient reverse substrate bias, a continuous depletion layer should be formed underneath the readout circuitry and the detector matrix, which ends near the outer edge of the guard ring and which has a thickness of several tens of microns. The periphery area treats the signals coming from the in-pixel frontend. It is based on double and triple well structures on the p-substrate which allow to use both type of CMOS transistors. The area of the n-well placed in the p-substrate at the periphery has to minimize the competitive detecting

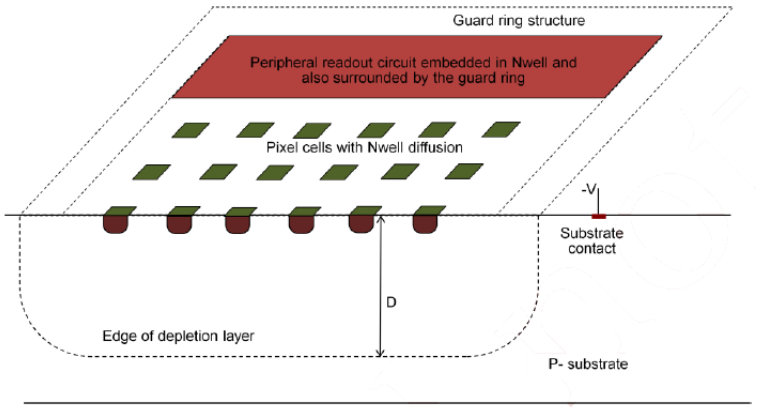

Figure 3.2: Schematic view of the detector structure showing the central part with the sensitive elements (n-well diffusions), the periphery placed in the n-well and the guard ring.

effect with the n-well structures placed in the central part of the matrix which are the sensitive elements of the chip; consequently, the area of the periphery is considerably lower than the area of the central part.
The main device challenges in the design phase are the depletion layer uniformity with small collection electrodes, the significant reverse bias of the substrate, incompatible with the standard protection structures against electrostatic discharge which typically are heavily connected to the substrate, and then finally the layer density rules: this set of problems will be further discussed in the next paragraphs.

3.3 Device Design

To maximize the signal to noise ratio, the size of the collection electrode should be minimized to reduce the input capacitance. However, reverse biasing a small electrode typically results in a non-uniform, bowl-shaped depletion. Consequently, it is not possible to use the planar junction approximation but a spherical junction approximation has to be used at least for moderate reverse biases. The depletion depth in a spherical junction, approximating the electrode to be spherical, is given by (see [36]):

$$d = \sqrt[3]{\frac{3\epsilon R}{qN} \cdot (V_{bi} + V_{appl})} \tag{3.1}$$

where ϵ is the dielectric coefficient of the medium, N is the substrate doping level, q is the electron charge, R is the radius of the spherical electrode, V_{bi} is the built in voltage and V_{appl} is the bias applied at the junction: it is possible to see the cubic root dependency on the bias voltage V_{appl}, instead of the square root of the planar junction, which requires higher substrate voltage to reach a 100% fill factor. In Fig. 3.3 it is possible to see the depletion

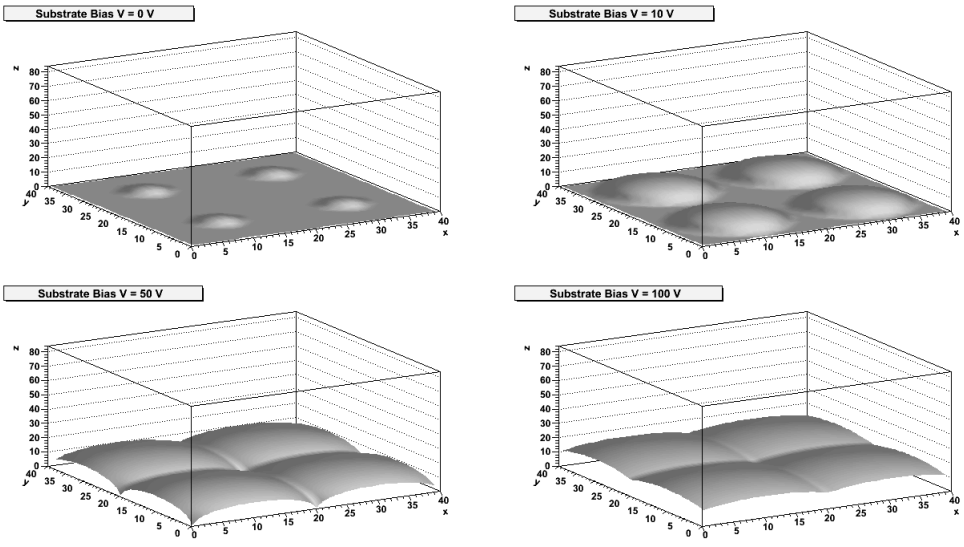

Figure 3.3: Depletion region shape for an ideal spherical pn junction ($V_{bi} \approx 0.7\ V$) having 1 μm semi-spherical electrodes with a pitch of 20 μm placed in a moderate resistivity substrate $\rho = 100\ \Omega cm$ for different substrate bias values.

region depth for a p-substrate of moderate resistivity ($\rho = 100\ \Omega cm$) with spherical n-wells having a radius of 1 μm and a pitch of 20 μm: the depleted region does not cover the full detector area up to $V_{appl} = 50\ V$ but there are some regions which are not depleted because of the bowl-shaped depletion layer. For substrate biases higher than $V_{appl} = 50\ V$, the depletion bowls of different electrodes start to merge allowing to have a depletion over the full area. It is possible to optimize the fill factor also for lower substrate voltages by working on the pitch of the electrodes or the doping level of the substrate, even if the latter is a less flexible parameter due to the limitations imposed by the foundry. In Fig. 3.4 it is possible to see a simulation made with the same parameters of the previous simulation but with a pixel pitch of 10 μm: already at a substrate bias around $V_{appl} = 10\ V$ it is possible to

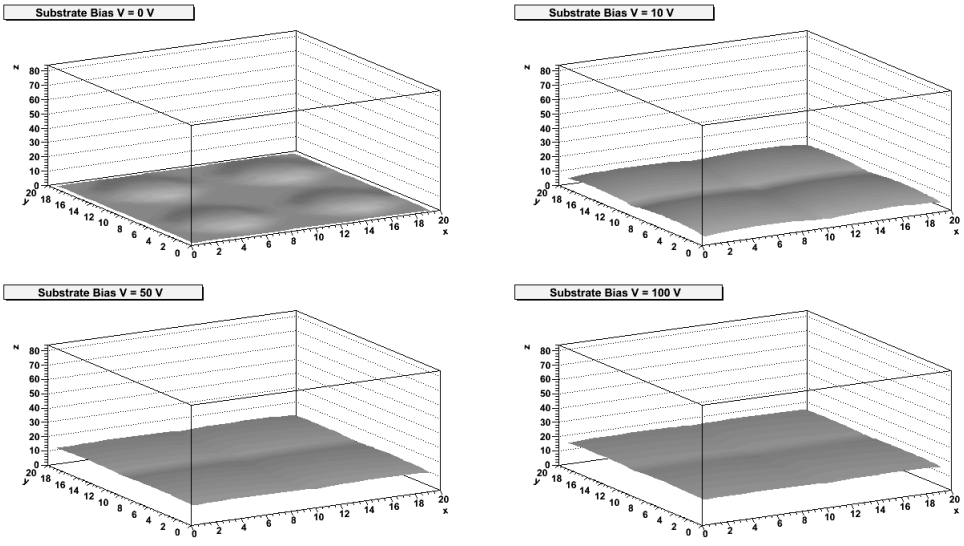

Figure 3.4: Depletion region shape for an ideal spherical pn junction ($V_{bi} \approx 0.7\ V$) having 1 μm semi-spherical electrodes with a pitch of 10 μm placed in a moderate resistivity substrate $\rho = 100\ \Omega cm$ for different substrate bias values.

have depletion over the full area. However, by reducing the pixel pitch it is possible to increase the capacitive coupling phenomena between neighbor pixels leading to the cross-talk problem. In Fig. 3.5 it is possible to see a simulation of a spherical ideal junction biased at $V_{bias} = 50\ V$ for different doping levels, from moderate to high resistivity: as already mentioned, a higher resistivity level allows to reach sooner a depletion over the full area. The goal of the LePix device design phase has been to obtain a structure combining small collection electrodes with uniform depletion maximizing the pixel pitch. During the simulation phase, a very low dose n-type implant over the full area of the matrix has been used: the n-implant is contacted by the small n-well diffusions forming the collection electrode. At low reverse biases, the low dose n-implant combined with the n-well diffusions would behave like a normal planar junction with an uniform depletion. However, at a certain point, the low dose implant would fully deplete as well, leaving the n-well diffusion, which would not fully deplete, as isolated collection electrodes in the matrix. The principle has been extensively verified by software simulation using a pixel pitch of 100 μm and a moderate substrate resistivity: the uniformity of the depletion has been obtained for a $\approx 100\ V$

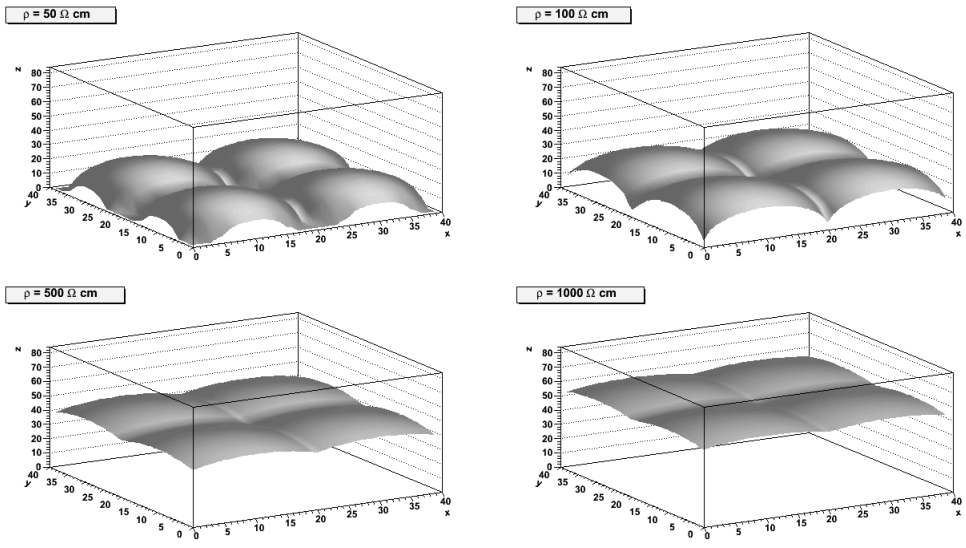

Figure 3.5: Depletion region for a spherical junction having 1 μm semi-spherical electrodes with a pitch of 20 μm, a substrate voltage of $V_{appl} = 50\ V$ at different resistivity values.

reverse bias; afterwards, the foundry offered also a high resistivity substrate ($\rho \approx 500\ \Omega cm$), which could be easily depleted. In Fig. 3.7 it is possible to

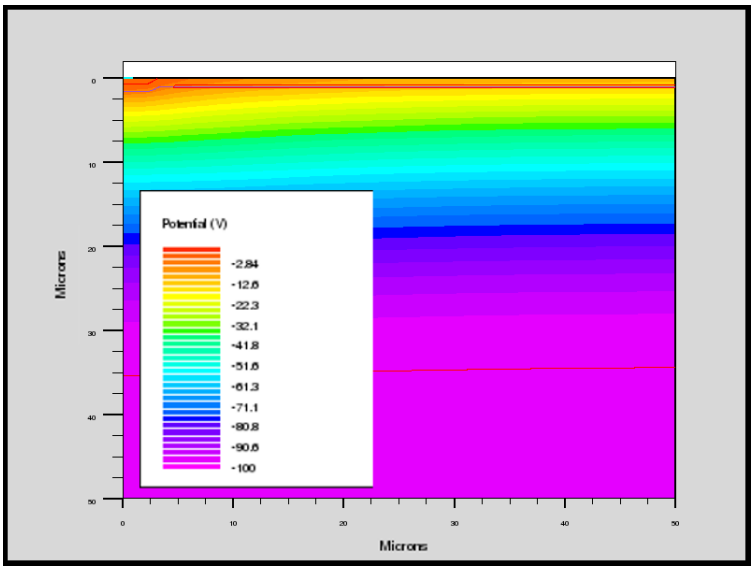

Figure 3.6: 2D device simulation illustrating a uniform depletion of $\approx 50\ \mu m$ at 100 V for an electrode of $\approx 5\ \mu m$ (with an n-implant over the area surrounding the electrode) and a substrate resistivity of $\rho \approx 50\ \Omega cm$.

see the basic pixel cell structure: in a p-type substrate, a n-well structure is placed surrounded by the n-implant previously described. Inside the n-well electrode, the input PMOS transistor of the readout circuit is placed: in this way it is possible to avoid having other low-doped p-wells, commonly used in the classical MAPS, which could interfere with the depletion region. Only a few devices can be placed in the electrode, due to the small sizes of the collecting element ($\approx 4 \times 4\ \mu m^2$ or $\approx 5 \times 5\ \mu m^2$). Consequently,

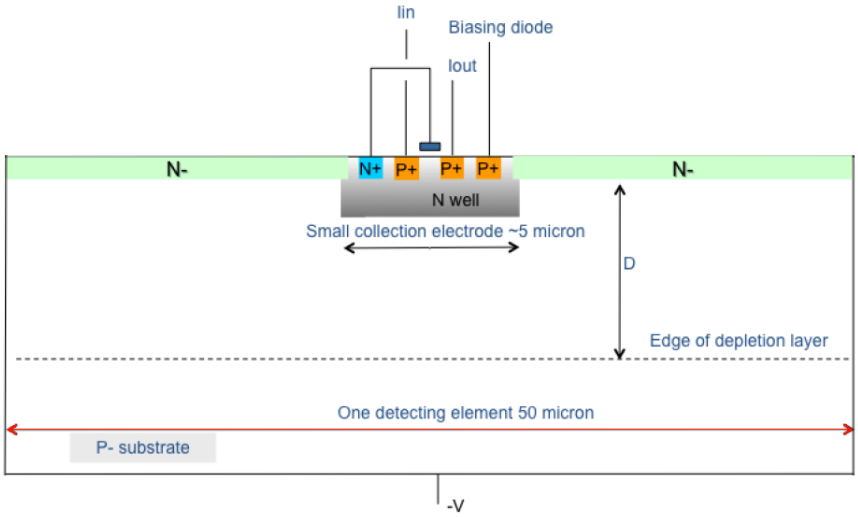

Figure 3.7: Schematic view of the pixel cell structure.

an analog signal is sent to the periphery, where it will be treated by the readout circuitry. The intrinsic advantage of this approach is the low power consumption due to missing clock distribution to every pixel. In fact, by considering a detector capacitance of a few tens of fF, the power consumption of a device with an in-pixel clock signal working at tens of MHz rate and biased at 1 V is a few mW per cm^2; by sending an analog signal to the periphery, it is possible not to use a clock signal for every pixel and, consequently, to limit the power consumption; however, for prototypes in large scale, a high density line, available in very deep submicron technology such as the 90 nm CMOS technology, is required to connect every pixel to the periphery.

3.4 Practical Device Implementation

In the previous section the utility of a n-implant to have a uniform depletion region has been explained; however, the low dose n-implant is not standard in the 90 nm CMOS technology used. Consequently, a special mask (the mask of the threshold implant of the high V_{th} transistors which are not used in the project) has been implemented; the pattern and the area of this layer has been highly influenced by the density rules of the technology. Moreover, polysilicon over the field had to be designed to reach the minimum polysilicon density: the polysilicon has been patterned on the shallow trench isolation. Also the metal layer has to follow the minimum density rule: it has been placed over the lowly doped active areas. The real impact of these two layers on the sensitive structure was not known in advance: the silicon-oxide interface under the shallow trench isolation over undoped substrate and the metal field region over the N-areas are not standard and may contain interface states or fixed oxide charges interfering with the signal charge. To have the possibility to act on the electric field on the silicon surface, the polysilicon layer and the metal layer have been biased by using a pad contacting both of them. In Fig. 3.8 a schematic view of the pixel cell with

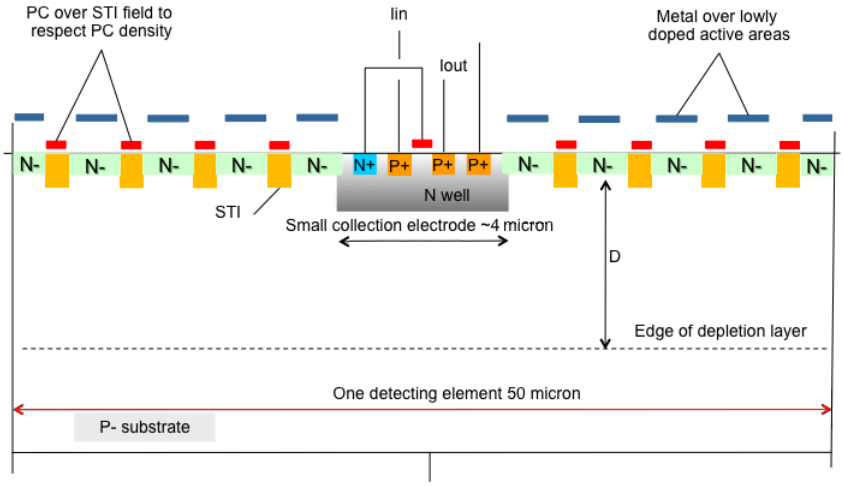

Figure 3.8: Schematic view of the pixel cell structure with the low-doped n-implant, the polysilicon layer and the metal layer.

the pattern used to respect the density rules of the technology is shown. An effort has been made to obtain a good approximation to a blanket low dose implant, yielding an unusual pattern for the pixel layout (shown in Fig. 3.9)

which maximizes the density of active area around the collection electrode. A continuous interaction with the foundry has been necessary to obtain only low dose implant and avoid the standard implant in the active area; other important requirements have been the automatic filling and the silicidation of the special active areas which have to be avoided. Moreover, another important issue was the design verification because design rules check for these special layers did not exist. From the circuitry point of view, the elec-

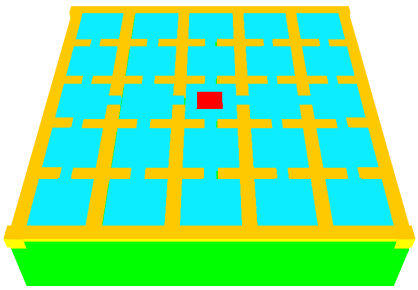

Figure 3.9: 3D view of the pixel cell layout: the red cube is the n-well collection electrode in the p-substrate (green), the orange lines represent the polysilicon layer and the blue cubes represent the low dose n-implant.

trostatic discharge (ESD) protection has represented an interesting design challenge. The electrostatic discharges are phenomena due to the transient discharge of static charge ([39]) which force the chip components to work outside their usual range: they are usually characterized by a transient of high voltage ($\approx kV$) or high current (from $\approx 1\ A$ to $\approx 10\ A$) having short transient time (usually $0.2-200\ ns$) which could cause oxide breakdown and thermal damage, such as interconnections burnout, in the integrated circuit. The ESD protection allows to protect the circuit when an ESD event occurs between two pins by shunting the current between them and by limiting the voltage drop between them. Usually, in integrated circuits the ESD protection is tightly connected to the substrate. In the LePix device this is not possible due to the negative bias voltage of the substrate. To satisfy the mandatory request to place ESD protection in the chip, a triple well structure has been used: in the n-well placed in the chip periphery, used for the readout electronics, a p-well structure connected to the circuit ground is used to connect the ESD protection between the p-well itself and the n-well. The chips submitted by the LePix project are not only matrices contain-

ing both the pixel and the front-end electronics. More simple structures have also been produced to test the sensor separately from the circuitry. In particular, the structures submitted are a large area diode, to test the reliability of the 90 *nm* CMOS technology with high substrate bias voltage, a so called *breakdown* structure, to test different geometries of the sensor and some matrices structures, to test both the detecting sensor and the frontend electronics connected together. The structures have been produced with the same layout on standard and high resistivity wafers. The standard substrate submission has been the first one to be received and tested; however, during the initial measurements, a short in the guard-ring has been discovered and the lot on high resistivity has been put on hold to have the possibility to correct the bug. The short did not allow to test deeply the structures but it has been possible to determine the high influence of the substrate-field oxide interface. In fact, in the initial version, the metal layer placed over the field oxide was directly connected to the analog ground line of the chip, thus not allowing to have control of the electric field on the silicon-oxide interface (this will better explained in the next chapters). However, since most of the masks had been already produced, only a few corrections have been possible; in particular, the short in the guard-ring has been removed and the metal has been disconnected from the ground line and linked to the polysilicon layer.
All the structures submitted on the high resistivity wafer will be described in detail in the next chapters, showing both the design solutions adopted and the results of the measurements done on the chips.

Chapter 4

Diode Structure

In this chapter, the diode structure will be described; in particular, the attention will be focused on the layout of the structure, the equipment used to test the diode and the measurements done to characterize the sensor. All the tests shown have been performed at CERN.

4.1 Diode Strategy

The diode is a simple structure based on a p-n junction and a guard ring designed to test the performance of the 90 nm technology in terms of high voltage tolerance, capacitance and leakage current of the sensor as a function of reverse bias. The considered technology has not been thought to be used for particles sensor and, consequently, it has not been optimized for that purpose. A simple schematic view of the sensor is shown in Fig. 4.1. The diode is formed by an n-well implant in the high resistivity p-type substrate; it is equipped with a guard ring structure, which includes rings in poly silicon over field oxide which can be biased using a resistor. This poly silicon resistor runs over field oxide from the edge of the Nwell forming the diode over the guard ring area to the exterior, crossing the different poly rings which thus are each connected to a tap of the resistor. There is a contact to the resistor on the inside of the guard ring structure and on the outside to which bias can be applied. These poly rings in addition to undoped active areas were imposed because of density rules in this deep sub micron technology. The structure has therefore four biasing contacts: a contact to the n-well, one to the substrate and the two contacts for the resistor. All pads for the

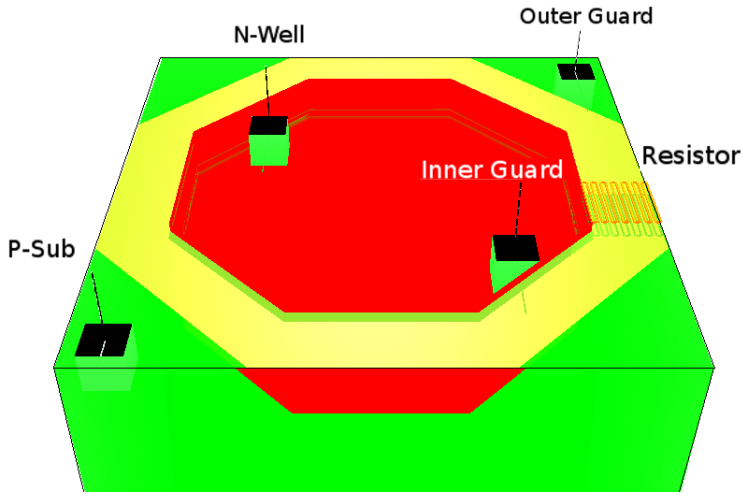

Figure 4.1: Schematic view of the diode structure and its pad contacts.

contacts are placed on the top part of the sensor. The n-well is octagonally shaped, as shown in Fig. 4.2. The distance between the two inner sides of the guard ring passing through the n-well in the central part of the diode is $\approx 915\ \mu m$ while the guard ring is about 200 μm wide. The diode surface can be approximated as a square having an area of 0.77 mm^2. The thickness of the structure is around 300 μm. The sensor size is considerably larger than single pixels in the matrix, but the purpose here was not to perform small capacitance measurements but to study the tolerance of the technology to high voltage and the depletion behavior. In any case, direct capacitance measurements in the low fF range are out of reach for many instruments and the input capacitance of the pixels has been measured using the matrices. Here there is just the diode without any circuitry. The structure reproduces approximately the layout used for the matrix with a central part based on the n-well, which is the sensitive part of the device, and the guard ring: in the matrix, the inner contact of the guard ring is shorted with the contact used to bias the polysilicon layer (whose layout has been explained in the previous chapter) while the outer contact is independent also in the matrix.

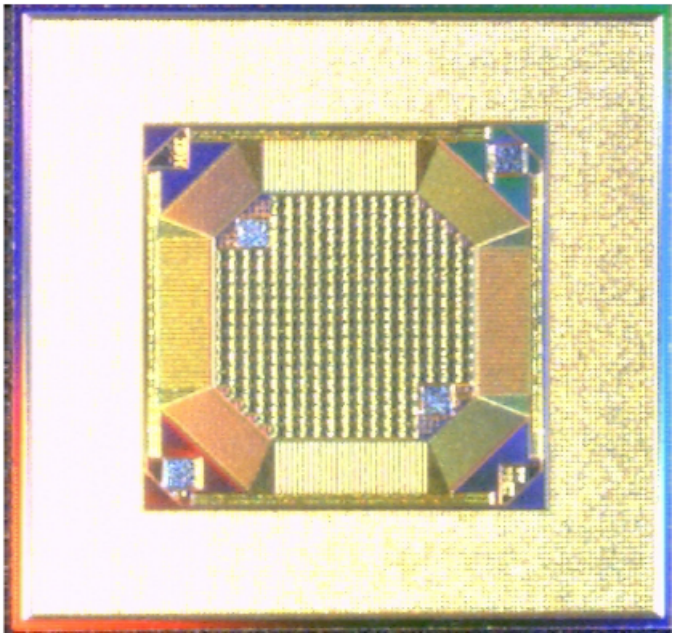

Figure 4.2: Picture of the diode structure.

4.2 Experimental Equipment

The tests performed on the structure are mainly $I-V$ and $C-V$ measurements. A schematic view of the setup is shown in Fig. 4.3: the right part is used to perform current measurement while the left part is used to perform capacitance measurements.

During the current measurement, the diode is reverse biased and the current flowing through the sensor is measured; the high voltage is applied on one pin of the sensor while the current is measured on the other pin: in this way it is possible to avoid using the current meter with its terminals at a high voltage respect to ground. A *Keithley 2410* has been used to reverse bias the junction while a *Keithley 6487* (high precision current meter) has been used to measure the current.

The circuit used to perform $C-V$ measurements on the reverse biased junction is slightly different. A high voltage power supply (*Keithley 237*) is used to reverse bias the junction; a LRC meter (*Agilent E4980A*) is used as AC voltage source and it performs the detector capacitance measurement. The amplitude and the frequency of the AC signal can be set externally. By applying an AC voltage and measuring the resulting AC current, the LRC

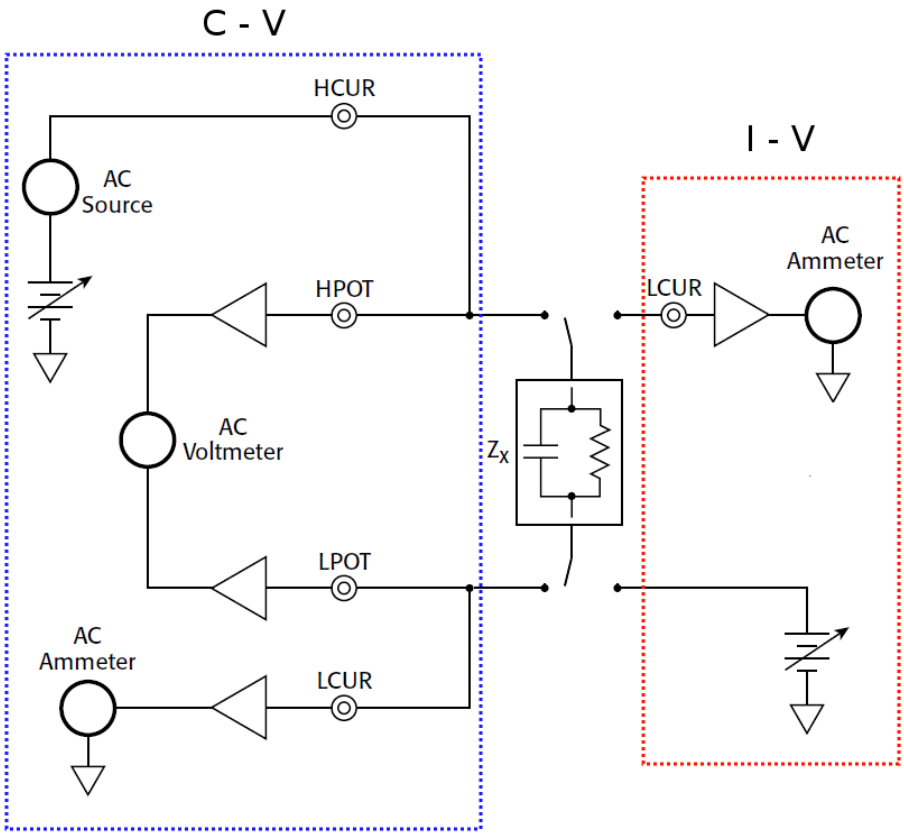

Figure 4.3: Setup used to perform the $I-V$ (on the right with the power supply providing the desired bias) and $C-V$ (on the left, with the power supply providing the desired bias and the AC source providing the desired amplitude and frequency used to measure the capacitance value) measurements.

meter can estimate the impedance of the device and, consequently, the capacitance value: the biases are sent to the equivalent circuit called Z_x in Fig. 4.3 and the admittance Y (which is the inverse of the impedance) of the capacitive bridge is measured as:

$$Y = \frac{1}{R} + j\omega C$$

where C and R are respectively the detector capacitance and the resistor in parallel and $\omega/2\pi$ is the frequency of the AC signal. The current flowing through the device is measured by a low current terminal (LCUR) while the

voltage drop on the device is measured by high and low potential terminals (LPOT and HPOT). There is also a second possible approach to estimate the capacitance of the sensor based on measurements done with the resistor in series (no more in parallel) to the capacitance which should give the same results. However, this solution has not been implemented in the experimental setup. In Fig. 4.4 the probe-station used to test the diode structure

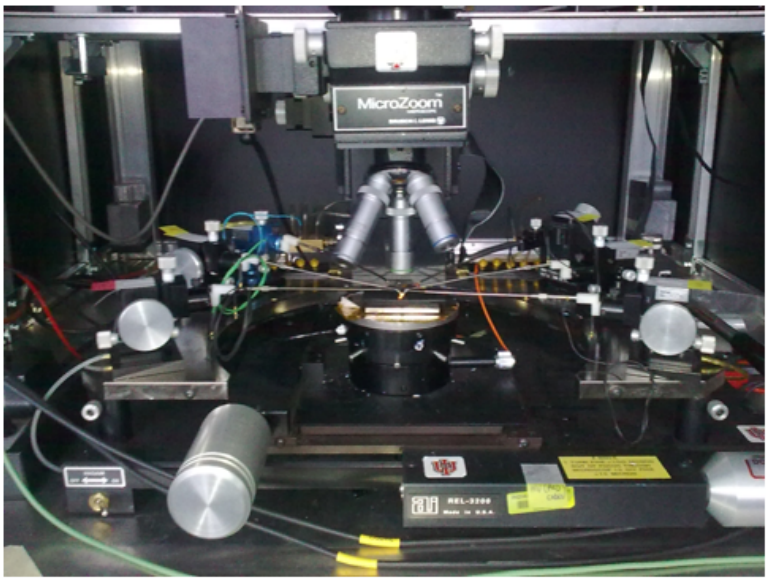

Figure 4.4: Probe-station used to perform the $I-V$ and $C-V$ measurements.

is shown. It is a LabView controlled probe station based on a chuck, used to back-bias the substrate, and some needles, used to bias the sensor. The probe-station is placed in a cupboard which can be closed to avoid to have the leakage current of the sensor influenced by external light and to shield from external interference. As an alternative to the connection with needles a printed board circuit (Fig. 4.5) has been produced to mount the diode on. In this way, it is possible to use the wire bonding technique to connect the pads of the sensor to the PCB lines and, by using small SMA connectors, it is possible to bias the sensor. Lines on the PCB match 50 Ω for a good impedance matching. By using the wire bonds, possible scratches caused by the needles contacting the pads are avoided. Two PCB lines are used to place a thermistor to evaluate the PCB temperature, which should be, in first approximation, the same temperature of the diode: in fact, the sensor

is connected to the PCB by using a thermally conductive glue.

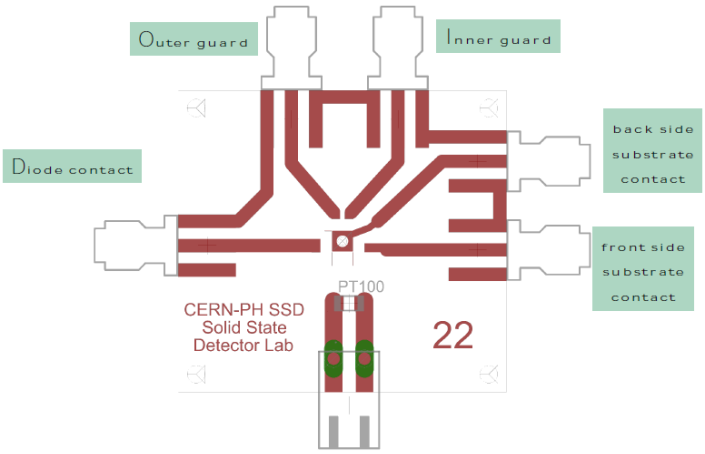

Figure 4.5: PCB used to test the diode.

4.3 Measurement Results

The measurements on the diode structure are current-voltage measurements, which have to establish the breakdown voltage and the possible existence of parasitic current coming from the edge of the sensor, and capacitance-voltage characteristics, used to evaluate the capacitance value, the depletion region depth and to estimate the doping profile.

4.3.1 Leakage Current Measurements

During the $I-V$ measurements, the n-well has been biased at a fixed potential ($V_{n-well} = 0$ V) and a negative voltage sweep has been done on the substrate terminal up to a possible voltage breakdown: in this way it is possible to reproduce the same testing conditions of the matrix, where the substrate is biased negatively. The inner guard contact has been negatively biased (V_{ig} = -30 V) to better reproduce the matrix conditions (this point will better explained later). The outer guard has been biased at different voltage values to see how much the current flowing in the diode is influenced by a voltage drop on the guard ring. The measurements have been taken at room temperature. In Fig. 4.6, the result of the $I-V$ test is shown. A

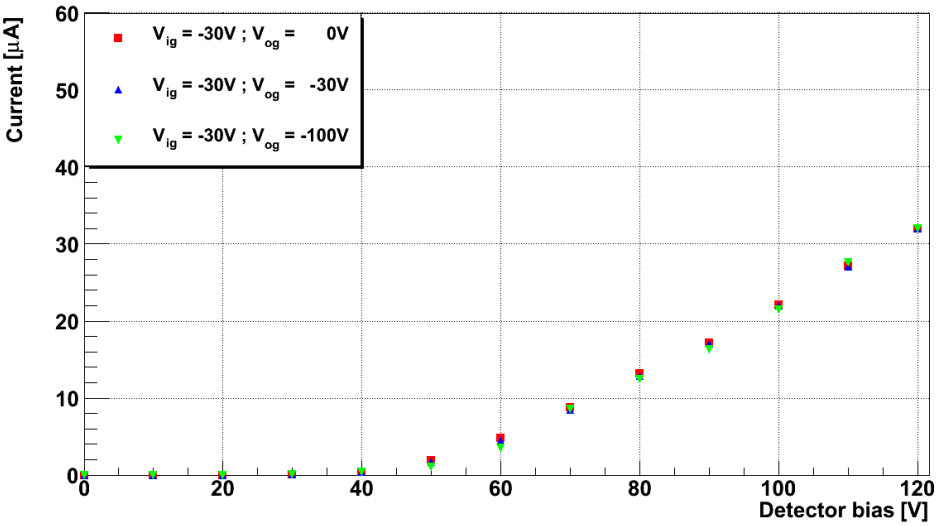

Figure 4.6: I-V curve at different outer guard voltage values.

large step sweep ($\Delta V = 10\ V$) has been done on the substrate voltage and the outer guard ring voltage value has been changed. The voltage value of the substrate is shown in absolute value. It is possible to see a negligible current flowing in the diode for voltage value below $|V_{sub}| < 40\ V$, while it is possible to see a current of a few tens of micro-Ampere flowing for higher substrate values; moreover, the current starts to flow independently on the outer guardring value. It is clearly visible that the current flowing is not due to a breakdown because of the constant slope of the curve; consequently, the current could be due to a parasitic current coming from the edges of the sensor. However, the $\approx 270\ \mu m$ distance between the electrode and the lateral surfaces of the chip cannot be covered by the depletion layer with a $40\ V$ substrate bias unless a conductive path between the electrode and the edges aids the current to flow in the diode independently on the outer guard voltage value. In Fig. 4.7 and Fig. 4.8 it is possible to see a simplified schematic view of a guard ring structure section: the polysilicon rings are alternated with a field oxide layer; no field plates are used on the oxide layer and, consequently, it is not possible to act on the electric field underneath the field oxide. It has to be noted that the N-areas in between the shallow trench isolation are non-standard in the technology. Normally active areas not covered by polysilicon gate are very heavily doped, but here the doping

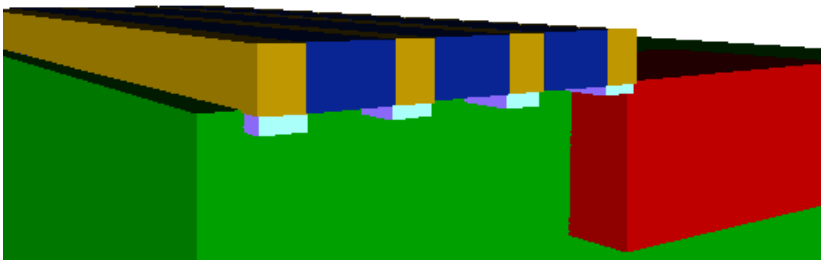

Figure 4.7: Simplified view of the guard ring structure with the substrate (green), the n-well (red), the polysilicon layer (gold) over the shallow trench isolation (light blue) and the field oxide layer (blue).

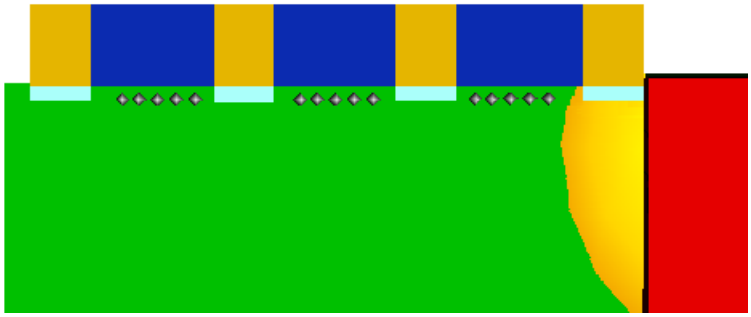

Figure 4.8: Simplified view of the conductive path due to the interface states and the oxide charges in the region not covered by polysilicon gate.

is much less, making the actual presence of interface states or oxide charge no longer irrelevant. A parasitic path from the N-well to the diode edge is caused by an inversion layer due to a combination of fixed oxide charges and interface states in the low doped active area (it will better explained in the next chapter). As soon as the depletion region touches the conductive path, an irregular extension of the depletion region is created which is now close to the sensor edges. Consequently, the voltage bias applied on the outer guard ring has no influence because it does not allow to remove the trapped negative charge from the silicon-oxide interface. In the matrix structure a metal layer is present over the lowly doped active areas allowing the trapped charge to be removed by negatively biasing the metal electrode. Since in the matrix the metal layer and the polysilicon layer are shorted, once the metal is negatively biased, also the polysilicon will be at the same potential (this

is why the polysilicon contact has been negatively biased during the diode test). Removing the inversion layer charge in the guard ring of the diode is not possible because there is no metal electrode over the lowly doped active areas and the polysilicon over the shallow trench isolation is too far away to be effective in controlling the interface states in these N-areas. A sweep by changing the inner guardring value has been also done (Fig. 4.9): smaller steps on the substrate has been used and the outer guard contact has been shorted with the inner, as the bias on the guard has been proven not to have any influence. Fig. 4.9 illustrates that the current is totally insensitive to the bias of the guard ring. The sweep on the guard ring voltage shows no

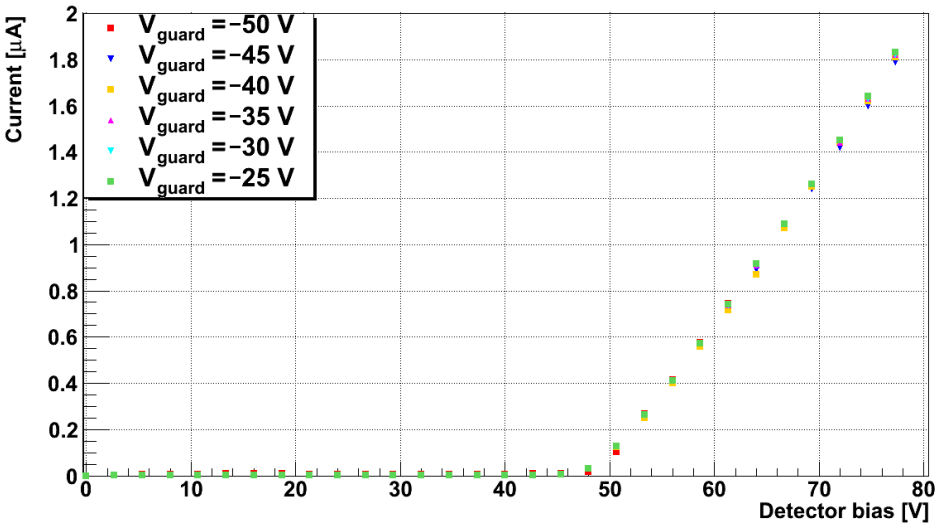

Figure 4.9: I-V curves for different values of guard ring biased (the inner and the outer guard are shorted).

influence at all also of the inner guard ring bias on the substrate current. In Fig. 4.10 the $I-V$ curve in logarithmic scale for a diode having the guard ring biased at $V_{gr} = -30\ V$ is shown: the current flowing in the sensor for substrate biases $|V_{sub}| < 40\ V$ is below one nanoAmpere. This result is extremely interesting in term of leakage current for a small sizes pixel. In fact, as already mentioned in the equation 1.4, the leakage current for a reverse biased diode is proportional to the depleted area:

$$I_{leak} \propto S$$

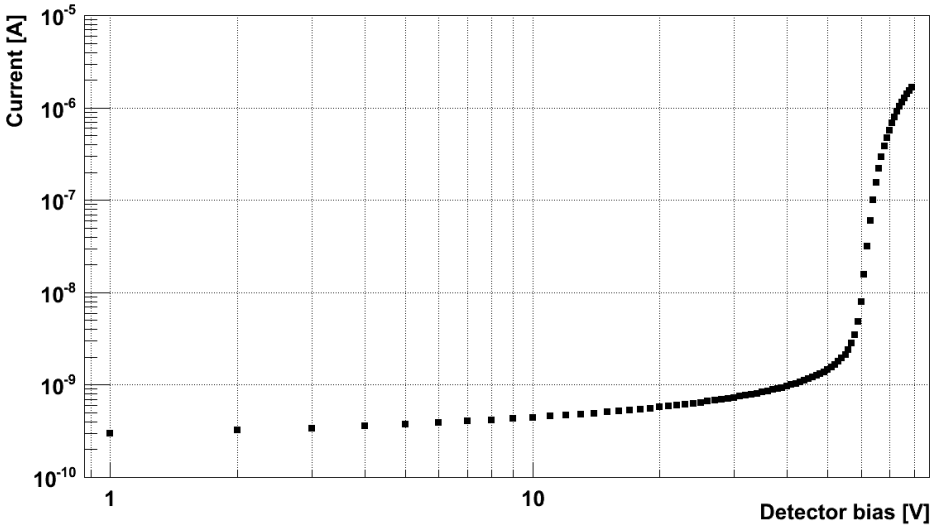

Figure 4.10: I-V curves in logarithmic scale for a diode having the guard ring biased at $V_{gr} = -30\ V$.

and the depleted area of a small sizes pixel is supposed to be more than two orders of magnitude lower than the diode tested ($\approx 0.77\ mm^2$ for the diode structure and $\approx 2500\ \mu m^2$ for the final pixel design). Consequently, assuming - in first approximation - a planar and abrupt junction with the same depletion depth both for the large diode and the pixel, one can estimate the leakage current of the pixel to be a few pA:

$$I_2 = \frac{S_2}{S_1} I_1 \approx 3\ pA$$

where I_1 and S_1 are, respectively, the leakage current and the depleted surface of a big size pixel while I_2 and S_2 are the leakage current and the depleted surface of a small size pixel.

4.3.2 Capacitance Measurements

The goal of the $C-V$ measurements is to establish the capacitance value of the sensor; moreover, once the capacitance value of the detector is known, it is possible to estimate the depth of the depletion region and the effective doping level of the sensor. During the $C-V$ measurements, voltage bias

values similar to the ones used in the $I-V$ measurements have been used; in particular, the inner and the outer guard have been fixed at $V_{guard} = -30\ V$, the n-well has been fixed at $V_{n-well} = 0\ V$ and a negative sweep on the substrate has been done. The measurements have been performed at moderate reverse biases ($|V_{sub}| < 60\ V$) only, avoiding too large currents and also parasitic current injection from the edge. The capacitance-voltage characteristic has been measured at room temperature, if not mentioned otherwise, and with a capacitance bridge in parallel mode with an AC signal of $\Delta V = 0.5\ V$. In Fig. 4.11, the $C-V$ measurement results at different frequency values are shown. Due to the substrate voltage limit imposed by the parasitic current, the minimum capacitance value obtained ($C \approx 1\ pF$) is higher than would have been obtained otherwise. If full depletion would have been reached, this would have yielded a capacitance of about 270 fF. As

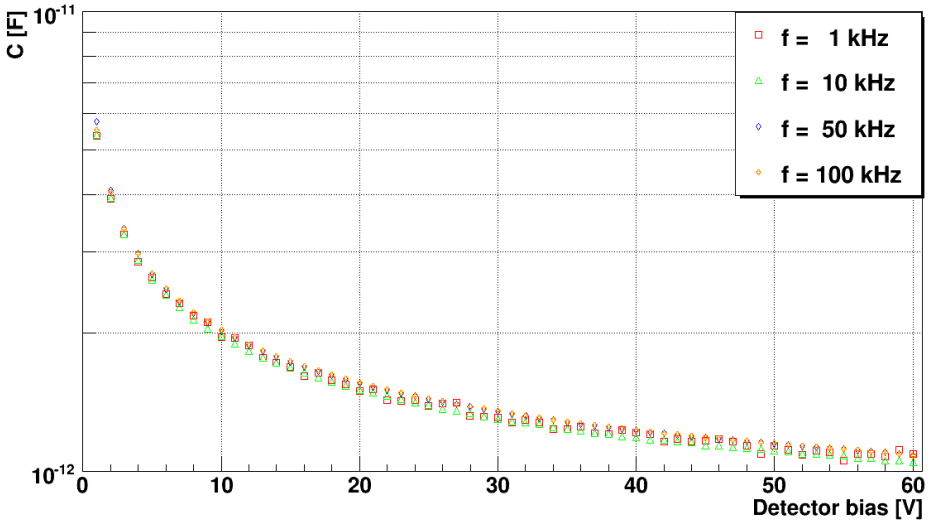

Figure 4.11: C-V curves for different frequency values.

already mentioned in the first chapter (see Fig. 1.4), the $1/C^2$ representation is often used, to better estimate the capacitance for small substrate values: this representation is shown in Fig. 4.12. The relationship between the inverse square capacitance and the substrate voltage in a ideal abrupt and planar approximation is given by:

$$\frac{1}{C^2} = \frac{2}{qN_{eff}\epsilon S^2}(V_{appl} + V_{bi}) \tag{4.1}$$

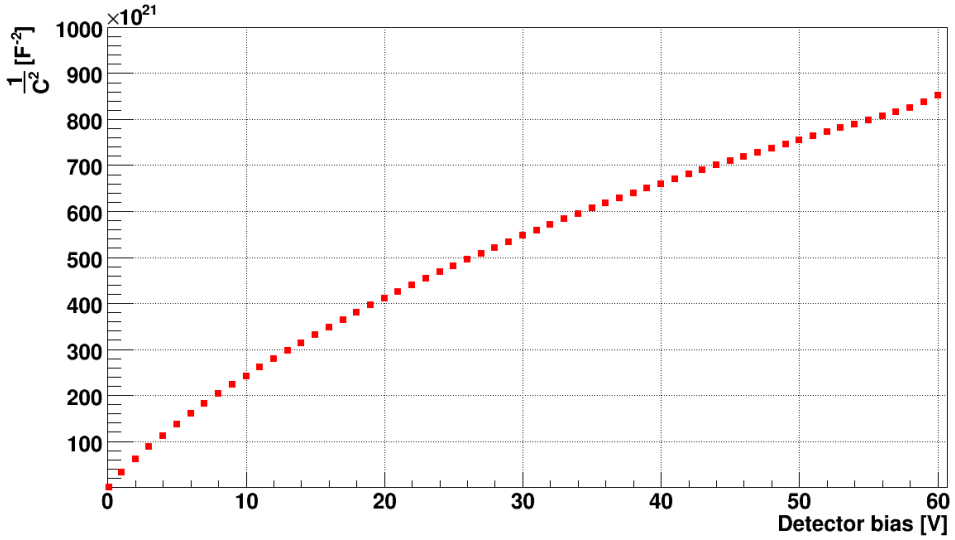

Figure 4.12: C-V curves based on the $1/C^2$ representation at $f = 100\ kHz$.

where the variables name is the same of the equation 1.2. However, Fig. 4.12 shows the inverse square capacitance is not linearly dependent on the substrate bias. In fact, the geometry of the device, which includes also the conductive path under the guard ring, does not allow to treat it as an ideal planar and abrupt junction. Consequently, it is difficult to evaluate the real depletion region depth and the effective doping level of the device due to the lack of an adequate model for the sensor itself. However, it is possible to compare the performance of the sensor with an ideal sensor (with a planar and abrupt junction) having the same size. In Fig. 4.13, the depletion depth is shown as a function of the substrate bias, obtained by following the equation:

$$d = \epsilon \frac{S}{C}$$

where S is the electrode surface of the LePix diode and C is the capacitance value obtained by the diode structure capacitance measurements. Fig. 4.14 shows a doping profile of a sensor estimated from the derivative of the curve of Fig. 4.13 as follows: the derivative (see 4.1)

$$\frac{d(1/C^2)}{dV} = \frac{2}{qN_{eff}\epsilon S^2}$$

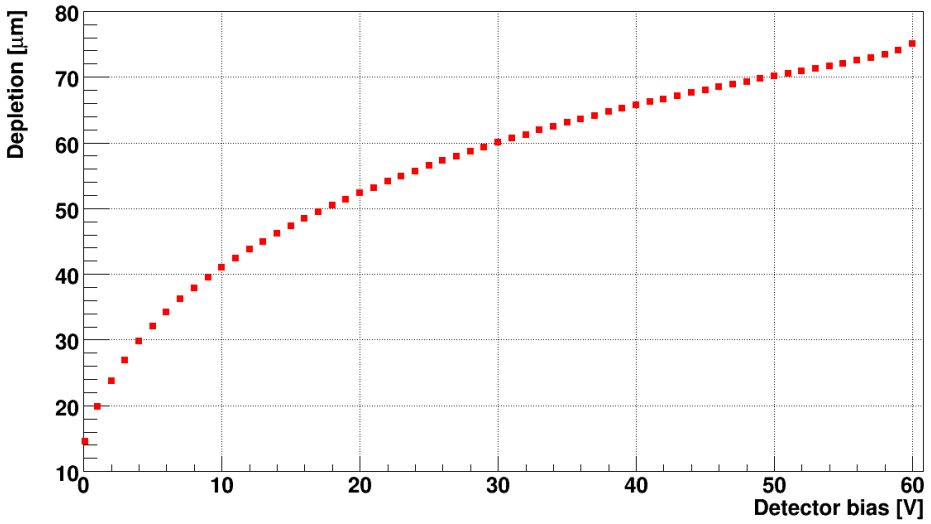

Figure 4.13: Depletion depth vs Substrate value for a ideal sensor having the same capacitance of the LePix diode structure.

is directly related to the doping level

$$N_{eff} = \frac{2}{q\epsilon S^2} \cdot \left(\frac{d(\frac{1}{C^2})}{dV_{appl}} \right)^{-1}$$

and this would allow to express N_{eff} as a function of the substrate bias, but it makes more sense to do this in terms of depletion depth:

$$N_{eff} = \frac{2\epsilon}{q} \cdot \frac{dV_{appl}}{d(d^2)}$$

and by using the numerical increment on both the substrate voltage and the depletion depth, obtaining:

$$N_{eff} = \frac{2\epsilon}{q} \cdot \frac{\Delta V_{appl}}{\Delta(d^2)}$$

The effective doping profile shows a doping level between $N_{eff} = 8{\cdot}10^{12}\ cm^{-3}$ and $N_{eff} = 2 \cdot 10^{13}\ cm^{-3}$ which corresponds to a resistivity level between $\rho = 400\ \Omega cm$ and $\rho = 500\ \Omega cm$. Fig. 4.15 shows a comparison of the measured capacitance and the capacitance of an ideal parallel plate capacitor of the same area with a substrate doping level of $N_{eff} = 10^{13}\ cm^{-3}$.

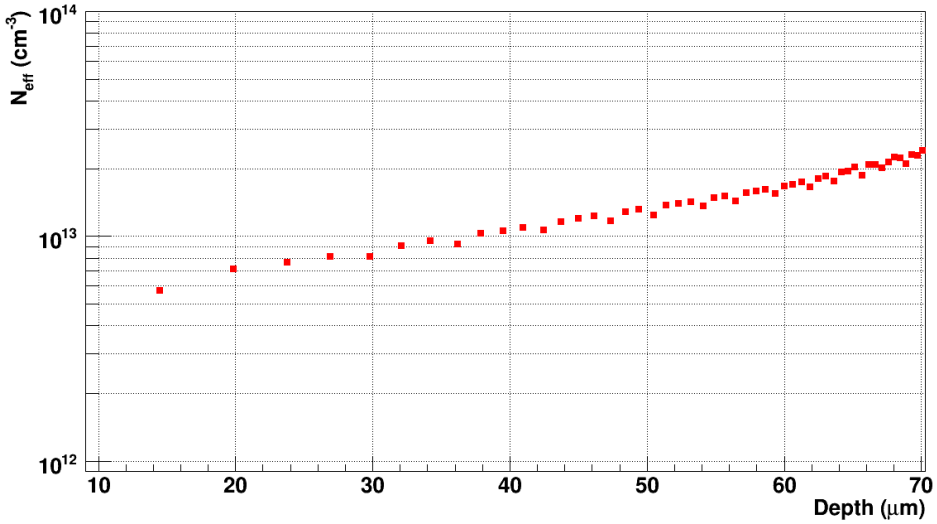

Figure 4.14: Doping level as function of the depletion depth for a detector having the same capacitance of the LePix diode structure.

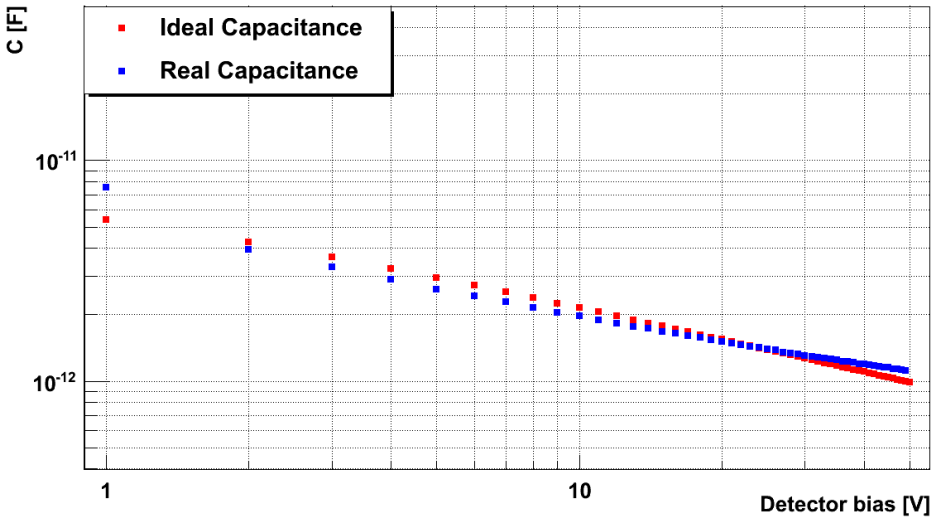

Figure 4.15: Comparison between the real capacitance measured on the diode structure and an ideal capacitance of a detector having a doping level of $N_{eff} = 10^{13}\ cm^{-3}$.

4.4 Conclusions

The diode performs well down to reverse substrate biases of $V_{sub} \approx -40\ V$. Beyond this point, parasitic current starts to be injected from the device pe-

riphery. This current is believed to be due to a parasitic current path caused by states at the silicon-silicon oxide interface, which could not be controlled in absence of a gate electrode on top of this area. These interface states are also expected to be present in other test structures, but in the matrices a metal gate electrode over these areas has been implemented allowing this region to be better controlled. Despite this parasitic effect it was possible to make a reasonable estimate of the substrate resistivity from the $C-V$ measurements ($400-500\ \Omega cm$) and also of the expected leakage current (a few pA) for a single pixel.

Chapter 5

Breakdown Structure

In this chapter the breakdown structure will be described. The layout of the structure will be described first, followed by the experimental setup and finally the measurement results.

5.1 Breakdown Structure Strategy

The breakdown structure contains small matrices of pixels without readout circuitry allowing detailed device measurements. The pixels are organized in a central group (inner pixels) surrounded by a set of pixels (outer pixels) which are contacted separately. Any perimeter effect is supposed to be absorbed by the outer pixel, so that one can assume "ideal" conditions for the central pixels. By examining in more detail the current flow between inner and outer pixels as a function of field plate bias and various other measurements, it was possible to better understand the role and condition of the non-standard low doped active areas and their interaction with the field plate and the substrate bias.
In Fig. 5.1 a simplified view of the breakdown structure is shown: both the inner n-well and the outer n-well are based on small electrodes shorted together (six electrodes for the inner well and fourteen for the outer well). There is a contact to bias the inner well and a contact to bias the outer well. Different pixel sizes have been implemented, to check the influence of the electrode geometry: in particular, groups of the previously described structure (an inner n-well surrounded by an outer n-well) having electrode sizes of 3 $\mu m \times 3$ μm, 4 $\mu m \times 4$ μm and 5 $\mu m \times 5$ μm have been tested. A metal

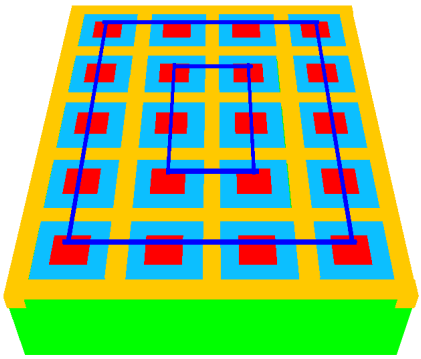

Figure 5.1: Schematic and simplified view of the breakdown structure with the electrodes (red), the oxide (light blue), the shallow trench isolation (orange) and the shorts used to contact the inner wells and the outer wells (dark blue).

layer and a polysilicon layer are placed respectively over the oxide region (light blue in Fig. 5.1) and over the shallow trench isolation (orange) and they can be biased independently. Moreover, samples have been fabricated with different implant doses in the low doped active area in an effort to find an optimum dose. However, as already mentioned, traps and fixed oxide charge had a significant impact on the threshold for inversion in these areas and it has been verified that these were not very well controlled and yielded a threshold variation for the same implant more or less similar to the one induced by the doping variation of the different splits on implant dose.
The goal of the measurements has been to check for possible parasitic currents flowing between the n-wells and the possibility to stop them by biasing the metal layer and the polysilicon layer. Since pixel collection electrodes are formed by N-wells and polysilicon and metal cover fractions of the oxide over silicon, one can look at these structures as special MOS transistors where the polysilicon and the metal are gates of transistors in series. This yields the simplified equivalent schematic shown in Fig. 5.2. The p-n junctions between the substrate and the electrodes are represented as diodes connected by two NMOS transistors in series having the metal and the polysilicon as gates; the electrodes are also the n-wells of the NMOS transistors (Fig. 5.3). In this context it is therefore clear that the threshold voltages of these transistors have a significant influence of the behavior of these structure. The

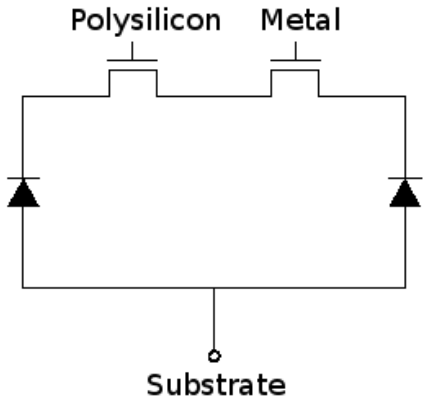

Figure 5.2: Schematic and simplified view of the equivalent circuit of the breakdown structure.

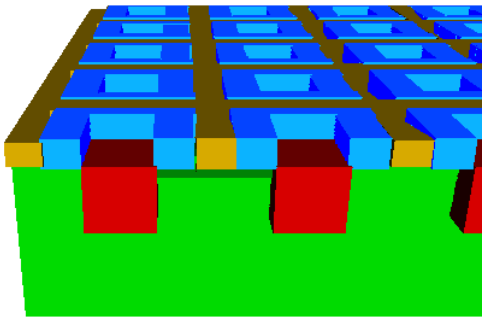

Figure 5.3: Schematic and simplified 3D view of the breakdown structure parasitic NMOS: a conductive channel (dark green) between the inner and the outer n-well (red) can be controlled by biasing the polysilicon over the shallow trench isolation (gold) and the metal over the oxide (blue) layer which act as gates of a NMOS transistor.

inversion layer around the N-wells has a strong influence not only on the current flowing between electrodes but also in terms of capacitance. In fact, it increases the collecting electrode area (given by the area of the n-well plus the area of the inversion layer) and, consequently, does not allow to reach a small capacitance regime.

To study the influence of the inversion layer around the n-well, the breakdown structure has been designed with two different contacts for the polysilicon layer and the metal layer: it allows to act on the electric fields on the

silicon oxide interface underneath the metal layer and under the shallow trench isolation biased by the polysilicon contact.

5.2 Experimental Set-Up

The tests performed on the breakdown structure are mainly I_{ds} *vs* V_{gs} curves to measure the NMOS transistor threshold. The samples (Fig. 5.6) are biased by needles placed on an electrostatic protected board allowing to bias up to sixteen pads contemporaneously (Fig. 5.4). The samples have been

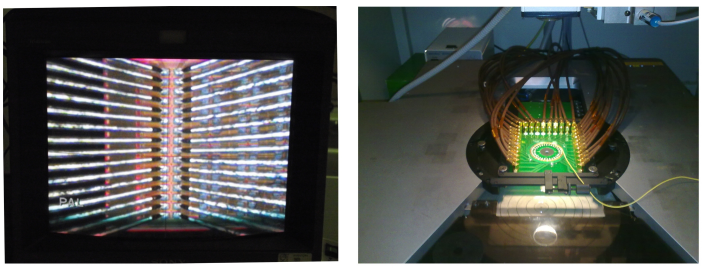

Figure 5.4: Monitor used to place the needles biasing the pads of the breakdown structure (left) and board used to bias the samples (right).

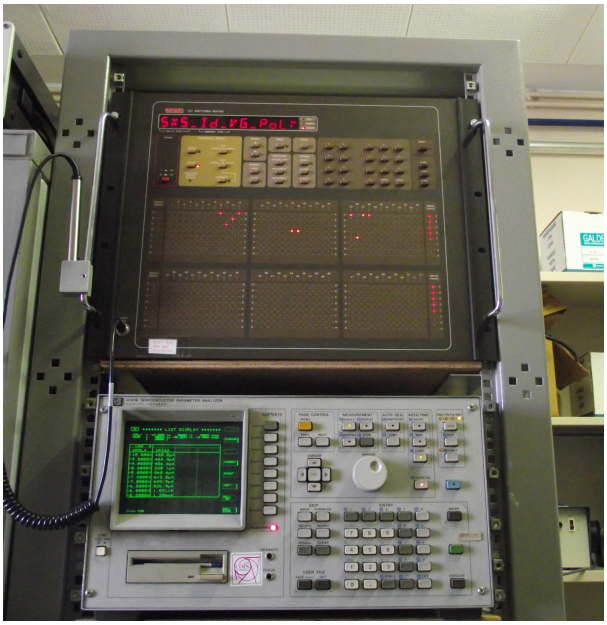

Figure 5.5: Switching matrix and semiconductor parameter analyzer used to characterize the breakdown structure.

biased by a semiconductor parameter analyzer ($HP-4145$) passing through a switching matrix ($Keithley-707$, see Fig. 5.5). Both the switching matrix and the semiconductor parameter analyzer have been controlled by a LabView interface.

Figure 5.6: Breakdown structure samples.

5.3 Measurement Results

The goal of the measurements on the breakdown structure is to characterize the parasitic transistor threshold to evaluate the polysilicon and metal bias which can stop any parasitic currents between the n-wells. As already mentioned, the parasitic transistors are in series; to characterize the threshold of one transistor, the other one has been used in a conductive regime: in this way, it has been possible to characterize one transistor with no current limitation due to the transistor in series.
A typical threshold voltage measurement is based on the so called *linear extrapolation method* where the drain-source current is measured as function of the gate voltage at low drain-source voltage (usually $50mV$ or $100mV$) to ensure operation in linear MOSFET region. It has been observed a negative threshold and, consequently, the sweep has been adjusted to be able to characterize it. In Tab.5.1 the biases used to characterize the sensor having the metal or the polysilicon layer as gate are shown: several trials have been done before obtaining this configuration. The outer pixels have been biased at a higher voltage compared to the inner pixels, which means that the inner pixels are equivalent to the source of this somewhat complicated

NMOS transistor. In fact, the outer pixels could be compared to the N-well surrounding the pixels in the matrix (and there its bias is 1.2 V) while the pixels are biased around $600mV$. The substrate has been biased down to $V_{sub} = -30\ V$. It has to be remarked that the goal of the measurements has been to check the current flowing between the n-wells of the structure and not to check parasitic currents between the outer n-well and the substrate (as done in the diode structure where a substrate voltage bias lower that $V_{sub} = -30\ V$ has been used).

	Gate Polysilicon	Gate Metal
Metal	-6 V to 0 V	0 V
Polysilicon	0 V	-50 V to 0 V
Inner N-well	0 V	0 V
Outer N-well	50 mV	50 mV
Substrate	-30 V to 0 V	-30 V to 0 V

Table 5.1: Biases used to characterize the parasitic NMOS transistors.

5.3.1 Polysilicon Gate

In Fig. 5.7 the $I_{ds}\ vs\ V_{gs}$ curve of a polysilicon-gate transistor having a $3 \times 3\ \mu m^2$ area electrodes with no implant underneath the oxide is shown; different substrate voltage biases have been used. The measured curves show significant current flow at zero gate bias and illustrate that the NMOS threshold is negative. This negative threshold is due to fixed charge but there is also an indication of interface traps as the weak inversion slope is affected (see Fig. 5.8). Positive oxide charge attracts electrons and hence facilitates inversion of the p-type substrate. The presence of fixed oxide charge shifts the $I_{ds}\ vs\ V_{gs}$ curve along the X axis. The effects of interface states are more complicated to predict: as the gate voltage changes, more interface states get charged or discharged. This results not only in a horizontal shift of the curve anymore, but also in a distortion with a smaller slope of the weak inversion region. The threshold of the NMOS transistor tested is strongly dependent on the substrate voltage. In fact, the threshold of a MOS transistor is defined as follows:

$$V_{th} = V_{th0} + \gamma(\sqrt{|2\Phi_F + V_{sb}|} - \sqrt{|2\Phi_F|}) \tag{5.1}$$

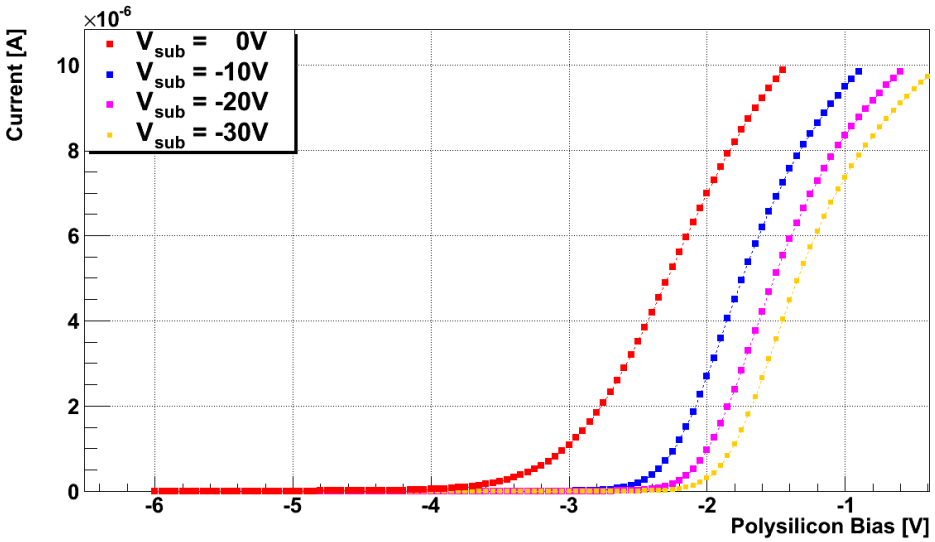

Figure 5.7: Drain-Source current *vs* Polysilicon-Gate voltage in the parasitic transistor having 3×3 μm^2 area electrodes for different substrate biases.

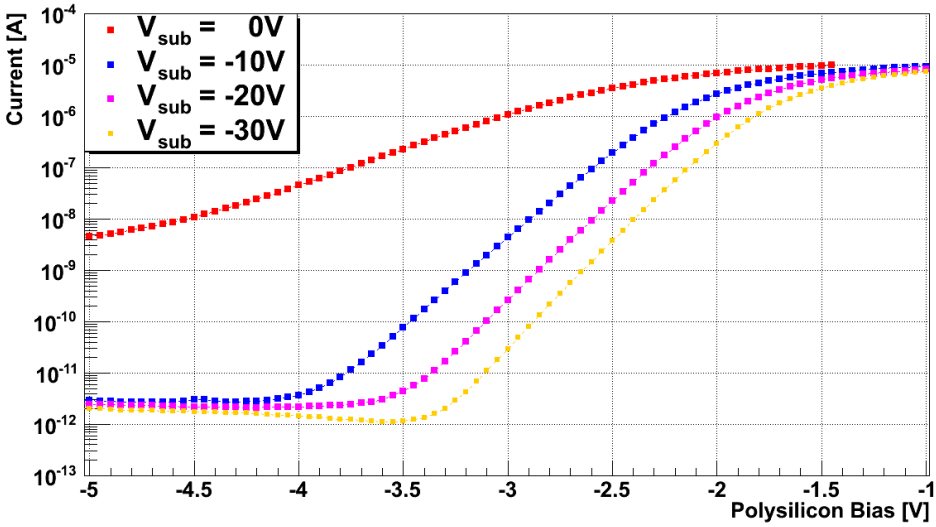

Figure 5.8: Drain-Source current in logarithmic scale *vs* Polysilicon-Gate voltage in the parasitic transistor having 3×3 μm^2 area electrodes for different substrate biases.

where V_{th0} is the threshold value when there is no voltage difference between the bulk and the source, $\gamma = \sqrt{2q\epsilon_{si}N_{eff}}/C_{ox}$ and $2\Phi_F$ is the surface potential; when the ΔV between the source and the bulk increases, the drain-source current (which is proportional to the difference between the gate-source voltage and the threshold voltage) decreases. In Fig. 5.9, the typical drain-source current as function of the substrate voltage for a NMOS transistor switched on is shown . The same sweep (based on the circuital

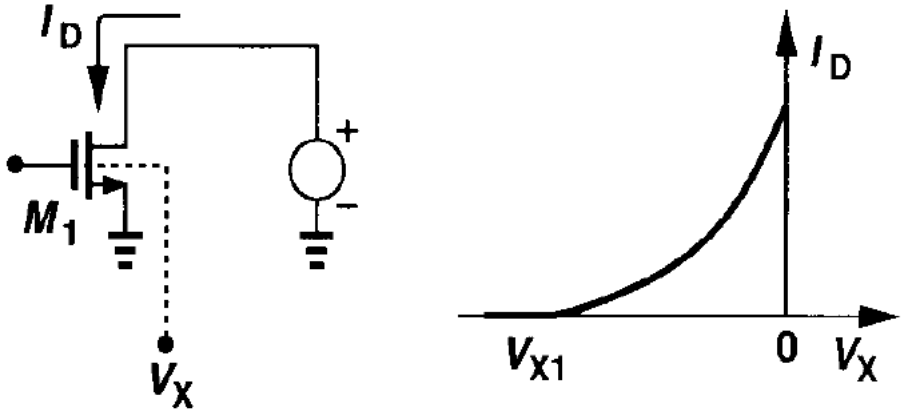

Figure 5.9: Drain-Source current flowing in a NMOS transistor as a function of the bulk bias.

configuration shown in Fig. 5.9) having $V_{ds} = 50\ mV$ has been done on the breakdown structure obtaining the plot shown in Fig. 5.10: different polysilicon-gate biases have been used to evaluate the effect of the substrate above ($V_{polysilicon} = -2\ V$), around ($V_{polysilicon} = -2.5\ V$) and below ($V_{polysilicon} = -3\ V$) the threshold.
The NMOS threshold should be independent on the size of the collection electrode. This is confirmed by the measurement result shown in Fig. 5.11. As already mentioned, samples having a different doping implant in the active area underneath the field oxide have been produced; the same threshold value measurements have been repeated for each implant value by testing five samples per implant value (see Fig. 5.12). Comparing different implant doses for the implant in the low doped active area gives the results shown in tables 5.2, 5.3, 5.4 and in Fig. 5.13, and illustrates that there is no correlation between implant dose and threshold (the threshold spread for

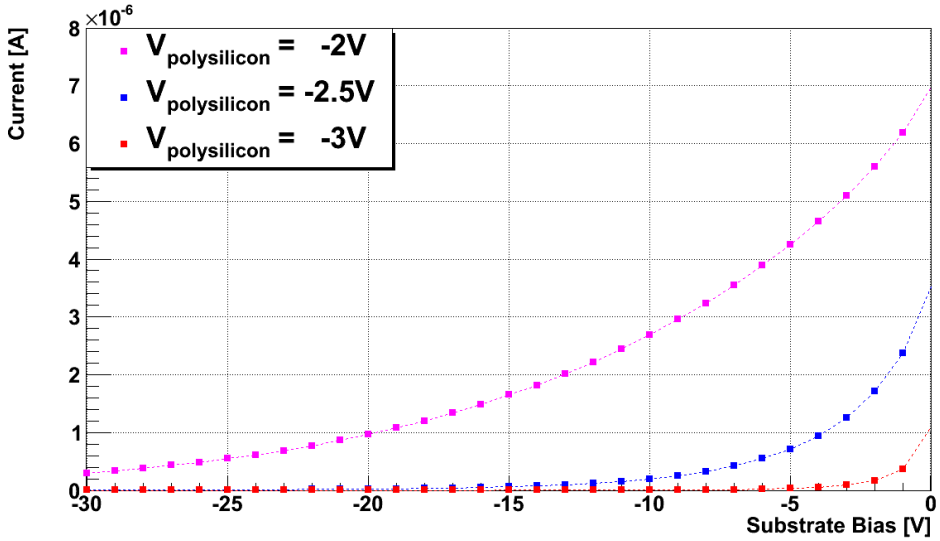

Figure 5.10: Drain-Source current flowing in a NMOS transistor of the breakdown structure as function of the substrate biases at different polysilicon biases.

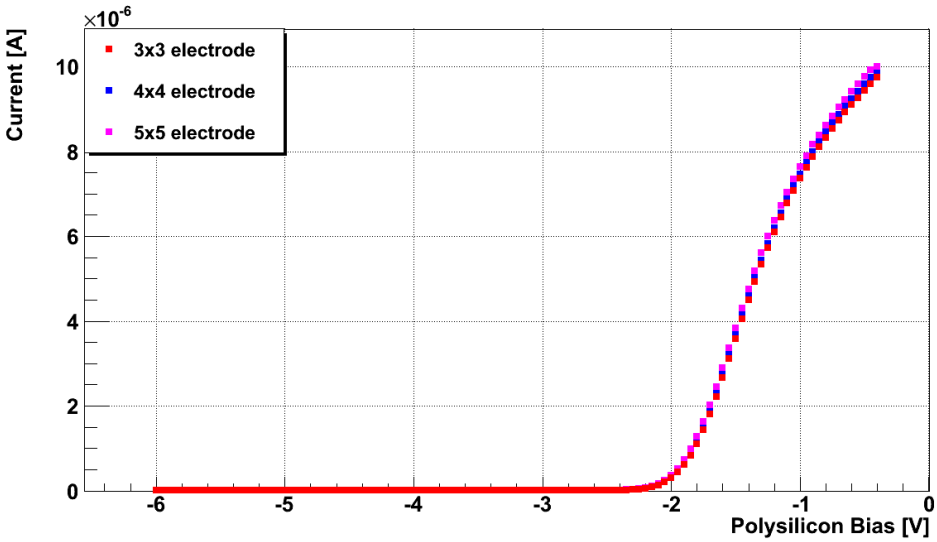

Figure 5.11: Comparison between the threshold voltage values of transistors having different n-well sizes.

Dopant	Doping Type	Dose $[cm^{-2}]$	$V_{th}[V]$	$\Delta V_{th}[V]$
Boron	p-type	$5 \cdot 10^{10}$	-2.0	0.3
Boron	p-type	$2 \cdot 10^{10}$	-2.1	0.2
No-Implant	–	0	-2.0	0.1
Phosphorus	n-type	$4 \cdot 10^{10}$	-2.2	0.1
Phosphorus	n-type	$8 \cdot 10^{10}$	-2.0	0.2
Phosphorus	n-type	$1.2 \cdot 10^{11}$	-2.3	0.3
Phosphorus	n-type	$1.6 \cdot 10^{11}$	-2.2	0.1
Phosphorus	n-type	$2.4 \cdot 10^{11}$	-2.2	0.2

Table 5.2: Transistor thresholds for a 3×3 μm^2 n-well transistors with different implant doses.

Dopant	Doping Type	Dose $[cm^{-2}]$	$V_{th}[V]$	$\Delta V_{th}[V]$
Boron	p-type	$5 \cdot 10^{10}$	-2.0	0.3
Boron	p-type	$2 \cdot 10^{10}$	-2.1	0.2
No-Implant	–	0	-2.0	0.1
Phosphorus	n-type	$4 \cdot 10^{10}$	-2.2	0.1
Phosphorus	n-type	$8 \cdot 10^{10}$	-2.0	0.3
Phosphorus	n-type	$1.2 \cdot 10^{11}$	-2.3	0.3
Phosphorus	n-type	$1.6 \cdot 10^{11}$	-2.2	0.2
Phosphorus	n-type	$2.4 \cdot 10^{11}$	-2.2	0.3

Table 5.3: Transistor thresholds for a 4×4 μm^2 n-well transistor with different implant doses.

Dopant	Doping Type	Dose $[cm^{-2}]$	$V_{th}[V]$	$\Delta V_{th}[V]$
Boron	p-type	$5 \cdot 10^{10}$	-2.0	0.3
Boron	p-type	$2 \cdot 10^{10}$	-2.1	0.2
No-Implant	–	0	-2.0	0.2
Phosphorus	n-type	$4 \cdot 10^{10}$	-2.2	0.1
Phosphorus	n-type	$8 \cdot 10^{10}$	-2.0	0.3
Phosphorus	n-type	$1.2 \cdot 10^{11}$	-2.4	0.3
Phosphorus	n-type	$1.6 \cdot 10^{11}$	-2.2	0.2
Phosphorus	n-type	$2.4 \cdot 10^{11}$	-2.2	0.3

Table 5.4: Transistor thresholds for a 5×5 μm^2 n-well transistor with different implant doses.

one split is comparable to the threshold spread between different splits).

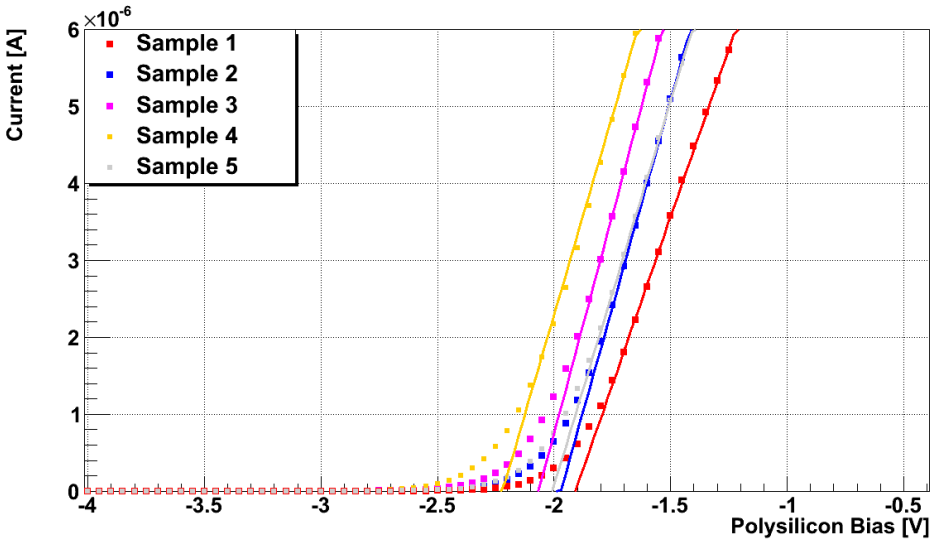

Figure 5.12: I_{ds} *vs* V_{gs} (with linear fit used to determine the threshold voltage) for five 3×3 μm^2, no implant samples.

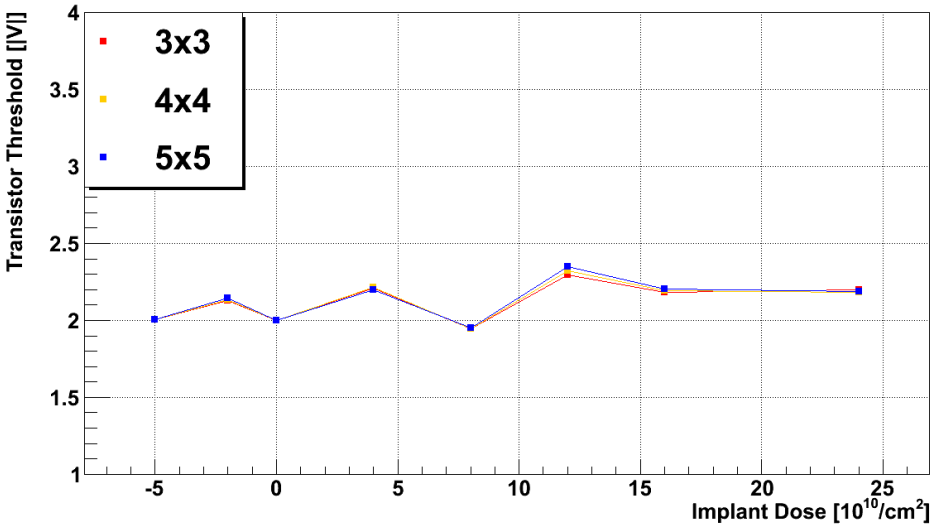

Figure 5.13: Absolute value of the threshold for different implants (the p-type implants are written with a negative dose value).

5.3.2 Metal Gate

The same measurements have been repeated using the metal contact as transistor gate and by using the same procedure: negative sweeps have been

done on the metal by changing the substrate values and having a $V_{ds} = 50\ mV$; as already mentioned, the polysilicon contact has been biased to have the polysilicon-gate NMOS on ($V_{polysilicon} = 0\ V$). The measurements result for a NMOS transistor having a $3{\times}3\ \mu m^2$ electrodes with no implant in the active area for different substrate values is shown in Fig. 5.14. As already

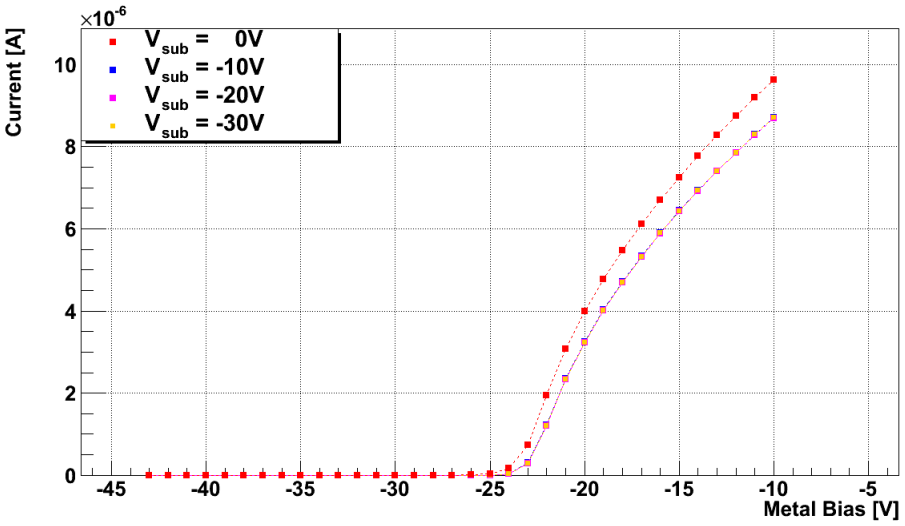

Figure 5.14: Drain-source current vs gate-source voltage for a $3 \times 3\ \mu m^2$ electrodes sizes NMOS transistor with no-implant.

mentioned for the transistor having the polysilicon as gate, the threshold of the NMOS transistor having the metal as gate is negative and it is dependent on the substrate voltage. However, the threshold value is lower (higher, in absolute value) than the polysilicon-gate case of several volts. The large difference in threshold voltage is related to the quality of the silicon-oxide surface: in the silicon-oxide interface case, it is worse than the shallow trench isolation interface. Moreover, it has to be taken into account the thickness of the oxide which is higher in the oxide placed underneath the metal: since the thickness is higher, also the number of charges in the oxide is larger. Due to those factors, a lower metal voltage then the polysilicon voltage is required to have no inversion layer in the silicon-oxide interface (see Fig. 5.15). Since the quality of the silicon-oxide interface is not constant from sample to sample, a large variation of the threshold voltage from chip to chip having the same implant is expected. In fact, in Fig. 5.16 it is possible to see the

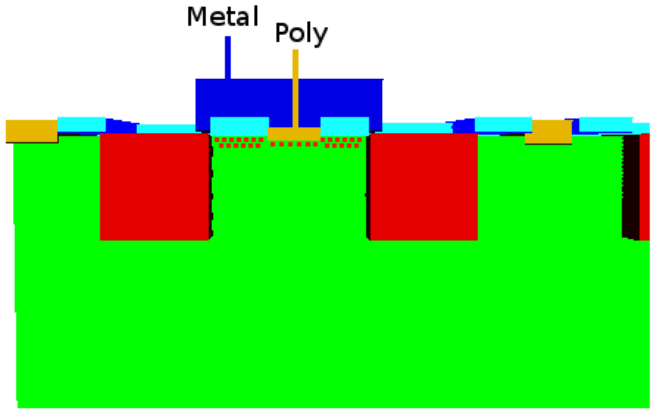

Figure 5.15: Simplified 3D view of the metal and polysilicon layer with inversion layer (red spots) on the oxide-silicon interface.

large spread of the threshold voltage in different samples with no implants. It can be observed that the variation between different chips for the same

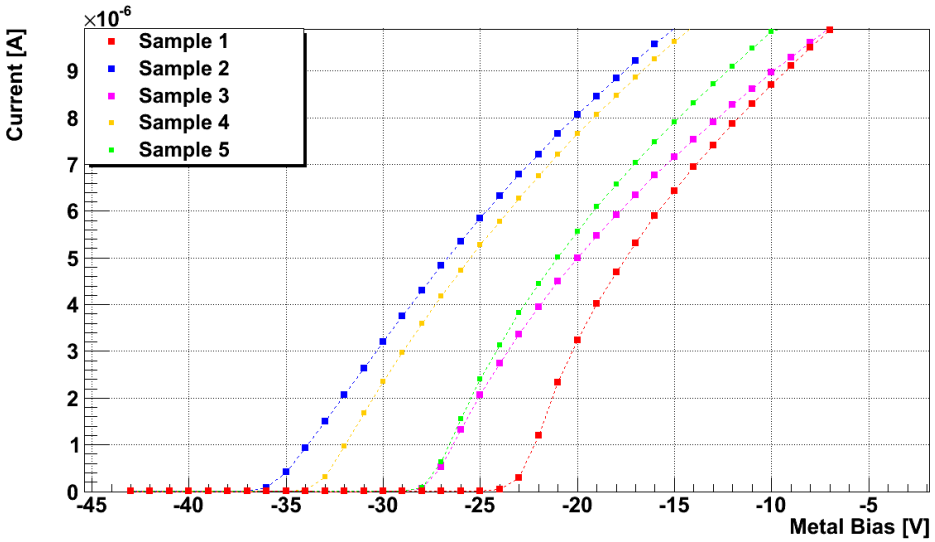

Figure 5.16: Drain-source current vs gate-source voltage with a substrate bias of $V_{sub} = -30\ V$ for five $3 \times 3\ \mu m^2$ electrodes sizes NMOS transistors with no-implant in the active area.

implant dose is comparable to the split-to-split variation, as shown in Fig.

5.17 (the same results have been observed also in the structures having electrode sizes of 4×4 μm^2 and 5×5 μm^2). From this it can be concluded that the large variations of the parasitic transistor threhsold values, due to a missing uniformity in interface states density and oxide charge, does not allow to well control the area surrounding the n-well making ineffective the low dose implant made in that area.

Only once the parasitic paths around the inner pixel have been interrupted,

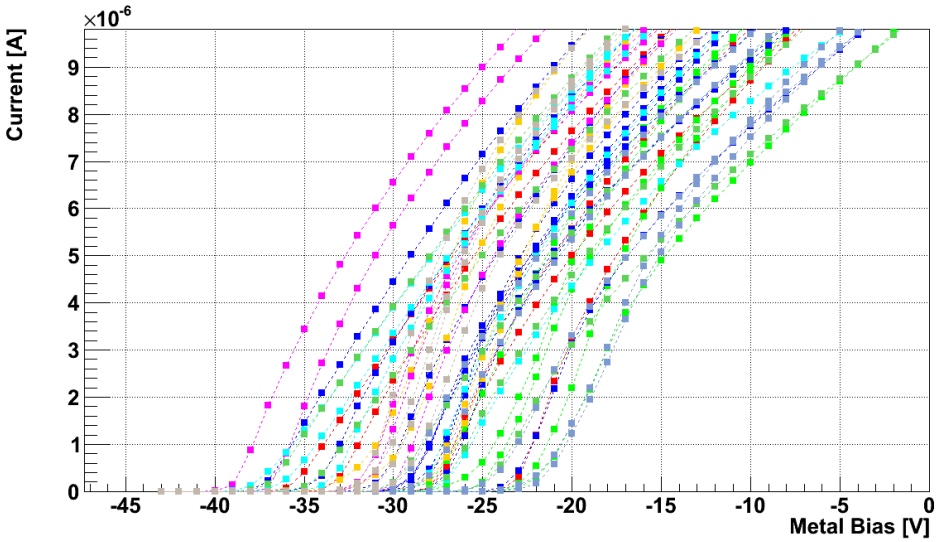

Figure 5.17: View of the drain-source current vs gate-source voltage curves ($V_{sub} = -30$ V) for five 3×3 μm^2 electrodes sizes transistors for each implant: samples having the same implant are shown with the same color.

it is possible to evaluate the breakdown voltage of the n-wells. Fig. 5.18 shows the typical $I-V$ curves for the inner and outer n-wells of a breakdown structure having 3×3 μm^2 electrode area and no-implant in the active area. As already happened in the diode structure, it is possible to see current flowing in the outer n-well without a real breakdown: that current is due to the parasitic path which connects the outer well with the sensor edge. Moreover, that current has no influence on the inner pixel because of the isolation offered by the polysilicon and metal layers.

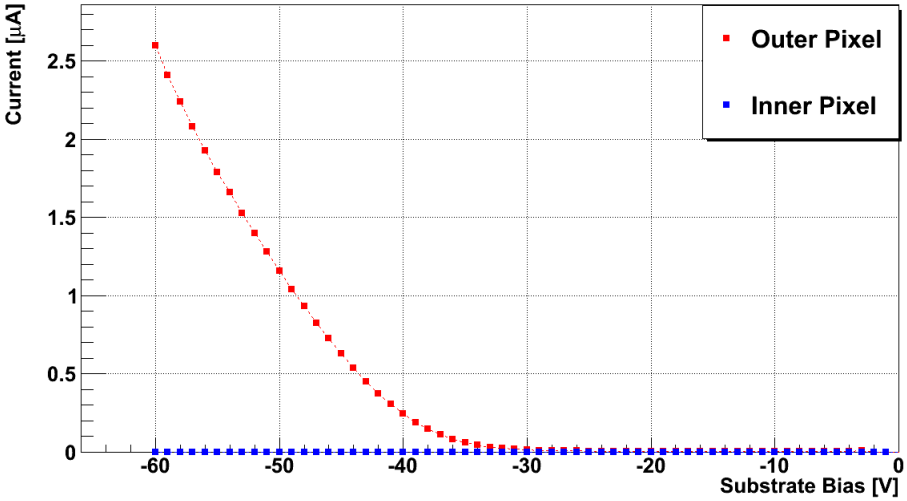

Figure 5.18: Inner and outer pixel currents vs substrate bias for a pixel with a $3 \times 3 \mu m^2$ area with no-implant in the active area.

5.4 Conclusions

Also in the breakdown structure inversion at the silicon-silicon oxide interface causes current flow between N-wells, unless (significantly) negative voltage is applied to the electrodes above this interface to switch these NMOS currents off. The inversion threshold underneath the polysilicon over shallow trench isolation is only a few volts negative, for the metal in much lower ($\approx -20\ V$) but measurements have demonstrated that this inversion threshold for the metal over low doped active area is very poorly controlled. Only once the inversion layer around the n-well is completely removed it is possible to have a small area collecting electrode and, consequently, to reach a small capacitance regime.

Chapter 6

Analog Front-end Matrix

In this chapter, the matrix structure will be described. In particular, the first part of the chapter will focus on the matrix strategy used during the design phase, the second part on the front-end electronics and the last part will describe the equipment used to test the matrix.

6.1 Matrix Strategy

The matrix structure is a prototype of a sensor matrix equipped with simple readout electronics to test the performance of the pixel. The main goals of the prototype are to reach a small capacitance regime, to collect the charge by drift, to have a uniform depletion layer and to be radiation tolerant. The matrix contains pixels with different collection electrode sizes and also different input transistors. Moreover, different approaches have been used in the read-out electronics: an analog and a digital read-out. The former will be treated in the following chapters while the latter will be discussed in the last part of the thesis.
The pixel layout has been already discussed in detail in the third chapter: a small size electrode has been used to work in a small capacitance regime and a pixel pitch of 50 μm has been used to obtain an uniform depletion layer at $V_{sub} \approx -100\ V$. However, the small electrode size reduces the possible options for the in-pixel electronics front-end: only a few transistors can be placed in the pixel cell while the remaining part of the front-end electronics has to be designed outside the pixel. Each pixel cell is connected to its own read-out cell through a metal line. In this way it is possible to develop a

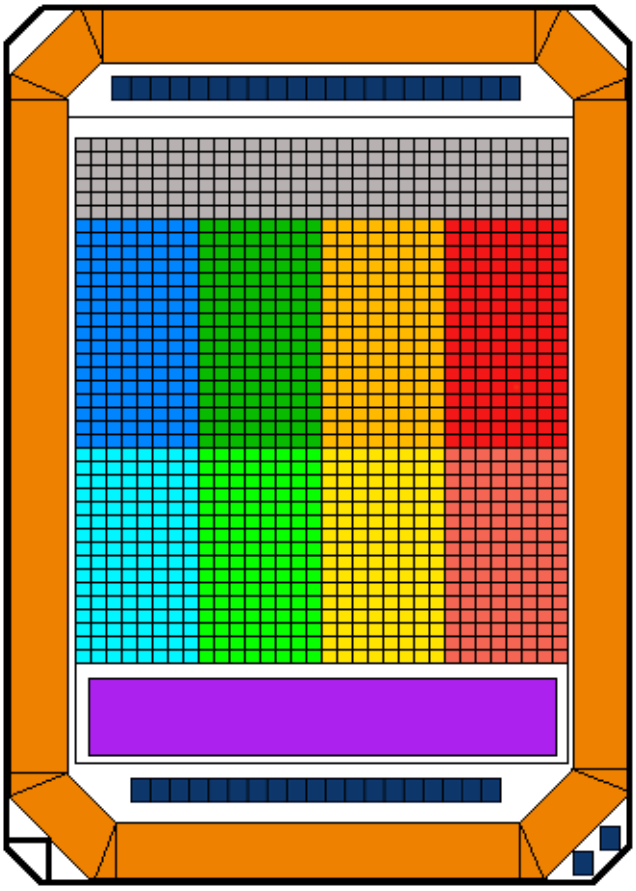

Figure 6.1: Schematic simplified view of the matrix layout.

parallel read-out of each pixel instead of a serial read-out commonly used in standard MAPS: the high line density required to connect each pixel to its own electronics is not a show-stopper in a very deep submicron technology such as 90 *nm* CMOS technology. This approach forces the matrix to be divided in two parts: a central part made of sensitive electrodes, which should be uniformly depleted and should collect the charges generated by an impinging particle, and a periphery where the read-out electronics is placed. In Fig. 6.1 a simplified view of the matrix is shown. It is based on a 32×32 pixel array divided in four sectors (blue, green, yellow and red) of 8 columns each having a slightly different front-end input transistor and a slightly different collection electrode. Moreover, the first sixteen rows (dark blue, dark green, dark yellow and dark red) and the second sixteen rows (clear blue, clear green, clear yellow and clear red) have a different pixel

reset mechanism. A group of pixels is placed on the top of the sensitive part (gray): those pixels have a simple read-out electronics based on a source follower connected to the sensor which allows to probe directly the sensor by an oscilloscope accessible output. The read-out electronics (violet) is placed in the bottom part of a n-well surrounding the central part. Both the central sensitive part and the n-well are surrounded by a guard-ring based on the same layout of the diode guard-ring: it can be biased from the outer side, by using its own contact, and from the inner side, by using the polysilicon layer contact. Forty pads are used to provide the main biases and the main currents to the matrix and to read the output. Twenty pads are placed in the top part of the matrix and the remaining pads in the bottom part (dark blue); two contacts are placed outside the guard-ring to bias the substrate and the outer contact of the guard-ring. The sensitive area of the sensor is estimated to be $A \approx 2.5\ mm^2$ (given by 1024 pixel having a 50 μm pitch).

6.2 Pixel Cell

The pixel cell is based on the n-well electrode containing the reset mechanism and the first stage of the front-end electronics; since that stage has to be placed in a n-well, only PMOS transistors are used. Also a solution with a triple-well structure hosting a NMOS transistor has been implemented. The approach is similar to the 3T approach used in standard MAPS front-end electronics: there is a reset mechanism which allows to bias the diode and an input transistor of a source follower stage DC coupled with the sensor (Fig. 6.2 and Fig. 6.3). The reset bias (V_{reset}) is in common to all pixels. The reset mechanism can be based on a PMOS transistor, also called *active reset* and working on the first sixteen rows of the matrix, or a diode, also called *continuous reset* and working on the second sixteen rows. The reset mechanism is used to bias the sensor. In the *active reset* approach, the PMOS transistor is used as switch: when the switch is on, the sensor is biased to a voltage value $V_{sensor} = V_{reset}$; when the switch is off, the high impedance of the reset transistor allows to have no charge due to the impinging particles flowing to V_{reset}, which is the highest potential in the pixel cell, before the source follower can react. Moreover, when the reset transistor is off, the input transistor gate (X in Fig. 6.2) has a voltage shift. In

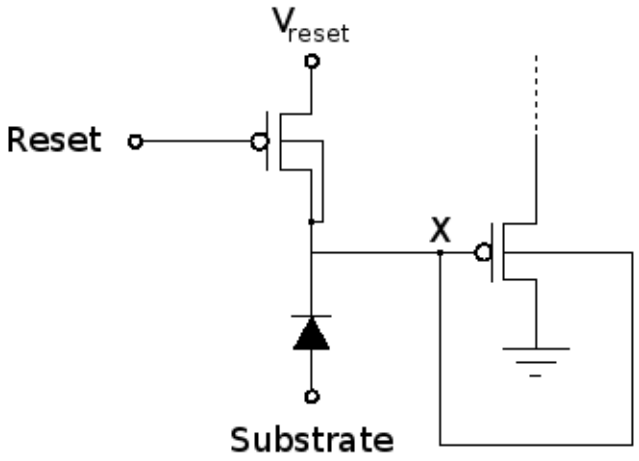

Figure 6.2: Schematic view of the pixel cell circuit (having an active reset mechanism) used to read the pixel signal.

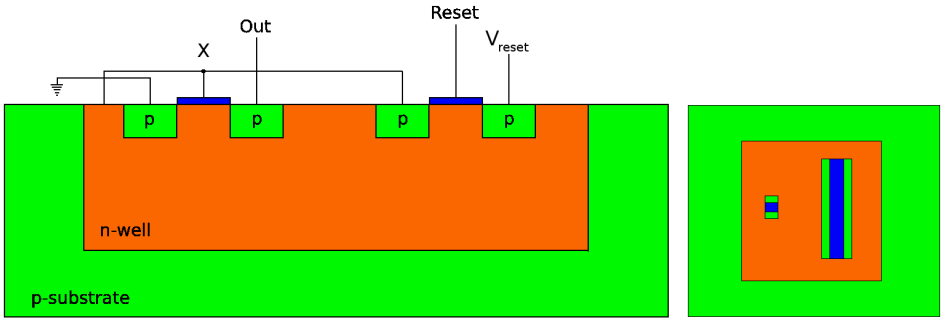

Figure 6.3: Schematic views of the pixel cell with an active reset.

fact, the collecting diode is reversely biased and, consequently, the leakage causes a voltage drop at the input node. The *continuous reset* mechanism is slightly different: a reset diode is placed instead of the reset transistor (Fig. 6.4 and Fig. 6.5). The reset diode provides the current required by the collecting diode (the leakage current); consequently, the low current flowing in the reset diode allows to have it slightly conductive bringing the X point voltage value at a fixed voltage lower than V_{reset}.
The voltage drop due to an impinging particle is also different in the two reset configurations. In fact, when a sensor having an active reset is hit and electron-hole pairs are created, the electrons flow to the n-well causing a negative voltage step on the gate of the input transistor; when the signal

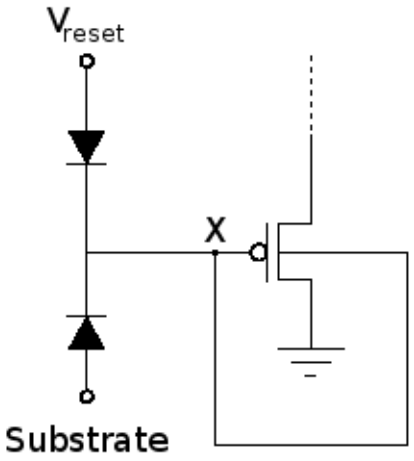

Figure 6.4: Schematic view of the pixel cell circuit (having continuous reset mechanism) used to read the pixel signal.

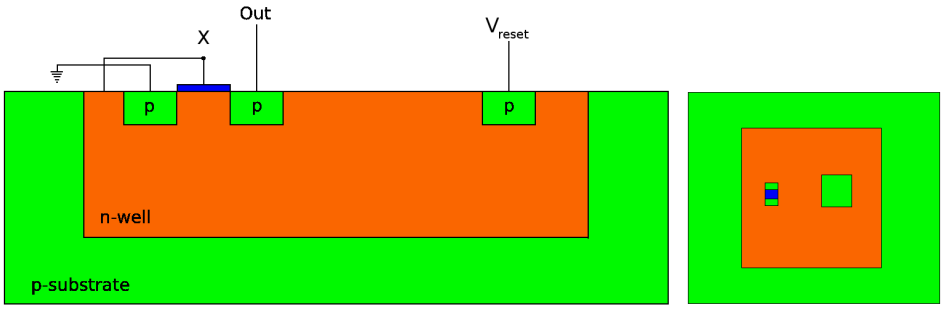

Figure 6.5: Schematic views of the pixel cell with a continuous reset.

charge is collected, the leakage current will continue to lower the voltage at the input node (Fig. 6.6). On the other hand, when a sensor having a continuous reset is hit, the input node has a voltage step and the reset diode is strongly biased in forward direction; consequently, it starts to provide current at the input node increasing the voltage level up to the point where ΔV on the reset diode allows to provide only the leakage current required by the collection diode (Fig. 6.7).

Many variants have been implemented in the same matrix (see Tab. 6.1), trying to optimize the device performance: four different types of transistor have been used (obtaining the already mentioned four sectors of 8 columns each); moreover, different pixel sizes have been used to physically place the

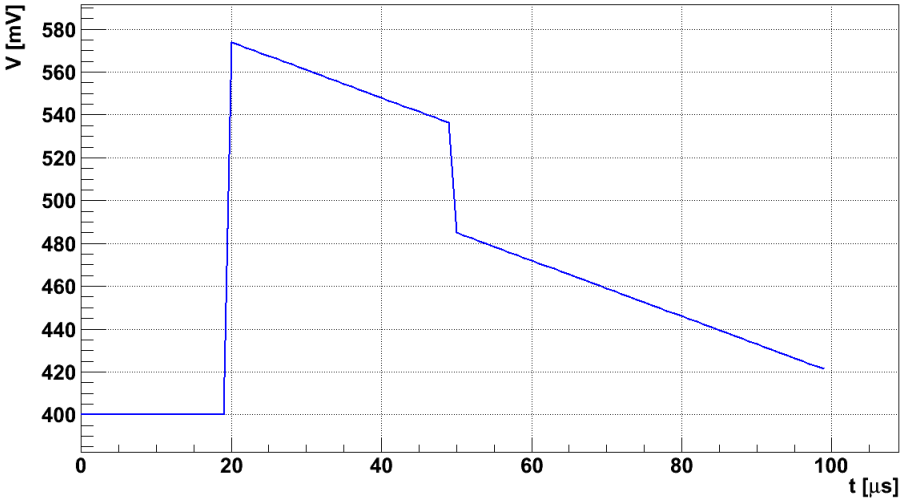

Figure 6.6: Voltage variations on the input node due to the reset switched on ($t \approx 20\mu s$) and to a particle hit ($t \approx 50\mu s$) for an active reset front-end electronics.

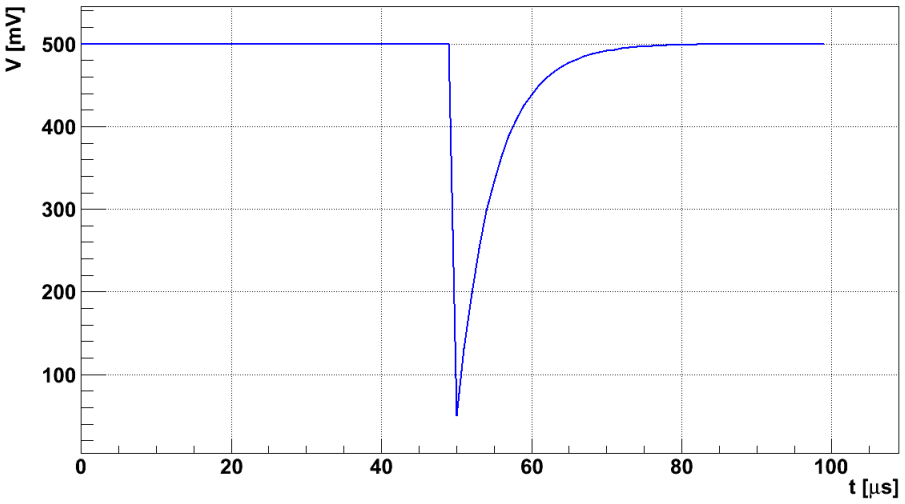

Figure 6.7: Voltage variation on the input node due to a particle hit ($t \approx 50\mu s$) for a continuous reset front-end electronics.

transistors inside the electrode. The last sector is based on a triple-well structure: on the p-substrate, a n-well acting as electrode is placed; the n-well hosts a p-well with a NMOS input transistor. The p-well is connected

to the source of the NMOS transistor. The behavior of transistors having

	Electrodes $[\mu m^2]$	Input Transistor	$W[\mu m]/L[\mu m]$
Sector 1	3.72×3.72	PMOS, low V_{th}	1.5/0.36
Sector 2	4.92×4.92	PMOS, low V_{th}	5/0.24
Sector 3	4.92×4.92	PMOS, Thick Ox.	5/0.24
Sector 4	4.12×3.72	NMOS, low V_{th}	0.48/0.48

Table 6.1: Collection electrode sizes and input transistor combinations.

a variable bulk voltage results particularly interesting. In fact, as already mentioned in the previous chapter, the transistor threshold is proportional to the square root of the V_{sb}: as soon as electron-hole pairs are generated, there is a voltage variation at the input of the front-end affecting both the gate and the bulk of the transistor, which are shorted. However, in first approximation, the small value of the variation should produce negligible effects on the transistor gain linearity.

Finally, the capacitance value at the input of the front-end electronics is particularly interesting. The different contributions to the input capacitance come from the collection electrode and the parasitic MOS capacitances. The source follower action will cause the gate-source capacitance and the bulk-source capacitance not to be seen. What remains is the gain-drain and the bulk-drain capacitance plus the routing and then the collection electrode capacitance.

The bias current of the pixel cell source follower is provided by a current source (one for each pixel) placed in the matrix periphery (Fig. 6.8). The

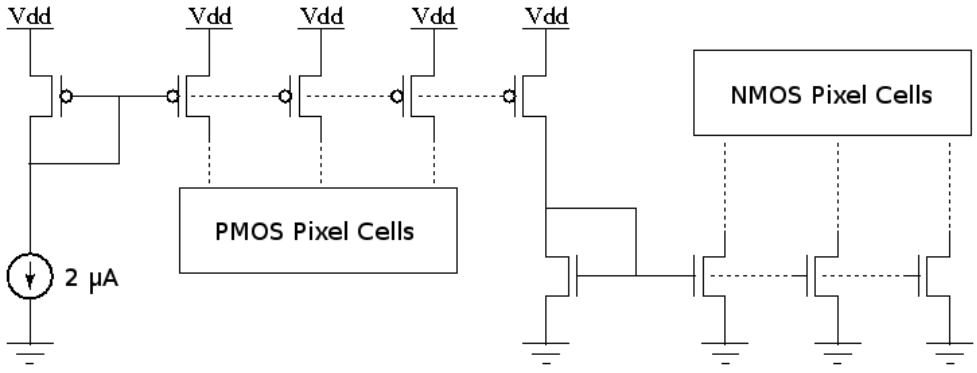

Figure 6.8: Current mirrors used to bias the pixel cells.

magnitude of the current can be set by a current mirror biasable by a matrix

pad: the current value can reach values up to 2 μA. Since the current to provide to the current mirror is in a few μA range, simple voltage dividers have been used to establish a voltage reference. This allows the use of discrete components. In Fig. 6.9 the resistors, the capacitors and the trimmers used are shown: they are external components placed on the biasing board.

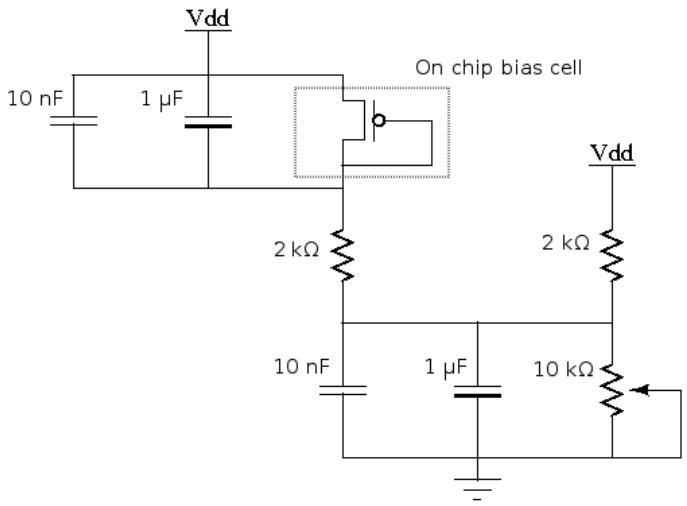

Figure 6.9: External circuit used to bias the current mirror inside the matrix chip.

6.3 Correlated Double Sampling

The pixel cell output is connected to the periphery by a metal line. As already mentioned, each pixel has it own metal line which connects the pixel cell to the corresponding read-out electronics; the metal line represents also an additional capacitive load from the pixel cell to the periphery with a simulated capacitance of $C_{line} \approx 200\ fF \pm 2\ fF$. The input signal is stored by using the *Correlated Double Sampling* (CDS) approach. The CDS method was introduced by [40] as signal processing technique removing the switching transient and the Nyquist noise introduced by the reset mechanism. It is based on a double storage of the output voltage value on two different capacitors: the first one in known conditions, the second one after a desired Δt; the value measured during the first sampling is then subtracted to the second value acquired to obtain a voltage value proportional to the signal

generated at the input by a particle. The main advantages of this technique are the offset voltage removal and the elimination of the reset noise. In fact, by acquiring the output voltage when there is no signal at the input, it is possible to produce the so called *pedestal* values which can be used to set a baseline during the acquisitions with events: in this way, by subtracting the pedestal values and the values taken during the acquisition, it is possible to obtain a voltage value due only to the impinging particles (see Fig. 6.10). The reset noise is also removed by applying the CDS. In fact, the Nyquist

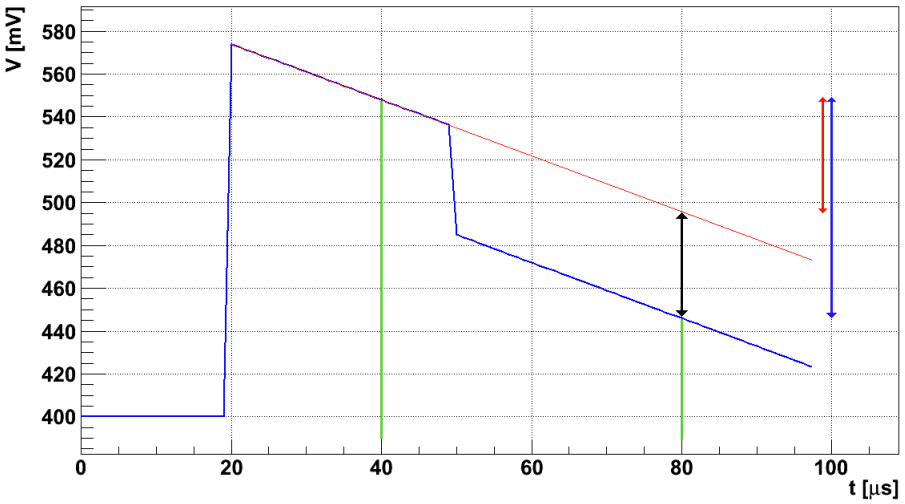

Figure 6.10: Schematic view of the CDS method: the green lines represent the two stores, the red line represents the acquisition with no signal (pedestal), the blue one with signal, the red and blue arrows the ΔV obtained with the double sampling and the black arrow the final ΔV obtained by removing the offset.

noise contribution of the reset switch is given by $V_n = (kT/C)^{1/2}$ (or $Q_n = (kTC)^{1/2}$ in terms of noise charge); since the signal at the output of the chain is given by the difference between two voltage values in a chosen time window, the reset noise results to be correlated within that time window. Summarizing, it can be written:

$$\begin{cases} V_{out1} = V_{off}(t) + V_{noise} \\ V_{out2} = V_{off}(t) + V_{noise} + V_{signal} \end{cases}$$

where $V_{off}(t)$ is due to the leakage effect on the voltage, which can be evaluated by pedestal acquisitions, V_{noise} is the noise at the sampling capacitors (given in both the capacitors by kT/C) and V_{signal} is the voltage drop due to the impinging particle: by subtracting the two values, it is possible to obtain:

$$\Delta V = V_{signal}$$

which is proportional to the input charge. The CDS approach is often used in monolithic detectors to store the signal inside the pixel cell; however, the main difference between the common CDS and the CDS used in the LePix approach is that the voltage levels are stored outside the pixel. In this way the duration of the sensitive period can be decoupled from the readout time, which could be too long for pixels to keep the signal charge if the leakage current is too large. In fact, it is difficult to estimate the leakage current since this technology is normally implemented to work with a nominal operating voltage of 1.2 V, which is not the case of the LePix sensor having a strongly reversed substrate.

The read-out electronics of the matrix is placed on the chip periphery, where a triple structure has been implemented; consequentially, both NMOS and PMOS transistors can be used. In Fig. 6.11 a schematic view of the double sampling mechanism implemented in the matrix is shown: a first couple of complementary CMOS is used to sample the pixel analog voltage on two external capacitors ($MEM1$ and $MEM2$). These switches are implemented with regular PMOS and NMOS small transistors in order to reduce the leakage current through $MEM1$ and $MEM2$. The capacitors are implemented as wide metal-to-metal structures placed along the pixel column: 64 capacitors are present on each column, two capacitors for each pixel cell. The value of the storing capacitances are estimated to be 270 $fF \pm 2$ fF. Two NMOS transistors, one per storage capacitor, are used in source follower mode as voltage buffer to transfer the analog information from the capacitors to the output pad (the circuit used to provide current to the source follower is similar to the circuit shown in Fig. 6.9); current flows only through these transistors when the storage capacitor is selected during the readout phase and the follower is biased by NMOS current source common to all pixels. In this way only one follower is active at a time avoiding unnecessary power consumption. Its current can be adjusted between 10 μA and 400 μA. The

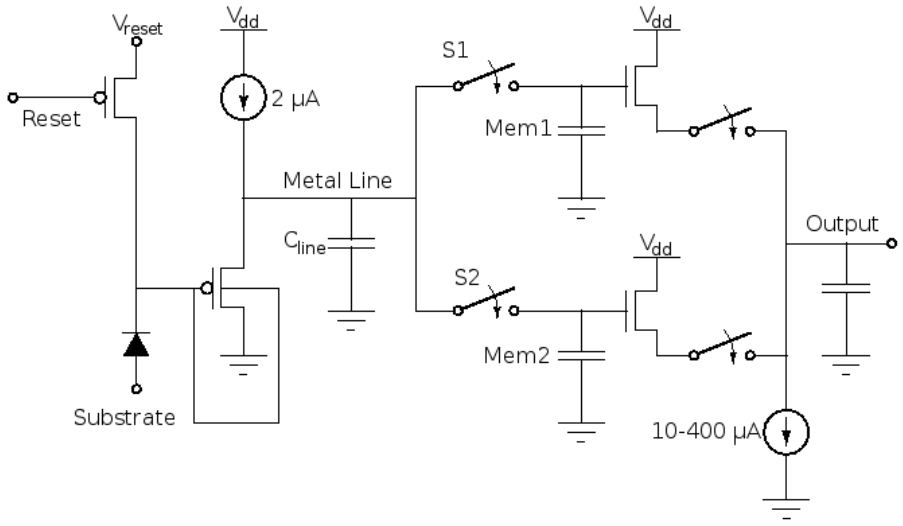

Figure 6.11: Simplified schematic view of the front-end and read-out electronics of the matrix structure.

read-out electronics for the last sector (NMOS input transistor) is slightly different: a PMOS source follower is inserted between the output of the NMOS follower in the pixel and the switches used to store the pixel signal; the PMOS follower drives the storage capacitors. The read-out electronics after the storage capacitors is identical to the read-out used in the other sectors.

The signals to control the analog storage and the serial read-out are controlled by the digital part of the electronics, placed in the matrix periphery. The digital part is based on five digital signals, which allow to set an acquisition time and store the analog values, and a shift register based on 2048 D flip-flops, which controls the switches to read the signal coming from storage capacitances. During the acquisition phase (see Fig. 6.12 and Fig. 6.13), the START signal is brought high and the clock signal is not propagated to the pixel matrix. The pixels equipped with a reset transistor and the shift register are reset using the signal RESET, and the reference analog value is stored in the first memory by signal MEM1. Storage in a second memory is carried out by the signal MEM2. MEM1 and MEM2 therefore define the time window corresponding to data taking. When START is brought low, the shift register starts to operate and pixels are read out sequentially. Two clock cycles are needed per pixel (corresponding to the two stored values).

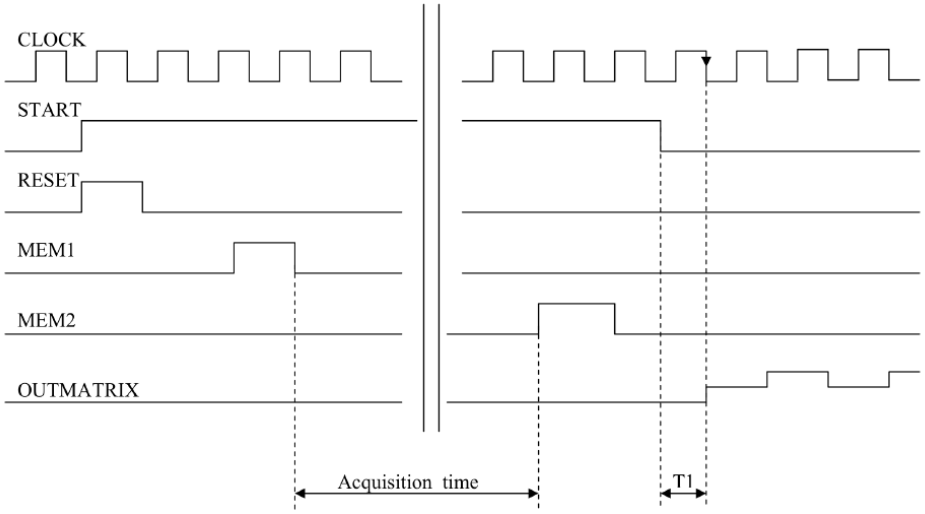

Figure 6.12: Digital signal of the matrix and analog output.

The shift register controls switches to connect the stored analog values to one unique output for the whole matrix. The transition to new data happens on the falling edge of the clock.

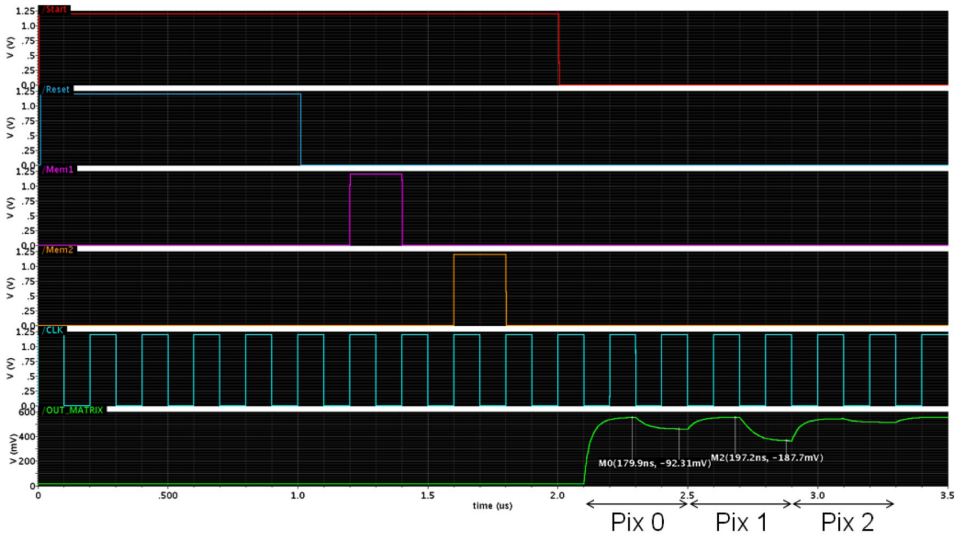

Figure 6.13: Simulated digital signals and output with analog serial readout for three different pixels (with respectively $2400e^-$, $4800e^-$ and less that $1000e^-$ generated by the impinging particle).

6.4 Experimental Equipment

The experimental equipment is based on a versatile DAQ system described in detail in [41]. The compact setup is made of a full custom DAQ analog board and a commercial FPGA development board. The DAQ analog readout board has five independent channels which can bias up to five sensors simultaneously. Each channel is composed by an analog input stage and a 14 bit-resolution and 105 Mega-Samples-Per-Second (MSPS) ADC ($ADS5541$). The ADC is driven by a 100 MHz reference clock; LVDS lines have been implemented for digital communication. The analog board is connected to a commercial FPGA development board through two high-speed SAMTEC connectors; the FPGA mounted is a $Xilinx\ Virtex5$. The development board allows to use many other support circuits such as a 64 bit access bus DDRAM, a complete set of communication devices (Ethernet, USB, RS232, RocketIO) and a clock generator. The system is controlled by USB 2.0 standard communication which allows to reach a stream capability up to 25 $Mbyte/s$. The DAQ analog board is then connected to a so called *mother*

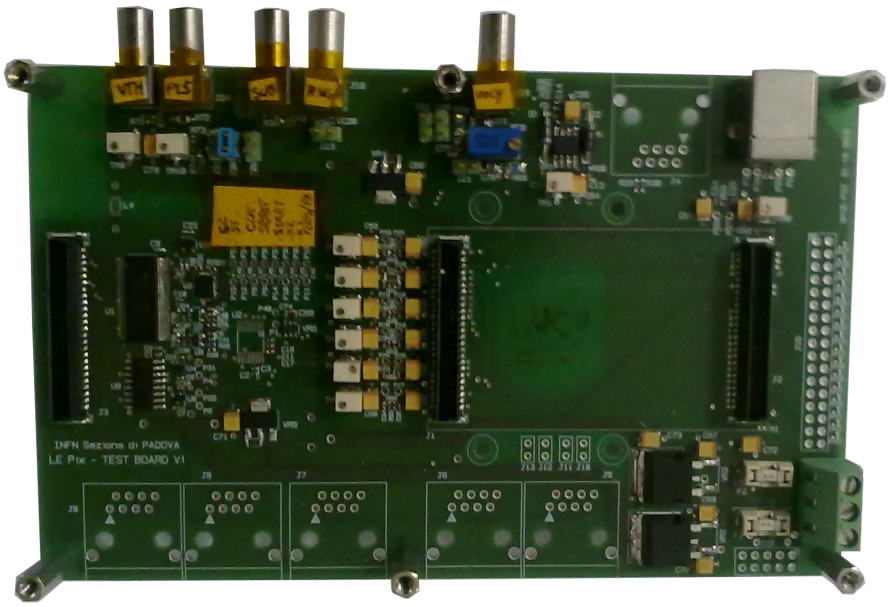

Figure 6.14: Mother board used to provide the main biases to the chip.

board (Fig. 6.14) which contains the circuitry to provide the main biases and power supplies to the chip (analog and digital power supplies, analog and digital grounds, current for the source followers etc.). Moreover, the mother board allows to connect external power supplies which can provide directly the biases, such as the substrate bias or the polysilicon layer bias, to the chip. A so called *daughter board* or *mezzanine* (Fig. 6.15) is then connected to the mother board through SMC-ERNI connectors. The sensor is glued to the mezzanine by a thermic glue and is biased by wires connecting the pads of the sensor with the metal lines of the mezzanine. The most crucial point

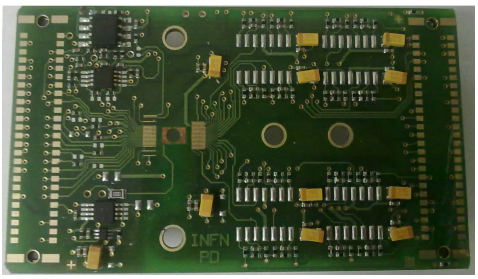

Figure 6.15: Mezzanine hosting the sensor.

in the mezzanine design is represented by the chip output: in fact it provides a signal which has to be sent to the ADC minimizing the noise. The analog signal path starts with a low power, high speed feedback amplifier ($AD8011$) which allows both to amplify the input signal and to adjust the signal offset by an external control (Fig. 6.16). The signal is then sent to a sideband, low-distortion, fully differential amplifier ($THS4501$) which provides two analog differential outputs (positive and negative). The differential signal is then sent via USB to the DAQ analog board where it is buffered by a fully differential, 300 MHz bandwidth amplifier($THS4503$). Finally, the signal is sent to the ADC to be digitalized: the exact sampling point can be externally set with a 70 ps resolution.
The DAQ system is controlled by a *ROOT* based online software ([46]) having a LabView look interface which handles all the communication to and from the DAQ itself (Fig. 6.17): in this way it is possible to set all the timing parameters which will be sent to the sensor, in particular the digital signals sent to the matrix (START, RESET, MEM1 and MEM2 signals). The software provides an online chip view (Fig. 6.18), which allows to check directly the response of each pixel, and allows the data saving for off-line

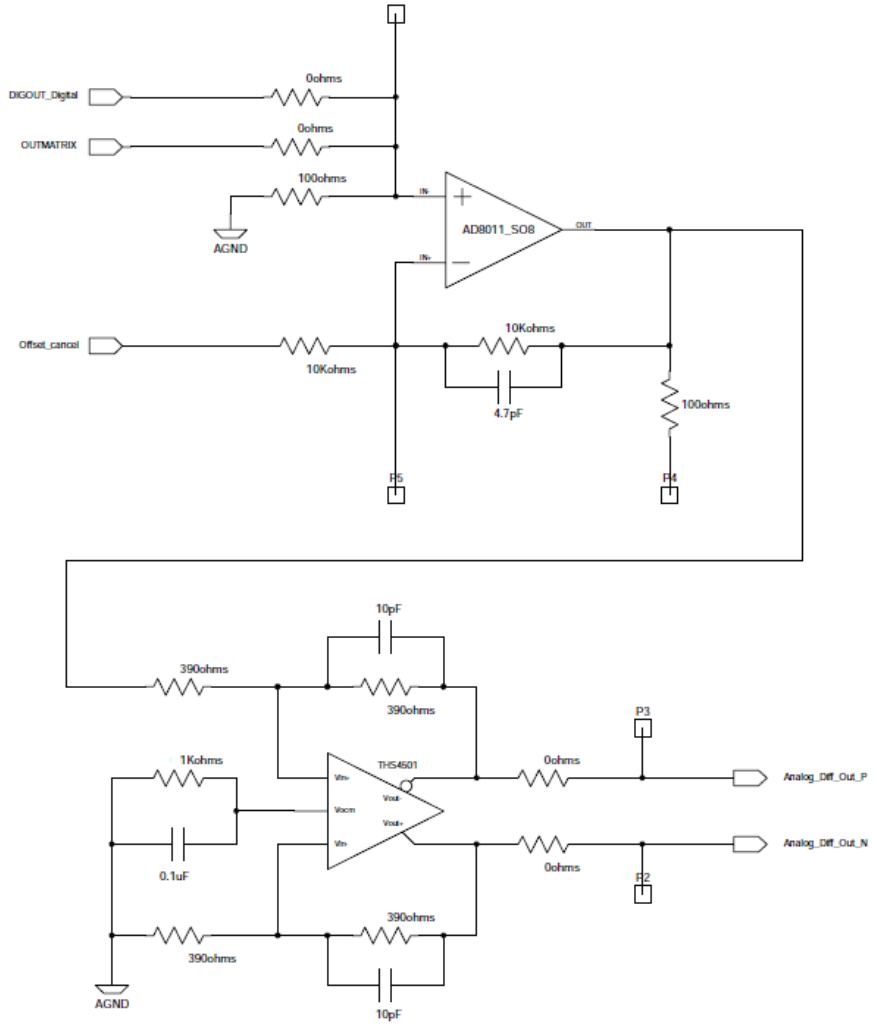

Figure 6.16: Schematic view of the circuitry on the mezzanine.

analysis. The DAQ system has been designed to work at a clock frequency up to 25 MHz. However, the $LePix$ prototype tested has not been thought to be used in an environment where high frequency is required but it has been designed to check the validity of the approach used; consequently, the DAQ has been used at a lower clock frequency ($f = 390\ kHz$): the frequency used allowed to have no problem due to slew rate limitation.

Figure 6.17: Schematic view of the I/O communications: the *ROOT* based software allows to set the timing of the signals sent by the DAQ to the boards; then the signals at the output of the boards are elaborated by the DAQ to be saved by the software.

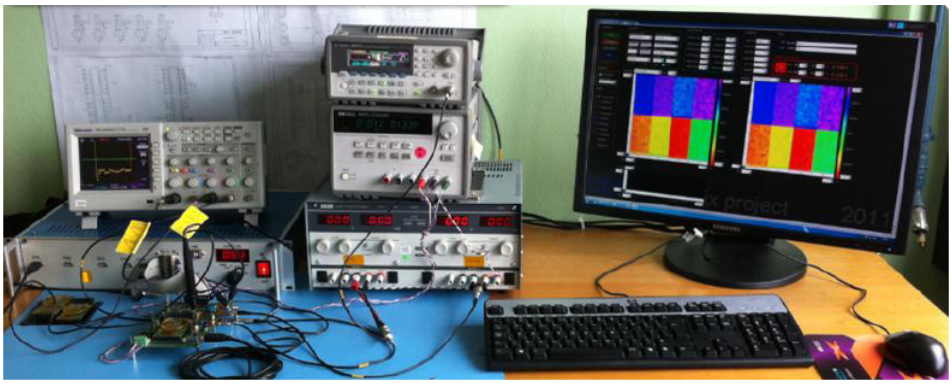

Figure 6.18: Experimental equipment used to test the LePix matrix: in the bottom part on the left it is possible to see the DAQ box and the boards, in the central part the power supplies used to bias the chip and on the right the online view with the matrix sectors.

Chapter 7

Analog Matrix Characterization

In this chapter, the measurements done to characterize the analog matrix will be described; in particular, in the first part the characterization of the experimental setup and the setting of the DC parameters will be shown while the second part will be focused on the sensor capacitance, the leakage current and the noise measurements.

7.1 Equipment and Bias Characterization

In the previous chapter, the circuitry placed on the mezzanine has been described: it is based on two integrated circuits which allow to amplify the signal (the former) of a nominal factor of 2 and to have a differential output (the latter). The signal is then sent to an ADC which digitizes the input voltage signal producing discrete ADC counts. The first step of the matrix characterization consists into a calibration to obtain the real conversion factor from the output of the chip to the output of the ADC (which means a conversion factor from ADC counts to milliVolts at the output of the chip). An input pulse has been sent directly to the amplifying stages of the mezzanines, by connecting the contact called *OUTMATRIX* (see Fig. 6.12) to a pulse generator, and the ADC output has been stored. By knowing the bit-voltage conversion of the 14-bits ADC and the slope of the calibration curve, it is possible to convert the ADC output in voltage values at the chip

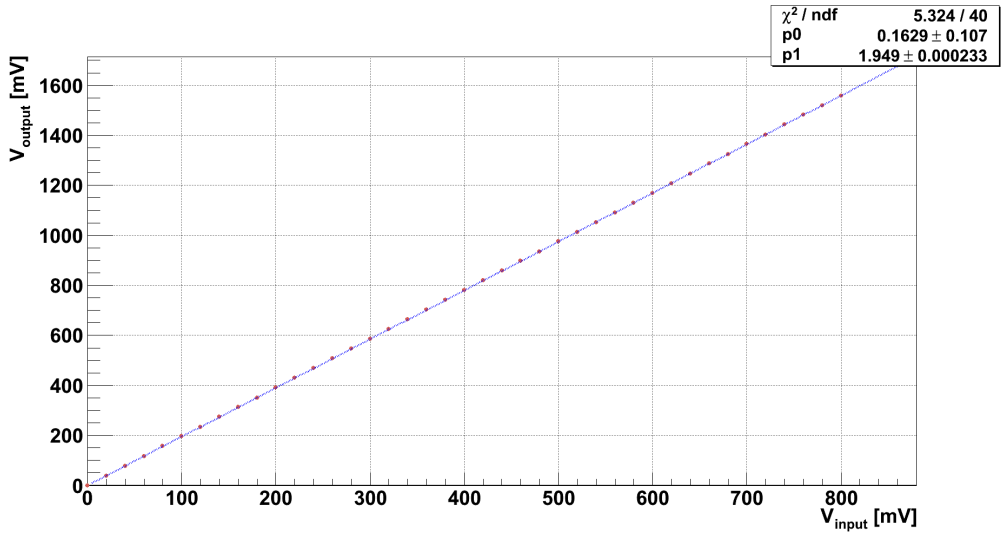

Figure 7.1: Calibration plot of the mezzanine circuitry.

output. The input pulse used to calibrate the circuitry has been chosen following the expected output of the chip: a negative pulse is expected having a DC value around $V_{dc} \approx 700\ mV \div 800\ mV$. In fact, the chip has been biased at $V_{dd} = 1.2\ V$ with a source follower as output stage. Consequently, a DC voltage of $V_{dc} = 800\ mV$ has been chosen at the input of the mezzanine circuitry, a negative pulse has been sent to the mezzanine circuitry and the output of the ADC has been stored; by knowing the ADC voltage range and the bits number, it has been possible to obtain the gain of the mezzanine circuitry (Fig. 7.1).

The second step of the matrix characterization has been the DC bias characterization based on the feedback obtained by the measurements on the diode structure and on the breakdown structure. In fact, by testing the previous structures it has been possible to understand the influence of the polysilicon layer and the metal layer biases (from the breakdown structure) and the influence of the parasitic current coming from the sample edges (from the diode structure). The main difference between the matrix structure and the previous tested structures is due to the shallow trench isolation and the oxide underneath the metal, which are now biased respectively by the polysilicon layer and the metal layer having a common contact (which is not the case of the breakdown structure, having two different contacts). Consequently, it has been possible to study the influence of the same param-

eters (metal-polysilicon bias and edges current) on the matrix structure. In

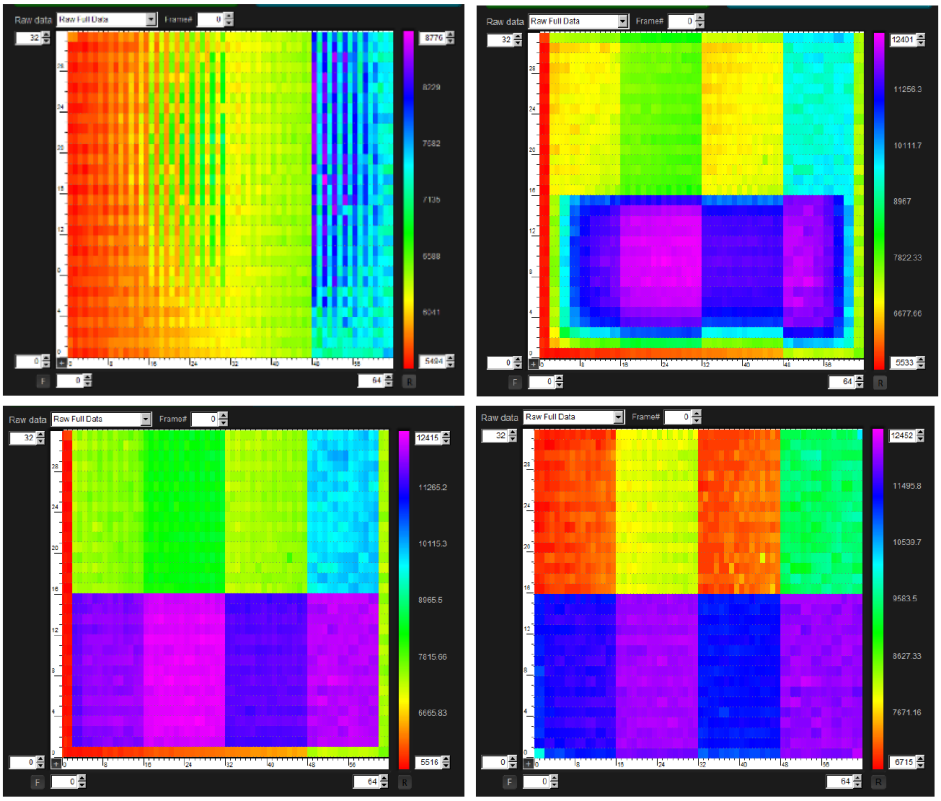

Figure 7.2: Polysilicon and metal layer bias effect on the matrix at $V_{poly-metal} = -2\ V$ (top-left), $V_{poly-metal} = -5\ V$ (top-right), $V_{poly-metal} = -20\ V$ (bottom-left), $V_{poly-metal} = -30\ V$ (bottom-right): the different colours represent the different voltage values for the matrix sectors.

Fig. 7.2 it is possible to see the influence of the polysilicon and metal layers bias on the matrix for a negatively biased substrate: when the layers are weakly negatively biased, there is current coming from the edges, there is current flowing between the sensitive part, made of several electrodes, and the n-well surrounding it and there is current flowing between electrodes whenever a ΔV between electrodes appears. When the polysilicon and the metal layers start to be strongly negatively biased ($V_{poly-metal} = -20\ V$), the current flowing within the sensitive part is stopped by the polysilicon layer which closes any current channel and the different sectors of the matrix start to be visible; however, in Fig. 7.2 it is possible to see a sort of frame

surrounding the sensitive part which is due to the current still flowing between the sensitive part and n-well (there is no current flowing in the upper part because of the electrodes used to monitor directly with the oscilloscope the sensors output, the gray electrodes shown in Fig. 6.1, which shield the inner sensitive part from the current). This current is due to the n-well which extends underneath the polysilicon layer placed in the outer part of the sensitive region of the matrix. The inversion layer in that region will be biased at the same voltage value of the n-well creating a conductive path from the n-well to the outer electrodes. The polysilicon is unable to turn off that parasitic path. Only when the polysilicon-metal contact is strongly negatively biased ($V_{poly-metal} = -30\ V$), the inversion layer is removed and there is no more parasitic current flowing in the sensitive part: this voltage is consistent with the very negative threshold for the metal layer, already seen in the breakdown structure. Since the polysilicon layer cannot turn off the current, it is necessary to go beyond the metal threshold and use the bias of that layer to suppress any parasitic path.
Only when the parasitic current is stopped by the polysilicon-metal layers, it is possible to pull down the substrate to check for possible breakdown of the n-wells. Consequently, by having the polysilicon-metal layers strongly negatively biased, the substrate has been pulled down measuring the substrate current (following exactly the same procedure used to obtain the plot shown in Fig. 4.6). In Fig. 7.3 the current flowing in the substrate reversely biased is shown. As already observed for the diode structure, it is possible to see an increasing current flowing in the sample, in particular for substrate bias higher than $|V_{sub}| = 50\ V$: it sets in when the depletion layer extends to the scribe-line which then injects current into the depletion layer which is then collected by the perimeter of the matrix (the n-well surrounding the central part). Moreover, an increase of this current has been observed over time, due to thermal runaway. The current is collected only by the n-well surrounding the central part while it will not affect the pixels in the matrix. Fig. 7.4 show the typical output of the matrix once the parasitic currents have been stopped by the metal and the polysilicon layers ($V_{poly-metal} = -30\ V$) and the substrate has been negatively biased ($V_{sub} = -30\ V$). As already mentioned in the previous chapter, the pixels are read sequentially, column by column, starting from the Sector 1 having the active reset. In Fig. 7.4 it is possible to see the four different sectors: the first one from 0

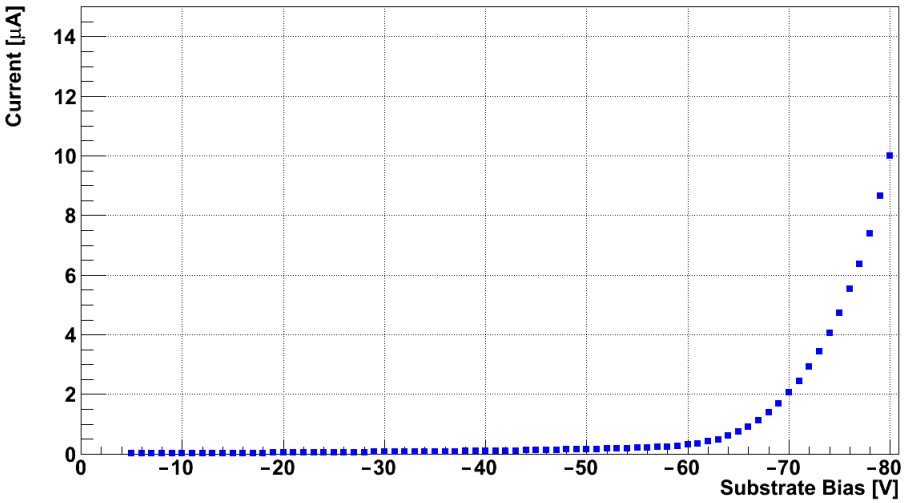

Figure 7.3: Substrate Current vs Substrate Voltage in the matrix structure .

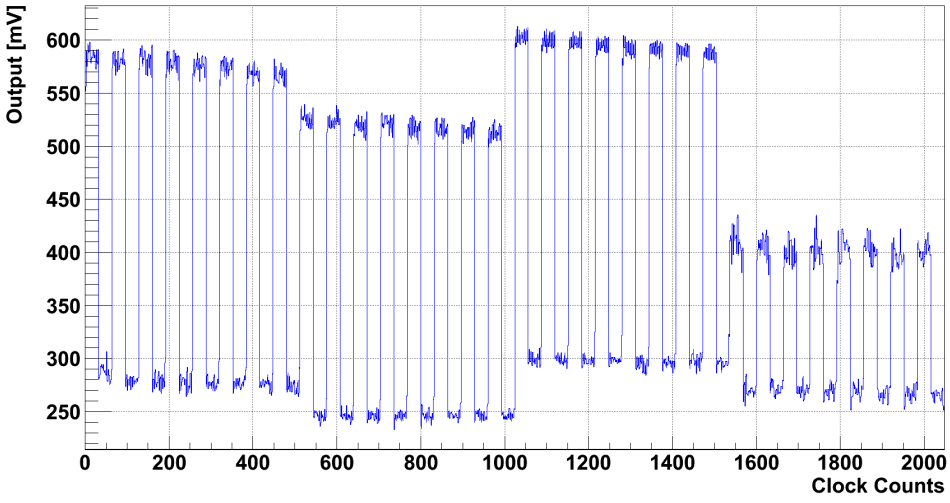

Figure 7.4: Typical output of the matrix.

clock counter to 512 clock counters (8 columns of 32 pixels each, for a total pixels number of 256 with two samples per pixel), the second one for the next 512 clock counters and so forth. For each sector it is possible to see a repetitive pattern due to the 16 pixels of the active reset and the continuous

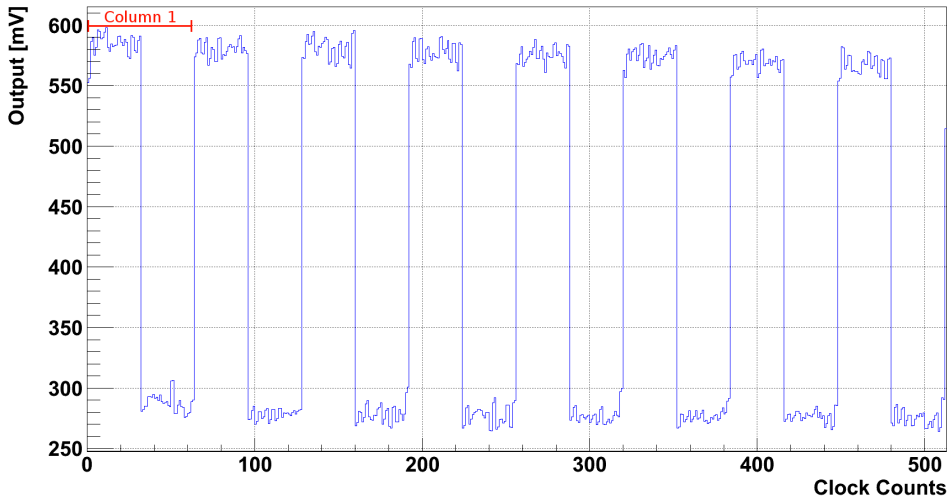

Figure 7.5: Sector 1 output.

reset, the formers having a DC value higher than the latters (see Fig. 7.5 for the first sector). The active reset gives a higher output voltage because the active reset transistor is capable of pulling the pixel input up to V_{reset}. The continuous reset is carried out by a diode: there is a voltage drop across this diode to have it absorbing the leakage current from the sensor. The difference between the different sectors is due to the difference in the input transistor: they absorb the same current but the V_{gs} required to do this depends on the transistor type.

7.2 Sensor Capacitance Evaluation

Once the DC points of the matrix have been set, it is possible to estimate the capacitance of the sensitive electrode of the matrix. As already mentioned in the previous chapter, the collecting electrode is biased by a fixed voltage (V_{reset}) in common to all pixels. However, the bias mechanism for the first row and the seventeenth row (which are respectively the first row of the pixels having an active reset mechanism and the first row of the pixels having a continuous reset mechanism) is slightly different (see Fig. 7.6). It is based on a voltage bias (V_{pulse}) which can pulse the sensor capacitance

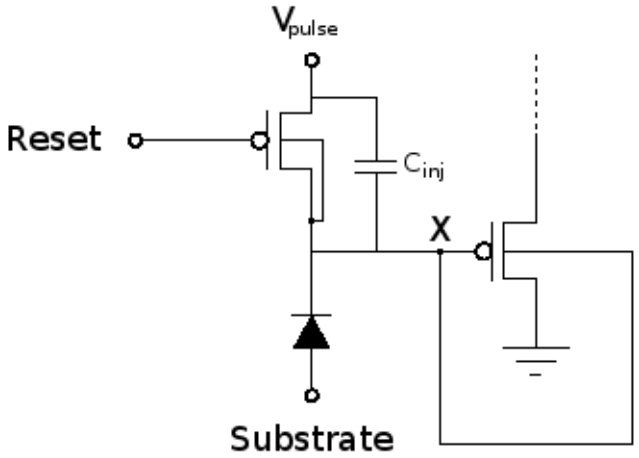

Figure 7.6: Pulse mechanism used to evaluate the sensor capacitance.

through an injection capacitance, having a simulated value of $C_{inj} = 1\ fF$. The injection capacitor is a metal to metal capacitor implemented as a line surrounded on all sides by neighboring metal, hence forming almost a tube around the line. The line in the tube is connected to the pixel and the tube is pulsed. By measuring the pulse at the output of the read-out chain, it is possible to evaluate the capacitance at the input. In Fig. 7.7, a schematic simplified view of the readout electronics is shown. The gain at the output

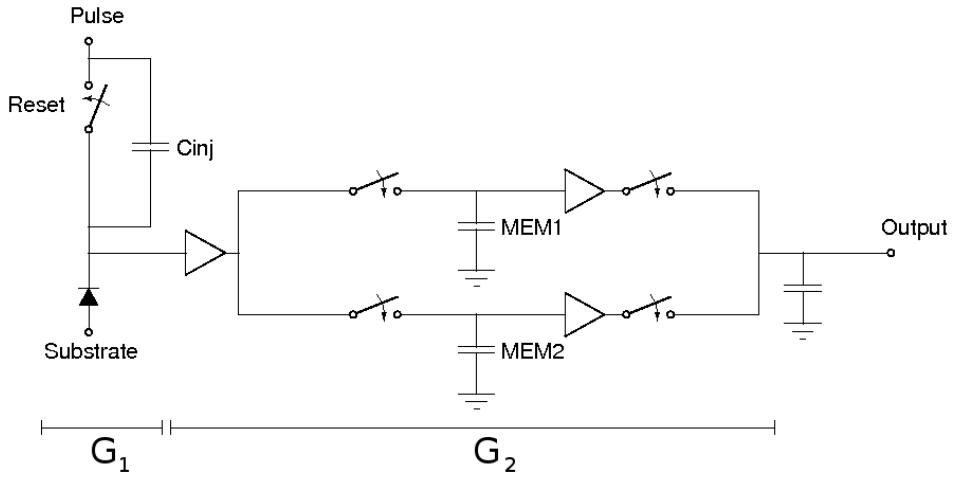

Figure 7.7: Simplified view of the pixel electronics readout.

of the readout electronics is given by the product of the first input stage,

a voltage divider made by capacitances, and the second stage, made of two source followers in cascade. The gain of the first stage is given by:

$$G_1 = \frac{C_{inj}}{C_{inj} + C_{in}}$$

where C_{in} is the input capacitance, given by the detector capacitance and the parasitic PMOS capacitances; the gain of the second stage is given by:

$$G_2 = G_{sf1} \cdot G_{sf2}$$

where G_{sf1} and G_{sf2} are the gains of the first and the second source follower of the electronics chain. Consequently it is possible to evaluate the capacitance at the input of the chain given by:

$$C_{in} = C_{inj} \left(\frac{G_2}{G_{tot}} - 1 \right)$$

The first step to evaluate the input capacitance has been to characterize the gain of the stage made by two source followers in cascade. To do that, a pulse signal having variable amplitude has been injected directly on the input transistor measuring the output pulse (Fig. 7.8) and, consequently, the gain; it has been possible only on the pixels having an active reset mechanism by having the reset transistor always switched on shorting V_{pulse} with the input transistor gate. During the circuit simulation phase, the DC ideal bias[1] has been found around $V_{dc} \approx 700 \div 800\ mV$ for the PMOS input transistors and above $V_{dc} \approx 900\ mV$ for the NMOS input transistor. Consequently, a wide-range approach has been used, by measuring the gain from $V_{dc} = 700\ mV$ to $V_{dc} = 1\ V$. In Fig. 7.9, the gains of the front-end stage for the four sectors are shown: while the PMOS sectors have their maximum gain for $V_{dc} \leq 800mV$, the last sector (NMOS) offers its best performance for higher V_{dc}. Consequently, since the pulse bias is in common to all sectors, it is not possible to optimize the source follower gain of all sectors at the same time. Fig. 7.9 allows to appreciate the "high" gain of the two source followers (PMOS the former, NMOS the latter) in the first three sectors: it is due to the bulk connected to the gate, for the PMOS follower, and the bulk connected to the source, for the NMOS follower, which allow to maximize the gain of the source followers. The gain of the last sector is lower

[1] from now on, it will be called indifferently $V_{dc-pulse}$,V_{dc}, V_{reset} or V_{res}

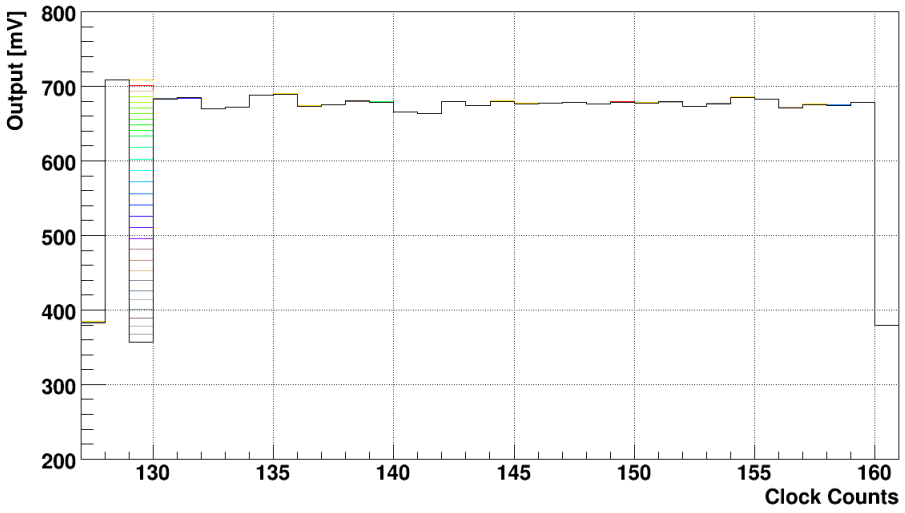

Figure 7.8: Typical oscilloscope output for a column of the first sector having an active reset mechanism: only the first pixel, connected to V_{pulse}, receives an input pulse, while all the other pixels of the column remain with a constant voltage value.

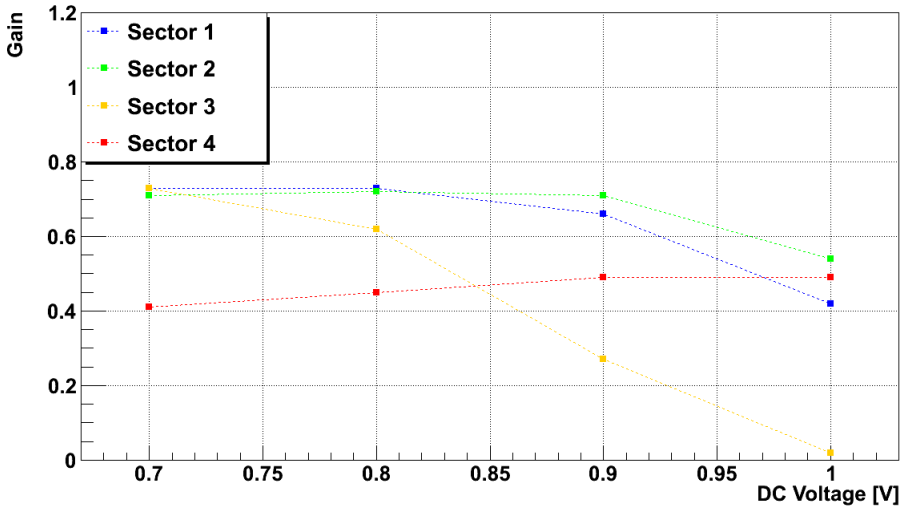

Figure 7.9: Measured source follower gain at different pixel input voltages.

due to a PMOS follower placed before the sampling stage: in that stage the fixed PMOS bulk causes a lower gain. In Fig. 7.10 the V_{output} vs V_{input} plot used to evaluate the gain of the two source followers in cascade of the third

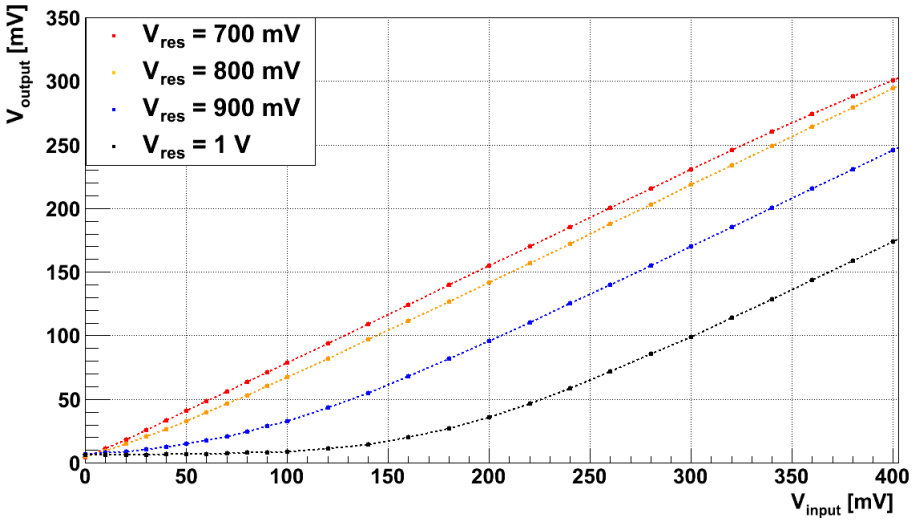

Figure 7.10: Measured output vs pixel input for the third sector for different pixel reset voltage.

sector (PMOS) is shown; similar plots have been obtained for all the other PMOS sectors (an opposite plot for the NMOS sector). In the PMOS sector it is possible to appreciate the gain decreasing with an increasing DC bias of the pulse. It can be explained as follows: by increasing the DC value of the pulse, also the input PMOS transistor source voltage value increases; however, for a too high DC voltage of the pulse signal, the transistor providing the current to the source follower is not saturated and, consequently, it cannot provide enough current to the output to follow the input, in particular for small pulses; when large pulses are set at the input, the transistor providing current can work in saturation and the slope of the gain curve is the same of the best condition slope. The situation is the opposite for the NMOS sector.

The measurement has been repeated by varying the substrate bias (from $0\ V$ to $-50\ V$) to check for possible influences of the substrate bias but it has been obtained a constant gain. Once the source follower gain has been characterized, it has been possible to estimate the input capacitance value for the pixel having an active reset using the timing shown in Fig. 6.12. In Fig. 7.11 the capacitance values for the different sectors are shown. The $V_{dc-pulse}$ has been optimized for the PMOS sectors ($V_{dc} = 700\ mV$) and

the NMOS sector ($V_{dc} = 1V$) measuring the capacitance values in different steps. Fig. 7.11 shows that the input capacitance is not very sensitive to the substrate bias. This indicates that the capacitance of the collection electrode to the substrate is only a fraction of the total capacitance, more dominated by the transistor capacitance and the capacitance of the collection electrode to neighboring electrodes at the surface. It is possible to see

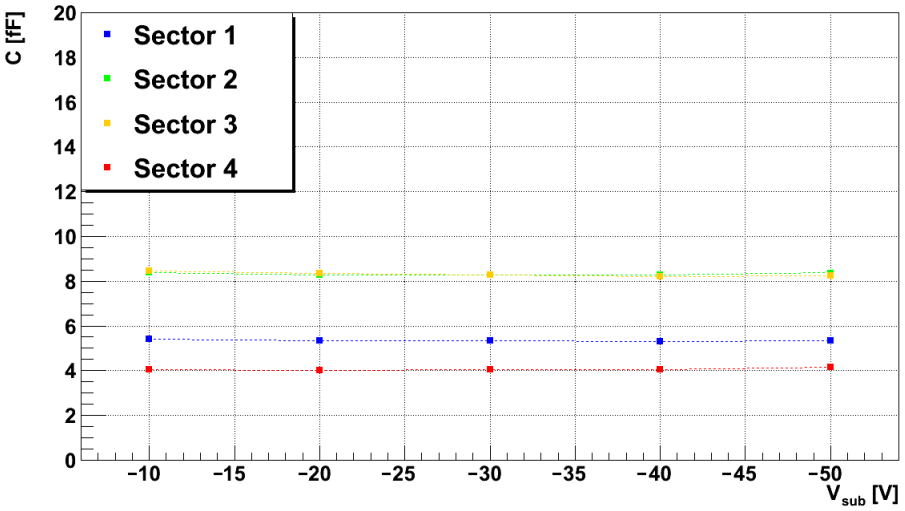

Figure 7.11: Input capacitance value for different substrate values.

the small femtoFarad regime reached by the input capacitance already for low reverse substrate biases.
The influence of the polysilicon-metal bias has been also evaluated, obtaining the result shown in Fig. 7.12. A strong influence of the polysilicon-metal bias on the capacitance value can be observed; in particular, the most important contribute is given by the metal layer. In fact, if the metal layer potential is above the inversion threshold, an inversion layer around the collection electrode is created, increasing the detector area and consequently the capacitance value. In Fig. 7.13, a simplified 3D view of the phenomena is shown: the charges surrounding the collection electrode create an inversion layer underneath the oxide. The inversion layer is connected to the n-well and, consequently, it has the same bias: the negative charges create a sort of n-doped layer which increases the sensitive area and the capacitance value. As already observed in the breakdown structure, by strongly reverse

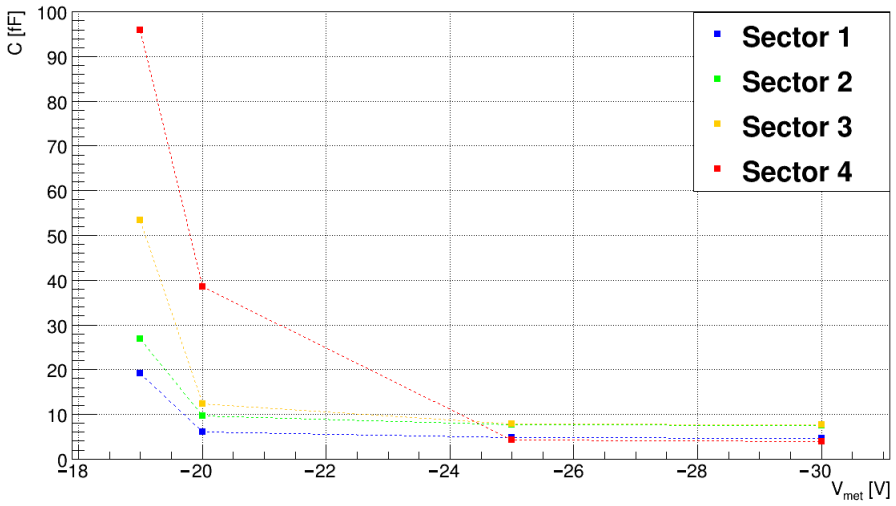

Figure 7.12: Input capacitance value for different polysilicon-metal values.

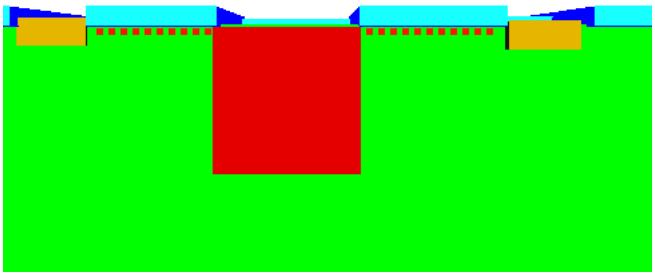

Figure 7.13: Simplified 3D view of the inversion layer increasing the electrode area.

biasing the polysilicon-metal contact, it is possible to remove those charges from that region and reach a small capacitance regime.
The evaluation of the capacitance for pixels having continuous reset is slightly more complicate. In fact, the reset mechanism, based on a diode, does not allow to have a direct access to the input of the front-end electronics; consequently, it is not possible to evaluate the contribute of the source followers in terms of total gain. Moreover, the DC value imposed by the diode on the gate of the input transistor is different compared to the value imposed

by the reset transistor: it can be clearly seen in Fig. 7.4 and in Fig. 7.5, where there is a several millivolts shift in the output between the active reset pixels and the continuous reset pixels. It can be assumed that the gain of the source followers in the continuous reset configuration will not differ much from the gain of the active reset transistor if the pixel bias (V_{reset}) is adapted to obtain the same output level as under nominal conditions for the active reset part. However, more accurate measurements are needed to evaluate the performance of the continuous reset sector: it will be better explained in the next chapter.

7.3 Leakage Current Evaluation

The effect of the leakage current on the circuit has been already discussed in the previous chapter: it causes a voltage drop for the pixels having an active reset mechanism while it is compensated by the reset diode for the pixels having a continuous reset mechanism. A direct measurement of the leakage current cannot be done. In fact, the current flowing in every single pixel cannot be measured directly by a current meter: by measuring the substrate current, it is possible to evaluate the current flowing in all pixels (plus the current flowing between the substrate and the n-well surrounding the central part of the matrix) which is not equally distributed because of the different pixels shape. Consequently, an indirect estimation of the leakage current has been done; it has been possible only in the pixels having an active reset mechanism, where the current causes a voltage drop at the input node. It can be written:

$$I = \frac{\Delta Q}{\Delta t} = C_{in}\frac{\Delta V}{\Delta t}$$

The term $\Delta V/\Delta t$ can be estimated by changing the integration time with no pulse at the input (that means to fix the timing of the first storing switch and to change the time of the second one), and measuring the output response, having an acquisition for each time-step of the second sampling.
In Fig. 7.14, the absolute value of the output response of one pixel of the first sector for different substrate values is shown (the real slope is negative because of the negative shift). It is possible to see a slope increasing with the substrate voltage, due to a higher leakage current, and a *plateau* reached

for high substrate voltage. This effect is due to the source-to-well diode of the reset transistor (Fig. 7.15). After the reset operation, the input node is released and the input drops due to the collection of leakage current until the source-to-well diode gets sufficiently forward bias to absorb the sensor leakage current. In fact, one evolves forward to the continuous reset situation. Both the leakage current of the sensor and the current provided by

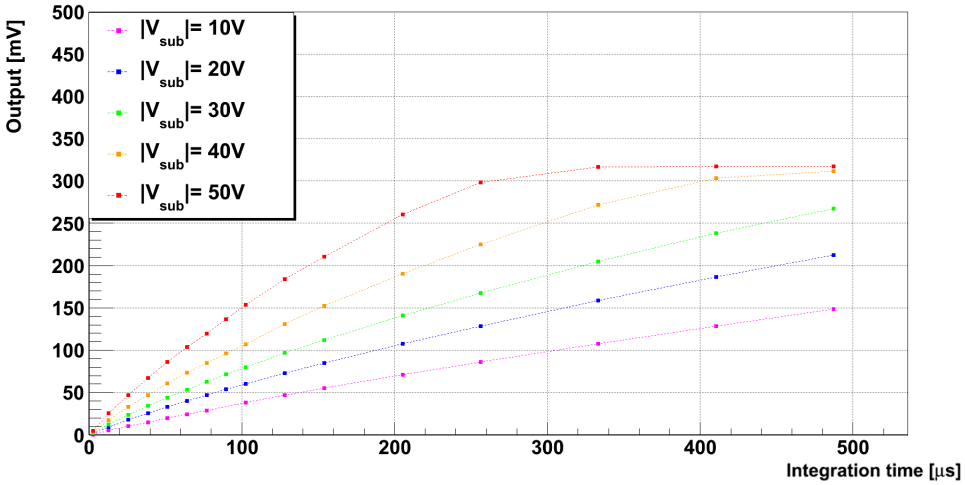

Figure 7.14: Output voltage variation for different integration time with no pulse at the input (the Y axis represents the difference between the first sample and the second sample).

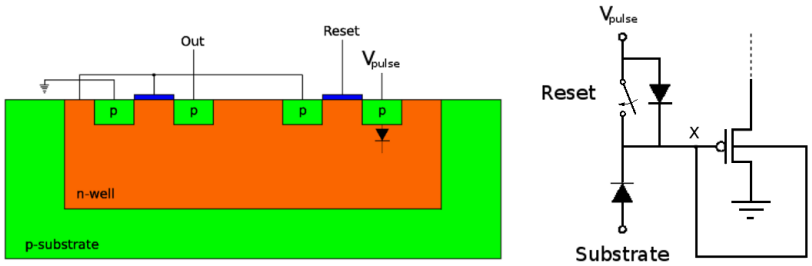

Figure 7.15: Simplified view of the active reset mechanism turning into a continuous reset mechanism for high substrate voltage and long integration time.

the conductive junction of the reset transistor are not constant with time.

However, the voltage drop at the X node can be considered negligible for the sensor leakage current (due to the high negative bias of the substrate) while the current provided by the conductive junction is slightly influenced by V_x; consequently, by using a linear interpolation of the dV/dt slope, an overestimation of the leakage current has been done. In Fig. 7.16, the leak-

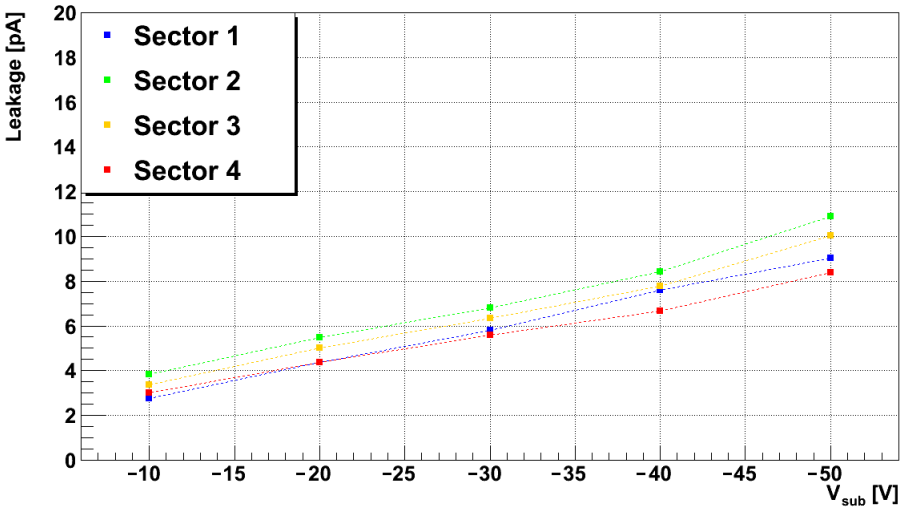

Figure 7.16: Leakage Current vs Substrate Bias for the four matrix sectors.

age current variation with the substrate bias is represented: it has been obtained by biasing the sensor with a DC voltage of $V_{dc-pulse} = 700\ mV$ for pixels having a PMOS input transistor and $V_{dc-pulse} = 900\ mV$ for pixels with a NMOS input transistor. In conclusion, by the measurements done it is possible to determine the leakage current to be around a few picoAmpere. Moreover, the leakage current measurement allows to establish the limit of the integration time at which saturation of the read-out electronics is reached. During the capacitance measurements, a safe-condition has been used by setting an integration time of $\approx 13\mu s$. Since the voltage drop at the input is expected to be a few hundreds of mV, most of the substrate voltage values down to $V_{sub} = -50\ V$ can be used by having an integration time $t \approx 100\mu s$.

7.4 Matrix Noise

The CDS method has the intrinsic advantage to remove the noise introduced by the reset mechanism. Consequently, in the LePix structure, the main sources of noise which affect the measurements are the leakage current of the diode and the noise of the front-end electronics.
It is well known that the leakage current in a reverse biased diode is due to the random generation of electrons and holes within the depletion region that are then swept by the electric field applied to the diode. The current can be modelled by a Poisson distribution having an error given by the square root of the number of electrons causing the leakage current. It can be written:

$$\Delta N \propto \sqrt{\frac{I_{leak} \cdot t}{e^-}}$$

where ΔN is the error in terms of number of electrons.
By knowing the leakage current and the integration time, it is possible to estimate the expected noise related to the leakage current: by having an integration time around 10 μs and a leakage current of a few picoAmpere, the noise contribution of the leakage current is a few tens of electrons.
The second source of noise is represented by the front-end electronics, in particular by the input transistor of the first stage based on a source follower. Since the noise related to the input transistor is in inverse proportion to the transconductance, by maximizing the transistor transconductance it is possible to decrease its noise contribute. In Fig. 7.17 it is possible to see the Equivalent Noise Charge (ENC) for the four matrix sectors with the pixels bias optimized ($V_{reset} = 700\ mV$ for the pixels having a PMOS input transistor and $V_{reset} = 900\ mV$ for the NMOS input transistor) and a substrate bias of $V_{sub} = -30\ V$. It is possible to appreciate the two different noise contributes: the input transistor noise, which is dominant for small integration times, and the noise caused by the leakage current of the diode, which is dominant for large integration times. Moreover, it is possible to compare the noise for the different sectors: the first sector, which is based on the smallest electrode, has the lowest noise while the noise in the central sectors is higher. The last sector, which has the same electrode sizes of the first sector, has to be discussed separately. In fact, it is based on a triple well structure (p-well inside an n-well) hosting the NMOS input

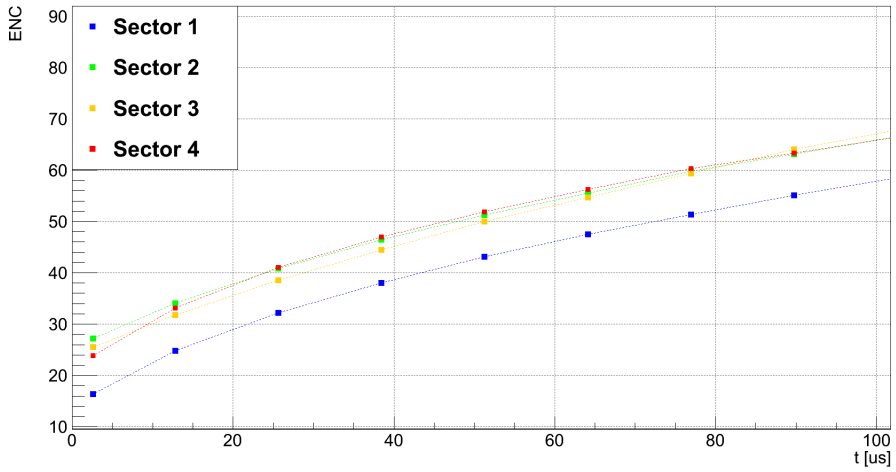

Figure 7.17: Matrix noise for all matrix sectors with the pixels biases optimized ($V_{dc-pulse} = 700\ mV$ for the pixels having a PMOS input transistor and $V_{dc-pulse} = 900\ mV$ for the NMOS input transistor) for an inverse substrate bias $V_{sub} = -30\ V$.

transistor. The capacitance between the p-well and the n-well junction has no influence on the input because of the source follower action which shields the input from the capacitance; however, this capacitance does contribute to the noise. Moreover, the voltage value at the input of the front-end electronics is particularly influential in terms of noise. It can be better understood by looking at the Fig. 7.18: it is represented the noise of the last sector for different V_{reset} and a substrate reverse bias of $|V_{sub}| = 30\ V$. It can be clearly seen the influence of the front-end electronics and of the diode leakage current. For small integration time, the dominant contribute is given by the input stage: for low V_{reset} the source follower does not work in saturation, degrading the noise performance. For large integration times, the noise is influenced by both the leakage current of the diode and the noise of the source follower stage which is completely pushed out of saturation by the leakage current; consequently, the noise saturates as actual response of the NMOS follower bias. For high V_{reset} and low integration time the source follower works in saturation, minimizing its contribution to the total noise. However, also in this case, for high integration time the source follower is pushed out of saturation degrading the noise performance.

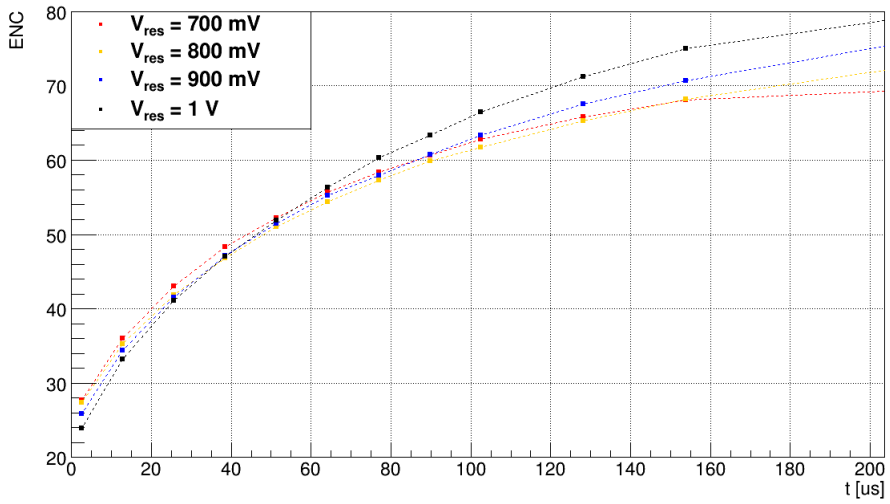

Figure 7.18: Noise for the last sector for different bias applied on the electrode and for an inverse substrate bias $V_{sub} = -30\ V$.

7.5 Larger Electrode Matrix

One of the goals of the previously described matrix is to reach a low capacitance range. As already described in the previous chapters, a low detector capacitance allows to increase the Q/C ratio having a large voltage signal at the input of the front-end electronics. In this way, it is possible to minimize the power consumption of the front-end electronics, which is one of the key-points in the design phase of a particle detector. However, a small size collection electrode tends to increase the electric field, in particular in the regions having a large voltage drop (ΔV) over a small distance (Δx). The main consequence could be local breakdowns due to the strong electric field which can cause unwanted large current in the diode.
During the design phase of the LePix matrix, an aggressive approach in terms of electrode size has been used by having the already describes electrodes. However, a backup option based on larger size electrodes has been designed, producing a matrix having the same front-end and read-out electronics but with larger collection electrodes. In Tab. 7.1, the main characteristics of the larger collection electrode matrix are shown. Similar measurements done for the smaller size electrode matrix have been done also for the larger size electrode matrix. The main consequence of the larger

	Electrodes [μm^2]	Input Transistor	$W[\mu m]/L[\mu m]$
Sector 1	8×8	PMOS, low V_{th}	1.5/0.36
Sector 2	8×8	PMOS, low V_{th}	5/0.24
Sector 3	8×8	PMOS, Thick Ox.	5/0.24
Sector 4	8×8	NMOS, low V_{th}	0.48/0.48

Table 7.1: Collection electrode sizes and input transistor combinations for the larger collection electrodes matrix.

electrode use is a larger capacitance compared with the previously tested matrix. In Fig. 7.19, the input capacitance for different substrate biases is

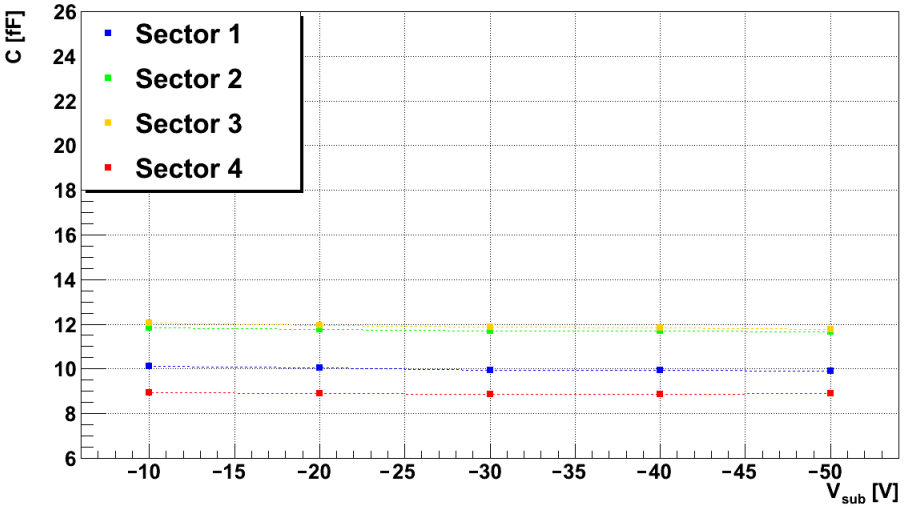

Figure 7.19: Capacitance of the larger collection electrode matrix for the four sectors.

shown. It is possible to see the different contributions of the input transistor capacitance for sensor having the same collection electrode: transistors having lower W and L have also a lower input capacitance. In Fig. 7.20, the leakage current of the four sectors for different substrate biases is shown. It is possible to see a lower leakage current than the smaller collection electrode matrix. In principle, the leakage current depends on the electrode size and on the depleted volume (see chapter 1). A larger collection electrode in spherical depletion approximation means a larger depleted depth; since the current in the larger electrode matrix is lower than the small electrode matrix, it can be assumed that the whole depleted volume is lower in the

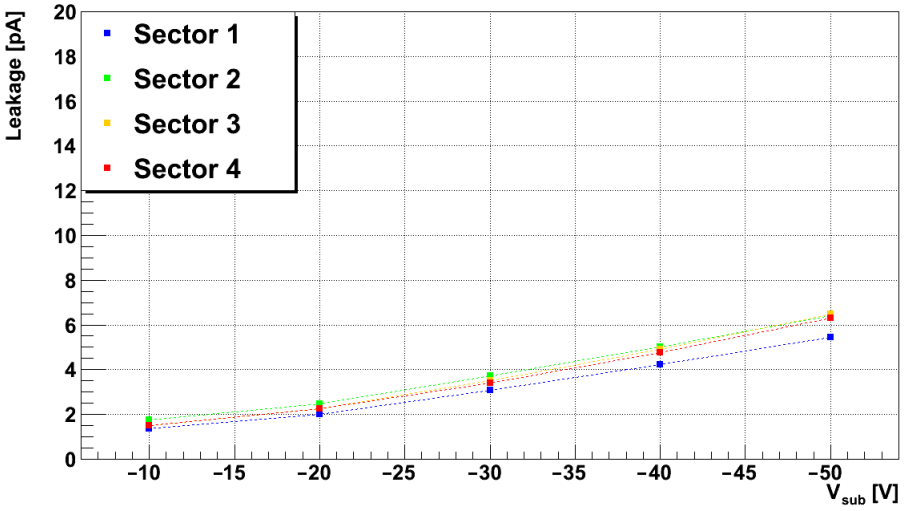

Figure 7.20: Leakage current of the larger collection electrode matrix for the four sectors.

former case than in the latter. However, it is not possible to have an exact estimation of the shape of the depleted volume only by pulsing the input: more complex measurements are required to define the shape of the depleted volume and to determine the real reason of the lower leakage current. The first part of the next chapter will be focused on the shape of the depleted volume.

7.6 Conclusions

The first measurements done on the matrix structure have been focused on the characterization of the main parameters of the detector, in particular the best DC working points, the input capacitance, the leakage current of the sensor and the input noise. The measurements show the validity of the LePix approach with interesting results in terms of input capacitance, evaluated to be in a few femtoFarad range, leakage current and noise, evaluated to be respectively a few pA and a few tens of electrons.
Also a less aggressive (in terms of electrode size) matrix has been tested obtaining similar performance but with a higher input capacitance: this matrix has been designed and produced to have a backup solution in case of a failure of the aggressive approach matrix. However, since the small

electrode matrix showed no failure during the first phase of the tests, the priority has been given to that matrix.

Chapter 8

Charge Collection Measurements

This chapter will be focused on the measurements done to test the matrix performance in terms of charge collection. In particular, it is divided in three parts: in the first one the laser measurements will be shown, in the second one the detection efficiency measurements with a X-ray source will be described and the last part will be dedicated to describe the sensor performance during a beam test.

8.1 Laser Test

During the first phase of the matrix measurements it has been possible to determine the basic detector parameters, such as detector capacitance, detector noise and leakage current, by using a calibration pulse or by changing the integration time. However, other parameters related to the charge generated by external agents are usually determined by high energy particle beams, which reproduce similar conditions as during the final use of detectors in particle experiments. The main problems related to the beam test are usually the availability of beam, the short amount of time available to make the test and the cost in terms of machine-time and man-power. Consequently, cheaper and more easily available alternatives are preferred. A useful alternative is represented by a well focused laser beam which offers a good spatial resolution together with a homogeneous energy charge generation. Usually, red laser (660 nm) or/and infrared laser (1060 nm) are

used: the former has a penetration depth of a few micrometers ($\approx 3.9\ \mu m$ in silicon) while the second one has an extinction depth of $\approx 890\ \mu m$, resulting particularly attractive for silicon detector because it can traverse the whole thickness of the sensor, mimicking a particle crossing. However, laser applications have a number of issues related in particular to the laser beam instabilities (due to small variation of the driver pulser, temperature changes, ambient humidities, etc.) and to reflection and refraction phenomena on the detector surface and on the subsequent layers (passivation, pads, protection, etc.).
A laser test on the LePix matrix can only be done via back-side illumination as the front-side is covered with many non-transparent metal layers. Moreover, it is well known that the depletion layer does not cover the full thickness of the sensor ($\approx 300\ \mu m$) reaching the backside of the chip; consequently, the backside has been tested only with a pulsed infrared laser ($1060\ nm$) capable to traverse the substrate reaching the depletion region. The pulsed laser has been set to have a time duration of $\approx 6\ ns$ and to be pulsed $\approx 80\ ns$ before the second sampling.
In Fig. 8.1 the typical output signal profiles obtained when the laser is moved in the region between two pixels with steps of $5\ \mu m$ and with two different substrate back-biases are shown: it is possible to see two peaks in the output profile having a distance $\approx 50\ \mu m$, corresponding exactly to the pixel pitch, and a clear signal loss in the region between two pixels; moreover, the signal loss does not depend significantly on the substrate voltage. Consequently, it can be assumed that the signal profile reproduces also the depletion region profile which causes an extensive charge loss in the region between two pixels, which is only slightly depleted. In fact, if there were no charge loss, the sum of the signal collected on the left and right pixels should remain constant versus laser position. However, the measurement confirms more signal is collected for an increased reverse bias, but also that charge is lost in between two pixels. As already explained in the previous chapters, a complex structure alternating metal layer over oxide and polysilicon layer over shallow trench isolation is placed in the region between two pixels; the metal layer and the polysilicon layer are both biased at $V_{poly-metal} = -30\ V$ to avoid parasitic unwanted currents flowing in the electrodes and to avoid an inversion layer around the electrodes. However, the strong reverse bias applied at the polysilicon-metal layer does not allow a correct expansion of

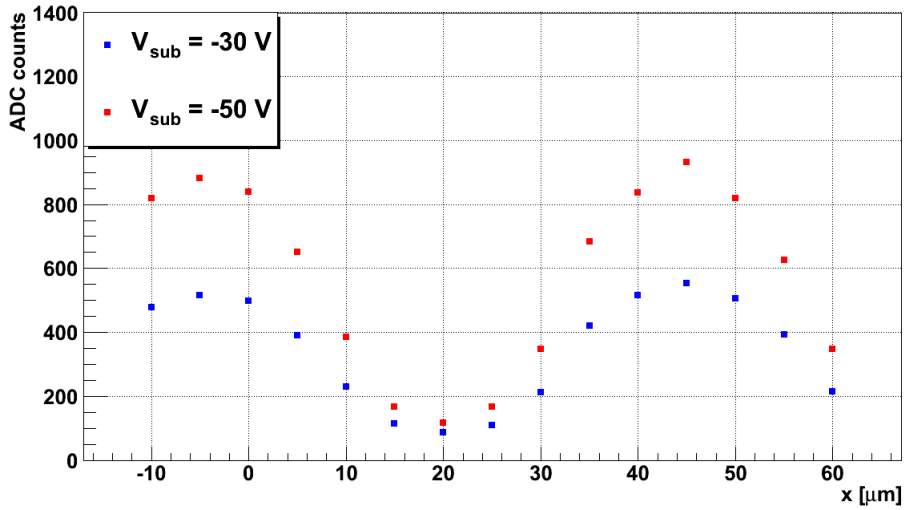

Figure 8.1: Laser scan results for two different substrate biases.

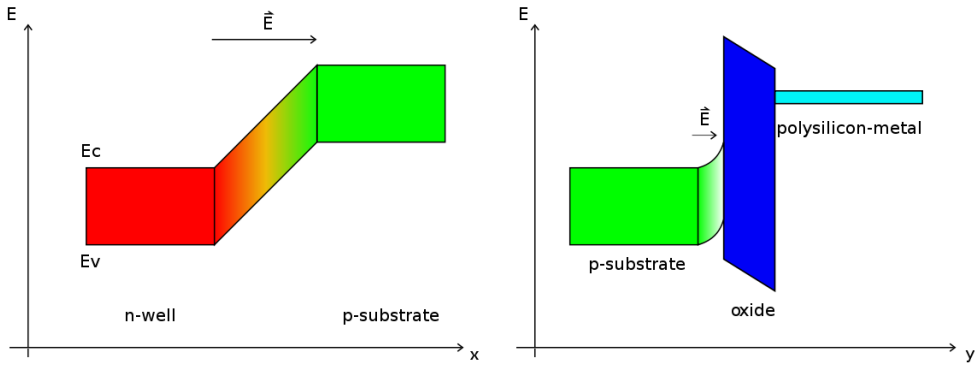

Figure 8.2: Simplified Energy-Band diagram of the n-well/p-substrate junction (left) and p-substrate/oxide/polysilicon-metal layer (right).

the depletion layer; in fact, the electric field is forced to be directed from the n-well to the p-substrate but, moreover, there is a second component which forces the electric field to move from the p-substrate to the silicon-oxide interface (Fig. 8.2). This effect is stronger on the interface between the silicon and the shallow trench isolation; in fact, the inversion threshold for the poly field transistor is very much closer to zero than that of the metal field, and biasing it at $V_{poly-metal} = -30\ V$ to turn off the region controlled by metal has the tendency to pull the silicon under the poly field into accumulation

hence reducing the depletion layer (Fig. 8.3). The inversion layer surround-

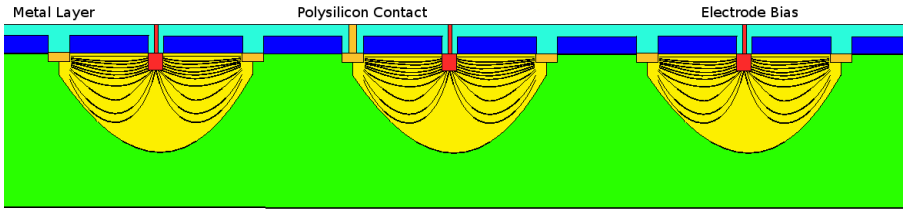

Figure 8.3: Simplified view of the depletion region and the electric field between matrix pixels (not to scale).

ing the pixel forces to operate with very high negative biases on the field plates and yields incomplete depletion and fill factor as the depletion layer does not extend over the full pixel area. The depletion can be extended further when an inversion layer is allowed but then the input capacitance is increased considerably. It is therefore clear that the area around the collection electrode has to be redesigned to prevent this issue.
By knowing the shape of the depleted volume, it is also possible to explain the different leakage current between the small electrode matrix and the large electrode matrix, described in the previous chapter. In Fig. 8.4 it is

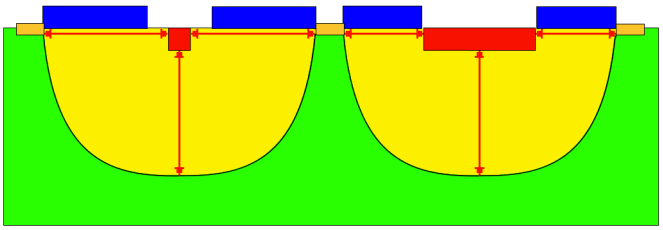

Figure 8.4: Simplified view of the depleted volume for small (left) and large (right) electrodes.

possible to see the approximated shape of the depleted volume for a small and a large electrode. By applying the same biases (substrate, polysilicon-metal and pixel bias) on both the matrices, it is possible to assume the depletion depth to be the same. Moreover, the depth of the n-well diffusions in the substrate can be considered to be the same in both the matrices. Consequently, the vertical expansion can be considered to be the same in both cases while the lateral expansion of the depleted volume, which is lim-

ited by the shallow trench isolation, causes a different depleted volume. In particular, it results to be larger for the small electrode. The main consequence of the different depleted volume is a lower leakage current for the larger electrode due to a lower depleted volume. However, the difference in terms of volume is not that high to justify the difference in terms of leakage current. In fact, by considering the shape of the depleted volume to be half a sphere, the difference in terms of depleted volume for the different electrodes should be $\approx 100\mu m^3$ to compare with a total volume of a few thousands of cubic micrometers. The main reason of a different leakage current is the electric field near the collection electrode. In fact, in a real p-n junction the electric field lines density is higher at the junction borders, due to the curved shape of the junction. The high electric field causes usually a higher leakage current also before the junction breakdown. This effect is stronger for smaller area junction, which is the case of the previous described matrices. Finally, also possible differences in the surface generated charges could be a contribution to the different leakage current.

8.2 X-Ray Source

A typical step in the silicon sensor characterization is represented by the response of the detector when irradiated by X-rays. The intensity of a monoenergetic photons beam penetrating a layer of material is given by the well known law:

$$I = I_0 e^{-\left(\frac{\mu}{\rho}\right)x}$$

where I_0 is the incident intensity, μ/ρ is the mass attenuation coefficient for a given density ρ and x is the thickness defined as the mass per unit area (which is obtained by multiplying the real thickness t by the density ρ: $x = \rho t$). In Fig. 8.5, the silicon thickness reducing the incident energy of a factor e for different photon energies is shown; at low energy it is possible to see a sharp rise corresponding to the electron binding energy of the $1s$ orbital ($E = 1839\ keV$) in silicon. Since the binding energy in silicon is well known, it is possible to tune the X-Ray beam energy to a precise absorption edge. In solid state detectors, K and L levels are usually used: they allow to probe most of the elements by staying in an energy range between 5 and 35 keV. X-Rays with photons having that energies are usually called *hard X-Rays* and they are preferred to the so called *soft X-Rays*, having

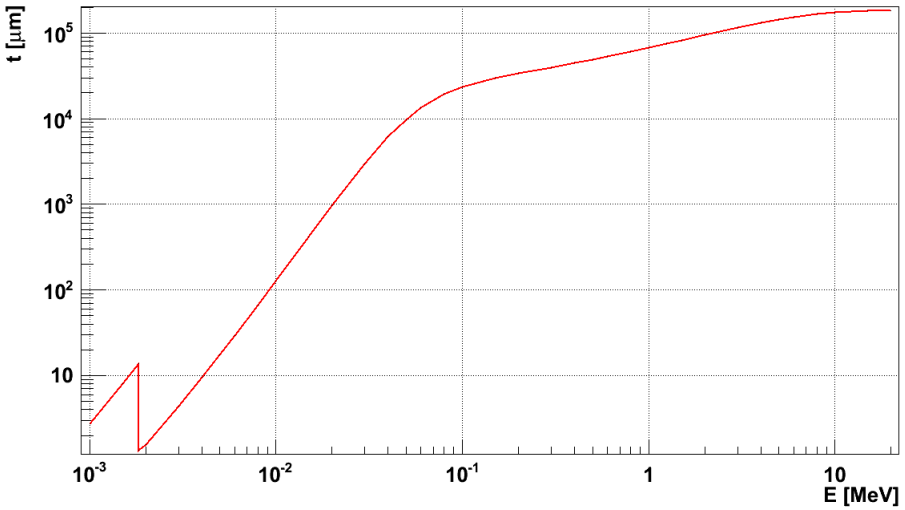

Figure 8.5: Photon penetration depth in silicon as a function of photon energy.

energy below $E \approx 5\ keV$, which are already easily absorbed in air or, more probably, by the layer placed over the silicon.
The X-Ray source used to test the performance of the LePix sensor has been Iron-55 (^{55}Fe), a radioactive isotope of iron which decays by electron capture to Manganese-55 (^{55}Mn); during the decay it can be emitted a $K_{1\alpha}$ line with energy of 5.889 keV (probability $\approx 16.2\%$), a $K_{2\alpha}$ line with energy of 5.888 keV (probability $\approx 8.2\%$) or a K_β line with energy of 6.49 keV (probability $\approx 2.85\%$). The energy of the K_α lines is so similar that they are usually referred as mono-energetic radiation with an energy around 5.9 keV. The energy released by the ^{55}Fe X-Rays excites electrons in the conduction band and the number of electrons excited is given by:

$$N = \frac{E_{X-Ray}}{E_{e-h}} = \frac{5.9\ keV}{3.6\ eV} \approx 1639$$

where E_{e-h} is the mean energy required to produce an electron-hole pair. However, the energy released by the incoming X-Ray is it not constant but it is subjected to statistical fluctuations by following the law:

$$< \Delta N^2 >= FN = F \cdot \frac{E_{X-Ray}}{E_{e-h}}$$

where F is the so called *Fano factor*. The theoretical determination of the Fano factor estabilishes it to be lower than 1 in semiconductor devices. However, an experimental determination of this quantity is difficult due to the several parameters influencing it (e.g. the device temperature).
It can be possible to see two main advantages of a X-ray source test: it allows to have a charge to ADC counts conversion factor and to determine the sensor charge resolution. In fact, by knowing the mean energy released by the X-Ray and the ADC counts at the output of the read-out electronics, it is possible to know how many electrons correspond to an ADC count. Moreover, the fluctuation around the mean energy released by the X-Ray, due mainly to the Fano factor, the noise of the device and possible mismatches from pixel to pixel allows to determine the best possible resolution of the semiconductor device.
In Fig. 8.6, the intensity decay law for a monoenergetic photon beam having about the same energy of the main energy line emitted by an ^{55}Fe source is shown: it is possible to see an intensity reduction of a factor e after about 30 μm in silicon. In a partially depleted device, such as MAPS devices and

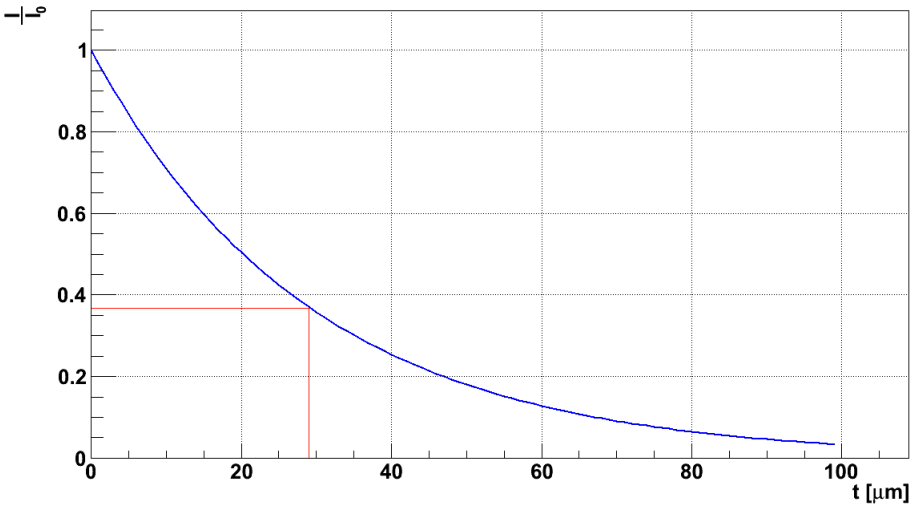

Figure 8.6: Intensity decay law for a soft X-ray beam having an energy of $E = 6\ keV$ traversing a silicon detector.

also LePix device, there are two possible scenarios: the X-Ray energy is released inside or outside the depleted region (Fig. 8.7). In the former case, the charge is collected by drift and the electric field of the depletion region

allows to maximize the charge collection on the electrode and, consequently, to maximize the voltage signal. In the latter case, the charges movement phenomena is due to diffusion (already described in the second chapter) which causes a large charge distribution width. Consequently only a fraction of electrons will reach the depletion region and will be detected (while the other will recombine): this fraction depends on the distance between the X-Ray energy release point and the depletion region (the nearer is the energy release point, the higher is the probability to have more electrons reaching the depletion region). In Fig. 8.8 it is possible to see the ^{55}Fe

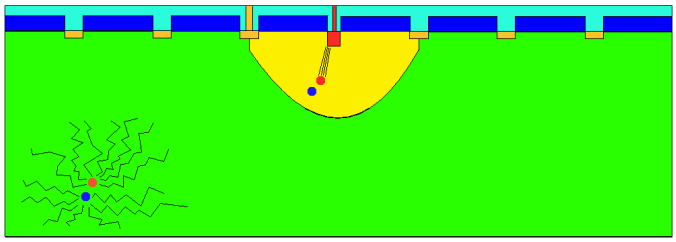

Figure 8.7: Simplified view of the two possible effects of an X-Ray in a p-substrate not fully depleted: if the charges are generated in the depletion region the electrons cloud (red) is moved by the electric field (drift) to the collection electrode while charges move by diffusion if generated outside the depletion region.

spectra for the four different sectors of the matrix having an active reset (the blue, green, yellow and red colours are respectively the first, second, third and fourth sector). They have been obtained by having a substrate bias $V_{sub} = -30\ V$, a polysilicon-metal bias $V_{poly-metal} = -30\ V$ and an integration time $t \approx 5\ \mu s$. The test has been done at room temperature. The pixel bias has been optimized to be in the best case for each sector. During the acquisition phase, a threshold cut on the pixel signal has been applied to avoid to acquire data due only to the noise. In Fig. 8.8 it is possible to see three different regions for each sector: at low ADC counts it is possible to see a peak due to the noise; for higher ADC counts, it is possible to see an almost flat distribution caused by the electron-hole pairs generated outside the depleted volume (only a fraction of those pairs will reach the depleted volume); finally it is possible to see a clear peak due to the main energy released by the source ($E_{X-Ray} \approx 5.9keV$) and a less clear second peak due to the K_β line with energy of 6.49 keV. The ADC counts for the peaks of each

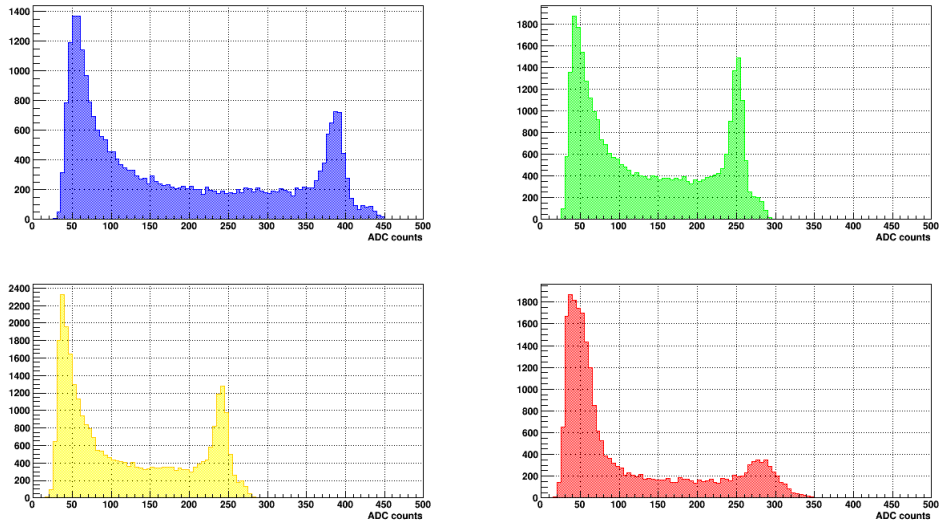

Figure 8.8: ^{55}Fe spectra for the different four sectors of the matrix.

sector correspond to the values expected from the capacitance values found by pulsing the input as described in the previous chapter. Moreover, it is possible to see similar results in the second sector and in the third sector, which have the same electrode size and the same input transistor size, while the first and the last sector, even by having a similar capacitance value, have different results, due to the different source follower gains. In Fig. 8.9 it is possible to better appreciate the two different peaks due to the ^{55}Fe in the first sector of the matrix. In Tab. 8.1 it is possible to see the ADC counts of the two different peaks of the ^{55}Fe and the peak resolutions obtained by biasing the pixels to obtain the best gain (which means $V_{dc-pulse} \approx 700\ mV$ for the first three sectors and $V_{dc-pulse} \approx 1\ V$ for the last sector). From

	E_1	ΔE_1	E_2	ΔE_2
Sector 1	386.3	11.8	426.6	10.5
Sector 2	250.3	8.9	276.0	7.8
Sector 3	240.8	9.0	265.8	7.2
Sector 4	285.3	20.2	315.3	10.6

Table 8.1: Peaks of the ^{55}Fe in ADC counts for the four different sectors of the matrix (the values are written in ADC counts).

the results obtained it is also possible to estimate the conversion factor from ADC counts to electrons of each sector (e.g. it is ≈ 4 for the first sector).

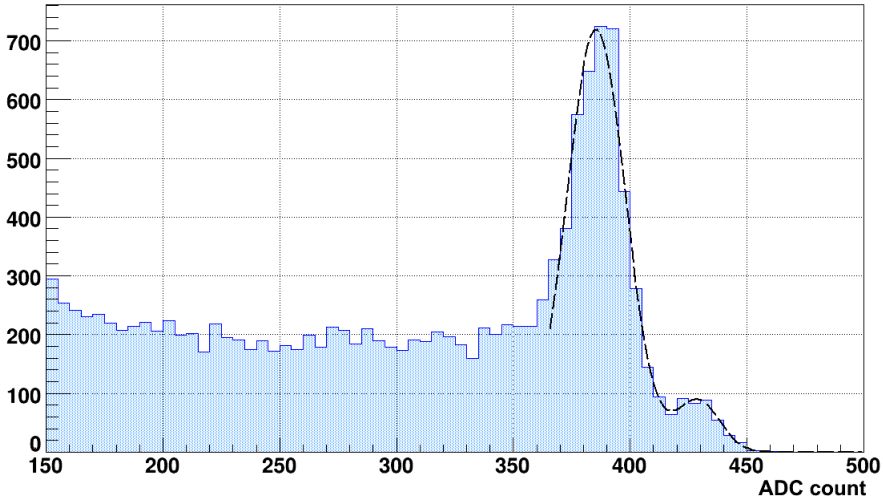

Figure 8.9: ^{55}Fe peaks for the first matrix sector.

Moreover, by knowing the conversion factor, it is also possible to evaluate the peak resolution of each sector: for example the first sector shows a resolution of $\approx 50\ e^-$ FHWM. Finally, the ADC values found for all sectors confirm the capacitances value measured by pulsing the input. In fact, by using the ADC peak value (for the 5.9 keV X-Ray) of the first sector, it is possible to write

$$S_1 = \frac{E_1 \cdot F_1}{G_{s.f.}} \approx 40\ mV$$

where S_1 is the signal at the input node of the front-end chain, E_1 is the peak value in ADC counts, F_1 is the conversion factor from ADC counts to mV at the output of the chip and $G_{s.f.}$ is the source follower gain. Consequently, it is possible to evaluate the capacitance at the input, given by:

$$C_1 = \frac{Q(5.9\ keV)}{40\ mV} \approx 6.5\ fF$$

which is the same value of the input capacitance evaluated by pulsing the input ($C \approx 5.5\ fF$) in parallel with the injecting capacitance ($C \approx 1\ fF$). In Fig. 8.10 it is possible to see the comparison between the seed and the cluster peak for the first sector of the matrix. The seed peak has been obtained by evaluating the signal of the pixel collecting most of the signal after the X-Ray hit; the cluster signal has been obtained by summing the

seed signal with the signal of the eight pixels surrounding the seed pixel. It is possible to see that the seed and the cluster peaks are almost the

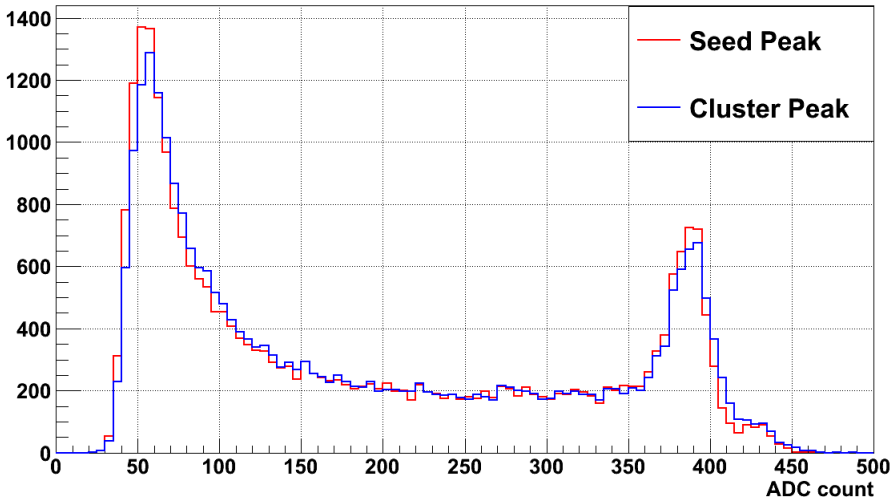

Figure 8.10: Seed and Cluster peaks for the first sector of the matrix.

same: this confirms that most of the charge is collected only by one pixel and there is no charge sharing between neighbor pixels. In fact, in a device having an uniform fully depleted volume, there are two different possibilities (Fig. 8.11): the pairs are generated exactly in the region underneath one pixel or the pairs are generated in the region in between different pixels. In the former case, all the charge is collected just by one pixel without charge sharing and the histogram of the seed peaks and the cluster peaks are the same. In the latter case, the charge is shared between neighboring pixels; consequently, the histogram of the cluster peaks (Fig. 8.12) will show only two regions: one peak at low ADC counts representing the noise and a second peak at high ADC counts due to the charges generated by the X-Ray. The main difference between the seed histogram and the cluster histogram should be the region in between the two peaks (the noise peak and the ^{55}Fe peak): it should not be present in the cluster histogram because all the charge is collected by neighboring pixels. For the same reason, the number of hits for the ^{55}Fe peaks should be higher in the cluster histogram.
The measurements have been also repeated for different biases of the pixels ($V_{dc-pulse}$) to see the effect of an X-Ray in the continuous reset part. In fact,

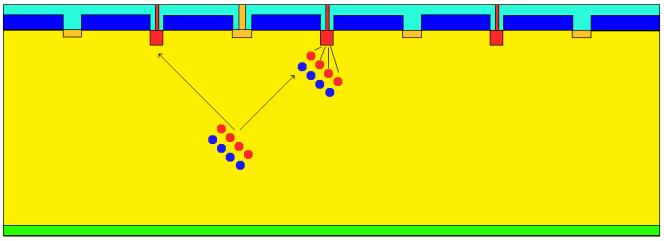

Figure 8.11: Simplified view of the two possible effects of a soft X-Ray in p-substrate depleted: the charge is collected by only one pixel, if generated exactly underneath the pixel, or by more pixels, if generated between more pixels.

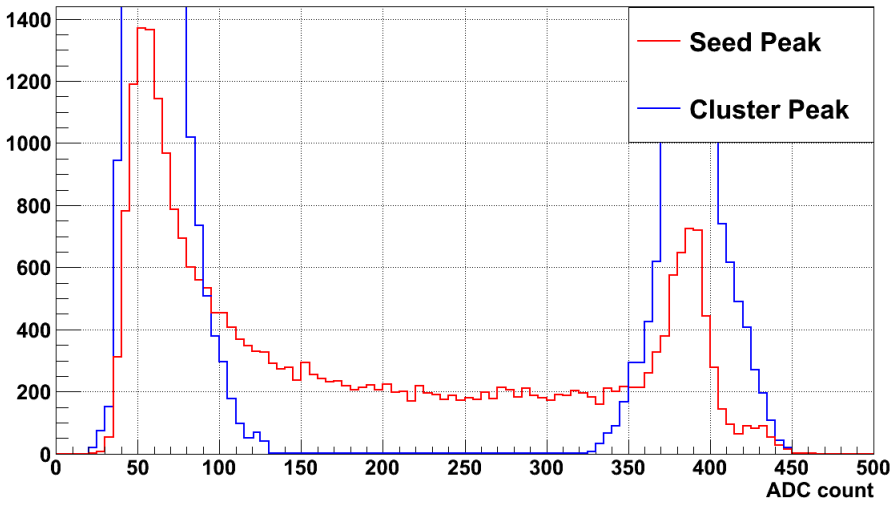

Figure 8.12: Possible scenario in terms of cluster peaks for a fully depleted device.

as already mentioned in the previous chapter, the front-end electronics of the continuous reset part needs a higher pixel voltage to be well polarized. The upper limit of the pixel bias is represented by the maximum voltage value allowed by the 90 nm technology ($V_{dd} = 1.2\ V$). The pixel bias has been increased from $V_{dc} \approx 700\ mV$ to $V_{dc} \approx 1.2\ V$. For each step, the position of the main ^{55}Fe peak (5.9 keV) has been evaluated for each sector and it has been compared with the position of that peak in the same sector having an active reset and a front-end electronics working in saturation (which means

$V_{dc} \approx 700\ mV$ for the PMOS sectors and $V_{dc} \approx 1\ V$ for the NMOS sector). The ratio between the peaks in the continuous reset part and in the active reset part for each sector are shown in Tab. 8.2. It is possible to see that,

$V_{dc-pulse}[mV]$	Sector 1	Sector 2	Sector 3	Sector 4
700	0.54	0.48	0.61	0.05
800	0.63	0.57	0.72	0.18
900	0.71	0.67	0.81	0.35
1000	0.84	0.78	0.94	0.58
1100	0.89	0.88	0.99	0.70
1200	0.93	0.92	1.00	0.85

Table 8.2: Peaks ratio between the continuous reset part and the active reset part for different $V_{dc-pulse}$ values in the continuous reset sectors.

even by using the highest pixel bias allowed by the 90 nm technology, it still remains too low to have all sectors having a continuous reset correctly polarized. In particular, only the front-end of third sector with continuous reset can be polarized to work in saturation at $V_{dc} \approx 1.2\ V$ and have the same peak position, in terms of ADC counts, of the active reset sector (see Fig. 8.13).

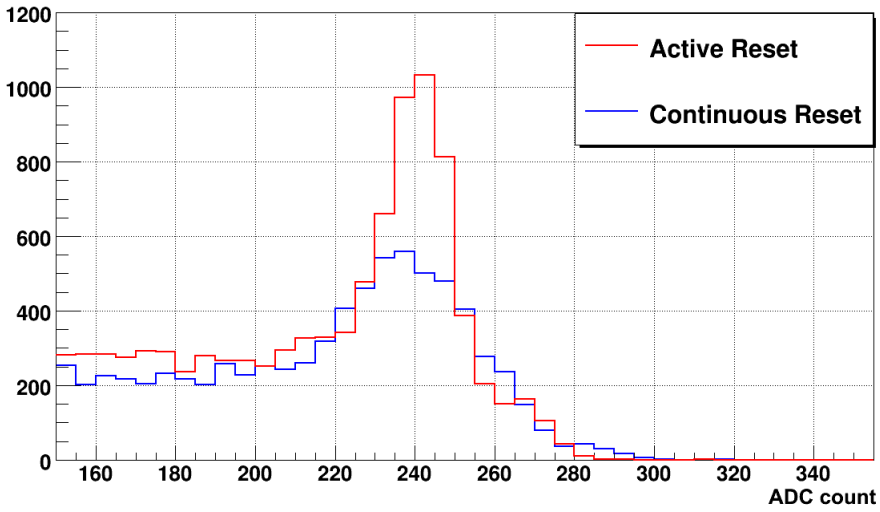

Figure 8.13: Comparison between the ^{55}Fe peaks of the third sector obtained by the active reset part ($V_{dc-pulse} \approx 700\ mV$) and the continuous reset part ($V_{dc-pulse} \approx 1.2\ V$)

8.3 Beam Test

A beam test allows to study the performance of a detector when traversed by particles, in such an environment for which it has been thought. Particles traversing a detector release energy through many scattering processes with electrons of the medium. The energy released creates electron-hole pairs and the charge produced is collected by the electrodes. The mean energy loss by moderately relativistic charged heavy particles is well described by the well known *Bethe-Bloch* formula ([42]). It has an accuracy of a few % in the region $0.1 \leq \beta\gamma \leq 1000$ for intermediate Z material. By knowing the energy lost by the impinging particle (dE/dx) and the ionization constant of the medium, it is possible to evaluate the number of electron-hole pairs generated in the medium (e.g.: in Fig. 8.14 the electron-hole pairs number generated in a 300 μm thick silicon detector for different impinging particles having different energy is shown). However, several corrections have to be applied on the

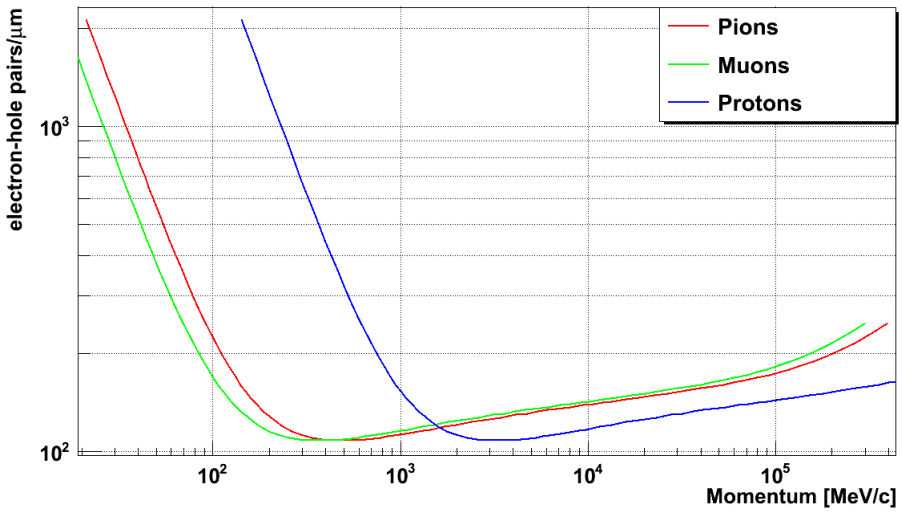

Figure 8.14: Electron-hole pairs generated by different particles in a 300 μm thick silicon detector.

Bethe-Bloch formula in the low and high energy range. In the low energy range, the velocity of the impinging particle is comparable to the atomic electrons velocity and the stopping power starts to depend on the projectile charge (the so called *Barkas effect*); for high energy radiative effects may

occur. In Fig. 8.15, the stopping power for positive muon, from the MeV to the TeV range, in copper is shown ([42]). The solid line represents the total stopping power, the dotted lines at low energy represents the Barkas effect, the brown line at high energy represents the Bethe Bloch formula with material density effect corrections (δ) while the celeste line without those corrections and the pink line the influence of the radiative effect correction; vertical lines show the transition between low energy, Bethe-Bloch and high energy regions. The ionization is also affected by statistical fluctuations and

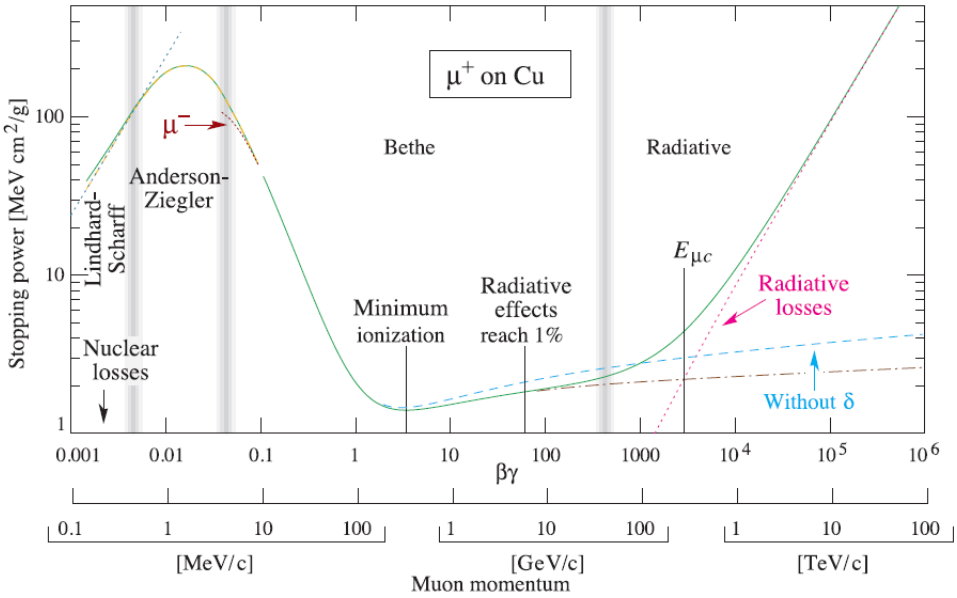

Figure 8.15: Stopping power for positive muon in copper with low energy and high energy correction to the Bethe Bloch formula ([42]).

the values returned by the Bethe-Bloch formula are the average value of the so called *Landau-Vavilov* (or *highly-skewed Landau*) distribution ([43], [44]). Since that distribution is not gaussian, the average value is different from the most probable value, which results to be lower than the average value. Moreover, the Bethe-Bloch formula does not depend on the medium thickness, which is the case of the Landau-Vavilov distribution. Finally, the Bethe-Bloch formula can be improved by applying medium density corrections, which are not included in the Landau-Vavilov distribution ([45]).

In Fig. 8.16, the stopping power for muons in silicon obtained by using the

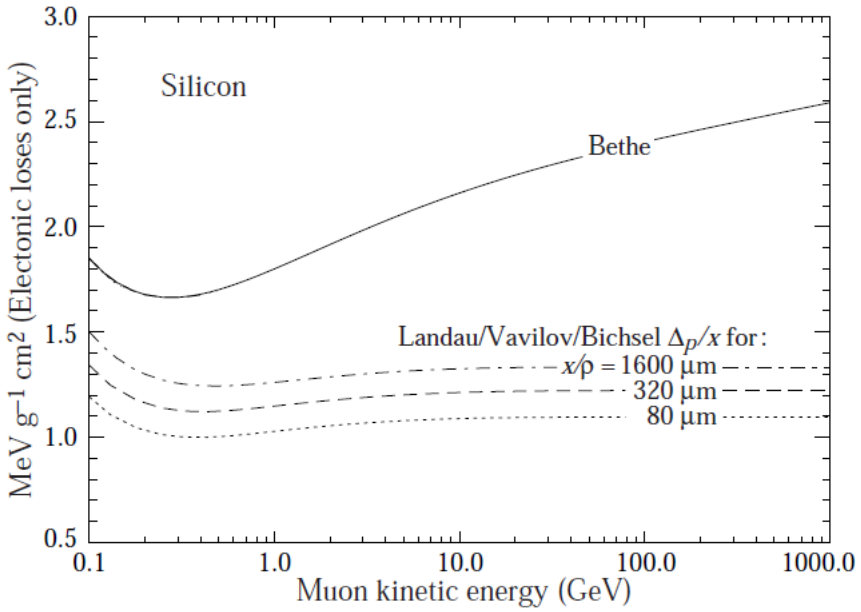

Figure 8.16: Stopping power for muons in silicon by using both the Bethe-Bloch formula and the Bethe-Bloch formula with thickness corrections ([42]).

Bethe-Bloch formula (with and without thickness corrections) is shown. The particle with a stopping power in the minimum of the Bethe-Bloch formula is usually called *minimum ionizing particle* (m.i.p.). If we suppose to have a m.i.p (by using only the Bethe-Bloch formula) in a 300 μm thick silicon detector, the number of electron-hole pairs per micron generated is around 110, while, by using the Landau-Vavilov-Bichsel corrections, it is around 80 (which is the most common value used).
During a beam test, beams having only minimum ionizing particles are typically used. Since the stopping power for thin silicon detector is almost constant for energy higher than a m.i.p., the range from a few hundreds of MeV to a few hundreds of GeV can be used.
Two different beam tests have been done with the LePix matrix: both have been done with pions beams with two different energies (≈ 300 MeV in the first case, ≈ 300 GeV in the second one). Even if the partially depleted substrate does not allow to have a 100% efficiency, it is interesting to study the performance of the sensor when traversed by charged particles.

The first beam test has been performed at the *PiM1* line at PSI, containing mainly high momentum pions ($\approx 300 MeV$) and spuria protons and electrons. A four plane telescope has been set to have a rudimental tracker set-up (Fig. 8.17). The four planes have been connected by ERNI con-

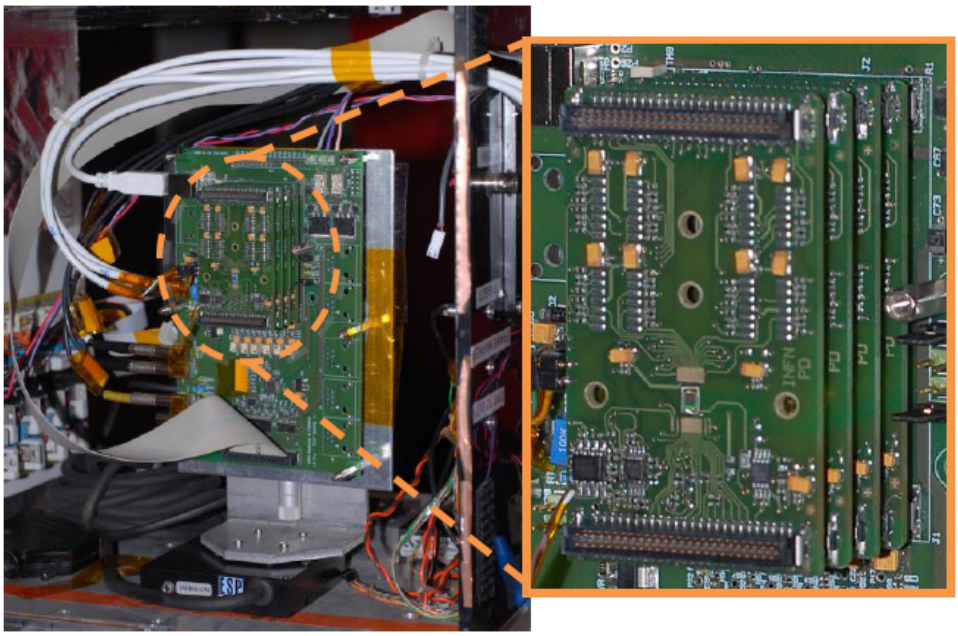

Figure 8.17: Four plane telescope assembled using electrical connectors.

nectors: this approch does not allow to have a micron-level alignment but represents an acceptable compromise in term of performance-time spent in the assembly phase.
Due to a set-up limitation, only the first two sectors for each plane have been optimized in terms of performance.
As already mentioned in the previous chapters, the LePix matrix works in two phases: during the first one (acquisition), the reset signal is sent to the pixel and the effects due to an impinging particle occurred during the integration time are stored in the storing capacitances; during the second phase, the matrix is serially read starting from the first pixel of the first sector and proceeding pixel-by-pixel column-by-column. Since the clock frequency of the system has been set at $f = 390\ kHz$, the read-out phase duration is forced to be $\approx 5.25\ ms$. The integration time is strictly related

to the substrate voltage, which determines the maximum integration time useable before having the p-n junction of the reset transistor forward biased (see the previous chapter for a deeper explanation); consequently, even by pushing the integration time to be around 200 μs, the integration time represents only a small percent (between 3% and 4%) of the total period (acquisition phase and read-out phase) of the matrix. This issue represents a strong limitation in term of statistics.
The results obtained by the off-line analysis of the detector performance can be described in terms of charge generated, collection efficiency and multiplicity.
The energy released in the medium by a m.i.p. is given by the Landau distribution. Consequently, also the number of electron-hole pairs generated and the output signal amplitude follow the Landau distribution. By evaluating the most probable value of the Landau distribution, it should be possible to obtain the number of electrons generated and, consequently, the depleted layer crossed by the impinging particle. In Fig. 8.18 it is possible to see the Landau curve for the first sector of the matrix obtained for a reverse substrate bias of $V_{sub} = -30\ V$. The signal in ADC counts has

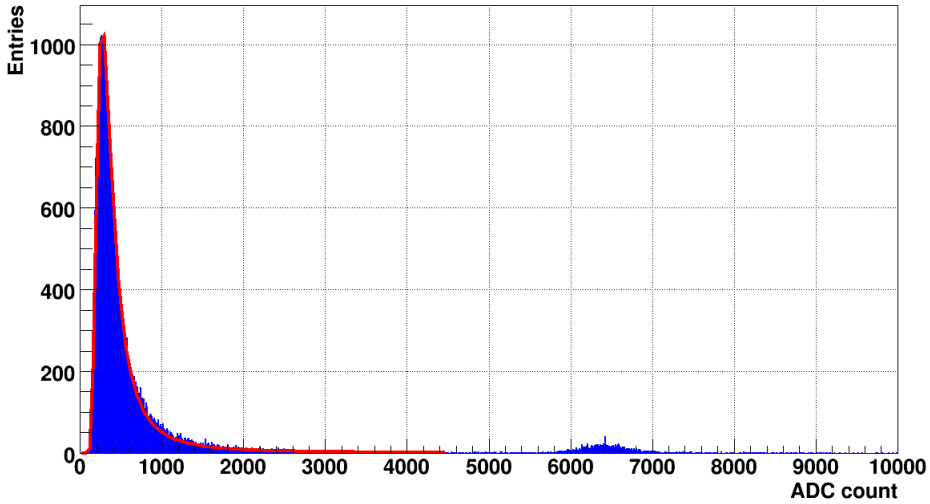

Figure 8.18: Landau curve for the first sector of the matrix.

been obtained as follows: the software is set to save a pixel ADC value only when a certain threshold is overcome; consequently, as soon as a particle

hits a pixel and the pixel signal overcomes the threshold, not only its value is saved but also the values of all pixels forming a small 5×5 matrix having the hit pixel in the center are saved. Only the ADC counts of a sub-matrix of 3×3 pixels having as center the hit pixel are summed to obtained the ADC value shown in the plot. Two different peaks are clearly visible: the first one due to pions (lower ADC counts) and the second one due to protons (higher ADC counts). By knowing the conversion factor (from ADC counts to electrons) and the most probable value of the Landau distribution, it is possible to evaluate the depletion region depth. For both the first and the second sector, the depletion region depth is lower than 20 μm. However, the irregular shape of the depletion layer has to be taken into account (it is not continuosly 20 μm thick over the whole matrix). Since the depleted layer extends only under the electrode, but not in the region between electrodes, it can be affirmed that only a small fraction of the substrate volume is ≈ 20 μm depleted. Consequently, it can be hypothesized that most of the charge is generated outside a depleted volume and only a fraction of them reaches by diffusion the depleted volume to be collected by the electrode by a drift mechanism. Moreover, it has been noticed an almost constant value of the Landau peak for different substrate values in a range between $V_{sub} = -20$ V and $V_{sub} = -60$ V. In principle, by having a more and more negative substrate bias, the Landau peak should shift towards higher ADC counts. In fact, in a substrate having a uniform depletion, the depletion depth is proportional to the square root of the bias applied to the substrate (using a planar and abrupt junction approximation). Consequently, by increasing the ΔV applied to the junction, it is possible to increase the depleted volume and the number of charges collected by the electrode when a charge particle passes through the detector, having a shift of the Landau peak. However, in the LePix matrix case, it has to be considered the shape of the depletion layer: the small size of the collecting electrode causes a spherical-shaped depleted volume (see chapter 3) having a depletion depth proportional to the cubic root of the substrate bias (consequently, not large differences can be noticed by working in a substrate voltage range between $V_{sub} = -20$ V and $V_{sub} = -60$ V). Moreover, it has to been taken into account the effect of the field plates which strongly affect the depletion shape. The irregular shape of the depleted volume strongly influences also the charge collection efficiency. In fact, due to the non depleted volume in

the region in between two pixels, it is not possible to have a 100% fill factor. This limitation is shown in Fig. 8.19. The signal generated by an impinging particle can be used to evaluate the crossing position by using a charge center of gravity approach: the signals coming from a group of pixels are used to establish the impinging particle crossing point. In Fig. 8.19 and

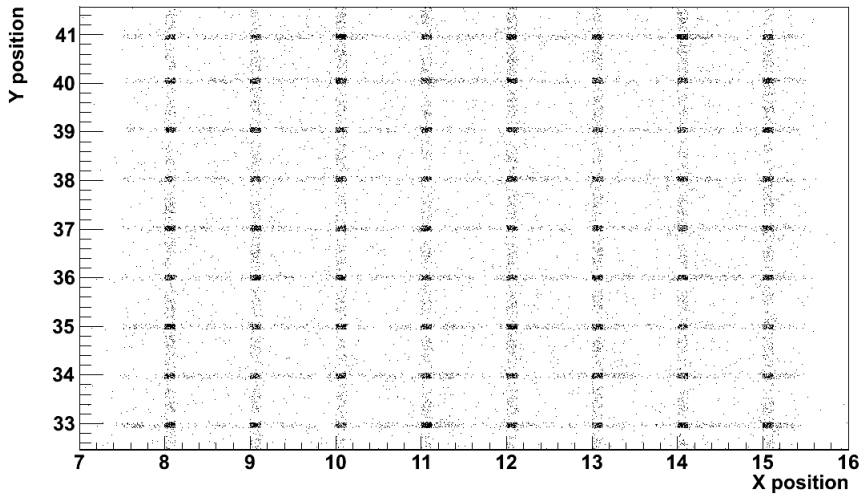

Figure 8.19: X-Y distribution of the charge generated by a particle for a region of the second sector of the matrix.

Fig. 8.20 it is possible to see that most of the charge is collected in the center of the pixel while there is almost no charge in the region in between four pixels. The efficiency of the detector has been evaluated to be slightly lower than 70%. However, even with that low efficiency, it has been possible to see pions passing through the four layers, as shown in Fig.8.21. Even if the substrate bias has a negligible influence on the depleted volume, it has a strong impact in terms of multiplicity. The multiplicity can be defined as the number of pixels per impinging particle which overcome a fixed threshold (in Fig. 8.22 the number of pixels overcoming the threshold for proton hits with a small substrate bias applied). As already mentioned in chapter 1 and chapter 2, the charge collection dominated by drift yields smaller cluster sizes than charge collection dominated by diffusion. When no bias is applied to the substrate, the charge collection mechanism is dominated by diffusion while it is dominated by drift when a reverse bias is applied to the substrate.

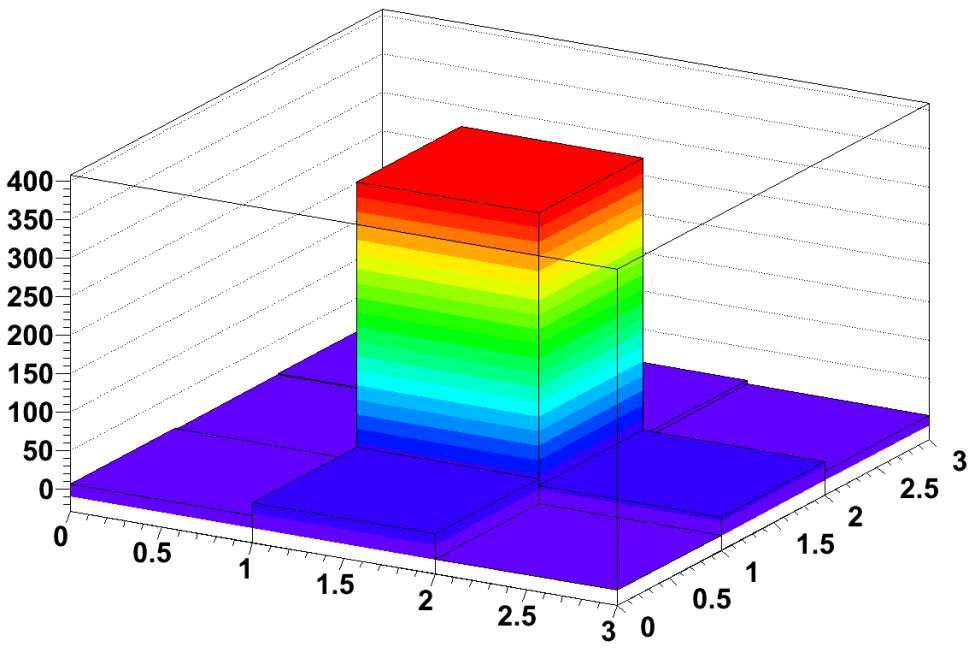

Figure 8.20: Typical hit event with the coordinates (X-Y) and the ADC counts (Z) which shows the charge collected by only one pixel.

In Fig. 8.23 and Fig. 8.24 it is possible to see the influence of the substrate bias for the multiplicity of both pions and protons. The substrate bias is particularly influent in the proton case, when a high number of electron-hole pairs is created.

A second beam test with $\approx$ 300 GeV pions has been done. Pixels bias values have been optimized to have all PMOS sectors correctly polarized and to have the possibility to increase the statistics (because of the higher number of working sectors). However, also in this case the results obtained during the first beam test in terms of charge collection efficiency have been confirmed. Several trials have been done to find an acceptable compromise between the metal-polysilicon bias value and detector performance obtaining no remarkable results.

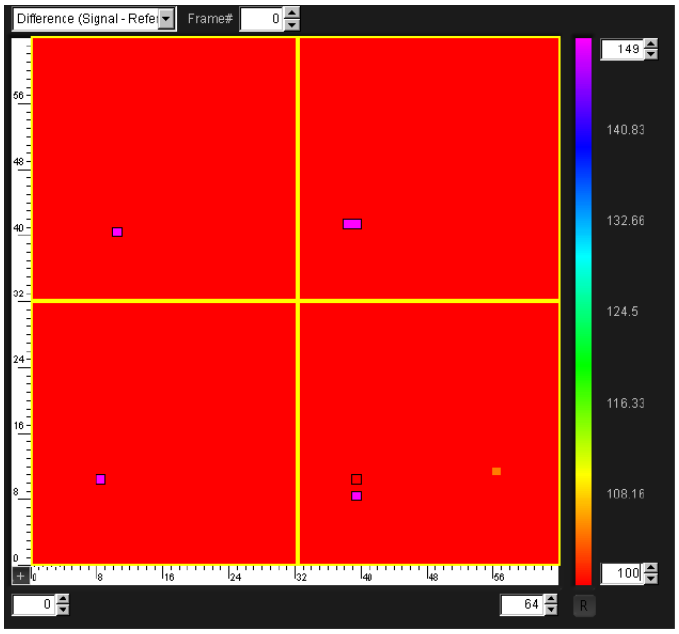

Figure 8.21: Pion track through the telescope. The XY plot shows the first plane in the top left corner, and the other planes in counter clockwise direction.

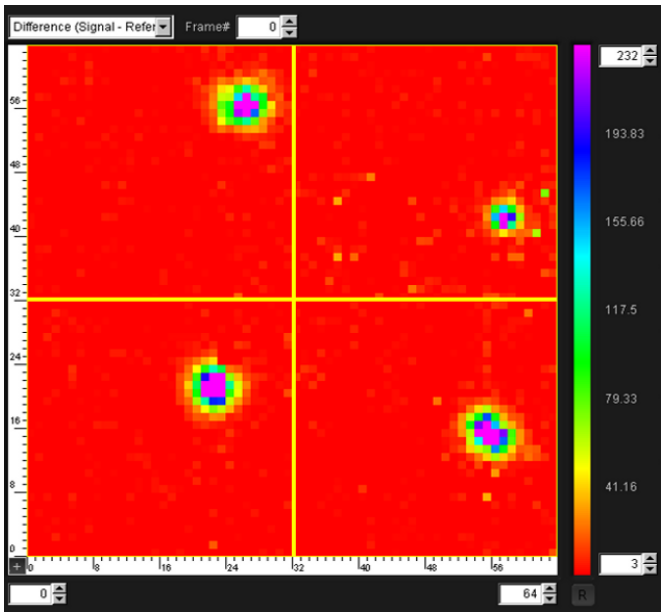

Figure 8.22: Proton track through the telescope for a substrate bias of $|V_{sub}| = 2V$.

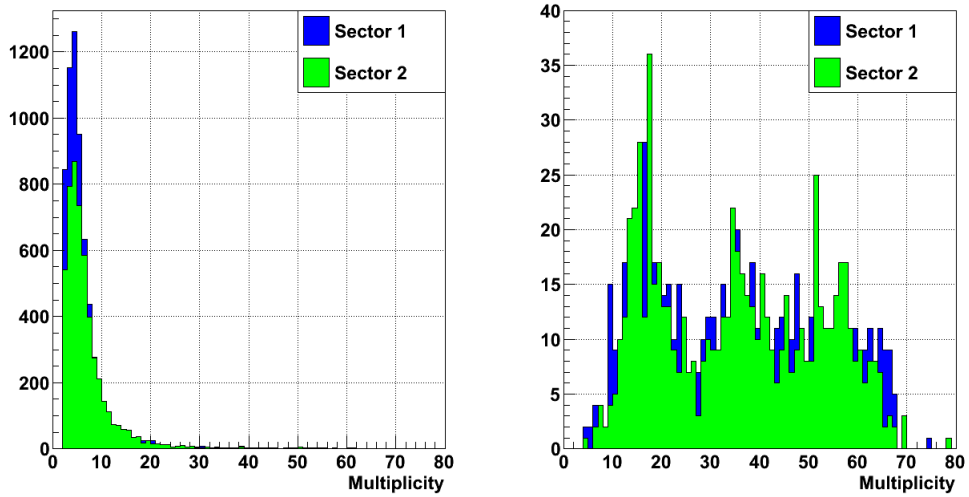

Figure 8.23: Multiplicity for pions (left) and protons (right) when a zero bias is applied to the substrate.

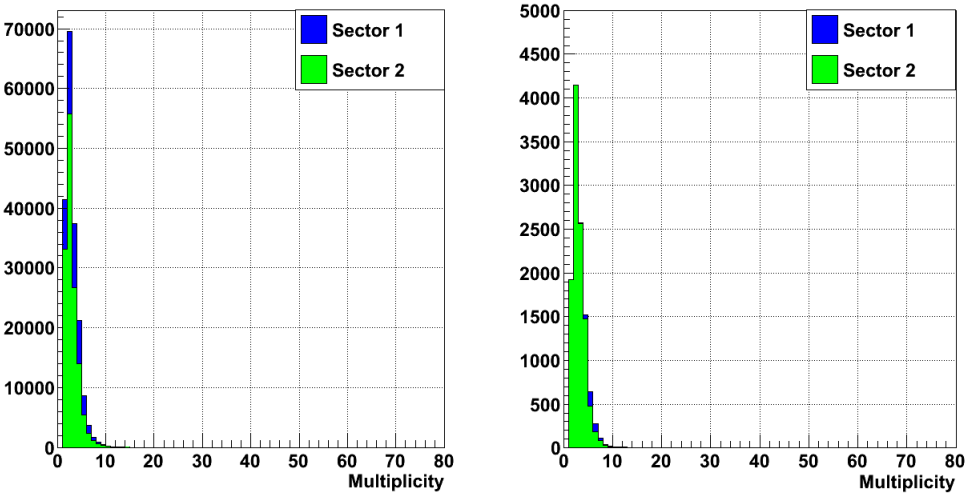

Figure 8.24: Multiplicity for pions (left) and protons (right) when the bias is polarized with $V_{sub} = -60\ V$.

8.4 Conclusions

After the charge collection measurements it is possible to make two interesting conclusions. The first one is based on the shape of the depleted

volume, which is not uniform but it is mainly confined in the region underneath the electrode. This is due to the strong negative bias applied on the polysilicon contact (forced to be strongly negative due to the short with the metal contact) which does not allow a correct expansion of the electric field. Consequently, the region between pixels is not depleted. The situation is also aggravated by the large pixel pitch ($\approx 50\ \mu m$) which increases the loss of the charge generated between pixels. It is confirmed by the laser test, which clearly shows the shape of the depleted volume based on the charge collected by moving the laser spot, by the ^{55}Fe measurements, where the peaks of the seed and the peaks of the clusters are almost the same, and by the beam tests, where the impinging particle crossing point reconstructed by applying the center of gravity methods shows no charge collected in the region between pixels. This issue represents a strong limitation of the device because it does not allow to have full efficiency. The second conclusion is based on the influence of the substrate bias. In fact, it can be assumed that a fraction of charge is collected by drift and it is confirmed by both the laser test, where the signal collected is higher for more negative substrate, and the beam tests, where the multiplicity is lower for more negative substrate. Finally, despite the efficiency issue, the ^{55}Fe spectrum obtained illustrates the potential of the technology in terms of sensitivity and signal to noise ratio: both the 5.9 keV and the 6.49 keV peaks are clearly visible and the spread of the peak measured at room temperature is around 50 electrons FWHM, in good agreement with the electrical noise value measured at the same integration time.

Chapter 9

Radiation Hardness

In this chapter, the effects of the radiation induced damage on the LePix structures (in particular, the diode structure and the matrix) will be shown. First radiation damage in silicon devices will be briefly introduced and then measurements and performance of irradiated LePix structures will be described.

9.1 Radiation Damage

The radiation damage effects are divided into *bulk damage* and *surface damage*. The former are more influential in the sensitive part of the detector while the latter are more influential in the detector part hosting the electronics. The effects of surface damage on the circuitry can be divided into *cumulative effects* (total ionizing damage) and *single event effects* (single event upset and single event transient). In this context, only the cumulative effects will be treated.
The bulk damage is due to massive particles crossing the device. They lose energy producing electron-hole pairs but they also interact with atoms: a particle hitting an atom can move it out from its initial position in the lattice producing a *Frenkel pair* (interstitial and left-over vacancy). The atom can release its energy (in the best case, up to a 1000 Å range) producing new displaced atoms and causing negligible ionizing effects. The final result can be a dense agglomeration of defects called *cluster*. The gravity of the damage depends on the impinging particle and its energy. For example, the energy required by an electron to remove an atom from its lattice position is

$E \approx 260\ keV$ while a proton and a neutron, which are more massive, need only an energy $E \approx 190\ eV$; the energy required by a neutron to produce clusters is much higher ($E \approx 35\ keV$). To be able to compare the damage caused by different particles on the lattice is used the *Non Ionizing Energy Loss* (NIEL) scale method: the fluence Φ_{eq} taken into account is the equivalent fluence of 1 MeV neutrons causing the same damage of the particles hitting the device. As already mentioned, this type of damage is more influential in the sensitive part of the detector, where a regular structure of the lattice is required to have high performance in terms of charge collection, depletion depth and leakage current, while it is less influential in the oxide, which has already an irregular structure.
Once the defect is produced in the lattice it can both annihilate without causing further damage or remain in the lattice causing a macroscopic deterioration of the detector properties. In fact, due to displacements of atoms from their initial position, trap levels are produced in the band gap; traps are excellent electron-hole pairs generation centers. Consequently, the generation lifetime decreases, the leakage current and the noise due to the leakage current increase proportionally to the fluence. The other main effect due to the charge trapping in the trap levels is the variation of the effective doping level N_{eff}. The consequences are a variation of the depletion region depth (see equation 1.2) and a variation of the silicon resistivity. Finally, the presence of traps in the band gap reduces also the charge collection efficiency. In fact, most of the traps are unoccupied in the depletion region, due to the lack of free charge carriers. Consequently, the charges generated by an impinging particle can be trapped; if the detrapping time is higher than the charge collection time, the trapped charges cannot reach the electrode causing a lower signal.
The *surface damage* are caused by ionizing radiations which produce problems in the silicon-dielectric surfaces. They represent a strong constraint for an Integrated Circuit which has to be optimized during the design phase to be able to reach the required performance also in a high radiation dose environment. The CMOS structures are almost insensitive to the displacement damage. In fact, the oxide is not affected by displacement damage because it has not a well defined lattice structure; the conduction mechanism is not also affected because the conduction region placed below the silicon-oxide interface does not extend deep in the bulk and the damage in such a small

volume can be considered negligible. The CMOS structures are more sensitive to ionization than to displacement damage. The most sensitive part of a CMOS structure to ionizing radiation is the oxide insulator. There are four major processes which contribute to the response of a MOS device (Fig. 9.1). In fact, a radiation crossing the oxide produces electron-holes pairs (first process). Electrons are swept out of the oxide in a few picoseconds because of the positive voltage usually applied on the gate and their high mobility. In this time, some fraction of electrons and holes will recombine. The remaining holes can both remain near their point of generation, causing a threshold voltage shift in the transistor, or move towards the silicon-oxide interface, causing a recovery of the initial threshold voltage (second process). The third process is due to the holes which reach the silicon-oxide interface falling in the trap states and causing a voltage shift which persists until a gradual annealing. Finally, an increase of the interface traps after irradiation has been observed: in fact, on the silicon-oxide interface the Si-atom is left with a dangling bond as an active defect as soon as one of its bond is broken. The threshold voltage shift occurring after irradiation in a

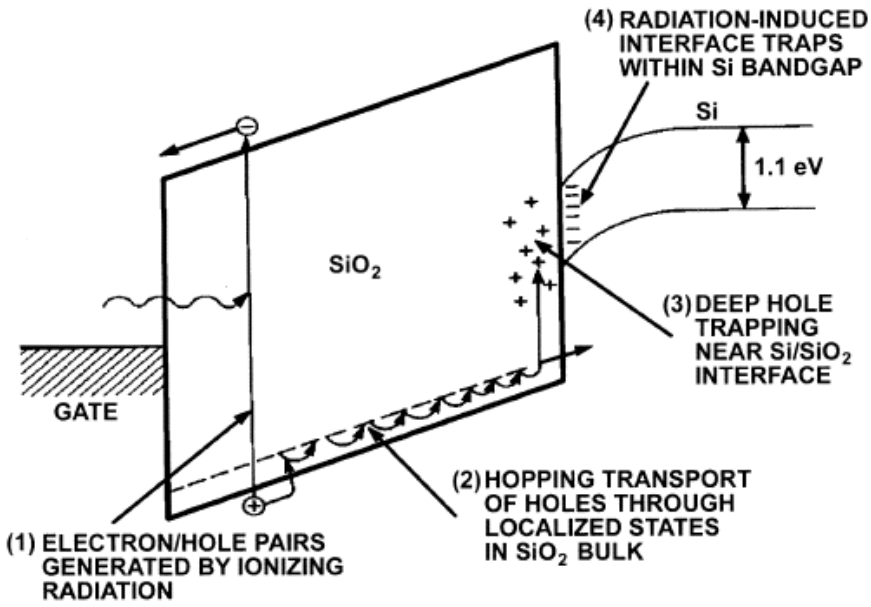

Figure 9.1: Schematic view of the main processes after ionizing irradiation ([11]).

MOS transistor is given by the sum of two contributions: the holes trapped

in the oxide and the charges trapped on the interface. The effect of the holes trapped in the oxide depends on the CMOS transistor type. In fact, in a NMOS transistor, the trapped holes attract electrons on the silicon-oxide interface easing the channel production and reducing the threshold voltage; vice-versa, in a PMOS structure, the trapped holes repel the holes in the channel. This effect (electrons attraction or holes repulsion) strongly depends on the position of the trapped holes in the oxide: the closer are the charges on the silicon-oxide interface, the bigger is the threshold voltage shift. The charges trapped in the interface also cause similar effects. In fact, in a NMOS structure the negatively charged traps cause a positive shift of the threshold voltage; vice-versa, in a PMOS structure the positively charged traps cause a negative threshold shift (in absolute value, the shift is positive both for the NMOS and the PMOS transistor). The threshold shift is tightly connected to the technology used. In fact, for a submicron technology (oxide thickness larger than 10 nm), the shift due to the holes trapped in the oxide is more influential than the shift due to the charge on the interface but for a very deep submicron technology the two contributes can be of the same order of magnitude.
The threshold voltage shift affects also the subthreshold current, having interesting effects in particular on the NMOS structures. In fact, in a MOS structure biased below the threshold voltage, a subthreshold current flows between the source and the drain. As soon as a negative threshold shift occurs, the current for fixed bias conditions increases. Another contribution to the parasitic current for irradiated transistor is given by the current path created under the so called *bird's beak region* (Fig. 9.2). These regions are due to the field oxide used to insulate devices. In fact, parasitic paths are produced in the oxide region causing parasitic transistors. The threshold of the parasitic transistors could be of the order of several volts, due to the thick oxide, but also the shift during irradiation could be of several volts. Consequently, the current flowing in the device could increase depending on the dose and the type of oxide (Fig. 9.3). In very deep submicron technology, the isolation is made by shallow-trench isolation (STI) but this new isolation does not eliminate the post irradiation parasitic paths.

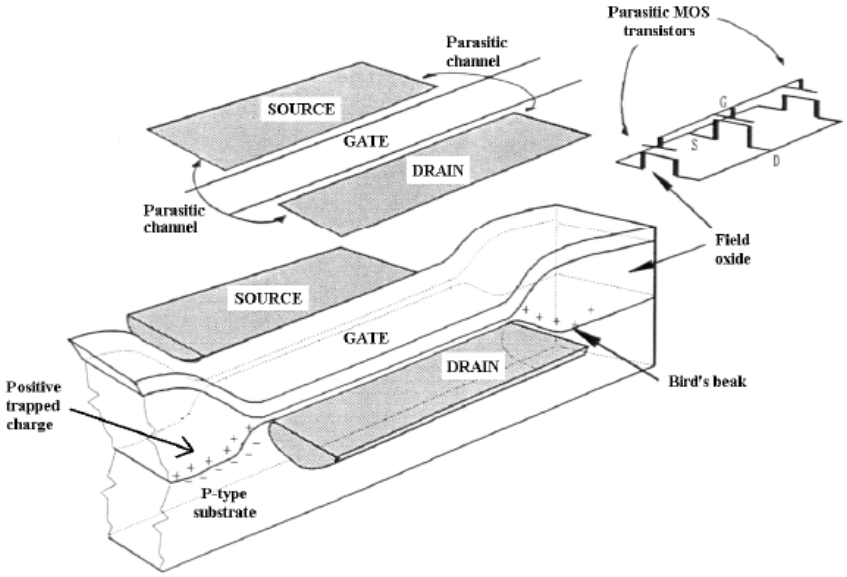

Figure 9.2: Schematic view of the parasitic transistors in the bird's beak region ([47]).

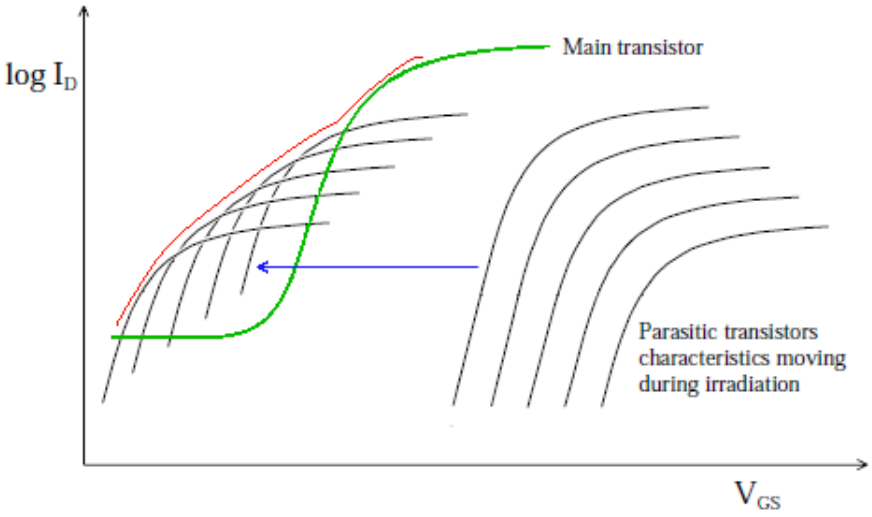

Figure 9.3: Qualitative plot of the parasitic current flowing in the device shown on Fig. 9.2 ([47]): before irradiation there are only the main current (green) and, for high V_{gs}, some parasitic currents (black); after irradiation, a several volts threshold shift occurs for the parasitic transistors increasing the current in the device (red).

9.2 Diode Radiation Hardness

The diode structure has been already described in detail in the fourth chapter. It is based on a n-well placed on a p-substrate and surrounded by a guard-ring. Since there is not a front-end electronics placed in the structure, only the radiation hardness based on the bulk damage has been tested.
Irradiations have been carried out at the neutron irradiation facility in Ljubljana, with fluencies between $10^{12}\ n(1\ MeV)/cm^2$ and $2{\cdot}10^{15}\ n(1\ MeV)/cm^2$. After the irradiations, the irradiated samples have been transported to CERN in a cooled box. Before being tested, they spent about one hour at room temperature to have the routine safety test and about half an hour to be glued on the PCB support and to be bonded. Consequently, it can be assumed that, even if a minimal annealing has been possible, the treatment for all samples has been the same, causing the same effects in the irradiated diodes. The samples have been stored in a fridge at a temperature $T = -20^oC$, to minimize the annealing effects.
The main measurements done on non-irradiated samples ($I-V$ and $C-V$) have been repeated also on irradiated samples: the experimental set-up and the biases have been the same. In fig. 9.4 it is possible to see the effects of the irradiation on the leakage current. The range has been limited to

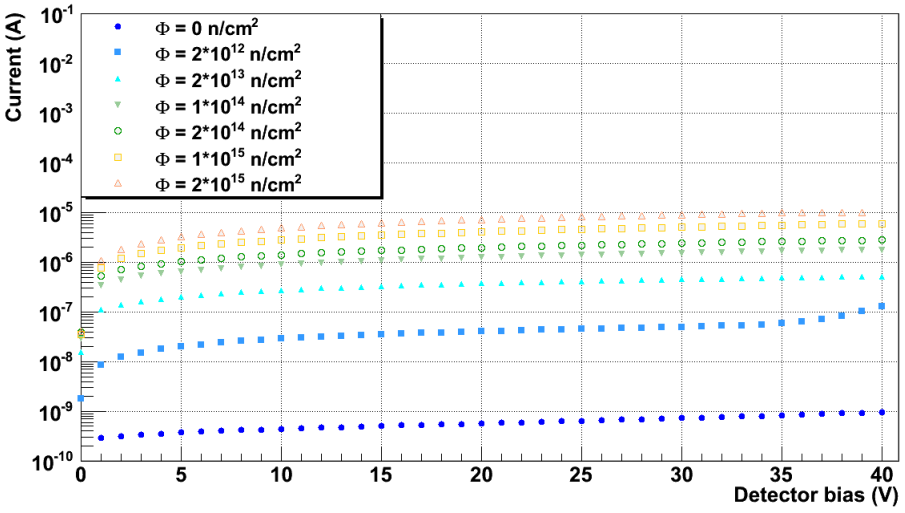

Figure 9.4: $I-V$ characteristic for irradiated samples (the substrate has to be considered to be negatively biased).

$|V_{sub}| \leq 40\ V$ to avoid the parasitic current coming from the edge. Due to its exponential dependence on the temperature, the leakage current has been normalized to a reference temperature of $T_R = 20^oC$ following [5]:

$$I(T_R) = I(T) \cdot \left(\frac{T_R}{T}\right)^2 exp\left[-\left(\frac{E_g}{2k_b}\right) \cdot \left(\frac{1}{T_R} - \frac{1}{T}\right)\right]$$

where $I(T)$ is the measured current, E_g is the energy band-gap in silicon and k_b is the Boltzmann constant. The temperature has been measured by using a thermistor placed on the PCB hosting the device. The measurements show a strong increase of the leakage current up to four orders of magnitude for the highest fluence.

Also measurements to evaluate the capacitance of the irradiated samples have been done. However, it has to be remarked that the capacitance measurements are based on pulsed voltage signals applied on the sensor used to measure the current variations and the phase angle between the voltage and the current. As already mentioned in the previous section, one effect of the neutron irradiation is the creation of traps in the energy band-gap. Usually, the traps capture charges to release them after a certain detrapping-time. If the detrapping-time is higher than the pulsing-time, some trapped charges could not reach the electrode in time, giving no-contribute to the measured current. However, the frequency used to pulse the signal ($f = 10\ kHz$) can give a realistic value of the detector capacitance. In Fig. 9.5, the capacitance measurement results are shown. Also in this case, the substrate voltage has been limited to $|V_{sub}| \leq 40\ V$. Moreover, the capacitance value measured for low substrate voltage (in absolute value) can be considered negligible, due to the pulse height comparable with the substrate voltage. For substrate voltage $|V_{sub}| \geq 10\ V$, it can be seen that for fluencies up to $2 \cdot 10^{13}\ n/cm^2$ the capacitance changes less than 1 pF, while it increases up to a few pF for higher fluencies.

By supposing a planar and abrupt junction, it is also possible to estimate both the depleted volume and doping level. In Fig. 9.6 it is possible to see the doping level at different depletion depths for difference fluence values. Also in this case, it can be seen an almost constant doping level for fluencies up to $2 \cdot 10^{13}\ n/cm^2$ while for higher fluencies, the doping level increase does not allow the depletion region to extend deeply in the substrate (it has to be reminded that the depletion depth is proportional to the square root of the

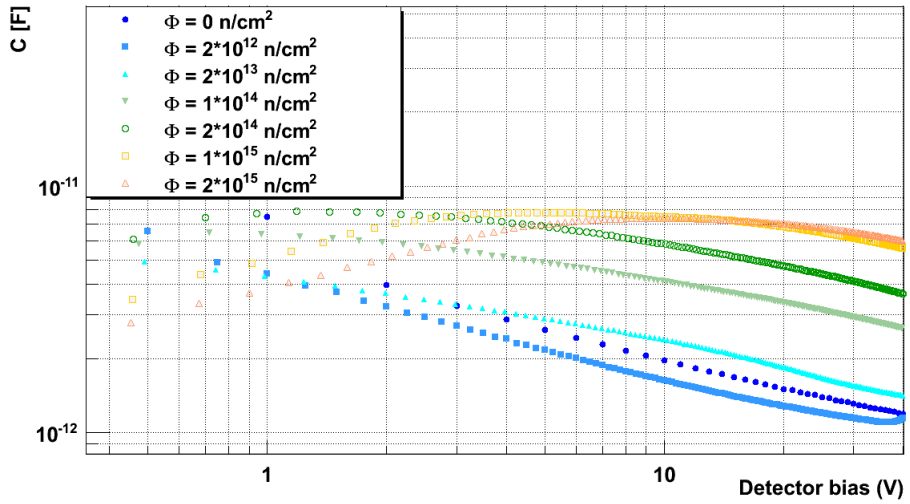

Figure 9.5: $C - V$ characteristic for irradiated samples (the substrate has to be considered to be negatively biased).

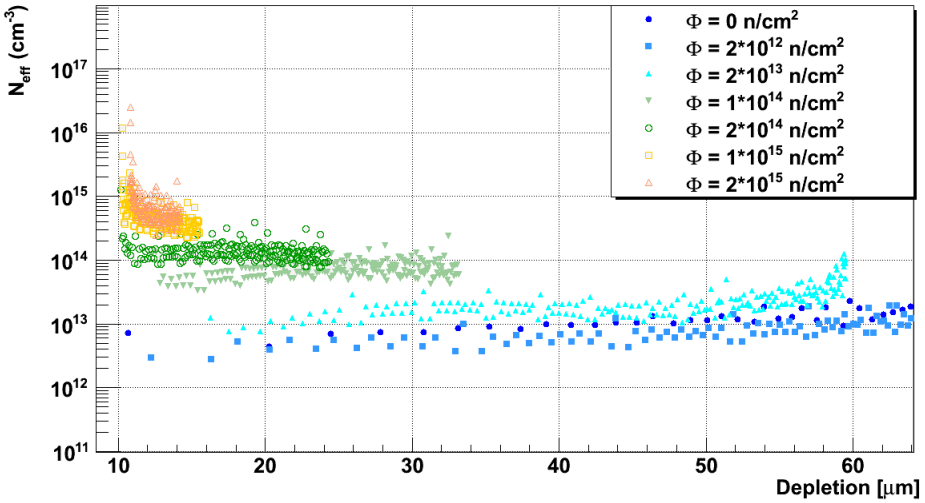

Figure 9.6: Doping level at different depletion depth for different fluencies.

inverse of the effective doping level). It can also be seen from the volume point of view (Fig. 9.7): for low fluencies, the depleted volume is almost constant, while for larger fluencies it is reduced.
Both the leakage current and the depleted volume are typically used to de-

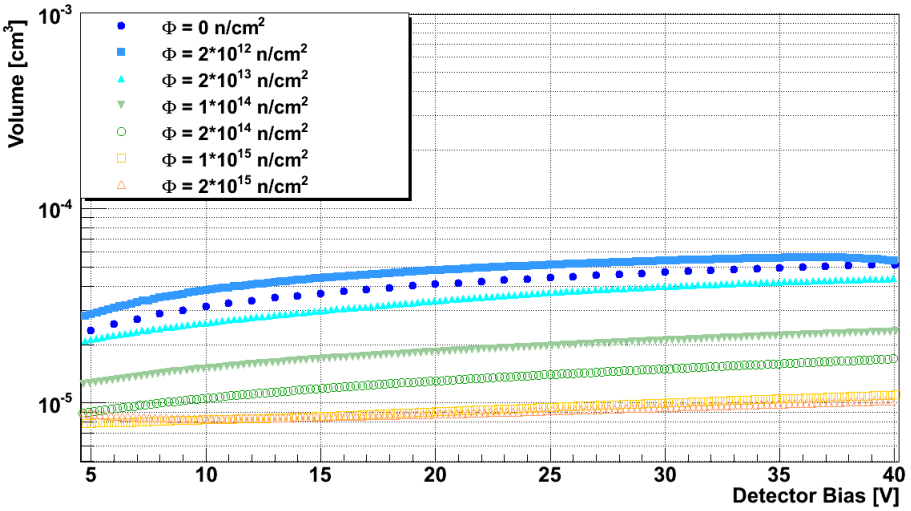

Figure 9.7: Depleted volume for different bias values applied on the substrate and for different fluencies (the substrate has to be considered to be negatively biased).

termine the so-called *current related damage rate* (α). In fact, in standard silicon detector, the measured increase in current is proportional to the fluence, following the equation:

$$\Delta I = \alpha \Phi V$$

where ΔI is the current increase, Φ is the equivalent fluence and V is the depleted volume. The current is usually measured after a heat treatment (80 min at 60^o). Moreover, the current is measured for a fully depleted device. In the LePix diode, the evaluation of the current related damage rate is not possible by following that approach. In fact, as already explained in the fourth chapter, the sensor is not fully depleted: a large leakage current coming from the edge does not allow to obtain realistic capacitance values. Moreover, for devices irradiated above $\Phi \geq 1 \cdot 10^{14}\ n/cm^2$ the leakage current flowing for $|V_{sub}| \geq 40\ V$ is large enough to have low accuracy in the capacitance measurements. However, it is possible to evaluate the current density variations for a fixed volume at different fluence values. It is shown in Fig. 9.8, where three different volumes have been taken as reference and the current per unit volume variations have been evaluated. It has not been

possible to use depleted volume values higher than $V = 0.03\ mm^3$, which is already a border line value in terms of leakage current flowing in the diode. By fitting the data with a linear fit, it has been possible possible to esti-

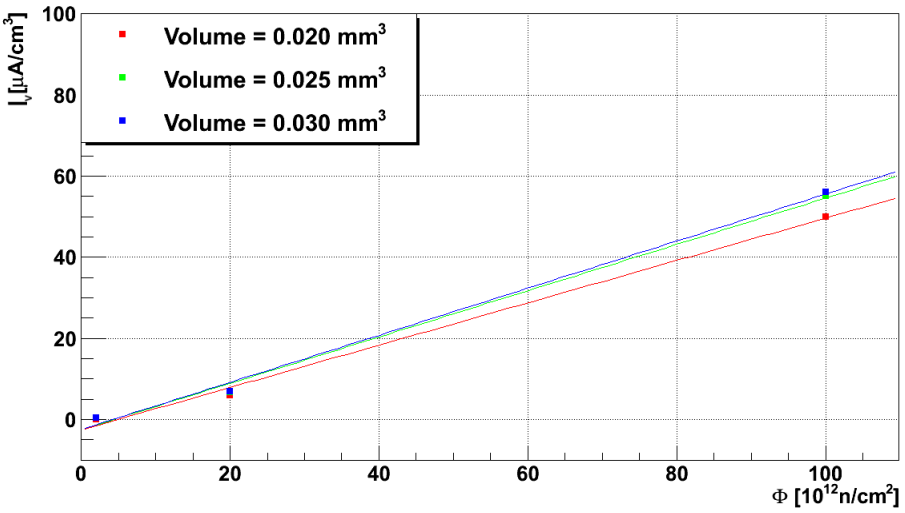

Figure 9.8: Current (per unit volume) as function of the fluence for different depleted volumes.

mated the α value for different depleted volumes: its value is not constant for different volumes but it is in a range between $\alpha = 5 \cdot 10^{-16} A/cm$ and $\alpha = 6 \cdot 10^{-16} A/cm$. The value obtained is higher than the value obtained with standard silicon devices, which is about one order of magnitude lower. Moreover it has to be taken into account the low accuracy of the linear fit, as it is possible to see in Fig. 9.8. However, it is hard to compare the α value obtained with standard silicon devices and the α value obtained with the LePix diode due to the several differences between the measurements conditions and the strong approximations done to evaluate the α value in the LePix diode case. In fact, no annealing procedure has been used on the LePix structure before measuring the α factor, to preserve the diodes in the same fluence conditions after irradiation; as already described previously, the irradiated diodes are not fully depleted and, consequently, the α factor has been evaluated only for fixed volume values. Finally, the geometry of the depleted volume is complex to evaluate and, consequently, not fully clear: the current per unit volume has been evaluated by using the volume obtained by a planar and abrupt approximation.

9.3 Matrix Radiation Hardness

The LePix matrix structure has been already described in detail in chapter 6. It is based on a matrix of sensitive diodes with a simple front-end and read-out electronics. Since the diode is more sensitive to the bulk damage while the electronics is more sensitive to the surface damage, the radiation hardness of the matrix structure has been tested in both the non ionizing and ionizing dose cases. The former will be the first one to be treated.
The LePix matrices have been irradiated with non ionizing particles in the same facility and in the same time of the diode structure, following the same procedures in terms of transportations, safety routine checks, PCB gluing, bonding and cold storage.
The goals of the measurements on the irradiated matrices have been to evaluate the capacitance, leakage and noise performance degradations after irradiation. As already explained in the first part of the chapter, one of the main consequences of the bulk damage is the increasing of the leakage current caused by trap levels in the band-gap region which increase the number of thermally excited charges which find a trap level able to host them. The leakage current has a strong influence on the integration time because it fix its upper limit. In fact, as already explained in the previous chapters, the leakage current causes a voltage drop of the input node up to a point causing the forward bias of the source-bulk junction of the reset transistor. As soon as that point is reached (it has been called *leakage regime*), the input node is linked by the source of the reset transistor, following it. Consequently, the capacitance measurements have to be done in a regime which allows to have the input node not linked directly to the input bias. By increasing the leakage current, the time required to reach that point is even lower. It has been demonstrated by increasing the substrate bias, as shown in Fig. 7.16. In the irradiated matrices it has been observed a *leakage regime* reached already after a couple of clock cycles. It has to be reminded that, due to limitations of the circuitry, the clock frequency used has been $f = 390\ kHz$, which represents a long integration time already for a setting based on a few clock cycles. Consequently, the measurements conditions have been set to minimize the effects of the leakage current. It is well known that the main terms influencing the leakage current are the reverse bias of the substrate and the temperature. Consequently, the first step has been to make all the

measurements with a reverse substrate bias $|V_{sub}| = 15\ V$. The second step has been to place the matrix under test in a climatic chamber able to reduce the temperature down to $T = -40^oC$. However, during the measurements it has been used a temperature of $T = -24^oC$ which represents an acceptable compromise between the matrix performance and the temperature gradient respect the room temperature. The measurements have been done on a non-irradiated sample and on two irradiated samples having respectively a dose of $\Phi = 2 \cdot 10^{13}\ n/cm^2$ and $\Phi = 1 \cdot 10^{14}\ n/cm^2$. For higher doses, it has been reached the *leakage regime* even by using the smallest integration time possible. Moreover, the measurements have been done only on the active reset part of the matrix, which is less sensible to the leakage current.
In Fig. 9.9 and Fig. 9.10 the capacitance and the leakage current as function of the fluence are shown (the non irradiated device is represented with a fluence of $\Phi = 1 \cdot 10^{13}\ n/cm^2$ to avoid a too large scale on the X axis). They

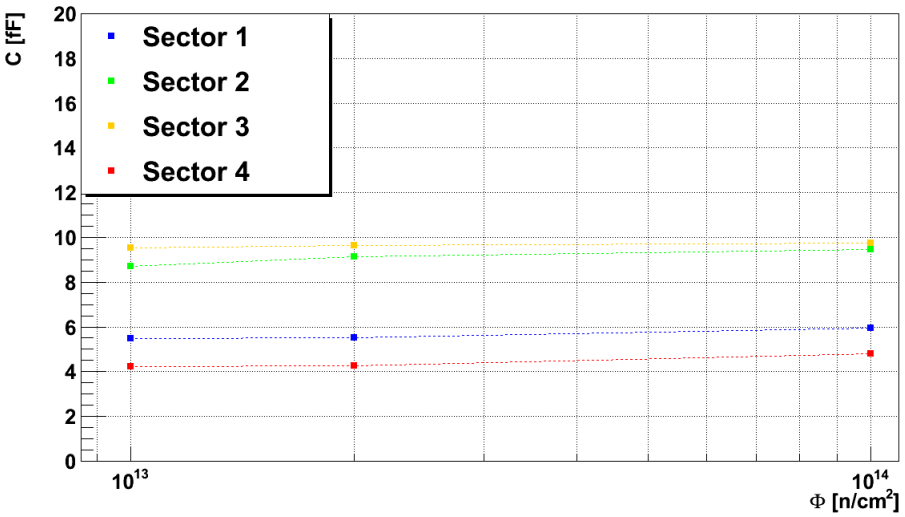

Figure 9.9: Matrix capacitance as function of the fluence for the four sectors.

have been obtained by following the same procedure explained in chapter 7. From the diode structure measurements, it could be expected a higher increment in terms of capacitance and leakage current values. It has to been reminded that the sensor capacitance is only one of the contributions to the input capacitance: while the sensor capacitance value is sensitive the bulk damage, the other contributions are almost constant. The leakage current

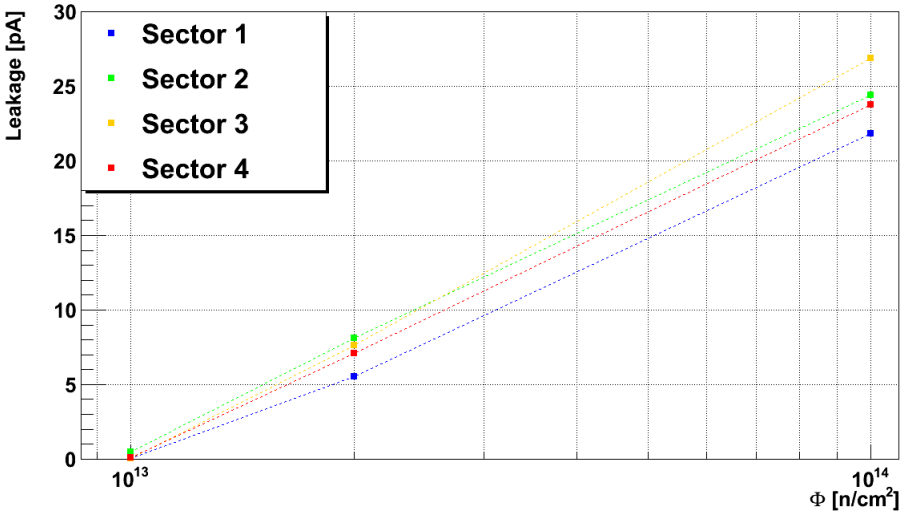

Figure 9.10: Matrix leakage current as function of the fluence for the four sectors.

increment is lower due to the shape of the depleted volume which expands only in a small region around the electrode. Consequently, most of the damage are created in the undepleted volume, where there is not electric field, giving no contribute to the leakage current: it could be assumed that, in a fully depleted matrix, the increment of the leakage current could be higher. Fig. 9.11 shows the noise increment of the first matrix sector for different fluence values. In chapter 7, the main contributes to the input noise have been explained: there is one contribute due to the input transistor, which is constant with time and represents the main contribute for small integration time, and one contribute due to the noise caused by the diode, which is proportional to the square root of the product between the leakage current and the integration time and represents the main contribute for large integration time. It can be seen that, due to the measurements temperature $T = -24^o\ C$ which reduces the leakage current and, consequently, the noise caused by the diode, the input transistor noise for a non irradiated device gives the main contribute to the total noise also for large integration time. Vice-versa, for a strong irradiated device ($\Phi = 1 \cdot 10^{14}\ n/cm^2$), the parallel noise gives the same contribute of the input transistor noise already for a small integration time.

The irradiated matrices performances have been also tested by using an ^{55}Fe

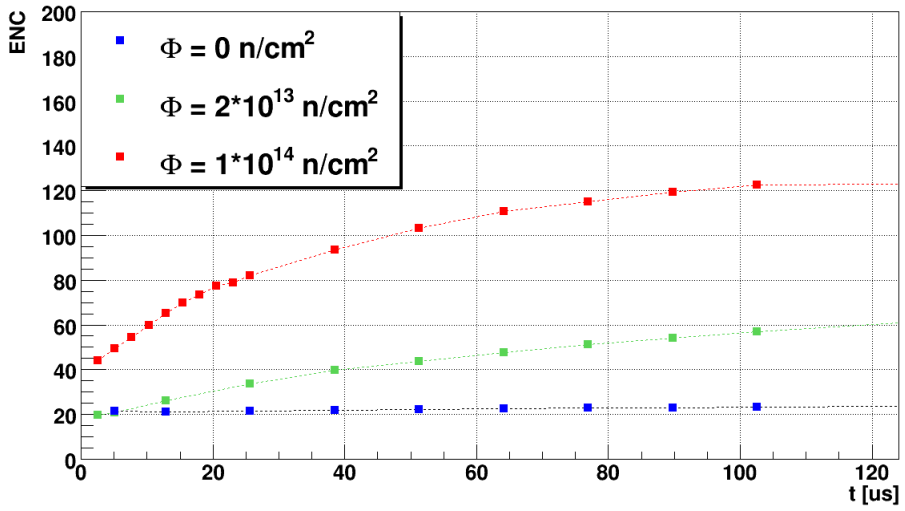

Figure 9.11: Input node noise of the first sector for different fluencies.

X-Ray source. The measurement conditions in terms of biases, integration time and temperature have been the same used to evaluate the capacitance, the leakage and the noise of the irradiated matrices. In Tab. 9.1, the 5.9 keV peaks in ADC values for each sector are shown: it is possible to see both a lower ADC peak value (due to the increasing capacitance) and a larger peak spread (due to the increasing noise) for higher fluencies. It can also

	$\Phi = 0\ n/cm^2$		$\Phi = 2 \cdot 10^{13}\ n/cm^2$		$\Phi = 1 \cdot 10^{14}\ n/cm^2$	
	E_1	ΔE_1	E_1	ΔE_1	E_1	ΔE_1
Sector 1	389.4	10.1	381.7	12.5	358.7	21.2
Sector 2	261.1	8.39	248.2	11.1	240.2	15.6
Sector 3	233.4	8.9	230.8	10.6	228.1	16.1
Sector 4	304	18.9	302.8	18.9	268.7	23.6

Table 9.1: Peaks in ADC counts for the 5.9 keV X-Ray of the ^{55}Fe source for different fluence values.

be seen in the Fig. 9.12, where the peaks of the first sector are shown: in the non-irradiated chip, the ADC conversion factor is high, the peak dispersion is low and the second ^{55}Fe peak is clearly visible while for a strongly irradiated chip ($\Phi = 1 \cdot 10^{14}\ n/cm^2$), the ADC conversion factor is lower, the peak dispersion is higher and the second peak is no more visible.
The matrix radiation hardness has been also evaluated with ionizing dose.

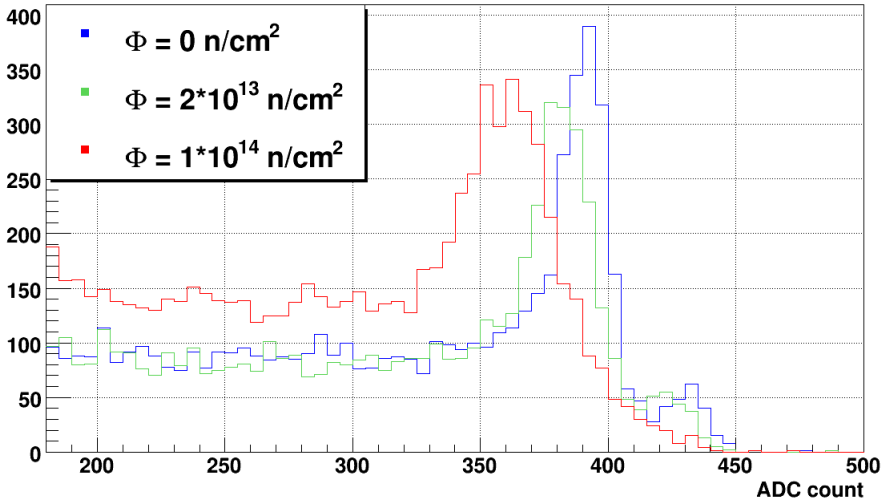

Figure 9.12: ^{55}Fe 5.9 keV peaks at difference fluencies for the first matrix sector.

In the total ionizing dose tests, the matrix has been exposed to $\approx 10keV$ photons provided by the CERN X-ray irradiation facility. A dose rate of 5 $kRad$ per minute has been employed, keeping the circuit at room temperature and under nominal bias conditions. However, since it is not possible to optimize all sectors in the same time in terms of pixel bias, it has been decided to use a bias optimizing the PMOS input transistor with active reset sectors. On the basis of the test performed on individual devices, only minor threshold shifts are expected on thin oxide transistors in the 90 nm CMOS technology. However, the metal introduced for filling purposes provides the gate to transistors that could be severely affected by ionizing radiation. The STI islands are another source of concern.
The matrix has been irradiated up to 10 $MRad$ with an exponential progression. After each step, the matrix has been characterized in terms of capacitance, leakage current and serial output voltage shift. In Fig. 9.13 and Fig. 9.14, the capacitance and leakage current variations up to a dose of 10 $MRad$ are shown. The capacitance can be considered constant up to 1 $MRad$, while the leakage current has an increasing trend. During the last irradiation step (from 1 $MRad$ to 10 $MRad$), a significant shift has been noticed: by optimizing the biases, it has been possible to recreate on the oscilloscope the classical matrix serial output path (see Fig. 7.4 for a non-

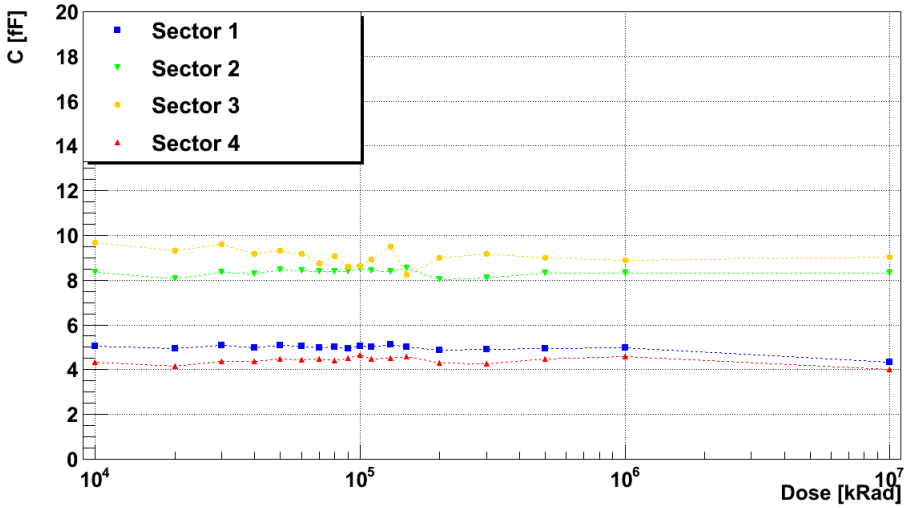

Figure 9.13: Capacitance variations with ionizing dose.

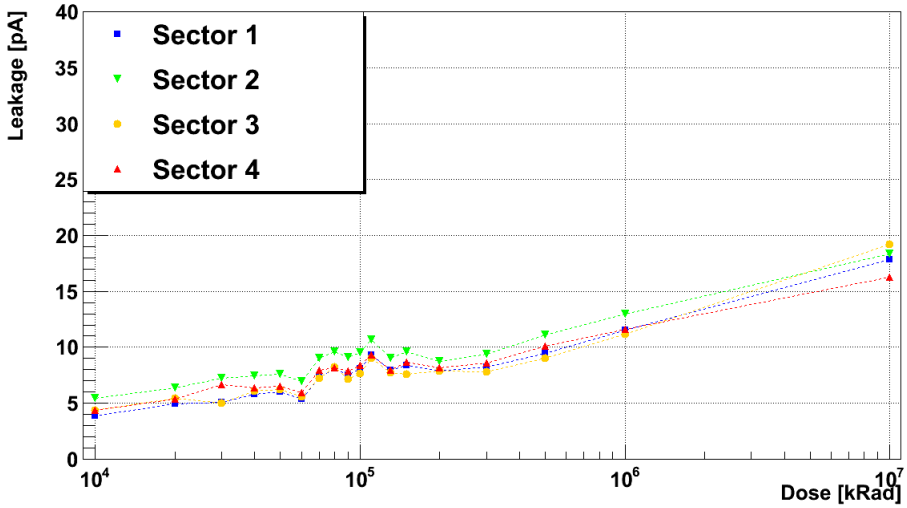

Figure 9.14: Leakage variations with ionizing dose.

irradiated matrix and Fig. 9.15 for an irradiated matrix) but a degradation of the source follower performance and a high leakage current have been noticed with the impossibility to have realistic measurements in terms of capacitance and leakage current. To estimate the capacitance and the leakage current after a 10 $MRad$ irradiation, an annealing procedure has been done.

Several procedures can be applied in terms of annealing for a device. One of the most common annealing practices for IC is based on an annealing of 1 week at a temperature $T = 100^o\ C$: it corresponds to an annealing of several years at room temperature. However, since the matrix is not only made by standard IC (such as CMOS based circuits) but has also a sensitive component (the diode), it has been decided to have a room temperature annealing monitoring the effects on the matrix. The capacitance and the leakage current at 10 $MRad$ shown on Fig. 9.13 and Fig. 9.14 have been obtained after an annealing procedure at room temperature of 6 months. In Fig. 9.15 the serial output of 16 active reset pixels of the first column

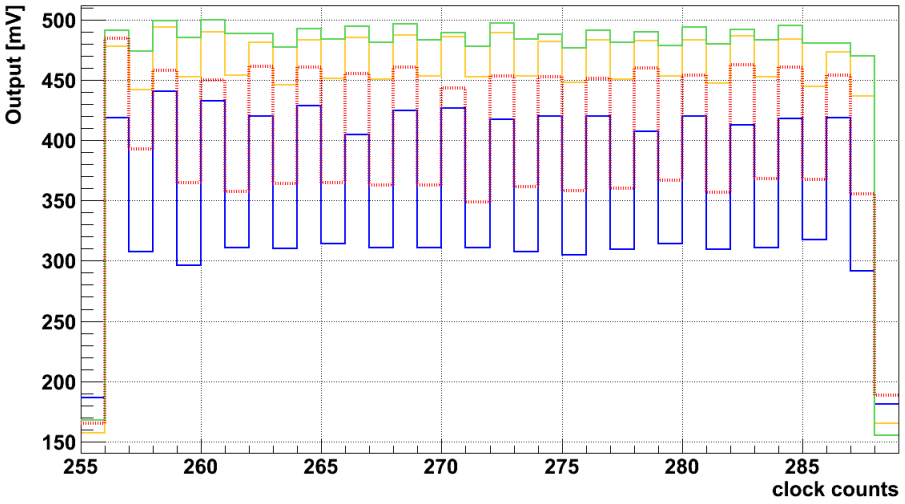

Figure 9.15: Serial output of a first sector column with active reset for different dose values (green for a 10 $kRad$ dose, orange for a 1 $MRad$ dose, blue for a 10 $MRad$ dose and dotted-red for a 10 $MRad$ dose with a six months annealing at room temperature).

is shown: it is possible to see a small DC shift for the 1 $MRad$ dose and a significant shift after the full dose (10 $MRad$). In Fig. 9.15 it is also possible to see the serial output of the same chip with the same bias conditions of an irradiated chip after the annealing. The matrix performance after the annealing has been also tested with a ^{55}Fe X-Ray source. In Fig. 9.16 it is possible to see the peaks for the third sector (which is expected to have the worst performance due to the largest collection electrode and the thickest oxide) which confirms the almost constant capacitance value. It is also

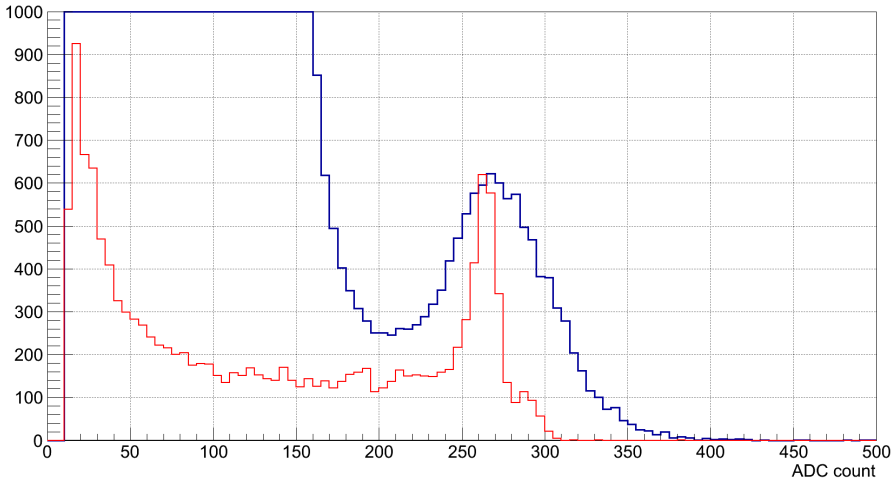

Figure 9.16: ^{55}Fe peaks for the third sector before irradiation (red) and after a 10 $MRad$ irradiation and a 6 months annealing at room temperature (blue).

possible to notice an increased width of the ^{55}Fe peak. This is mainly due

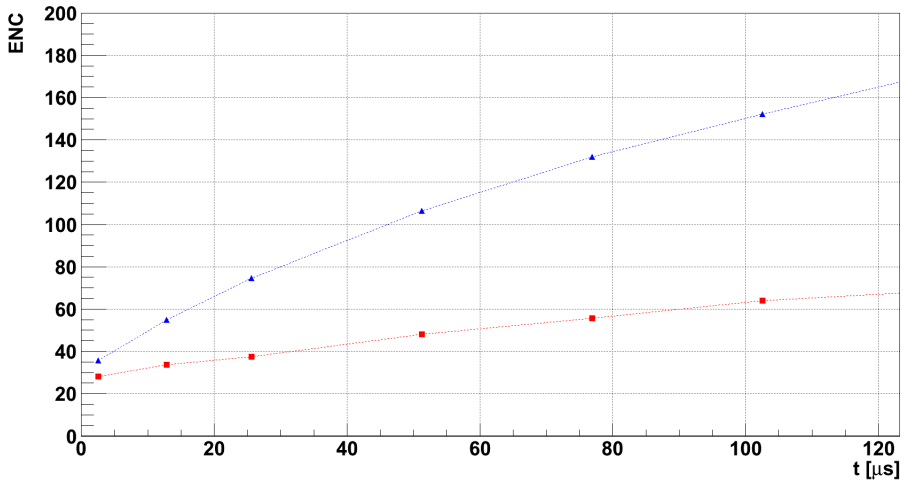

Figure 9.17: Equivalent noise charge (ENC) of the third sector before irradiation (red) and after a 10 $MRad$ irradiation and a 6 months of annealing at room temperature (blue).

to the increased leakage current and, consequently, of the detector noise. In Fig. 9.17, it is possible to see the noise increased of about a factor two after

a 10 $MRad$ irradiation and a 6 months annealing at room temperature.

9.4 Conclusions

The diode structure and the matrix structure radiation hardness has been evaluated in terms of non-ionizing radiation and ionizing radiation. In the neutron irradiated diode structures it is possible to observe an increasing leakage current up to four orders of magnitude higher than a non-irradiated diode. It is also possible to see an increasing capacitance due to a variation of the effective doping level and, consequently, a smaller depletion depth. The matrix structure shows interesting performance in terms of non-ionizing dose up to a fluence of ($\Phi = 1 \cdot 10^{14}\ n/cm^2$); however, the radiation resistance is mainly limited by the relatively long integration time, which makes the device sensitive even to moderate increase of the leakage current. Consequently, it has been not possible to estimate the capacitance value for higher fluencies. Ionizing dose measurements have been also performed: the matrix shows negligible variations for dose lower than 1 $MRad$; for higher dose, it is possible to see a significant shift in the matrix output which recovers in a few months of annealing at room temperature.

Chapter 10

Binary Front-end Matrix

In this chapter, the matrix equipped with a binary front-end will be described. In particular, during the first part a general overview of the circuitry will be shown; in the second part every single stage of the read-out electronics will be discussed in details.

10.1 Binary Front-end

The binary front-end matrix has been designed as an alternative to the analog front-end matrix in terms of read-out approach: the output signal is only one bit which changes in case of a particle hit. The digital matrix maintains the same pixel-cell structure, based on a reset mechanism and a source-follower input transistor used to buffer the signal at the matrix periphery. However, the read-out electronics is completely different. It is based on a preamplifier, a discriminator and a memory cell which allow to detect and digitally store a particle hit as soon as the signal charge is collected onto the pixel. After a tunable sensitive time, the digital signals for all pixels are read out serially. Shaping the preamplifier signal allows the circuit to be even less sensitive to leakage current than for the analog serial read-out. Moreover, since only one bit per pixel is transmitted (and consequently only one clock cycle is required per pixel), the time spent to read the whole matrix is reduced of a factor two compared to the analog matrix, where two clock cycles per pixel are required.
In Fig. 10.1 a schematic view of the binary front-end is shown. The pixel cell is the same of the analog front-end matrix. The signal is then sent

to the periphery by a metal line (one for each pixel) having a parasitic capacitance C_{line} of about 250 fF. The pixel is AC-coupled to the front-

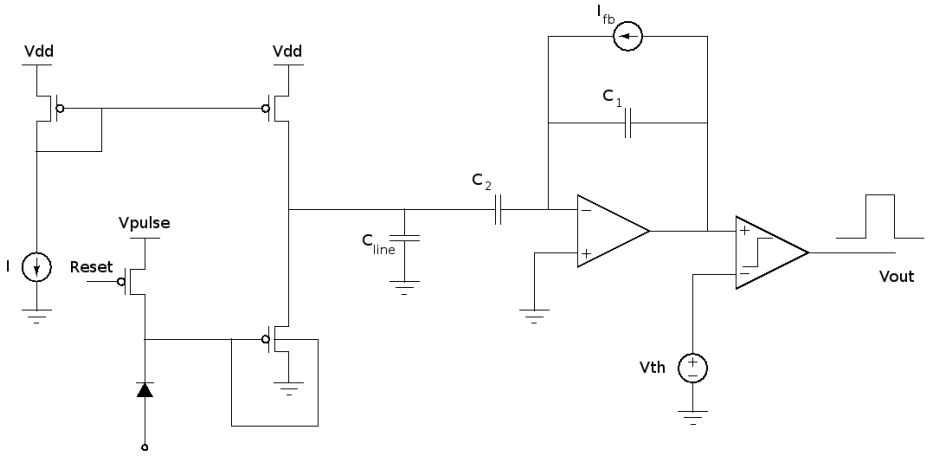

Figure 10.1: Schematic view of the front-end electronics of the matrix.

end electronics via the capacitor C_2. The first stage of the front-end chain is a voltage amplifier with a capacitive feedback. The closed-loop voltage gain is defined by the ratio C_2/C_1 and has a nominal value of 12. Both the capacitors are implemented as metal-to-metal capacitors. The current source in parallel to C_1 establishes the necessary DC path to properly bias the amplifier and to discharge C_1 after a signal has been detected. The feedback current source is implemented with an PMOS transistor which is driven in saturation region when the voltage at the preamplifier output rises of a few tens of millivolts above the baseline. The value of the feedback current can be externally adjusted. The output of the preamplifier is then fed to the comparator. The threshold is set globally by the voltage applied to an external pin. Consequently, it is not possible to perform a threshold tuning in each pixel. The output of the discriminator acts as clock for a flip-flop, allowing to have a logic 1 value whenever there is a transition from low to high level at the output of the discriminator. The flip-flop of different channels are configured as a shift register to allow a serial read-out of the stored bits. In Fig. 10.2, the output architecture used in the digital matrix is shown: it is based on a shift register consisting of 1024 flip-flops, one for each pixel. Similar to the analog front-end matrix, the binary read-out is controlled by external signals (see Fig. 10.3). During the acquisition phase,

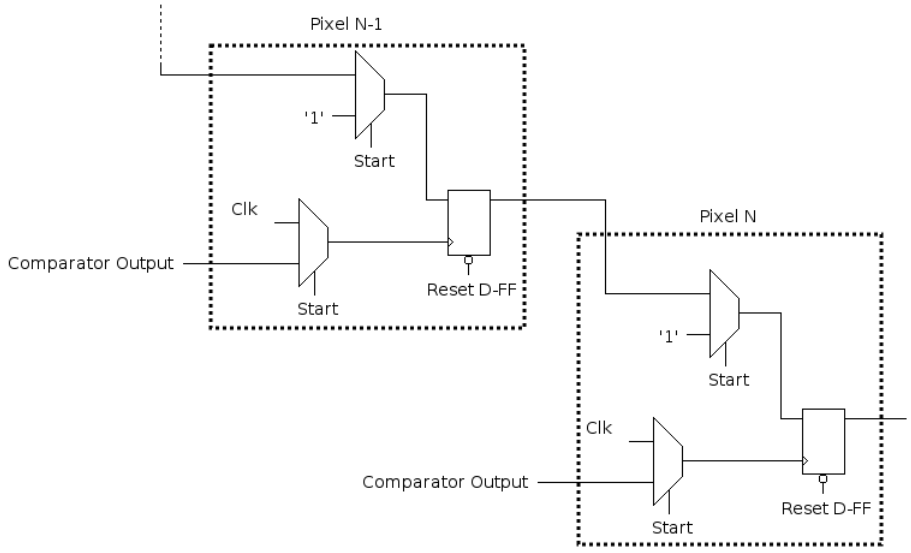

Figure 10.2: Output architecture for the digital read-out.

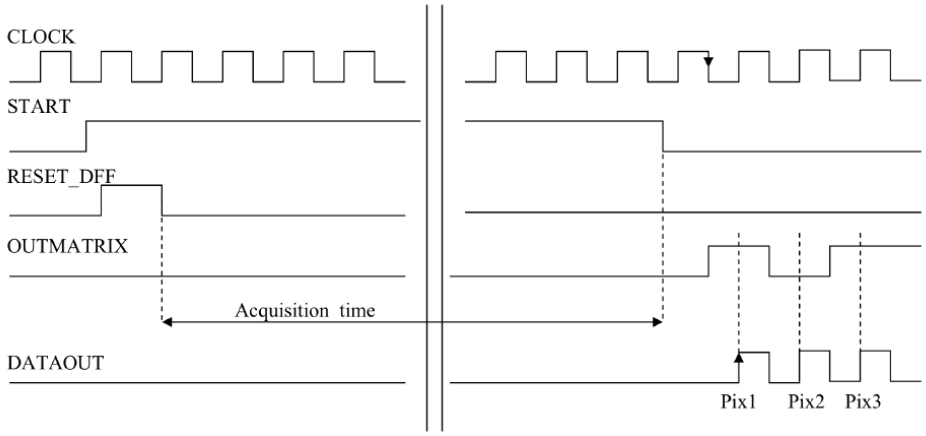

Figure 10.3: External signals driving the operation of the binary front-end based matrix.

the START signal is high and the CLOCK signal is not propagated to the register. Both the pixel and the shift register are reset; the clock input of the flip-flop is connected to the comparator output of the corresponding pixel. When a pixel is hit, the comparator creates a digital pulse storing a bit in the flip-flop. When the START signal is set to zero, data and clock inputs of the N^{th} flip-flop are switched respectively to the output of the $(N-1)^{th}$

flip-flop and the external clock. In this mode, the flip-flops are configured as a shift register and data are automatic serialized. The cycle continues for 1024 clock cycles and then START is brought high again.

10.2 Front-end Amplifier

The front-end amplifier is based on a cascode stage having a NMOS input transistor and a PMOS load, as shown in Fig. 10.4. To have an acceptable DC gain, regulated cascodes have been used for both the input device and the load. In fact, when a pixel is hit, a negative pulse reaches the input

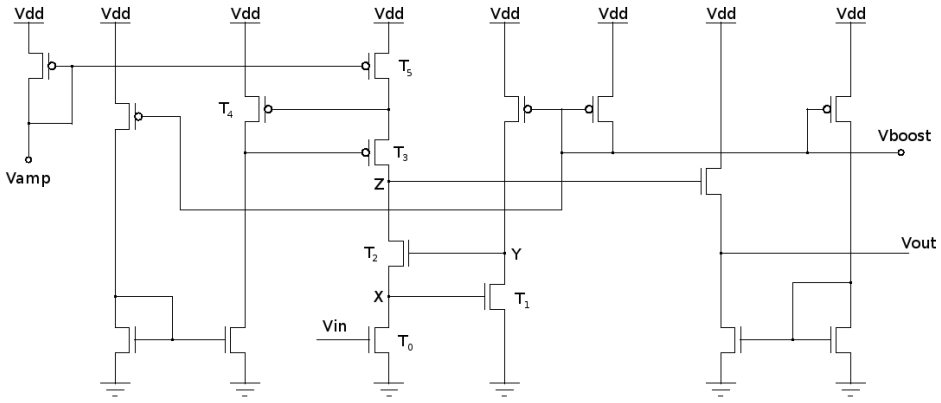

Figure 10.4: Front-end amplifier stage.

of the cascode stage, reducing the V_{gs} of the input transistor T_0. Consequently, the drain-source of that transistor increases; also the V_{gs} of the NMOS transistor T_1 increases. However, the current flowing in that branch has to be constant: the T_1 transistor is forced to reduce its drain voltage (called Y). The NMOS transistor T_2 has consequently a reduction of the gate voltage (Y) and an increase of the source voltage (X) and it is forced to increase the voltage at the Z node. That node is then connected to a source follower which guarantees a proper matching between the DC levels in the internal nodes of the amplifier. The pin V_{amp} allows the regulation of the bias current in the main branch of the amplifier, while the pin V_{boost} allows the regulation of the bias current in the gain-boosting auxiliary amplifiers and in the source follower. The transistors designed in diode configuration are in common to all channels on the chip. The circuit used to bias both the

main amplifier and the gain-boosting stage is the same shown in Fig. 6.9. As already mentioned previously, a capacitive feedback regulates the gain of the stage. The capacitors are implemented as metal to metal structures. There are two different approaches to implement metal to metal capacitors: *MIM-cap* (metal-insulator-metal) and *MOM-cap* (metal-oxide-metal). The former (see Fig. 10.5) is based on two metal plates separated by a dedicated thin insulator with high dielectric constant (e.g. Silicon nitride, Si_3N_4): this allows to have high capacitance per unit area and, consequently, relatively compact components. Moreover, the design software tools can guarantee a high precision for the values of those capacitances. However, this approach suffers some drawbacks. In particular, a minimum size capacitance is im-

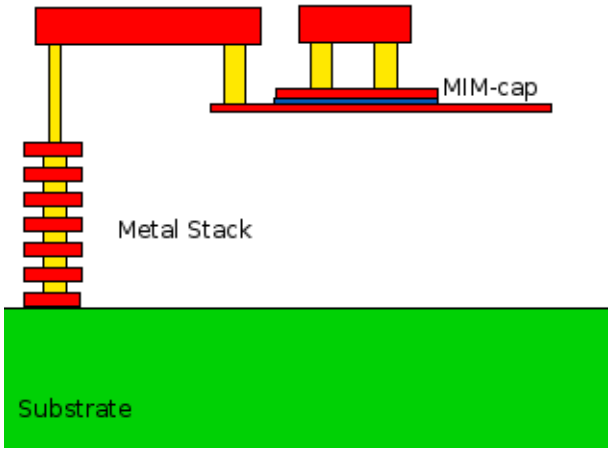

Figure 10.5: Simplified view of a MIM-cap.

posed by the technology (which does not allow to use the *MIM-cap* approach for capacitances in a few femtoFarad range) and an additional mask (plus its photo-step) is required in the fabrication process.
The *MOM-caps* are the second possible approach. They are based on capacitances composed by two (or more) metal layers of the ordinary metal stack separated by the oxide. The main difference compared to the metal-insulator-metal capacitor is represented by the dielectric between the metal layers which is standard oxide. Since some technologies offer the possibility to use low dielectric constant in the metal stack, they can reach capacitance value lower than the *MIM-caps*. There are two possible approaches to develop a metal-oxide-metal capacitor: an horizontal approach and a vertical

approach. In the former case, the capacitance is realized by horizontal metal plates separated by oxide. One of the factors limiting the minimum value of those capacitances is represented by the thickness of the oxide placed in the metal stack which is fixed by the technology used. The vertical approach

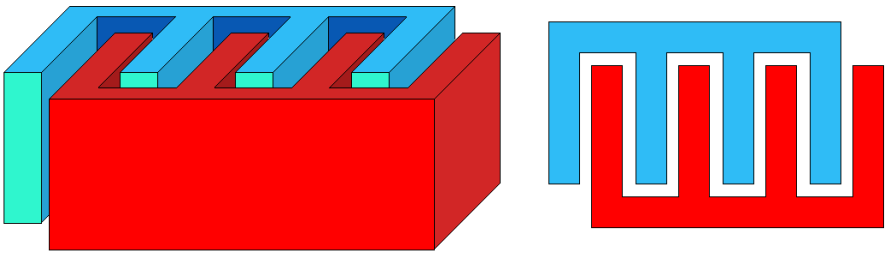

Figure 10.6: 3D (left) and top (right) simplified views of a metal-oxide-metal capacitor based on a vertical approach.

(see Fig. 10.6) allows to overcome that limit. They are based on fingers of metal wires and vias developing over the whole metal stack. Since they have vertical plates, the minimum allowed distance is fixed by the metal pitch of the technology used, which is considerably lower than the typical thickness of the oxide separating two metal plates in a horizontal capacitance. In principle, it could be possible to reach capacitance values in a few femtoFarad range. Typically, Integrated Circuits design tools implement that type of capacitance by using a design layer which allows to define with high accuracy the capacitance value obtainable. The price to pay to use that layer and obtain a capacitor with a precise value is the minimum distance between vertical metal plates which has to be higher than the metal pitch. In fact, only in that case the design tools can determine the capacitance value with high precision. Consequently, the advantage to have the possibility to determine the capacitance value with high accuracy has the drawback to limit the minimum capacitance value.
The capacitors used to implement the feedback in the front-end amplifier are *MOM-caps* having vertical plates. However, since small capacitances were desired, it has been decided not to use the layer to determine the values of the capacitors, allowing to use the desired pitch between metal plates. The drawback of this choice is the real value of the capacitors and, consequently, the real gain of the stage which cannot be determined with high precision during the schematic simulations (the closed-loop voltage gain has a nominal

value of 12). Only after the post-layout simulations it has been possible to determine the gain of that stage, which is reduced of about a factor 2 with respect to the nominal gain.
Finally, also the current feedback has to be taken into account to determine the real gain of the stage. In fact, due to the low bias current (in the μA range) the amplifier has a rise time of several tens of nanoseconds. Therefore, the discharge of the feedback capacitor may start before the voltage has reached the maximum theoretical value given by $V_{out} = -V_{in} \cdot (C_2/C_1)$. As a result, the value of the feedback current regulates the effective gain of the amplifier: the lower will be the feedback current, the higher will be the stage gain.

10.3 Discriminator

A schematic view of the discriminator is shown on Fig. 10.7. The circuit consists of a differential pair with active load followed by two common source amplifiers and one inverter. Theoretically, when the input signal is below the threshold, the output voltage is zero while when it exceeds the threshold, the output voltage flips from zero to one. However, the real case could be

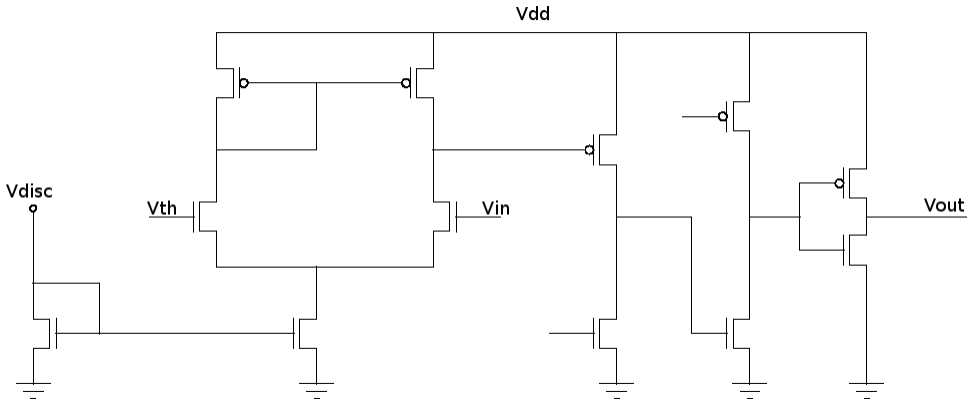

Figure 10.7: Schematic of the discriminator.

slightly different because of the non-infinity gain of the stages and the noise. To evaluate the influence of each contribute, it is possible to assume as a first assumption to have a noiseless input on the differential pair. For large voltage difference on the input pair, the output has only two possible values

which are logic 0 and logic 1. However, for an arbitrary small difference

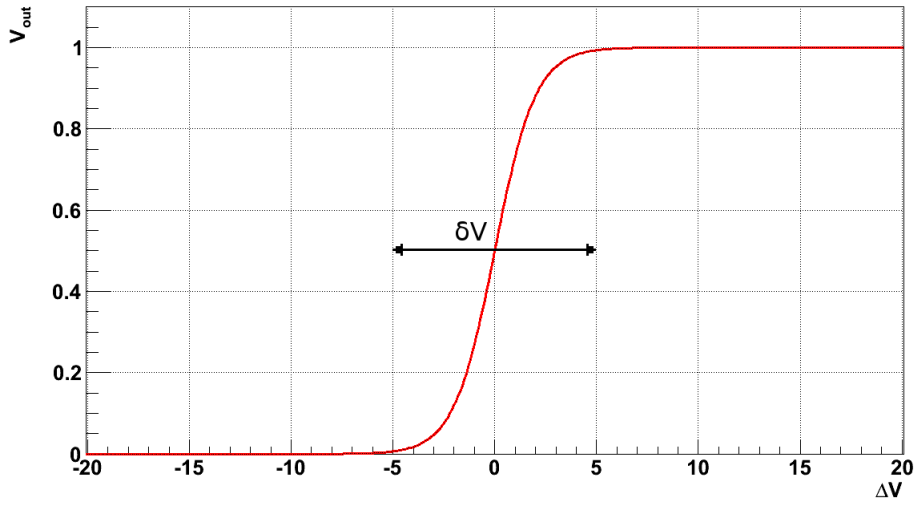

Figure 10.8: Noiseless discriminator output for an arbitrary small voltage difference on the input pair (the X and Y axis are in arbitrary unit).

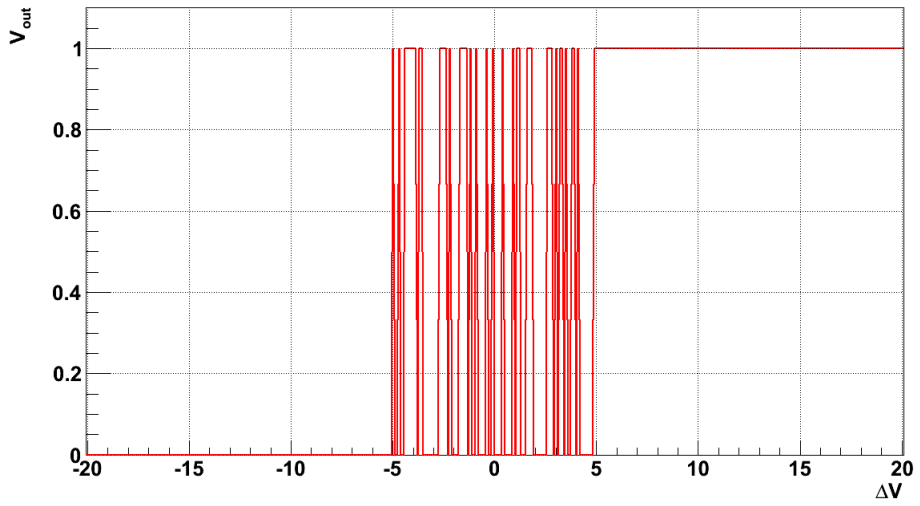

Figure 10.9: Discriminator output in case of noise at the input (the X and Y axis are in arbitrary unit).

on the input pair, it could be possible to have an undefined output which is not a logic 0 or a logic 1 (see Fig. 10.8). It has to be considered that it is

possible only for a small range of δV due to the effect of two common source stages and the inverter which reduce the possibility to have an undefined state. It is now possible to consider also the influence of the noise at the input: if the noise is lower than the δV range causing the undefined state, the curve shown in Fig. 10.8 will shift on the X axis; for noise value higher than δV, which is a more realistic case, the discriminator output will flip randomly also in the region causing the undefined output (see Fig. 10.9).

Chapter 11

Digital Matrix Characterization

In this chapter, the measurements done to characterize the digital matrix will be described; in particular, the first part will focus on the discriminator stage characterization, the second part will describe the measurements done to characterize the gain of the pre-amplifier, the third part will show the measurements performed with the laser setup while the last one the ^{55}Fe measurement results.

11.1 Discriminator Characterization

The discriminator stage is based on a high gain differential pair, two common source amplifiers and an inverter. On the positive input of the discriminator a pre-amplifier is placed while the negative input is connected to an external reference voltage. The output is connected to the clock of a flip-flop which allows to register a transition from a low value to a high value of the discriminator. In this way it is possible to digitize the signal coming from the previous stage: the discriminator can be thought as a sort of 1 bit ADC. The threshold of the discriminator has to be a reasonable compromise which allows to be indifferent to signals caused by the noise but as sensitive as possible to signals caused by real events. Consequently, the characterization of the discriminator stage is based on threshold scans which allow to determine the DC voltage level on the positive input, the input noise and

the comparator noise. In the remaining part of the section, the procedures followed to obtain those parameters and the results will be described.
It is possible to define the voltage at the positive input of the discriminator as $V_{in} = V_+ \pm \Delta V$, where V_+ represents the noiseless DC value on the positive input, which depends on the voltage output of the pre-amplifier stage, and ΔV represents the noise. As it is possible to see on Fig. 11.1, when the threshold voltage (V_{th}) is lower or higher than V_{in}, there is no commutation at the output of the discriminator and consequently, there is no commutation at the output of the flip-flop. When $V_{th} = V_{in}$, there is at least one commutation at the output of the discriminator which is registered by the flip-flop. By having a threshold scan it is possible to determine the values of both V_+ and ΔV. In fact, by storing the voltage range of the discriminator commutations ($V_{min} = V_+ - \Delta V$ and $V_{max} = V_+ + \Delta V$), it is possible to estimate the DC value on the positive input (V_+), which is imposed by the output stage of the pre-amplifier, by averaging V_{min} and V_{max}, and the voltage difference between those two values can be used to obtain a realistic estimation of the noise at the input of the discriminator. Moreover, by averaging several identical acquisitions of the same comparator, it is possible to obtain the comparator *S-curve*, which allows to define the noise of the discriminator.
Since the pre-amplifier is AC coupled with the pixel front-end, there is no influence of that stage in terms of DC bias. Consequently, the DC value at the input of the discriminator does not depend on the matrix sector. This allows to evaluate possible transistors mismatch over the whole matrix by comparing the homogeneity of the threshold of all matrix comparators.
The main parameters of each discriminator (DC input value on the positive input, noise, comparator noise) have been obtained as follows: a threshold scan has been done, by changing the threshold (V_{th}) with a 50 μV step, obtaining for each pixel the plot reported in Fig. 11.2, which shows the output of the discriminator of the matrix first pixel for different voltage biases of the threshold. Moreover, for each step, 1024 acquisitions have been taken automatically by the acquisition system. In Fig. 11.3 the average values for each step of the pixel used in Fig. 11.2 are shown: when the output bit is 0, there are no commutations at the discriminator output, when it is 1 there are continuous commutations. The rising and the falling edges of the curve are used to determine the discriminator noise which has been obtained as

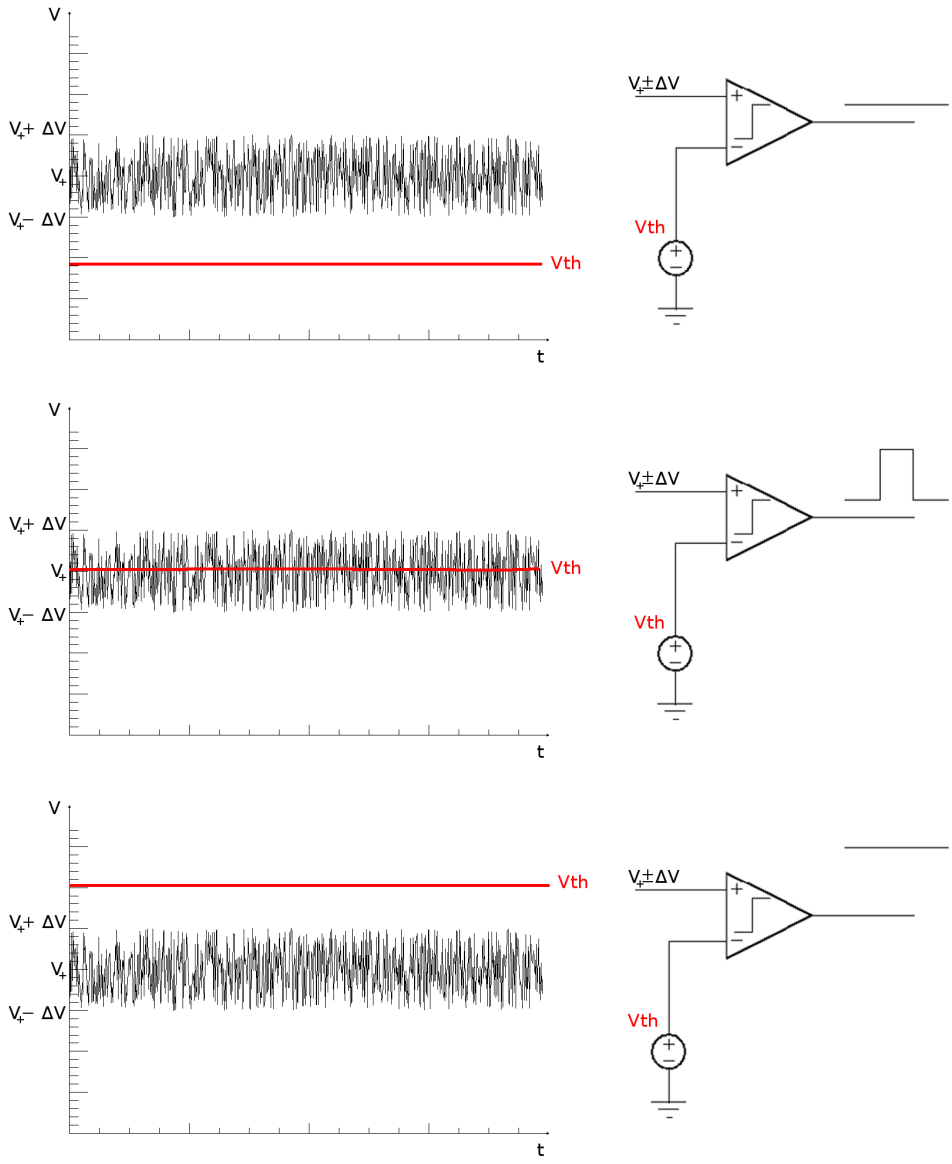

Figure 11.1: Possible outputs in case of threshold scan.

follows: the curves fitting the rising and the falling edges have been derived; the derivatives (Fig. 11.4) have been fitted by gaussian fits and their RMS has been considered to be equal to the comparator noise. The two peaks of the gaussian fits and their RMS values have been also used to evaluate the DC voltage value at the positive input of the discriminator by the following

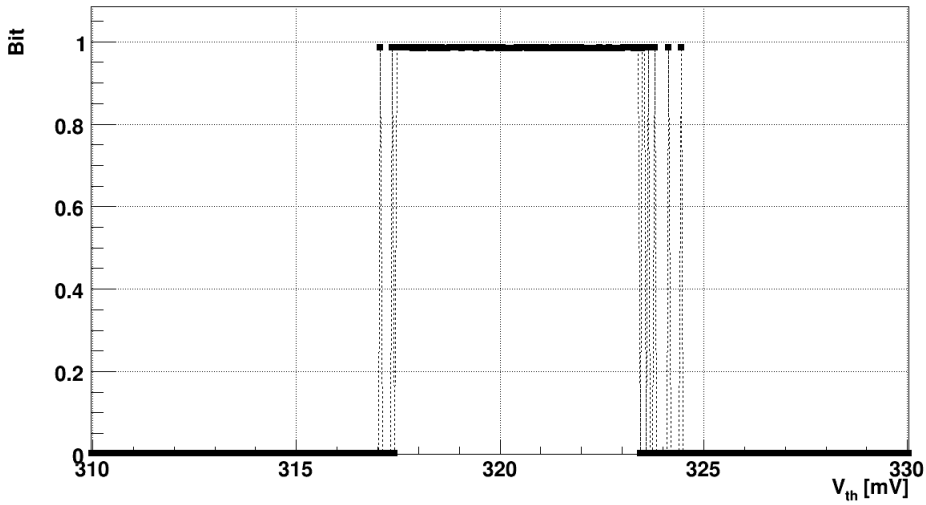

Figure 11.2: Discriminator output for the first pixel of the matrix.

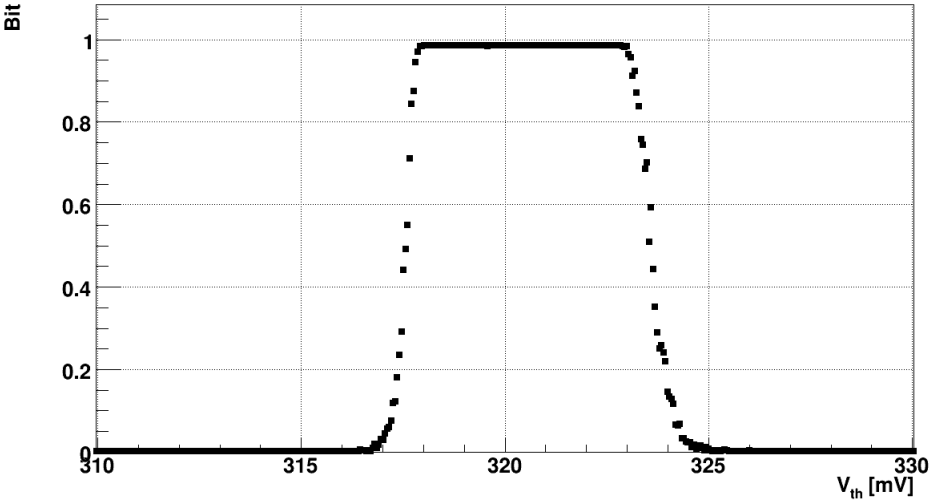

Figure 11.3: S-curve for the first pixel of the matrix.

relationship:

$$V_+ = \frac{(V_{ris} - 3 \cdot \sigma_{ris}) + (V_{fall} + 3 \cdot \sigma_{fall})}{2}$$

while the noise has been obtained by:

$$\sigma_{tot} = \frac{(V_{fall} + 3 \cdot \sigma_{fall}) - (V_{ris} - 3 \cdot \sigma_{ris})}{6}$$

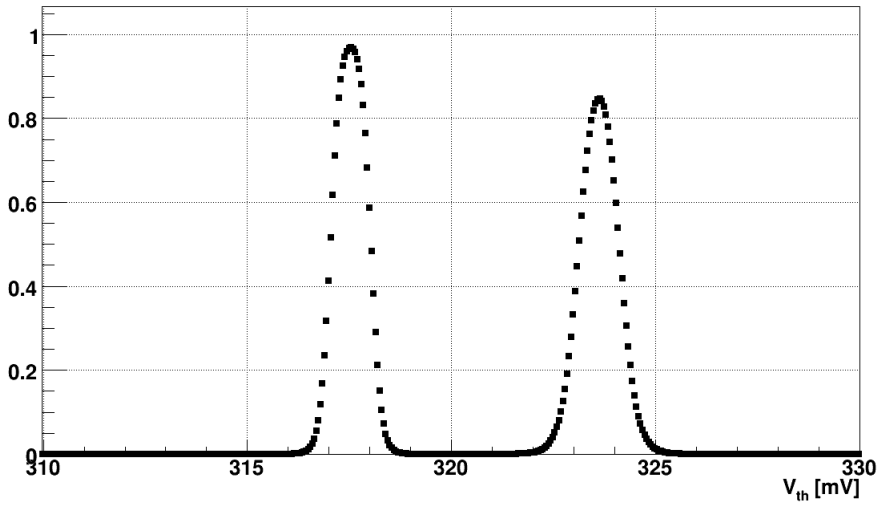

Figure 11.4: Curves obtained by deriving the curves fitting the rising and the falling edge of Fig. 11.3.

The procedure has been repeated for all pixels to obtain the homogeneity in terms of threshold, noise at the input of the discriminator and comparator noise. Fig. 11.5 shows the different threshold for discriminators of the same chip. Usually, an on-chip trimming system is implemented to apply an on-line correction of the threshold and eliminate the threshold dispersion shown in Fig. 11.5. This approach has been not possible: after the design of the front-end and read-out electronics already described, no more space was available to place a trimming system.
By following the procedure already described, the noise at the input of the comparator and the comparator noise have been evaluated obtaining the results shown on Fig. 11.6 and Fig. 11.7. The same measurements have been repeated by decreasing the pre-amplifier current. The two main effects related to the current variation are a DC shift and a noise variation at the output of the pre-amplifier. In fact, since the input and the output of the preamplifier are linked by a feedback, by reducing the current in the main branch of the pre-amplifier, also the V_{gs} of its transistors and the output voltage will decrease. Moreover, by decreasing the current in the main branch of the pre-amplifier, also an increment of the noise is expected.

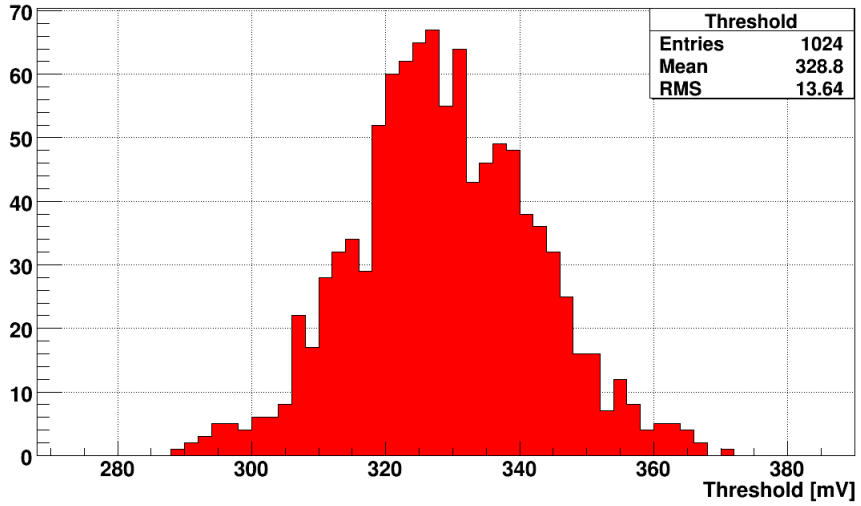

Figure 11.5: Histogram of the threshold homogeneity in the matrix.

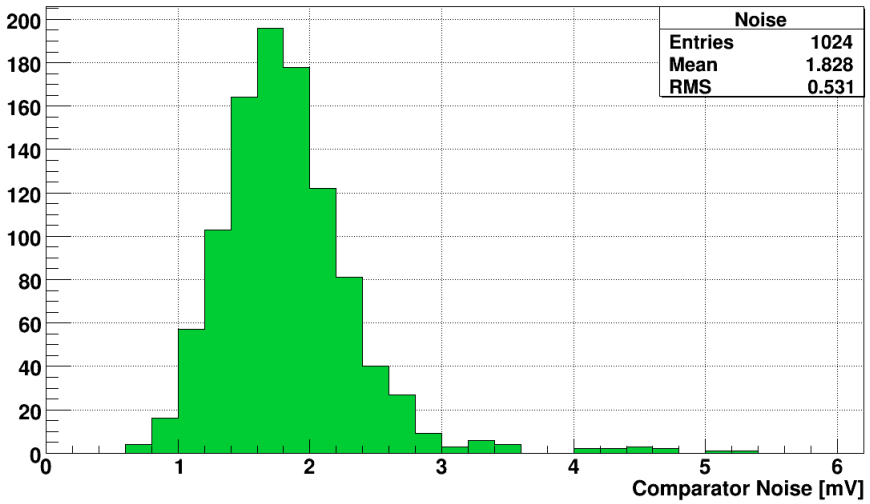

Figure 11.6: Histogram of the noise at the input of the comparator.

Both the DC shift and noise variation are shown in Fig. 11.8 and Fig. 11.9.

Also the current flowing in the differential pair of the discriminator has been changed (in a range from $0.25\mu A$ to $1.5\mu A$) to evaluate its influence in

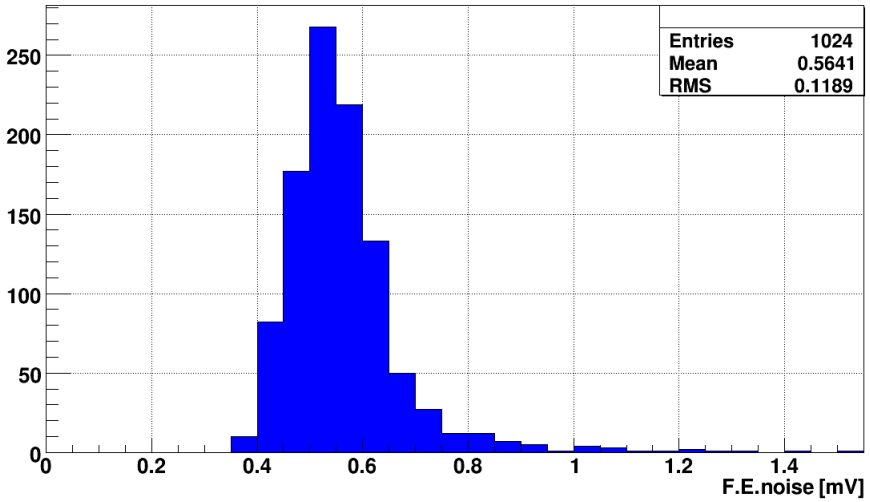

Figure 11.7: Falling Edge (F.E.) noise of the matrix comparators.

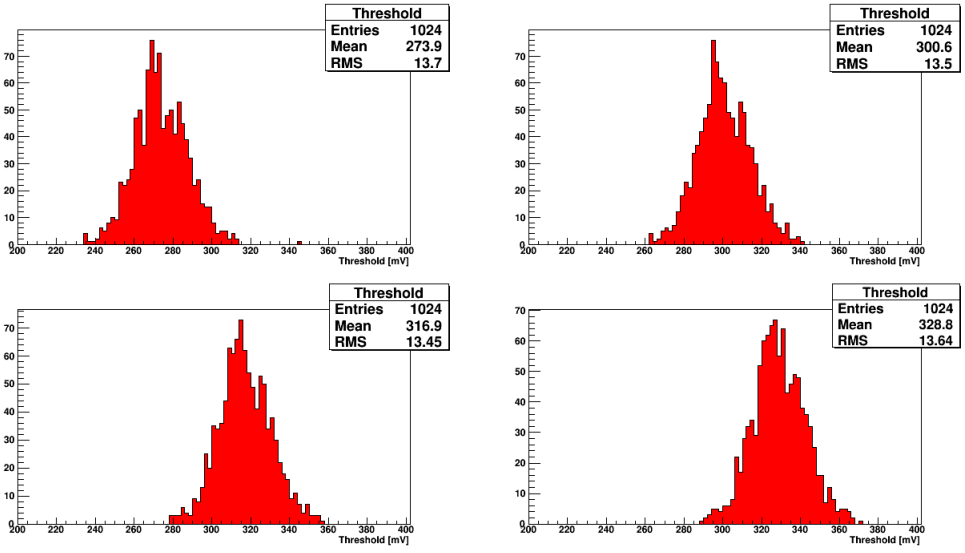

Figure 11.8: DC shift at the output of the pre-amplifier for different pre-amplifier current values (from the top-left histogram $I_{pre} = 0.5\ \mu A$, $I_{pre} = 1\ \mu A$, $I_{pre} = 1.5\ \mu A$, $I_{pre} = 2\ \mu A$).

the discriminator resolution but no notable variations have been seen.

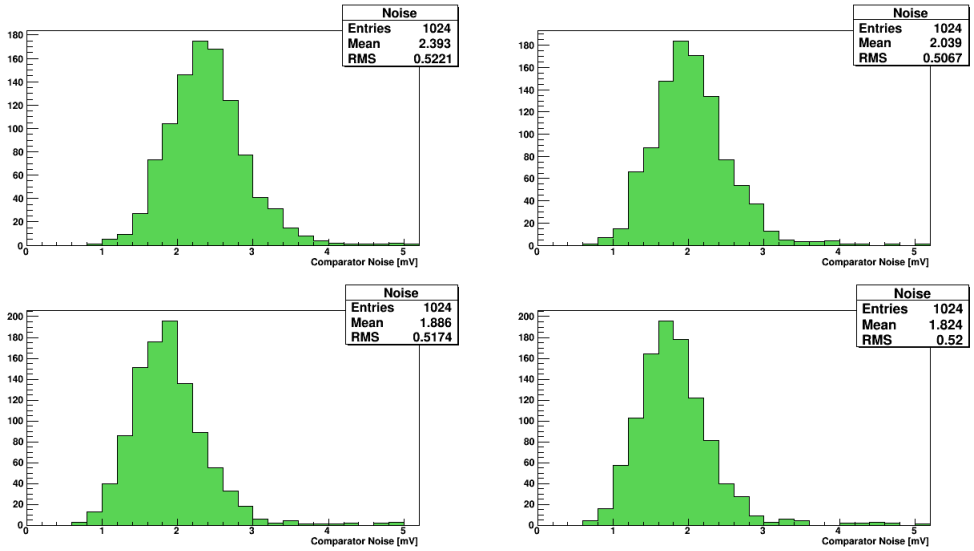

Figure 11.9: Noise at the output of the pre-amplifier for different pre-amplifier current values (from the top-left histogram $I_{pre} = 0.5\ \mu A$, $I_{pre} = 1\ \mu A$, $I_{pre} = 1.5\ \mu A$, $I_{pre} = 2\ \mu A$).

11.2 Pre-Amplifier Gain

The pre-amplifier stage has been already discussed in details in the previous chapter: it is based on a high gain amplifier with a capacitive feedback. The gain is regulated by the ratio between the capacitance connecting the pre-amplifier to the pixel source follower and the feedback capacitance. The nominal value of the gain has been estimated to be 12 but the post layout simulations showed a gain reduction of a factor two. Moreover, during the estimation of the pre-amplifier real gain it has to been taken into account the influence of the current feedback which starts to discharge the capacitance before the pre-amplifier can react, reducing the gain.

The goal of the measurements has been to evaluate the gain of the pre-amplifier and its variations for different values of the feedback current. In principle, the gain of the pre-amplifier could be obtained by pulsing directly the input transistor of the pixel front-end (by having the reset transistor always switched on, as already done in the analog read-out matrix) and having a threshold scan. In fact, by using an increasing pulse at the input, the discriminator will flip for higher and higher threshold, moving also the

falling edge of the S-curve as shown on Fig. 11.10. However, it has been

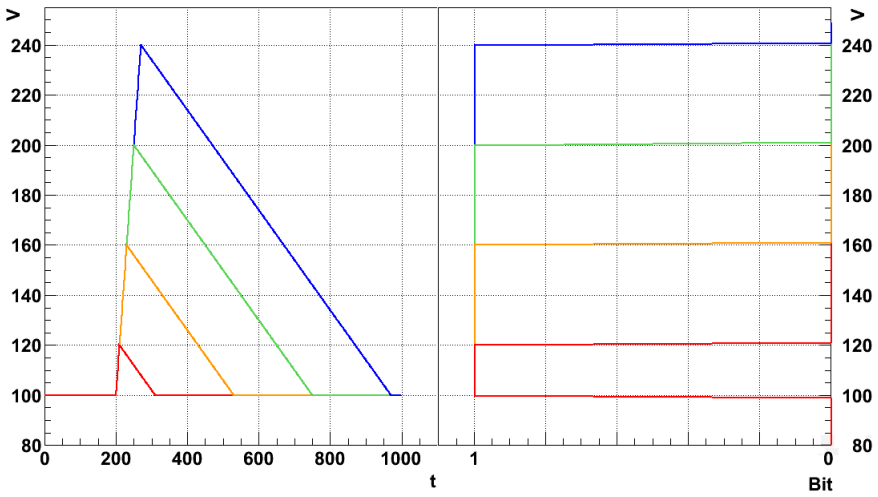

Figure 11.10: Pulses with different amplitude at the input of the discriminator and falling edge shifts due to them

noticed a random commutation of the discriminators by having the reset transistor always on, probably due to an injection of the clock signal on the input transistor of the front-end electronics by the reset transistor. This random commutation of the discriminators has not been noticed by resetting the pixels only at the beginning of the acquisition cycle. Consequently, it has been decided to reset the pixels only at the beginning of the acquisition cycle and to suppose the first source follower having a gain $G_{sf} \approx 0.9$.
The second step has been to pulse the input with different pulses and to have a threshold scan for each pulse value, by monitoring the falling edge variation in the S-curve. Fig.11.11 shows the falling edge variation as a function of the input pulse for different feedback current values. It is possible to see an increasing gain of the pre-amplifier due to the lower value of the feedback current which allows a higher charge of the feedback capacitance. In fact, as already mentioned in the previous chapter, the long rise time of the signal at the output of the pre-amplifier allows to the feedback current to start the discharge of the feedback capacitance before the signal can reach its maximum value.
As already explained in details during the previous chapter, during the de-

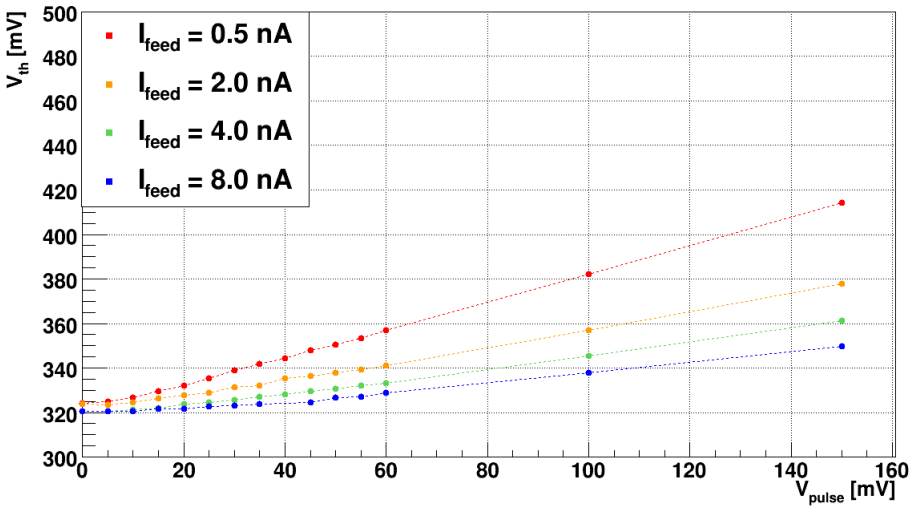

Figure 11.11: Falling edge variation in the S-curve of a pixel of the first sector with active reset as a function of the input pulse.

sign phase the layer implemented by the tool to evaluate the real capacitors value has been removed, allowing to use the minimum pitch between the capacitor plates but obtaining also, from the post-layout simulation, a real gain lower than the nominal gain: a gain reduction of a factor 2 is expected. Moreover, it has to be taken into account the mismatch of the feedback transistors providing the feedback current: due to that mismatch, a gain spread for read-out electronics of pixels of the same sector is expected. In Fig. 11.12 the gain of the whole pixel chain (front-end and read-out chain) for the 8 pixels of the four sectors with a feedback current $I_{feed} = 0.5\ nA$ is shown. It is possible to see a clear non-uniformity of the gain for pixels of the same sector. However, by knowing the input capacitors values (obtained by the measurements done with the analog matrix), by supposing the gain of the front-end source follower to be $G_{sf} \approx 0.9$ and by using the average values of the full chain gain for each sector it is possible to estimate the gain of the pre-amplifier stage to be around $G_{pre} \approx 5$.

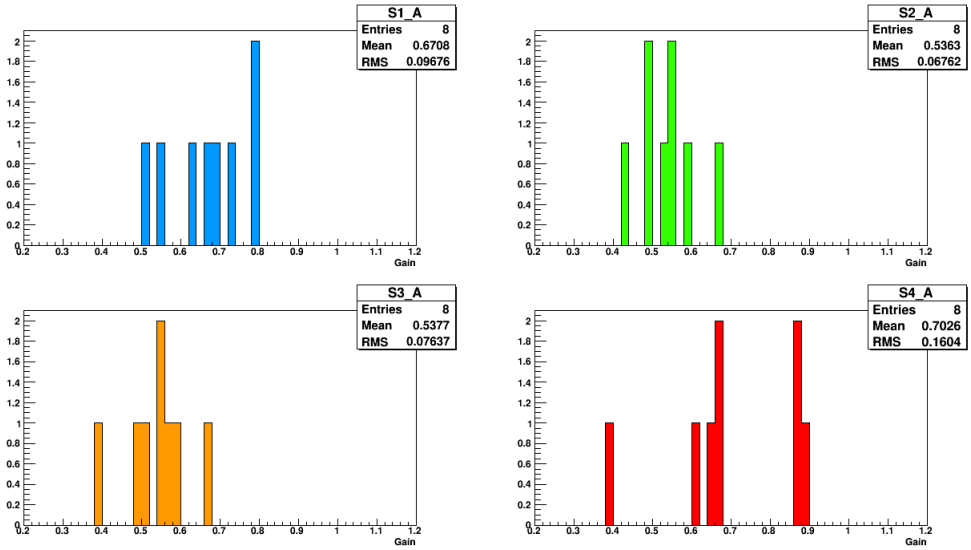

Figure 11.12: Gain of the front-end and read-out chain for the four sector with active reset.

11.3 Laser Test

The digital read-out matrix has been tested by using the same laser setup already used to test the analog read-out matrix. Fig. 8.1 shows the output response of the analog matrix to the laser test: it is possible to see two peaks corresponding to the electrode position and the signal lowering in the region between two pixels. Moreover, it can be seen that the signal in that region is slightly higher that zero. The goal of the measurements done with the digital read-out matrix is to see if the charge generated in the region between pixels is large enough to have the discriminators flipped. Consequently, it has been done a laser scan on the X and Y axis by having the substrate voltage at $V_{sub} = -30\ V$, by setting the feedback current of the pre-amplifier in such a way to maximize the gain of the pre-amplifier and by using a step of 5 μm on both the X and Y directions. For each position of the laser, four different threshold voltage values have been set on the negative input of the discriminator ($V_{th} = 400\ mV$, $V_{th} = 500\ mV$, $V_{th} = 550\ mV$, $V_{th} = 600\ mV$). The results obtained with the voltage scan are shown on Fig. 11.13. The figure must be interpreted as follows: the X and the Y axes allow to evaluate the laser position while the different colors represent different pixels. One pixel is colored when there is a commutation

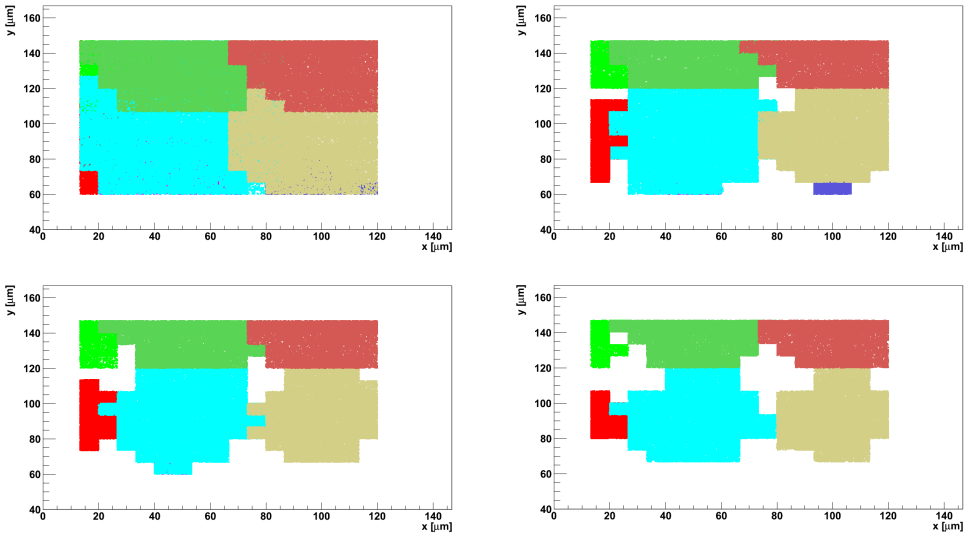

Figure 11.13: Laser test scan result for four different threshold values: $V_{th} = 400\ mV$ (top-left), $V_{th} = 500\ mV$ (top-right), $V_{th} = 550\ mV$ (bottom-left), $V_{th} = 600\ mV$ (bottom-right).

at the output of its discriminator. In Fig. 11.13 it is possible to see that each position of the laser allows to have at least one discriminator flipped for the lowest threshold while, for higher threshold, some positions of the laser do not allow to have discriminators commutations (the white regions clearly visible for a threshold of $V_{th} = 600\ mV$ when the laser is placed between four pixels). Consequently, for low threshold values, the charge generated in the region between four pixels is large enough to have commutations at the output of the discriminators of the pixels surrounding the charge generation point. This does not mean that the depletion region of the pixels reach the region in between four pixels (in fact, the depletion region is identical to that observed in the analog matrix) but it means that the number of the charges generated in the region between four pixels which reach the electrodes is large enough to have commutations on the discriminator. Moreover, it cannot be assumed that, by using the digital read-out matrix it is possible to have a 100% efficiency: in fact, the size of the laser spot is higher than size of a particle track. However, it can be assumed that, by using the digital matrix, a higher efficiency than the analog read-out matrix could be reached.
Due to a graphical limitation, in Fig. 11.13 it is not possible to appreciate the regions covered by the laser which can cause the commutation of more

than one discriminator. This aspect is better shown in Fig. 11.14 where it is possible to see the region covered by the celeste pixel which intersects the regions covered also by the neighboring pixels: the dark-green pixel (top), the violet pixel (bottom), the red and clear-green pixels (on the left). It means that, for some positions of the laser, up to four pixel discriminators can switch at the same time.

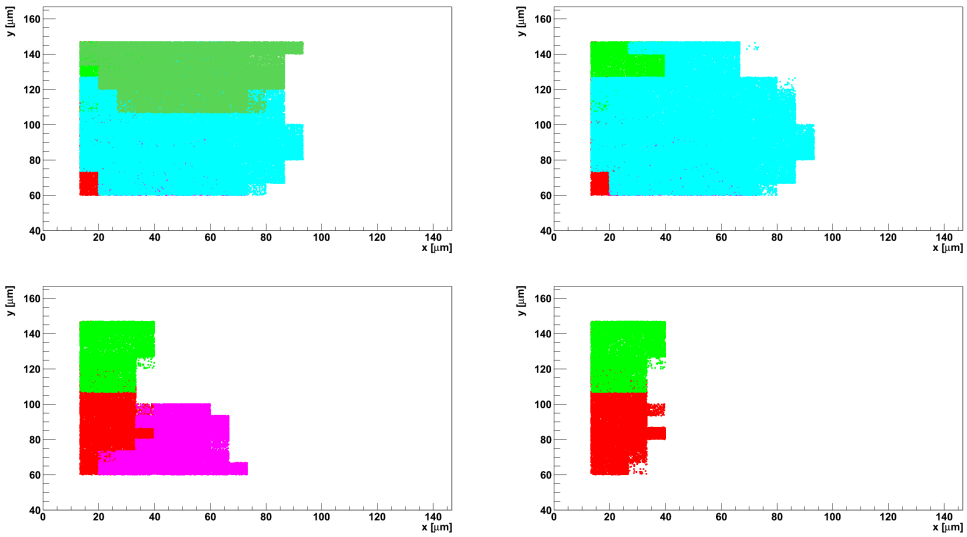

Figure 11.14: Regions covered by different pixels during the laser scan for a threshold voltage of $V_{th} = 400\ mV$.

11.4 X-Ray Source

The digital read-out matrix performance have been tested also by using an X-rays source (^{55}Fe), as already done for the analog read-out matrix. The pixel bias has been optimized only for the first three sectors. One of the advantage of the digital read-out for the first three sectors is represented by the pixel front-end electronics which has only one PMOS source follower. It allows to optimize the bias for both the active and continuous reset parts. In fact, in the analog read-out matrix, the NMOS source follower placed in cascade to the PMOS follower forced to have two different pixel biases for the active and continuous reset part, due to the different bias on the input PMOS transistor caused by the different voltage drop of the reset transistor and the reset diode: the voltage drop of the reset diode does not allow to

have the pixel bias at $V_{dc} \approx 700\ mV$ to avoid to have the NMOS source follower not correctly polarized. In the digital read-out matrix, the first PMOS source follower is AC coupled with the preamplifier: the lack of the NMOS source follower allows to have both the active and continuous reset sectors correctly biased with a value of $V_{dc} \approx 700\ mV$.
The goal of the measurements is to evaluate the number of hits in a preset time-window for a given threshold. It is expected a decreasing number of hits for increasing thresholds up to the point where no more hits are seen due to the high threshold. Moreover, by evaluating the different number of hits for each threshold it could be possible, in principle, to evaluate the threshold step with the largest difference of hits compared to the previous one: the signal caused by the main ^{55}Fe peak should be placed in that threshold interval.
The main constrains in terms of testability are represented by the different discriminator threshold values and the different gain values within the same sector (see Fig. 11.5 and Fig. 11.12): while the former can be overcome by using an off-line threshold correction, the latter cannot be corrected because it cannot be evaluated the gain of each pixel (in fact, only the first and the seventeenth rows are pulsed and allow to evaluate the gain). That constrain represents a strong limitation in terms of statistics because it cannot allow to treat together the information coming from pixels of the same sector but it forces to work at pixel level, studying the decrement of hits for each single pixel. However, by proceeding at the pixel level, a too long time is required to have a significant statistics. Consequently, it has been decided to approximate the gain of pixels of the same sector with the same reset mechanism to be equal, to have the possibility to group pixels of the same sector to increase the statistics, and only a threshold off-line correction has been used.
In Fig.11.15, the ^{55}Fe spectra in terms of number of hits for the sectors having a PMOS input transistor are shown. On the X axis, the voltage difference on the differential pair after the off-line threshold correction is shown while on the Y axis the number of hits is shown. It is possible to see a decreasing number of hits for increasing threshold up to a threshold value (it can be called *max-threshold*) with no more hits. The max-threshold value is higher in the first sector because of the smallest input capacitance. It is also possible to have a rough estimation of the input capacitance. For example,

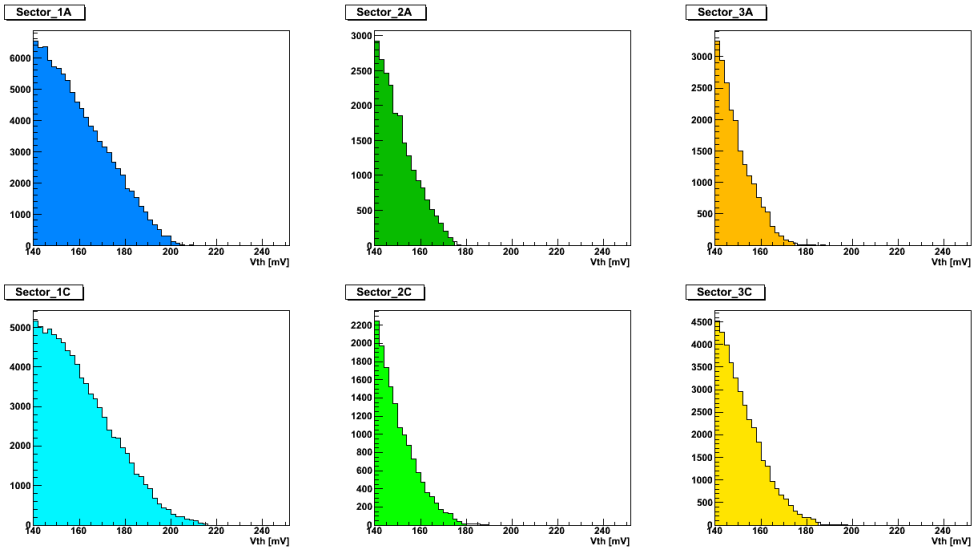

Figure 11.15: ^{55}Fe spectra in terms of number of hits for the sectors having a PMOS input transistor.

in the first sector with active reset, the main peak of the ^{55}Fe source can be supposed to have a voltage amplitude at the input of the discriminator of $V_{sig} \approx 200\ mV$. Considering the gain of the pre-amplifier to be about $G_{pre} \approx 5$ and the gain of the source follower to be about $G_{sf} \approx 0.9$, the signal on the input node of the first PMOS transistor is given by:

$$V_{in} = \frac{200}{5 \cdot 0.9} \approx 44\ mV$$

Consequently, the input capacitance can be estimated to be:

$$C = \frac{Q(5.9\ keV)}{44\ mV} \approx 6\ fF$$

which is not that far from the value obtained by the estimation of the capacitance based on the ^{55}Fe main peak in the analog read-out matrix.

11.5 Conclusions

The digital read-out matrix has been tested. No system failure has been noted during the test phase: the digital read-out approach has shown its potentiality in terms of minimum signal detection which allows to be opti-

mistic in terms of efficiency. The problems related to the impossibility to work with the reset transistor always switched on, the non-homogeneities in discriminator threshold values and in different pre-amplifier gains have not been a show-stopper in evaluating the performance of the read-out electronics. Several measurements are required to define the full potentiality of the digital matrix (in particular measurements after neutron and X-Ray irradiations and measurements in a beam facility) but the preliminary results obtained are encouraging.

Conclusion

A new type of monolithic sensors has been described. The device is based on a commercial deep-submicron CMOS process (90 nm). That technology node offers the possibility to work with high resistivity substrate (above 400 Ωcm), to easily deplete the substrate itself. Moreover, the high density line offered by that technology allows to design a pixels matrix implementing most of the read-out electronics at the periphery and having a single metal line for each pixel connecting it to its own read-out electronics placed at the periphery.

A reverse bias voltage is applied to deplete as much as possible the substrate and collect the charge by drift. Measurements done on the diode structures show the possibility to apply a several tens of $Volts$ reverse bias on the junction reaching a depletion depth around 70 μm. However, current flowing from the sensor edge to the collection electrode through the guard-ring has been noticed for substrate value lower than $V_{sub} = -60\ V$. This current is due to an inversion layer on the silicon-oxide interface in the guard-ring, due to the fixed charge in the oxide and the states at the interface, which causes a parasitic conductive path which connects directly the n-well to the sensor edge.

The inversion layer due to the fixed charge in the oxide and the states at the interface is also present in the breakdown structure which reproduces a small matrix based on a group of inner pixels and a group of outer pixels. Due to the different biases between the inner and the outer pixels and to the inversion layer, an unwanted parasitic current starts to flow between them. Moreover, the inversion layer around the electrode increases also the surface of the electrode itself, causing also a higher capacitance. However, by using an adapt set of biases on the polysilicon layer over the shallow trench isolation and on the metal layer over the oxide, it is possible to isolate the inner

part from the outer current, as shown in the breakdown structure measurements. Only once the central pixels are isolated, it is possible to reduce the substrate bias depleting it.
Matrix prototype measurements show the possibility to work with a detector having a capacitance in a few fF range, with a leakage current of a few pA and an input noise of a few tens of electrons. Infrared laser measurements show an irregular depletion region, due to the set of biases used to remove the inversion layer around the collection electrodes which does not allow a lateral expansion of the depletion layer and, consequently, which limits the detection efficiency of the matrix. However, laser measurements show also an incresing charge collected with the reverse substrate voltage, which demonstrates a charge collection mechanism based on drift. This assumption is also confirmed by the beam test results, where the multiplicity is reduced for a highly biased substrate. Moreover, measurements done with an X-rays source allow to appreciate the interesting performance in terms of peak resolution at room temperature: for a ^{55}Fe X-rays source it has been possible to clearly see both the source peaks at $E_1 = 5.9\ keV$ and $E_2 = 6.49\ keV$. The resistance to total ionizing dose and bulk damage has been also investigated using both the diode-prototype and the matrix-prototype. Even if an increasing leakage current has been noticed in both cases (ionizing and non-ionizing dose), only minor variations have been noticed in terms of collection capacitance for ionizing dose up to 1 $Mrad$ and non-ionizig fluence up to $10^{14}\ n(1MeV)/cm^2$: the results obtained suggest that the detection of minimum ionizing particles should still be possible. Finally, a matrix based on a binary read-out has also been tested: due to the use of a pre-amplifier stage which allows to detect signals generated by a few hundreds of electrons, promising performance results have been obtained in the preliminary test phase activity.
Due to a radical change in the policy of the supplier, the LePix project has been officially interrupted. However, the know-how and most of the men-power have been transferred to a project based on an almost identical approach in a 180 nm CMOS technology which is also used for the upgrade of the $ALICE$ detectors. At the time of writing, a matrix-prototype in a 180 nm CMOS technology has been already produced. In that prototype, several electrode pitches have been used to evaluate the configuration giving the best performance. During a preliminary beam test, interesting results

have been obtained in terms of collection efficiency (close to 100% efficiency), which demonstrate the validity of the LePix approach.

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