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Design of High Dynamic Range Front-End Electronics for Particle Detectors in a $0.13\mu m$ CMOS Technology

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Abstract

PANDA (anti**P**roton **AN**nihilation at **DA**rmstadt) is a fixed target subnuclear experiment. Scheduled for operation in 2018, PANDA will exploit the FAIR accelerator complex, now under construction at GSI, to perform study of the strong interaction in a energy range beetween the non-perturbative and the perturbative regime of the **Q**uantum **C**hromo **D**inamics (QCD). The innovation of PANDA is due to the high luminosity of the incident antiproton beam which allows to have a large number of events recorded by the detector system. The INFN group of Turin is studying the front-end electronic for the Micro Vertex Detector (MVD), which is the detector closest to the interaction point. The sensors used into the MVD will be silicon pixels and double sided silicon strips. The VLSI group of Turin is developing the chip ToPix designed to process the signal coming from the pixel sensors. The Time Over Threshold (ToT) technique will be employed to measure the charge released by the impiging particles over a large dynamic range ($\approx 100\ fC$) and with a low power consumption ($\approx 20\ \mu W$ for pixel). It would be interesting to use the same approach also in the front-end of the strip sensors. In this way, the pixel and the strip subsystems could share the same read-out electronics after the front-end chip. This synergy would lead to a significant reduction in both development time and cost of all the electronics following the front end. Therefore preliminary studies to adapt to the strips the front-end electronics developed for the pixels have been started. The design of an integrated chip is a multistep project which starts with schematics simulations and ends-up with laboratory tests. Several iterations may be necessary before the circuit attains its final performance. Front-end chips for particle detectors are in general mixed mode systems, which incorporate on the same silicon substrate both analog and digital circuits. Their development typically requires 5 to 10 man-years of man power.

This thesis addresses the first steps of such a complex activity, which is the schematic design of the most critical blocks. The work has started from the analysis of the circuit optimized for the pixels. Several modifications were necessary to adapt the existing design to the needs of the strip system.
The chip is designed in a 0.13 μm CMOS technology. The analog part of each channel is made of a first stage which amplifies the signal charge coming from the detector, and a second stage which allows to apply the Time Over Threshold technique to calculate the charge collected by the detector. In its final version, the ASIC will have 128 channels. The voltage supply is 1.2 V and the power consumption per channel is lower than 800 μW.
Chapter 1 of the thesis provides a concise introduction to the PANDA detector, while chapter 2 discusses some general aspects which are relevant for the design of an integrated circuit. The design of the circuit, which is the central topic of this work, is described in chapter 3 to 7.

Contents

Chapter 1

PANDA

PANDA (anti**P**roton **AN**nihilation at DArmstadt) is a subnuclear physics experiment, planned for 2018, which will study the strong interaction in an energy range ($3 - 5\ GeV$) between the non-perturbative and the perturbative regime of the **Q**uantum **C**hromo **D**inamics (Q.C.D.): this becomes possible by studying the interactions between antiprotons and fixed target protons and nuclei in the momentum range of $1.5 - 15\ \frac{GeV}{c}$. Fixed target and collider beams experiments are the main tools useful to study Particle Physics. The most important differences are due to the energy in the center of mass (it is higher in collider beams experiments) and to the number of events after the collision (it is higher in the fixed target experiments because the full cross section of the beam is involved during the collision). The innovation of PANDA, compared to other fixed target experiments, is due to the high luminosity and very good collimation of the incident antiproton beam which allow to have a large number of events and a more accurate statistics. PANDA will built at the F.A.I.R. (**F**acility for **A**ntiproton and **I**on **R**esearch) complex of **G**esellschaft f*ü*r **S**chwer**I**onen-forschung (G.S.I.) located at Darmstadt (Frankfurt) and it will be the result of a collaboration of more then 53 institutes in 16 countries with more than 400 collaborators [1].

Figure 1.1: Layout of the future FAIR complex.

1.1 PANDA Physics Case

In particle physics, hadrons are particles that interact via the strong force. They are made up of two or three quarks, elementary particles and fundamental costituents of matter; there are six types (flavors) of quarks: up, down, charm, strange, top, bottom. Quarks have a property, called *colour charge*, that has no manifestation at distances above the size of the atomic nucleus ($\approx fm$). The colour charge, characteristics of strong interaction, has analogies with the notion of electric charge used in electromagnetic interaction. Due to *colour confinement*, quarks are never found in isolation: they combine to form composite particles called hadrons. The strong colour charge interaction is mediated by the *gluons*, that are equivalent to photons in electromagnetic interaction. The PANDA experiment will study physics of strange and charm quarks in high energy region, with $\bar{p}$ beams with momenta up to 15 $\frac{GeV}{c}$ [4]. The research program will investigate:

- **Gluonic degrees of freedom**: elementary particles of Standard Model earn their mass through the Higgs mechanisms but the mass of non elementary particles is bigger than the sum of the masses of the elementary particles constituting them. For example, the protons

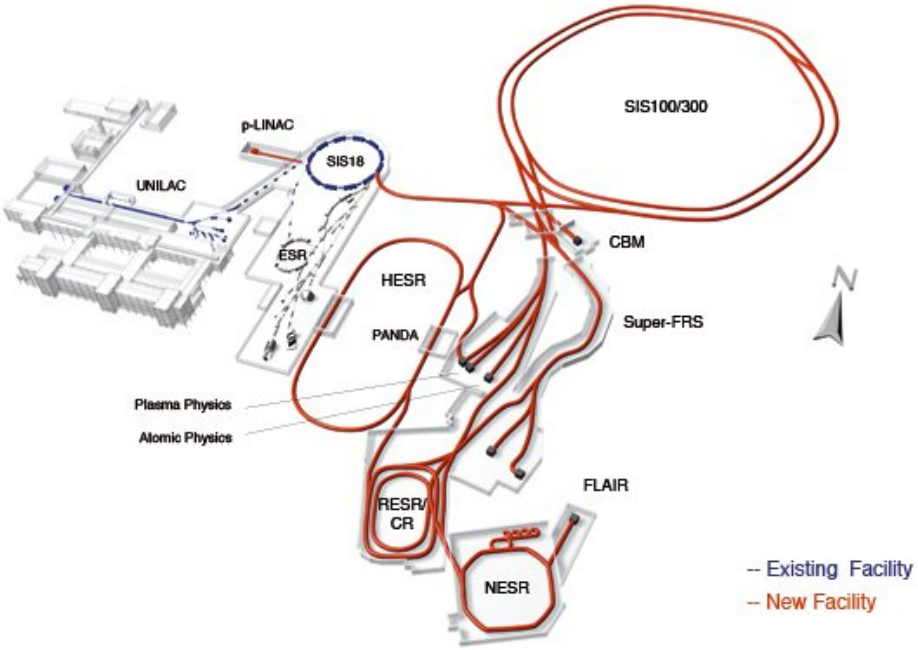

Figure 1.2: Detail of the planned FAIR accelerator complex.

are composed of three quarks (u u d). The mass of the quark up is $\approx 4\ MeV$, the mass of the quark down is $\approx 8\ MeV$ while the mass of the proton is $\approx 1\ GeV$. The difference is due to unknown processes of strong interaction. The possibility to study a whole spectrum of bound states of gluons, called glueballs, might be the key to understand the mass creation in strong interaction.

- **Charmonium spectroscopy**: charmonium is a bound state of charm-anticharm ($c\bar{c}$). Charmonium spectroscopy gives important results in the investigation of the quark-antiquark interaction and antiprotons beams are well suited to do high precision studies. This spectroscopy may reveal important informations about the colour confinement, the mass of the ground state η_c, the existence of first radial excitation of the η_c, the existence of the h_c resonance of the charmonium system, the radiative transition of the χ_j charmonium states, the missing charmonium states above the $D\bar{D}$ threshold.

- **Hypernuclear spectroscopy**: an hypernucleus is an atomic nucleus with one or more hyperons. The goal of hypernucleon physics is to determine the energetic levels and decay properties of hypernuclei. P.A.N.D.A. will particularly study double Λ hypernuclei.
- **Study of properties of hadrons inside nuclear matter**: mass and width modification of adrons in nuclear matter will be investigated in the charm region.
- **Study of the structure of nucleons**: hard exclusive antiproton-proton reactions will be used to study the structure of nucleons and the relevance of certain theoretical models.

The Antiproton Accelerator Complex is constituted by a proton accelerator (SIS100), where 30 GeV protons can be used to produce antiprotons, and a storage ring (HESR), where antiprotons are provided with a momenta between 1.5 and 15 $\frac{GeV}{c}$. The HESR has two ways of working: high luminosity mode (luminosity $\approx 2 \cdot 10^{32} cm^{-2} s^{-1}$, momentum spread $\frac{\delta p}{p} \approx 10^{-4}$) and high resolution mode (luminosity $\approx 10^{31} cm^{-2} s^{-1}$, momentum spread $\frac{\delta p}{p} \approx 10^{-5}$).

1.2 The PANDA Detector

The most important detector requirements are: 4π angle coverage, high rate capability (2×10^7annihilation/s), good particles identification (γ, e, μ,π, K, p) and high momentum resolution ($\approx 1\%$) [3]. The planned detector is divided in two parts: a target spectrometer surrounding the interaction region, subdivided into backward endcap, barrel and endcap, and a forward spectrometer, mounted behind the target spectrometer (Fig. 1.3). Using these spectrometers it is possible a full angular coverage of the spatial region around the interaction point.

1.2.1 Target Spectrometer

The target spectrometer surrounds the interaction point and measures charged tracks for polar angles larger then 22°. It is formed by:

- **Solenoid Magnet**: this is a superconducting solenoid coil with an inner radius of 90 cm and a length of 2.8 m. It provides a maximum

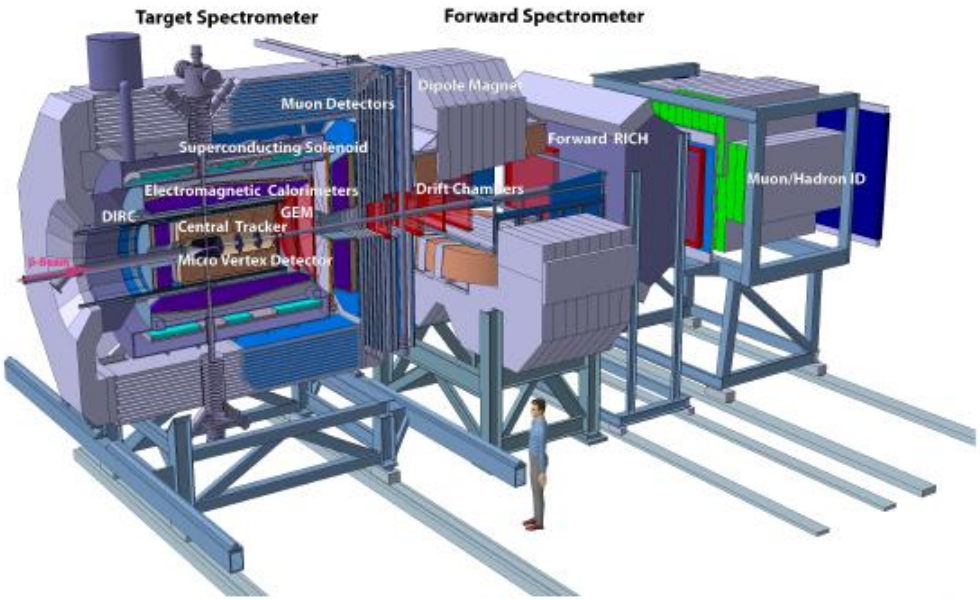

Figure 1.3: Artistic view of PANDA detectors.

magnetic field of 2 T with a homogeneity better than 2% over the volume of the vertex detector and central tracker.

- **Micro Vertex Detector**(MVD): it is based on radiation hard solid state detectors, pixel and microstrip, set next to the interaction point. The design is optimized for the detection of secondary vertices from D and hyperon decays and maximum acceptance close to the interaction point. In the current MVD design, there are two barrels of pixel detectors, two barrels of strip detectors and six disks arranged perpendicularly to the beam pipeline. The inner four layers of the disks are made of pixels, the following two are made of pixels on the inner part and strips on the outer one.

- **Central Tracker**: it is based on a barrel detector surrounding the MVD. It is useful to obtain a good detection efficiency for secondary vertices. There are two methods proposed to achieve the desired detection efficiency. The first one is covering a large area around the MVD with straw tubes (STT) or a time-projection chamber (TPC). The second one, based on three sets of GEM trackers similar to those

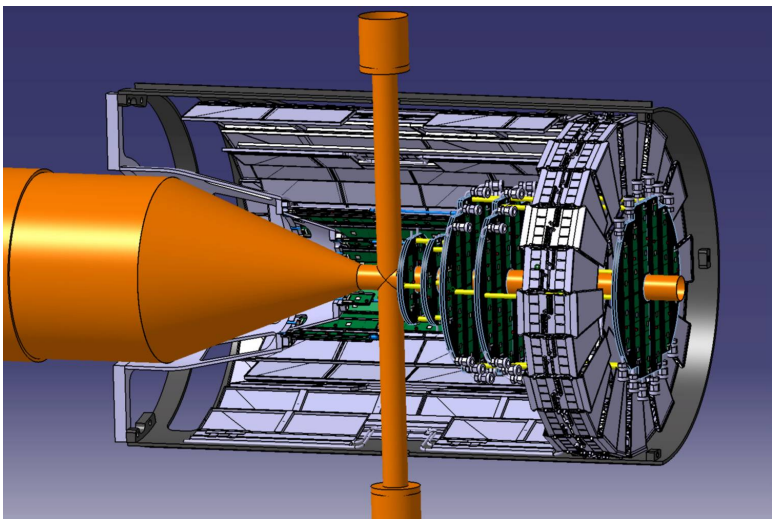

Figure 1.4: The Microvertex Detector of PANDA.

used for the COMPASS experiment, is employed to detect particles emitted at angles below 22° which are not covered fully by STT or TPC.

- **Cherenkov Detectors and Time-of-Flight**: they are used for particle identification. Cherenkov Detectors cover the part of the momentum spectrum above 1 $\frac{GeV}{c}$ while the time-of-flight barrels identify slower particles. In particular, the mass of the detected particles can be determined by combining the information from these barrels with the momentum information from the tracking detector.

- **Electromagnetic Calorimeters**: they are based on lead-tungstate inorganic scintillators. Lead-tungstate is chosen for its good energy resolution in photon, electron and hadron detection, fast response and high density. The EMC is required to cover a large energy range, from a few MeV up to several GeV.

- **Muon Detectors**: they are 72 strips of plastic scintillator counters mounted behind the iron yoke of the target spectrometer (Fig.1.3). In addition, an equal number of strips will be placed perpendicular to the beam axis, at the front of the solenoid magnet.

1.2.2 Forward Spectrometer

The forward spectrometer is used to detect small angle tracks. It is formed by:

- **Dipole Magnetic**: used for momentum analysis of charged particles in forward spectrometer. It covers the entire angular acceptance ($\pm 10^\circ$ in the orizontal direction and $\pm 5^\circ$ in the vertical direction). The maximum bending power, 2 Tm, could deflect an antiproton beam at the maximum momentum of 15 $\frac{GeV}{c}$ by 2.2° from the original track.
- **Forward Trackers**: they are based on a set of wire chambers allowing to track particles with high momenta as well as very low momentum particles. Furthermore, it can be possible to reconstruct tracks in each chamber separately, in case of multi-track events. The expected momentum resolution of the system for 3 $\frac{GeV}{c}$ protons is $\frac{\delta p}{p} = 0.2\%$.
- **Forward Particle Identification**: it is based on a Ring Imaging Cherenkov (RICH) which separes $\pi/K/p$. Two radiators, silica aerogel and C_4F_{10} gas, having two different indices of refraction, makes possible this separation.
- **Forward Electromagnetic Calorimeter**: it is a Shashlyk-type calorimeter with high resolution used to detect photons and electrons. The detector is based on lead-scintillator sandwiches readout with wavelength shifting fibres.
- **Forward Muon Detector**: it is based on 20 vertical strips for muon detection similar to the muon system of target spectrometer.

1.3 Micro Vertex Detector

The INFN microelectronic group of Turin is studying the front-end electronic for the MVD. The key specification for the MVD are:

- **Dynamic Range**: until 2.25 MeV of energy lost in the detectors, corresponding to 625 ke^- (100 fC);
- **Spatial Resolution**: lower than 100 μm;
- **Time Resolution**: about 10 ns (interaction rate $\approx 2 \cdot 10^7$ $\frac{events}{s}$);

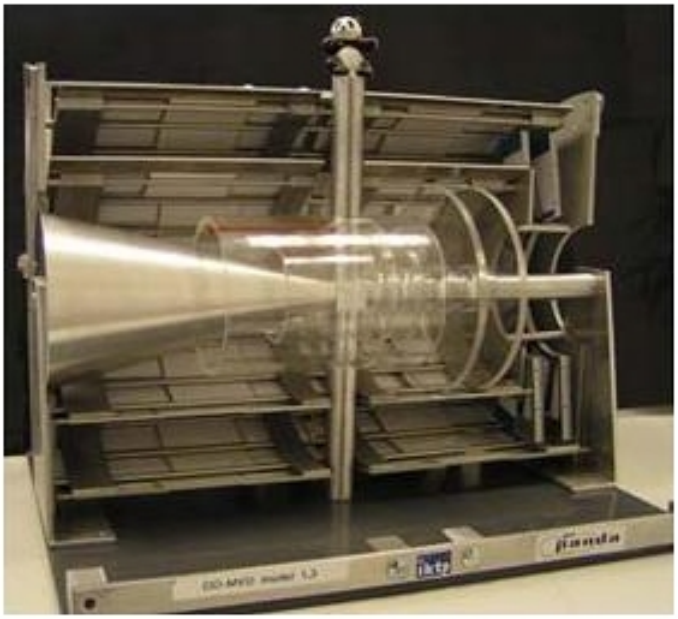

Figure 1.5: First mechanical model of the MVD.

- **Readout Speed**: about 50 $\frac{Gb}{s}$ (the readout system is triggerless and it is based on a FPGA device);
- **Device Thickness**: under 1 mm (1% of radiation length), to be able to detect low momentum particles and to avoid multiple scattering.

The MVD is optimized for the detection of secondary vertices and maximum acceptance close to the interaction point: this region will be surrounded by radiation hard detectors and frontend electronics. The total ionizing dose over 10 years is estimated to be in the order of 1 $Mrad$. A cooling system is necessary to cool the sensors and the electronic systems. The detectors used in the MVD will be silicon pixel detectors and double side silicon strip detectors (DSSD, which reduces the number of readout channels and minimizes the power dissipation). The pixels will be used in the inner part, where the density of particles is higher, and they will have an active area of 100 $\mu m \times 100\ \mu m$. The strips will be used in the outer part, where the density of particles is lower. Since the region closest to the interaction point has a high density of events, the strips cannot be employed.

The DSSD are made by an upper layer of strips arranged in rows and by a lower layer arranged in columns. When a particle hits the detector (Fig. 1.6A), the position of the particle is given by the intersection of the strip of the upper layer and the strip of the lower layer; in this way it is possible to obtain a two dimensional information. When two particles hit the detector at the same time, generating similar signals (Fig. 1.6B), it is more difficult to obtain the exact position of each particle by analyzing the cross points between the upper layer and the lower layer hit because more combinations are possible: the cross points where there is no interaction with the particle hitting are called ghost hits (the blue crosses).
The pixel detectors do not have the ghost hits problem: in a matrix of pixel detector, each element correspond to one only pixel and, consequently, when a particle hits one pixel, there isn't ambiguity about the position of the particle.
The shape used for strip is rectangular, in the barrel part, and trapezoidal, in the disk part. The pitch chosen is 130 μm for rectangular sensors and 70 μm for trapezoidal sensors. The number of events expected for strip detectors is up to several million events per second. There will be 12 million pixel and $200,000$ strip readout channels, leading to a total power dissipation of 4 kW.

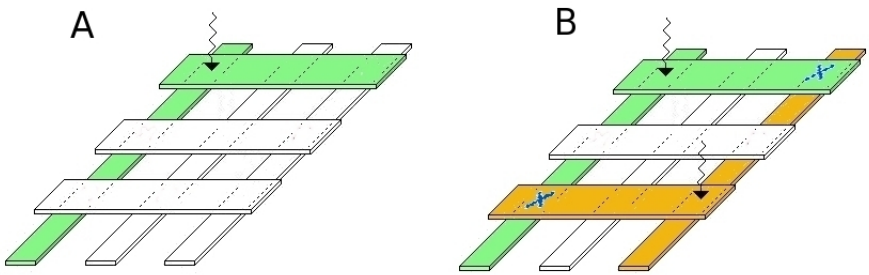

Figure 1.6: The ghost hits problem: the coloured strips represent the strips hit, the blue crosses represent the ghost hits.

Chapter 2

Integrated Circuits

Microelectronic technology has known an impressive development during the last decades. The continuous increase of integration level of microelectronic devices allows to realize more and more complex systems. The design of a new integrated circuit is a process requiring the work of a large number of experts which analyze the specifications, design, produce and test the chip.

2.1 Integrated Circuits

The **Integrated Circuits** (IC) are electronic devices made on the surface of a thin substrate of semiconductor. The integration of a large number of transistors on one chip has two advantages over circuits using discrete components: cost and performance. Cost is low because all components are mounted during the same process, by photolitography, and they aren't constructed one transistor at time so much less material is used. The performance is high because the devices consume less power. The classification of IC is based on the number of transistors and other electronic components per chip:

- **Small Scale Integration** (SSI): up to 100 electronic components per chip;
- **Medium Scale Integration** (MSI): from 100 to $3,000$ electronic components per chip;
- **Large Scale Integration** (LSI): from $3,000$ to $100,000$ electronic components per chip;

- **Very Large Scale Integration** (VLSI): from $100,000$ to $100,000,000$ electronic components per chip;
- **Ultra Large Scale Integration** (ULSI): more than $100,000,000$ electronic components per chip.

The IC are divided into analog, digital and mixed-mode circuits.
The **analog circuits** use signals that are defined over a continuous range of time and a continuous range of amplitudes.
The **digital circuits** use signals that are defined only at discrete values of amplitude. The digital signal is a binary weigthed sum of signals having only two defined values of amplitude (logic level 1 and logic level 0).
The most important differences between analog and digital circuits are shown in the following table:

	Analog	**Digital**
Noise	influential	non influential
Resolution	high	low
Design Difficulty	high	low

Table 2.1: Differences between analog and digital circuit

The **mixed-mode circuits** have both analog and digital circuits on a single semiconductor die. Complementary metal oxide semiconductor (CMOS) technology has been the mainstream in mixed signal implementations because it provides density and power savings on the digital side and a good mix of components for analog design.

2.2 Analog IC Design

An ASIC (**A**pplication **S**pecific **I**ntegrated **C**ircuit) is an integrated circuit fabricated for a particular use. Design *ex novo* allows to optimize the performance, minimizing the space occupied and the power dissipation. In Fig. 2.1 [10] the most important steps during the design are shown.

The designer is responsible for all the steps exclusive of the fabrication. The first step consists in defining the physical context of the design. This

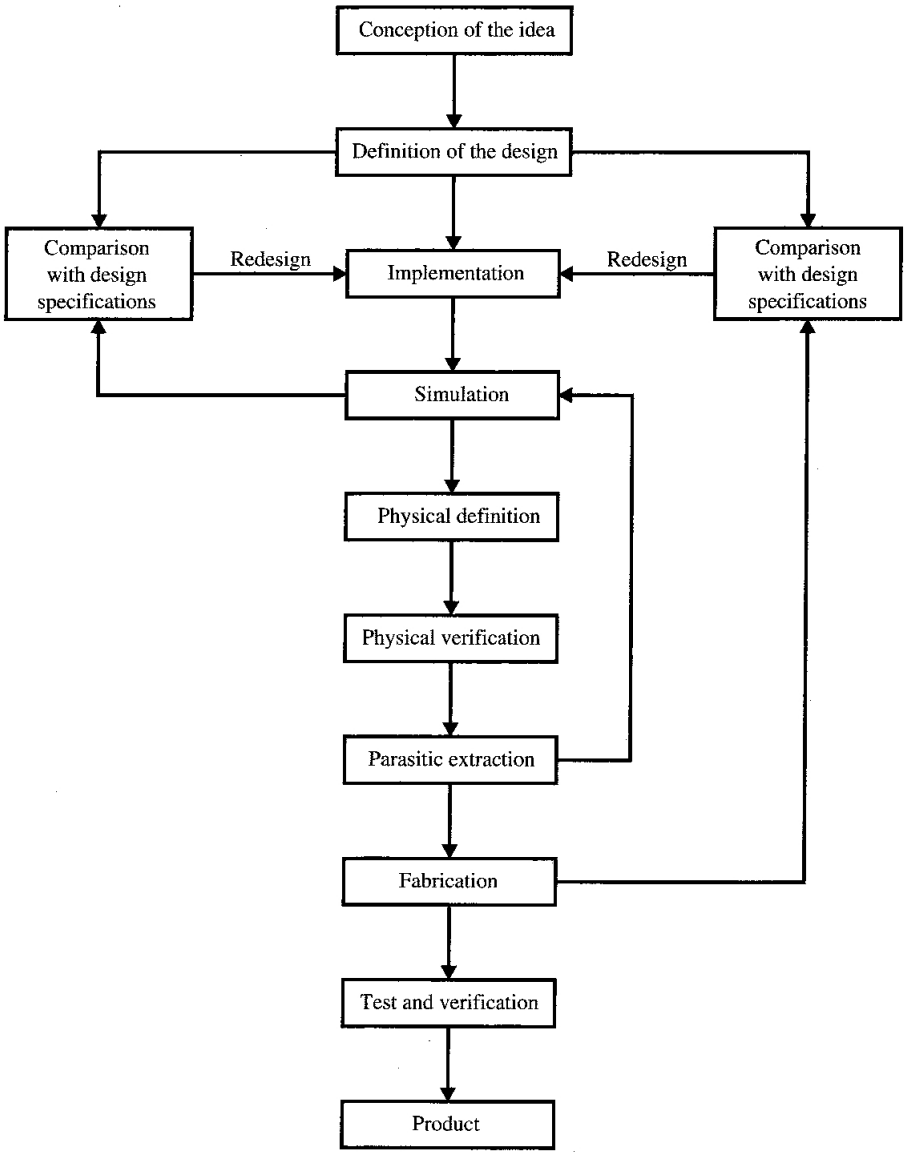

Figure 2.1: Design flow for an analog integrated circuit

step includes the study of the key specifications. When this analysis is concluded, it is necessary to synthesize the circuit: the circuit configurations are decided trying to follow the key specifications. These steps (analysis and synthesis) are fundamental because they determine the performance of the circuit. When these steps are completed, the designer simulates the circuit by CAD to predict the performance of the circuit. The advantages due to the

CAD simulations include the exclusion of the breadboards, the possibility to monitor the signal in any point of the circuit, the possibility to easily modify the circuit. Initially, the designer works only with ideal circuits, disregarding the effect due to noise, process and mismatch errors, temperature variations, etc. In fact, modern CAD offer the possibility to simulate the circuits with or without these variations. Later, the designer addresses the geometrical description of the circuit, also called layout which is closely related to the performance of the circuit (Paragraph 2.3). When the layout is finished, it is necessary to include the layout-related effects in the simulation: if the results are satisfactory, the circuit is ready to be fabricated. After the fabrication, the chip is tested, to ensure that it satisfies the requirements: if the chip stands the test, it is ready for the production. The realization of a chip is a highly reiterative process oriented to find the best solutions. Realization time means the time spent between the conception of the idea and the fabrication (Fig.2.1): it is closely related to the chip complexity and it regards the definition and the simulations of the design (man-power of $\approx 3-4$ man year for mid-complexity chips), the dead-time due to the fabrication ($\approx 3-4$ months), the test and possible improvements (man-power of $\approx 2-3$ man year for mid-complexity chips) and the production time. A mid-complexity chip designed for front-end electronic of Particle Physics experiments usually requires an equivalent man-power of $5-10$ man year.

2.3 Layout

During the layout, the position of each components of the device is chosen. There are several rules to minimize geometrical parasitics effects during the layout. For example, the widths and the lengths of each electrical component have to exceed the minimum value allowed by the technology used, to avoid excessive variation due to fabrication errors; the geometries built must be separated by minimum spacing to avoid short circuits; the n-well (or p-well) has to be enough large to contain the transistors for all expected misalignments during fabrication; some geometries has to extend beyond the edge of the other to ensure proper transistor action at the edges but there are maximum allowable dimensions to avoid litoff problems. The most important techniques used during analog layout to reduce the layout-related problems

are: the use of multifinger transistors, the maximization of symmetries into the circuit, the reference distribution in the current domain rather than in the voltage domain, the use of differential signals to convert the effects of capacitive coupling between various lines to common mode disturbance.

2.4 Processing

The performance of the devices produced in a CMOS technology highly depends on the quality of the wafer used: it has to have a very small number of defects, as unwanted impurities or dislocations. The technique used to obtain high purity wafer is the *Czochralski method*, where a seed of crystalline silicon is immersed in melted silicon and slowly pulled out while rotating. In this way, a single-crystal cylindrical ingot is obtained and then, it is cut into wafers. The wafer is polished and chemically etched to obtain a smooth and clean surface with thickness of approximately 500 to 1000 μm. During the Czochralski process it is possible to dope the melted silicon to obtained a doped wafer, even if the devices producers prefer to dope the silicon after the cut in wafers and by using other techniques, which are explained later, to obtain a more homogeneous doping.
The first step is to isolate the doped wafer surface with a thin (about 150 nm to 2 μm) layer of SiO_2. This is grown at a temperature between 900^oC and 1200^oC in a oxygen atmosphere: the oxygen reacts with the silicon to form the oxide. The addiction of chlorine during oxidation is useful to avoid the formation of unwanted impurities on the surface of the wafer.
When the bulk is covered by the oxide layer, it is possible to open windows of exposed silicon by photolithography. During this process, the oxide layer is covered with a photoresist, a transparent glass mask with opaque regions is placed on the photoresist and the pattern of the opaque region is projected onto the wafer by ultraviolet light. There are two types of photoresist: the negative one which hardens in the area exposed to light and the positive one which hardens in the area not exposed to light.

When the windows are opened, it is possible to selectively introduce the dopants into the wafer by *ion implantation* or *diffusion*. During ion implantation, ionized and accelerated atoms are shot directly into the wafer; the doping level is determined by the intensity and the duration of the implantation and the penetration depth can be adjusted by choosing the energy

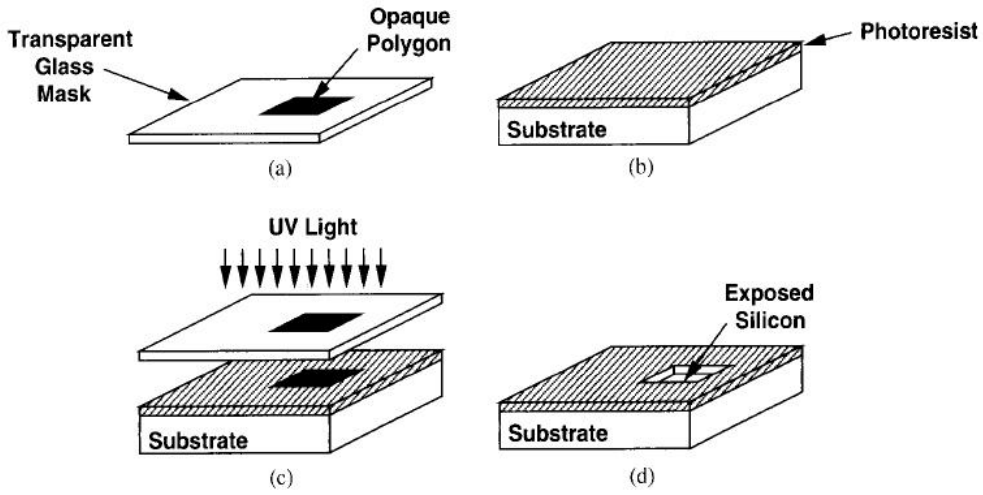

Figure 2.2: (a)The transparent mask with the opaque region, (b)the photoresist placed on the substrate,(c) the exposure to UV light, (d) the window opened after the photolitography [14].

of the ions. Since the implantation damages the silicon lattice, the wafer is heated to $\approx 1000^oC$ for 15 to 30 minutes, allowing the lattice bonds to form again. This operation is called *annealing*. During diffusion, the wafer is placed in a furnace at a temperature of $800 - 1200^oC$ and the dopants are added directly as gas: they diffuse into the silicon because of the concentration gradient. The depth of the doped layer depends on the duration, temperature and surface concentration.

When the doping is finished, the wafer must be metallized to provide a low resistivity connection between several devices on the same silicon substrate or to form bond pads. The first step of the metallization is the silicidation: a thin layer of a highly conductive material covers the doped silicon to reduce its resistance . An oxide spacer is placed on the edges of the gate, to avoid shorts between the gate and the source/drain. After that, the device is covered by a thin layer of oxide with some contact hole created by lithography: the wafer is ready to be covered by a layer of metal (aluminum). This first metal layer is then etched by lithography. A new layer of silicon oxide, or silicon nitride, can be used to cover the metal layer and new windows can be opened in the oxide to create new metal contact levels: in this way, it is

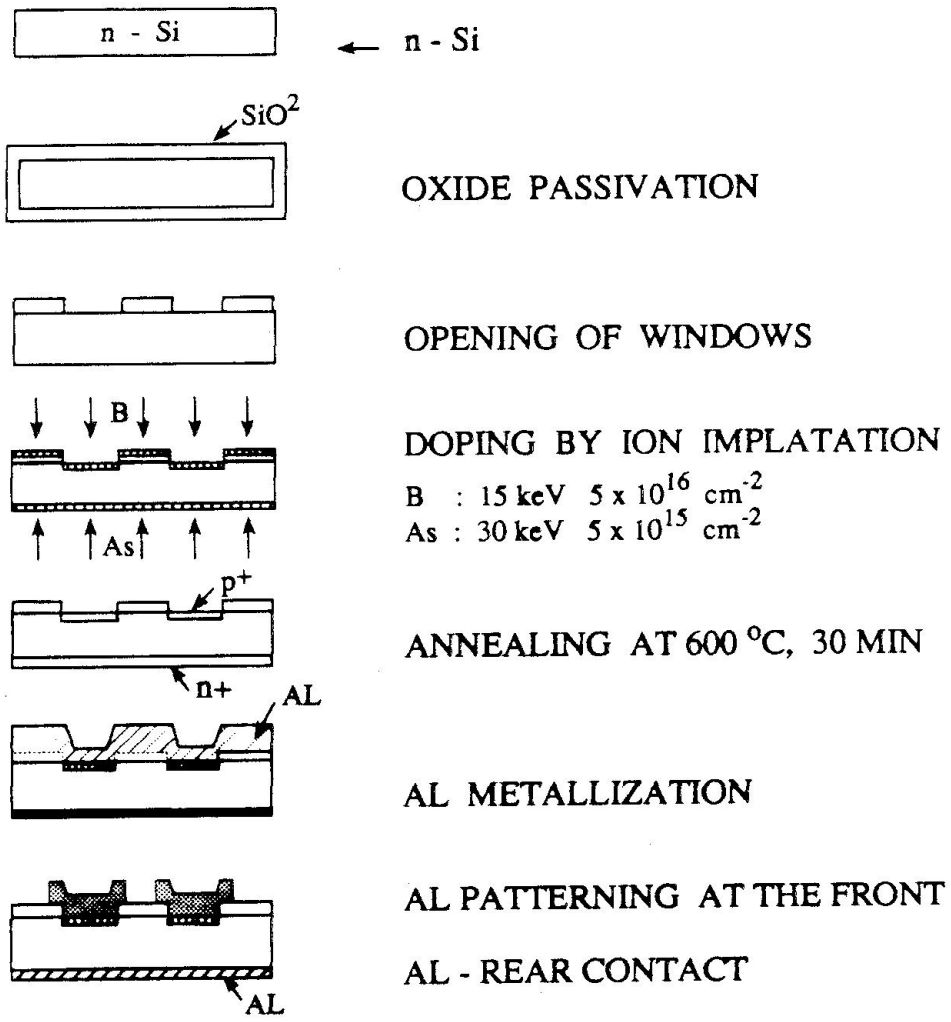

Figure 2.3: The planar process for semiconductor device fabrication.

possible to create new connections between the metal contacts of the first level. When the wanted connections are created, the wafer is ready to be cut.

These types of processing show their influence on the performance of the integrated circuit through the deviations of the device parameters (as doping values or sizes) from their ideal, as-designed values. These deviations are due to *mismatch* and *process variations*. The mismatch causes differ-

ent performance of two or more devices on a single integrated circuit while process variations cause different performance of devices on different integrated circuits. The difference between the real and the ideal value of the circuit parameters is an indipendent random variable with a Gaussian distribution. The unwanted effects due to the deviations can be minimized by a good design; for example, the transistor sizes relative mismatch ($\Delta W/W$ and $\Delta L/L$) decreases when W and L increase their values and the mismatch decreased also when a transistor is divided into many small parallel transistors, because the overall variation ΔL_{eq} is directly proportional to $\Delta L_0/\sqrt{n}$, with ΔL_0 statistical variation of the length and n number of transistors.

2.5 Design Quality

Measuring the design quality allows to improve the chip design. There isn't an universal accepted method to measure the quality of a chip, but the following criteria are considered to be important: testability, yield and reliability.

The **testability** is important to detect chip faults which could cause system failures. The task of chip testing is more and more difficult because of the number of transistors integrated into a single chip increases. The test phase attempts to detect faults in fabrication (e.g.:defects in silicon substrate, photolithographic defects, mask contaminations and scratches, process variations and oxide defects), design (e.g.: shorts, excessive change in threshold voltage, excessive steady state current) and failures due to stressful operating conditions.

The most strict definition of **yield** can be the number of good tested chips divided by the number of chip sites available at the start of the wafer processing. The chip yield can be divided into functional yield (that is obtained by testing the functionality of the chip at a speed lower than the speed required by the chip: it is useful to weed out the problems of shorts, opens and leakage current) and parametric yield (that is obtained by testing the functionality of the chip at the speed required by the chip).

The **reliability** depends on the design and process conditions. The most important causes of chip reliability problems are: electrical overstress, electromigration, oxide breakdown, noise and crosstalk. There isn't an unambiguous solution to solve the reliability problems.

These types of analysis are useful to test digital circuits or mass production circuits (when high tolerances are accepted), while an ASIC requires a more complex analysis, due to the low tolerances: each circuit could be specifically tested according with its goal, checking if it works properly (these further tests could consist in the study of the behaviour of the circuit in the presence of an input signal, or in the study of the noise effects or in the study of circuit behaviour when the temperature changes).

2.6 IC in Particle Detectors

Modern particle detectors, particularly high energy detectors, have a large number of read-out channels. These channels need a fast read-out electronics. Fast, in this context, means circuits able to manage all signals coming from the detector, avoiding to overlap them and avoiding to ignore some signal. The digital clock of the systems usually works at tens of MHz. Furthermore, the features of the front-end electronic have to be high density and low power consumption, to avoid excessive heating of circuits and smaller performance. These features (fast electronics, high density, low power) are satisfied by integrated circuit. The IC have to be optimized according to the detector used and, usually, according to the specific measure: the experiments need ASIC. The ASIC complexity depends on the measure that they have to perform.
The Front-End (FE) electronics stage is a circuit standing between the detector and the electronic system: it converts the charge signal coming from the detector into a signal manageable by digital interface. The classic Front-End consists of a Charge Sensitive Amplifier (CSA) used as preamplifier and a pulse shaper [20].

The preamplifier is usually a current integrator which converts the current pulse coming from the detector into a step pulse with a long decay time. It

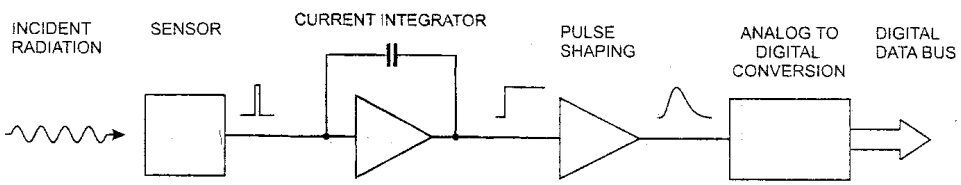

Figure 2.4: Typical AFE

has to amplify the charge signal coming from the detector, since it can be quite small ($\approx 4\ fC$ in a typical high energy tracking detector).
The pulse shaper has to shape the signal coming from the preamplifier introducing the desired decay and rise times through RC high-pass and low-pass filters. These filters have to limit the bandwidth maximizing the signal to noise ratio, since the frequency spectra of the signal and the noise are different.
The continuous amplitude variations at the output of the shaper are converted into discrete steps by an ADC: each step corresponds to a single output bit. Since the power consumption of the ADC is high, it is not usually assembled into the chip and it doesn't process all the signals but it works only when is activated by a trigger.
When no information about the amplitude of the signal but only about the particle transit is required, the FE can be made of an amplifier and a comparator: the comparator voltage output switches when the amplifier voltage output crosses the reference voltage set at the input of the comparator. The power consumption of this FE is lower than the power consumption of the previous FE because only two stages are required. An information with high resolution about the value of the input charge can be obtained even if this FE is used: it is possible by measuring the time between two switchings of the comparator. This is the start point to apply the Time over Threshold technique described in the next chapter.

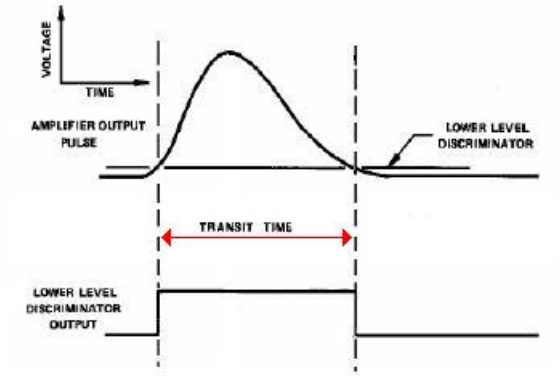

Figure 2.5: The signals at the input and at the output of the comparator.

Chapter 3

Time over Threshold

The microelectronics group of the INFN in Turin is developing the front-end electronics for the pixel sensors of the MVD. In this context first studies on the extension to the strips of the techniques developed for the pixels have been started. The developments are done in a 0.13 μm process which combines low power digital circuits with good analog performance

3.1 Time over Threshold technique

The limits of the classic FE described in the previous chapter are due to the small voltage supply. In fact, the 0.13 μm CMOS technology allows a maximum circuit voltage supply of 1.5 V, in order to prevent the oxide breakdown. Since the voltage output dynamic range is limited, with a high gain of the CSA even a small charge may saturate the preamplifier. An output signal coming from a saturated CSA doesn't reproduce faithfully the input signal.

The Time over Threshold (ToT) technique allows to obtain accurate informations about the charges collected at the input of the amplifier even if it is working in saturation: the physical observable is the time spent by a current constant feedback to discharge the charge collected at the input. The input charge can be calculated by solving the equation:

$$v_{out}(t) = A_v v_{in}(t) = \frac{A_v}{C_{in}} \int_0^t (I_{in} - I_{dis}) dt$$

with

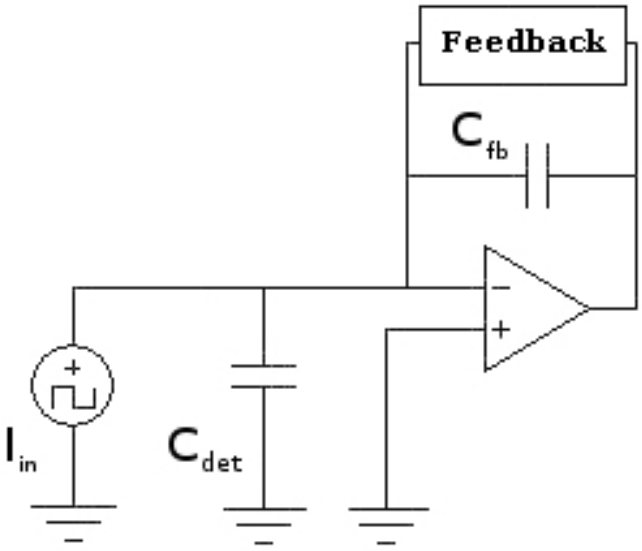

Figure 3.1: Circuit useful to use the ToT technique.

- A_v amplifier gain;
- C_{in} input capacitance[1];
- I_{dis} discharging current.

Since the discharging current is constant, the equation can be re-written as:

$$v_{out}(t) = \frac{A_v}{C_{in}}(\int_0^t I_{in}dt - I_{dis}t)$$

and then:

$$v_{out}(t) = \frac{A_v}{C_{in}}(Q_{in} - I_{dis}t) \tag{3.1}$$

By solving the equation when $v_{out}(t = ToT) = 0$, it is possible to obtain:

$$Q_{in} = I_{dis}ToT \tag{3.2}$$

By knowing the discharging current, the charge collected on the detector can be calculated: the discharging time of the input capacitance doesn't depend on the working point of the amplifier and the relationship between

[1] $C_{in} = C_{det} + C_{Miller}$ with $C_{Miller} = (A_v + 1)C_{fb}$

Q_{in} and ToT is linear even if the amplifier works in saturation.

A circuit using the ToT technique doesn't need an ADC to convert the analog signal into a digital signal. The ToT approach needs a comparator to know when the analog signal is over the threshold and a clock counter, which counts the number of clock cycles between two commutations.
Summarizing, the most important advantages of the ToT technique are:

- Linear relation between ToT and Q_{in};
- Possibility to work even if the amplifier is saturated;
- Simple interface with the digital part of the circuit.

The Time over Threshold technique is reliable if the current supplied by feedback circuit is constant. This situation isn't verified if the transistors which supply the feedback current don't work in saturation region: the relation between ToT and Q_{in} will not be linear. Furthermore, the input node of the charge amplifier isn't a virtual ground because of the saturation of the amplifier: when V_{out} reaches saturation voltage, the input voltage changes significantly. In fact, the input voltage is given by:

$$v_{in} = \frac{Q_{in}}{C_{in}}$$

When the amplifier works in linear region ($A_v \gg 1$ and $(A_v+1)C_{fb} \gg C_{det}$), the input capacitance is given by:

$$C_{in} \approx AC_{fb}$$

and consequently, the input voltage is given by:

$$v_{in} = \frac{Q_{in}}{AC_{fb}}$$

Since $\frac{Q_{in}}{AC_{fb}} \rightarrow 0$, the input voltage variation are negligible and the input node is a virtual ground. When the amplifier works in saturation, the input voltage is given by:

$$v_{in} = \frac{Q_{in}}{C_{det}}$$

Since the relation $\frac{Q_{in}}{C_{det}} \rightarrow 0$ is not valid, the input voltage is no more a virtual ground.

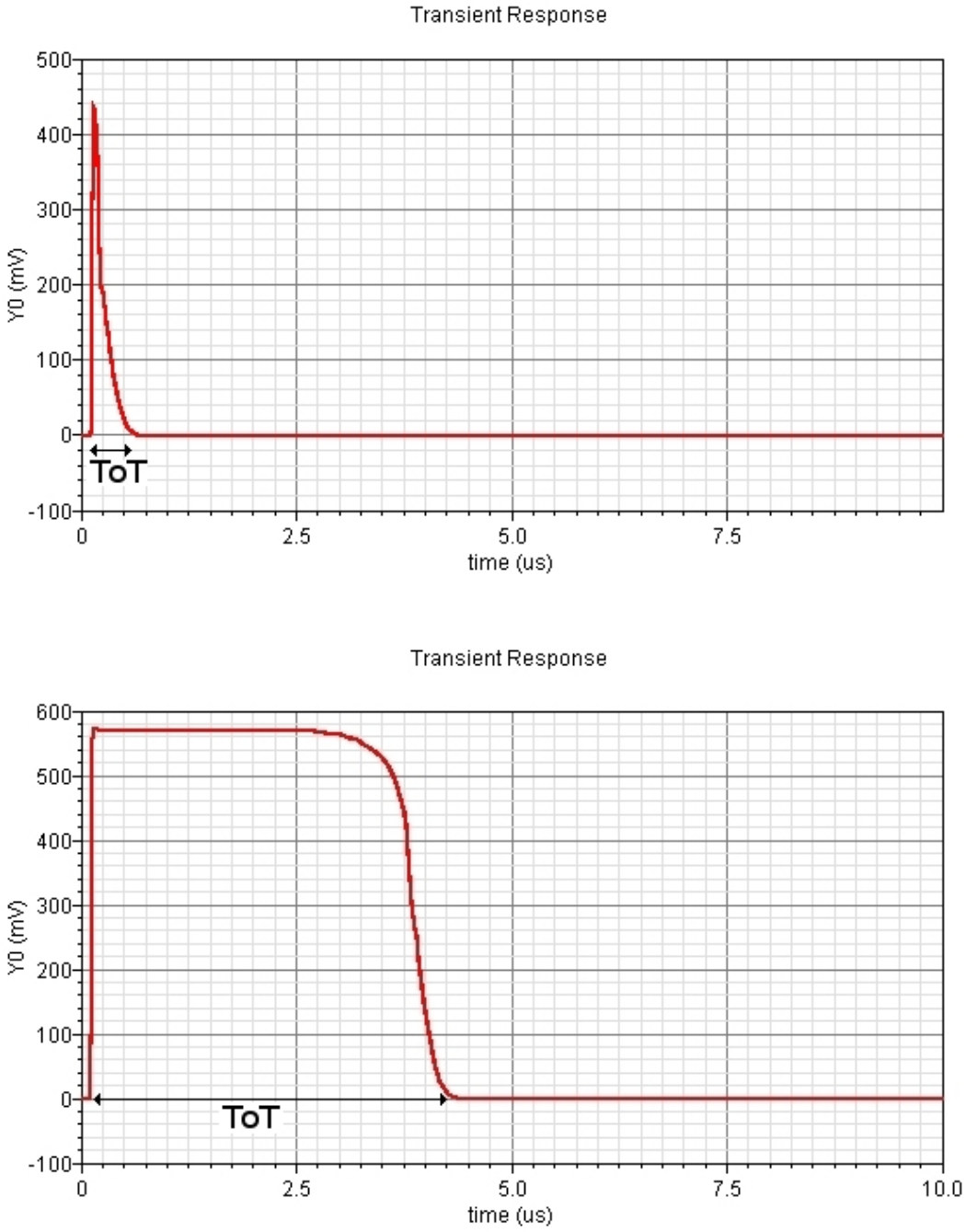

Figure 3.2: An example of ToT output signal when the amplifier works in linear region (up) and in saturation region (bottom).

The most important consequence of the large variation of the input node voltage is an increase of cross-talk.

3.1.1 Cross-Talk

The Cross-Talk is a phenomenon caused by parasitic capacitances of pixel and strip detectors. The most important capacitances in the strip and in the pixel are the backside capacitance and the interstrip, or interpixel, capacitance. The capacitance to backside can be estimated using the formula for a parallel plate capacitor:

$$C = \epsilon_r \epsilon_0 \frac{A}{W}$$

where A is the strip, or pixel, area and W is the thickness of the depletion zone. The interstrip, or interpixel, capacitance is a parasitic capacitance and it can be obtain by analytical calculation. It is proportional to the perimeter of the detector: its value is higher in the strip than in the pixel, because the perimeter of the strip is higher than the perimeter of the pixel. The cross-talk is verified when a charge Q, deposited on one detector ele-

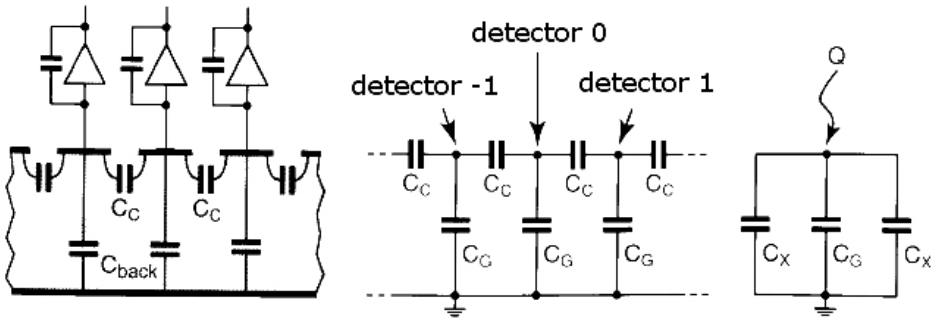

Figure 3.3: Model used for the estimation of cross-talk

ment, induces a signal on its neighbours because of parasitic capacitances. This phenomenon disperses the signal hitting a microstrip to its neighbours. Fig. 3.3 shows a model simplified of strip detectors, which is made by: the backside capacitances, the interstrip capacitances and the feedback capac-

itances [18]. The feedback capacitance of the amplifier can be referred to the input node via the Miller effect. The input capacitance (C_G) is the sum of the Miller capacitance and the backside capacitance. The others capacitances (the network consisting of C_c and C_G) can be grouped together into a unique capacitance C_x. The total capacitance at the input of the amplifier is given by:

$$C_{tot} = C_G + 2C_x$$

The voltage across the input capacitance is:

$$V_{in} = \frac{Q_{in}}{C_{tot}} = \frac{Q_{in}}{C_G + 2C_x}$$

The charge on the capacitance C_G is given by:

$$Q_G = C_G V_{in} = Q_{in} \frac{C_G}{C_G + 2C_x} \tag{3.3}$$

The charge on the capacitance C_{2x} is given by:

$$Q_{2x} = Q_{in} - Q_{in}(\frac{C_G}{C_G + 2C_x}) = Q_{in} \frac{2C_x}{C_G + 2C_x} \tag{3.4}$$

If $C_G \gg C_x$, the hit detector collects all the charge (eq. 3.3): $Q_G \approx Q_{in}$, while the charge collected on the neighbour detectors is negligible (eq. 3.4): $Q_{2x} \approx 0$.
If $C_G \approx C_x$, the hit detector collects a fraction of the charge: $Q_G \approx \frac{Q_{in}}{3}$.
The ToT technique is very susceptible to cross-talk phenomenon because the voltage across the interstrip capacitances changes when the amplifier works in saturation region and it isn't a virtual ground: when this voltage changes, the interstrip capacitance can charges itself and a signal can be generated on the neighbours sensors (Fig.3.4)

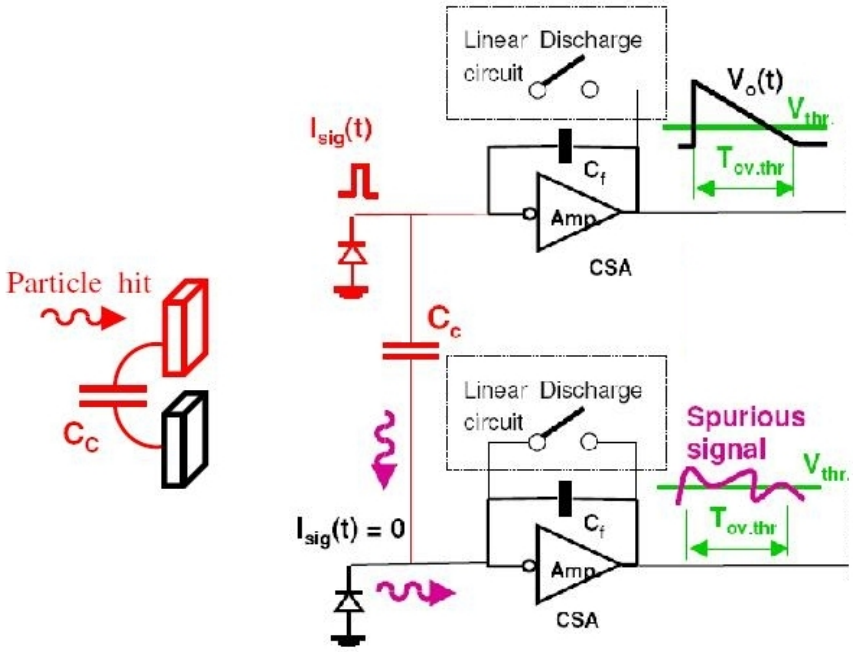

Figure 3.4: The effects of cross-talk.

3.1.2 Noise

Noise is an unwanted random signal characteristic of all electronic circuits [17]. To minimize the noise effects means to find the principal noise source (generally the first stage of the amplifier chain) and to reduce its contribution. The noise performance of a CSA circuit is generally expressed as Equivalent Noise Charge (ENC). The Equivalent Noise Charge is defined as the ratio of the rms noise caused when there is no signal input to the output signal amplitude due to one electron charge [19]. The noise of the detector read out front end can be modelized as a voltage noise generator, as shown in Fig. 3.5. The equivalent input voltage noise generator value is given by:

$$v_{eq}^2 = \frac{8}{3}kT\frac{1}{g_m} + \frac{K_f}{C_{ox}^2 WLf} \tag{3.5}$$

where g_m is the transconductance of the input transistor and K_f is the $1/f$ noise coefficient of the CMOS process used. The first term is due to the thermal noise while the second one is due to the $1/f$ noise. The noise at the

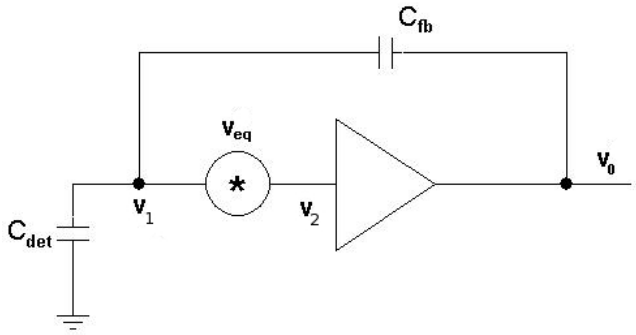

Figure 3.5: The voltage noise source in a detector read-out system.

output of the charge sensitive preamplifier[2] is given by:

$$v_o^2 = \mid (\frac{C_{fb} + C_{det}}{C_{fb}}) \mid^2 v_1^2 \tag{3.6}$$

Since v_1,v_{eq} and v_2 form a loop, the sum of their values must be zero:

$$v_1 = v_2 - v_{eq} \tag{3.7}$$

The output voltage can be re-written as:

$$v_o = A_v v_2 \tag{3.8}$$

with A_v gain of the amplifier. Supposing to have an inverting amplifier ($A_v = -A$), introducing eqn. 3.8 and eqn. 3.6 into eqn. 3.7 yields:

$$v_{eq}^2 = v_1^2 \mid (\frac{1}{A} + \frac{C_{det}}{AC_{fb}} + 1) \mid^2$$

if $A \gg 1$ and $AC_{fb} \gg C_{det}$, since $|v_1| \approx |v_{eq}|$ the output noise can be re-written as:

$$v_o^2 = \mid (\frac{C_{fb} + C_{det}}{C_{fb}}) \mid^2 v_{eq}^2$$

Since the output voltage due to one electron is given by:

$$v_{o,q} = \frac{q}{C_{fb}}$$

[2]The parasitics capacitances and the leakage current has been neglected

the value of the ENC can be calculated:

$$ENC^2 = \frac{v_o^2}{v_{o,q}^2} = \frac{(C_{det} + C_{fb})^2}{C_{fb}^2} \frac{C_{fb}^2}{(q)^2} v_{eq}^2 \tag{3.9}$$

Since $C_{det} \gg C_{fb}$, the ENC can be re-written as:

$$ENC^2 = \underbrace{\frac{C_{det}^2}{g_m} \frac{8kT}{3(q)^2}}_{ENC_{th}^2} + \underbrace{\frac{C_{det}^2 K_f}{C_{ox}^2 WLf(q)^2}}_{ENC_{1/f}^2}$$

The thermal noise contribution is proportional to the ratio of the detector capacitance to the square root of the transconductance of the input MOS transistor of the amplifier ($ENC_{th} \propto \frac{C_{det}}{\sqrt{g_m}}$). The noise due to the capacitance of the detector sets a restriction to the total noise of the system. The thermal noise can be decreased by increasing the tranconductance gain (g_m): a good solution to increase the transconductance of a MOSFET transistor is to have it working in weak-inversion because its transconductance is directly proportional to I_{ds} (when a transistor works in strong-inversion, its transconductance is proportional to $\sqrt{I_{ds}}$). By using transistors working in weak-inversion, it is possible to have a good signal to noise ratio without to have excessive power consumption.
The $1/f$ noise contribution is proportional to the ratio of the detector capacitance to the square root of the transistor area ($ENC_{th} \propto \frac{C_{det}}{\sqrt{WL}}$), so it can be decreased by using larger transistor.
Since noise has a Gaussian distribution, the error due to noise in the ToT measures also has a Gaussian distribution and its standard deviation is commonly called *jitter*.

The slope of the output voltage has a constant value imposed by the constant discharging current. Consequently, by knowing the standard deviation of the output voltage (which is the rms noise) and the value of the discharging current, the jitter value can be calculated. In fact:

$$v_{out}(t) = \alpha t$$

with

$$\alpha = \frac{dv_{out}}{dt}$$

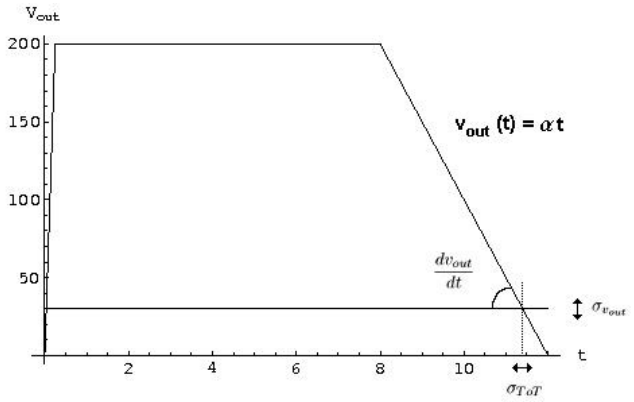

Figure 3.6: The influences of the rms voltage noise ($\sigma_{v_{out}}$) on the jitter (σ_{ToT}).

imposed by the constant discharging current. Consequently:

$$\sigma_{v_{out}} = rms_{noise} = \frac{dv_{out}}{dt}\sigma_{ToT}$$

and

$$\sigma_{ToT} = jitter = \frac{rms_{noise}}{\frac{dv_{out}}{dt}}$$

The jitter value can be minimized by decreasing the rms noise of the circuit or by increasing the constant discharging current (and consequently, increasing $\frac{dv_{out}}{dt}$).

3.2 Atom and FEI3

The Time over Threshold technique is frequently used in the integrated circuits for particle detectors. The first one who introduced this technique was Nygren. Atom [21] and FEI3 [22] are two examples of read out chips which use the ToT technique respectively in BaBar and ATLAS. The main features of these circuits are shown in Tab. 3.1.

- **Atom** processes the signal coming from strip detectors. It is made by 128 channels which process in parallel the signals coming from 128 strip detectors. The analog stage of the circuit is made by a preamplifier, a shaper and a comparator. The preamplifier is a common source

	Atom	FEI3
Detector	microstrip	pixel
Minimum input charge	$\approx 1fC$	$\approx 1fC$
Power consumption per channel	$3.5mW$	$40\mu W$
Voltage supply	$2V or 5V$	$1.6V$
Process Technology	$0.8\mu m$	$0.25\mu m$

Table 3.1: Atom and FEI3 main features.

high gain cascode with a capacitive feedback. the shaper is made by three RC filters: two RC integrators and 1 CR differentiator. The output signal is semi-Gaussian shaped. The signal coming from the preamplifier is presented to a comparator with a preset threshold: it is made by a simple operational amplifier with mild AC positive feedback which limits the effects of the hysteresis loop on the ToT measures. The comparator output is sampled at a 15 MHz rate. Streams of pulses are written during a ToT interval and the number of ones in the stream gives the digital value of the ToT.

- **FEI3** processes the signal coming from pixel detectors. It is made by 2880 read out cells (50 μm $\times$ 400 μm) arranged in a 18×160 matrix. The analog stage of the circuit is made by a charge sensitive amplifier, a leakage current compensation circuit and a comparator. The charge sensitive amplifier is a high-gain folded cascode with a capacitive feedback. The leakage current compensation circuit is a feedback circuit which injects current at the input node to avoid the problems caused by the dark current coming from the detector. The output of the charge sensitive amplifier is DC coupled to a comparator. The output signal of the comparator is analyzed by the digital circuit which samples the input signal at a 40 MHz rate.

3.3 ToPix 2.0

ToPix 2.0 is a prototype chip of pixel read-out for the pixel detector of the PANDA experiment [23]. It follows the key specifications of the PANDA MVD pixel detector and front-end electronics: pixel sizes of 100×100 μm^2, large dynamic range and triggerless read-out. It is designed using a 0.13 μm technology, its total area is 5×2 mm^2 and its power consumption is 15 μW

per pixel for a 1.2 V power supply. It uses the ToT technique. It can work with signals of either polarity. It is made of 320 pixel cells organized in two columns with 128 cells each and two test columns with 32 cells. Each pixel contains the full analog chain and the digital registers for local data storage (Fig.3.8).

The analog stage of ToPix 2.0 is composed by a preamplifier and a comparator (Fig.3.9). The preamplifier is a low noise circuit with a feedback capacitance ($C_{fb} = 24\ fF$), a constant current discharge circuit (to be able to use ToT technique) and a detector leakage current compensation circuit (to eliminate the dark current). The discriminator compares the analog output of preamplifier with a threshold voltage. The digital stage of the circuit measures the clock cycles during the time over threshold. Each pixel contains a digital logic which receives at the input the timestamp bus, the address bus and the output of the comparator. There are three 12 bits shift registers: the first one stores the value of the timestamp bus when the comparator output switches from 0 V to 1.2 V (leading edge register); the second one stores the value of the timestamp bus when the comparator output switches from 1.2 V to 0 V (falling edge register); the last one stores

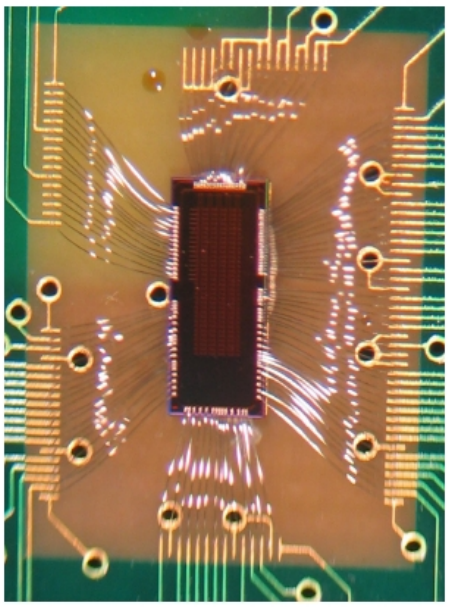

Figure 3.7: ToPix 2.0 chip

the values of the configuration bits (configuration register). The time stamp value in the leading edge register gives the timing information, while the difference between leading and trailing edge time stamps gives the amplitude information. The position of the hit pixel is given by the bits of the address bus.

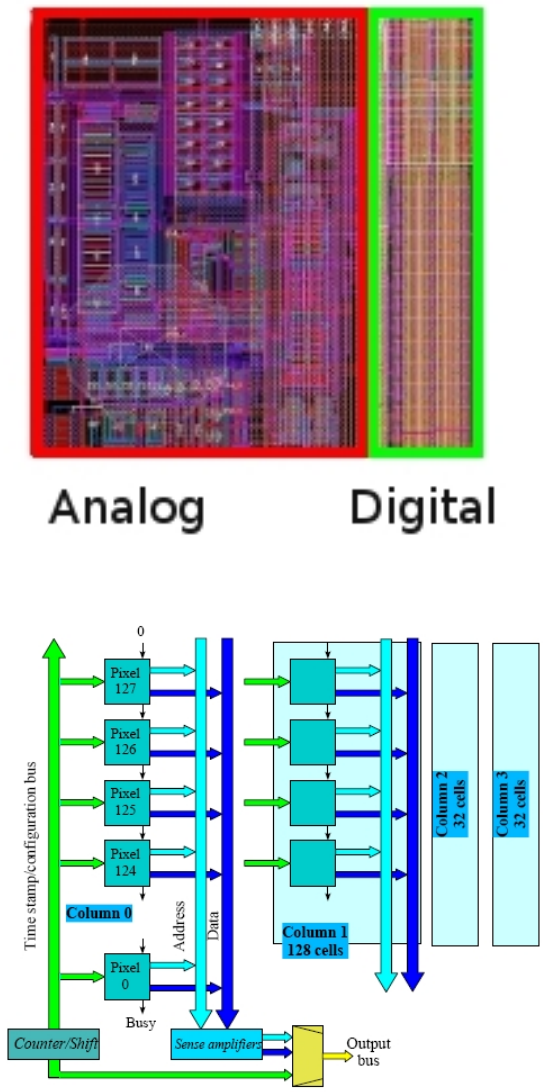

Figure 3.8: Analog and Digital part of ToPix 2.0 (up) and its diagram (bottom)

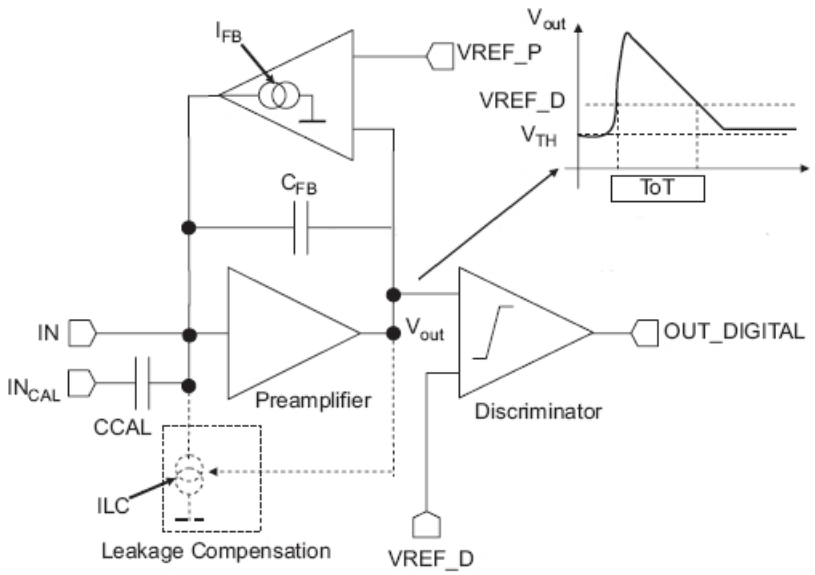

Figure 3.9: ToPix 2.0 analog circuit

The digital signal is then sent to a read-out logic that sends the data for external use by means of an output bus.

3.4 ToT for Strip Readout

The microelectronic group of INFN of Turin is also studying new solutions to apply to the front-end electronic of double sided microstrip detectors. The fundamental idea consists in using the same electronic data acquisition apparatus used for pixel detector modifying the frontend chip, changing only the chip between the detector and the remaining electronics: ToPix 2.0 will be replaced with another chip designed to read a signal coming from strip detector. The most important differences to consider during the design of the strip front-end chip are:

- the dimensions of the strip and of the pixel detectors are different. In Fig.3.10 the dimensions of the three types of strip sensors are shown.
- the capacitance of strip sensor is higher than the input capacitance of pixel ($C_{pixel} = 200\ fF$,$C_{strip} = 10 - 20\ pF$);

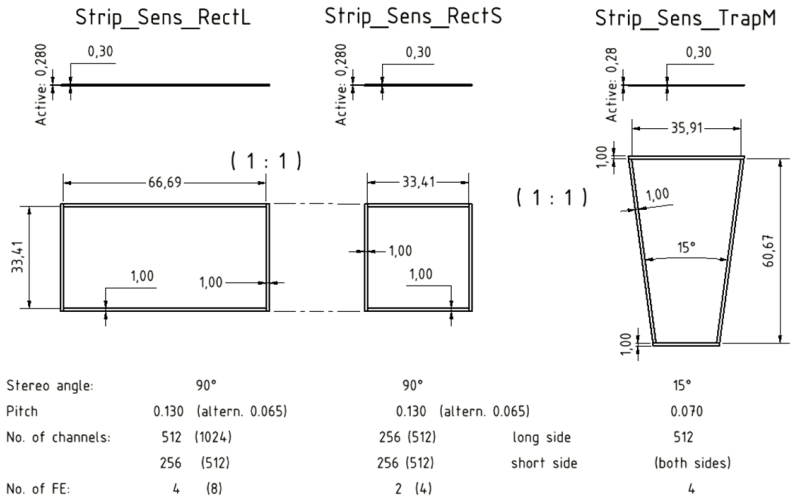

Figure 3.10: Sensor dimensions for the DSSD part of the MVD.

- the number of elementary sensor cells used to cover a per unit area $(n \times n)$ is higher than the number of strips used to cover the same area $(2n)$. Consequently, the number of read-out channels is higher in pixel detectors;

- the sizes of the electronics chips are different. In fact, since the pixel chip is directly assembled on the sensor, there must be exact matching between the size of the pixel cell and the size of the corresponding front-end electronics channel. The strip detector chip is not directly assembled on the strip and, consequently, the form factor of the electronic channel is not strictly bound by the strip size;

- the power consumption per channel of the strip chip is higher than the power consumption per channel of the pixel chip but the power consumption per unit area is lower in strip detectors. In fact the typical power consumption per channel in strip frontend chip is ≈ 3 mW while the typical power consumption per channel in pixel chip is ≈ 20 μW. Supposing to have a 10 $cm \times 10$ cm area and supposing the strips sizes to be 100 $\mu m \times 10$ cm and the pixel sizes to be 100 $\mu m \times 100$ μm. The strips number required to cover the area is $2 \cdot 10^3$ (the factor 2 is due to the double sided strip detector) while the pixels number is 10^6. Consequently, the overall power consumption of the strip read-out system is 6 W and the power consumption per unit area

is 60 mW/cm^2 while the overall power consumption of the pixel is 20 W and the power consumption per unit area is 200 mW/cm^2;

- the interstrip capacitance is higher than the interpixel capacitance.

The analog part of the new chip is divided in two mainblocks: a preamplifier (Chapt. 4), which amplifies the detector charge, and a ToT stage (Chapt. 5), which uses the ToT technique. The voltage supplied is always 1.2 V.

Chapter 4

Preamplifier

The preamplifier is the first stage of the processing chain. In a well-optimized system, this circuit should give the dominant contribution to the noise. Furthermore the preamplifier, which is directly connected to the strip sensor, plays a key role in defining the cross-talk performance.

4.1 Cross-Talk Reduction

The preamplifier employs the standard topology consisting of a charge integrator followed by a pole-zero cancellation network. The overall circuit can be seen as a current amplifier. The most important features of this circuit are the low input resistance ($R_{in} \rightarrow 0$) and the high output resistance ($R_{out} \rightarrow \infty$). The low input resistance allow to have no voltage variation even if a current variation is present at the input: the Ohm law ($V = RI$) shows that when a current variation arrives at the input, the voltage variation is negligible when the input resistance approaches zero. The input node of each preamplifier becomes a virtual ground. The interstrip capacitance, which is the cause of the cross-talk, can't be charged because the variation of voltage at the both ends is zero. The cross-talk becomes then negligible (Fig. 4.1).

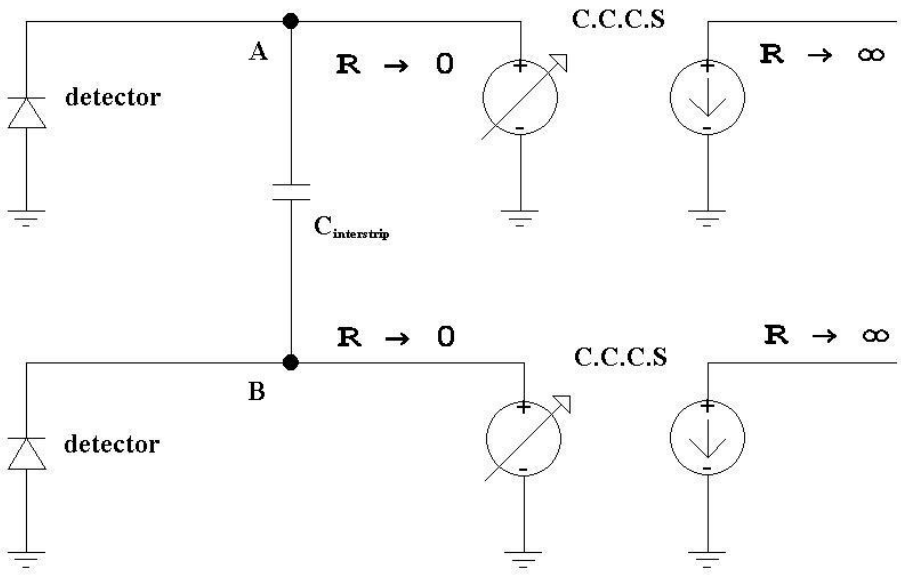

Figure 4.1: The figure shows the detectors, the interstrip capacitance and the Current Controlled Current Source (C.C.C.S.) representing the preamplifier, with its low input resistance and its high output resistance. The input nodes (A and B) are virtual grounds.

4.2 Detector Equivalent Model

The detector equivalent model is made of a current generator, which simulates the current pulse due to the particle hit, and a capacitance for the detector capacitance ($C_{det} = 20\ pF$).

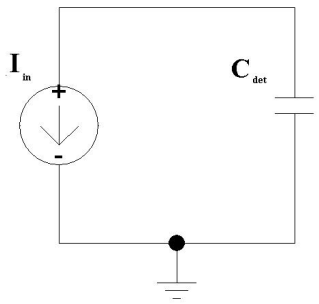

Figure 4.2: Detector equivalent model.

When a particle hits the strip active region, it creates electron-hole pairs,

losing its energy. Supposing the detector as a capacitor, when the charge q is placed in the middle of the capacitor, it induces an opposite charge on the inner side of the plates.

The current is given by the time rate of change of charge on one plate. The drift velocity of the semiconductor is given by:

$$\vec{v_d} = \mu\vec{E}$$

where μ is the charge mobility and $\vec{E}$ is given by:

$$\vec{E} = qN_{D,A}\frac{x}{\epsilon}$$

with x position of the charge created, $N_{D,A}$ concentration of donors (acceptors) and ϵ semiconductor dielectric constant. Then

$$v_d = \frac{x\mu qN_{D,A}}{\epsilon} = \frac{x}{\tau}$$

We can also write

$$v = \frac{dx}{dt}$$

And so

$$\frac{dx}{dt} = \frac{x}{\tau}$$

$$x(t) = x_0 e^{-\frac{t}{\tau}}$$

$$v(t) = x_0\frac{e^{-\frac{t}{\tau}}}{\tau}$$

The current can be written as:

$$I = \frac{q}{t} = \frac{q}{\frac{d}{v}}$$

with d plates distance. Therefore:

$$I(t) = \frac{q}{d}\frac{x_0}{\tau}e^{-\frac{t}{\tau}}$$

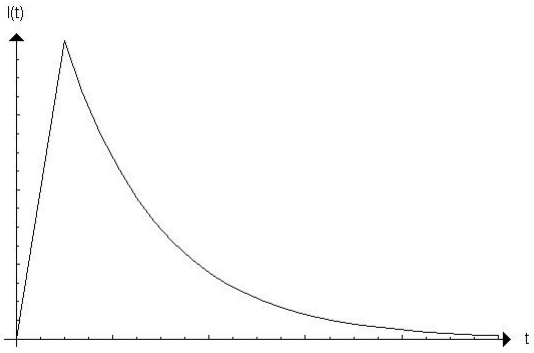

Figure 4.3: The input signal.

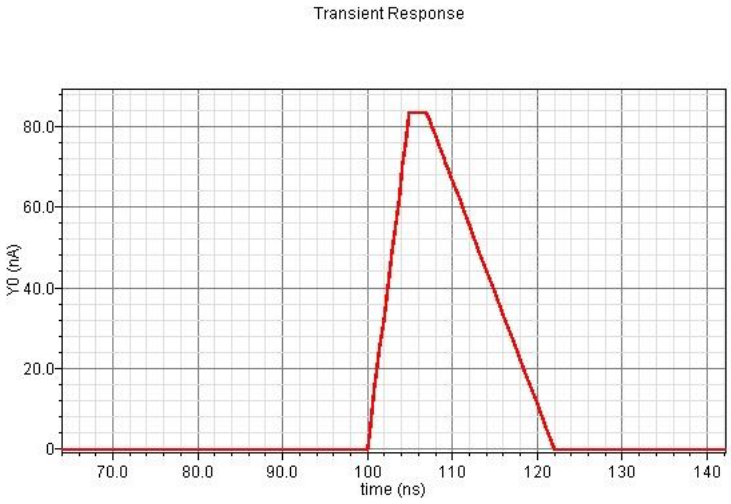

Figure 4.4: Input signal used in the simulation to approximate the detector signal.

4.3 Integration Stage

The integration stage integrates the charge signal coming from the detector. It is made by a high gain voltage amplifier with a capacitive feedback. The capacitor collects the charges coming from the detector. The close loop gain of the amplifier is inversely proportional to the feedback capacitance. In fact, the consequences of the Miller effect are that the feedback capacitance (C_{fb}) contributes to input capacitance as $C_{fb}(A+1)$. The closed loop gain

is given by:

$$v_{out} = Av_{in}$$

$$v_{out} = A\frac{Q_{in}}{C_{in}}$$

$$v_{out} = A\frac{Q_{in}}{C_{det} + C_{fb}(A+1)}$$

If $C_{fb}(A+1) \gg C_{det}$ and $A \gg 1$

$$v_{out} \approx A\frac{Q_{in}}{AC_{fb}}$$

$$v_{out} \approx \frac{Q_{in}}{C_{fb}}$$

$$G = \frac{v_{out}}{Q_{in}} = \frac{1}{C_{fb}}$$

with G closed loop gain. Since the capacitance has to be discharged, to avoid to have the integrator saturated, a resistor has to be connected in parallel with it. This resistor is necessary also to establish a DC feedback to allows to have the amplifier opportunely polarized. It has to be not too small to avoid an excessive noise but a large resistance causes the pile-up between two successive pulses . The pile-up can be ameliorated by using a derivator stage which allows the output of the integrator to return to the baseline before the second pulse arrives.
The integration stage is made by a cascode amplifier and a source follower. The cascode amplifier has a high open loop gain and an high output impedance. In Fig.4.5 the configuration of cascode used in the preamplifier is showed.

By knowing the output impedance of the circuit, one can easily calculate the open-loop gain. In Fig. 4.6 the circuit used to study the output impedance of the cascode stage is showed while the small signal model is reported in Fig 4.7.

The output impedance is given by solving the equation at node D_1:

$$\frac{v_{01}}{r_{01}} + g_{m2}v_{01} + \frac{v_{01} - v_x}{r_{02}} + g_{mb2}v_{01} = 0$$

And then:

$$v_x = \frac{v_{01}}{r_{01}}\left[r_{01} + r_{02} + r_{01}r_{02}(g_{m2} + g_{b2})\right]$$

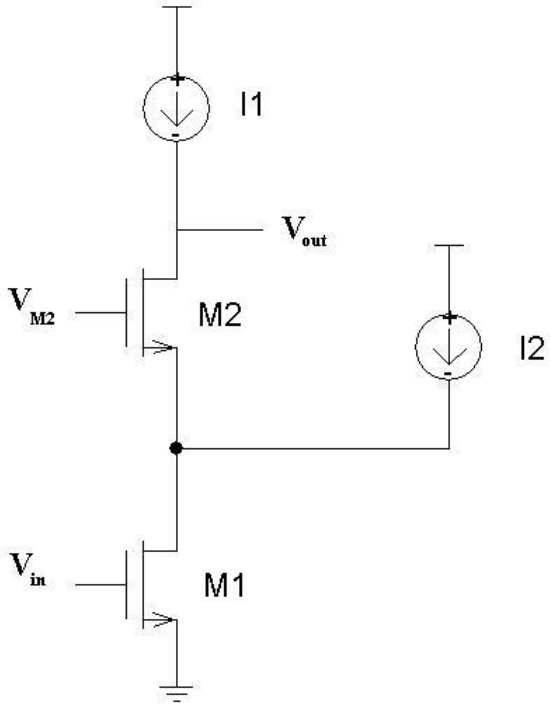

Figure 4.5: Diagram of cascode.

The current I_x is given by:

$$I_x = \frac{v_{01}}{r_{01}}$$

The output impedance of the circuit is given by:

$$Z_{x,nmos} = \frac{v_x}{I_x} = r_{01} + r_{02} + r_{01}r_{02}(g_{m2} + g_{b2}) \tag{4.1}$$

The circuit used to implement the current source $I1$ has to have a high output impedance. In fact, the current supplied from an ideal current source doesn't depend on the variation of the output voltage:

$$\frac{dI}{dV} \to 0$$

and then $R \to \infty$. The circuit chosen to implement the current source is p-mos type current mirror with cascode. The output impedance of a p-mos cascode is the same of the n-mos cascode. The output impedance of the overall amplifier is given by the parallel combination of the impedance of

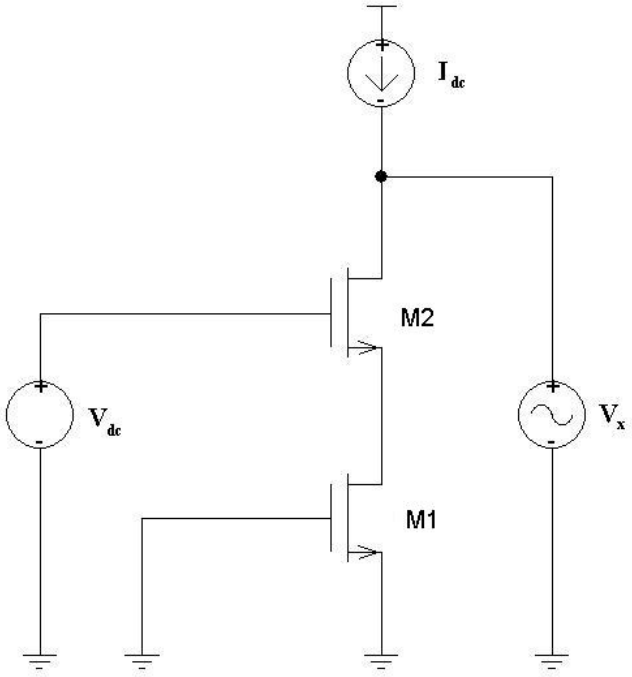

Figure 4.6: Circuit used to study the output impedance of the cascode stage.

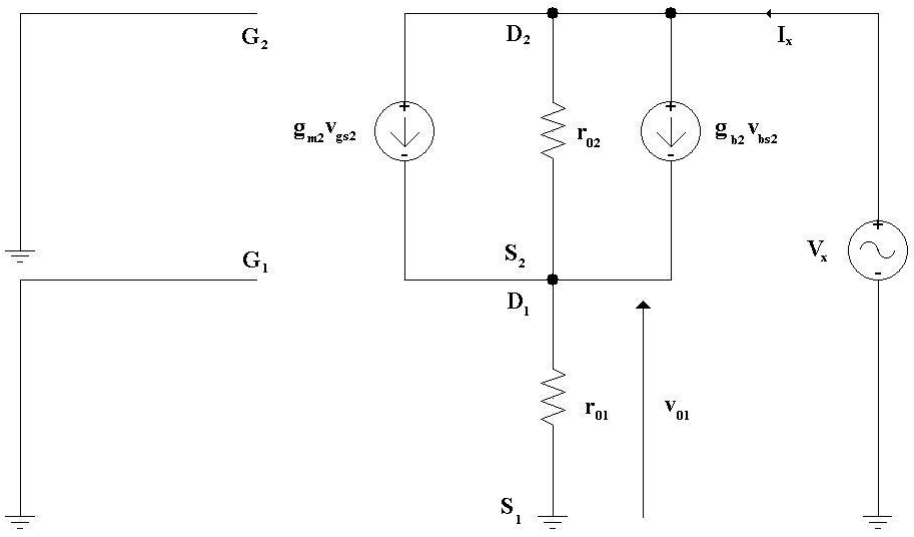

Figure 4.7: Cascode small signal model.

the n-type cascode and p-type cascode:

$$Z_{tot} = [r_{01} + r_{02} + r_{01}r_{02}(g_{m2} + g_{b2})] \parallel [r_{03} + r_{04} + r_{03}r_{04}(g_{m3} + g_{b3})] \tag{4.2}$$

The output impedance has been calculated by simulating the circuit shown in Fig.4.6, calculating the voltage to current ratio at the input of V_x by the CAD. A second way to calculate the output impedance consists in substituting the transistors parameters, given by the CAD, in the small signal model (eq.4.2). In the first case the result is $Z_x = 578\ k\Omega$ and in the second one it is $Z_x = 459\ k\Omega$. The second value is less accurate because it is the result of an approximation (small signal model). The open loop gain of the cascode configuration is given by:

$$A_v = g_{m1}Z_{tot} = 728 \tag{4.3}$$

with g_{m1} transconductance of $M1$. The cascode configuration and the sizes of all transistors used in the preamplifier are showed in Fig.4.8 and Tab.4.1. The gate voltage of $M2$ is fixed by a voltage source $V_{dc,1} = 450\ mV$ which allows to have $M2$ working in the saturation region. The current flowing into $M5$ is fixed by the current generator. Consequently, its V_{gs} is fixed too. Infact, the source-drain current of a p-mos transistor working in the saturation region is given by:

$$I_{sd} = \frac{1}{2}\mu C_{ox}(\frac{W}{L})(V_{sg} - V_{th})^2(1 + \lambda V_{ds})$$

Since the current is fixed by the current mirror, the V_{sg} of $M5$ is given by:

$$V_{sg} = \sqrt{\frac{2I_{sd}}{\mu C_{ox}(\frac{W}{L})(1 + \lambda V_{ds})}} + V_{th} \tag{4.4}$$

Consequently, the drain of $M6$ is fixed. The voltage source placed on the gate of $M6$ ($V_{dc,2} = 700\ mV$) allows to fix the voltage value of the source of $M6$. The gate voltage of the transistors $M4$ and $M3$ is fixed too. Since the output impedance of the cascode formed by $M3$ and $M4$ is high, the current variation due to an input signal at the drain of $M3$ are small. Therefore, the voltage variations at the drain of $M4$ (or gate of $M3$) are negligible. The transistor $M4$ has V_{gs} and V_{ds} fixed and it can be considerated as an ideal current source.

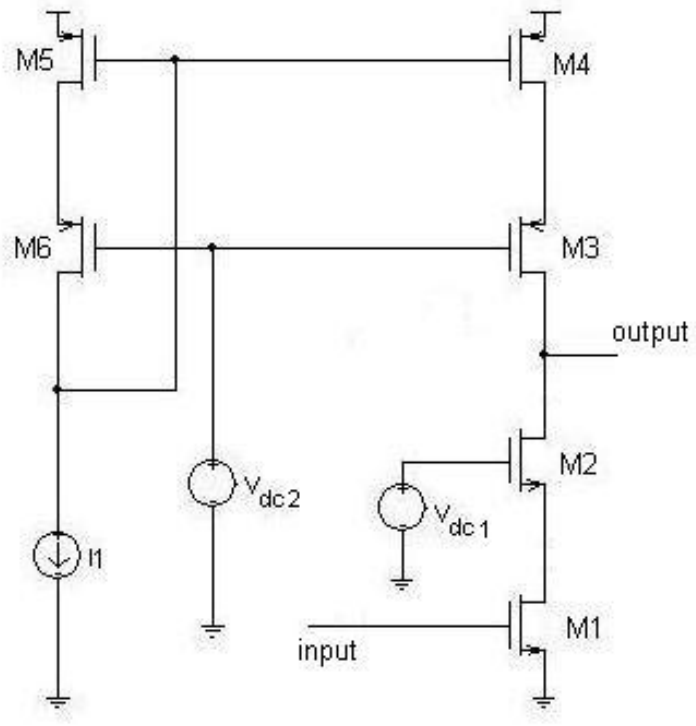

Figure 4.8: Cascode used in the preamplifier.

$(W/L)_{M1}$	$200\mu m/500nm$
$(W/L)_{M2}$	$50\mu m/500nm$
$(W/L)_{M3}$	$60\mu m/500nm$
$(W/L)_{M4}$	$120\mu m/2\mu m$
$(W/L)_{M5}$	$120\mu m/2\mu m$
$(W/L)_{M6}$	$60\mu m/500nm$

Table 4.1: Size of transistors

$I1$	$50\mu A$
$V_{dc,1}$	$450mV$
$V_{dc,2}$	$700mV$

Table 4.2: Voltage and current source values.

A further current source I_2 is used to increase the transconductance of the transistor $M1$: this transistor works in the weak-inversion region

and its transconductance depends on the current I_{ds} ($g_{m1} \propto I_{ds}$), with $I_{ds} = I_1 + I_2$. The current source I_2 is made by a current mirror (Fig.4.9): the configuration is the same used in the previous current mirror. A second stage is used to isolate the cascode amplifier from the other parts of the circuit . The second stage is a source follower, also called common-drain stage (Fig. 4.10). It operates as voltage buffer.

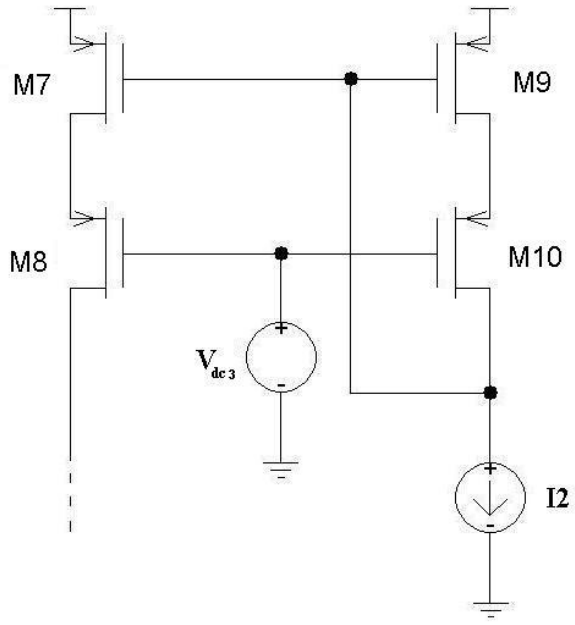

Figure 4.9: Current mirror.

$(W/L)_{M7}$	$120\mu m/2\mu m$
$(W/L)_{M8}$	$60\mu m/500nm$
$(W/L)_{M9}$	$120\mu m/2\mu m$
$(W/L)_{M10}$	$60\mu m/500nm$

Table 4.3: Size of transistors in the current mirror.

$I2$	$150\mu A$
$V_{dc,3}$	$560mV$

Table 4.4: Voltage and current source values.

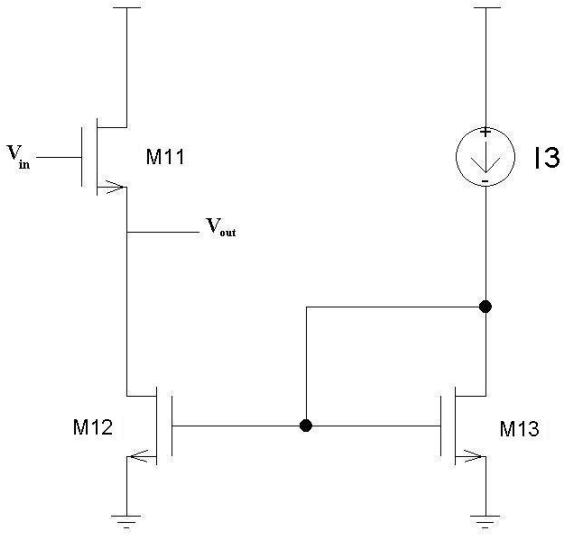

Figure 4.10: Source follower

$(W/L)_{M11}$	$10\mu m/500nm$
$(W/L)_{M12}$	$15\mu m/1\mu m$
$(W/L)_{M13}$	$15\mu m/1\mu m$

Table 4.5: Size of transistors in the source follower.

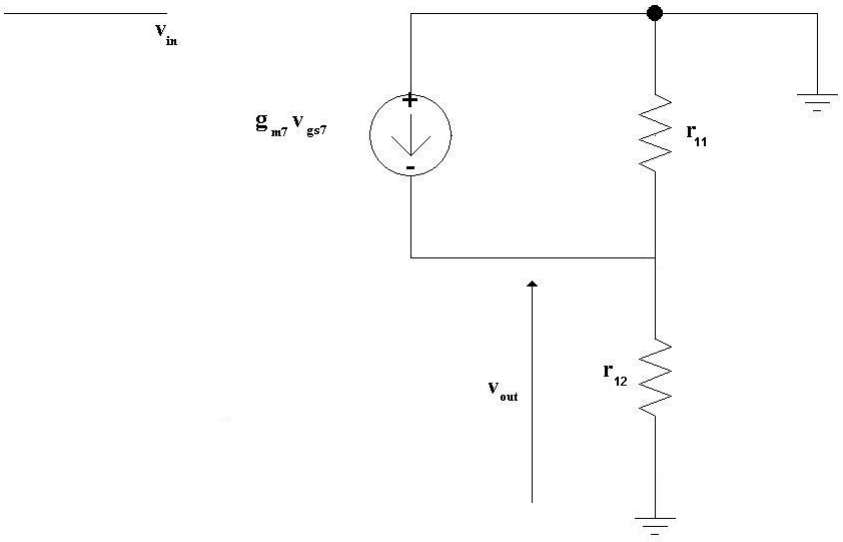

Figure 4.11: Small signal model of the source follower.

The current into the source follower is $I_3 = 100\mu A$. The gain of the source follower is given by the solution of:

$$v_o(\frac{1}{r_{11}} + \frac{1}{r_{12}}) - g_{m11}(v_{in} - v_o) = 0$$

The gain of the source follower therefore is:

$$A_{sf} = \frac{v_o}{v_{in}} = \frac{g_{m11}}{g_{m11} + \frac{1}{r_{11}} + \frac{1}{r_{12}}} \approx 1 \tag{4.5}$$

In fact, the simulated value of the gain is:

$$A = \frac{1.066mS}{\frac{1}{28k\Omega} + \frac{1}{16k\Omega} + 1.066mS} \approx 1$$

The feedback applied to the amplifier is made by a capacitor ($C_1 = 200\ fF$), which integrates the signal, and a resistor ($R_1 = 1\ M\Omega$), which decreases the input resistance (the equivalent Miller input resistance is $\frac{R_1}{A+1}$) and discharges the capacitor.

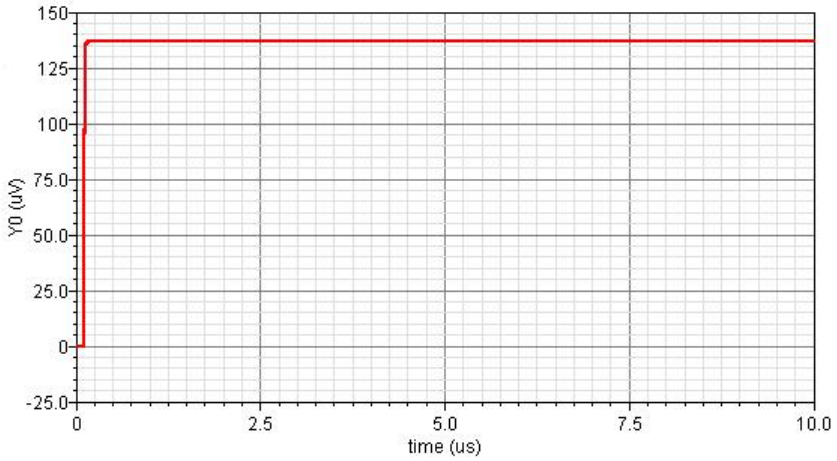

Figure 4.12: Output signal withtout resistive feedback.

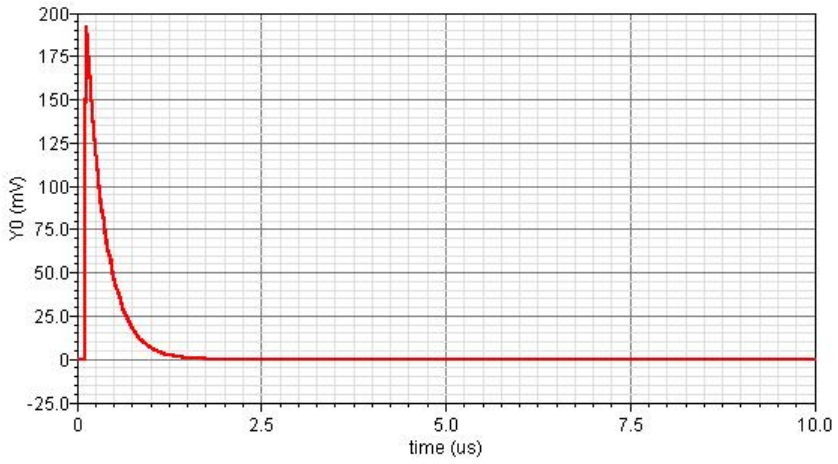

Figure 4.13: Output signal with resistive feedback.

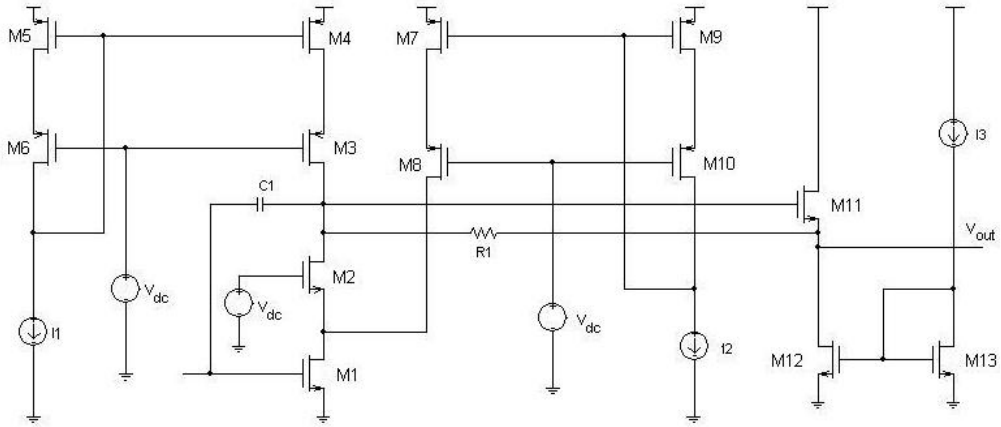

Figure 4.14: The preamplifier with feedback.

4.4 Pole-zero cancellation

The pole-zero cancellation stage derives the signal coming from the previous stage, increases the bandwidth and allows to change voltage variations of the output node into current variation. It is made by a resistor and a capacitor connected in parallel (Fig.4.15). The increasing of the bandwidth

can be understood by studying the transfer function. The transfer function of stages in cascade can be written as the product of the transfer function of each single stage.

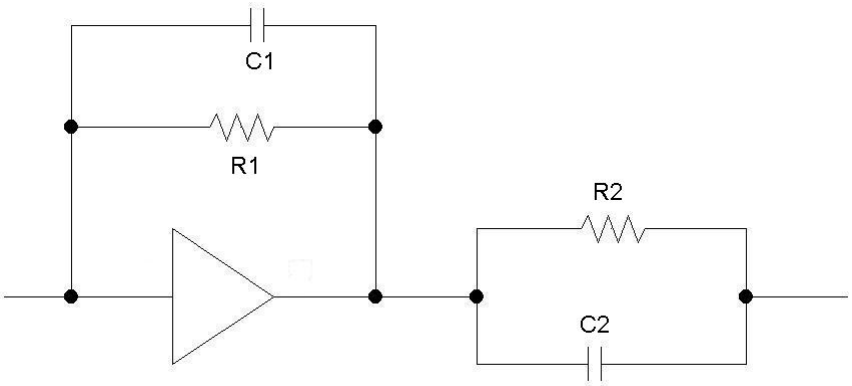

Figure 4.15: Schematic of the complete preamplifier.

The first stage (integration stage) is made by a high open loop amplifier and a feedback network made by a resistor and a capacitor connected in parallel. In Fig.4.16 the feedback system is showed , with $H(s)$ open loop gain and β feedback network.

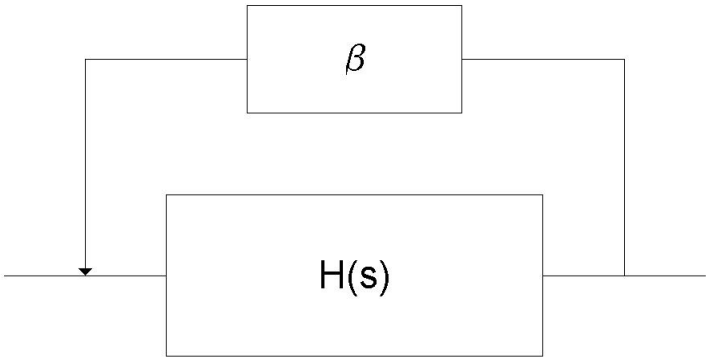

Figure 4.16: The feedback system.

The transfer function is given by:

$$T_1(s) = \frac{H(s)}{1 + \beta H(s)} \approx \frac{1}{\beta} \tag{4.6}$$

since $\beta H(s) \gg 1$. The term β is given by:

$$\beta = (R_1 \parallel C_1)^{-1} = \frac{1}{R_1} + sC_1 = \frac{1 + sR_1C_1}{R_1}$$

The transfer function can be written as:

$$T(s) = \frac{R_1}{1 + sR_1C_1} \tag{4.7}$$

The transfer function of the second stage (Fig.4.17) is given by:

$$T_2(s) = \frac{I_3}{V_2}$$

with

$$I_3 = \frac{V_2}{Z_{tot}}$$

and

$$\frac{1}{Z_{tot}} = \frac{1}{R_2} + sC_2 = \frac{1 + sR_2C_2}{R_2}$$

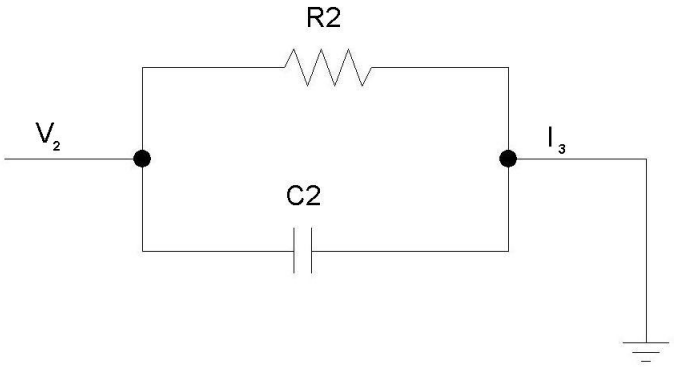

Figure 4.17: Pole-zero cancellation stage.

The transfer function of the second stage can be written as:

$$T_2(s) = \frac{1 + sR_2C_2}{R_2} \tag{4.8}$$

The transfer function of the system is given by:

$$T(s) = T_1(s)T_2(s) = \frac{R_1}{R_2}\frac{1 + sR_2C_2}{1 + sR_1C_1} \tag{4.9}$$

The DC gain of the system is given by the ratio $\frac{R_1}{R_2}$.The transfer function has a dominant pole due to the first stage ($s = \frac{1}{R_1C_1}$) and a zero due to the second stage ($s = \frac{1}{R_2C_2}$). By choosing $R_1C_1 = R_2C_2$, the pole-zero cancellation becomes possible. By erasing the pole due to the first stage, the bandwidth increases its value until the pole due to the cut-off frequency of mosfet comes up. Fig.4.18 shows the bandwidth increasing. In the first case, the Bode diagram shows the gain versus the frequency without pole-zero cancellation. The cut-off frequency is given by:

$$f = \frac{1}{2\pi R_1C_1} = \frac{1}{2\pi\ 1M\Omega\ 200fF} \approx 7.96 \cdot 10^5 Hz$$

In the second case, the Bode diagram shows an improper pole-zero compensation: it is useful to see the effects of the derivation stage. The zero due to this stage is placed at $\approx 10^6\ Hz$. In the last case, the Bode diagram shows a proper pole-zero compensation. The value of the resistor and of the capacitor used in the pole-zero cancellation stage are $R_2 = 200\ k\Omega$ and $C_2 = 1.18\ pF$. The resistor value is chosen to have $\frac{R_2}{R_1} = 5$. The ratio $\frac{C_2}{C_1} \neq 5$ is due to the parasitics capacitances in parallel to C_1 which increases the value of the feedback capacitance. Consequently, the effective value of C_2 is higher than the theoretical value. The difference between the cut-off frequency of the first and the last case is around $100\ Hz$.

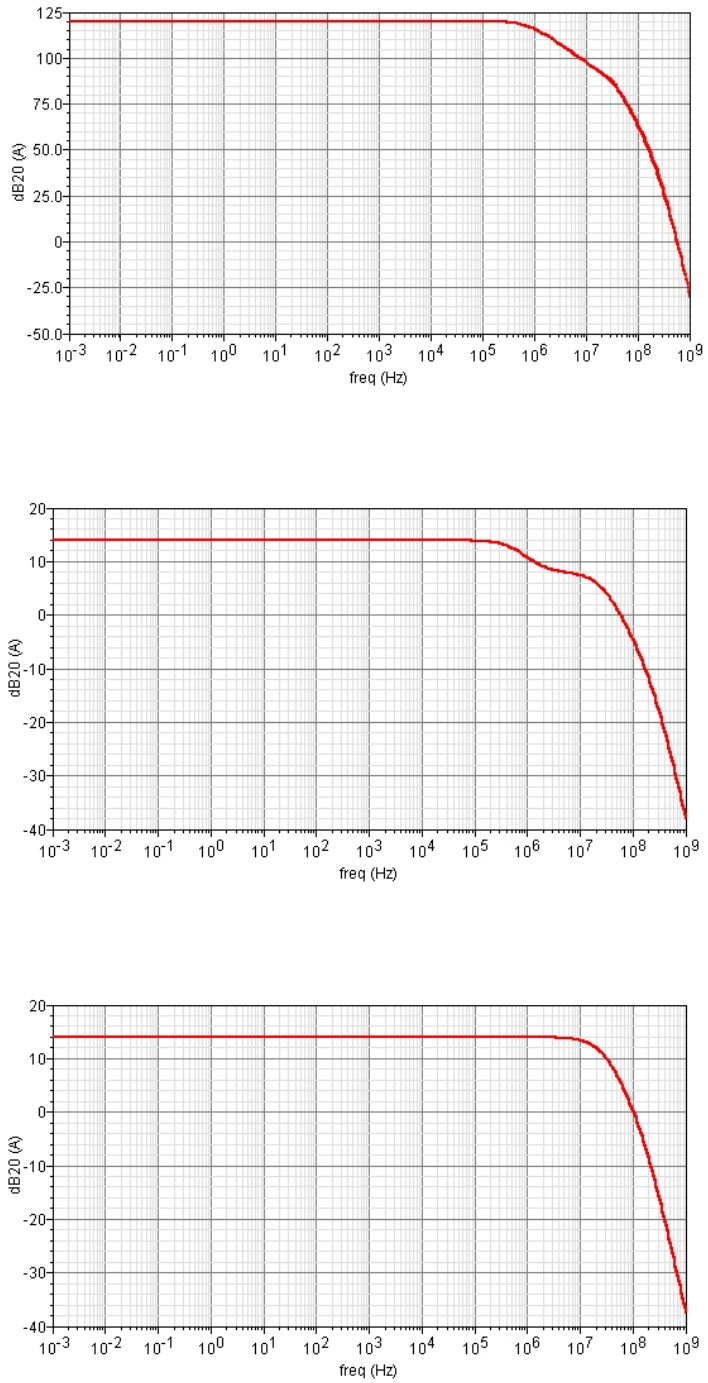

Figure 4.18: Pole-zero cancellation.

4.5 Linearity

A good charge amplifier should have a linear charge amplification.The best way to test the linearity of the preamplifier is to measure the output signal changing the input signal by a parametric simulation : the Q_{out} to Q_{in} ratio has to be constant. The input signal is a variable amplitude current pulse (an example is showed on Fig.4.4), from I_{min} to I_{max}.The charge value is given by:

$$Q = \int_0^t I dt$$

The values of the parameters used are shown in Tab.4.6. Fig.4.19 shows the output charge value (Q_{out}) versus the input charge value (Q_{in}). Using the software *Mathematica*, it is possible to find the best fit of the values simulated. The best linear fit slope is ≈ 5, equal to the ratio $\frac{R_1}{R_2}$.

parameter	**value**
I_{min}	$83.3nA$
I_{max}	$8.3\mu A$
Q_{min}	$1fC$
Q_{max}	$100fC$
Pulse Rise Time	$5ns$
Pulse Fall Time	$15ns$
Pulse Width Time	$2ns$

Table 4.6: Input signal features.

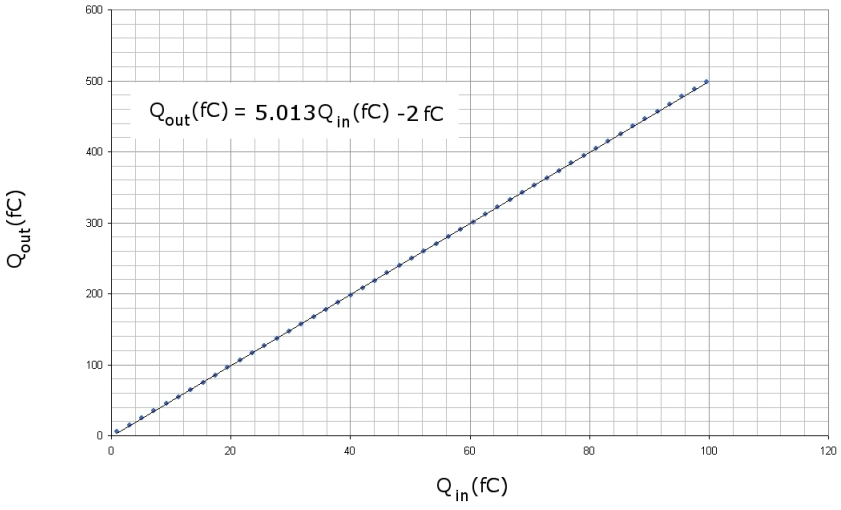

Figure 4.19: Preamplifier linearity.

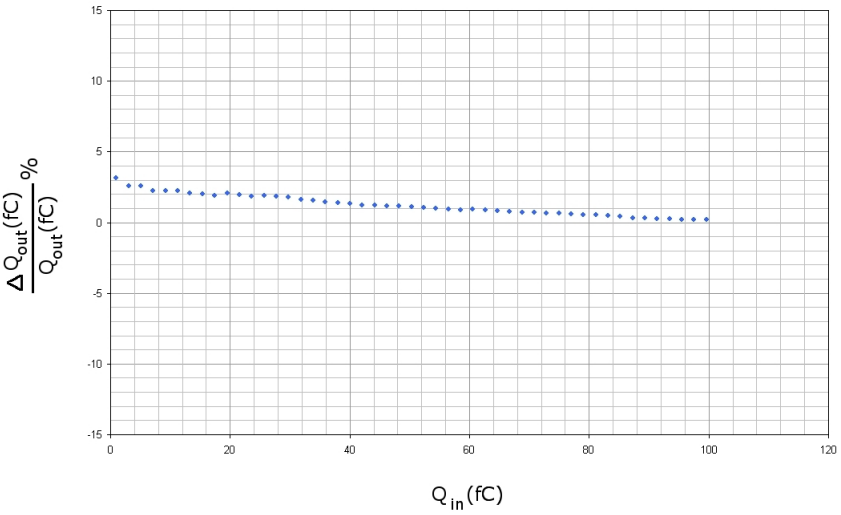

Figure 4.20: The relative percent error of the output charge.

Chapter 5

The Time over Threshold Stage

The ToT stage generates a pulse whose width is proportional to the charge collected at the input node. It is made by an amplifier with a capacitive feedback, which amplifies the input signal, a costant current feedback circuit, which discharges the input node and a feedback circuit which fixes the DC voltage output injecting current in the input node. When the amplifier is working in the linear region, the output voltage is given by:

$$v_{out} = \frac{Q_{in}}{C_{fb}}$$

The maximum value available by the voltage output is given by the voltage supply of the amplifier (V_{dd}). When the input charge is so high to have $v_{out} = V_{dd}$, the amplifier is said to work in saturation; if a higher charge comes at the input of the amplifier, the voltage output doesn't increase its value. Consequently, the relation between v_{out} and Q_{in} is no more linear and the amplifier gain decreases its value. For example, let's suppose to have $C_{fb} = 125\ fF$,$V_{dd} = 1.2\ V$ and the DC output voltage $V_{out,DC} = 300\ mV$. When $Q_{in} = 10\ fC$, the output voltage is $v_{out} = 380\ mV$; when $Q_{in} = 112\ fC$, $v_{out} \approx 1.2\ V$; for input charge higher than $Q_{in} = 112\ fC$, the output voltage continues to be $1.2\ V$.
With this technique one does not measure the peak amplitude of the output signal but the time spent by the current feedback to discharge the feedback capacitance: when the amplifier is saturated, the charge is accumulated on

the input node, forcing the input voltage to change value. However, the work condition of the amplifier doesn't influence the ToT measures.

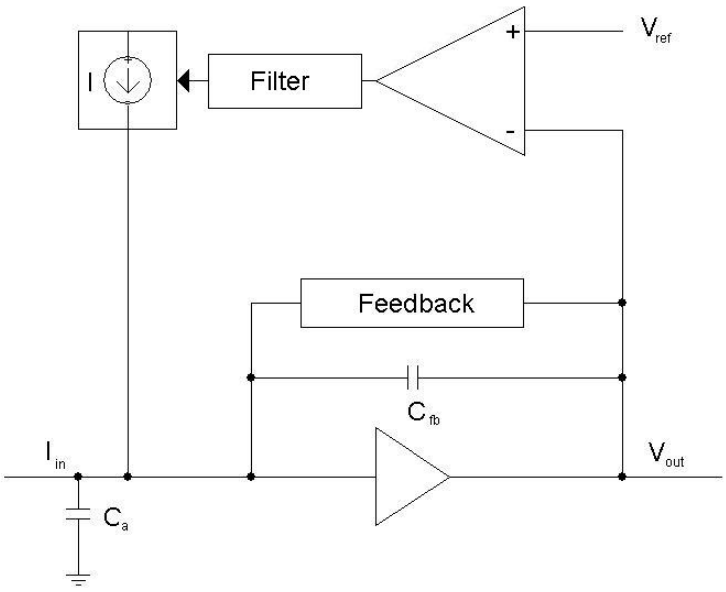

Figure 5.1: The ToT stage.

5.1 Core Amplifier of the ToT Stage

The amplifier is a high open loop gain stage. It is made by a cascode stage and a source follower (the small signal models are the same used in the previous chapter). The feedback capacitor ($C_{fb} = 125\ fF$) is used to collect charges at the input node. It is discharged by a costant current. The value of the capacitor is chosen to maximize the amplification of the circuit ($v_{out} \propto \frac{1}{C_{in}}$) and to have a stable loop.

The capacitor $C_a = 1.2\ pF$ limits the voltage variations at the input node when the amplifier is working in saturation region. In fact, when the amplifier works in the saturation region, the input charge is collected by the input capacitance C_{in}:

$$C_{in} = C_a + (A_v + 1)C_{fb}$$

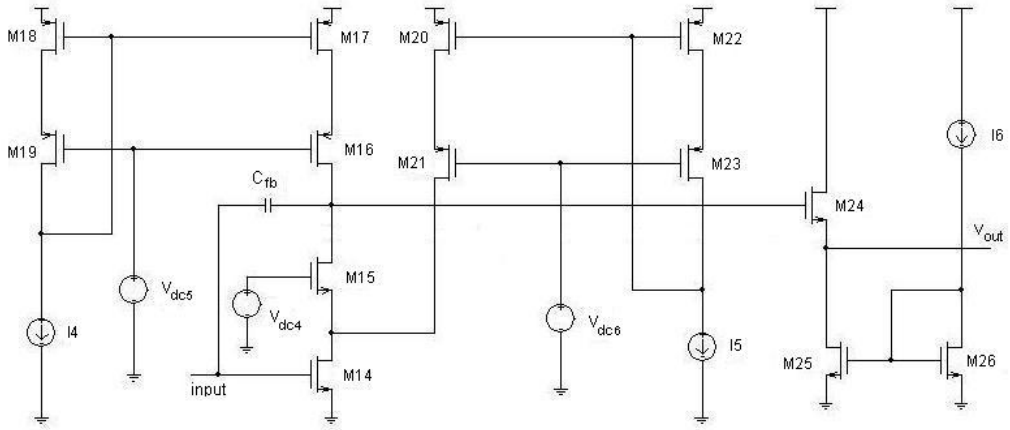

Figure 5.2: The amplifier of the ToT stage.

$(W/L)_{M14}$	$125\mu m/500nm$
$(W/L)_{M15}$	$5\mu m/500nm$
$(W/L)_{M16}$	$15\mu m/500nm$
$(W/L)_{M17}$	$15\mu m/2\mu m$
$(W/L)_{M18}$	$15\mu m/2\mu m$
$(W/L)_{M19}$	$15\mu m/500nm$
$(W/L)_{M20}$	$40\mu m/2\mu m$
$(W/L)_{M21}$	$40\mu m/500nm$
$(W/L)_{M22}$	$40\mu m/2\mu m$
$(W/L)_{M23}$	$40\mu m/500nm$
$(W/L)_{M24}$	$15\mu m/500nm$
$(W/L)_{M25}$	$5\mu m/1\mu m$
$(W/L)_{M26}$	$5\mu m/1\mu m$

Table 5.1: Sizes of transistors

$I4$	$10\mu A$
$I5$	$30\mu A$
$I6$	$50\mu A$
V_{dc4}	$500mV$
V_{dc5}	$500mV$
V_{dc6}	$650mV$

Table 5.2: Voltage and current source values.

When the amplifier works in the linear region, $A_v \gg 1$, $A_v C_{fb} \gg C_a$ and $C_{in} \approx A_v C_{fb}$; when the amplifier works in the saturation region and $C_a > (A_V + 1)C_{fb}$, $C_{in} \approx C_a$. Since the voltage variations at the input node is given by:

$$\Delta V = \frac{Q_{in,ToT}}{C_{in}}$$

(with $Q_{in,Tot}$ charge value at the input of ToT stage), when the amplifier works in the linear region, the voltage variations at the input of the ToT stage are small ($\approx$ mV). Supposing to have no capacitor at the input of the ToT stage ($C_a = 0\ fF$), when the amplifier works in saturation region the input capacitance is given by the parasitic capacitances of the input MOS of the ToT stage ($\approx$ fF) and consequently, the voltage variations would be significantly bigger (Fig.5.3 and 5.4).

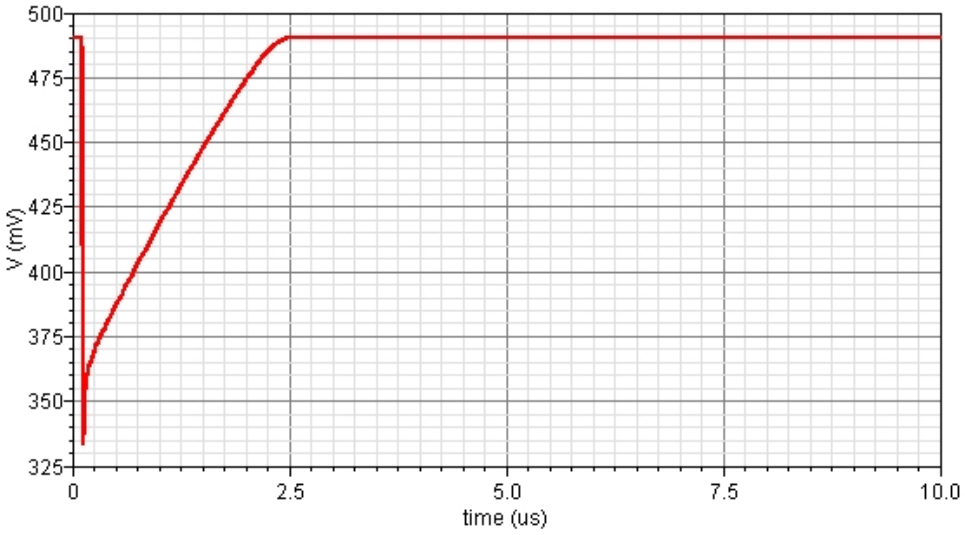

Figure 5.3: The voltage swing at the input of the ToT stage with C_a ($Q_{in} = 30\ fC$).

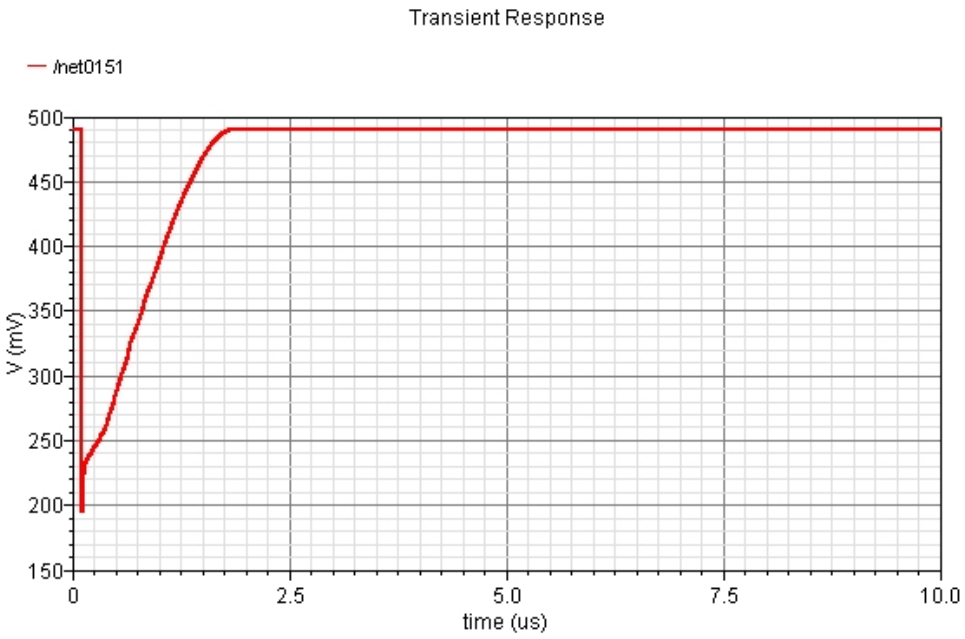

Figure 5.4: The voltage swing at the input of the ToT stage without C_a ($Q_{in} = 30\ fC$).

5.2 The Current Feedback

The constant current feedback gives constant current to the input node to discharge the input capacitance when it is charged by an input signal. It is made by a differential stage whose inputs are the output voltage of the ToT stage and a reference voltage. The current I_{fb} flowing in the two branches of the differential amplifier is given by a current mirror: when there is no signal at the input and the DC voltage levels at the input nodes of the differential amplifier have the same value (Fig.5.6), I_{fb} is equally divided between the two branches. When the voltage levels at the output nodes are different, the difference of current flowing in the two branches restores the equality between the inputs.

When a negative input signal is amplified, V_{out} increases (Fig.5.7). Consequently, $V_{gs,M46}$ decreases, the current flowing in the right branch decreases and the current flowing in the left branch increases. $M50$ and $M52$ act as a cascode current source and limit the current flowing to ground to $\frac{I_{fb}}{2}$. Therefore, the extra current supplied by $M45$ and $M47$ flows into the

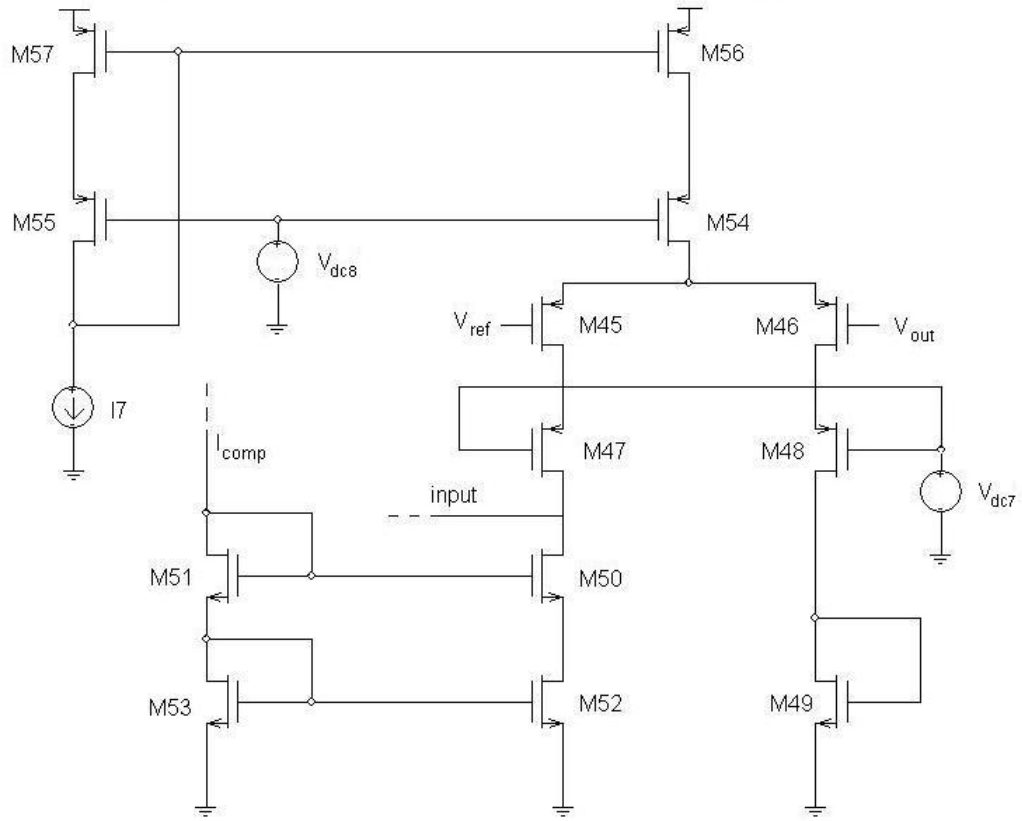

Figure 5.5: The constant current differential feedback.

$(W/L)_{M45}$	$3\mu m/1\mu m$
$(W/L)_{M46}$	$3\mu m/1\mu m$
$(W/L)_{M47}$	$1\mu m/5\mu m$
$(W/L)_{M48}$	$1\mu m/5\mu m$
$(W/L)_{M49}$	$4\mu m/60\mu m$
$(W/L)_{M50}$	$4\mu m/90\mu m$
$(W/L)_{M51}$	$4\mu m/90\mu m$
$(W/L)_{M52}$	$9\mu m/60\mu m$
$(W/L)_{M53}$	$9\mu m/60\mu m$
$(W/L)_{M54}$	$4\mu m/19\mu m$
$(W/L)_{M55}$	$4\mu m/19\mu m$
$(W/L)_{M56}$	$6\mu m/30\mu m$
$(W/L)_{M57}$	$6\mu m/30\mu m$

Table 5.3: Sizes of transistors.

$I7$	$400nA$
$V_{dc,7}$	$0V$
$V_{dc,8}$	$650mV$

Table 5.4: Voltage and current values.

input node and is integrated on the feedback capacitor. As a consequence, the output node voltage decreases till the equilibrium condition $V_{out} = V_{ref}$ is restored. When the input signal is positive, the situation is inverse and the current provided by $M50$ and $M52$ flows from the input node to the feedback stage. The cascode configuration is used to maximize the output impedance. When the voltage difference between V_{ref} and V_{out} is greater than $\approx$ 40 mV, the differential pair is fully unbalanced and, depending on the sign of $V_{out} - V_{ref}$, the current I_{fb} flows entirely in one of the two branches of the differential pair.

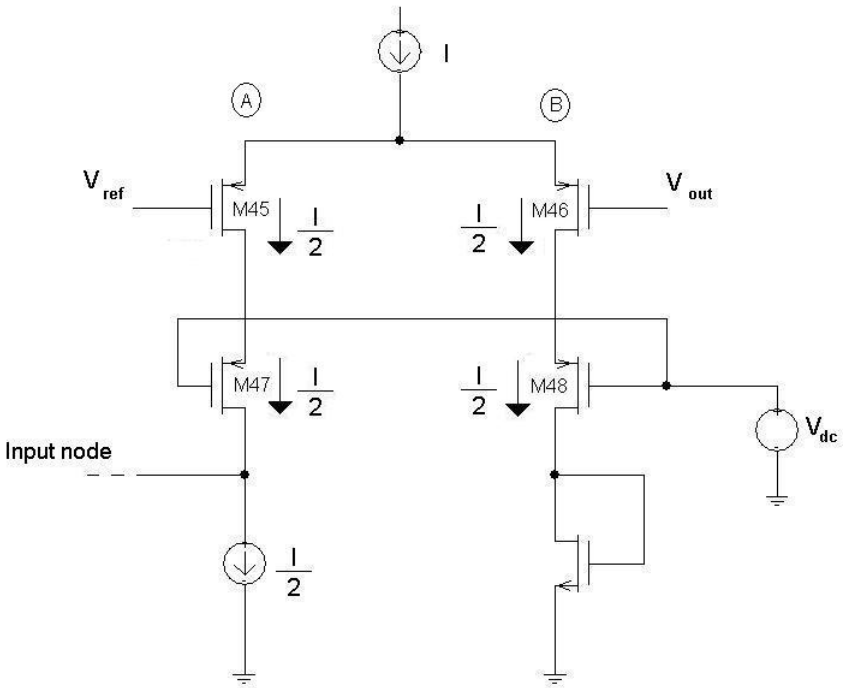

Figure 5.6: The current in the feedback system at the equilibrium.

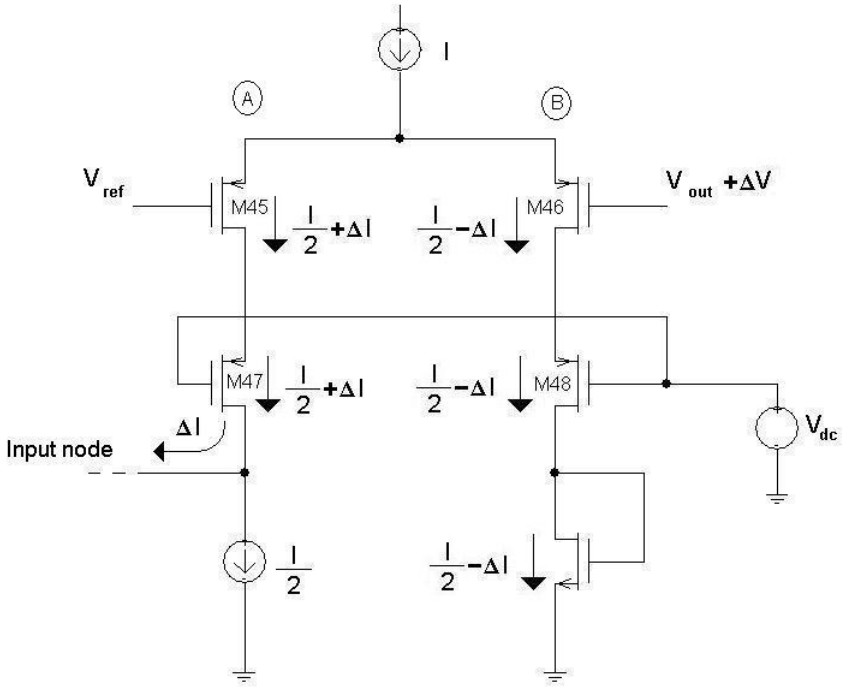

Figure 5.7: The current in the feedback system when an asymmetric condition is created.

5.3 Baseline Restorer

The baseline restorer is a circuit which fixes the output DC voltage level. It is made by a differential amplifier and a filtering stage. These stages drive a voltage-controlled current source which injects current at the input node, changing the output DC voltage. Furthermore, the baseline restorer compensates the DC currents coming from the previous stage.

5.3.1 Differential Amplifier

The baseline restorer is based on a differential amplifier with the output signal proportional to the difference of two input signals driving a voltage controlled current source. The cascode configuration used in the differential amplifier allows to have an high open loop gain: this stage is highly sensitive to the output level difference. In Fig.5.8, the configuration used is shown. When $V_{out} = V_{ref}$ (Fig. 5.9), the drain-source current of $M27$

and $M28$ ($I_{balance}$) is the same[1], the voltage values of $V_{d,M38}$ and $V_{d,M39}$ are fixed and the currents $I_{ds,M38}$ and $I_{ds,M39}$ are fixed, too. When $V_{out} > V_{ref}$ (Fig. 5.10), the circuit becomes asymmetric: the current of $M27$ becomes $I_{M27} = I_{balance} + \Delta I$, while the current of $M28$ becomes $I_{M28} = I_{balance} - \Delta I$. Since $V_{gs,M31}$ is fixed by the current mirror, $V_{ds,M31}$ increases its value. So the value of $V_{d,M31}$ decreases while $V_{gs,38}$ and $V_{gs,39}$ increase. The current $I_{comp} = I_{ds,38} + I_{ds,39}$ increases its value and it discharges the input node, decreasing the voltage DC input level. Consequently, the value of V_{out} decreases, re-establishing the initial condition $V_{out} = V_{ref}$. The behaviour of the circuit is opposite when $V_{out} < V_{ref}$.

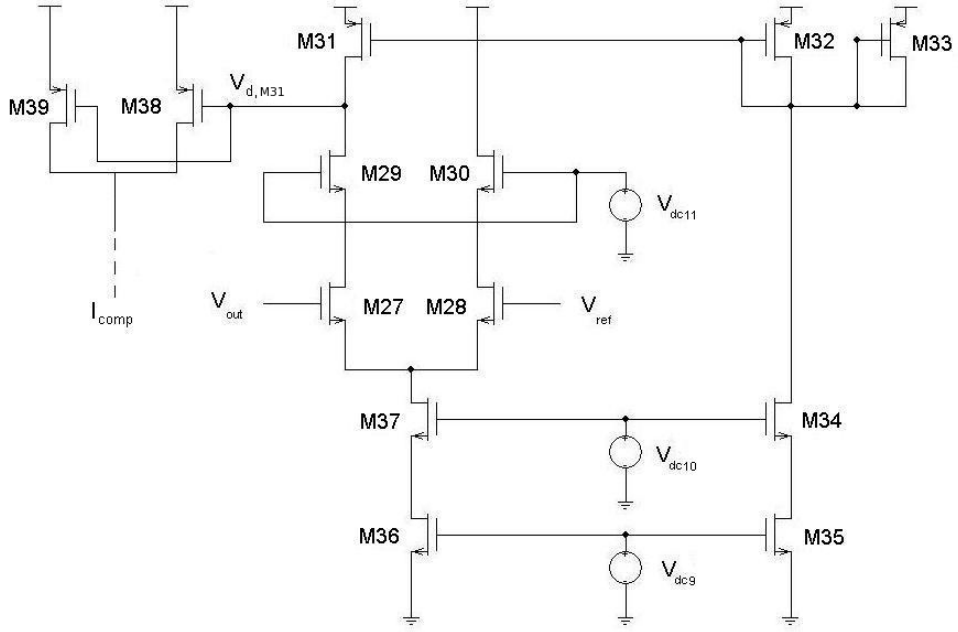

Figure 5.8: The differential amplifier; the low-pass filter is not shown.

[1]The difference due to the drain-source voltage are neglected.

$(W/L)_{M27}$	$90\mu m/2.7\mu m$
$(W/L)_{M28}$	$90\mu m/2.7\mu m$
$(W/L)_{M29}$	$60\mu m/5\mu m$
$(W/L)_{M30}$	$60\mu m/5\mu m$
$(W/L)_{M31}$	$6\mu m/60\mu m$
$(W/L)_{M32}$	$6\mu m/60\mu m$
$(W/L)_{M33}$	$6\mu m/60\mu m$
$(W/L)_{M34}$	$6.8\mu m/50\mu m$
$(W/L)_{M35}$	$6.8\mu m/50\mu m$
$(W/L)_{M36}$	$6.8\mu m/50\mu m$
$(W/L)_{M37}$	$6.8\mu m/50\mu m$
$(W/L)_{M38}$	$8\mu m/30\mu m$
$(W/L)_{M39}$	$8\mu m/30\mu m$

Table 5.5: Sizes of transistors.

$V_{dc,9}$	$192.8mV$
$V_{dc,10}$	$331.1mV$
$V_{dc,11}$	$1V$

Table 5.6: Voltage and current values.

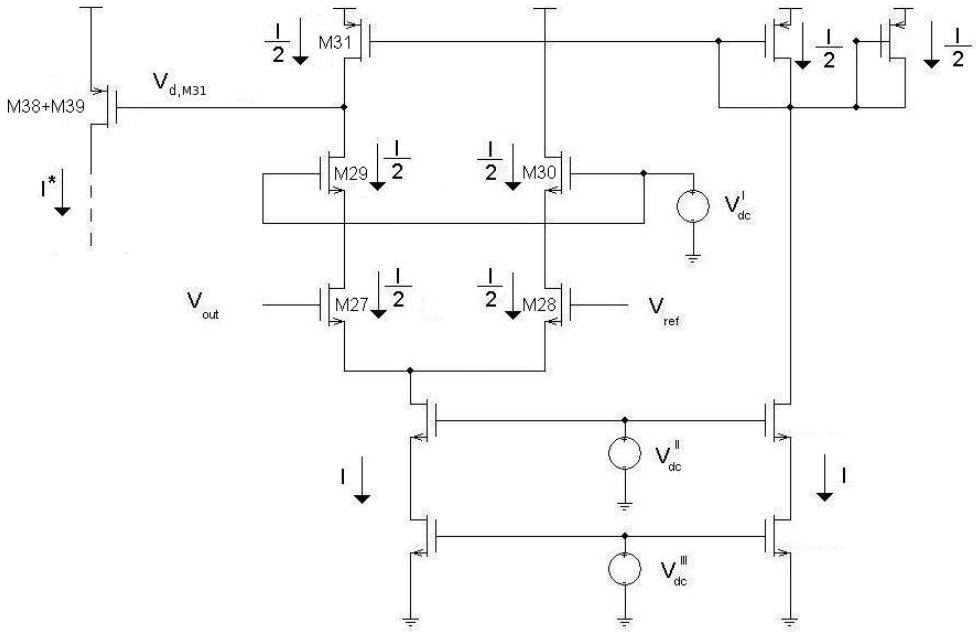

Figure 5.9: The differential amplifier.

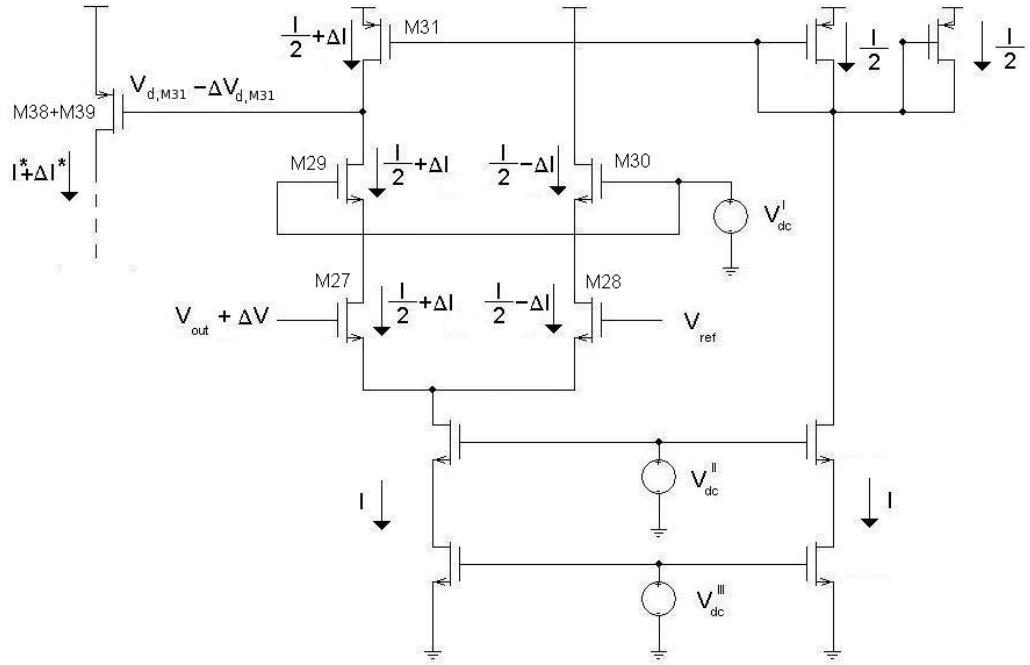

Figure 5.10: The asymmetric differential amplifier.

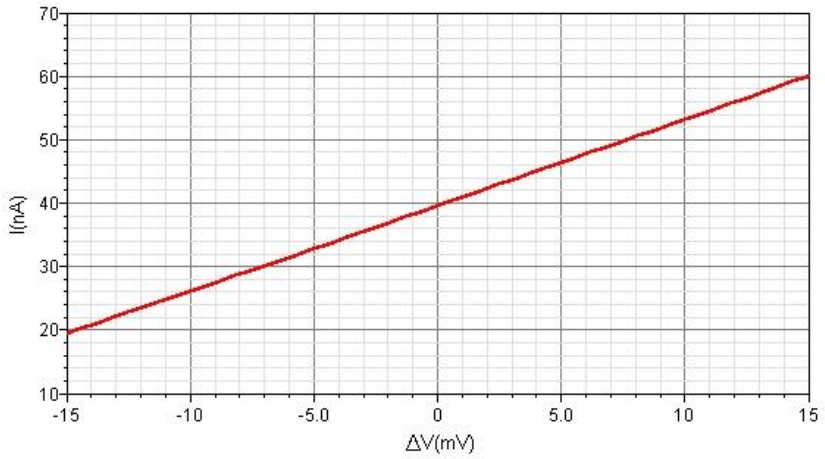

Figure 5.11: The current variation due to the voltage variation at the input of the differential stage.

5.3.2 Filtering stage

A key difference between the baseline restorer and the constant-current feedback is that the former should be sensitive only to very slow variations. Therefore, its bandwidth must be strongly limited. This is obtained with a low-pass filter, formed by a capacitor and a resistor of very high value which is implemented with a p-mos transistor.
A diode connected MOS-FET can be used as small-signal resistor; the source voltage and the gate voltage have the same value.

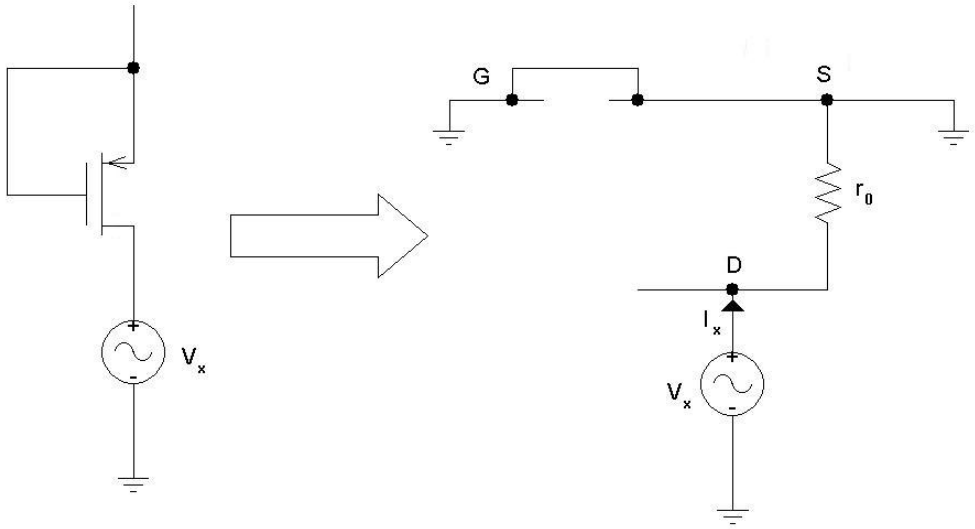

Figure 5.12: Diode connected MOSFET.

The impedance of the circuit is given by:

$$Z_x = \frac{V_x}{I_x} = r_0$$

Furthermore, since $V_{gs} = 0\ V$, only very small subthreshold currents will be present in the device, leading to a very high value of r_0. A transistor can be used as capacitor, too. When the drain and the source are shorted, the transistor can be considered a two terminal device. When it works in saturation region, a layer of free charges begins to form under the oxide: the device can be modelized as a capacitor with two plates (the layer of free charges and the gate) separated by an insulator (the oxide). The unit area capacitance of C_{ox} is a technical parameter and it is independent from the

V_{gs} value.

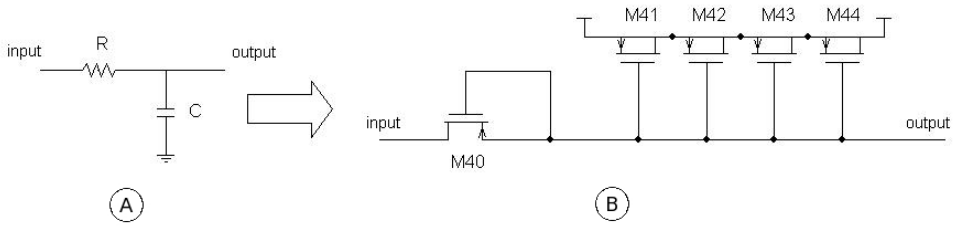

Figure 5.13: The filtering circuit.

$(W/L)_{M40}$	$90\mu m/2.7\mu m$
$(W/L)_{M41}$	$90\mu m/2.7\mu m$
$(W/L)_{M42}$	$60\mu m/5\mu m$
$(W/L)_{M43}$	$60\mu m/5\mu m$
$(W/L)_{M44}$	$6\mu m/60\mu m$

Table 5.7: Sizes of transistors.

A good way to study the cut-off frequency of the RC low pass filter is to compare the Bode diagram of the circuit made by resistor and capacitor (Fig.5.13, circuit A) and the circuit made by transistor (Fig.5.13, circuit B). The capacitor value used is given by the equivalent capacitance value of the transistors in parallel ($C_{eq} \approx 1\ pF$) and the resistor value is given by the equivalent transistor resistance ($R_{eq} \approx 1.76\ G\Omega$). In Fig.5.14 the Bode diagram of the circuit A (blue line) and the circuit B (red line) are showed: the cut-off frequency of the circuits is $f_{cut-off} \approx 25\ Hz$. The expected cut-off frequency of the circuit A is given by:

$$f^*_{cut-off} = \frac{1}{2\pi\ R_{eq}C_{eq}} \approx 45\ Hz$$

The difference between the values obtained is due to the parasitic capacitances C_{gs} and C_{gb} of $M38$ and $M39$: by comparing the cut-off frequency, it is possible to calculate the value of the parasitic capacitances. The capacitance giving the cut-off frequency of 25 Hz is:

$$C_{tot} = \frac{1}{2\pi\ R f_{cut-off}} = 3.6\ pF$$

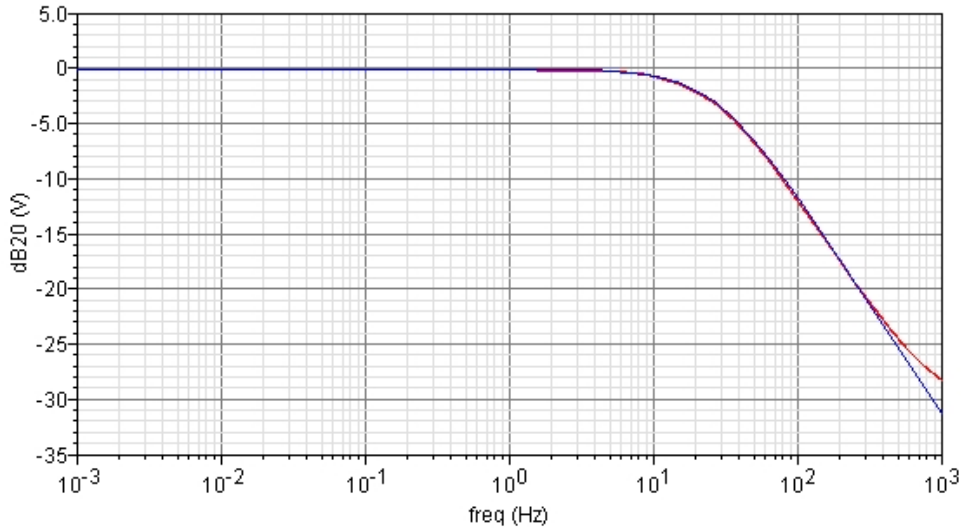

Figure 5.14: Bode diagram of the low-pass filter.

Since $C_{eq} \approx 1\ pF$, the value of the parasitic capacitance is $C_{par} = 2.6\ pF$, in good agreement with the value given by the software.

5.4 Linearity

The linearity of the ToT stage has been studied using the same method employed to test the linearity of the preamplifier. The input signal (injected directly at the input of ToT stage) is a variable amplitude current pulse. The maximum charge used (500 fC) reflects the maximum charge collected on the detector (100 fC) and amplified by the preamplifier ($A_{pre} = 5$). The DC voltage of the output signal is 300 mV. However, the threshold voltage has to be put higher, otherwise the circuit will fire continuously on the noise. The noise at the output of the ToT stage has been evaluated to 6 mV RMS. The threshold voltage for the ToT stage has been set to 330 mV ($\approx 5\ RMS$ above the noise level).

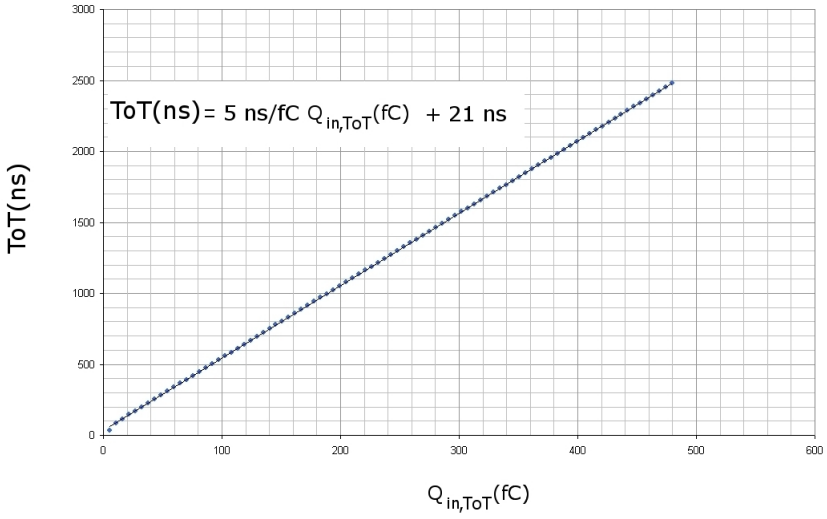

Figure 5.15: Linearity of the ToT stage; the charge is injected at the input of the ToT stage.

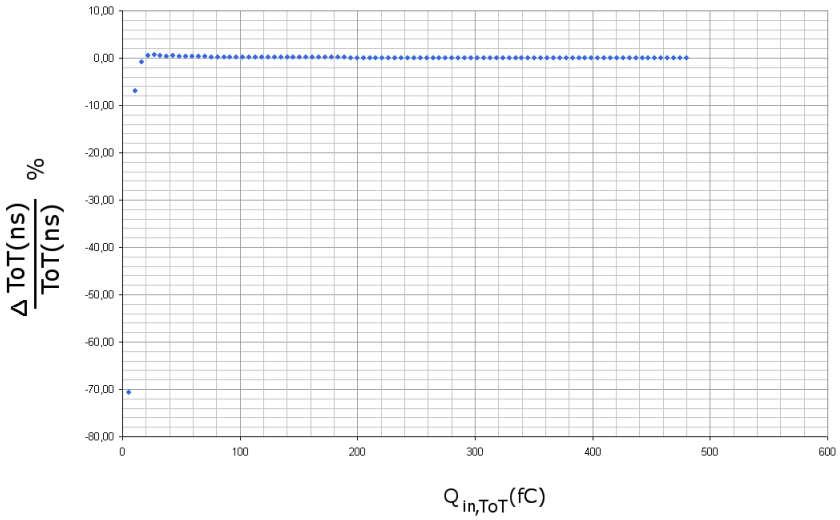

Figure 5.16: The relative percent error of the ToT.

Chapter 6

Current Buffer

The step by step design allows to design and optimize each stage separately. However, an excellent performance of each stage, studied separately, doesn't assure a good performance of the global system. The addition of intermediate stages may become necessary.

6.1 Why a buffer?

The circuit designed to analyze a signal coming from strips consists of a preamplifier, which isolates each strip from its neighbours and amplifies the input current signal, and a ToT stage. In these stages, tested separately, the ToT and the injected charges are directly proportional (Fig.4.19 and Fig.5.15) but when these stages are connected together, the relation is not linear. In Fig. 6.1, the difference between the simulated ToT as function of the input charges and the ToT expected (directly proportional with the input charge) are showed.

For high input charge values, the ToT obtained by simulation is lower than the expected ToT. Since each stage individually tested shows an excellent linearity, the problem is due to the interface between the stages. In particular, the output impedance of the preamplifier causes the missed linearity. The output impedance should be infinite (Fig.4.1). However, the output impedance of the amplifier is given by the resistance of the pole-zero cancellation stage in series with the source follower output impedance.

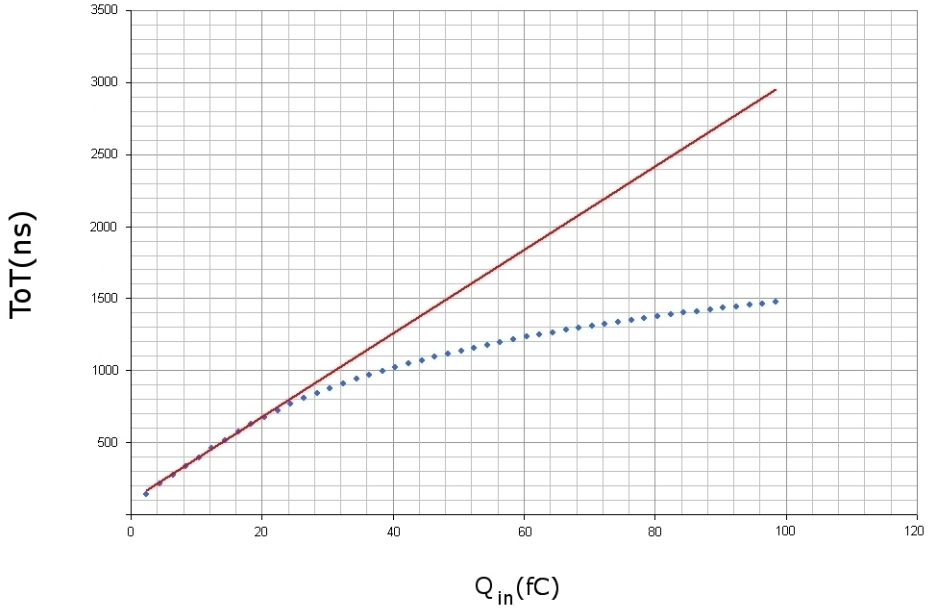

Figure 6.1: The ToT of the global system.

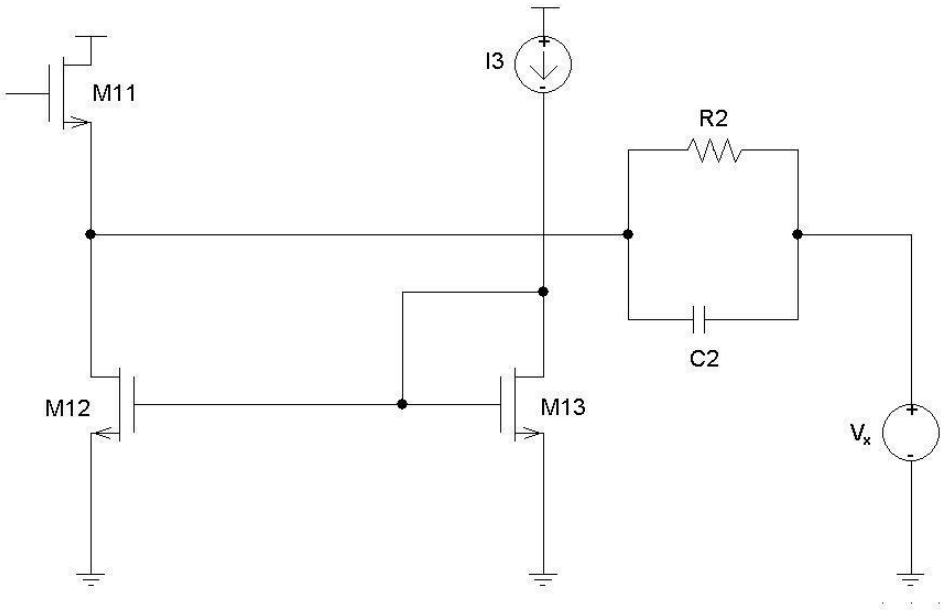

Figure 6.2: The impedence of the preamplifier.

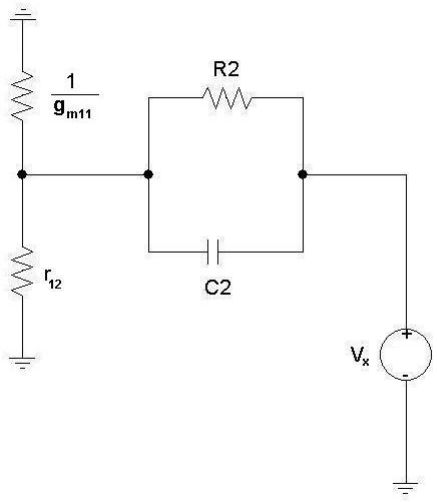

Figure 6.3: The small signal model.

Neglecting the capacitor and considering

$$R_{tot} = R2 + (\frac{1}{gm_{11}} \parallel r_{12}) \approx 200k\Omega$$

the current I_x is given by:

$$I_x = \frac{v_x}{R_{tot}}$$

Consequently, the output impedance is given by:

$$Z_x = \frac{v_x}{I_x} = R_{tot}$$

When a signal is processed by the circuit, it causes voltage variations at the output of the preamplifier and at the input of the ToT stage. Since the output resistance doesn't approach infinite, there is unwanted extracurrent (Fig. 6.4) at the input node of the ToT stage, coming from the preamplifier:

$$I_{pre}(t) = \frac{v_1(t) - v_2(t)}{R_{tot}}$$

The total current which discharges the input node is given by:

$$I_{dis} = I_{ToT} + I_{pre}$$

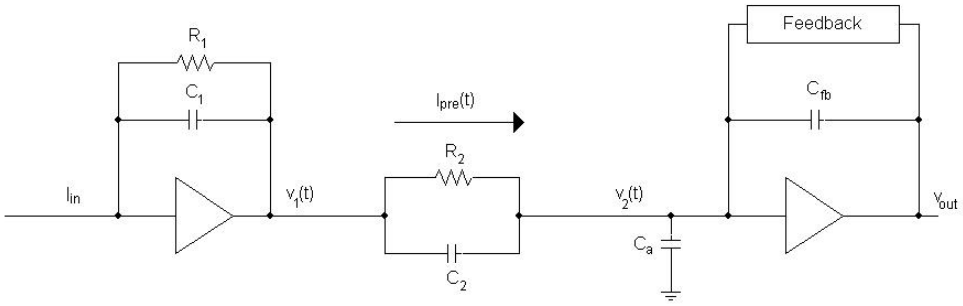

Figure 6.4: The extracurrent at the input of the ToT stage.

A very high output impedance becomes necessary to have no extracurrent coming from the preamplifier: a good way to eliminate the extracurrent is to use a current buffer, i.e. a circuit with very low input impedance and very high output impedance.

6.2 Buffer Configuration

The current buffer has a common gate input and a regulated cascode output. The common gate allows to mirror the input signal at the output, while the regulated cascode allows to have a large output impedance.

$(W/L)_{M58}$	$30\mu m/500nm$
$(W/L)_{M59}$	$30\mu m/500nm$
$(W/L)_{M60}$	$30\mu m/250nm$
$(W/L)_{M61}$	$20\mu m/500nm$
$(W/L)_{M62}$	$20\mu m/500nm$
$(W/L)_{M63}$	$13.24\mu m/500nm$
$(W/L)_{M64}$	$10\mu m/500nm$
$(W/L)_{M65}$	$35\mu m/500nm$
$(W/L)_{M66}$	$50\mu m/500nm$
$(W/L)_{M67}$	$10\mu m/1.7\mu m$

Table 6.1: Sizes of transistors.

The small signal model is shown in Fig.6.6. The output impedance[1] is

[1]The bulk-source transimpedance has been neglected.

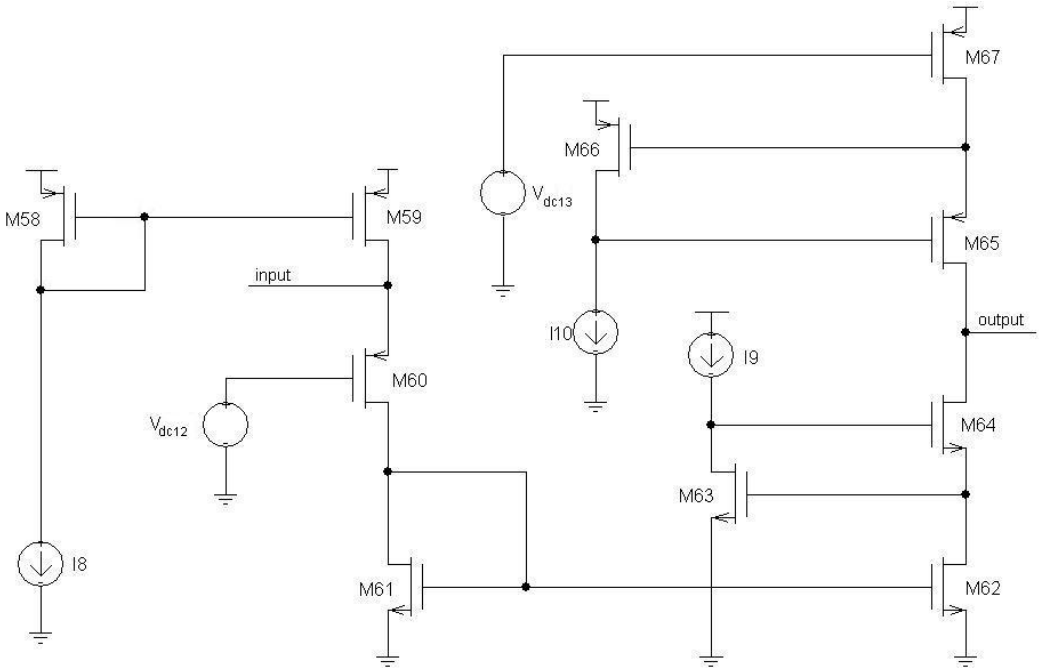

Figure 6.5: The buffer.

$I8$	$20\mu A$
$I9$	$20\mu A$
$I10$	$20\mu A$
$V_{dc,12}$	$537mV$
$V_{dc,13}$	$689.72mV$

Table 6.2: Voltage and current values.

given by:

$$Z_x = \frac{V_x}{I_x} = r_{62} + r_{64} + r_{62}r_{64}g_{m64} + r_{62}r_{64}r_{63}g_{m64}g_{m63}$$

The value of the output impedance obtained by the small signal model is 97 $M\Omega$ and the value simulated by the software is 79 $M\Omega$ (the difference is due to the approximations done in the small signal model, but the two values are of the same order of magnitude).

The difference between the output impedance of the regulated cascode and the classic cascode (4.1) is due to the feedback transistor: it can be understood by studying the output impedance with a current source I_x at

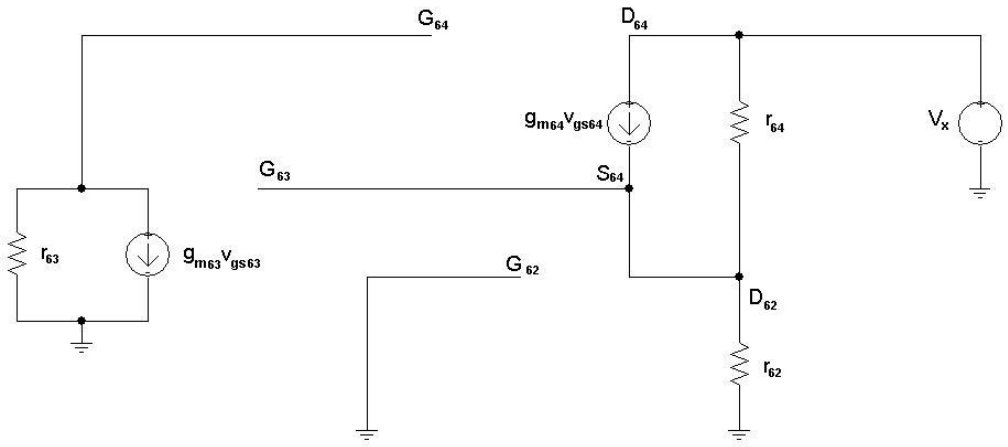

Figure 6.6: The small signal model of the regulated cascode.

the output and grounding the gate of the input transistor (Fig. 6.7). In fact, in the classic cascode, the gate voltage of the cascode transistor $T2$ is fixed by a voltage source V_{dc}. Since the source and the gate voltage values of $T1$ are fixed, when a current I_x is injected into the cascode stage, the drain of $T1$ increases its value, the V_{gs} of $T2$ decreases and, consequently, its V_{ds} increases. In the regulated cascode configuration, the gate of transistor $T5$ is not fixed. When the drain of transistor $T3$ (which is the gate of transistor $T4$) increases its value, the drain of $T4$ decreases because its current it is fixed by the current source I_{dc}: the V_{gs} of $T5$ decreases because the source increases and the gate decreases (it is not fixed by the voltage source as the classic cascode). The drain voltage of $T5$ increases its value because it has to compensate the decrease of the V_{gs}: this increase is higher than the increase of the classic cascode. Since the output impedance is given by:

$$Z_x = \frac{\Delta V_x}{\Delta I_x}$$

and ΔV_x is higher in the regulated cascode, the output impedance of the regulated cascode is higher than the output impedance of the classic cascode.

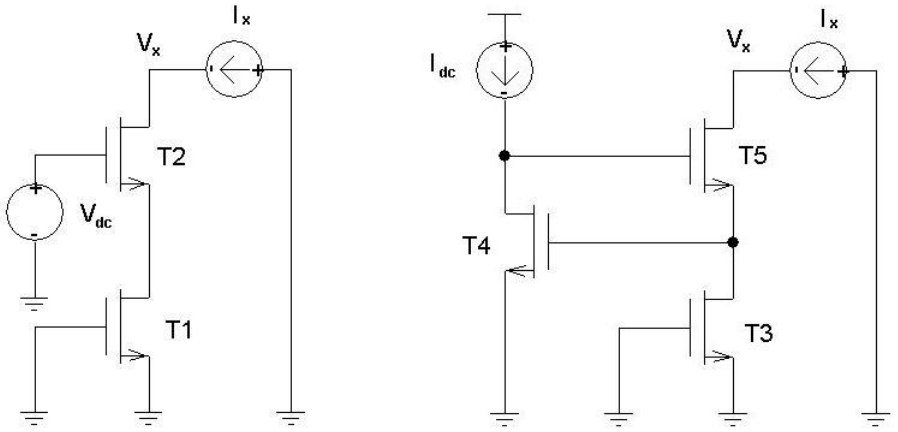

Figure 6.7: The classic cascode and the regulated cascode.

6.3 Differential Cascode

The current mirror inverts the polarity of the signal, so the ToT stage has to be optimized to the new polarity. Furthermore, the current buffer requires an accurate DC voltage value at the output to have all transistor saturated: the voltage value ($\approx 500\ mV$) is fixed by the current flowing in the regulated cascode but the voltage value of the ToT input is also fixed ($179\ mV$) by the current flowing in the input transistor. When the buffer and the ToT stage are connected together, the regulated cascode has not all the transistors saturated.
A differential stage, which replaces the cascode used as the core amplifier of the ToT stage, avoids these problems. In Fig.6.8 the differenzial cascode amplifier is shown. A reference voltage value (V_{dc14}) is applied at the positive input, while the signal is applied at the negative one. If the amplifier has enough open-loop gain, by virtue of the virtual ground principle, node $V_{dc,14}$ will track the reference voltage applied to the other input of the differential stage. By a proper regulation of the reference voltage, the DC output of the buffer can be set at value adequate to keep all transistors in saturation.

The feedback capacitance value is $C_{fb} = 125\ fF$. The current flowing in the differential cascode is fixed by a current mirror. The open loop gain

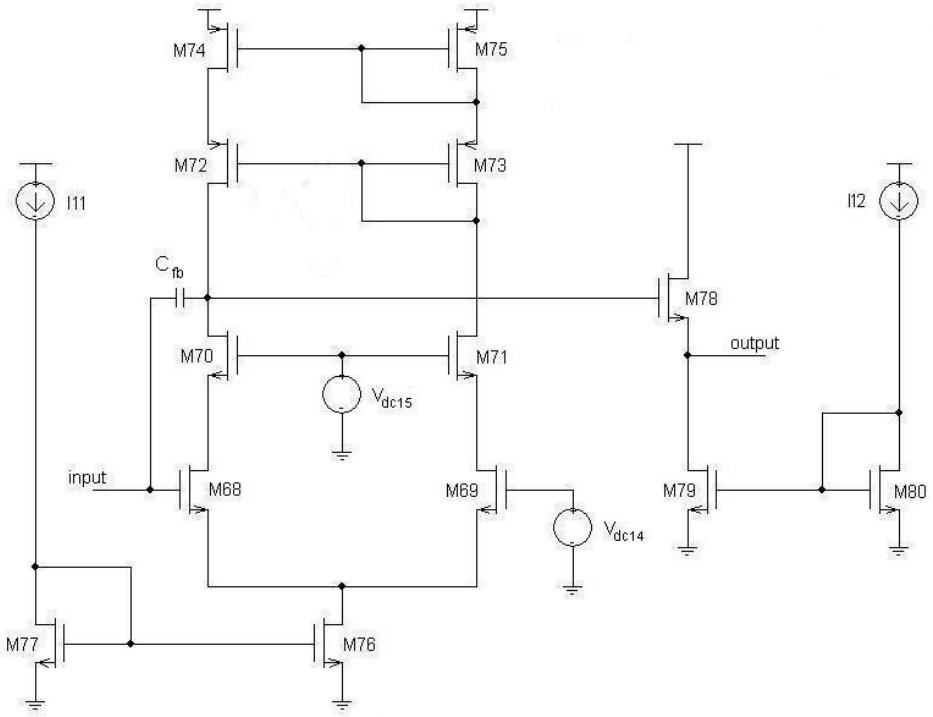

Figure 6.8: The differential cascode.

$(W/L)_{M68}$	$125\mu m/1\mu m$
$(W/L)_{M69}$	$125\mu m/1\mu m$
$(W/L)_{M70}$	$80\mu m/1\mu m$
$(W/L)_{M71}$	$80\mu m/1\mu m$
$(W/L)_{M72}$	$50\mu m/1\mu m$
$(W/L)_{M73}$	$50\mu m/1\mu m$
$(W/L)_{M74}$	$60\mu m/1\mu m$
$(W/L)_{M75}$	$60\mu m/1\mu m$
$(W/L)_{M76}$	$20\mu m/1\mu m$
$(W/L)_{M77}$	$20\mu m/1\mu m$
$(W/L)_{M78}$	$15\mu m/500nm$
$(W/L)_{M79}$	$20\mu m/2\mu m$
$(W/L)_{M80}$	$20\mu m/2\mu m$

Table 6.3: Sizes of transistors.

of the circuit is given by:

$$A = g_{m,68} Z_{out}$$

with Z_{out} output impedance of the cascode configuration made by the tran-

$I11$	$80\mu A$
$I12$	$50\mu A$
$V_{dc,14}$	$489.66mV$
$V_{dc,15}$	$560mV$

Table 6.4: Voltage and current values.

sistors $M68, M70, M72, M74$ and $g_{m,68}$ transconductance of $M68$. Since $M68$ works in weak inversion, $g_{m,68}$ is proportional to the current flowing in it. The value of the amplification of the differential cascode obtained by the small signal model is $A = 365$; the value given by the simulation is $A = 311$.

6.4 Constant Current Feedback

The buffer imposes a change in the constant current feedback stage. The DC voltage value at the input of the ToT stage is not compatible with the four transistors making the cascode configuration of the differential stage: the voltage difference between the source of $M45$ and the input node is too small to have $M47$ saturated.
In Fig.6.9 the new configuration is showed.

$(W/L)_{M45}$	$3\mu m/10\mu m$
$(W/L)_{M46}$	$3\mu m/10\mu m$
$(W/L)_{M49}$	$1\mu m/30\mu m$
$(W/L)_{M52}$	$4\mu m/22\mu m$
$(W/L)_{M53}$	$4\mu m/22\mu m$
$(W/L)_{M54}$	$5\mu m/10\mu m$
$(W/L)_{M55}$	$5\mu m/10\mu m$
$(W/L)_{M56}$	$20\mu m/30\mu m$
$(W/L)_{M57}$	$20\mu m/30\mu m$
$(W/L)_{M81}$	$2.5\mu m/10\mu m$
$(W/L)_{M82}$	$10\mu m/30\mu m$

Table 6.5: Sizes of transistors.

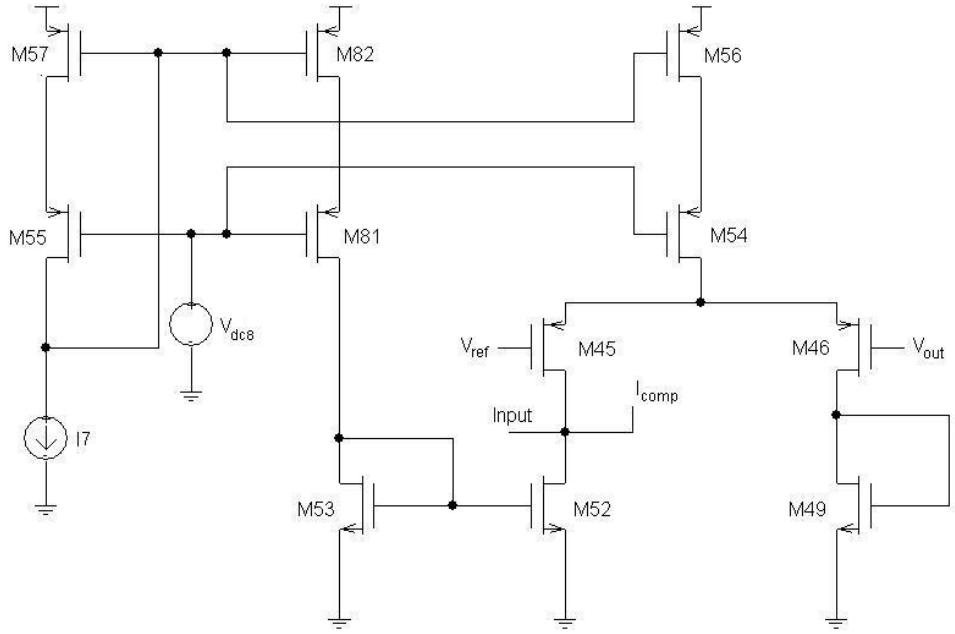

Figure 6.9: The constant current feedback.

$I7$	$200nA$
$V_{dc,8}$	$650mV$

Table 6.6: Voltage and current values.

6.5 Linearity

The linearity of the ToT stage has been studied using the same method used to test the linearity of the ToT stage in the previous configuration but using as input node the input of the buffer. The linearity of the complete chain has been studied, too (the input node is the input of the preamplifier): the relation between Q_{in} and ToT is linear. The minimum charge for which the linearity is better than 10% is $\approx 4\ fC$. The issue of non-linearity for small charges will be discussed in more detail in chapter 7.

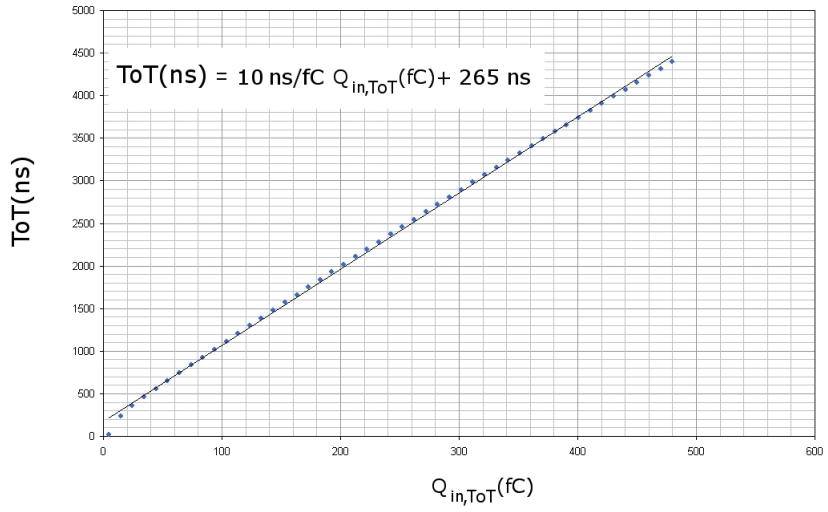

Figure 6.10: Linearity of the ToT stage, the charge is injected in the ToT stage.

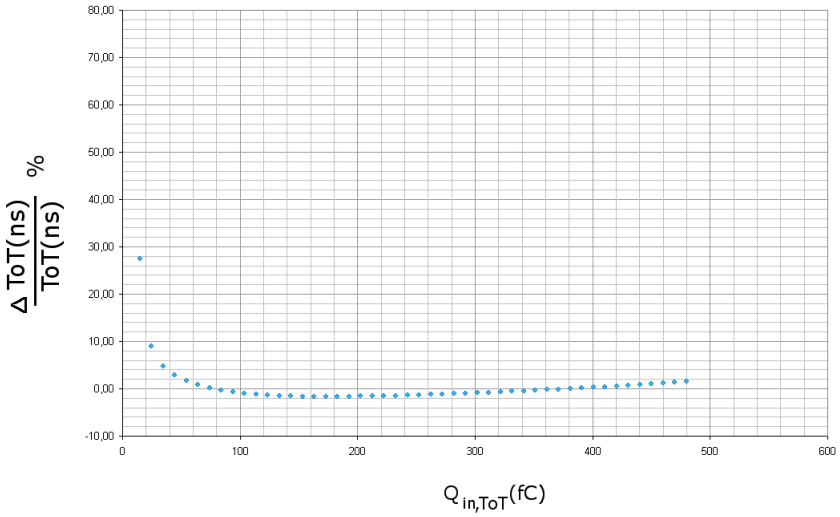

Figure 6.11: Relative percent error of the ToT stage.

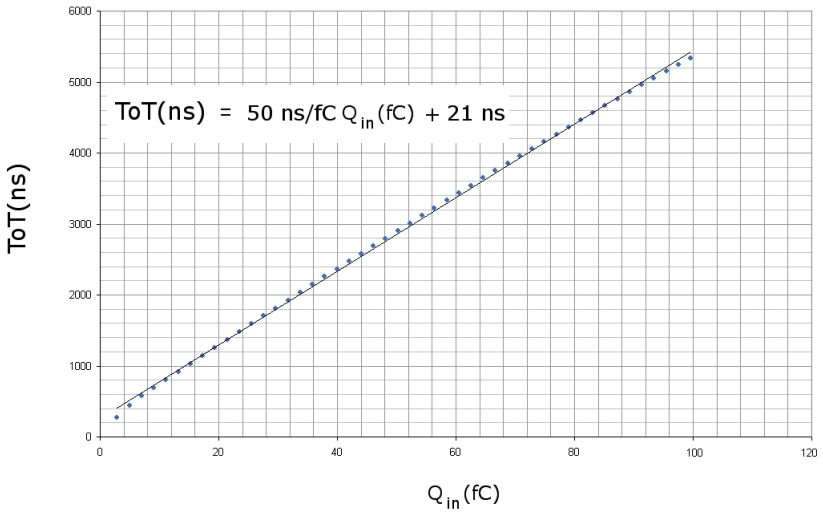

Figure 6.12: Linearity of the whole system, the charge is injected in the preamlifier.

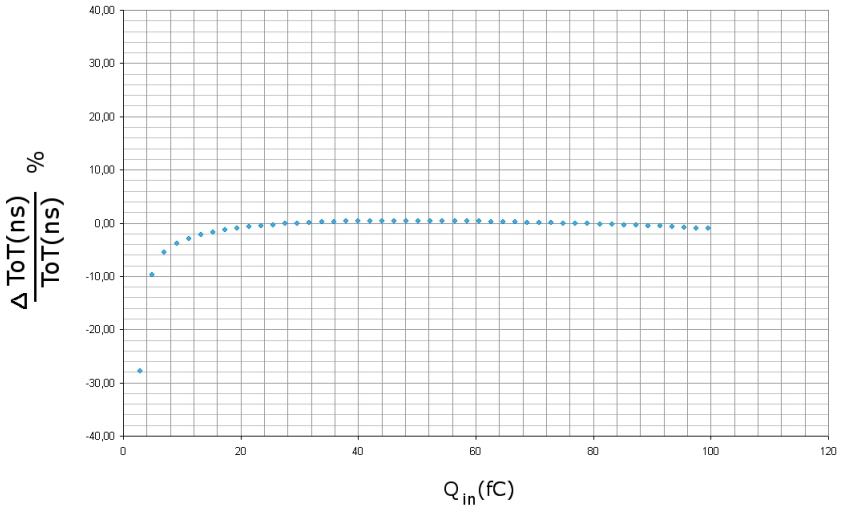

Figure 6.13: Relative percent error of the ToT with the charge injected at the input of the system.

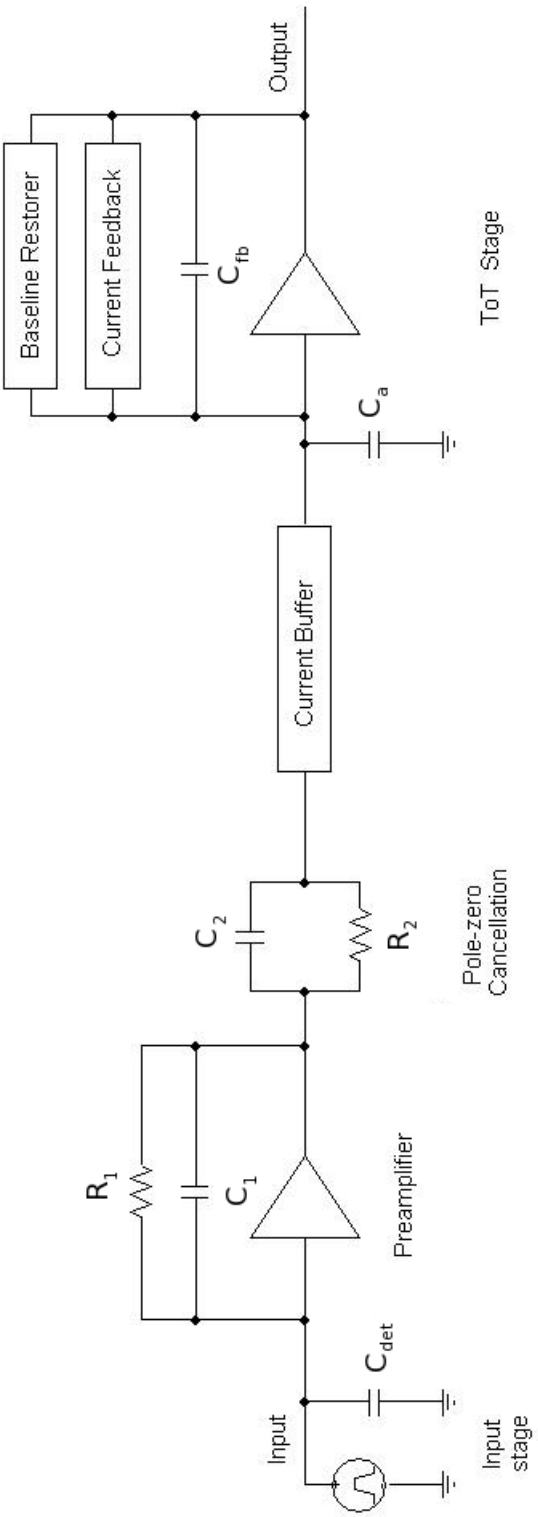

Figure 6.14: The full chain.

Chapter 7

System Optimization

In this chapter we discuss some aspects related to the optimization of the performance of our circuit. In particular, the performance of the circuit has been tested by changing the shape of the input signal, by improving the signal to noise ratio, by extending the linearity of the system also to very small input charges. In the end, a comparator has been connected at the output of the ToT stage, to complete the front-end architecture.

7.1 Input signal

The first study regards the relation between the ToT and the shape of the input current signal (in particular, the fall time of the input current pulse). The signal coming from the detector is amplified by the preamplifier which changes the shape of the signal. In fact, the fall time of the signal at the output of the preamplifier depends on the costant $\tau = \frac{1}{RC}$ due to the RC filters placed in the preamplifier. If the value of the input charge is fixed, a change of the fall time of the input signal should not influence the following stage and the ToT measurement.
A fix charge (Q_{in}) has been chosen; the fall time of the input signal has been changed and, consequently, the current injected in the preamplifier has been adjusted to have a constant charge at the input. Infact

$$Q_{in} = Iinj(\frac{t_{fall} + t_{rise}}{2} + t_{width})$$

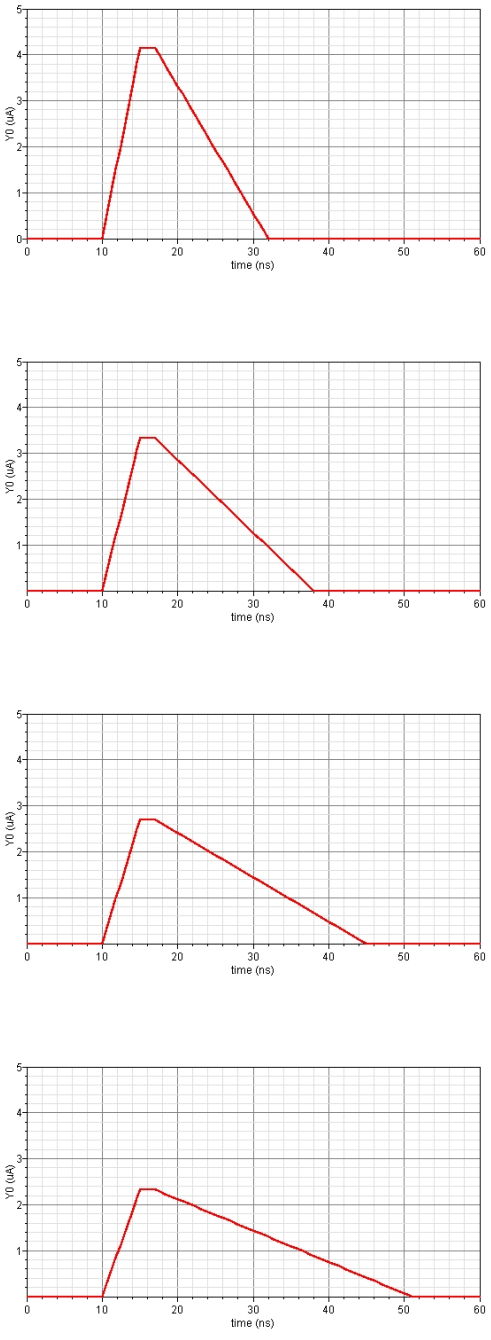

Figure 7.1: Examples of input signal with identical charge and different shape.

with $Q_{in} = 4\ fC$, $t_{rise} = 5\ ns$ and $t_{width} = 2\ ns$. Consequently

$$I_{inj} = \frac{2Q_{in}}{t_{fall} + t_{rise} + 2t_{width}} = \frac{8fC}{t_{fall} + 9ns}$$

t_{fall} (ns)	I_{inj} (nA)	ToT (ns)
15	333	326
16	320	327
17	308	327
18	296	327
19	286	327
20	276	327
21	267	327
22	258	327
23	250	328
24	242	328
25	235	328
26	228	328
27	222	328
28	216	328
29	210	329
30	205	329

Table 7.1: The t_{fall}, I_{inj} and ToT values, $Q_{in} = 4\ fC$.

The simulation has been repeated with $Q_{in} = 50\ fC$ and $Q_{in} = 100\ fC$, obtaining the results shown in Tab. 7.2 and in Tab. 7.3.

The time resolution of the system is $\approx 2\ ns$. Infact, the clock frequency of the digital readout electronic is 160 MHz corresponding to a period of $\tau = 6.25\ ns$. The time calculated t has a standard deviation given by:

$$\sigma = \sqrt{\int_{-\tau}^{\tau} \frac{t^2}{\tau} dt} = \frac{\tau}{\sqrt{12}} \approx 2ns$$

Since the ToT variations are $\approx 2\ ns$, which is the same value of the time resolution of the complete system, the response of the system is not influenced by the variations of the input current signal shape.
The response of the circuit has been also studied for long fall time input signal.

t_{fall} (ns)	I_{inj} (μA)	ToT (μs)
15	4.16	2.414
16	4.0	2.414
17	3.85	2.415
18	3.70	2.415
19	3.57	2.415
20	3.45	2.415
21	3.33	2.415
22	3.23	2.415
23	3.13	2.415
24	3.03	2.415
25	2.94	2.415
26	2.86	2.415
27	2.78	2.415
28	2.70	2.415
29	2.63	2.415
30	2.56	2.415

Table 7.2: The t_{fall}, I_{inj} and ToT values, $Q_{in} = 50\ fC$.

t_{fall} (ns)	I_{inj} (μA)	ToT (μs)
15	8.33	4.319
16	8.00	4.319
17	7.69	4.320
18	7.41	4.320
19	7.14	4.319
20	6.89	4.319
21	6.67	4.319
22	6.45	4.320
23	6.25	4.320
24	6.06	4.320
25	5.88	4.320
26	5.71	4.320
27	5.55	4.320
28	5.40	4.320
29	5.26	4.321
30	5.13	4.321

Table 7.3: The t_{fall}, I_{inj} and ToT values, $Q_{in} = 100\ fC$.

Since the transfer function of the first stage of the preamplifier is given

Q_{in} (fC)	t_{fall} (ns)	I_{inj} (μA)	ToT (μs)
4	50	0.13	0.330
	100	0.07	0.338
50	50	1.69	2.415
	100	0.92	2.415
100	50	3.39	4.322
	100	1.83	4.325

Table 7.4: The t_{fall}, I_{inj} and ToT values for long fall time input signal.

by:

$$T(s) = \frac{R_1}{1 + sR_1C_1}$$

When the frequency of the input signal is lower than the cut-off frequency of the circuit ($s \ll \frac{1}{R_1C_1}$), the transfer function becomes $T(s) \approx R_1$ and the stage acts as an amplifier: since the impedance of the feedback capacitance is large ($Z_C = \frac{1}{sC}$), the current signal flows only through the resistor. When the frequency of the input signal is higher than the cut-off frequency ($s \gg \frac{1}{R_1C_1}$), the stage acts as an integrator.

7.2 Small Charges Linearity

The ToT is directly proportional to the charge injected at the input but this relation is no longer valid for too small charges injected: the missed linearity is caused by the differential stage of the current feedback (Sec. 5.2) which doesn't provide constant current. In fact, when a too small charge at the input of the ToT stage causes a voltage different between the input nodes of the differential stage lower than 40 mV, it is not fully unbalanced and, consequently, only a fraction of $I_{fb}/2$, depending on the output signal amplitude, flows in the input. Since the current provided by the feedback is no more constant, the relation between the input charge and the ToT is no more linear.

The ToT error has been calculated, to decide the minimum charge which has a direct proportionality with the ToT: it is given by the distance between the ToT values obtained by the simulation and the corresponding value

belonging to the best fit (Fig.6.12). Since

$$Q_{in} = \alpha ToT$$

with $\alpha = 5 \cdot I_{discharge}$ constant term (the factor 5 is given by the close loop gain of the preamplifier), the charge error is given by:

$$\sigma_{Q_{in}} = \frac{dQ_{in}}{dToT}\sigma_{ToT} = \alpha\sigma_{ToT} \tag{7.1}$$

The charge having $\frac{\sigma_{Q_{in}}}{Q_{in}} = 0.1$ has been chosen as minimum charge having a linear relation with the ToT: smaller charges have a higher error and a no-linear relation while higher charges have a smaller error and a linear relation. The minimum charge of the circuit having the linear relation is $Q_{in} \approx 4\ fC$. To improve the linearity of the circuit is possible by increasing the gain of the preamplifier because the voltage peak of each signal becomes higher.
The preamplifier has been modified to have a close loop gain of 7. The new value of the minimum charge having the linear relation is 3.03 fC but the relation between Q_{in} and ToT is not anymore linear for high input charge (Fig. 7.3). In fact, when a too high charge arrives at the ToT stage, the voltage variation at the input pushes the current feedback out of saturation. In fact, if the $V_{ds,52}$ decreases its value, $M52$ works in linear region, decreasing its current. Since its current value increases but the current flowing in $M45$ is the same, the current flowing at the input node increases. This current excess allows to the input node to have a faster discharge and a lower ToT.

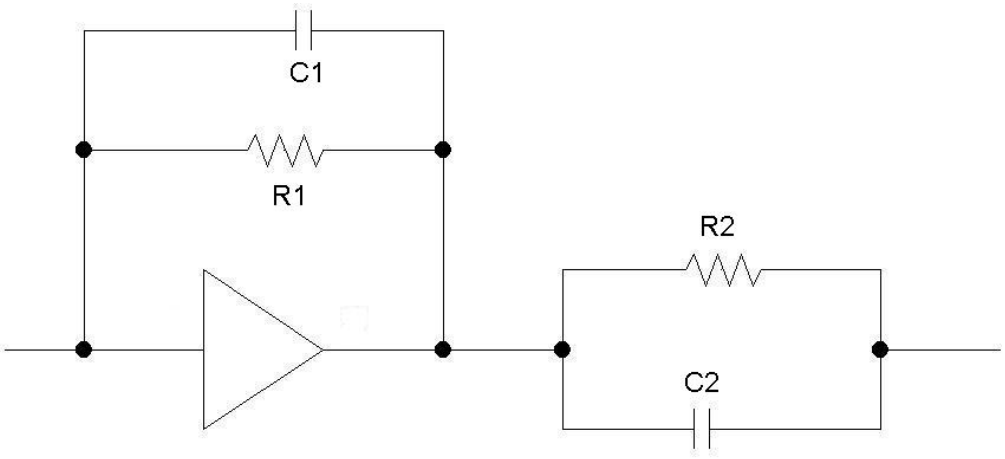

Figure 7.2: Schematic of the complete preamplifier.

$R1$	$1M\Omega$
$C1$	$200fF$
$R2$	$142.857k\Omega$
$C2$	$1.86pF$

Table 7.5: Resistors and capacitors values of the preamplifier.

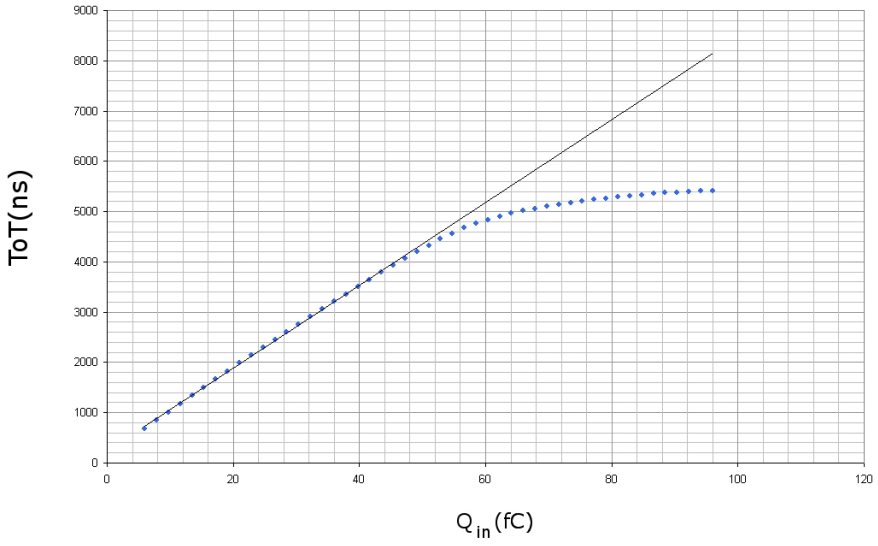

Figure 7.3: The linearity of the ToT stage when the closed loop gain value of the preamplifier is 7.

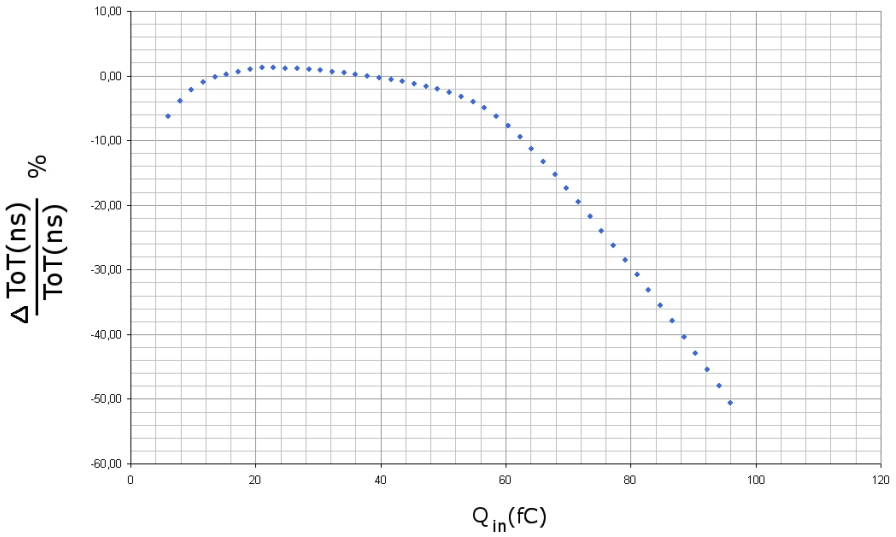

Figure 7.4: Relative percent error of the ToT with the charge injected at the input of the system and when the closed loop gain of the preamplifier is 7.

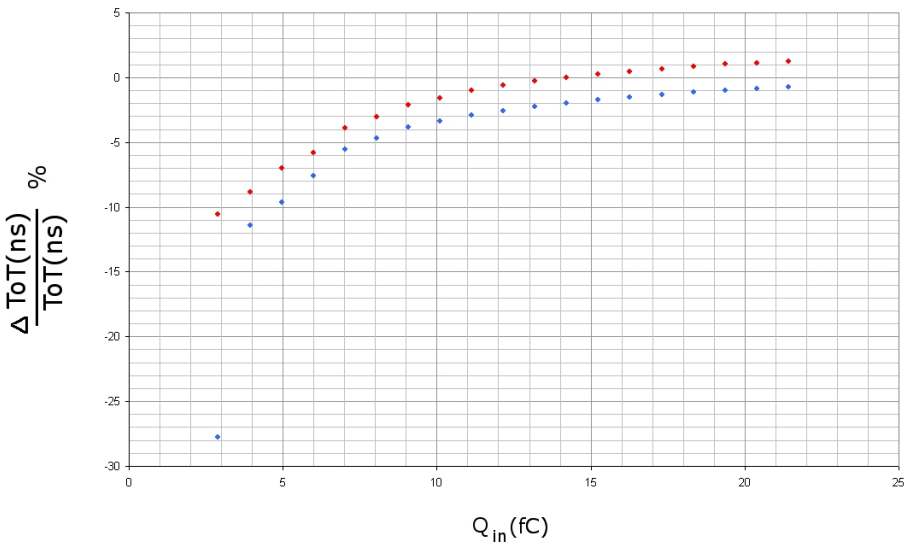

Figure 7.5: Relative percent error of the ToT with small charges injected at the input of the system when the closed loop gain of the preamplifier is 7 (red dots) and when it is 5 (blue dots).

7.3 ENC Optimization

The ENC (Sec.3.1.2) of the system has been studied to try to increase the noise performance of the circuit. The ENC is given by the ratio between the RMS noise and the voltage value obtained at the output of the system when there is the charge of one electron at the input:

$$ENC = \frac{RMS}{V_{out,1e^-}} \tag{7.2}$$

Since the system resolution doesn't allow to reveal the charge of one electron, the voltage value at the output due to a electron charge has been obtained by dividing the voltage output value obtained by a test charge of 1 fC with the number of electrons contained in 1 fC ($6250e^-$):

$$ENC = \frac{RMS}{V_{out,1fC}}\, 6250$$

Since the noise has a Gaussian probability distribution, theoretically the noise amplitude is unlimited but practically the noise amplitude is given by:

$$V_{noise,pp} = \pm 3 V_{RMS} \tag{7.3}$$

The CAD allows also to have transient noise simulation plotting the noise voltage versus the time: the $V_{noise,pp}$ value at the output of the system when there is no charge at the input can be calculated and, consequently, the RMS noise value of the circuit, given by:

$$V_{RMS} = \frac{V_{noise,pp}}{6}$$

Moreover, the CAD allows to calculate automatically the RMS value of the circuit, giving a more accurate result. The value of the RMS calculated by the CAD is $V_{RMS} = 13.55\ mV$. The ENC of the overall system is given by:

$$ENC = \frac{13.55mV}{28mV}\, 6250 \approx 3024e^-$$

The CAD can also identify the most influential noise source of the circuit and the type of noise (thermal, shot or low-frequency noise). It is the transistor $M1$, belonging to the first stage of the system, according to the noise theory and the noise is thermal-type: by decreasing the noise in the first

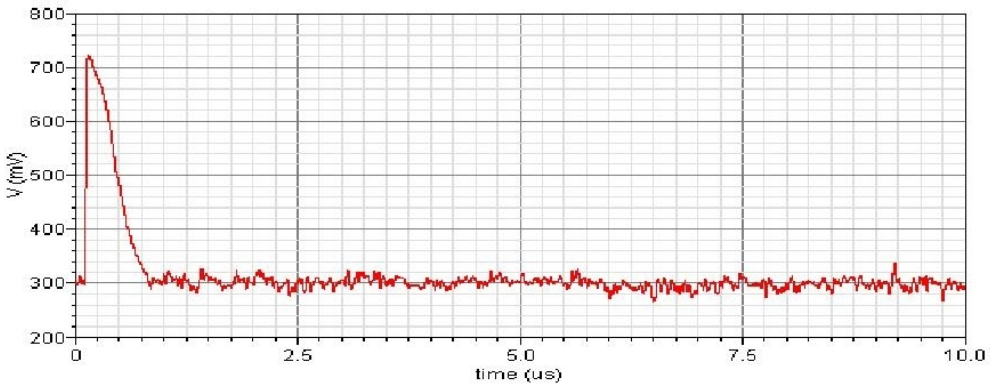

Figure 7.6: An example of noise simulation.

stage, to decrease the noise of the entire circuit becomes possible. Since $ENC_{th} \propto g_{M1}^{-1}$, it is useful to increase the gain of the first stage of the amplifier. To avoid to have a circuit which spent too much power, the current flowing in the ToT stage has been decreased while the current flowing in the preamplifier has been increased. In the following tables, the modifications of the circuit are showed.

$(W/L)_{M1}$	$1.5mm/500nm$
$(W/L)_{M2}$	$50\mu m/500nm$
$(W/L)_{M3}$	$60\mu m/500nm$
$(W/L)_{M4}$	$120\mu m/2\mu m$
$(W/L)_{M5}$	$120\mu m/2\mu m$
$(W/L)_{M6}$	$60\mu m/500nm$
$(W/L)_{M7}$	$120\mu m/2\mu m$
$(W/L)_{M8}$	$60\mu m/500nm$
$(W/L)_{M9}$	$120\mu m/2\mu m$
$(W/L)_{M10}$	$60\mu m/500n$
$(W/L)_{M11}$	$10\mu m/500nm$
$(W/L)_{M12}$	$15\mu m/1\mu m$
$(W/L)_{M13}$	$15\mu m/1\mu m$

Table 7.6: Sizes of transistors of the preamplifier.

$I1$	$130\mu A$
$I2$	$220\mu A$
$I3$	$100\mu A$
$V_{dc,1}$	$450mV$
$V_{dc,2}$	$570mV$
$V_{dc,3}$	$450mV$

Table 7.7: Voltage and current values of the preamplifier.

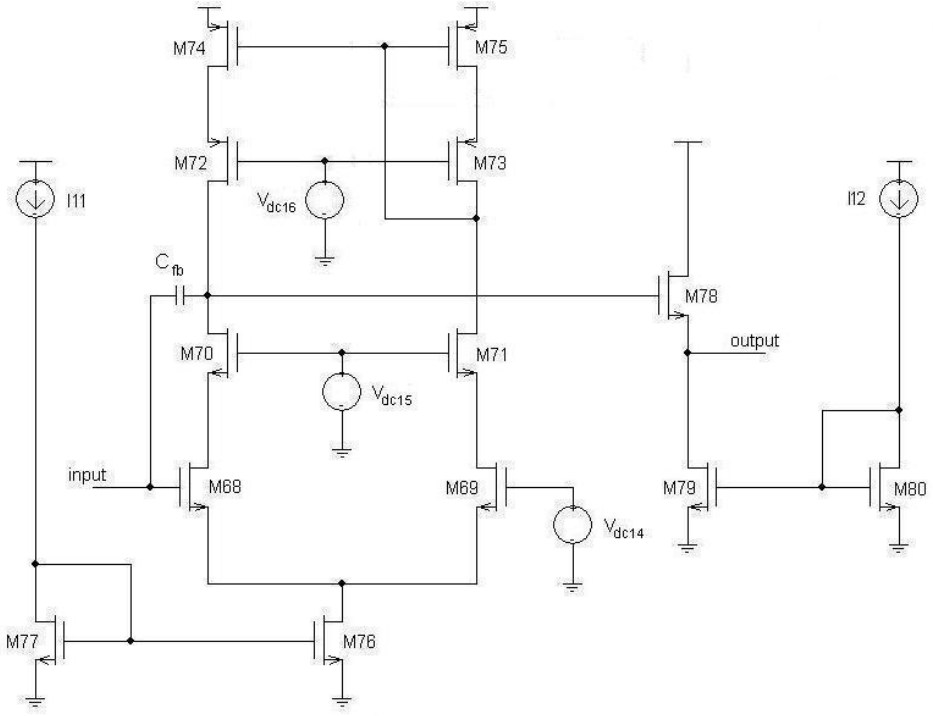

Figure 7.7: The new configuration of the differential cascode used in the ToT stage.

The new value of the ENC is:

$$ENC = \frac{11.35mV}{36.19mV}\, 6250 \approx 1960e^{-}$$

The most influential noise sources after the modifications are the transistor $M61$,$M62$,$M58$ and $M59$ of the current buffer and their contribution is given through the $1/f$ noise. Since $ENC_{1/f} \propto (WL)^{-1}$, it is useful to increase the sizes of the transistors, paying attention to have all transistors saturated. In Tab. 7.10, the modifications of the transistors sizes are

$(W/L)_{M68}$	$125\mu m/500nm$
$(W/L)_{M69}$	$125\mu m/500nm$
$(W/L)_{M70}$	$70\mu m/1.5\mu m$
$(W/L)_{M71}$	$70\mu m/1.5\mu m$
$(W/L)_{M72}$	$50\mu m/2\mu m$
$(W/L)_{M73}$	$50\mu m/2\mu m$
$(W/L)_{M74}$	$80\mu m/1\mu m$
$(W/L)_{M75}$	$80\mu m/1\mu m$
$(W/L)_{M76}$	$20\mu m/1\mu m$
$(W/L)_{M77}$	$20\mu m/1\mu m$
$(W/L)_{M78}$	$15\mu m/1\mu m$
$(W/L)_{M79}$	$20\mu m/2\mu m$
$(W/L)_{M80}$	$20\mu m/2\mu m$

Table 7.8: Sizes of transistors of the differential cascode.

$I11$	$20\mu A$
$I12$	$5\mu A$
$V_{dc,14}$	$489.66mV$
$V_{dc,15}$	$600mV$
$V_{dc,16}$	$750mV$

Table 7.9: Voltage and current values of the differential cascode.

showed.

$(W/L)_{M58}$	$30\mu m/1.5\mu m$
$(W/L)_{M59}$	$30\mu m/1.5\mu m$
$(W/L)_{M61}$	$20\mu m/1.5\mu m$
$(W/L)_{M62}$	$20\mu m/1.5\mu m$

Table 7.10: Sizes of transistors of the current buffer.

The most influential noise source after the modification is the input transistor of the preamplifier. The final value of the ENC has been obtained by increasing the current in the input transistor ($I_2 = 300\ \mu A$). The value of the ENC is:

$$ENC = \frac{5.9mV}{31.3mV}\, 6250 \approx 1178e^{-}$$

The simulation has been made by using the minimum value of detector

capacitance $C_{det} = 10\ pF$. The ENC value obtained is:

$$ENC = \frac{5.2mV}{31.3mV}\ 6250 \approx 1038e^{-}$$

Since $ENC \propto C_{det}$, the value obtained with the capacitance $C_{det} = 10\ pF$ is lower than the previous value.

7.4 The comparator

The discriminator compares the output voltage of the ToT stage with a reference voltage, switching its output to indicate which is larger. Since its output can have only two voltage output levels ($0\ V$ and $1.2\ V$), compatible with the digital logic levels 0 and 1, it is the stage used to connect the analog circuit with the digital part of the front-end electronic.
The ToT voltage output is connected to the positive input while the reference voltage is connected to the negative input of the comparator: it is fixed at 330 mV, that is the voltage value chosen to calculate the ToT. When there is no signal at the input of the system, the voltage output of the ToT stage is lower than 330 mV, the voltage value of the negative input is higher than the voltage value of the positive input and, consequently, the output voltage of the comparator is $0\ V$; when there is a signal at the input of the system which allows to the ToT voltage to be higher than the reference voltage, the comparator switches its output and its voltage output becomes 1.2 V. When the ToT voltage becomes again lower than 330 mV, the voltage at the output of the comparator returns back to $0\ V$ (Fig. 7.8).

In Fig. 7.9, the schematic of comparator is showed: it is made by a classic differential stage. The current of the circuit is given by the current mirror made by $M83$, $M84$ and $M85$. The transistors $M86$, $M87$ and $M90$ act as current sources. Since the ratio between the sizes of $M86$ and $M85$ ($\frac{(W/L)_{M86}}{(W/L)_{M85}} = 4$) and the ratio between the sizes of $M90$ and $M84$ ($\frac{(W/L)_{M90}}{(W/L)_{M84}} = 5$) are different, the total current flowing in $M86$ and $M87$ ($I = 8 \cdot I13$) is higher than the current flowing in $M90$ ($I = 5 \cdot I13$). Consequently, the current flowing in $M86$ is divided between $M88$ and $M91$ (and the current flowing in $M87$ is divided between $M89$ and $M92$). In this way, the sum of the currents flowing in $M88$ and $M89$ is equal to the current

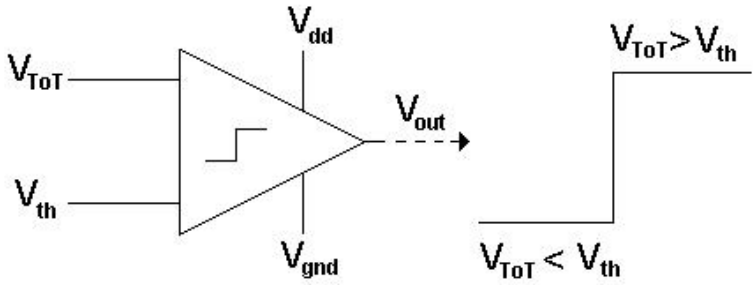

Figure 7.8: The output of a the comparator: when $V_{ToT} < V_{th}$, the value of the output voltage is $V_{gnd} = 0V$, while when $V_{ToT} > V_{th}$, the value of the output voltage is $V_{dd} = 1.2\ V$.

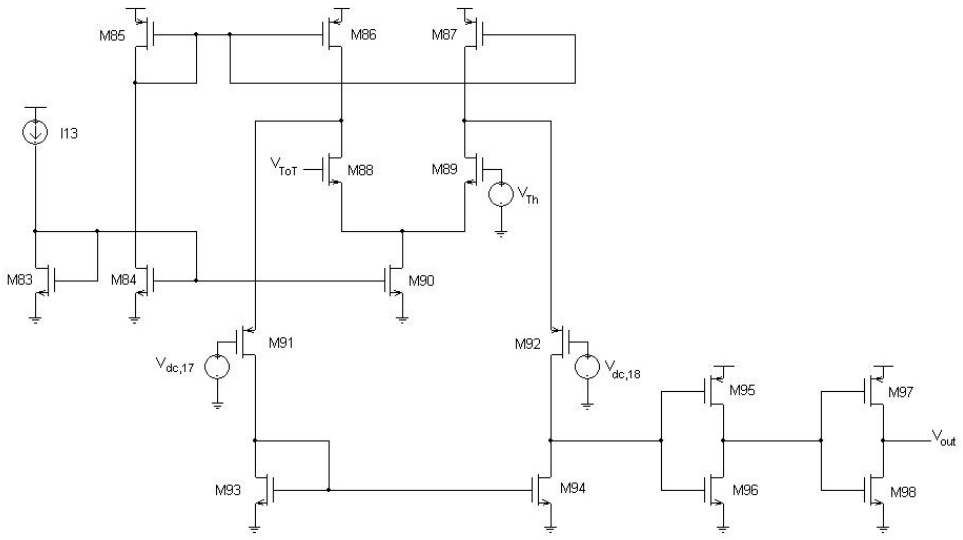

Figure 7.9: The schematic of the comparator.

$(W/L)_{M83}$	$1\mu m/1\mu m$
$(W/L)_{M84}$	$1\mu m/1\mu m$
$(W/L)_{M85}$	$750nm/3\mu m$
$(W/L)_{M86}$	$3\mu m/3\mu m$
$(W/L)_{M87}$	$3\mu m/3\mu m$
$(W/L)_{M88}$	$24\mu m/500nm$
$(W/L)_{M89}$	$24\mu m/500nm$
$(W/L)_{M90}$	$5\mu m/1\mu m$
$(W/L)_{M91}$	$1\mu m/1\mu m$
$(W/L)_{M92}$	$1\mu m/1\mu m$
$(W/L)_{M93}$	$3\mu m/3\mu m$
$(W/L)_{M94}$	$3\mu m/3\mu m$
$(W/L)_{M95}$	$700nm/140nm$
$(W/L)_{M96}$	$300nm/140nm$
$(W/L)_{M97}$	$14.01\mu m/140nm$
$(W/L)_{M98}$	$6\mu m/140nm$

Table 7.11: Sizes of transistors of the comparator.

$I13$	$1\mu A$
V_{th}	$330mV$
$V_{dc,17}$	$200mV$
$V_{dc,18}$	$200mV$

Table 7.12: Voltage and current value of the comparator.

flowing in $M90$.

When $V_{ToT} = V_{Th}$ (Fig. 7.10) the current flowing in $M88$ (branch A) and $M89$ (branch B) is the same ($\frac{I_b}{2}$); since $I_a > \frac{I_b}{2}$, the current in excess coming from $M86$ flows in $M91$ (branch C) and the current in excess coming from $M87$ flows in $M92$ (branch D): the current flowing in the branches C and D, and consequently in $M93$ and $M94$, is the same ($I_c = I_a - \frac{I_b}{2}$). The voltage value of the gate and the drain of $M94$, in this situation, are respectively called V_A and V_B.

When $V_{ToT} < V_{Th}$ (Fig. 7.11), the current flowing in the branch A ($\frac{I_b}{2} - \Delta I$)is lower than the current flowing in the branch B ($\frac{I_b}{2} + \Delta I$). Since the current given by $M86$ is constant (I_a) and the current flowing in the branch A decreases, the current flowing in the branch C, and in $M93$, increases ($I_c + \Delta I$) and the voltage value of the gate of $M93$ increases ($V_A + \Delta V_A$). In the meantime, the current flowing in the branch B increases and the current

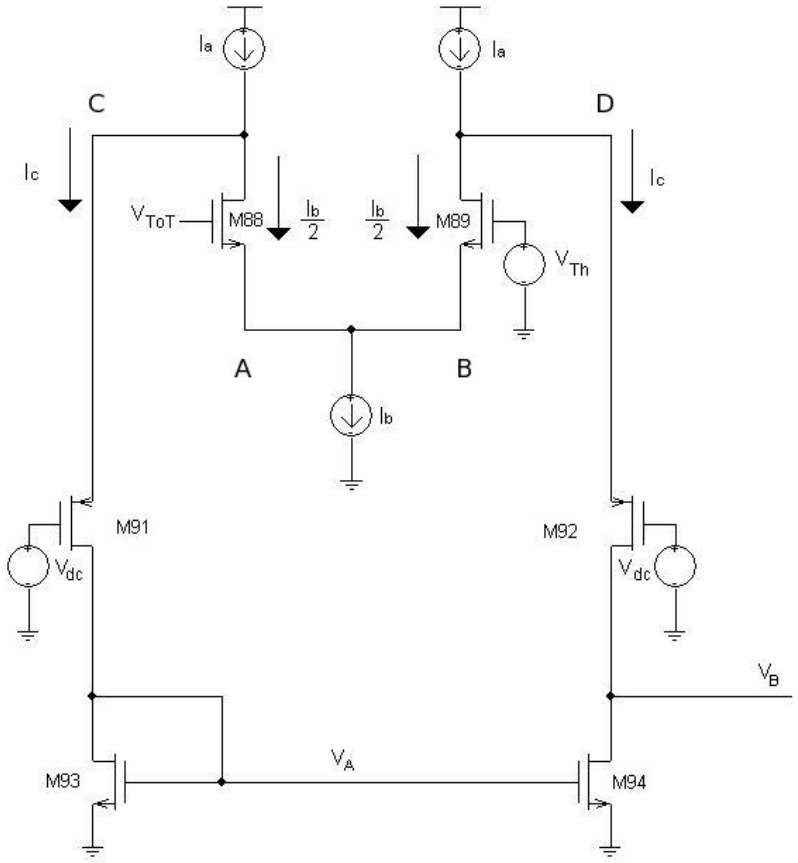

Figure 7.10: The comparator having $V_{ToT} = V_{Th}$.

flowing in the branch D, and in $M94$, decreases. Since the current flowing in $M94$ decreases but its V_{gs} increases ($V_A + \Delta V_A$), its drain-source voltage decreases ($V_B - \Delta V_B$).

When $V_{ToT} > V_{Th}$ (Fig. 7.12), the current flowing in the branch A increases, the current in the branch C decreases and the gate-source voltage of $M93$ decreases its value ($V_A - \Delta V_A$). In the meantime, the current flowing in the branch B decreases, the current in the branch D increases and the current flowing in $M92$, and consequently in $M94$, increases its value. Since the gate-source voltage of $M94$ decreases ($V_A - \Delta V_A$) but the current flowing increases, the drain-source voltage value increases its value ($V_B + \Delta V_B$). Summarizing, when $V_{ToT} < V_{Th}$, the voltage value V_B becomes $V_B - \Delta V_B$; when $V_{ToT} > V_{Th}$, the voltage value V_B becomes $V_B + \Delta V_B$.

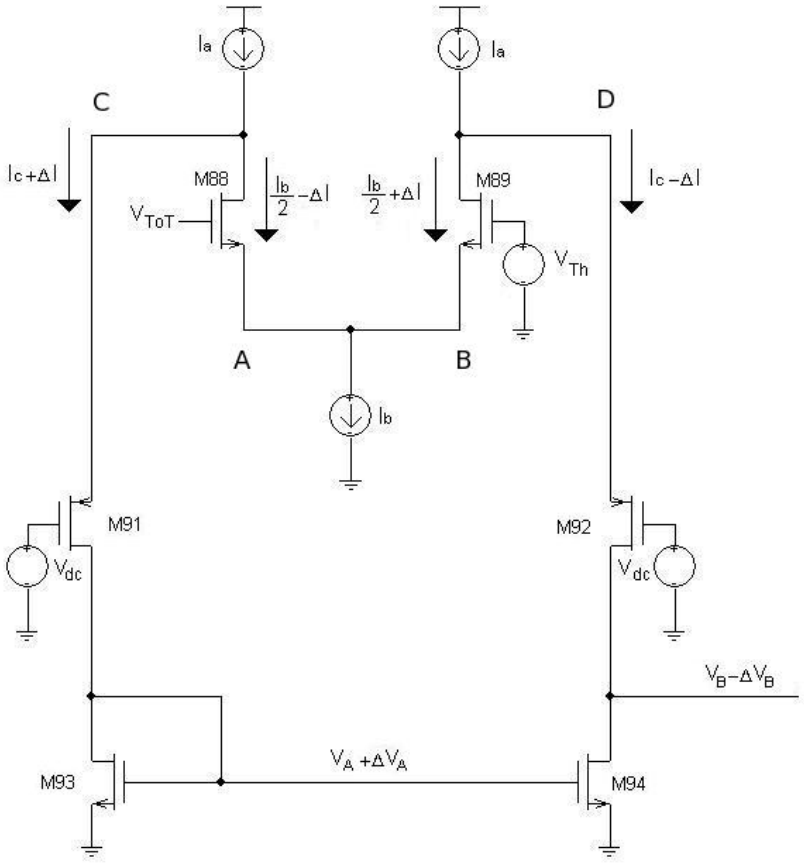

Figure 7.11: The comparator having $V_{ToT} < V_{Th}$.

The output voltage V_B is connected to two CMOS inverters: they are circuits which use a combination of n-type and p-type transistors to implement the boolean function $Y = \bar{A}$, where A is the input and Y the output of the circuit (Fig. 7.13). The transistors of the CMOS inverter act as switches which conduct only when the gain-source voltage is higher than the threshold voltage. When V_{in} is high, the p-mos transistor doesn't conduct because its source-gate voltage approaches zero; the n-mos transistor conducts because its source-gate voltage overcomes the threshold voltage. Consequently, the output voltage value is $V_{out} = 0V$. When V_{in} is low, the p-mos conducts while the n-mos doesn't conduct and the output voltage approaches V_{dd}. Summarizing, when the input is low, the output is high and when the input is high, the output is low.

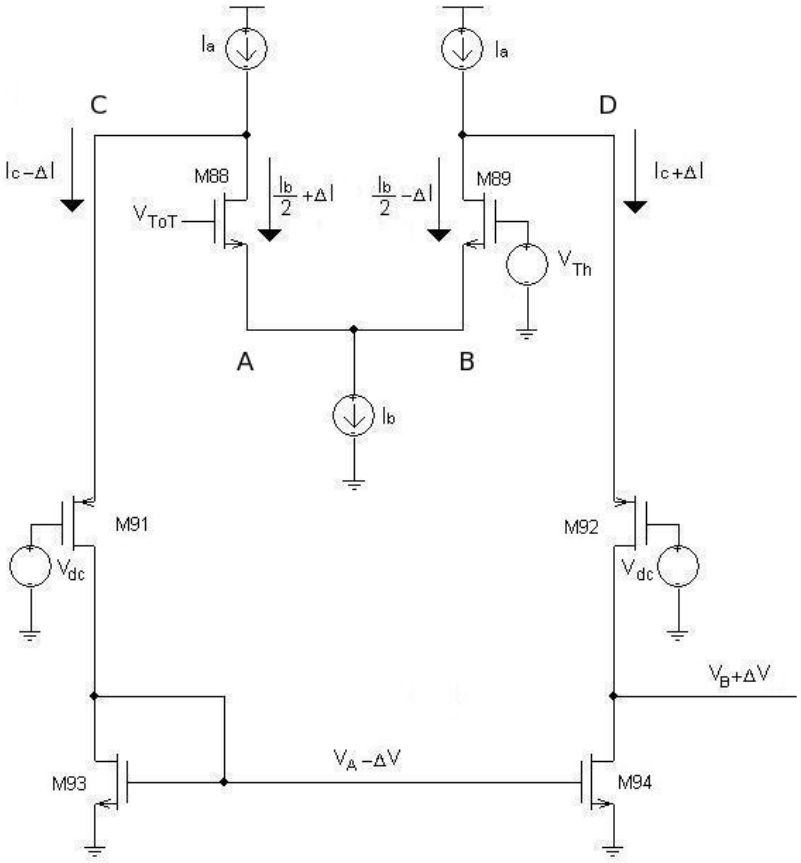

Figure 7.12: The comparator having $V_{ToT} > V_{Th}$.

The CMOS inverters used in the circuit are useful to have the output voltage value of the comparator equal to $0V$ or $1.2V$. Furthermore, two inverters are used to have the output voltage high when $V_{ToT} > V_{Th}$ and the output voltage low when $V_{ToT} < V_{Th}$.

In Fig. 7.14, the output of the ToT stage and the comparator are showed. The voltage value of the cross points of the two line is $\approx 330\ mV$. Since the time amplitude of the comparator output signal is directly proportional to the time amplitude of the ToT voltage output, which is directly proportional to the input charge, also the time spent between two switchings of the comparator is directly proportional to the input charge value. Consequently, it is possible to study the time linearity of the comparator as regards to the input charge (Fig. 7.15).

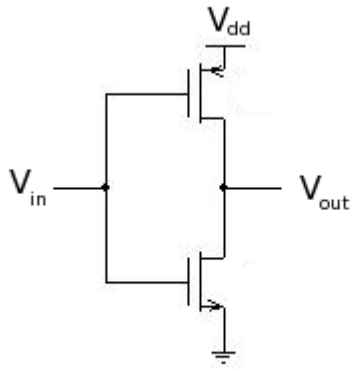

Figure 7.13: The CMOS inverter.

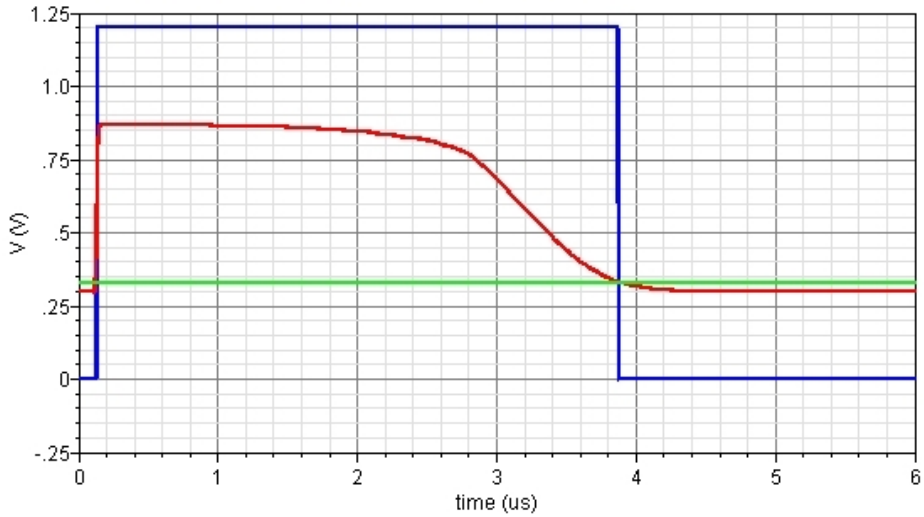

Figure 7.14: The output voltage of the comparator (blue line), of the ToT stage (red line) and the threshold voltage of the comparator, $V_{Th} = 330mV$ (green line).

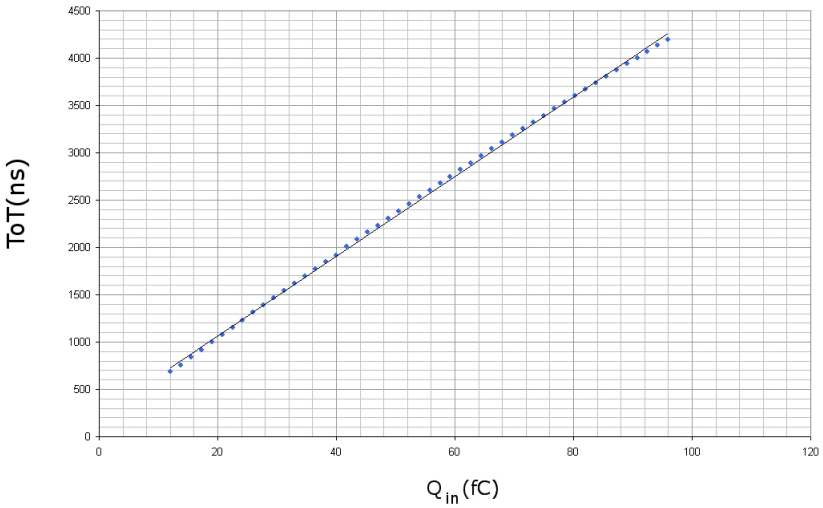

Figure 7.15: The linearity of the system with the comparator.

By knowing the rms noise of the system and the current discharging the input node, it is possible to calculated the jitter (Section 3.1.2) value at the output of the comparator:

$$jitter = \frac{rms_{noise}}{\frac{dV_{out}(t)}{dt}}$$

Since the rms noise of the system is 6 mV and the voltage variation at the output is:

$$\frac{dV_{out}(t)}{dt} = \frac{I_{fb}}{C_{fb}} = 6 \cdot 10^5 \frac{V}{s}$$

the jitter expected value is:

$$jitter \approx 10ns$$

Since the CAD allows to simulate the transient noise, it is possible to compare the expected and the simulated value of the jitter. In Fig. 7.16, the voltage at the output of the comparator after 30 transient noise simulations, is shown. The different switching-time is due to the noise of the system. In Fig. 7.17, the ToT variations during the transient noise simulation are shown. The jitter value obtained by the transient noise simulation is ≈ 12 ns, in good agreement with the expected value.

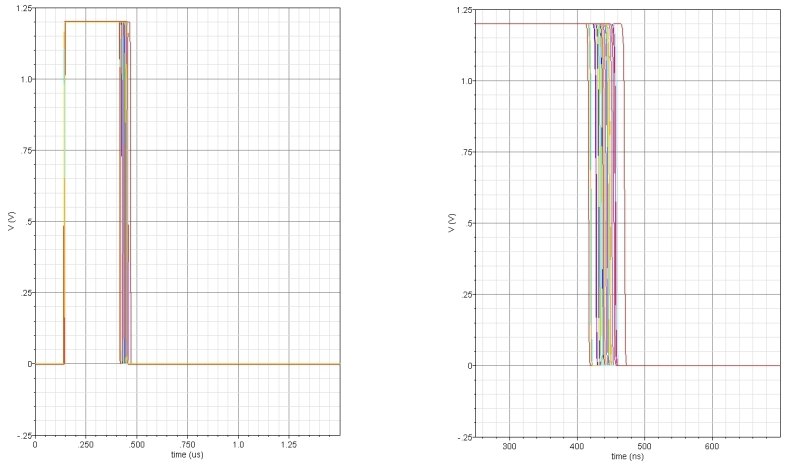

Figure 7.16: The voltage output of the comparator after 30 transient noise simulations, with particular attention to the different trailing edge.

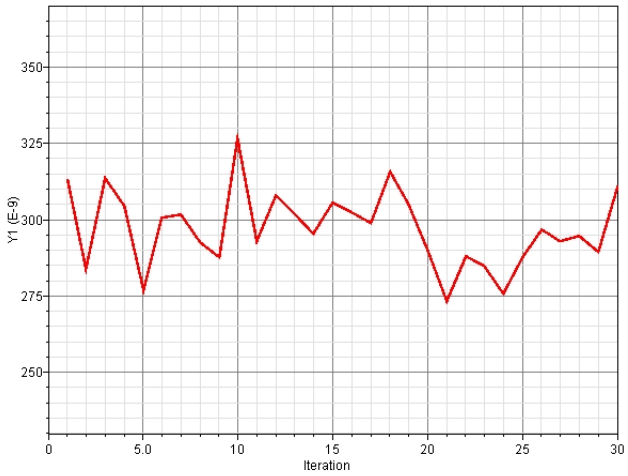

Figure 7.17: The ToT variations during 30 transient noise simulations.

7.5 Detection efficiency

The maximum ToT value due to an input charge of 100 fC is $\approx$ 5 μs. During this time, called *dead-time*, the signals due to other particles are not processed by the ToT stage. It is useful to estimate the probability to lose signals because of the dead-time. The statistical distribution of events in time follows a Poisson distribution:

$$P(n) = \frac{(r\Delta t)^n e^{-r\Delta t}}{n!}$$

with r frequency of the signals, Δt dead-time, n number of occurrences of an event, the probability of which is given by the distribution. The maximum rate estimated for each strip is $\approx 10\ kHz$.
The probability to have no events after the first one is given by:

$$P(0) = \frac{(0.05)^0 e^{-0.05}}{0!} \approx 0.9512$$

The probability to have more events after the first one is given by:

$$P(n > 0) = 1 - P(0) \approx 0.0488$$

There is a 4.88% probability to have more particles, which will not be processed, after the first one. Using more stages in a time-interleaved configuration improves the detection efficiency, reducing the probability to not process signals coming during the dead-time. Supposing to have only two ToT stages working in a time-interleaved configuration, if there is only one particle after the first one, it will be processed by the second ToT stage. The probability to have more particles after the second one is given by:

$$P(n > 1) = 1 - P(0) - P(1) \approx 0.0012$$

Since the probability is only 1.2‰, it is not necessary another stage working in a time-interleaved configuration.

Conclusions

The innovation of PANDA is due to the high luminosity of the incident antiproton beam and consequently to the high number of the events recorded by the detector. Furthermore, PANDA will use a triggerless DAQ. The events of interest will not be selected by a specific signal (*trigger*) but the row data will be processed on-line by a farm of FPGA. This will allow a more flexible operation, which is important in an experiment looking at many different physics channels. The large number of events requires high granularity semiconductor detectors, pixel and strip, surrounding the interaction point. The front-end electronics has to process large amount of data, consuming less power as possible . The Time over Threshold (ToT) technique, used in the front-end chip of the pixel detectors represents a good way to obtain an accurate information about the energy value of the hitting particle with a low power consumption. The implementation of a front-end chip for the strip detectors using the same technique and, consequently, the same readout electronic after the front-end, allows to reduce the development time, the number of device components and the costs of the overall electronic system. The production of a new chip for particle detectors requires accurate preliminary studies of the circuit design, numerous schematic simulations and laboratory tests: the typical man power required for a mid-complexity chip is 5 to 10 man-years.

During this thesis, the design and the simulations of the most critical blocks of the circuit have been done. The first block of the processing chain amplifies the signals coming from the strip detector and the second one allows the use of the ToT technique. During the design, the addition of an intermediate stage (a current buffer) and several modifications of the stages were necessary to obtain the desired results. Several aspects related to the optimization of the performance of the circuit have been studied: the relation

between the ToT and the shape of the current input signal, the optimization of the noise figure and the limits of the linearity between the input charge and the ToT.
These are the performance achieved for the circuit: power consumption lower than $\approx 800\ \mu W$ per channel for a power supply of $1.2\ V$, high dynamic range (up to $100\ fC$), minimum detectable charge of $\approx 1.5\ fC$ and ENC of ≈ 1000 e^- for a detector capacitance of $20\ pF$. The circuit has been designed in a $0.13\ \mu m$ CMOS technology.
Two issues need to be addressed before the circuit can be sent for fabrication. The first is minimizing the impact of the relatively long dead-time of the ToT stage on the efficiency of the system. This can be solved by using more stages working in a time-interleaved configuration. The critical point here will be the proper management of the switching between the different ToT units.
The second point is to implement a circuit which processes signals of both polarities: this aspect is critical since double sided detectors will be used in PANDA. In addition, such a feature will give to the chip more flexibility and will make it easier to re-use it in different applications. This is an important point since the prototyping cost of custom microelectronics circuits increases significantly with the reduction of the feature size of the process. The dual-polarity mode has already been succesfully implemented in the chip for the pixels and we don't expect particular problems in extending it to the strip case.
The key conclusion of this work is that no show-stopper has been found in adapting to the strips the front-end architecture of the pixels and that a unified read-out approach for the whole microvertex detector should be possible, with a significant reduction in its development time and costs.

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