A new pixel readout chip for the CMS experiment at HL-LHC

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Background

- two major ***LHC upgrades*** referred to as ***Phase 1*** (after LS1) and ***Phase 2*** (after LS3)

- while ***SST*** replacement will be done once in the life of the experiment (LS3),
  SPT replacement is required ***more times due to radiation damages*** (~ mod 2yr LHC)

  - ***new*** vs. ***present*** (e.g. **PSI46_v1** → **PSI46_v2**)
  - present pixel sensors need replacement after ***100-200 fb $^{-1}$*** (LS1)
  - building a ***new pixel detector*** for Phase 1 (LS2, 3 layers → 4 layers)
  - replacing innermost layer(s) ***during Phase 1*** (2019) → ***Phase 1b***
  - building a further ***new pixel detector*** for Phase 2 (> 2021)

- Phase 1 2014 → 2016 pixel detector will be made of ***present pixel sensors*** and a modification of ***present* PSI46 *chip*** in VLSI 250 nm

Phase 1b idea

- LHC Phase 1 period has some free parameters
  - ***length*** is not yet clearly defined (max. up to 2021)
  - ***bunch spacing*** (50 ns vs. 25 ns) could bring to 2x PU and higher radiation damage
- Phase 1 pixel detector (i.e. PSI46_v2) will work fine up to **2 x 10^{34} $cm^{-2}s^{-1}$**
- proposal is to launch the development of a ***new generation of pixel detector***
  - ***new sensors*** with a much higher radiation tolerance (***3D***, ***planar***, ***diamond*****, ...**)
  - completely ***new readout chip***
- ***Phase 1b idea*** : we want to be ready to implement improvements ***already at the first opportunity***
  - new ROC, new sensor, same read-out links and controls as Phase 1
  - final targets are ***Phase 2 requirements***
  - opportunity of replacing L1 BPIX between LS2 and LS3 using this new pixel detector
- ***TDR Appendix: Evolution of Phase 1 pixel detector*** (under work)

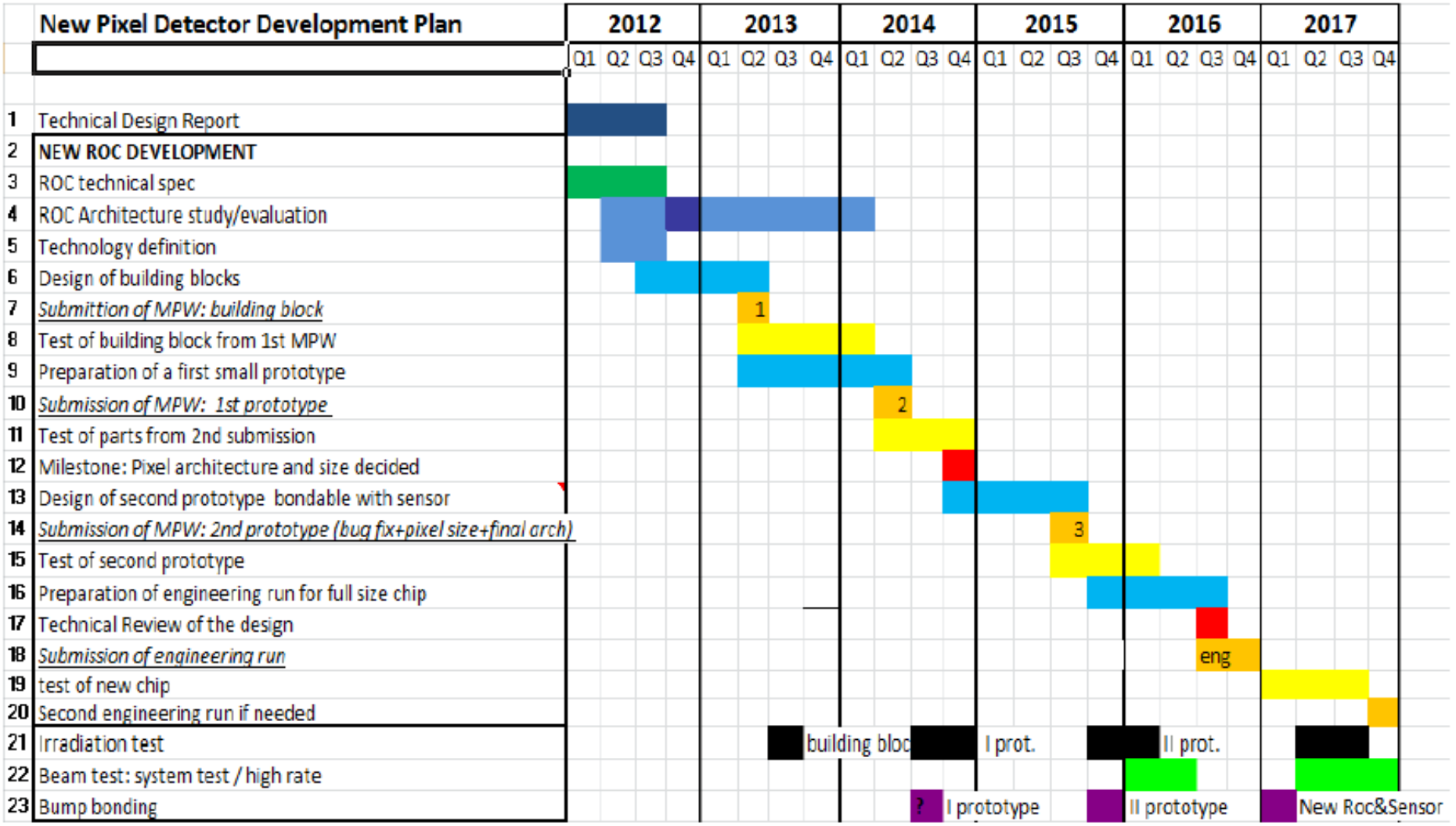
ASIC design group

- a strong collaboration between ***experienced groups on ASIC design*** is essential
- a first workshop has been held in Turin (21st-23st May)
  - *https://indico.cern.ch/confe renceDisplay.py?confId=191883*
  - discussion/choice of the ***technology***
  - ***basic specs and guide lines*** for the chip development
  - definition of a ***working model*** for the ASIC design
- at present interested groups are ***CERN***, ***FNAL***, ***Perugia***, ***Pisa*** (FE-I4 experience) and ***Turin***
- definition of a ***first 6 months work plan***

Guide lines for ASIC design

- VLSI technology: **TSMC 65 nm**
- pixel size: **< 50 μm x 100 μm**
- thickness: **200 μm**
- event rate: **2 GHz/cm^2**
- detection inefficiency: **< 1 %**
- L1 trigger latency: **6.4 μs**
- ***trigger-matching on the pixel region*** **(+ *self triggering ???*)**
- ***pixel sensor*** *???*
  - ***planar***, ***3D***, ***diamond*** *???*
  - ***sensor-independent*** analog read-out (***double polarity***)
  - input capacitance: **< 100 ÷ 200 fF**
  - leakage current compensation is required *???*
- very front-end: **CSA/shaper + 4 bit ToT (FE-I4 style) or 4 bit ADC**
- ***analog-oriented chip*** (50% analog, 50% digital)

ROC – 5 years development plan



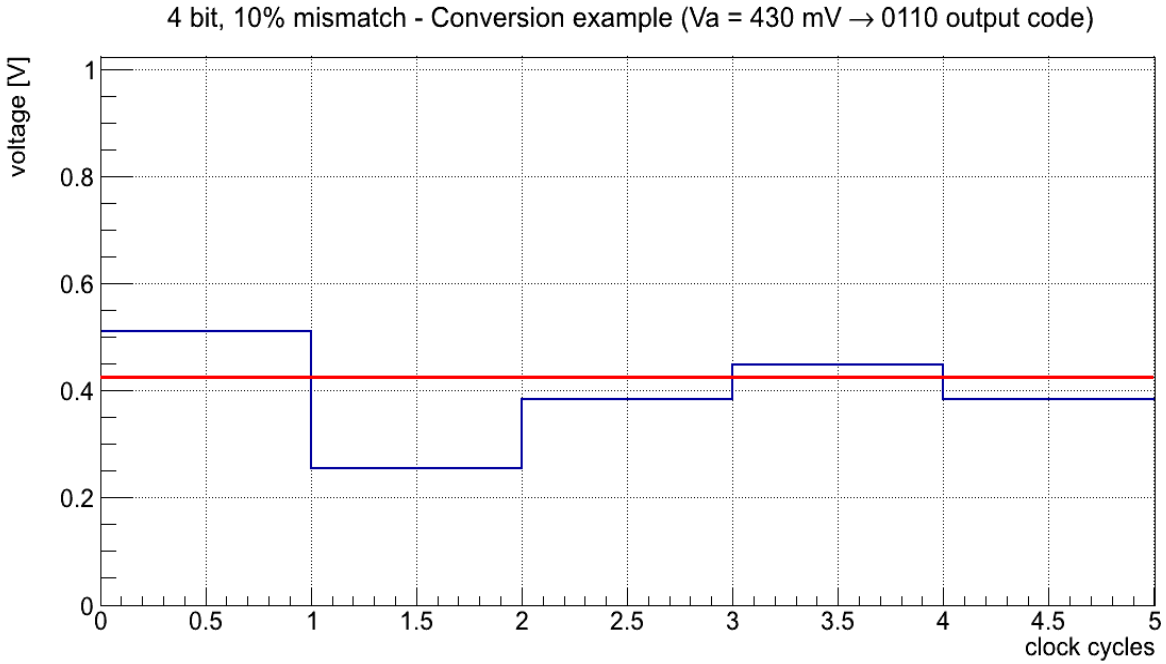
To do list for next 6 months

- accessing ***TSMC 65 nm libraries*** and ***design-kit***
  - OK analog
  - many digital libraries!
- define and set up a ***collaborative framework***
  - define common tools and computing environments
  - installation of ***ClioSoft*** SW in all sites
- starting ***simulations for analog parts*** (FNAL and Turin)
- getting started with ***basic architecture studies*** (CERN + Perugia)
  - ***System Verilog*** HDL language adopted
  - digital simulations oriented to ***trigger matching in the pixel region*** and ***Phase 2 specs***

Getting started with CR SAR ADCs

- Turin ***analog*** interests on an ***ADC-based FE*** **(CSA/shaper + ADC)**
  - ***in-pixel ADC*** (4 bit) for charge detection
  - ***chip-periphery ADCs*** (e.g. 10 bit) for slow control structures
- state of the art for medium speed (40-100 MHz) ADCs are ***CR SAR ADCs***
- CR SAR ADCs use ***binary-weighted capacitor arrays*** for the DAC
  - proper choice of DAC reference capacitance is fundamental
  - modeling ***capacitor array mismatch effects*** becomes important in order to understand component requirements
- high-level ***simulation software*** is under development (Python)

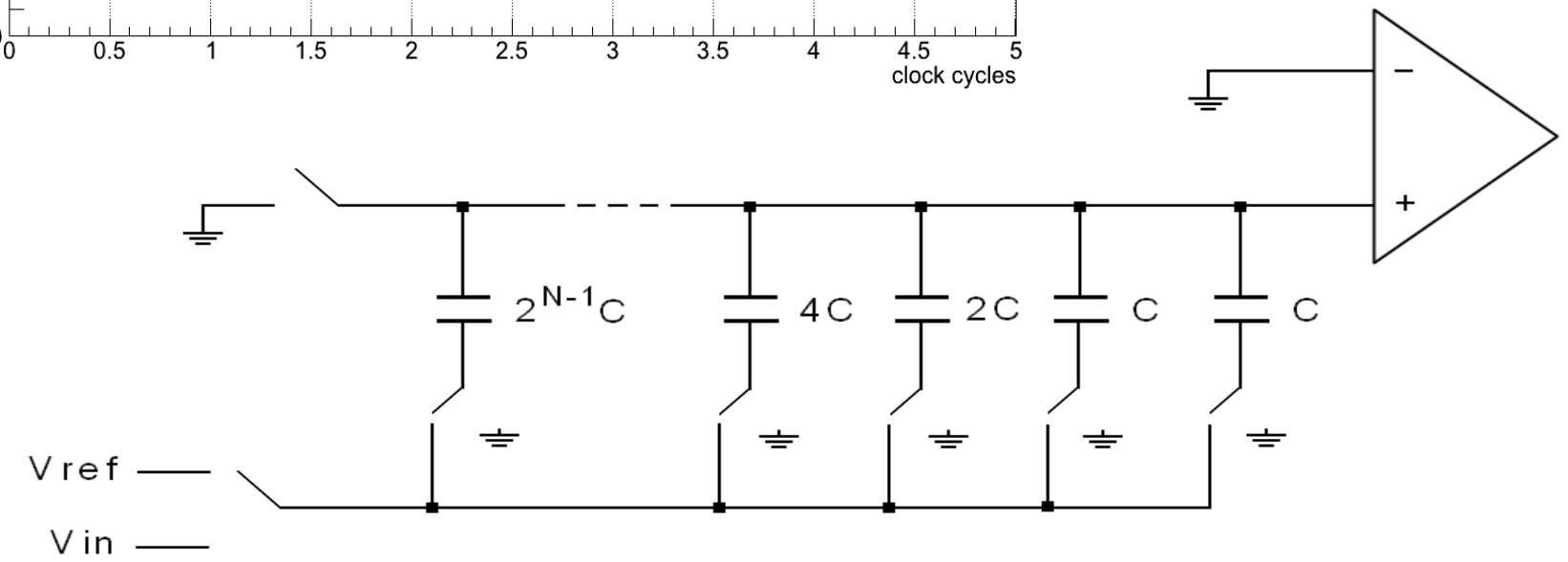
Single-ended CR SAR ADC example



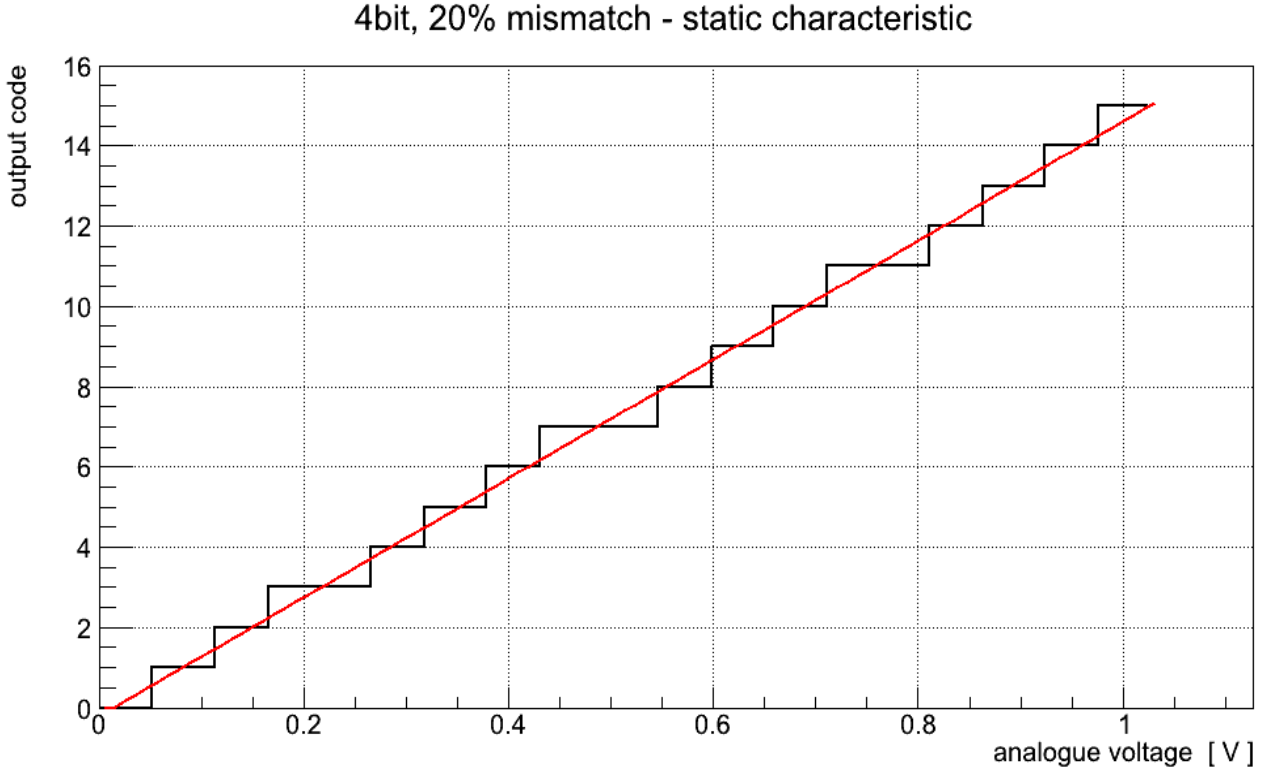
$$V_{DIGIT} = \frac{V_{ref}}{2^N} \sum_{i=0}^{N-1} B_i \, 2^i$$

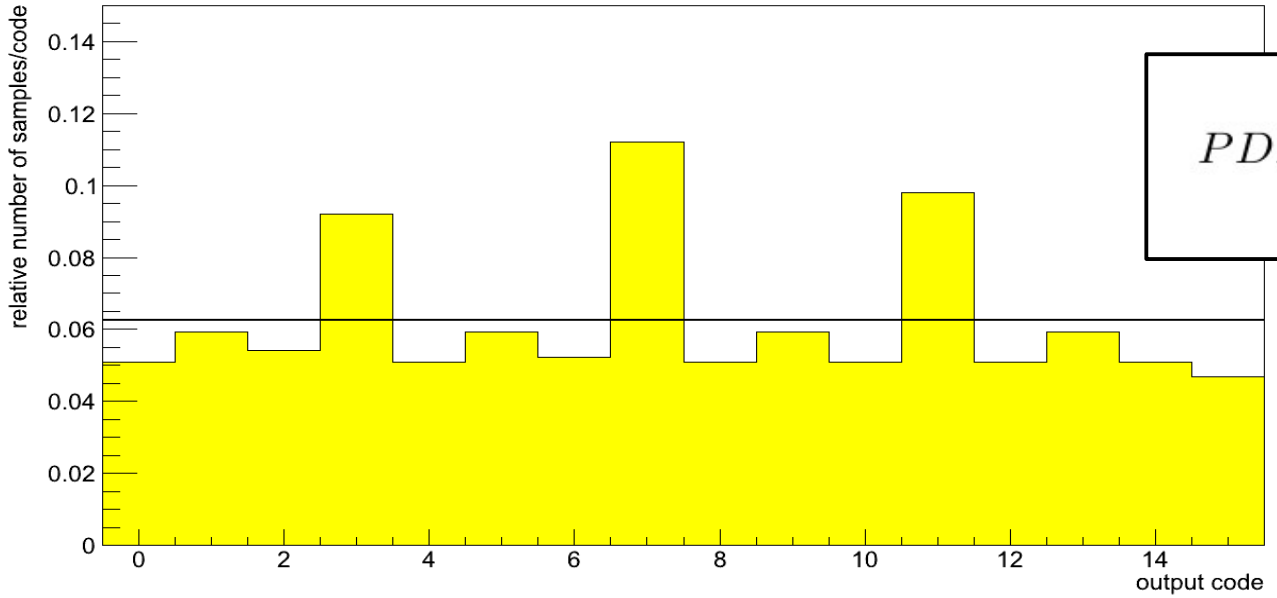
$$= V_{LSB} \left[\underbrace{B_{N-1}}_{MSB} 2^{N-1} + \ldots + \underbrace{B_0}_{LSB} 2^0 \right]$$

$$V_{DAC}(k) = -V_{in} + \underbrace{\left[\frac{1}{C_{TOT}} \sum_{i=N-1}^{N-k} B_i \, C_i \right]}_{MC} V_{ref}$$



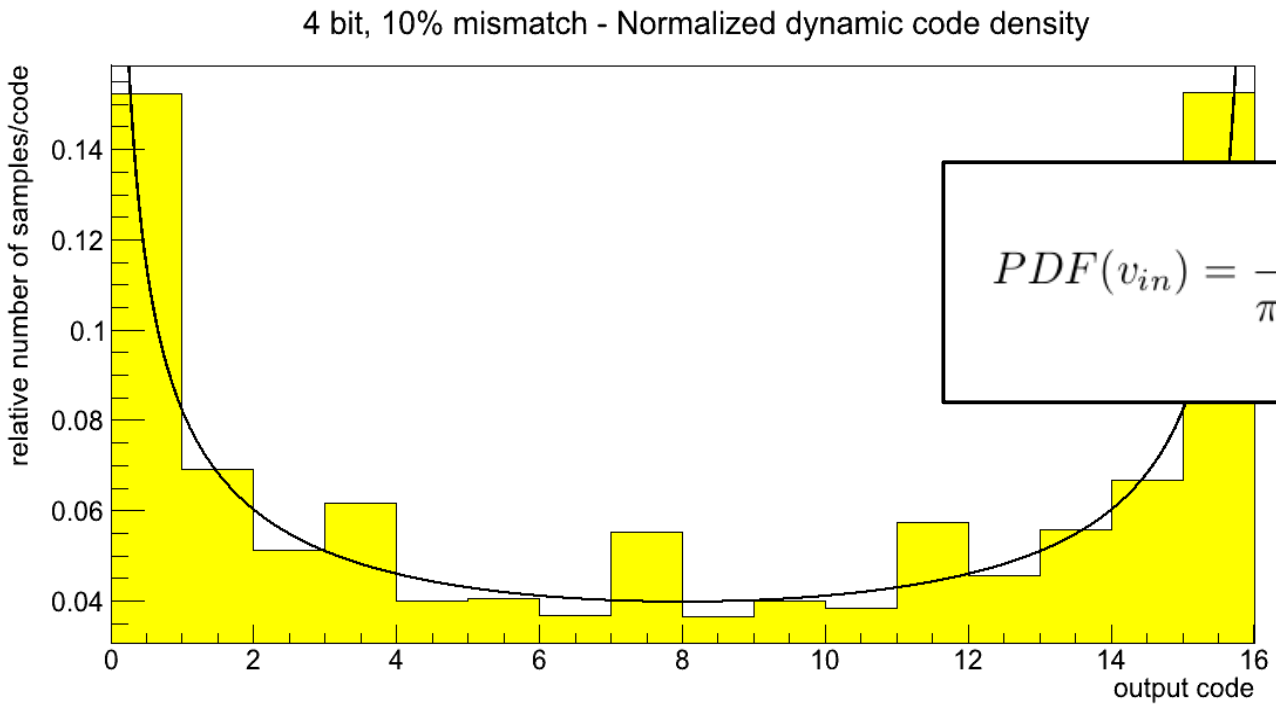
Static characteristic





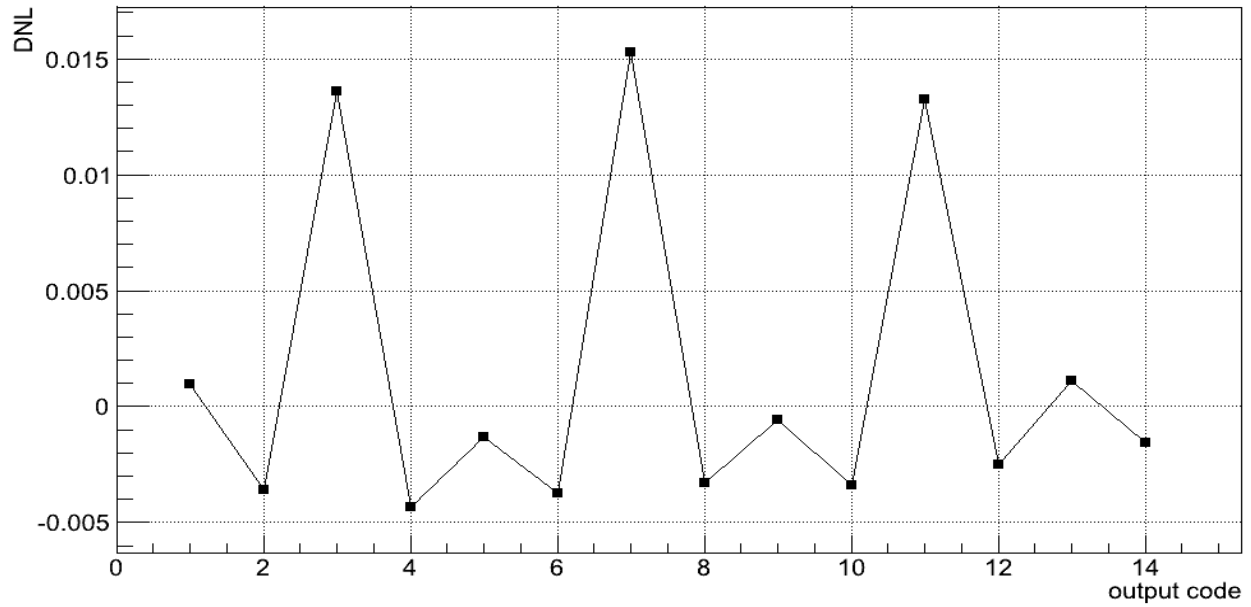
$$PDF(v_{in}) = \frac{1}{V_{ref}}$$

Dynamic characteristic



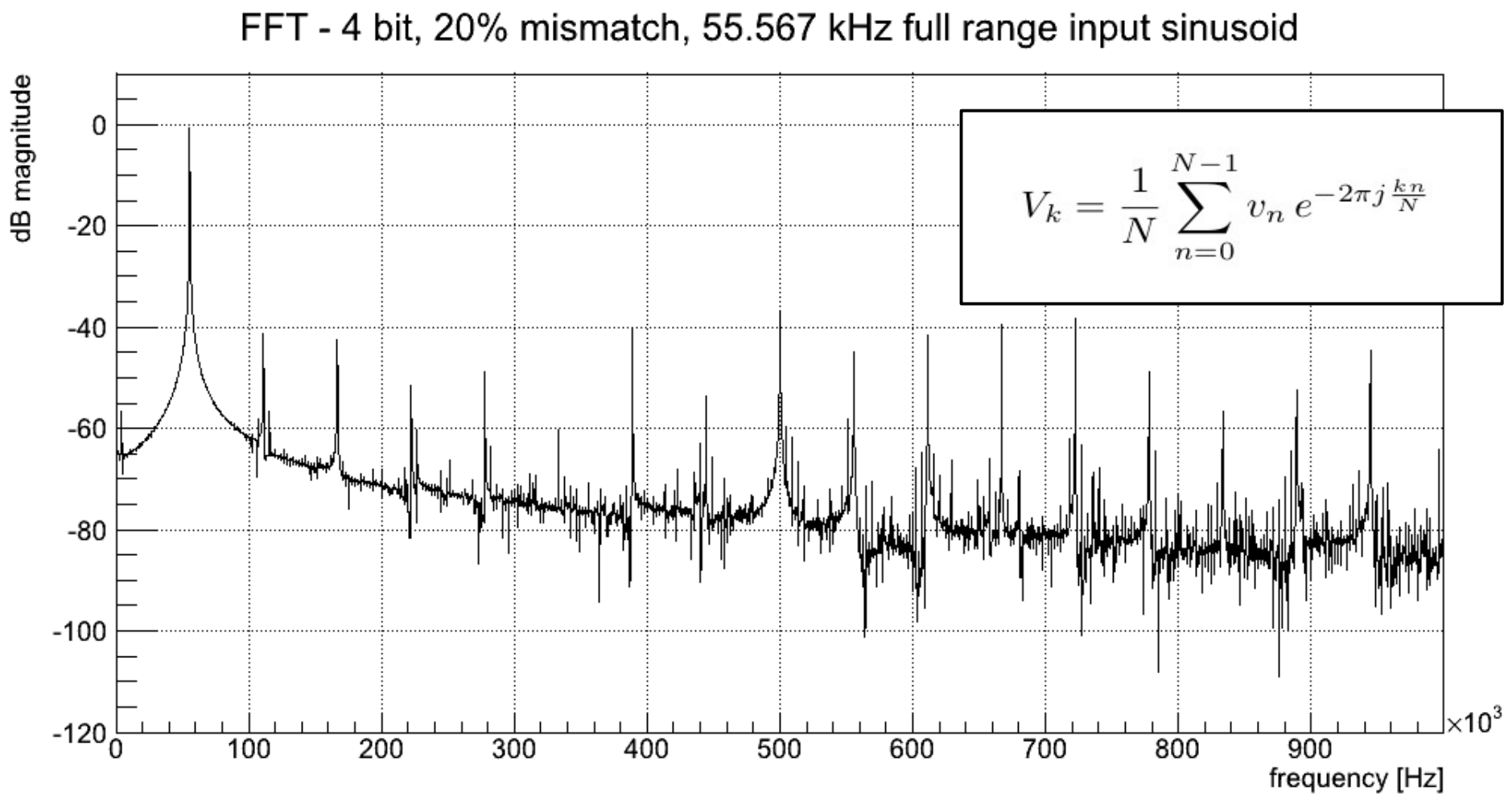
$$PDF(v_{in}) = \frac{1}{\pi\sqrt{A^2 - (v_{in} - V_o)^2}}$$

$$f_{sig} < \frac{f_s}{2} = f_{Nyquist}$$



DNL and ***INL*** can be immediately evaluated from the ***code density***

FTT test



THD, SINAD, SNHR, SFDR, ENOB extracted from the FFT

My next steps

- starting with the ***TSMC 65 nm technology***
  - first simulation results are required for next collaboration meeting (~ 5th July)
  - ***DISC building block*** schematic design, simulation, optimization
  - getting started with ***layouts*** in 65 nm (i.e. learning TSMC ***design rules*** from scratch)
- link my basic ADC simulations with more realistic ***process corners*** and ***cadence MCs***
- learning some ***VHDL*** and ***Verilog*** (if not time consuming)